Using signal attenuation and self-biasing to create translation circuits with fewer external components

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Each type of clock logic features a different common-mode voltage and swing level; see Table 1. Because of these differences, clock logic translation is necessary between the driver and receiver sides in system design. This article describes how to translate one type of differential clock logic into another by adding attenuation resistors and bias circuits between them, to attenuate the swing level and re-bias the common-mode for the input to the receiver.

First, however, before designing a logic translation circuit, a solid understanding is necessary of the input/output structures of each type of clock logic.

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LVPECL Input/Output Structure

Logic low-voltage, positive-referenced, emitter-coupled logic (LVPECL) originates from emitter-coupled logic (ECL), adopting a positive power supply. The LVPECL input is a current-switching differential pair with high input impedance; see Figure 1. The input common-mode voltage should be approximately V_{cc} – 1.3V to allow operating headroom, either from internal self-biasing or external biasing.

The LVPECL output consists of a differential pair amplifier that drives a pair of emitter followers (or open emitters) as shown in Figure 1. The output emitter followers should operate in the active region with DC at all times. The output pins OUT+ and OUT– are typically impedance-matched to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω). The proper termination for LVPECL output is 50Ω to V_{cc} – 2V and OUT+/OUT– will typically be V_{cc} – 1.3V, resulting in approximate DC flow of 14mA.

Another way to terminate LVPECL output is to apply 142Ω to GND, which provides a DC-biasing for LVPECL output and a DC path to GND. Because the LVPECL output common-mode is at V_{cc} – 1.3V, the DC-biasing resistor can be selected by assuming direct current of 14mA (R = V_{cc} – 1.3V/14mA), resulting in R = 142Ω (150Ω also works) for V_{cc} – 3.3V.

LVDS Input/Output Structure

Low-voltage differential signalling (LVDS) input requires a 100Ω termination resistor across the pins of IN+ and IN–, with a common-mode voltage of approximately 1.2V; see Figure 2. If the 100Ω termination is not included on the chip, it must be included on the printed circuit board (PCB).

The LVDS output driver consists of a 3.5mA current source that's connected to differential outputs through a switching network. The output pins of OUT+ and OUT– typically connect to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω) for impedance matching, terminated with a 100Ω resistor across the receiver inputs, resulting in 350mV swing for the LVDS logic.

CML Input/Output Structure

Most current-mode logic (CML) input structures have a 50Ω resistor to V_{cc} on-chip; see Figure 3. If not, one must be applied to V_{dd} on both inputs IN+ and IN– on the PCB.

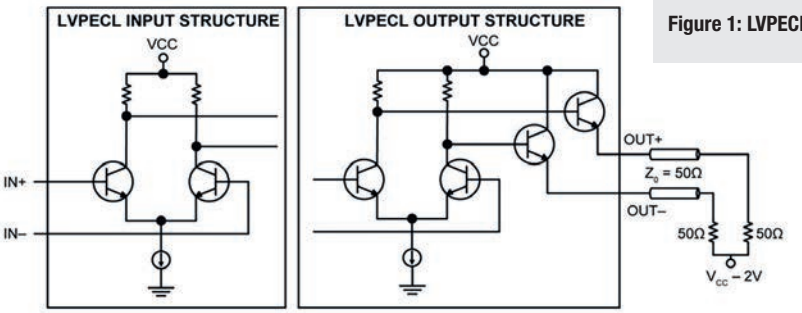

Figure 1: LVPECL input/output structure

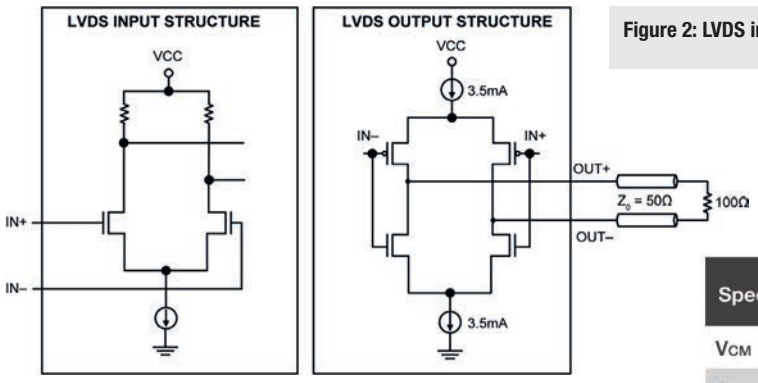

Figure 2: LVDS input/output structure

Specification	LVPECL	LVDS	CML Terminated (50Ω to Vcc)	HCSL
V_{CM}	Vcc – 1.4V	1.2V	Vcc – 0.2V	350 mV
V_{SWING_SE}	800 mV	325 mV	400 mV	700 mV
V_{OH}	Vcc – 1V	1.3625V	Vcc	700 mV
V_{OL}	Vcc – 1.8V	1.0375V	Vcc – 0.400V	0V
Reference	Vcc	Ground	Vcc	Ground

Table 1: Common-mode voltage and swing levels of different clock logic types

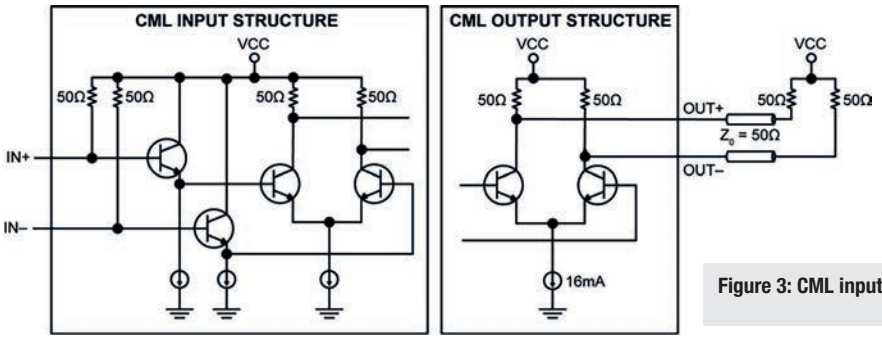

Figure 3: CML input/output structure

The input transistors are emitter followers driving a differential-pair amplifier. The CML output consists of a differential pair of common-emitter transistors with 50Ω collector resistors; see Figure 3. Outputs OUT+ and OUT– are typically connected to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω) for impedance matching.

The signal swings are provided by switching the current in a common-emitter differential bipolar junction transistor (BJT). Assuming the current source is 16mA (typical) and the CML output is loaded with a 50Ω resistor, which is a pull-up to V_{cc}, this will result in an output voltage swing from V_{cc} to V_{cc} – 0.4V with a common-mode voltage (V_{cc} – 0.2V).

HCSL Input/Output Structure

The high-speed current-steering logic (HCSL) input requires the single-ended swing of 700mV on both input pins of IN+ and IN– with a common-mode voltage of approximately 350mV; see Figure 4.

A typical HCSL driver is a differential logic with open-source outputs, where each of the output pins switches between 0 and 14mA. When one output pin is low (0), the other is high, driving 14mA. The output pins OUT+ and OUT– are typically connected to differential transmission lines (Z_0 = 100Ω) or a single-ended transmission line (Z_0 = 50Ω), which requires an external termination resistor (50Ω to GND), resulting in a 700mV swing level for HCSL input structures.

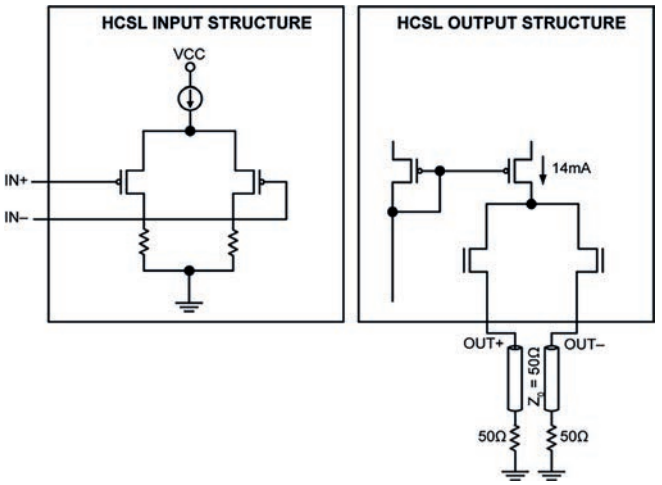

Figure 4: HCSL input/output structure

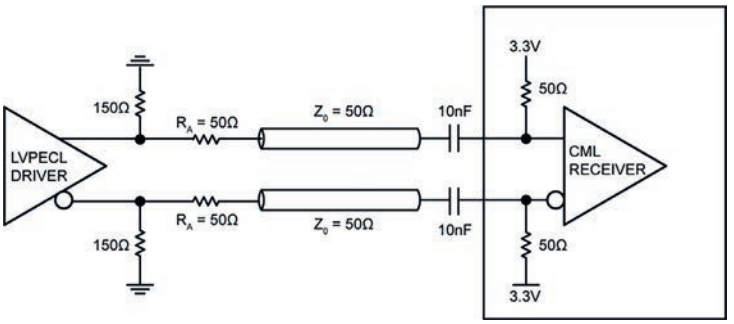

Figure 5: LVPECL-to-CML translation

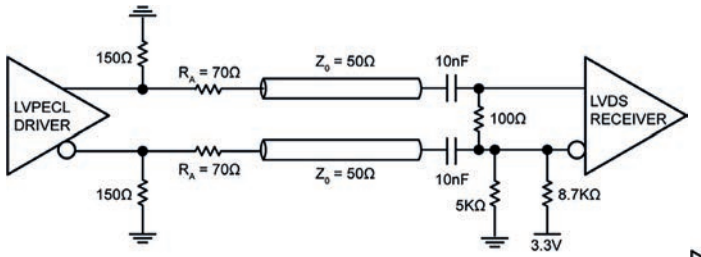

Figure 6: LVPECL-to-LVDS translation

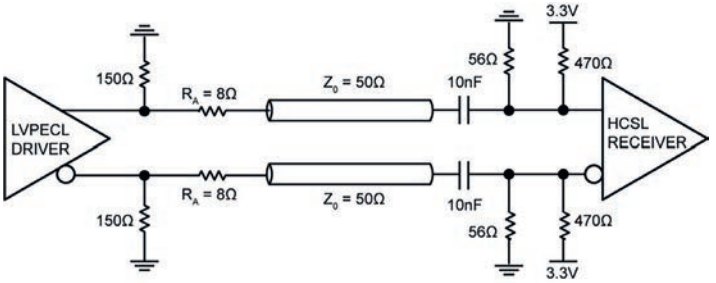

Figure 7: LVPECL-to-HCSL translation

Translation Examples

LVPECL-to-CML Translation

As shown in Figure 5, placing a 150Ω resistor to GND at the LVPECL driver output is essential for the open emitter to provide DC biasing as well as a DC path to GND. To attenuate the 800mV LVPECL swing to 400mV CML swing, place a 50Ω attenuating resistor (R_A) after the 150Ω resistor to attenuate half of the LVPECL swing level. Additionally, self-biasing inside the CML receiver input must be confirmed.

If the self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{cc} must be placed on the PCB for CML biasing and transmission line termination. Microchip's ultra-low-jitter crystal oscillators and clock generators (i.e. MX55, MX57, SM802xxx, SM803xxx, MX85xxx) can provide < 0.3PS RMS phase jitter with any type output logic, except CML. The translation circuit shown in Figure 5 makes it easy to achieve CML output from LVPECL logic.

LVPECL-to-LVDS Translation

Placing a 150Ω resistor to GND at the LVPECL driver output is essential for the open emitter to provide DC biasing, as well as a DC path to GND; see Figure 6. To attenuate the 800mV LVPECL swing to a 325mV LVDS swing, a 70Ω attenuating resistor must be applied after the 150Ω resistor. A 10nF AC-coupled capacitor should be placed in front of the LVDS receiver to block DC level coming from the LVPECL driver.

Following the AC-coupled capacitor, re-biasing is required for the LVDS input. This can be done by placing an 8.7kΩ resistor to 3.3V and 5kΩ resistor to GND to achieve a 1.2V DC level for the input common-mode of the LVDS receiver.

If the LVDS receiver already has a 100Ω resistor integrated across the differential input pins, the external 100Ω resistor is not required. This LVPECL-to-LVDS translation circuit is very useful in designs that use Microchip's LVPECL fan-out buffers (i.e. SY89831) but require LVDS logic on some outputs.

LVPECL-to-HCSL Translation

As shown in Figure 7, placing a 150Ω resistor to GND at the LVPECL driver output is essential for the open emitter to provide DC biasing and a DC path to GND. To attenuate an 800mV LVPECL swing to a 700mV HCSL swing, an attenuating resistor (R_A = 8Ω) must be placed after the 150Ω resistor. A 10nF AC-coupled capacitor should be placed in front of the HCSL receiver to block DC level coming from the LVPECL driver.

After the AC-coupled capacitor is placed, re-biasing is required for the HCSL input. This can be done by placing 470Ω resistor to

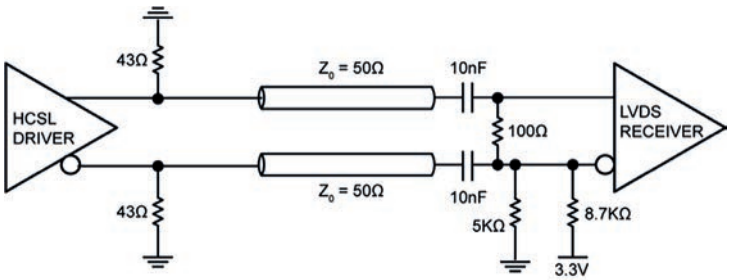

Figure 8: HCSL-to-LVDS translation

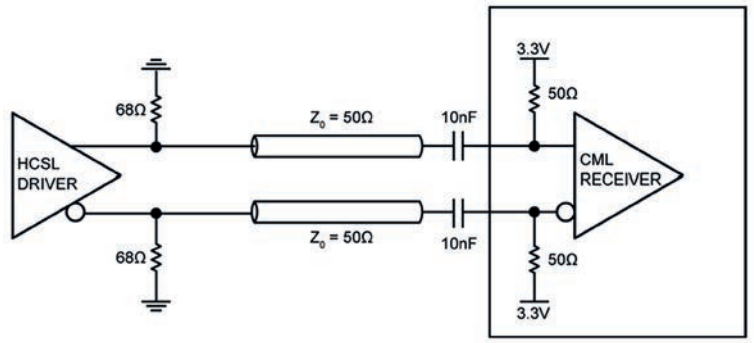

Figure 9: HCSL-to-CML translation

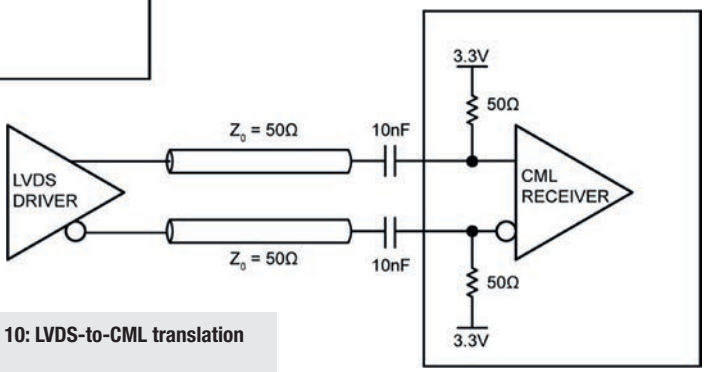

Figure 10: LVDS-to-CML translation

3.3V and 56Ω resistor to GND for a 350mV DC level for the input common-mode of the HCSL receiver.

This LVPECL-to-HCSL translation circuit is very useful in designs that use Microchip's LVPECL fan-out buffers (i.e. SY89831) but require HCSL logic on some outputs.

HCSL-to-LVDS Translation

In Figure 8, each HCSL output pins switches between 0 and 14mA. When one output pin is low (0), the other is high (driving 14mA). Equivalent loading for the HCSL driver is 48Ω parallel to 50Ω, which equates to 23.11Ω. Swing level at the LVDS input is 14mA × 23.11Ω = 323mV.

A 10nF AC-coupled capacitor should be placed in front of each LVDS receiver to block DC coming from the HCSL driver. After the AC-coupled capacitor is placed, re-biasing is required for the LVDS input, done by placing an 8.7kΩ resistor to 3.3V and 5kΩ resistor to GND to achieve 1.2V DC for the common-mode input of the LVDS receiver. If the LVDS receiver already has a 100Ω resistor integrated across the differential input pins, the external 100Ω resistor is not required.

This HCSL-to-LVDS translation circuit is very helpful for designs that use Microchip's HCSL fan-out buffers (i.e. SY75576L, SY75578L) but require LVDS logic on some outputs.

HCSL-to-CML Translation

In Figure 9, each of the HCSL output pins switches between 0 and 14mA. When one output pin is low (0), the other is high (driving 14mA). The equivalent loading for the HCSL driver is 68Ω parallel to 50Ω, which equates to 28.81Ω. The swing level on the CML input is 14mA × 28.81Ω = 403mV.

A 10nF AC-coupled capacitor should be placed in front of the CML receiver to block DC level coming from the HCSL driver. Additionally, self-biasing inside the CML receiver input must be confirmed. If the self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{cc} must be placed on the PCB for CML biasing and transmission line termination.

LVDS-to-CML Translation

The LVDS output drives a ±3.5mA current through the termination of a 100Ω resistor, resulting in a 350mV swing level in front of the CML receiver; see Figure 10. Confirmation that the CML receivers are capable of receiving a 350mV swing is required because the standard swing of CML is 400mV. Additionally, self-biasing inside the CML receiver input must also be confirmed.

If self-biasing at the input of CML is not present, a 50Ω termination resistor to V_{cc} must be placed on the PCB for CML biasing and transmission line termination. EW