Cascade multi-level inverter design

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Inverter design continues to be an important study in the field of power electronics. One of the most popular inverter designs is the multi-level topology. Multi-level inverters are widely used in high-power and high-efficiency alternative energy sources. Their advantages include low harmonics in the output voltage, low switching frequencies and high efficiencies, compared to conventional inverter designs. Because of these benefits, multilevel inverters are increasingly found in all-electric vehicles (EV) and hybrid-electric vehicle (HEV) motor drives, too.

Indispensable

Inverters have become an indispensable element in many industrial applications today, widely used in the control of various engine types and power devices, but also in battery-powered systems, fuel and solar cells, wind-turbines/micro-turbines, and more.

Their widespread use and the goal to make them even more efficient has led researchers to study them on an ongoing basis, one of which is to obtain better quality output voltage and load current by keeping the number of switches at a minimum. This research has led to many new inverter structures and switching techniques. In multi-level inverters, as the number of levels increases, the change in output voltage becomes similar to that of a sine signal, which helps achieve high-quality current and voltage.

Alternating current (AC) power supplies must produce high power and low harmonics whether feeding a load or a network; it is desirable that the inverter's output voltage waveform be sinusoidal since harmonic levels are then low, achieved with multi-level topologies.

Multi-level inverter topologies can be mainly classified into three groups: diode-clamped, flying-capacitor and cascaded, although there are others, such as cascaded transformers and cascaded half H-bridge inverters.

Since multi-level inverters have graduated voltage levels, dv/dt voltage stress on the switching elements is low and the output voltage high. Low efficiency and electromagnetic interference problems arise due to the high switching frequency of the pulse width ratio (PWR) inverter and the stress-imposed high dv/dt. As a result, an output filter must be used to reduce the high switching frequency components and to obtain sinusoidal output voltage in series. Here, multi-level inverters compete with classic PWR inverters.

New Multi-Level Inverter Prototype

The principle diagram of a multi-level inverter prototype is shown in Figure 1. The 11-level inverter basically comprises two modules: levels and H-bridge. Using a phase inverter in the design helps expand the structure, since by increasing the number of level modules, the number of output voltage levels can easily be increased.

The level module (Figure 2) consists of one switching element and one direct current (DC) source. The voltage of the source in each level module is thus:

$$2^{(k-1)}.V_d \qquad (1)$$

where k = 1, 2, 3 ... m, and m is the number of level modules found in single-phase inverters, with V_d being the voltage of the first level:

$$V_d = \frac{2.V_{max}}{n_{fn}-1} \qquad (2)$$

Here, V_{max} is the maximum value of the voltage change in a phase and n_{fn} is the number of levels of phase-neutral voltage.

The structure of the H-bridge module (Figure 3) is the same as that of a conventional H-bridge inverter. The H-bridge module is fixed in the inverter system; Figure 1 shows an H-bridge module in each phase.

We've named the multi-level inverter structure in this work

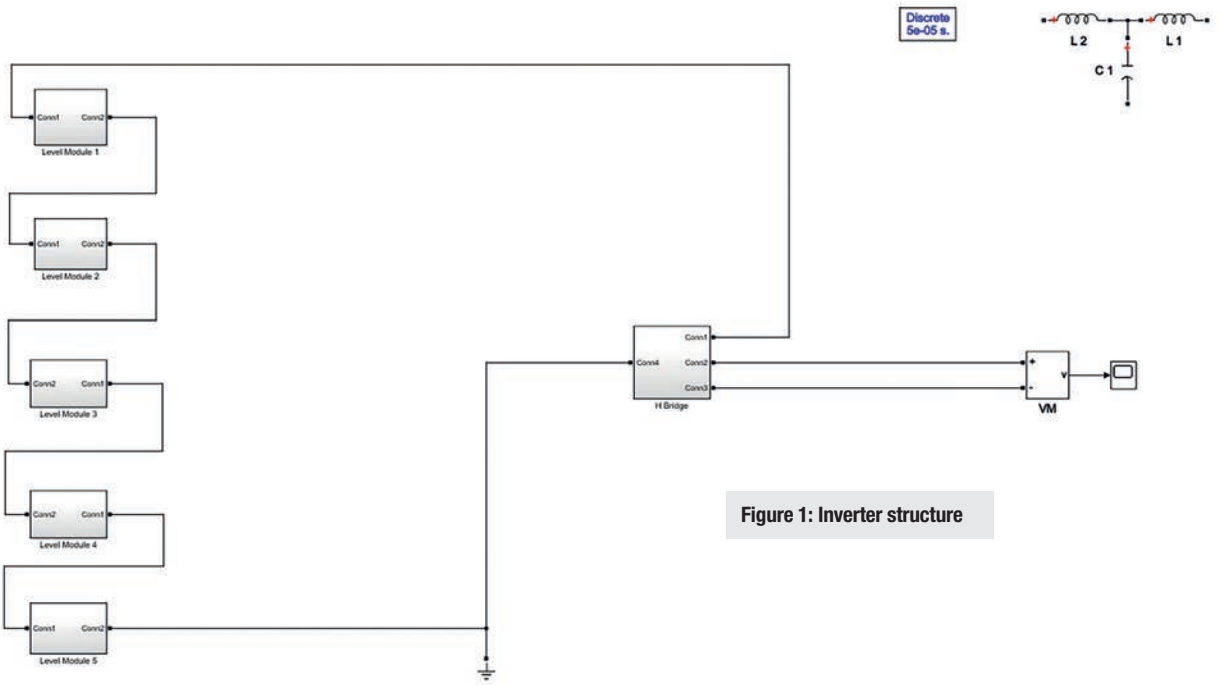

Figure 1: Inverter structure

"binary cascade" because the source voltage values change in multiples of two, like in the binary numbering system. Thanks to this structure, the number of auxiliary switching elements and resources can easily be increased to a different number of levels. Compared to classical multi-level inverters, the increase in the number of switching elements is lower than the increase in level numbers.

There is a correlation between the numbers of level modules, switching elements and output voltage; see Equations 3 and 4:

$$n_{fn} = 2^{(m+1)} - 1 \qquad (3)$$

$$r_{1\varphi} = 2m + 4 \qquad (4)$$

where n_{fn} is the number of levels of phase-neutral voltage, and $r_{1\varphi}$ represents the number of switching elements of a single-phase inverter.

Measurements

We built an 11-level inverter with a switching frequency of 20kHz, L = 0.01H and R = $2.10^{-6}\Omega$; see the voltage graph in Figure 4.

We then simulated our design and carried out a series of experiments, which confirmed that this design significantly reduces dv/dt stress on the switching elements and produces a good output voltage. EW

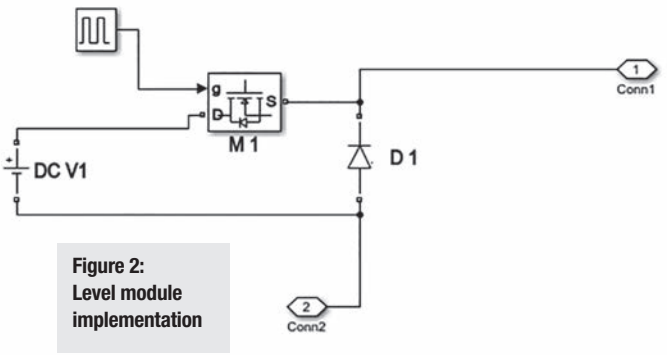

Figure 2: Level module implementation

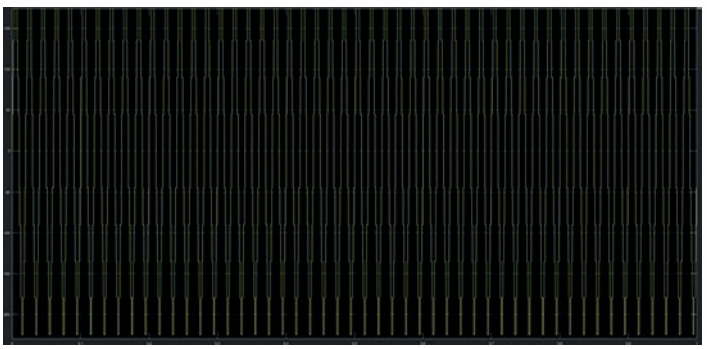

Figure 4: Simulation results

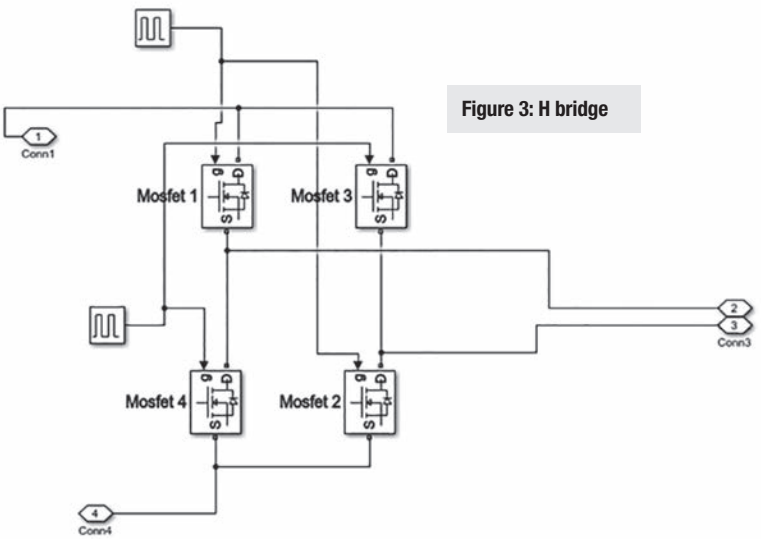

Figure 3: H bridge