Ultra-wideband calibration-free 6-bit 4GSps folding-interpolating ADC

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In high-speed optical communication receivers, high-speed analogue-to-digital converters (ADCs) provide sample information for use with DSP-based signal equalisation. High-speed ADCs are also needed for spectral identification of high-speed signals and can provide the interface to an on-chip Fast Fourier Transform (FFT) engine. But, to improve the performance of such systems, high sampling rate and medium-resolution ADCs are being pursued.

Ultra-Wideband ADCs

Ultra-wideband ADCs are required in a wide range of receiver applications, including digital radar receivers (DRRs) and ultra-wide bandwidth (UWB) communication. Figure 1 shows an example DDR system, where the antenna signal is directly digitised for further processing, after its conditioning. It can be employed in military surveillance, airborne early warning and target recognition. In these situations, low latency and no idle time for calibration are required of the ADC's analogue core. In some high-speed ADC designs with GHz sampling frequency, there's need for large latency because of the architecture's multiple pipeline stages. Dedicated time for calibration is necessary, since the CMOS technology's matching properties are poor.

In this architecture, the output of the track-and-hold circuit is applied to the input of four folding amplifiers, where it is compared to reference voltages generated by a resistor ladder

In addition to wide instantaneous bandwidth, accommodating high intermediate frequencies (IF) offers significant system advantages by reducing or eliminating costly RF down-conversion circuitry. Existing silicon-based designs with resolution higher than 6-bit and 1.33GSps sample rate use flash memory for high-speed operation. However, these designs do not successfully sustain their baseband effective number of bits (ENOB) performance at input frequencies higher than the sampling rate.

Here, we describe a calibration-free 6-bit 4GSps folding-interpolating monolithic ADC, fabricated in advanced SiGe BiCMOS technology. We use the folding-interpolating architecture because it consumes less power and occupies less space than its flash counterpart while sacrificing less speed and latency.

The matching properties of hetero-junction bipolar transistors (HBTs) are about ten times better than that of metal oxide semiconductor field effect transistors (MOSFETs). By using an on-chip highly-linear track-and-hold amplifier (THA), the architecture can sample input frequencies up to 5.5GHz with 5.45 ENOB performance, which is close to the ideal value of 6.

Block Diagram

The ADC's block diagram is shown in Figure 2. The folding-interpolating architecture exhibits flash-like speed of operation but requires fewer preamplifiers and comparators than the traditional flash approach. An equally important benefit of folding-interpolating is the significant reduction in capacitive loading on the analogue signal path, and the resultant contribution toward increased sampling rate.

In this architecture, the output of the track-and-hold circuit is applied to the input of four folding amplifiers, where it is compared to reference voltages generated by a resistor ladder. The output of the folding amplifiers is a set of phase-shifted sinusoid-like signals, which, in turn, are applied to an array of comparators. The outputs of the comparators are eventually converted to binary code by a digital encoder, to produce four least significant bits (LSBs). The two most significant bits (MSBs) are produced by a coarse quantiser.

To further reduce the die area and power dissipation, D_4 is extracted directly from comparator #16, and the coarse quantiser is only used to generate D_5. A bit-synchronisation circuit is included in the coarse quantiser to align the LSBs and MSBs.

The folding-interpolating architecture is highly applicable to high-resolution converters that need large analogue bandwidth. Figure 2 shows that each folding amplifier has five inputs, and each input consists of a pair of differential signals.

Circuit Design

An input THA improves the dynamic performance of an ADC. For gigahertz sampling rate operation, THA becomes essential to achieve the desired converter resolution with wide input bandwidth. By holding the analogue sample static during digitisation, the THA largely removes errors due to skews in the clock delivery of a large number of comparators, limited input bandwidth prior to latch regeneration, signal-dependent dynamic nonlinearity and aperture jitter.

As seen in Figure 3, The THA consists of an emitter-follower preamp driving a Schottky diode bridge, followed by an emitter-follower post-amplifier. The SiGe Schottky diodes used in this work provide

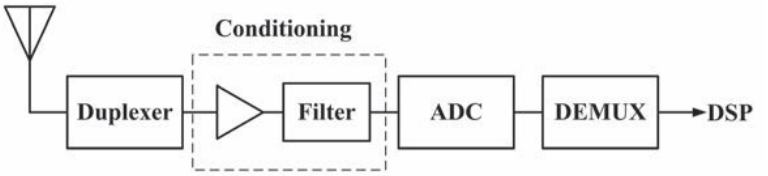

Figure 1: DRR system

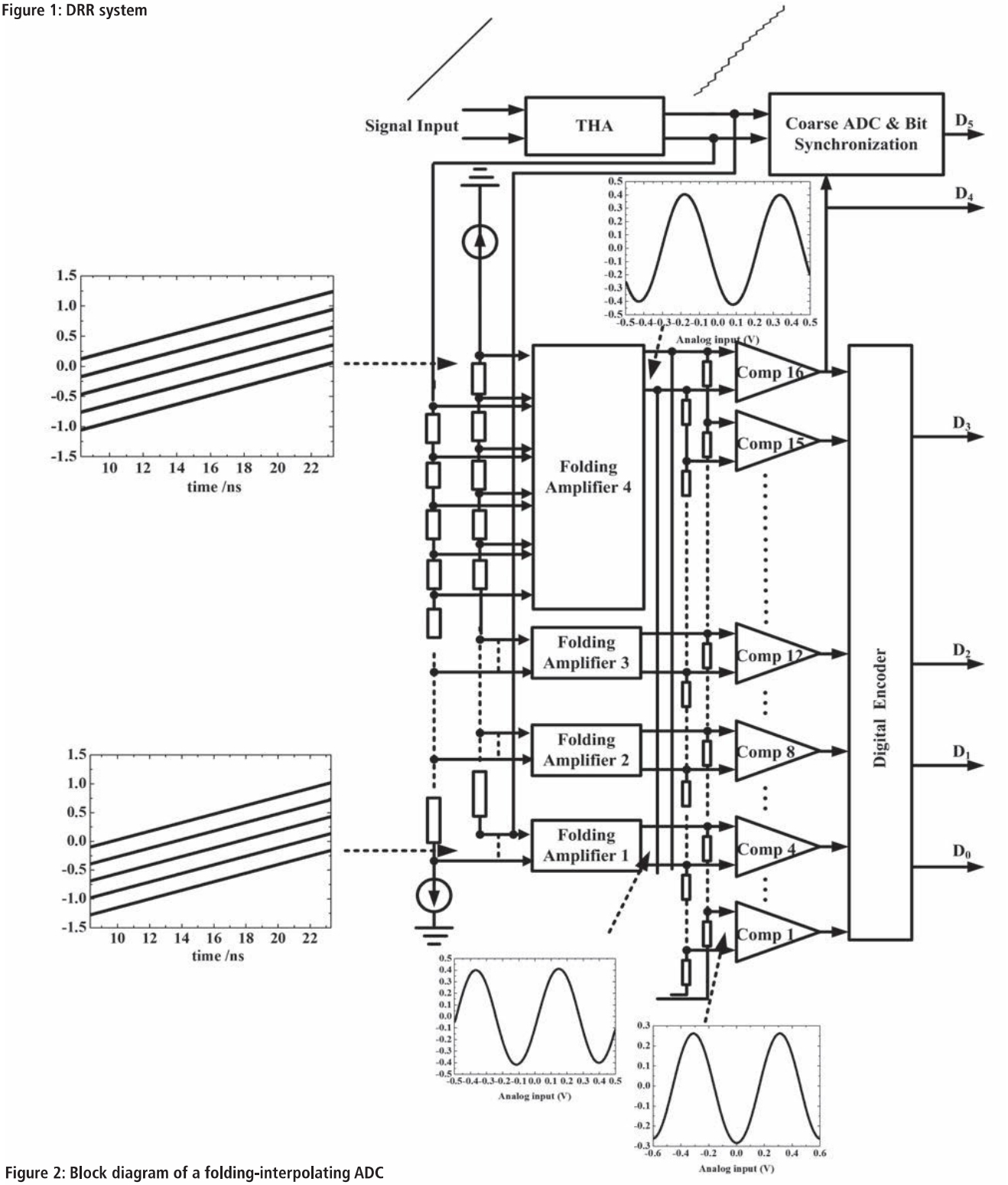

Figure 2: Block diagram of a folding-interpolating ADC

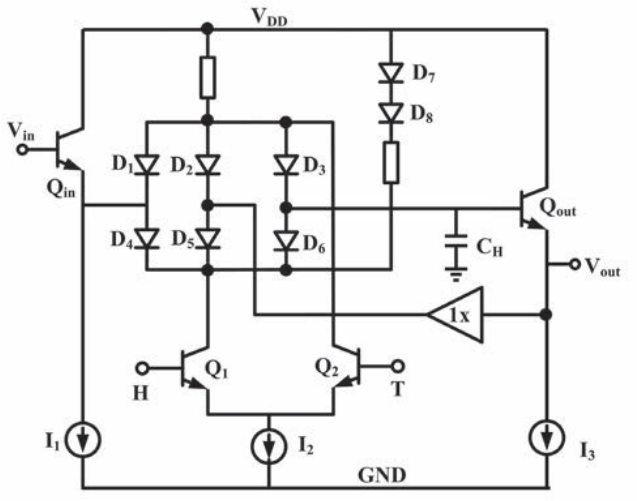

Figure 3: Simplified track-and-hold amplifier circuit

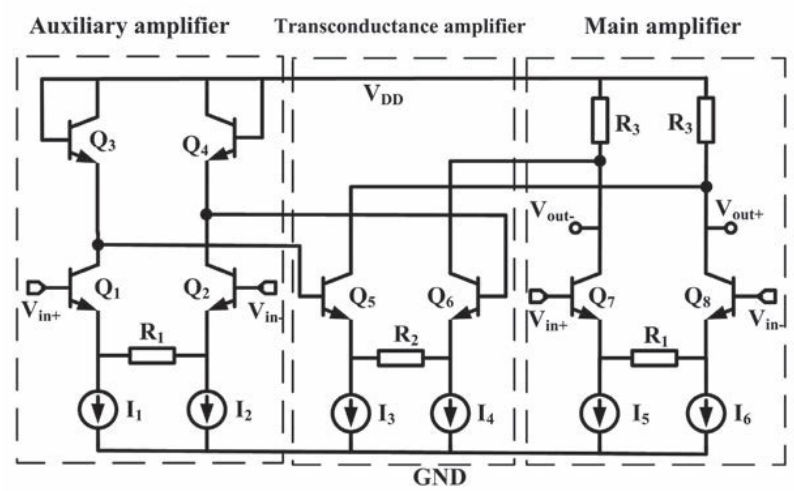

Figure 4: Highly linear input buffer

true majority-carrier device performance and are key to achieving sustained ADC performance at very high frequencies. The centre tap of the diode bridge is bootstrapped to reduce hold-pedestal distortion.

To achieve high resolution at the ADC output, we used a highly linear input buffer; see Figure 4. It consists of auxiliary, transconductance and main amplifiers. The auxiliary and main amplifiers together provide linearisation effect better than that of the traditional common emitter amplifier with resistor load and a wide input voltage swing.

The auxiliary amplifier loads consist of the Q_3 and Q_4 transistors that produce output voltages to drive the transconductance amplifier formed of Q_5, Q_6 and emitter resistor R_2. The transconductance amplifier is characterised by $G_m=1/R_2$ and is connected to the load resistor R_3 of the main amplifier.

In the input buffer, R_1 is set to be $2R_3$ for unity gain. Resistor R_2 is chosen to be lower than R_1 to cancel out the systematic gain error of the transconductance amplifier. As a result, the differential diode voltages are summed up with the main amplifier outputs at nodes V_{out+} and V_{out-}. Thus, distortion is compensated without requiring series connections of diodes and load resistors with the main amplifier's collector loads.

Folding Amplifiers

The basic function performed by folding amplifiers is the conversion of input signals into sinusoid-like output signals; see the topology of the folding amplifier used in our work in Figure 5.

Each folding amplifier with a folding factor of five generates four zero-crossings within the ADC's full-scale range (the one out-of-range folding factor minimises threshold distortion due to end effect). The folding amplifier is designed to be fully differential, which cancels any common-mode noise. Four folding amplifiers generate the required 16 zero-crossings.

Interpolation is implemented using 4× resistive-string networks because of their simplicity and power efficiency, and, also, because using resistor averaging improves the ADC's linearity. In the folding architecture, the number of folding amplifiers is equal to the number of reference levels in the fine quantiser. However, this problem can be solved by creating only a small number of folding signals and deriving the other folding signals by resistive interpolation between the outputs of two adjacent signals.

The circuit diagram for interpolation between two folding amplifier outputs is shown in Figure 6. Here, the folding signals of V_1, V_2 and V_3 can be obtained directly from V_0 and V_4, which are the outputs of two consecutive folding amplifiers.

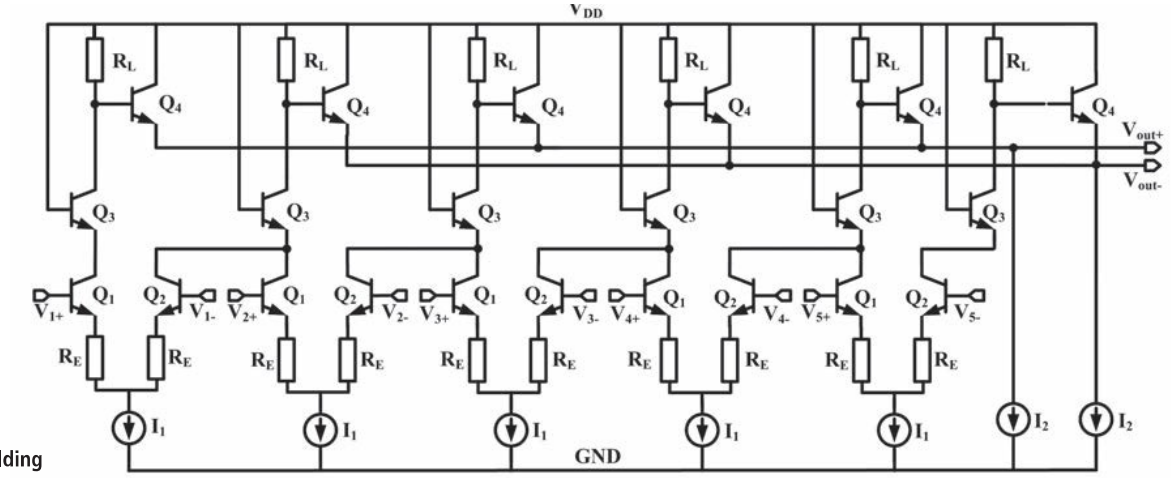

Figure 5: Folding amplifier

$$V_1 = 3V_0/4 + V_4/4 \quad (1a)$$

$$V_2 = V_0/2 + V_4/2 \quad (1b)$$

$$V_3 = V_0/4 + 3V_4/4 \quad (1c)$$

The transfer function of the folding-interpolating circuits is shown in Figure 7. Observe that 64 thresholds are within the analogue input full-scale range to provide the overall 6-bit resolution. In the figure, curves 1, 2, 3 and 4 represent the output signals of the folding amplifiers 1, 2, 3 and 4, respectively.

Complete Comparator Circuit

The complete comparator circuit used in our work is shown in Figure 8. It consists of a preamplifier and two cascaded differential comparators in a master-slave configuration. The preamplifier is designed in a differential amplifier configuration to achieve the required gain and bandwidth.

The master-slave comparators are identical and driven by complementary clocks. When the master comparator goes into track mode, the slave comparator is in latch mode and holds its digital value. Alternatively, when the master comparator goes into latch mode, the slave comparator is in track mode and tracks the latched signal of the master comparator. This ensures that a fully digital output is obtained at the output of the comparator. Buffers (emitter followers Q_3) are used to level shift the signals between the master and slave comparators and the preamplifier.

Digital Encoder and Coarse Quantiser

In the fine quantiser, the four LSBs (D_0-D_3) are extracted using a digital encoder. The encoder consists of three functional blocks: an XOR array, a bubble error correction (BEC) circuit, and a 15-to-4 ROM. A set of circular codes generated by the comparators are applied to the XOR array where they are converted into a set of 1-of-N codes. The 1-of-N codes are then sent to the BEC block where any error inside the circular codes is corrected by virtue of the NOR logical operation. The output of the BEC block is applied to the 15-to-4 ROM, where the final binary codes of the ADC are generated. The MSB D_4 is extracted directly from comparator #16 and the remaining one MSB D_5 is obtained by the coarse quantiser.

Implementation and Results

For test purpose, a 1:4 demultiplexer (DEMUX) with output drivers has been implemented on-chip. The ADC-DEMUX chain has been fabricated in HHNEC 0.18μm SiGe BiCMOS technology. The ADC occupies an area of 3.8mm×2.92mm; see Figure 9.

Two power supplies used for the analogue building blocks (AVCC = 3V) and the digital parts (DVCC = 3V). Of the 212 bonding pads, 120 are dedicated to the power and ground networks, to supply enough current with low bond-wire inductance.

We performed an ADC test using a high-speed evaluation board;

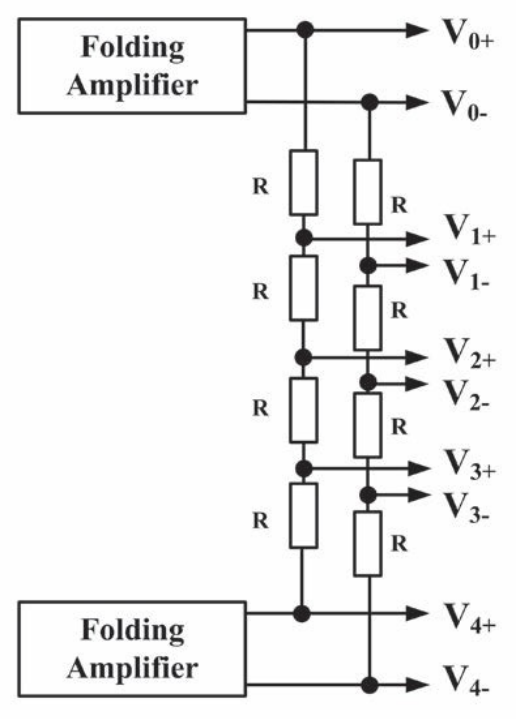

Figure 6: Interpolation between two folding amplifier outputs

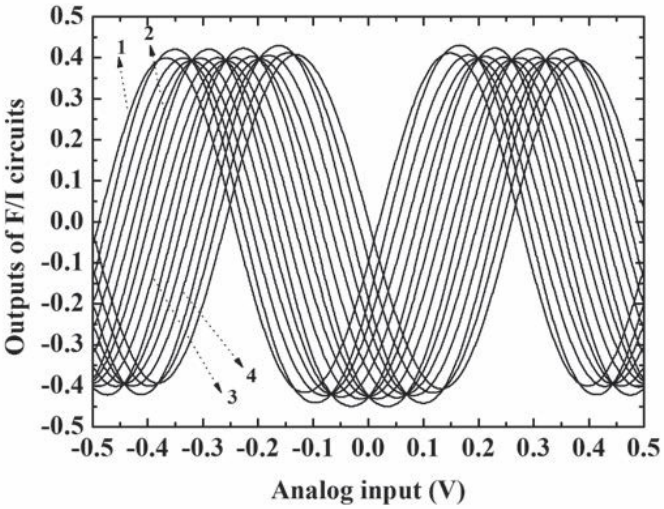

Figure 7: Transfer function of the folding-interpolating circuits

see the setup in Figure 10. Two wide-bandwidth baluns convert the outputs of the signal generators to supply the ADC with a differential analogue input and a differential clock input, respectively. The output data was captured with a high-speed data acquisition unit for analysis. At the clock frequency of 4GHz, the ADC's power dissipation is 1.1W.

Figure 11 shows the measured static linearity of DNL and integral nonlinearity (INL) at 4GSps, where the peak DNL is 0.35 LSB and the peak INL is 0.55 LSB, respectively. The high DNL and INL result from the interpolation topology, the nonlinearities in the sampling circuit and the resistive reference ladder.

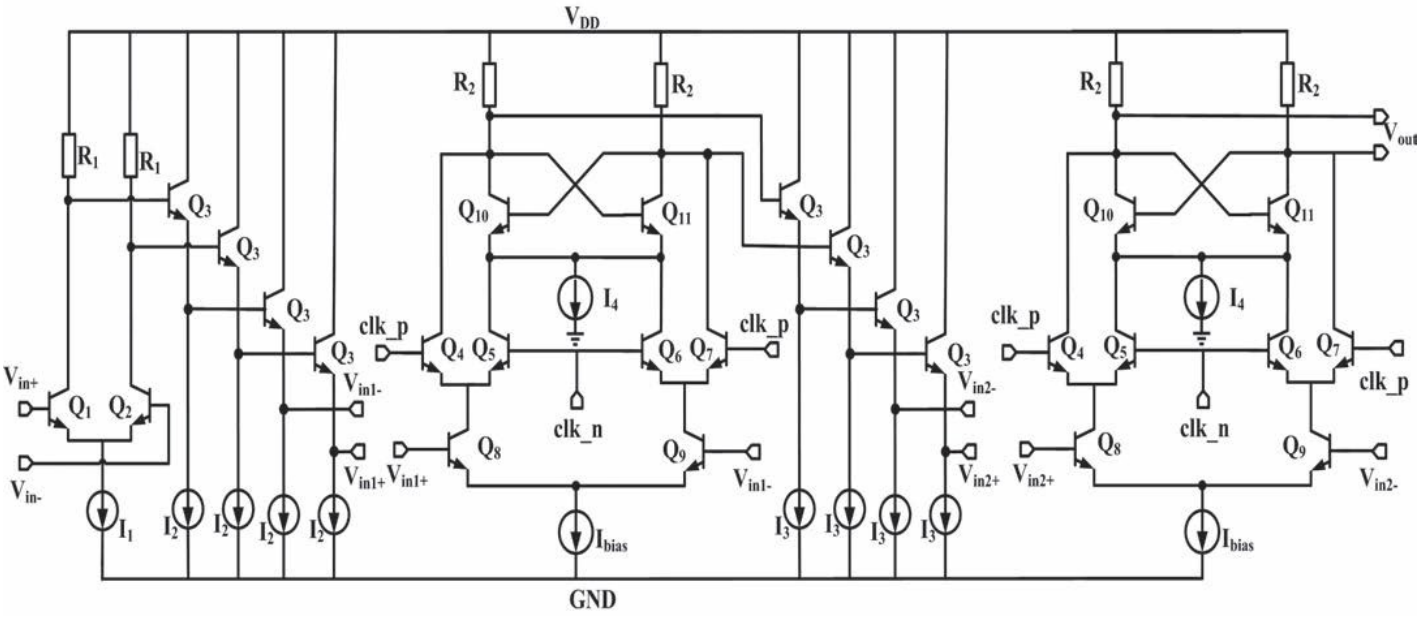

Figure 8: Master-slave comparator

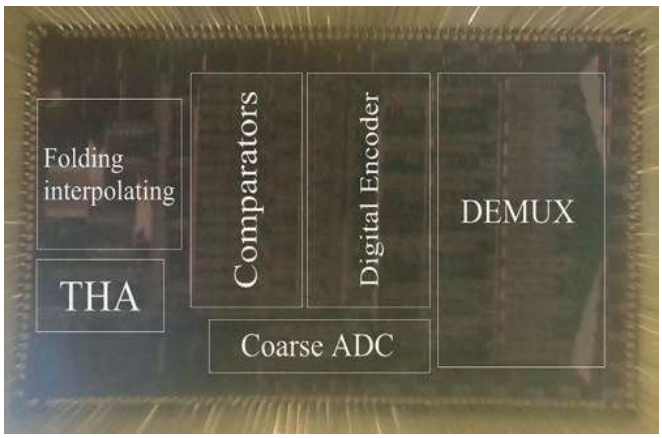

Figure 9: Chip microphotograph of the ADC-DEMUX chain

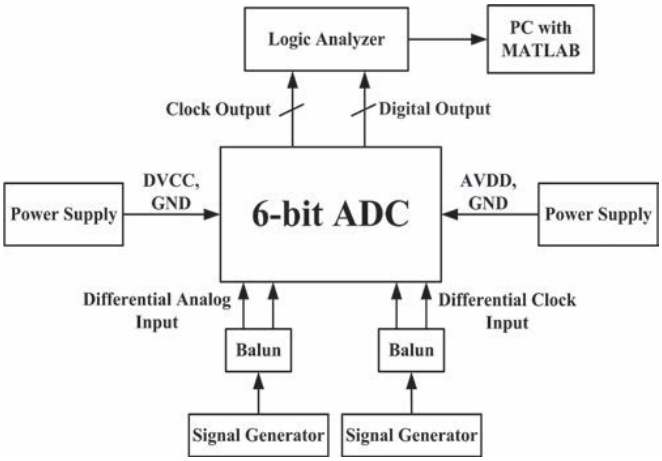

Figure 10: Block diagram of the ADC test setup

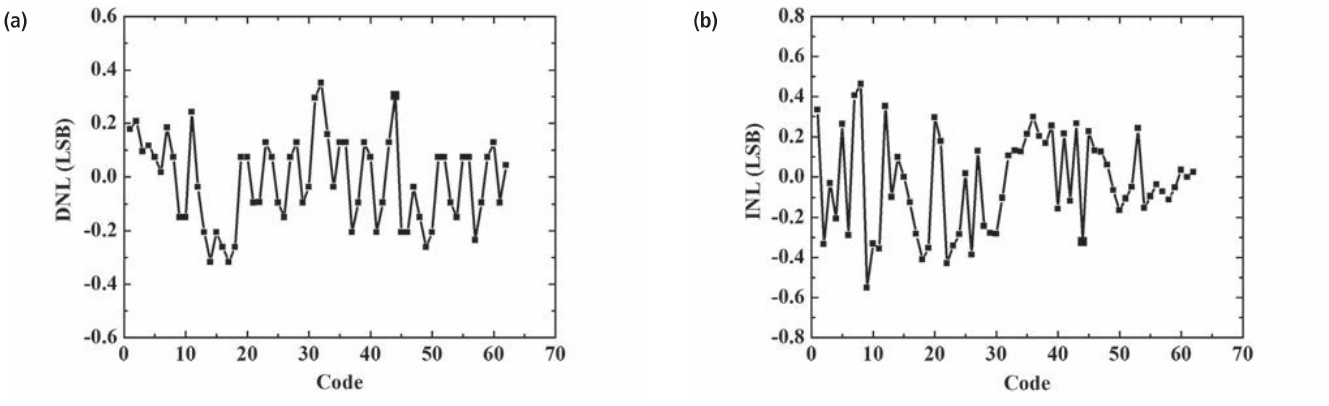

Figure 11: Measured (a) DNL; and (b) INL, at 4GSps

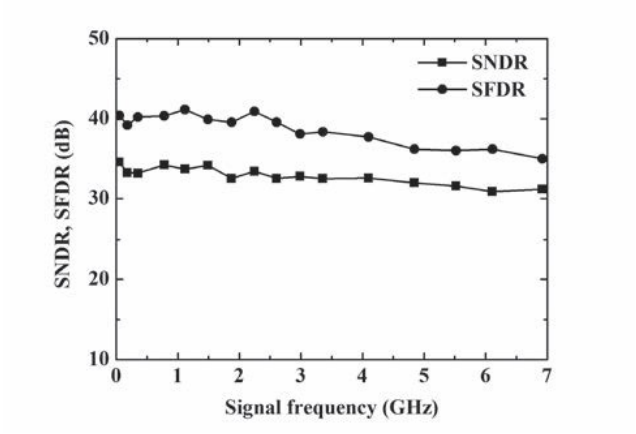

Figure 12: Measured SNDR and SFDR at 4GSps

To measure the ADC's dynamic performance, a low distortion sinewave input was applied to it, and the reconstructed waveform was obtained by binary weighted adding of the ADC's output codes. The reconstructed waveform was then analysed using MATLAB, to calculate the signal-to-noise-and-distortion ratio (SNDR), ENOB and spur-free dynamic range (SFDR). Figure 12 shows the ADC's SNDR and SFDR at different input frequencies when the converter is clocked at a sampling frequency of 4GSps.

PARAMETER	VALUE
Technology	0.18µm SiGe BiCMOS
Sampling rate	4GSps
Resolution	6 bits
Input range	$1V_{p-p}$
Maximum DNL	0.35 LSB
Maximum INL	0.55 LSB
SNDR	34.57dB
Peak ENOB	5.45
SFDR	40.4dB
ERBW	5.5GHz
Power dissipation	1.1W
Chip area	3.8mm × 2.92mm

Table 1: Summary of the 6-bit ADC characteristics

At low frequencies, the converter's SNDR is 34.57dB (5.45 ENOB). The ERBW where the SNDR drops 3dB from its low frequency value is 5.5GHz.

Table 1 summarises the 6-bit ADC's main characteristics. ❖