A three-stage fully-differential hybrid-compensated CMOS amplifier

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The amplifiers having a single stage achieve high gain by cascading, but this may lead to a low output swing

There's no slowing the current needs for low-power analogue, digital and mixed-signal circuits, especially in portable devices. Furthermore, in nanometre devices, the constraints of low power and the need for large voltage swings of low supply voltages call for unorthodox design using multi-stage amplifiers. This is further complicated by the need for higher data rates, continually rising bandwidths and high drive capabilities, leading to the ongoing design of output stages to drive large capacitive loads.

The class-AB output stage is a primary contender for increasing speeds and output swings. With only a single stage, this amplifier achieves high gain by cascading, which may, however, lead to low output swing because of the small supply voltages in nanometre CMOS technology. To maintain high gain and a high output swing would logically force the designer to apply a two- or three-stage fully-differential amplifier for doubling the output swing.

Here, we suggest an amplifier with a self-biasing configuration.

There are many advantages to self-biasing amplifiers: they enable simplified design without a biasing circuit, which saves on power dissipation and die area. In addition, the self-biased amplifier's circuit parameters don't change significantly with variations in process, voltage and temperature (PVT), so our aim is to achieve a low-power, three-stage, hybrid-compensated, fully-differential, self-biased amplifier with low supply voltage and large bandwidth. Target applications include front-end sample-and-hold and multiplying digital-to-analogue converter (MDAC) modules in pipelined analogue-to-digital converters (ADCs).

A Three-Stage Fully-Differential Amplifier

Compensation is an important design step in multi-stage amplifiers. In our amplifier, compensation is achieved by modifying the current buffer compensation topology with a split hybrid technique so that compensation capacitors C_{c1} and C_{c2} are connected to input nodes with low impedance. Common-mode feedback (CMFB) for the second stage uses a circuit with a resistor-capacitor topology as a replacement for the switched capacitor circuit. The output common-mode level for the input stage is adjusted with a continuous-time common-mode feedback circuit.

Figure 1 shows the proposed amplifier's circuit. It comprises two cascaded identical stages based on an inverter configuration and a class-AB output stage. The inverter input stage consists of a differential pair (M_{12} and M_{13}), connected to M_{11} that acts as a current source and to M_{14} that acts as a voltage-controlled resistor (VCR).

Similarly, the second stage has the same configuration with the differential pair transistors M_{22} and M_{23}, current source M_{21} and VCR M_{24}. Input nodes V_{ba} and V_{bb} are divided for connecting the compensation capacitors, which further split into two equal hybrid-compensation capacitors.

This compensation method is useful because there's no forward path for linking the first- and second-stage outputs, hence avoiding the occurrence of a zero at a low frequency that could cause instability.

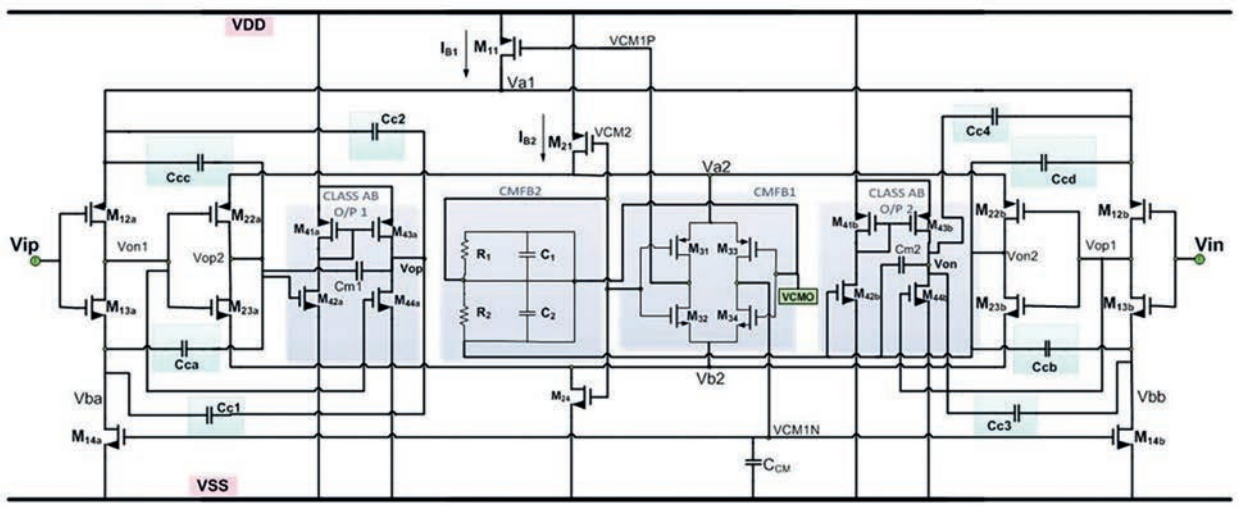

Figure 1: Our three-stage amplifier topology

The output stage also uses a hybrid-compensation technique, which achieves high unity gain bandwidth and a much-improved settling time.

Figure 1 shows the common-mode feedback circuits; see the CMFB1 and CMFB2 boxes. CMFB1 controls the input- and second-stage voltage levels and provides biasing for the entire amplifier circuit.

As previously discussed, the output of the common-mode level is also tuned by a resistive-capacitive circuit, or it can be replaced with a switched capacitor circuit. Also, $v_{cm2} = (v_{op2} + v_{on2})/2$, which controls the M_{21} voltage biasing and biases M_{24}, and produces the biasing voltage for the first-stage circuit.

CMFB1 is an inverter-topology differential pair, comparing V_{CM2} with V_{CM1}, and producing the control voltages v_{cm1p} and v_{cm1n} that bias stage one. The CMFB1 circuit is attached to nodes V_{a1} and V_{b2}, avoiding the need for a separate biasing circuit. Transistors M_{32} and M_{33} are sized by down-scaling transistors M_{22} and M_{23}, respectively.

Design Methodology and Optimisation

The following design considerations can be used as a starting point for this complex amplifier architecture:

- The compensation capacitor C_c should be chosen very carefully.

Table 1: The proposed amplifier's parameters

Device	Width (µm)	Length (µm)	VDS (mV)	VGS (mV)	gm (mS)	Operating Region
M11	100	3.2	-650	-782	1.48	Triode
M12	99	1.7	-933	-539	1.74	Saturation
M13	10	0.09	159	553	2.56	Saturation
M14	26	0.5	657	380	2.77	Saturation
M21	25	2.4	-614	-150	1.23	Triode/Saturation
M22	9	0.26	-976	-970	1.50	Saturation
M23	90	0.09	433	439	9.47	Saturation
M24	20	0.13	378	804	14.4	Triode/Saturation
M31	23	0.26	-169	-982	1.00	Triode
M32	23	0.26	124	426	6.00	Triode
M33	23	0.26	-140	-360	0.03	Triode
M34	23	0.26	281	137	0.02	Triode
Cc	50fF					

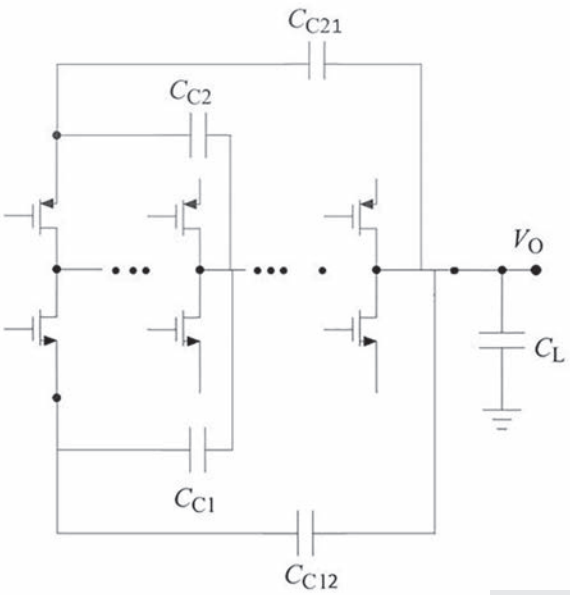

Figure 2: Proposed hybrid compensation scheme for a three-stage amplifier

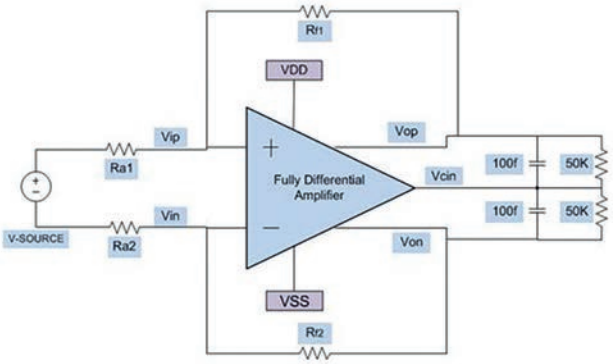

Figure 3: Simulation setup for amplifier characterisation

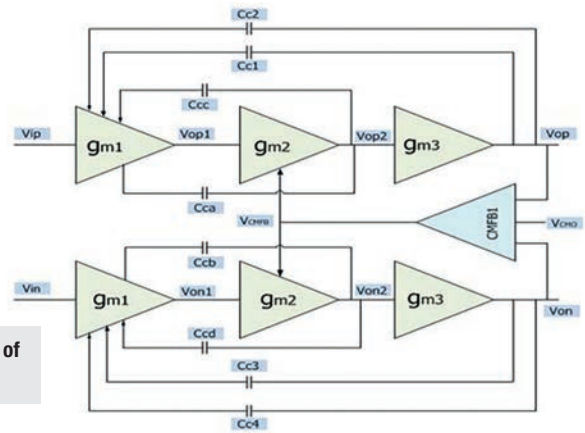

Figure 4: Block diagram of the amplifier's circuit

To avoid a zero and promote accurate adjustment of the dominant pole, a small value for C_c is chosen. If a good phase margin (PM) is attained ($65^o < PM < 75^o$), then a high-quality time response is achievable.

- The M_{12}'s gate length is set as a large value to attain a large DC gain. This technique also sets a low value for V_{DSsat} and a high g_m to transfer the zero to high frequency.
- The gate lengths of transistors M_{13} are also set to attain a high value DC gain. A high g_m value helps the compensation by providing a pole splitting effect. The V_{DSsat} of this transistor should be selected with care, to maintain small C_{O1} and C_{gs13}.
- M14 is set to attain a large g_m, so it's recommended to use a small channel length and small overdrive voltage V_{ov}.
- To increase the output swing, transistors M_{22} and M_{23} should have a very low V_{DSsat}. Gate lengths for both transistors are set so they attain high gain.
- Transistor M_{11} is biased so it operates at the boundary of the triode/saturation region by adjusting V_{DS} to keep M_{12} in saturation.
- Transistors M_{21} and M_{24} are set so to operate at the boundary triode/saturation region.
- Transistors M_{32} and M_{33} are sized by down-scaling the values of M_{22} and M_{23}, respectively.

Device	Width (µm)	Length (µm)	VDS (mV)	VGS (mV)	gm (nS)
M41a	54	0.09	-6.79	-6.77	2
M42a	99	0.09	1.932	-389	0.0035
M43a	5	0.09	-1.589	-6.77	139
M44a	99	0.09	389	5.97	596
M41b	54	0.09	-650	-782	2.32
M42b	99	0.09	-933	-539	0.0024
M43b	5	0.09	-1.6	-7.77	146
M44b	99	0.09	402	19	902

Table 2: Class AB output stage device parameters

Compensation Scheme

The compensation technique used in our amplifier design is based on a hybrid topology, or more specifically, the hybrid cascode feed forward compensation (HCFC) method. Here, capacitor C_c that's normally used in the Miller compensation is equally divided (into C_{c1} and C_{c2}) to make two feedback loops, which considerably enhances the bandwidth and stability of the amplifier.

Figure 2 shows our proposed hybrid compensation circuit for the three-stage amplifier. Without increasing the size of the capacitor or supply voltage, this method boosts the total current (AC) that's fed back into the first stage and, consquently, enhances the stability. Weighted against other prevailing schemes, the HCFC technique demonstrates vital improvements in capacitor size, bandwidth, dissipated power and settling time.

The Class-AB Output Stage

Many methods are used in multi-stage amplifiers to enhance the slew rate and settling time. The one selected for this amplifier is the pseudo class AB topology.

The fundamental idea of this method is to apply a current dependent on the signal coming from the previous stage on to the common-source transistor. To achieve a fast settling time and avoid overshoot of the step response, a pseudo-class-AB output stage consists of M_{41}-M_{44}, which is added to both outputs of the proposed amplifier; see Table 2. This buffer stage can drive large capacitive loads (CL).

Although bandwidth is reduced to some extent, using this output stage results in significant improvement to the settling time.

Simulation Results

The circuit proposed here is designed for a 1.2V supply and low-leakage 1P-9M standard CMOS transistors; the capacitors are based on a metal-insulator-metal (MIM) structure. Figure 3 shows the common-mode feedback, CMFB2, a resistor-capacitor circuit consisting of two 50k resistors and two 100fF capacitors. As mentioned before, CMFB2 can be replaced with a switched capacitor circuit for applications that require sample-and-hold front-end amplifiers.

For small-signal analysis and determining differential mode gain, we used the amplifier half-circuit shown in Figure 5; its common-mode input voltage was set at 550mV.

Using the transfer function thus obtained, the approximate low-frequency differential gain of the amplifier half-circuit can be determined by:

$$A_{v0} \approx \frac{g_{m2}}{g_{ds2}} \cdot \frac{(g_{m13}^{\ 2} - g_{m1} \cdot (g_{m13} + g_{ds14}))}{(g_{ds13} \cdot g_{m13} - g_{ds1} \cdot (g_{m13} + g_{ds14}))} \qquad (1)$$

where

$$g_{m1} = g_{m12} + g_{m13}$$
$$g_{m2} = g_{m22} + g_{m23}$$
$$g_{ds1} = g_{ds12} + g_{ds13}$$
$$g_{ds2} = g_{ds22} + g_{ds23}$$

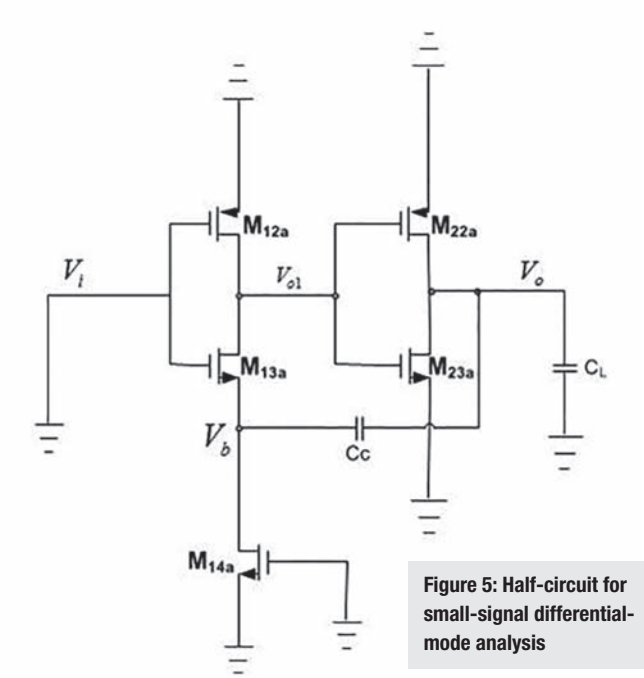

Figure 5: Half-circuit for small-signal differential-mode analysis

The pseudo-class-AB output stage in the unity gain condition does not contribute to the gain of the amplifier, so it's ignored in Equation 1. For better frequency response, the split compensated capacitors C_{ca} and C_{cc} (Figure 4) can be added to the single capacitor C_c in the half circuit of Figure 5.

Similarly, split compensated capacitors C_{cb} and C_{cd} are also added to the other half of the circuit. The frequency response of the amplifier is shown in Figure 6. The proposed amplifier achieves a gain bandwidth of 1.53GHz with a phase margin of 75°. The amplifier provides good differential gain, almost zero common-mode gain and a very high common mode rejection ratio (CMRR).

Transient Analysis

To find the step response, a square wave signal of 50mV peak-to-peak was applied, with the results shown in Figure 7. To optimise settling time, the value of PM should be set between 70° and 75°. However, depending on the PM only, this may not suffice there with an increased number of poles, as is the case in three-stage amplifiers.

The amplifier's settling time can be divided into two separate parts, or periods. The first is known as "slew time" through which the output reaches a maximum output value in a non-linear manner. It's calculated using the output current that charges the compensation capacitor C_c.

In the second part, the output reaches its final value and proceeds in a quasi-linear manner. Generally, in high-speed amplifiers, the first part is very small and the second relatively large. Research shows that the second part is considerably affected by the pairs of poles and zeros. The compensation is liable to degrade the settling time due to the creation of inevitable pairs of poles and zeros that the feed-forward path C_c establishes. To counter this effect, the class-AB push-pull output stage is used in our design to optimise settling time and slew rate. The applied compensation topology, having equally divided capacitors, balances both the rising (positive) and falling

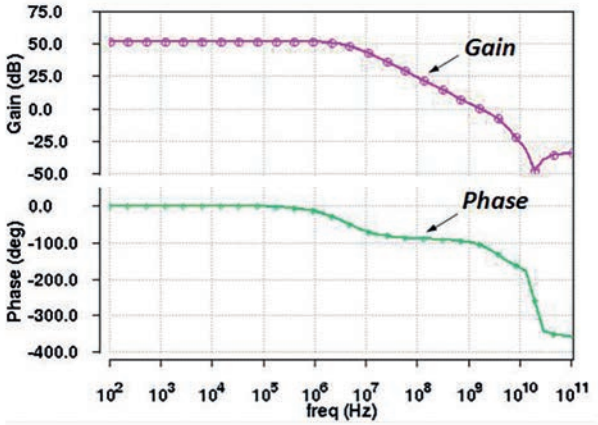

Figure 6: Amplifier gain and phase bode diagram

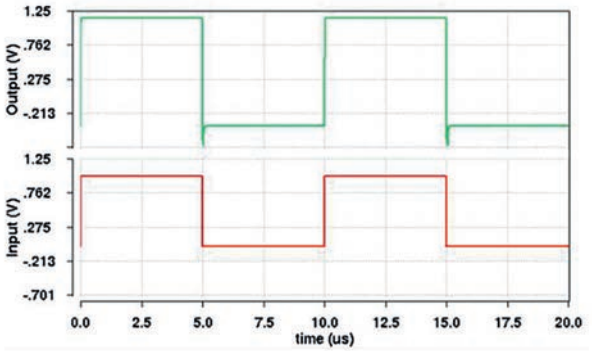

Figure 7: Step response with a load capacitor C_L = 15pF

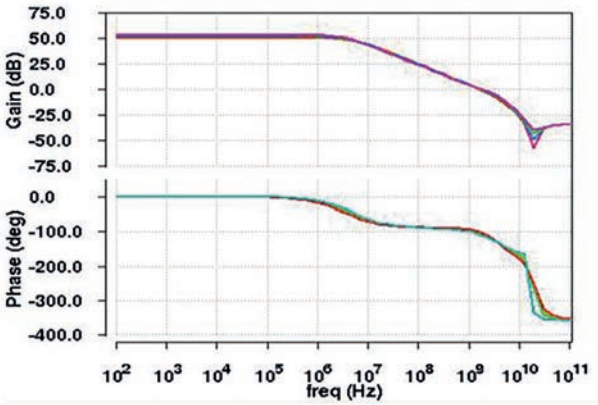

Figure 8: Temperature variation of the amplifier's gain and phase

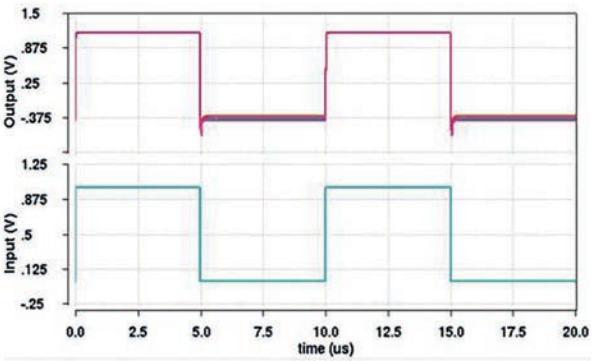

Figure 9: Temperature variation in step response of the amplifier

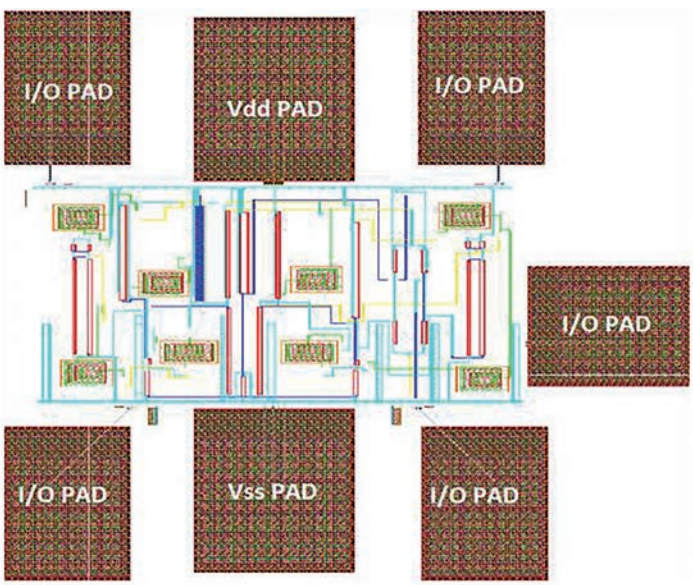

Figure 10: Complete layout and floorplan of the proposed amplifier

(negative) slew rates. The internal slew rate (SR_{INT}) and external slew rate (SR_{EXT}) are given by:

$$SR_{INT} = \frac{I_B}{C_{C1}+C_{C2}} \quad (2)$$

$$SR_{EXT} = \frac{I_L}{C_{C1}+C_{C2}+C_L} \quad (3)$$

Slew rate was improved by increasing I_B and I_L using Equations 3 and 4. An improvement was also observed by decreasing the compensation and load capacitors. Settling time for the proposed amplifier was found to be 54ns.

Temperature Variations

To analyse the effects of temperature variation on the amplifier parameters, we applied a temperature sweep of 0-100°C. The gain of the amplifier showed only a 3dB variation; see Figure 8. Settling times for its step response in Figure 9 remained almost constant over the temperature variation, making for a very stable amplifier. Figure 10 shows its layout. EW