ELECTRONICS WORLD

JUNE 2006 £4.50

INSIDE:

Design Issues Around Deterministic Ethernet, PoE, CAN and IEEE 802.11b/g

Creating Resonant Circuits with RLC and RCL Sections

Automotive Technology Stories

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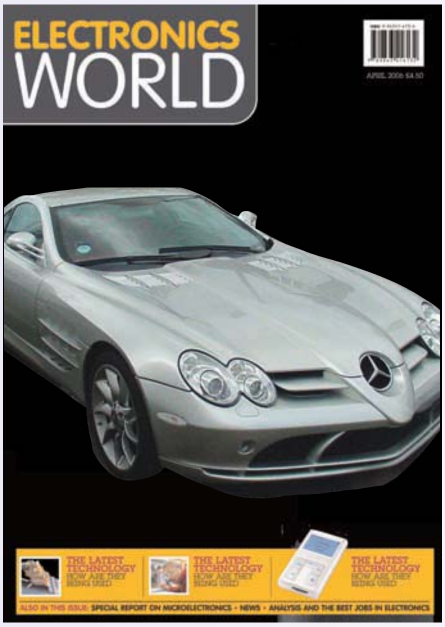

New look Electronics World

As of the next issue — July cover month, but published at the end of May — Electronics World will be coming to you in a different guise.

As the electronics industry continues to evolve, so do the magazines covering it. We felt it was time that Electronics World became a bit more modern and attractive to our existing as well as a new generation of readers.

We hope you enjoy the new look. As always we welcome your feedback!

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Too much information can be a bad thing

A recent two-day conference on the subject of automotive electronics turned out to be an enlightening experience. Although I only attended the communications side of the conference, the mind boggles at the thought of the ambition this industry has for the car.

Car-to-car communication and car-to-infrastructure communication are to be harnessed to create a dynamic network of road-side and in-car systems which will detect and warn of potential accidents, or accidents that have already occurred; it will pinpoint where an oil spill or black ice is on the road; it will give detailed information of the state of the traffic on your favorite route and a lot more. But, information is just one aspect of it, the other — which could be a lot tougher to implement — is managing the road infrastructure (traffic lights, toll booths, dynamic lanes etc) to avoid road blocks, alleviate traffic bottlenecks and, indeed, prevent accidents.

Several standards are already in the progress of being worked on for very specific aspects of this ambition, such as prevention of accidents or emergency calls, but more or less all of them will rely on several wireless technologies that we already use or will use in the near future as consumers, with the added one or two, such as the millimeter wave technology. Spectrum usage has already been requested for certain frequencies to allow devices built into vehicles to operate across, not only Europe, but Japan and the US, too.

When laid out as methodically as this, the goal appears simple and, hence, achievable. But, when one has to delve into the protocols, systems, devices and technology interoperabilities themselves to make all of this happen seamlessly and smoothly — at all times — well then, it all becomes a bit of a blur. How is all of it going to work together? And are drivers likely to want to use all of that information bombarding them in the car — whether on a head-up display or a unit attached to the dashboard – or, indeed, as some would have it, on the mobile phone?

According to one automotive consultant, whose company conducted a survey of car users and their interests in future in-car devices, what people want first and foremost is in-car diagnostics, immediately followed by in-car entertainment. So, why is there such a discrepancy between what the industry seems to think drivers want and what drivers seem to believe they need?

Svetlana Josifovska
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Walter Tuttlebee of the MobileVCE

Mobile phones "good enough" to get into the driving seat

It is in the pocket of almost a third of the world's population and now the mobile phone is aiming to get into each vehicle on the planet too. According to Dr Walter Tuttlebee, executive director of MobileVCE, the handset and the 3GMS network – with its subsequent standard evolutions – is the perfect device for vehicles to communicate with the roadside infrastructure and each other.

"We need to combine ITS [Intelligent Transport Systems] services with mobile communications. We are at that point when the two can inter-work," he said. "We could start with the simpler services and then move on to the complex ones."

"We can create the market for users in cars, it can be achieved with very little new infrastructure needed. However, it requires an integrated approach, an inter-industry cooperation, standard protocols and a coordinated approach to policy," added Dr Tuttlebee.

However, Paul Kompfner, head of new initiatives within Ertico, who also focuses on initiatives involving vehicle communication, such as CVIS (Cooperative Vehicle Infrastructure Systems) launched in February this year, said: "3GSM [alone] is not a viable bearer for telematic services."

This is particularly true as the public mobile phone network can be switched off (as in the case of an act of terrorism, for example), and the network's problems with density and capacity — we all know what happens on New Year's Eve — are well documented. This goes in the face of what the 'connected vehicle' should be about.

"We'd like the vehicle to always be connected to offer high bandwidth, real-time response, with priority messaging of safety messages," added Kompfner.

New buck-boost IC extends runtime in Li-ion batteries

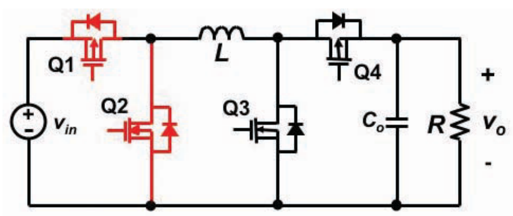
Texas Instruments (TI) launched a buck-boost converter IC to help extend battery life in lithium-ion (Li-ion) powered devices. The DC/DC converter delivers up to 96% efficiency over a wide input voltage range of 1.8V to 5.5V, while generating an output current up to 1.2A.

"The developers who use this technology [Li-ion] get very excited about a few percent improvement in efficiency, because that means that they can get an extra few hours of battery run-time," said Uwe Mengelkemp, the head of the worldwide DC/DC converter operation at TI.

TI's new TPS63000 buck-boost converter provides up to 28% greater run-time compared to a standard high-efficiency buck converter with a 3.3V output. Based on a fixed frequency, pulse-width modulation (PWM) technique, the device uses synchronous rectification to maintain high efficiency.

"There are some battery technologies that offer better energy densities, like Li-ion and Li-mangenese. This [trend] is changing so much that it's driving the need for buck-boost converters rather than a buck converter," said Mengelkemp. "Future battery technologies will require a bigger range of input voltages and that also requires a buck-boost conversion."

This device runs with different size inductors and the number of external components has been reduced.



High efficiency non-inverting buck-boost DC/DC converter

Chipmaker has coax to thank for sales boom

Sony's high-definition DVR

The widespread use of coaxial cables inside US houses is the only way forward for the next generation of home networks, claims a semiconductor start-up that is already cashing in on the idea.

Manufacturers of set-top boxes, digital video recorders (DVR), broadband routers and optical network terminals are embedding their products with Entropic Communications's c.LINK-270 chip already, which uses coax installed inside the walls to distribute multimedia content – including multiple simultaneous high-definition (HD) video streams and multiplayer gaming – to every room.

Field trials conducted by the Entropic showed the solution is capable of delivering a minimum data rate of 100Mbit/s to 97% of coax outlets currently deployed in the US.

"There are some 110 million homes in the US and all of them but about 3 million have coax. There are about 100 million subscribers to cable and satellite. Every single one of those TVs (including those receiving terrestrial services) is reached by coax. So, if you want to do triple-play – or just video services – you have to get to the TVs," said Ladd Wardani, president of the Multimedia over Coax Alliance (MoCA) and vice president of business development with Entropic.

If coax is to become the medium of choice for the next generation of home networks, it will need to prove its worth against the competition offered by four rival technologies including power lines (standardised as HomePlug A/V), telephone lines (HPNA 3.0), WiFi networks (802.11x) and CAT5 cables (Fast Ethernet).

Of these, Wardani says the only two platforms capable of offering the raw speed and reliability demanded by heavy multimedia content flowing through the new breed of HD DVDs, DVRs, game consoles and flat screens are coax and CAT5. But, while coax is already installed in practically all homes in North America, Ethernet over CAT5 wiring is used in only a handful of households.

Wardani accepts WiFi has so far been the dominant networking technology for whole-house broadband access and printer sharing. But he insists the limitations imposed by the unlicensed spectrum in which Wi-Fi operates will make it unworkable for high-end video applications.

PoE is gaining in power

Companies have already started preparing the silicon for Power over Ethernet (PoE) IEEE 802.3at switches ahead of its ratification, which is expected in late 2007.

PowerDsine, a supplier of PoE solutions says that it will start offering silicon based on the new standard at the end of this year. "By the time the new standard is ratified, many companies will have products ready, if they started embedding our silicon, which is going to be ready in the fourth quarter of this year," said Igal Rotem, CEO and co-founder of Power Dsine.

PoE allows the transmission of power as well as data to remote devices over a standard twisted-pair cable in an Ethernet network. It is useful for powering wireless LAN access points, IP telephones, webcams, Ethernet hubs, computers and other systems. PoE eliminates the need to run 110/220 VAC power to wireless access points and other devices on a wired LAN.

The current standard, the IEE 802.3af, was ratified in 2003. It allowed power of up to 15.4W per port. However, some complained that this was not enough for most of the IP phones and security systems currently on the market. Therefore, moves have been made to have power of up to 45W per port. This is the new IEEE 802.3at standard, which will be backward compatible with the previous one.

Although at the moment it is the enterprise and SME markets that are mostly using PoE, the standard is already being promoted into the residential market. Netgear is one of the first companies to reach the residential market. "It will take until the end of 2007 for the equilibrium to take place between the SME and residential markets. But without a doubt the residential one will be bigger at one point in the future," said Rotem.

Power limitation	
– Current	350mA
– Voltage	44-57V
– Max power at source	15.4W
– Max allowed power consumption	12.95W
Power transfer allowed modes	
– Data Vs. Spare lines	Either data OR spare lines
Safety	
– Line detection	identifying PoE comply unit connection
– Protections	High current, disconnect and more

IEEE802.3af limitations

Yozan steams ahead with a WiMax service in Japan

Japan's WiMax wireless coverage continues unabated with Yozan's plans to extend its service not only to the whole of Tokyo, but also all of Nagoya and Osaka by the end of June this year.

Yozan uses the restricted license-exempt 4.9GHz frequency band to offer two services – one for the corporate user, called WiMax Direct, and one for the residential user, called BitStand. They are both based on the IEEE 802.16d and e standards, optimised for fixed and nomadic access.

The basestations are provided by AirSpan and will require a software-only upgrade to support Mobile WiMax, enabled by picoChip devices lying at the heart of the basestation. With the upgrade, the base stations will simultaneously support both 256 OFDM fixed CPEs and SOFDMA mobile WiMax laptop cards and handsets.

The 16eUSB from AirSpan

AirSpan will also supply Yozan with a Mobile WiMax USB v2.0 device, called 16eUSB, which connects laptop computers to the service. The USB device carries all of the software on board and it automatically knows if it's in the vicinity of a WiFi or WiMax network and which one, without having to switch on the laptop.

Yozan will make this product available to its customers by the middle of next year. "Such a device normally has a window of opportunity [as a standalone] of three years. Eventually, these devices will end up in the laptop," said Paul Senior, vice president of product marketing at AirSpan.

Project launched to make cars 'talk' to each other

A major new European project was launched last month to build a platform for vehicle to vehicle and vehicle to road infrastructure communication. The CVIS (Cooperative Vehicle Infrastructure Systems) is a four-year project, funded by the EU to the level of €41m and it involves 63 partners, coordinated by Ertico. Among the consortium members are Alcatel, Volvo, Vodafone, DaimlerChrysler, Bosch, BAE Systems, BMW, Fiat, Ericsson and others.

The platform will consists of in-vehicle sensors, a CVIS host and OEM gateways. The communication network will fall under the CALM (Continuous Air interface for Long- and Medium-range distance) architecture's umbrella.

At present, DaimlerChrysler is preparing a trial system, where information from various vehicles' sensors will be gathered and fed into the CVIS network, which will then be used to implement schemes such as traffic calming, cooperative acceleration/deceleration of the traffic, dynamic lanes etc.

"This four-year project will be nowhere near deployment when it finishes, but we can aim to create open and royalty-free standards. We need to place these things on the OEMs' roadmaps as it [the CVIS platform] will be a flexible communications centre for the vehicle to communicate in the future," said Paul Kompfner, head of new initiatives within Ertico. "We also need to inform the public that this is coming."

CVIS is not the only project along these lines. Others include the IVSS in Sweden, Invent, Activ and Network on Wheels (NOW) in Germany and Safespot in the UK.

The hard disk drive (HDD) market will go through rapid growth through to 2010, fuelled by digital consumer electronics, says Future Horizons.
According to market research firm, shipments of HDDs reached record levels in 2005 of 385 million units and volumes are set to more than double by 2010 to 891 million units.
Over the past few years, the HDD industry has seen its products become smaller, lower power and with greater storage capacity per dollar. Even though there's a limit to how much the product can shrink, reports indicate that it will realistically reduce beyond the 1-inch and 0.85-inch package sizes to even smaller formats.

Ω

Cambridge Consultants, the technology-based design company, is planning to reactivate its spin-out business with the creation of a new venture fund. The company has a track record of developing start-up companies.
The fund will be created jointly by Cambridge Consultants and an investment partner with the aim of having it established and operating by the summer of 2006. Several blue-chip investors have already shown interest in the fund.

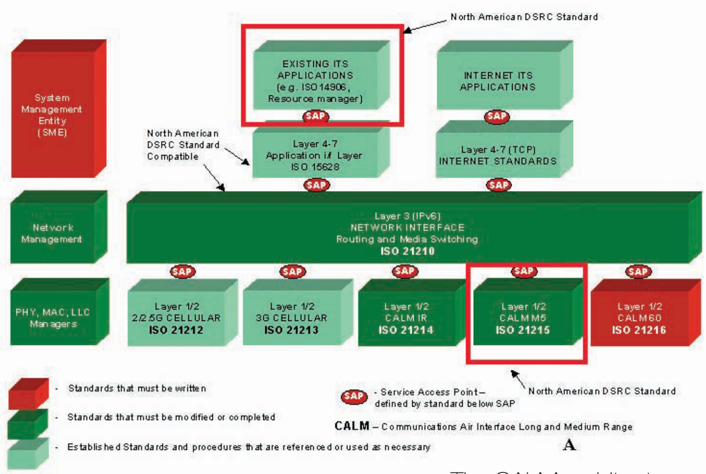
Ω

Sony will continue its domination of the video console market through 2010, though its lead will likely shrink due to stronger competition from Microsoft and Nintendo, reports In-Stat.
Through 2010, the Sony PS3 will account for just over 50% of the installed base of next-generation consoles, while the Microsoft Xbox 360 will have 28.6% and the Nintendo Revolution 21.2%, says the market research firm.
The PS3 is expected to include Blu-Ray DVD playback, a high-definition format that is central to Sony's corporate strategy.
Central to Nintendo's console is a new type of controller that allows the user's arm movement to affect the movement of game characters.

The umbrella standard for vehicle communications is CALM

Despite the quest to find a single standard that will connect the car to the road-side, other cars, the home and office, it is very likely that the industry will have to use more than one.

"You need different communications systems for different applications. For example, for emergency calls and crash warning messages you will need as long and wide a coverage area as possible, but for traffic lights communicating to the cars nearby you'll need something more local to avoid ambiguity," said Nigel Wall, manager at the Shadow Creek Consulting. "There isn't a single standard to cover all these requirements, so it's likely that we will combine more than one."



The CALM architecture

Possible systems that can be used to work in cooperation to deliver various requirements for the connected vehicle are 2G, 3G, DAB, RDS, Tetra and satellite for long range communication; DSRC (dedicated short range communication) on the range of below 50 metres; and IEEE 802.11p(WAVE)/CALM M5 medium range of between 50 and 500 metres.

The ISO TC204/WG16 CALM (Continuous Air interface for Long and Medium distance) architecture can support all these systems for ad-hoc communication and is one standard that is being worked on at the moment, by the Working Group 16, and expected by many in the industry. CALM engulfs the IEEE 802.11p, GSM, UMTS, infrared, millimetre-wave and IPv6 protocols. It will also easily incorporate messages from within the car itself, such as from the CAN or LIN networks that connect various electronic control units and sensors. The CALM Forum is also working on bringing the WiFi, ZigBee and Bluetooth protocols under the CALM umbrella, too.

"CALM is the standard that we need in Europe," confirmed Paul Kompfner, head of new initiatives within Ertico, the European multi-sector, public/private partnership, pursuing the development and deployment of Intelligent Transport Systems (ITS) and services.

At present, the requested spectrum in Europe for CALM is between 5.85MHz and 5.925MHz. This will coincide with the US equivalent, and potentially the Japanese one too, which will help cars that are being imported to communicate anywhere on the same frequency.

"It is critically important to make [CALM] work and we need to make people much more aware of it," added Wall.

Environmental Compliance

TOP 10 TIPS

- On the eve of major changes to environmental legislation affecting the sector, electronics manufacturers need to start preparing now to ensure that they are compliant with the new regulations.
- Assess the impact of environmental legislation on your current product portfolio.
- Consider compliance with environmental legislation as a business opportunity.
- Start designing products for reuse and recycling by making them simple and inexpensive to take apart.
- Work with suppliers and customers to agree cost-effective ways to make changes throughout the supply chain.
- Give somebody within the business responsibility for implementing the necessary changes.
- Make sure that staff throughout the company understand the implications of environmental legislation.
- Take advantage of a free Design Track visit from Envirowise (Tel: 0800 585794).
- Log onto the NetRegs website — www.netregs.gov.uk — for clear guidance on what environmental legislation means for your business.
- Keep updated on changes to the legislation by registering for NetRegs e-alerts.

This month's Top 10 Tips were supplied by NetRegs — www.netregs.gov.uk — a free website set up by the UK's environmental regulators to provide clear guidance to small businesses on how to comply with environmental legislation. NetRegs also offers advice to help businesses make cost savings and become more competitive.

If you'd like to send us your top five or top ten tips on any subject you like, please write to the Editor at **EWeditor@nexusmedia.com**

IBM scientists have developed a new technique for exploring and controlling magnetism at atomic level. In experiments, IBM researchers created chains of up to 10 manganese atoms atop an extremely thin electrically insulating surface and measured how the magnetic properties changed as each new atom was added.
The new method will help understand the operation of future computer circuit and data-storage elements as they shrink toward atomic dimensions, but also lay the foundation for new materials and computing devices.

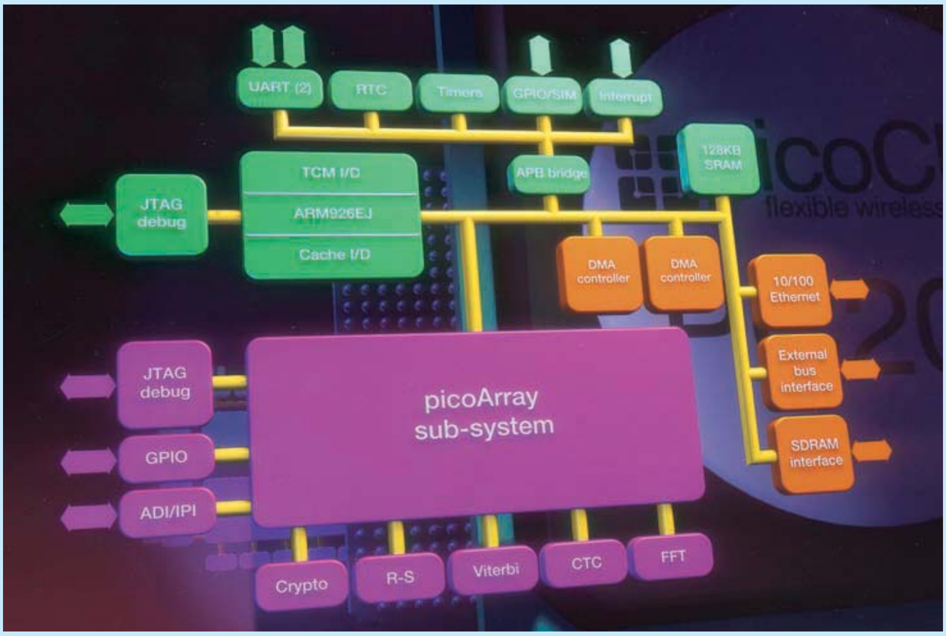
Ω

The European Commission has launched a €6.5m initiative to provide integrated microsystem services. INTEGRAMplus will offer design, prototyping and manufacturing expertise in highly integrated microsystems over a period of three years.
This is a new Framework 6 Integrated Project and it will be co-ordinated by the UK firm QinetiQ, but draw on the expertise and facilities of ten partners from seven different European countries.
INTEGRAMplus will focus on integrating silicon-based MEMS with polymer backplanes, and platforms which provide additional functions, packaging and interfacing to the macro-world. One of three first proof-of-concept demonstrator components will be a bio-diagnostics sensor for the healthcare market.

Ω

Graphite, the material that gives pencils their marking ability, could be the basis for a new class of nanometer-scale electronic devices that have the properties of carbon nanotubes but could be produced using established microelectronics manufacturing techniques.
Using thin layers of graphite known as graphene, researchers at the US Georgia Institute of Technology, in collaboration with the Centre National de la Recherche Scientifique (CNRS) in France, have produced proof-of-principle transistors, loop devices and circuitry. Ultimately, the researchers hope to use graphene layers less than 10 atoms thick as the basis for revolutionary electronic systems that would manipulate electrons as waves rather than particles, much like photonic systems control light waves.

picoChip's parallel processors change the face of wireless technologies



What lies at the heart of the picoChip PC202 processor

"Wireless technology is getting tougher," said Rupert Baines, vice president of marketing at Bath-based picoChip. "Demands on algorithms have been doubling every 15 months – rather than as in Moore's Law every 18 months – and there are so many fragmentations within it, such as with UMTS, for example."

Baines says the solution to keep up with these changes and demands is a programmable one, and that picoChip has just the ticket, with a new family of multicore devices, consisting of PC202, PC203 and PC205. They each pack in about 200 individual processors in each die, fabricated in TSMC's 90nm process. They deliver over 100GIPs and 25GMACs, but according to Baines, are very cost-effective and among the first to break the $1 per GMAC barrier. "You'll find that standard chips now are near the $10 per GMAC, but [our] PC202 is a mass-market device at the price of $1 per GMAC."

picoChip's family of products is aimed at WiMax and cellular basestations with a firm roadmap to keep upgrading to future generation standards, such as HSDPA, HSUPA, WiMax 16d and 16e, among others.

PicoChip's devices are based on the company's invention – the picoArray architecture, which consists of heterogeneous parallel 16-bit processors (3-way LIW Harvard architecture). The processors are programmed individually, where tasks are "mapped" onto them, "much as in a block diagram of a whiteboard" said Baines. The novel part of the architecture, however, is its interconnect and the peer-to-peer communication between any of the processors in the fabric. Baines describes the architecture as "the best of both worlds of DSPs and FPGAs".

Analogue 'design renaissance' in Europe

Europe is seeing a resurgence of high-tech company design centres, says **John Phelps**

Analogue is the key enabling technology which translates analogue signals (such as voice, e.g. the words we are speaking into our handsets) into digital signals (i.e. the ones and zeroes that our handset can transfer to the handset of another person, even at the other end of the world) and often back into analogue again, so that we can work, play and live in our modern world.

In short, analogue semiconductors provide us with indispensable capabilities, and the more "digital" devices we use in our daily lives, the more "analogue" we need. These analogue-intensive solutions can differentiate customers' products — providing better audio and sharper images in electronics systems such as MP3 players, game machines, notebooks and mobile phones, better energy efficiency in all portable equipment, more precision and security functions in cars and medical equipment such as ultrasound systems, MRIs, etc.

Europe has a huge customer base for analogue technologies; just think of the leading worldwide telecommunications or automotive manufacturers headquartered in this region, and of the many other companies providing leading-edge products for the broad market. In order to work with them, on defining and creating the products of today and of the future, analogue companies need and want to be near to them, speak to them in real-time, in their time zone, face-to-face, on a daily basis.

Along with a superb European customer base comes exciting applications. Europe has always been known for excellent scientific and engineering capabilities and has produced a number of brilliant scientists who have had great impact on the way we live today, for example, Albert Einstein, Werner von Siemens, Carl Zeiss and Robert Bosch. These personalities stand for innovation and their legacies continue to provide us with leading-edge technology and world-class products right out of Europe. I mention these names because I often feel that Europeans do not stress enough, or don't even seem to be aware of, the brilliant technology that has been created and is still being developed in this region.

While much manufacturing has left Europe, many customers are opening design centres here, such as Motorola's new (4th) 3G design centre in the UK, the new Siemens VDO design centre and many other companies that are finding that European design talent is not replaceable overseas. We see a "design renaissance" taking place here in Europe. Combine this trend with the recent weakening of the Euro and it is clear that the total cost of ownership is becoming more competitive than in China.

> *"While much manufacturing has left Europe, many customers are opening design centres here; companies are finding that European design talent is not replaceable overseas"*

Getting products up and running in China entails many risks, time delays in the event of problems, and higher logistics and inventory costs. I saw this demonstrated in a recent visit to Italy, where many local companies prefer to work with one of the local contract manufacturers who specialise in high mix and lower volumes. The efficiency of working with nearby factories does wonders for the concept of design for manufacturing and also time to market. This scenario appears to be gaining strength and, at National, we honour and appreciate this environment and are proud of the technical talent and expertise we can offer to our customers by recruiting and developing engineers from universities across Europe.

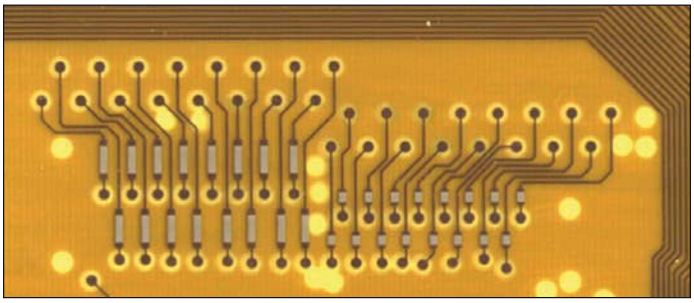
We currently have 10 European design centres — often located near a university — and many of the products and applications that we develop with and for our customers are designed here. In the Nordic Region there's the design of LDOs and lighting management units; in the Netherlands/Delft is the design of LMV microphone drivers; in Munich, Germany, we created the 3GSps analogue-to-digital converter and the newly formed Power Applications Design Centre is now located there. In Scotland we design audio sub-systems, as well as fabricate analogue devices.

Our new design centre in Munich will provide our customers with access to reference designs that solve the tough power design challenges for a diverse set of applications. This is a significant investment that demonstrates our belief in the European market and our commitment to supporting the design teams of our customers. We are committed to the European region and will continue to contribute to the innovative force of this fascinating continent.

John Phelps is vice president and general manager for Europe at National Semiconductor

Passives
Set To Go Underground

By Keith Gurnett and Tom Adams



Grey items are printed OhmegaPly resistors on an IC. Longer ones at left are approximately 3 squares length; shorter ones at right are approximately 1 square

In five years or so, taking a peek at a PC board may yield a surprise. The familiar clusters of capacitors and resistors may be missing from the board surface. Design trends and cost factors are beginning to re-locate passive components to more efficient locations, usually within the layers of the board or even within the top layers of the chip itself.

Since the 1960s it has been possible to create capacitors and resistors during the final stages of chip manufacture, and various manufacturers have been doing so to meet the specific needs of their customers. The on-chip capacitors are not really replacements for surface-mount capacitors because their values are necessarily much lower – less than 10pF on-chip, for example, as opposed to 10,000-plus picofarads for the surface-mounted variety. But where the lower value is 'fit for purpose', or acceptable, the on-chip design may be used.

Building passive components on the chip itself isn't feasible for all applications. Consider, for example, the large number of chips where the area of the chip is shrinking in relation to the performance — chip-scale packages are a highly popular example. In many such chips, there is simply no space left on the chip for passives. Surface area may be wanted for solder ball attach purposes.

Aside from situations where a manufacturer puts a capacitor onto a chip to meet a specific customer's needs, passives that are not surface-mounted are mostly winding up embedded between the layers of the board. At Berlin's Fraunhofer Institute, Oswin Ehrmann and his colleagues have been developing forward-looking methods of incorporating resistors – but not, as you might expect, printed resistors. Instead, they are using discrete resistors some 70 microns thick. The use of discrete embedded components makes it possible for the user to select tolerance (e.g. ±15%) before the resistor is embedded.

"It increases cost a little because it is one more mask layer, one more metal layer," Ehrmann observes. "The normal redistribution layer has four masks, and now we have five masks."

Ehrmann's group has performed full prototyping of their method, which is now ready for production. Will it save money in the right application? "Yes, you can save money," says Ehrmann, "because you can avoid placing six or seven resistors around the die." In high-volume production, where a lot of pull-up, pull-down resistors are needed, the cost savings are especially dramatic.

Fraunhofer — along with many other firms and institutes — is also investigating other ways to place both active and passive components within the layers of the PC board. One of the benefits is the superb protection that components receive from shock and vibration, a concern with military users as well as with many commercial manufacturers — think of a mobile phone dropped onto a hard surface, for example.

> *"They [embedded passive components] present some significant issues in manufacturing, particularly when one of those parts that is embedded fails"* **Thilo Sack, principal engineer, Celestica**

There are a couple of obvious drawbacks in embedding passive components in the board. One is heat dispersal; unless a method is designed for adequate heat transfer, the component's power rating needs to be downgraded, since it has no exposure to air. More important from a cost-of-assembly viewpoint is the relative impossibility of rework. A surface-mounted capacitor or resistor can be taken off and replaced if it is defective, but replacement of an embedded passive hardly seems feasible.

Actually, rework might be possible in some applications. Thilo Sack, principal engineer at Celestica, once worked on a high-end product that used embedded passives. "I can tell you that it did present some significant issues in manufacturing, particularly when one of those parts that was embedded failed."

"Keep in mind that the part that's embedded is connected to other parts of the circuit, so it's going to have some capacitance effect to the whole circuit. So, in order to isolate that component, you typically can't just go in and drill around that embedded part. You have to try to find points on the printed circuit board where you can physically contain that part as part of the circuit, and then figure out how to reconstruct that circuit with some components on the top of the board in order to salvage the board."

This was of course an unusual product, having high intrinsic value. Gail Auyeung, global component quality engineer at Celestica, notes that they currently see few products that use embedded passives, and that most of the ones they do see are prototypes from firms that want to be ready for the embedding of passives when the trend takes off. Right now only 1% to 2% of passives are embedded.

The potential, though, is far higher than this. Sack points out that the NEMI roadmap suggests that up to 40% of passives could be embedded. The reasoning goes like this: about 60% of the capacitors in a typical application have a capacitance above 0.1nF, but the other 40% have a capacitance below 0.1nF, meaning that they could be — if costs were not a factor — embedded in the board.

While the 40% level may seem fanciful, embedding passives may pay off in ways that are not immediately obvious. "In some cases, people are looking at a bare board," explains Auyeung. "They ask themselves, 'How much will it cost to embed passives in it?' — but they don't look at assembly." One other possibility is that second-side assembly might be eliminated completely.

"In lead-free, no longer does your board have to go through two heat cycles. In other words, if you look at the whole life-cycle costs, embedding might actually make the entire board cheaper."

Probably the embeddable resistor material with the longest history of availability is Ohmega's OhmegaPly material. More recently Ohmega collaborated with Oak-Mitsui to make a two-layer embeddable "sandwich" to serve as both resistors and capacitors. Ohmega vice president Bruce Mahler notes that the combination material effectively reduces costs and has proven to be robust. OhmegaPly by itself is probably the most widely used embeddable material.

"One of the issues that a lot of designers face, and that we have to deal with, is number of layers on a board," says Mahler. "The thickness the board gets, how many layers they have to put into a board and there's a certain maximum height they have to live with. So anything they can do to reduce the layer count, which ultimately will reduce cost of design and make it easier for them, makes sense."

"So the idea of combining the two technologies, of putting the OhmegaPly particularly on a voltage plane which acts as a capacitor plate for distributive capacitance material and having that RC network essentially together, the resistor termination on that capacitive plane for that distributive capacitance and by-pass type reasons, made a lot of sense," he continued.

Mahler, who is in a good position to know, thinks that embedded resistors may eventually take about 5% of the market — perhaps up to 10%. Embedded capacitors, he feels, may take from 10% to 15% of the market. Why not more? Because surface-mount resistors and capacitors have become so inexpensive that they will still be the component of choice for many applications.

One of the cost-sensitive problems with embedded passives is the matter of component tolerance. A given resistor, say 10Ω, can be required as a ±1% or anywhere up to ±25% tolerance. This tolerance requirement impacts on the manufacturing yield, hence cost. Conventionally, resistors can be individually trimmed with a laser, but trimming introduces another process step and adds costs. Similar arguments apply to on-chip capacitors too.

But there may be other, less expensive ways. "Right now we use a probe card [for trimming]," explains senior product development manager Frank Durso at MacDermid. "So you have to make a probe card for each circuit or for each part of the circuit, depending on how big the board is.

"But one of our guys is playing around with software, where you can trim resistors to a reasonable area without the use of a probe card." Other companies are researching their own methods, and it appears likely that the added cost represented by trimming may be significantly reduced.

Trimming passives to obtain a specific function as against a specific resistor/capacitor value does require knowledge of the network's application. This can be different for various applications. Thus, software controlled functional trimming not only adds cost but also limits numbers to that application.

Dave Sawoska, senior research chemist at MacDermid, thinks that embedded passives will be widely used in a few years, and that the push will in large part come from OEMs. The IPC, he notes, is in the process of writing the design grades and test specifications that will be needed for embedded resistors and capacitors.

"They're about 80% to 90% through writing the specifications," he reports. "Up until now everybody pretty much did their own thing, but the IPC is now trying to formalise testing, so that everybody would test to that sheet and you'd have comparable data system to system, line to line things of that nature."

Deterministic Communication Methods for Distributed Systems

Rob Sims, Applications Engineer, and **Tristan Jones**, Technical Marketing Engineer from National Instruments in the UK and Ireland present a case for deterministic Ethernet and how to implement it in the simplest way

During the past 15 years there has been a revolution in communications for the consumer. Through mobile phones, e-mail, the Internet and voice over IP (VoIP) people can stay in touch and obtain the information they require where and when they need it.

The communication revolution has also extended into the lives of engineers — the growth of Ethernet has greatly improved the capability and integration of networked measurements, remote monitoring and distributed control applications. In both manufacturing and test, engineers continue to find new ways to take advantage of PC-based technology to build individual test stations or machines. These measurement and control systems utilise Ethernet to connect to management, data and quality systems.

Distributed systems such as these can deliver a level of flexibility and efficiency to machines or processes that may not be so easily achieved with a centralised system. However, the distribution of a system can also result in communication latency. With nodes being physically separated, engineers must take into account the time it takes to transfer data between nodes. Furthermore, when the latency is indeterminable, nodes on the network must be prepared to wait on data to be sent or received.

What makes standard Ethernet non-deterministic?

The unknown latency characteristic of Ethernet networks is inherent in the design of the Ethernet standard. For the transmission of data by many devices on a single network, Ethernet uses the Carrier Sense Multiple Access, with Collision Detection (CSMA/CD) mechanism. When multiple nodes on an Ethernet network wish to transmit data, each node must wait until the network is silent, in other words, no other device is transmitting, to begin its own transmission. However, it is statistically possible for a situation to arise in which multiple devices simultaneously attempt transmission, known as a network collision. In order to overcome this, the devices should detect that a collision has occurred and then wait for a random period of time before trying to retransmit.

High-level protocols, such as the commonly used Transmission Control Protocol (TCP), introduce additional handshaking to ensure the data sent across the network has been received. Senders of TCP data wait until the receiver sends a positive acknowledgement to confirm receipt of data. If confirmation is not received within a certain timeout period, then the data is retransmitted. Flow control methods such as TCP, when coupled with the collision detection mechanism contribute to a timing uncertainty in Ethernet networks. Other factors such as the communication protocol used, aggregate network traffic, the number of Ethernet devices and available bandwidth also contribute to this timing uncertainty, which makes standard Ethernet inherently non-deterministic.

In many cases, engineers can compensate for these timing limitations by implementing techniques such as buffering to compensate for the inconsistent latencies. For example, a server on a busy network may need to stream video to a client machine. The client will often take several seconds of video and place it into a buffer so video playback is continuous, while the data it receives from the server may come in separate short, fast bursts.

The need for deterministic networking

While buffering methods may be suitable for applications such as media streaming, they may not always be appropriate for more specialised, or advanced, distributed applications. For example, a fly-by-wire aircraft simulation may involve a flight control simulator passing a new angle value to the rudder control simulator. In this type of distributed system, it is imperative that the rudder simulator receives the latest angle parameter within a fixed period of time or the response of the rudder will be late and the flight control system will fail. In a case such as this, buffering the data will not alleviate the issue, because buffered data is effectively useless in a dynamic system like aircraft flight controls.

Although an extreme application, the fly-by-wire simulator demonstrates some of the challenges associated with distributed systems. Industrial control systems have similar requirements when I/O and processing is distributed among nodes. In order to meet the requirements of such distributed control applications, the communication network itself must have a real-time (deterministic) response.

Standard Ethernet networks do not offer an adequate solution for deterministic communication; engineers often resolve this issue with bespoke deterministic buses, such as the controller area network (CAN) bus for automotive applications and MIL-STD-1553 for military applications. In the industrial arena, widely adopted buses, such as DeviceNet and PROFIBUS, are utilised in applications by control engineers. Other solutions include expensive reflective memory networks, with fixed traffic patterns, on token ring networks. The network infrastructures of these deterministic buses are generally vertical in use and design. For example, the CAN bus is designed for automotive networks, while DeviceNet is designed for industrial sensor networks. This tends to limit the scope of these applications to specific industry areas.

Despite these deterministic transfer solutions being available and the technical challenges involved in achieving real-time Ethernet networks, there is a growing trend toward using Ethernet to solve these applications. Several factors drive this trend: firstly, Ethernet ports and networks are widespread. As more devices are shipped with Ethernet ports, there is increased potential to connect downstream activities, such as a sorting machine, to upstream activities, such as inventory management applications. Such a combination can increase productivity and reduce the cost of large systems.

Secondly, when compared to specific buses for vertical application areas, such as the MIL-STD-1553 and CAN, Ethernet offers a relatively low-cost alternative. Thirdly, many existing solutions currently have bandwidth limitations which can be solved by Ethernet. For instance, the maximum transfer rate of 100Mbit Ethernet is close to 200 times that of DeviceNet.

These factors have driven development leading to the arrival of several real-time Ethernet solutions in the marketplace. These solutions range from soft real-time protocols, such as Ethernet/IP, to SERCOS III, a hard real-time Ethernet protocol for distributed motion control. Furthermore, the arrival of the IEEE 1588 precision time protocol (PTP) has made it feasible to use Ethernet for synchronised, distributed applications. IEEE 1588 provides a standard method to synchronise devices on a network with sub-microsecond precision.

Overcoming non-deterministic Ethernet

With any deterministic network it is necessary that strict timing rules be put in place by the system governing the network. These rules can be implemented in a number of ways to achieve the desired outcome, although they usually have two common elements. Firstly, all components of the network synchronise their time to a master clock. This master clock is not established by a specialist piece of hardware, but simply by one of the nodes on the network designated as the master of the system. The IEEE 1588 protocol, for example, can establish the clock synchronisation for a deterministic Ethernet network. The second element in setting up a deterministic Ethernet network is to configure the network nodes such that collisions do not occur. This can be done by creating a schedule that determines when each node on the network transmits data during each network cycle. To create such a schedule, the system must know the amount of data to be transferred in order to reserve the appropriate amount of time needed to send the data across the network.

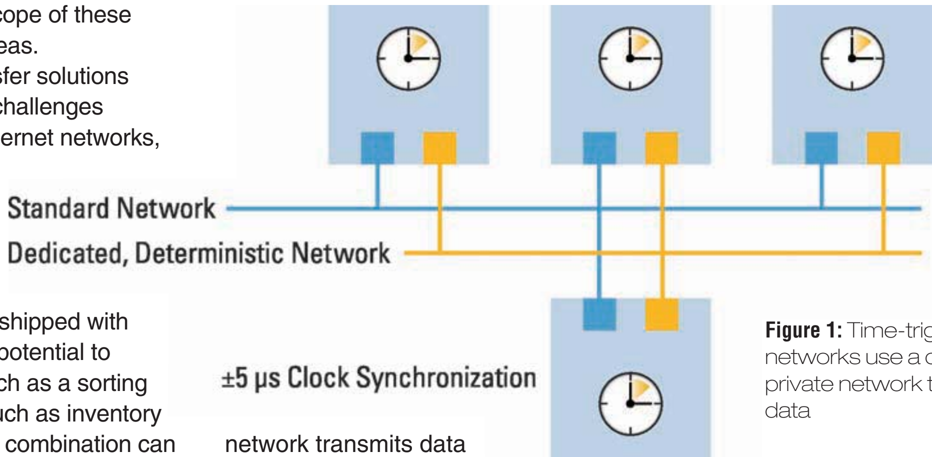


Figure 1: Time-triggered networks use a dedicated private network to transfer data

One way of implementing deterministic Ethernet, using commercial off the shelf (COTS) hardware is the time-triggered network, part of the National Instruments LabVIEW 8 Real-Time Module. This technology is an example of how to achieve deterministic transfer of data across an Ethernet network. The time-triggered network allows two or more PC or PXI targets to transfer data deterministically across a private network using COTS interfaces. As shown in **Figure 1**, each PC is

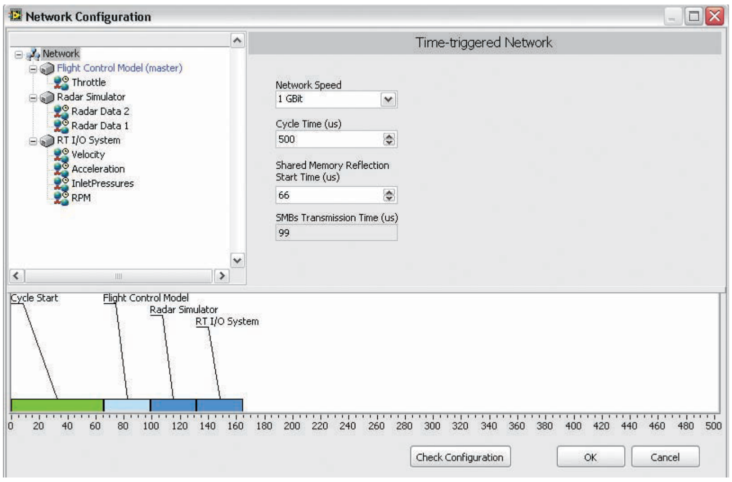


Figure 2: Shared memory blocks share and update data between nodes

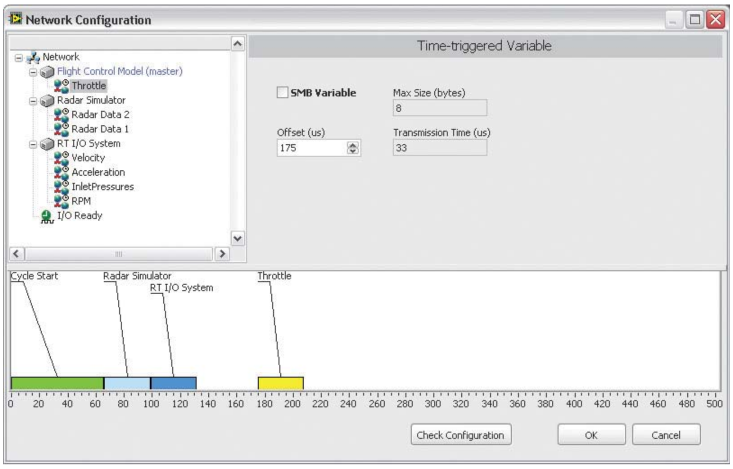


Figure 3: Dedicated slot variables send data across the network at scheduled times in each network cycle

connected to both a time-triggered network for deterministic communication and a public network for normal network traffic and communication with non real-time nodes. This dual network offers not only deterministic data transfer, but also a level of redundancy to communications.

Other deterministic Ethernet protocols, such as ETHERNET PowerLink, split the network cycle time so that regular Internet traffic, such as TCP/IP, can occur after deterministically scheduled packets are sent and received. This method requires less wiring between real-time nodes, but typically requires a gateway to schedule traffic coming from outside the real-time network.

National Instruments time-triggered network implements the previously discussed master clock synchronisation and collision prevention. One network node is designated as the master node, while all other nodes are slaves. The period of each network cycle is also configured and can be between 100μs and 100ms. At the start of each cycle, the master node sends a cycle start packet to the slave nodes. Once the start cycle packet has ended, other network transfers can be scheduled.

One method of transferring data across a deterministic Ethernet network is through a shared memory system. In such a system all nodes on the network allocate a block of memory for each node on the network, including itself. Shared memory blocks take all the data from one node and send it to all other nodes as one packet. This data may often include several shared variables. The configuration of National Instruments shared memory deterministic communication is shown in **Figure 2**.

An alternate method of transferring data is using a dedicated slot method. When using this method, a user explicitly schedules when each data item will be transferred during the network cycle. The advantage is that a control loop can be closed during a single network cycle.

The practical implementation of the system can perform acquisition and actuation when the network is busy. For example, a distributed motion controller contains a Controller node and an I/O System node. In this example, the deterministic Ethernet requires time during the network cycle to maintain clock synchronisation. During this period, the I/O node performs its I/O operation. The I/O node then sends feedback across the network to the controller, which processes and transmits an output back across the network before the network cycle completes.

Engineers can use this method for closing any type of control loop across the network, allowing a decentralised system for control that reduces overall wiring and complexity. The timing diagram for dedicated slot communication on National Instruments time-triggered networks is shown in **Figure 3**.

A distributed system can often also use multiple processors to complete an application. These systems can have the same or different architectures – for example the PC, embedded microprocessors, FPGAs, PDAs or DSPs.

Given the variety of deterministic communication methods available, coupled with the tiers of setup and programming involved in some programming languages, the incorporation of deterministic communications into modern distributed systems, although advantageous, can often lead to increased system development times.

High level graphical programming tools, such as National Instruments LabVIEW 8, provide technologies and tools to meet these challenges for building distributed systems. Within this graphical programming environment, it is possible to program all nodes of a distributed system – both host and hardware targets of varying architectures. Engineers can view, edit, run and debug the code running on any target in the distributed system, all from the LabVIEW 8 Project. A shared variable system makes it easy to pass data among systems — even real-time systems — without impacting performance.

Furthermore, the added ability to implement deterministic Ethernet in order to synchronise distributed devices and systems is a significant advantage. With systems based on this technology, engineers can get inside the device and program the inner workings for much more flexible solutions than traditional instrument or PLC approaches allow.

Where do we go from here?

While standard Ethernet has already permeated many parts of the business and industrial worlds, deterministic Ethernet will undoubtedly expand the reach of the CAT-5 cable even further. With reduced cost and readily available hardware for deterministic Ethernet, engineers can now implement deterministic communication in their systems by leveraging Ethernet controllers that come as standard on many modern devices. Such controllers are not only lower cost than alternatives such as DeviceNet or CAN, but can also provide equal, if not greater, data transfer rates. In addition, deterministic Ethernet does not require bespoke hardware, enabling the widespread applications already mentioned, including: fly-by-wire and distributed motion control systems, among others such as machine condition monitoring or liquid flow control.

With such a wide range of possible applications, the use of distributed systems has become an essential solution for engineers. Until now, the task of establishing deterministic communications between distributed nodes has been cost-prohibitive in terms of both time and money. With the development of deterministic Ethernet technology, engineers and scientists now have the option of greatly reducing the cost of deterministic communication, opening up distributed systems as a valid and competitive solution.

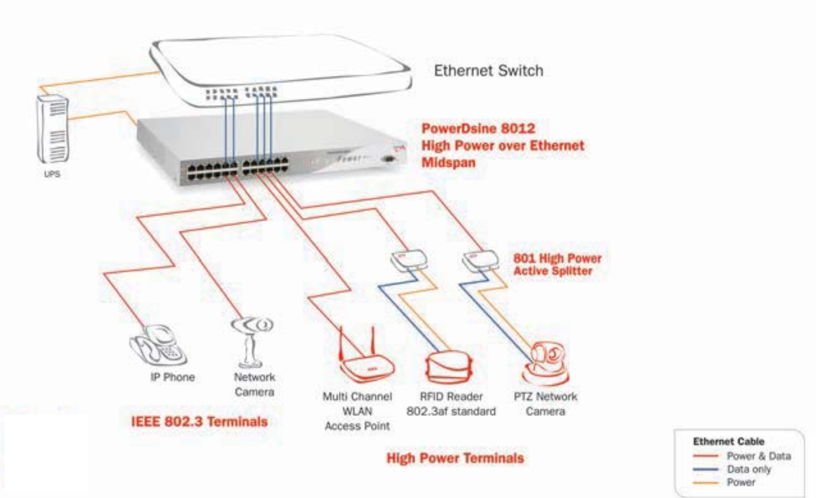
Power over Ethernet: How High Can You Go?

Daniel Feldman – Senior Product Manager at PowerDsine presents the roadmap of the IEEE 802.03 standard

When the IEEE created the IEEE802.3af task force, which pursued the addition of power transmission to the venerable IEEE802.3 standard, the IT world was a different place. In 1999, Cat3 was still considered to be an abundant connectivity option to the desktop, enterprise IP telephony did not really exist and WLAN APs (access points) were nowhere to be seen.

Since then (and since the approval of IEEE802.3af in 2003) this has changed. The cabling infrastructure was upgraded to Cat5 and above, while IP telephony has become a part or in the plans of every enterprise. WLAN is found everywhere. These, together with network cameras, were the main applications enabled by the original Power over Ethernet (PoE) standard. And for the most part, these applications can do pretty well with the power limit imposed by IEEE802.3af, 12.95W.

However, the popularisation of these applications triggered the inventiveness of developers into creating more power hungry derivative devices, such as video IP phones, multi-channel WLAN access points (like the ones in the IEEE802.11n upcoming MIMO standard) and pan-tilt-zoom IP cameras. All these applications require typically more than 13W, normally between 13W and 30W. Going forward, laptops and even desktops could be powered too.



The High Power over Ethernet Midspan delivers up to 39W power over standard Ethernet infrastructure

Enhancing Power over Ethernet

With these new high-power applications in mind, in December 2004, the IEEE802 created a study group called PoEPlus, which studied the market needs and possible technical solutions to address these, still maintaining backward compatibility with IEEE802.3af.

As a result, the group laid out a set of objectives, approved in September 2005, as binding for the IEEE802.3at Power over Ethernet Enhancements task force:

- 802.3at should operate on Class D and higher infrastructure, unlike 802.3af, that had to take into account the Cat3 limitations
- 802.3at should follow the power safety rules and limitations pertinent to 802.3af
- A high power 802.3at PSE must be backward compatible with 802.3af, being able to power both 802.3af and high power 802.3at powered devices (PDs)
- 802.3at should provide the maximum power to PDs as allowed within practical limits
- 802.3at should provide at least 30W to PDs
- 802.3at PDs, when connected to a legacy 802.3af PSE, will provide the user an indication that an 802.3at PSE is required
- 802.3at PDs with power levels up to 12.95W shall be supported by legacy 802.3af PSE
- Research the operation of midspans for 1000BASE-T
- Research the operation of midspans and endspans for 10GBASE-T

Cabling and high power

The assumption of using Class D cables that are Cat5 and up, and not Cat3 cabling, is a crucial one as Cat5 cables have by default eight wires, twice the amount of the wires present at Cat3 cables.

This means that without any modification in the current or voltage parameters of the IEEE802.3af, it should be straightforward to get twice the power.

But the advantages don't stop here: Cat5 cables have only 62.5% of the resistance found in Cat3 cables and, therefore, dissipate proportionally less power for any given current.

Even though the final current level allowed by IEEE802.3at has not been yet defined, the task force considers cabling temperature rise as the key limiting factor for the specification. There is existing large 60ºC grade cabling installation. Using high current level, which can cause high temperature rise, may result in legal and technical issues. This is particularly of importance in the worst case installation scenario when a bundle of cables is used, as the ambient temperature and the internal cable temperature will significantly differ. This means that the current flowing through all eight wires, in big bundles of cables, should be limited to 10ºC. Some cabling manufacturers recommend to further decrease the temperature rise to a maximum of 5ºC for having adequate design margin. There are other views who state that temperature rise more than 1ºC is not possible in 60ºC grade cables, which makes the ISO/IEC 175mA/conductor specification as the current valid specification. The group is looking for test results and manufacturers input for clarifying this issue and moving forward.

Voltage levels

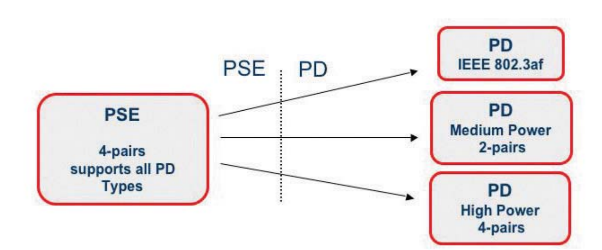
Raising the current is not the only key of getting more power through the existing infrastructure. Increasing the minimum voltage is also possible. When the IEEE802.3af standard was written, several companies believed that it was important to have support for battery-based powering. This is the source of the minimum 44V PSE output. Based on the experience acquired with IEEE802.3af installations on the field, this seems to be a common limitation and one that can be overcome by boosting the battery voltage.

Therefore, the IEEE802.3at task force intends to raise the minimum PSE output voltage from 44V to ~51V, increasing the power available to the PD.

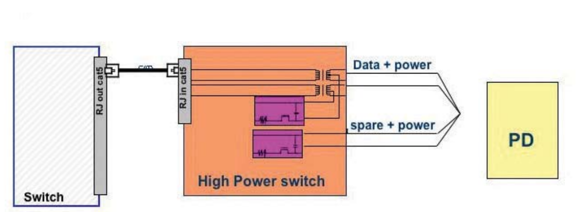
With Cat5 cabling, an undefined current and a higher voltage level, one question remains: is IEEE802.3at a synonym for always using all of the eight wires available to feed the PDs, or is there a place for rising current and voltage but use only four wires?

While, clearly, using the eight wires gives more power (double the power), depending on the final maximum current determined by the IEE802.3at task force, four-wire solutions could be enough to power many applications. The group believes that the decision point is 30W: if it is possible to transmit at least 30W over four wires, this medium power solution should be an option in the new standard.

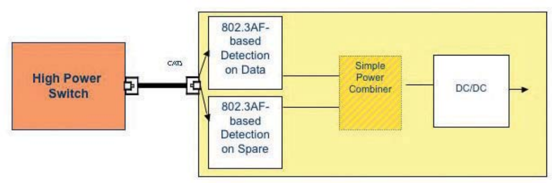
In any case, eight wires are required to provide as much power as feasible to the PD.



PSE/PD topology - IEEE agreement



Pre-standard IEEE802.3at PSE



Pre-standard IEEE802.3at PD

Backward compatibility

Interoperability with existing hardware is key for the success of any standard, and this not different with IEEE802.3at. Backward compatibility with IEEE802.3af PSEs and PDs is a mandatory requirement. If from the IEEE802.3at PSE perspective this seems a relatively simple task, as the new IEEE802.3at PSE would be detecting an existing IEEE802.3af PD, the same cannot be said about IEEE802.3at PDs. There are two possible interoperability scenarios envisaged by the IEEE802.3at task force:

a) IEEE802.3at PD can work in a low power mode: the IEEE802.3at PD should be able to identify the PSE to which it is connected as an IEEE802.3af one and automatically operate in the low power consumption mode.

b) IEEE802.3at PD requires more than 12.95W to operate: the IEEE802.3at PD must actively indicate to the end-user that it is connected to a legacy IEEE802.3af PSE that cannot power it.

Another aspect of the IEEE802.3at specification is related to data: can it operate with IEEE802.3an 10Gbit/s Ethernet? How about Gigabit Ethernet and midspans?

The group has committed to study how raising the power influences the new IEEE802.3an PHY.

Gigabit midspans, which were not precluded by IEEE802.3af but were out of scope of the specification, have now become very popular in the marketplace and are expected to be formally addressed by the new IEEE802.3at standard.

Classification

Another important aspect is the method of classification. IEEE802.3af provides five classes (0 to 4), which translate into three PSE power allocation values: 4.0 Watts, 7.0 Watts or 15.4 Watts.

This scheme, which is not efficient even for IEEE802.3af applications (every WLAN access point that requires 7.1 Watts receives a 15.4 Watts allocation, more than 50% waste), is clearly not fit for higher power applications.

One of the goals of the IEEE802.3at task force is therefore to increase the granularity of the classification method, leaving also place for future enhancements. This must be done in a backward compatible way, so IEEE802.3af PDs can still be classified by IEEE802.3at PSEs, and IEEE802.3af PSEs don't wrongly classify IEEE802.3at PDs.

Another way to make the standard more user-friendly to systems with power management is to add provisions so that PDs power requirements can be read via network management for even higher granularity and, also, to support ongoing changes in power consumption requirements. This is planned to be achieved via the definition of a PD MIB, in addition to the existing PSE MIB, specified in IETF's RFC3621.

Summary

Power over Ethernet is about to change in ways that most of us cannot imagine. The increase in the power available to a PD from 12.95 Watts to 40, 50 or even 60 Watts will transform the RJ45 connector in the first universal power plug. With the IEEE802.3at activities expected to be finished in 2007, and pre-standard equipment such as PowerDsine's PD8012 already available, High Power over Ethernet is closer to your desk than you think.

Modular Baseband Design – Enabling a Low Cost, Reusable Wireless Infrastructure

Bertan Tezcan, Senior Systems Architect from the Systems Technology Group at IDT and **Bill Beane**, Senior Product Manager from the Flow-Control Management Division at IDT analyse various designs for basestations

Over the last decade, wireless basestation designers have made major strides in their constant struggle to reduce cost, power and footprint. For these designers the goal for 3G basestation development is simple — to achieve ten times the bandwidth at one tenth the cost.

The processing power required to handle baseband algorithms continues to increase with new wireless protocols. As shown in **Figure 1**, conventional digital

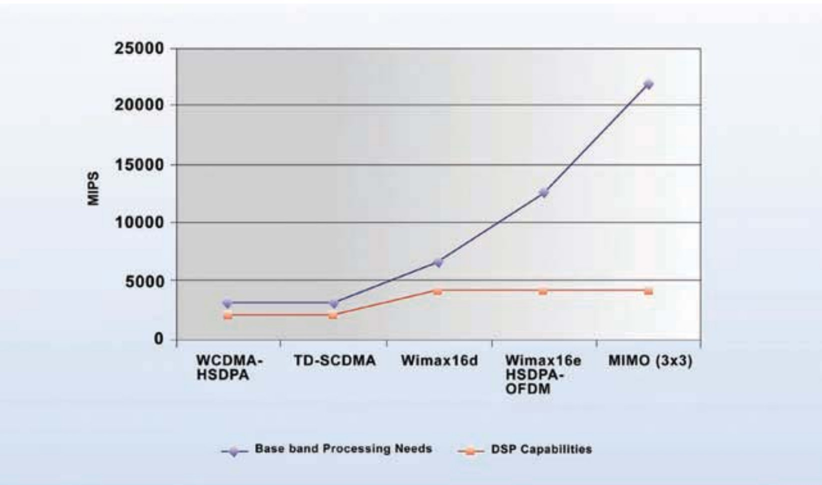


Figure 1: MIPS requirements for different wireless protocols

signal processors (DSPs) may not have enough MIPS power to perform baseband processing, resulting in the need for hardware acceleration to supplement the DSPs. A typical architecture may consist of a cluster of DSPs and hardware accelerator blocks on the baseband card, where multiple channels are processed.

Today's basestation typically relies on a sequential processing scheme, and every block and processing is time aligned. The architecture often looks as in **Figure 2**. One chip-rate processor (CRP) interfaces to the time-sliced backplane and receives "samples" from the RF card.

In CDMA-related systems (such as WCDMA, CDMA2000) samples are converted to 'chips' and, eventually, to symbols before transitioning to the DSP, often via the parallel memory interface. The DSP performs the 'symbol-rate processing' such as error correction and voice/data channel processing.

In orthogonal frequency division multiplexing (OFDM) systems (such as 802.16x, WiMax), the CRP is replaced by the OFDM PHY, which performs synchronisation and FFT before handing symbols to the DSPs. DSPs perform similar operations to the CDMA architecture.

This architecture is not very scalable as ASIC and DSP processing allocations are fixed at the time of design and are tightly coupled with the selection of the hardware. As a result, some DSPs and CRPs might be under-used in some basestations, but this inefficiency is allowed to exist because it is very difficult to shift resources from one processing block to another during run time.

It is also not easy to have the same architecture for pico basestation, micro and macro basestation, as it is a challenge to scale algorithms developed for the CRPs and DSPs in a given application. For a small performance increment, a whole new group of CRPs and DSPs may need to be added.

In some architectures, one of the CRPs interfaces to the backplane (RF card) and the rest of the CRPs talk to the first CRP (uplink card). This requires a different design for the backplane interface CRP, as one cannot replicate the same design to the subordinate CRPs without reducing their effectiveness and, thus, decreasing the return on investment for developing the CRPs.

The memory interface between the CRPs and DSPs can also be a problem for the system software. The bi-directional nature of a standard memory interface can make it harder to fully utilise this interconnect. Usually, baseband algorithms are sensitive to non-deterministic delay, which may be introduced using a bi-directional interface.

Emerging standards to the rescue

In recent years, the industry has thrown its support behind a number of standards-based efforts to promote modularity at the system and network levels, allowing for cost-effective reuse of engineering efforts and scalable architectures.

One of the best examples of this trend is the Open Basestation Architecture Initiative (OBSAI). OBSAI defines modular basestation architecture with standardised interfaces between each module in the basestations.

Six months after OBSAI was launched, a competing standard, Common Public Radio Interface (CPRI) was announced. Far simpler than OBSAI, CPRI focuses on the UMTS basestation by dividing it into a RF and control block connected via a standard digital interface.

To address the needs of network equipment manufacturers and service providers at the chassis level, the PCI Industrial Computer Manufacturers Group (PCI-MG) has defined a standard chassis form-factor called the Advanced Telecom Computing Architecture (ATCA).

DSP blades in wireless basestation applications need highly simplified, high-speed interconnects for data transfer and protocol management. These computationally-intense embedded applications require the system to quickly move data between signal processors in a tightly-coupled DSP farm. The serial RapidIO (sRIO) specification was developed as an open standard and was expressly designed to address the needs of high-performance embedded systems.

The sRIO standard complements the modularity benefits that standards like OBSAI, CPRI and ATCA bring at the chassis and system levels by extending those advantages to the board level. Neither OBSAI nor CPRI define the line-card interface in a basestation design.

Moreover, sRIO's highly tuned support for DSP clusters allows equipment designers to develop very flexible and scaleable architectures in a cost-efficient manner that simply cannot be replicated in FPGA or ASIC-based designs. For example, using sRIO, a basestation designer can build a DSP-intensive system for macro cell applications, allowing the rapid deployment of new technology to support wide areas of coverage and then reuse much of the original design in scaled-down solutions for micro or pico-cellular environments that deliver the desired saturation and density in the most cost-effective manner.

Most importantly, sRIO simplifies inter-processor communications by integrating control and data traffic, offloading simple and time-consuming tasks from the processor, and differentiating between high- and low-priority data traffic. sRIO is also one of the most efficient protocols in terms of packet overhead and throughput.

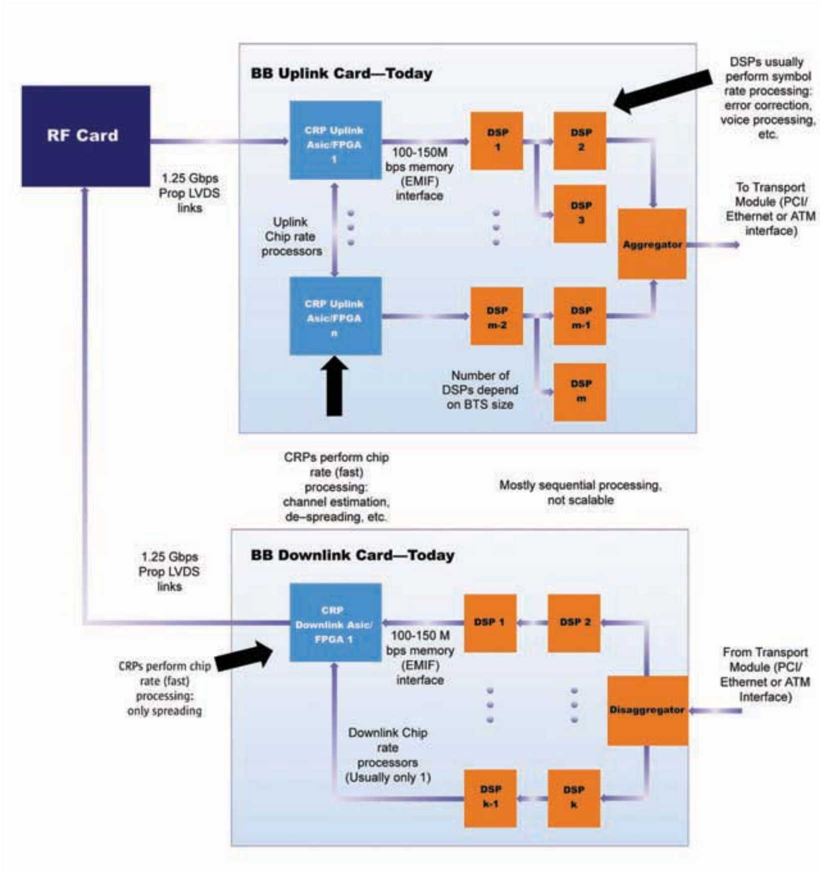


Figure 2: Today's typical baseband card architecture

Basestation development

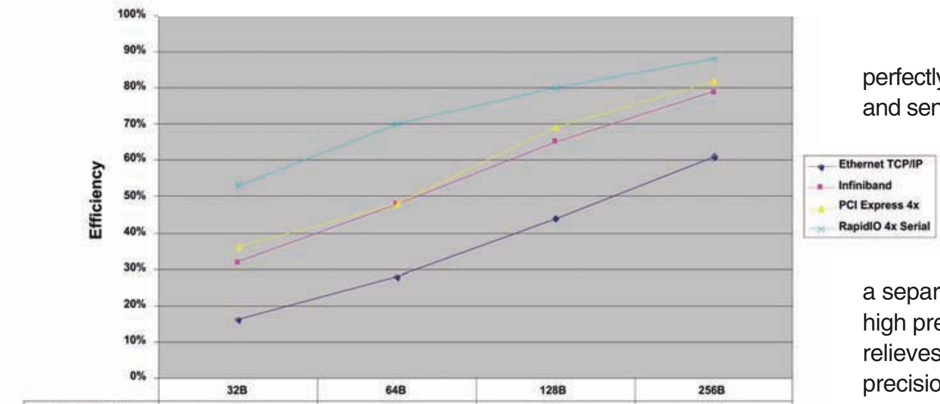
The next question is: How do we put all of these together for basestation development? What is missing to get a complete baseband card design?

Before looking into next-generation architectures, let's look at the algorithm-protocol partitioning for the basestations.

The light blue blocks are mathematical operations needed for CDMA based (UMTS, CDMA2000, etc.) baseband transceiver. An ideal baseband card has a cluster of DSPs and hardware accelerator blocks (or CRPs) in the form of FPGAs or ASICs. **Figure 3** shows partitioning of algorithms to DSP and CRPs. There might be multiple DSPs and CRPs, depending on the processing requirements for the baseband card, therefore, these blocks need to be connected. A similar partition and observation can be made for OFDM-based algorithms.

Serial RIO and CPRI/OBSAI interfaces are also shown in **Figure 3** designated with red lines. Serial RIO is used to connect multiple processing blocks on the baseband card, as shown in **Figure 4**. These interfaces are also shown on **Figure 3** with algorithm partitioning. Note the green blocks next to the interfaces are necessary for data formatting between the interface and algorithms such as sign extension,

Figure 3: Packet efficiency with link and end-point acknowledge



	32B	64B	128B	256B
Ethernet TCP/IP	16%	28%	44%	61%
Infiniband	32%	48%	65%	79%
PCI Express 4x	36%	48%	69%	82%
RapidIO 4x Serial	53%	70%	80%	88%

Packet Size

packetisation of samples/symbols and multiple-packet alignment (from multiple CRPs) before summation. These functions have to be performed by one of the neighbouring devices to this interface. The question is: What is the ideal architecture to handle this partitioning?

Figure 4 shows a close-to-ideal architecture for next-generation baseband cards. A fabric interface component (FIC) translates CPRI/OBSAI to sRIO, and the rest of the baseband card interface is sRIO. The new interfaces are useful for various reasons.

➾ ***Backplane interface (CPRI or OBSAI):*** CPRI or OBSAI RP3 in new systems replaces mostly proprietary parallel TDM interfaces in the old systems. Both CPRI and OBSAI are fast serial interfaces which increase the bandwidth between RF and BB cards and, also, decrease number of connections.

One important design constraint in the BTS is synchronisation. Each RF card has to be synchronised perfectly with all other RF cards in terms of receiving and sending packets, otherwise the whole BTS fails.

Both of the standards help with this problem via different features. Less number of connections means less connections to synchronise as routing of traces is a critical design task. OBSAI sends system clock on a separate trace to all line cards. CPRI embeds a high precision system clock on the interface which relieves basestation designers from routing the high precision system clock separately.

New features also enable "smarter" basestation designs, such as integrated command and data on the same interface. Commands are well protected with CRC. There is no protection for samples as samples are already protected by FEC algorithms on the baseband card. Not having CRC for samples also maximises the bandwidth between RF to baseband card.

➾ ***Line card interface (sRIO):*** On the line card, sRIO actually replaces two separate interfaces with one interface. Control path, which traditionally was on PCI or other slower interfaces, and data path, which traditionally was on parallel memory interface (such as EMIF interface on most DSPs), are collapsed into single sRIO interface. sRIO is also a fast serial interface which enables higher throughput in the system.

sRIO enables processing clusters such as DSP clusters on the baseband card. In old systems, DSP core had to handle the memory interface and, if more than one DSP are connected through this interface, managing that link in DSP software becomes a nightmare. sRIO is an autonomous link that can push data to or pull it from the internal DSP memory. This relieves the software from interface management and enables DSP core to do other "value-add" operations such as algorithms.

Another benefit of sRIO is scalability. sRIO line card switch enables connection of more processing blocks (DSP or CRP) for macro basestation or less for pico basestations. One key point in scalability is software; same software stacks can be reused for different sized basestations. Only an update to routing table in the switch will suffice.

When basestation designers become more comfortable with sRIO, they can also push it to other portions of the system such as RF-baseband card interface, or baseband card to

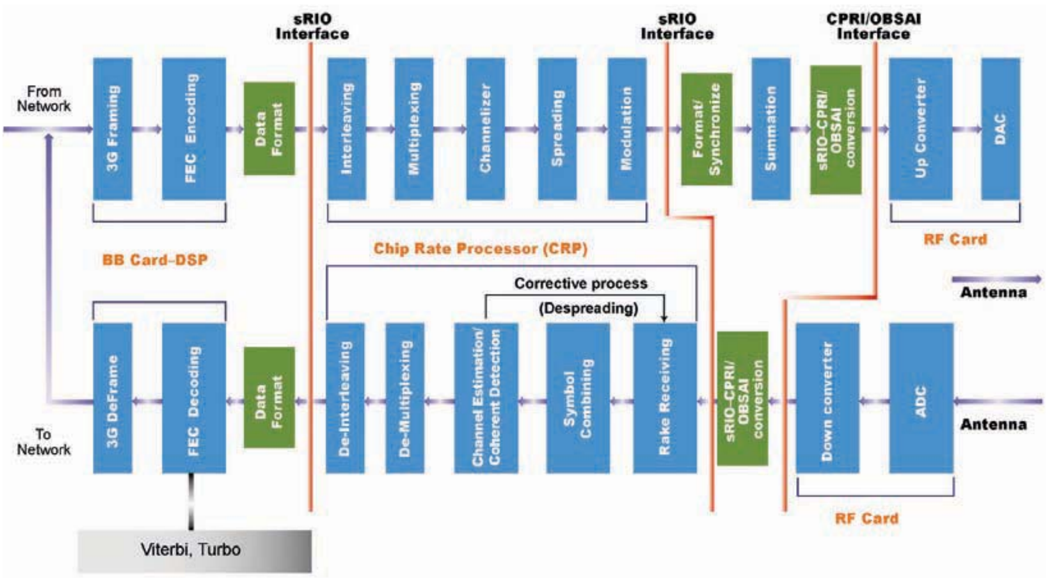


Figure 4: Algorithm-protocol partitioning for CDMA based systems

transport module interface to eliminate other legacy protocols.

➾ ***Chassis (ATCA, AMC):*** ATCA defines many different parameters down to AMC level such as power, cooling, area, etc. This enables different teams of hardware designers to work with these parameters, and all work when combined later. It also enables modularity at the board level: for example, transport module cards from 3G BTS can be reused in WiMax BTS immediately.

There are some special operations needed in baseband card which differentiates it from other DSP cluster line cards. A regular sRIO switch will not be enough to handle special operations needed. There are two distinct traffic flows on the baseband card:

1) Between the FIC and CRPs: High-speed traffic (spread samples) with deterministic timing. Latency on this link needs to be deterministic to support timing requirements in the basestation. Packets are multicast to multiple CRPs on uplink, summed on downlink.
2) Between CRPs and DSPs: Much more flexible in latency, lower bandwidth (symbols) traffic, as well as control and maintenance packets.

A regular sRIO switch needs to be supported with a summer and synchroniser device, which aligns packets from multiple CRPs, sums them on the uplink and multicasts them to CRPs on the uplink.

Different devices and algorithms work on different sample and symbol sizes. For example, CPRI defines sample size ranging from 8 bits to 40 bits. Processors like to work on sample sizes 8, 16 or 32. Also different algorithms want samples in specific order (I-Q together or separate, oversamples together with regular samples or separate, etc.), therefore, these data formatting operations need to be performed in the CRP and the DSP. Depending on selection of DSP and CRP, there are a lot of combinations of these operations that system designer need to be aware of and processors might spend a lot of MIPS to do these operations.

Baseband card sizes can be small to large depending on the system. Micro-TCA form-factor can be close enough for all different cards in the basestation. This will give designers the means to build a large and varied selection of interchangeable modules to meet the needs of telecommunications equipment manufacturers.

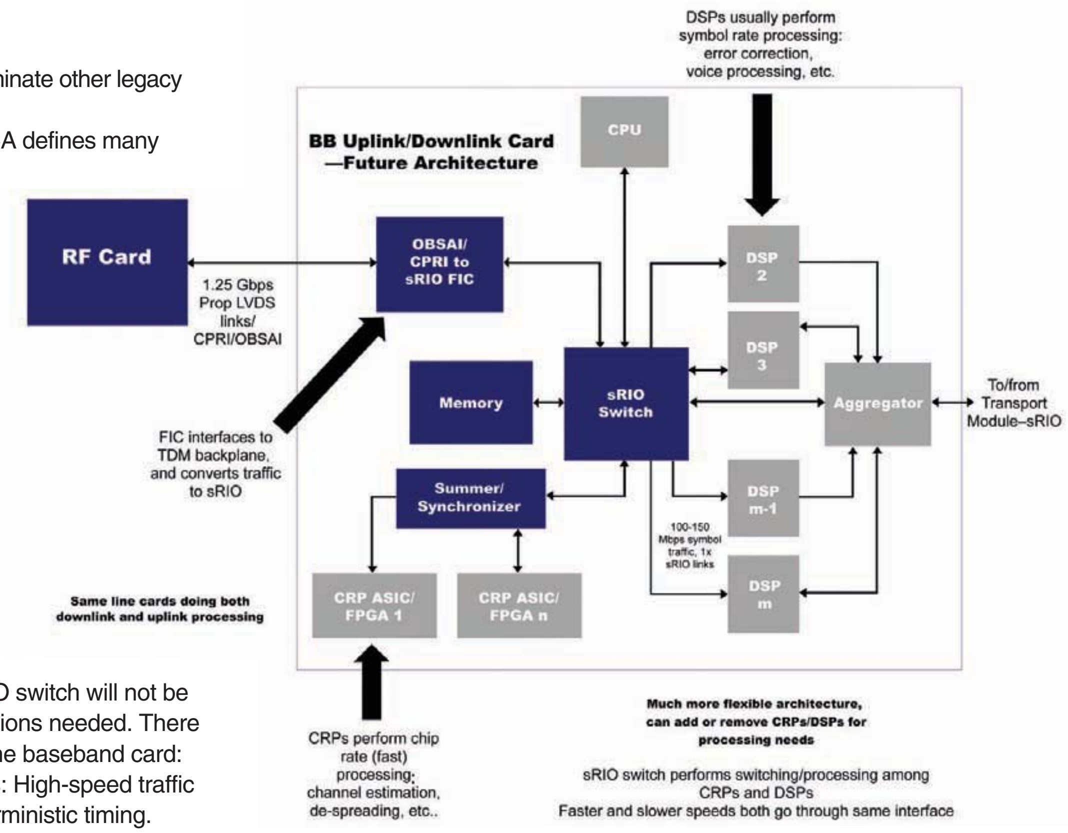


Figure 5: Ideal baseband architecture

This architecture also supports flexible and scaleable basestation designs.

1) **Flexible:** Exchanging CRPs with OFDM PHYs; the same design can be used for both CDMA and OFDM based systems
2) **Scaleable:** Number of CRPs and DSPs can be changed easily to adapt the same design for pico to macro basestations. Traffic and processing power can also be shifted from one device to another at run time since the architecture is not tightly coupled with algorithms anymore.

At a crossroads

The development of 3G wireless networks is at a crossroads. Subscribers expect higher levels of service at lower cost. Yet, the bandwidth and performance requirements implicit in delivering triple-play services will demand increasingly sophisticated and complex basestation designs.

The key to meeting those needs while lowering costs will lie in the adoption of modular, standards-based architectures. By embracing emerging industry standards such as ATCA, OBSAI and CPRI and leveraging the high degree of design flexibility and adaptability in DSP-based arrays using the sRIO interface, basestation designers can deliver high performance next-generation wireless services at a cost structure users will embrace.

CAN can do more than just automotive messaging

Marius van Arkel says that there is no need for detailed knowledge of the CAN protocol, just a simple setup is enough to create CAN-enabled instruments

Despite the impressive capabilities of the CAN protocol, the actual application can be very simple. To a large extent, there is no need for detailed knowledge of the protocol, no need for special software to drive it, no need for a bus master to coordinate bus access, just some hardware and two wires.

The architecture

A possible architecture is shown in **Figure 1**. The main components are:

- Two instruments, connected to a CAN bus,
- A bridge between CAN and an RS232 link,
- A PC to control and display results from the instruments.

This architecture is actually quite comparable to systems found in industry, at the simpler end of the scale.

The instruments chosen to be built are:

- A frequency meter (to generate messages at CAN level and display on the PC),
- An AF signal generator (to control from the PC).

Standard building block

The bridge, frequency meter and AF generator are all built around the Microchip PIC 18F458 IC, which includes a full function CAN controller and is widely available at low cost. Each unit will be supplied with 12V AC and will contain its own power supplies for +5V, +12V and -12V as necessary, to supply the electronics for each unit.

The chip is clocked by a 10MHz crystal. Using the in-built PLL gives a clock frequency of 40MHz and, thus, a basic instruction cycle time of 100ns.

Figure 2 shows the schematic for the power supply, PIC chip, CAN interface and ICSP (In Circuit

CAN Basics

CAN is a peer-to-peer protocol. It relies on the detection of collisions, i.e. near simultaneous attempts by one or more network nodes to access the medium. It has the concept of inherent message priorities. When a collision occurs, the lower priority message transmissions are aborted, while the highest priority message stays unaffected by the collision.

To achieve this, CAN introduces the slightly unusual concept of bits that are dominant or recessive, rather than zero or one. The CAN specification does not define the physical layer (medium). It does stipulate, however, that a dominant bit overrules a recessive one. This could be achieved by transmitting a dominant bit, by placing a voltage on the medium, for example. A recessive bit would then be characterised by the absence of energy.

Like other serial protocols, a message is composed of a series of bits. These are part of a frame that contains various fields, such as message identifier, data length, the data itself and a checksum. The data stream contains clock information that may be extracted to detect the individual bits. A transmitter puts the message on the medium, a receiver monitors what is happening and, when the receiver does not agree with the transmitter, a collision has occurred.

With CAN a dominant bit cannot be corrupted by a recessive one. If two transmitters are sending data simultaneously, nothing will happen until they "disagree". At that point, the transmitter sending the recessive bit can just stop without affecting the other transmission(s).

The CAN protocol includes extensive protection against many possible failure modes to ensure that communication between nodes that function correctly is affected as little as possible. The defences against malfunction are all part of the specification.

Message size and data rates

The data size is restricted to 0-8 bytes per message. The maximum data rate depends on the length of the medium. It may be as high as 1Mbit/s for a 40m segment, but must be decreased for longer segments. For the arbitration to work, all nodes must have the same view of the medium for each transmitted bit. The minimum bit time is thus related to the end-to-end propagation delay of the medium.

A node typically consists of a main processor, a CAN controller and a CAN transceiver. The medium may be implemented as a two wire differential bus, similar to RS422. Dedicated CAN transceiver ICs are available from various manufacturers.

Serial Programming) connection.

The PIC chip can be programmed by removing it from its socket and inserting it in a PIC programmer. It can also be programmed by using an ICSP connector, which leaves the chip in situ but requires special design arrangements. The main considerations here are that the pins RB7/PGD and RB6/PGC are dedicated to the ICSP port, the Vcc pin on the ICSP socket only supplies the PIC chip, the decoupling capacitors are the recommended 100nF and that the Vpp pin is isolated from all other electronics during programming.

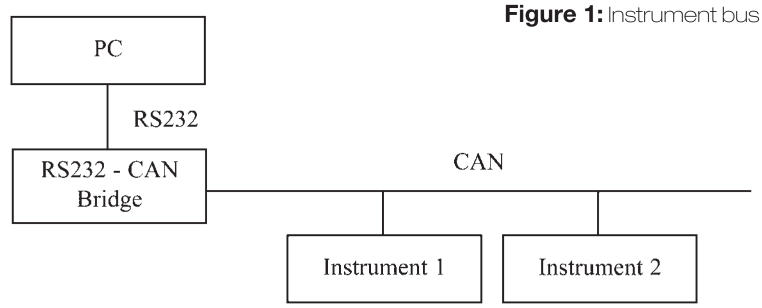


Figure 1: Instrument bus

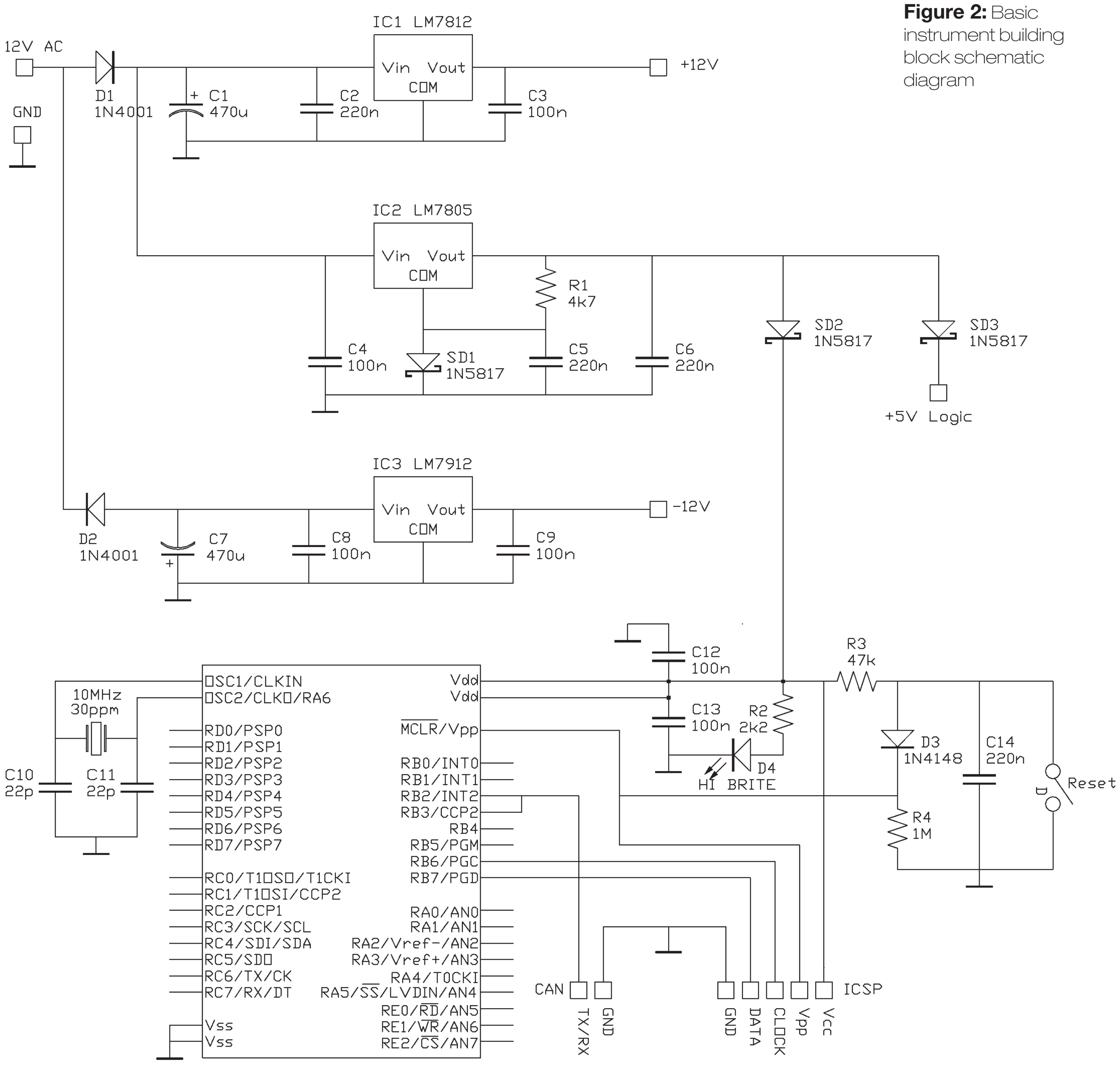


Figure 2: Basic instrument building block schematic diagram

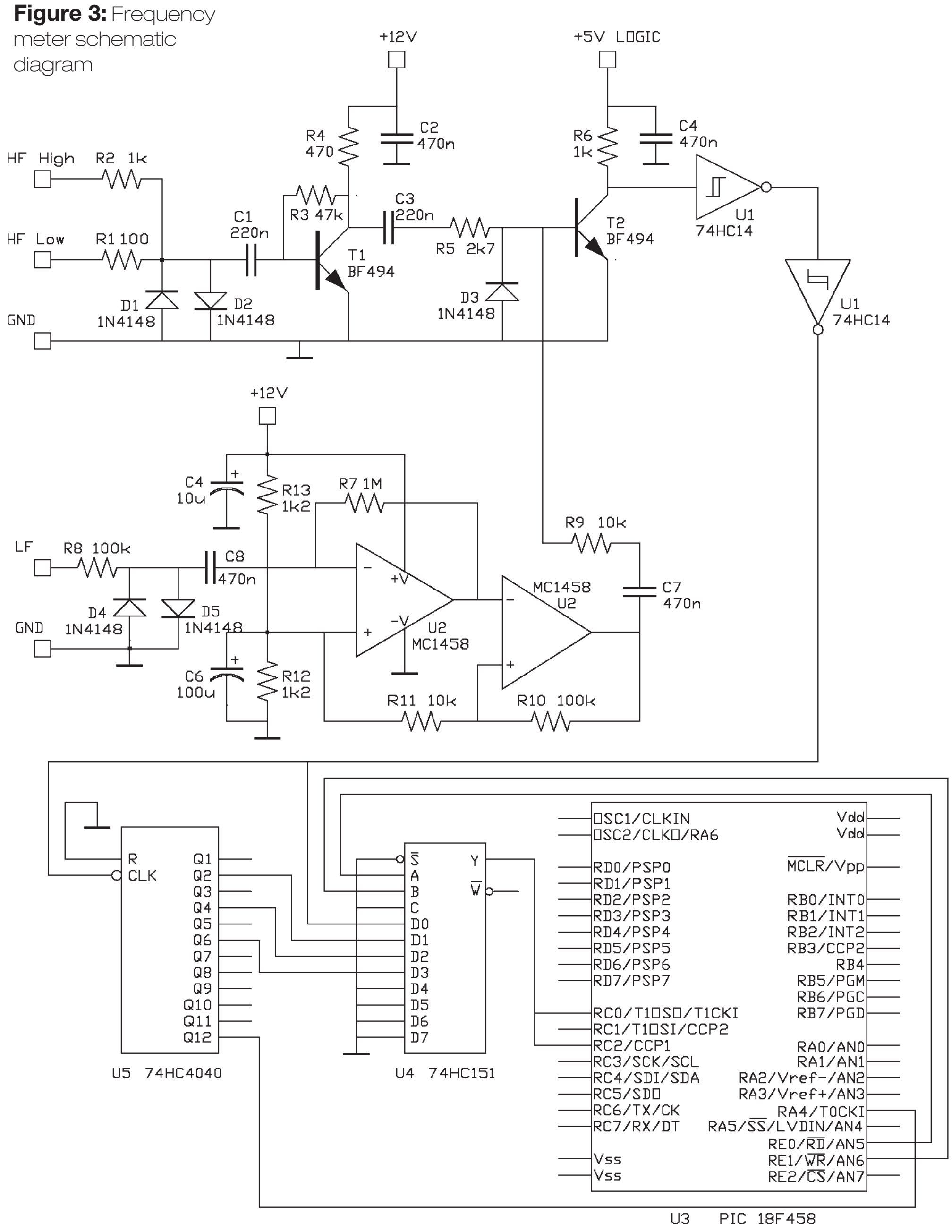


Figure 3: Frequency meter schematic diagram

ensure that it is isolated from the reset circuitry during programming.

CAN network

The 18F458 chip supports a tri-state mode on the transmit pin (RB2/CANTX), in which it is high impedance when recessive and low impedance zero when dominant. The RB3/CANRX pin is connected directly to the transmit pin, illustrating the principle of monitoring the transmission for collision detection purposes.

The CAN network does not work properly with a single unit. Sending a single message from this unit results in the message being repeated continuously. This is because the protocol requires the acknowledgement of each message by at least one other node sending a dominant acknowledgement bit. Failing that, the trans-mission is deemed to have failed and is repeated automatically.

Lack of isolation on the network does mean that it must not be active while one or more nodes are powered down, due to the risk of SCR latch-up via the receive and transmit pins. It would be possible to limit this effect by the inclusion of series resistors. This, however, sev-erely limits the potential number of units on a network. It is simpler to switch all units off at once, considering they are all supplied from the same 12V AC supply.

The +5V power supply actually delivers around 5.3V (5V plus a Shottky diode drop). The Shottky diode in the PIC 5V supply line ensures that it is isolated from the rest of the logic during programming. The Shottky diodes were chosen because their forward voltage drop is less than 0.5V, so that the difference between logic supply and PIC supply is guaranteed to be much less than that. This in turn ensures that no CMOS protection diodes can conduct, which otherwise may happen if a pin is more than 0.5V above Vcc.

The reset pin (MCLR/Vpp) also has a diode to

Frequency meter

This instrument generates a constant stream of messages on the CAN bus, containing measurement results. These are transmitted via the bridge to the PC, where the data is displayed on the VDU, via a small set of programs. The bridge and the PC software will be described later.

The instrument was designed for the frequency range of 10Hz-20MHz, with an input sensitivity of 200mVpp, although 1Vpp is more realistic towards the top end of this range.

Using an inexpensive 10MHz crystal with 30ppm accuracy, the accuracy of the instrument cannot exceed 0.003% of the measured frequency. Allowing for temperature and ageing effects, the long term accuracy cannot be expected to exceed 0.01% (1 in 10,000), which roughly corresponds to four significant digits. The instrument displays five. The least significant digit is intended to show short term drift effects etc, but cannot be considered reliable.

Principle of operation

The measurement period was chosen to be one second. The 18F458 chip includes facilities for period measurement and counting. Frequencies of 10kHz or more are measured by counting pulses over a one second period, thus achieving the required resolution of better than 1 in 10,000. Frequencies of less than 10kHz are determined by period measurement. The period counter runs at 10MHz (100ns increments). For frequencies over 200Hz, a PIC 16X pre-scaler is used to average the period measurement over 16 periods, thus again achieving a resolution better that 1 in 10,000 for a single period.

Frequencies below 200Hz are measured via a single period to ensure that the overall measurement interval stays well below one second, but for these frequencies resolution is not an issue.

In addition to the standard building block (without the -12V supply), the electronics consist of three main parts:

- An LF amplifier and pulse shaper,
- An RF amplifier,
- A configurable pre-scaler.

The schematic diagram is shown in **Figure 3.**

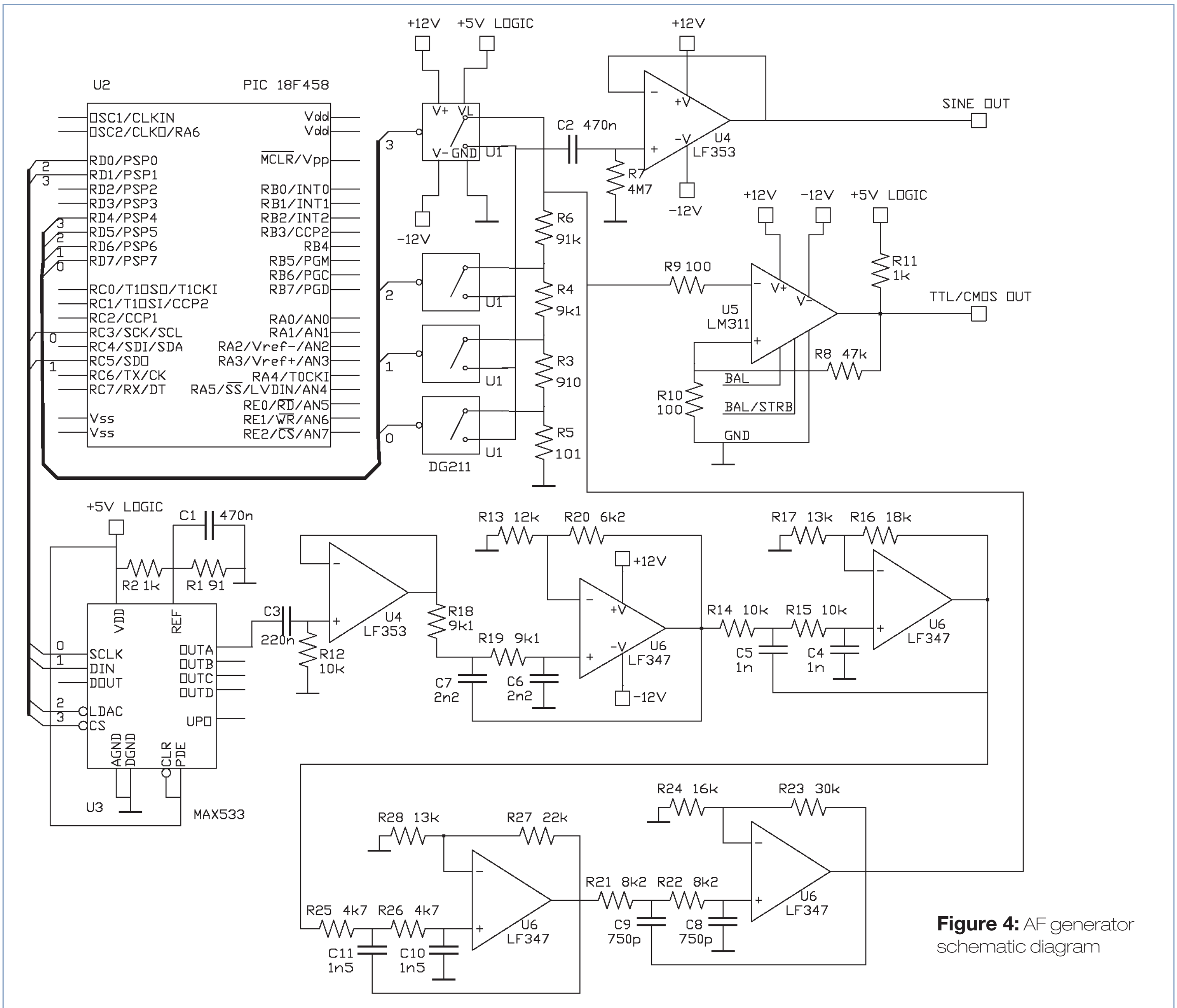


Figure 4: AF generator schematic diagram

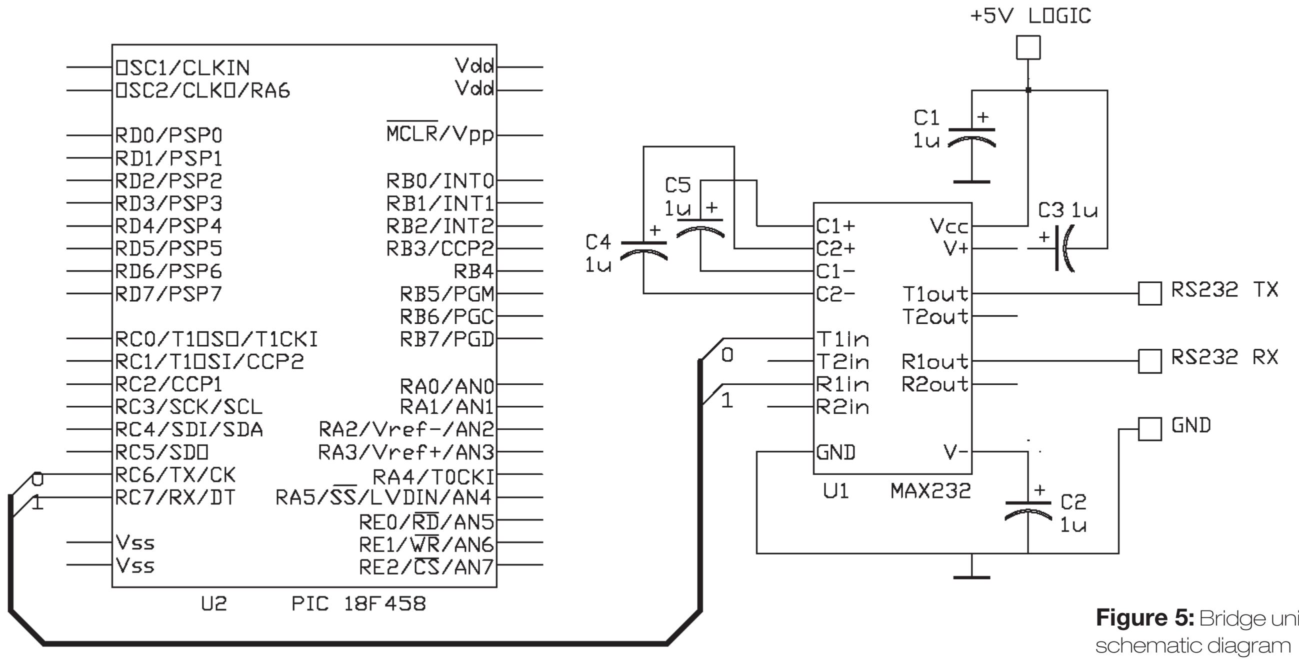


Figure 5: Bridge unit schematic diagram

The "interface" between the digital world of the PIC pre-scaler and the PIC chip and the analogue world of the input signals, is a 74HC14 inverter with Schmitt-trigger inputs. CMOS data sheets generally specify input rise times of better than 1µs, which is used as a design reference value here.

The RF section uses the "brute force" technique of amplifying the input signal, to create a rough square wave signal of around 10Vpp, due to power supply and ground clipping. This drives a common emitter stage into saturation, in turn driving the Schmitt trigger input. With this approach, a 100kHz input signal at 200mVpp results in a rise time of around 1µs. The input impedance of the RF amplifier is around 100Ω.

Below 100kHz, a different technique is used. An LF amplifier followed by a comparator with around 1V of hysteresis. The amplifier gain is -10, giving a hysteresis (and thus minimum sensitivity) at the input of 100mVpp, which seems a reasonable compromise between sensitivity and the ability to deal with noisy signals. The input impedance of the LF amplifier is around 100kΩ.

The LF and RF sections are essentially run in parallel, requiring the user to select the appropriate input for the signal to be measured.

The PIC data sheets are vague on the maximum frequencies for the various counters, but in practice, frequencies above 3MHz cannot be counted reliably. Therefore, a pre-scaler is employed to extend the range to over 20MHz, in four ranges: 0-500kHz, 500kHz-2MHz, 2MHz-8MHz and over 8MHz. The division ratio is selected by the 74HC151 IC and the PIC signals RE0 and RE1. The switch between ranges is performed by the PIC software, based on an algorithm that switches up to the next higher range when the PIC input frequency exceeds 550kHz and down to the next lower range when it is less than 110kHz, thus providing around ± 10% hysteresis. Initially, the pre-scaler is switched to the lowest range, switching up or down as required during operation.

Aliasing

There is an interesting complication in this scheme when trying to measure the highest frequencies. Initially, with the pre-scaler switched to the lowest range, but input frequencies of over 3MHz, these high frequencies are seen directly on the PIC counter input, causing mis-measurement. This is essentially a manifestation of aliasing, because the PIC inputs are sampled at the highest frequency allowed by the PIC chip, which is (far) too low for the highest signal frequencies. This results in a, seemingly, much lower measured frequency, which then prevents the software from switching to a higher range, perpetuating the mis-measurement.

To combat this problem, the input frequency is also divided by the highest available ratio (2^{12} = 4096). The result is measured by a separate PIC counter. If it is over 750 pulses per second (i.e. 3MHz), the pre-scaler is forced to the 2MHz-8MHz range, which will then allow accurate measurement of the actual input frequency so that the normal ranging logic can take over.

AF signal generator

This instrument takes commands from the PC, via the bridge and the CAN bus. To achieve frequency programmability, two approaches were contemplated for the design. The first one was a PLL with a programmable divider in its feedback loop and a clocked switched capacitor filter to turn the square wave into an acceptable sine wave. The second possibility was direct digital synthesis (DDS), with a low pass filter to eliminate clock related artefacts. The latter was preferred, because it can be kept very simple, without pushing the PIC platform to its limits.

The frequency range was designed to be 10Hz-25kHz, with programmable output levels of nominally 10mVpp, 100mVpp, 1Vpp and 10Vpp.

Principle of operation

The DDS here works as follows. The processor keeps a 24-bit accumulator in memory. Every 10μs, a constant value is added to this. The accumulator operates in a cyclic fashion, i.e. it goes up to 2^{24} and then starts again at zero. The ten most significant bits of the accumulator are used as an index in a table of sine function values. The table has 1024 entries of 8 bits each, representing one complete period of the sine wave. The 8-bit value is sent to a DAC. Thus, the output of the DAC will be a stepwise approximation of a sine wave.

A single cycle of the sine wave corresponds to a single cycle of the accumulator and vice versa. As the accumulator is incremented periodically (every 10μs), the size of the incremental value determines the frequency of the sine wave. The incremental value is called the "tuning word". In our design, the output frequency is: (tuning word / 2^{24}) * 100kHz, giving a basic resolution of approximately 0.006Hz.

Essentially, the output signal of the DAC is equivalent to that of a sample-and-hold circuit operating at a sample frequency of 100kHz. The Nyquist criterion states that the highest frequency that can be sampled and reconstructed in this way is 50kHz. In this design the maximum frequency has been chosen as 25kHz. **Figure 4** shows the schematic diagram.

The DAC is followed by an eight pole Chebyshev low-pass filter with a design cut-off frequency of 26kHz and 0.5dB pass-band ripple, theoretically providing over 60dB suppression from the second harmonic onwards for signals below 26kHz, resulting in a respectable sine wave. In practice, there are two causes for deviation from this ideal: component tolerances and compromise values for components.

This design uses 1% resistors in the E24 value range and 1% capacitors with even more restricted values, which results in greater pass-band ripple (measured around 3dB) and slightly unpredictable fall-off in the stop band.

The filter is followed by a programmable attenuator, using DG211 analogue switches. The ranges are nominally 10mVpp, 100mVpp, 1Vpp and 10Vpp, although pass-band ripple causes variation over the frequency range.

There is also a TTL/CMOS compatible output, provided by the LM311 comparator.

DAC and bridge unit

The MAX533 chip has four DACs, but only one is used here. It has an SPI (Serial Peripheral Interface) with the CPU. The output buffers have a slew rate of around 0.6V/s. The overall gain of the filter is around 28.5. To obtain a 10Vpp minimum at the output of the filter over the entire range, the DAC reference voltage has been set at 0.4V, mitigating the relatively poor DAC output slew rate.

According to the data sheet, the temperature dependence of the DAC output amplifiers may cause the lowest codes all to be output as 0. Therefore, the sine table in the PIC memory has been set up to produce a minimum code of 16 and a maximum of 255.

Bridge unit

Figure 5 shows the schematic diagram of the RS232 to CAN bridge unit. It passes messages received via the RS232 link to the CAN bus and vice versa. The CAN controllers in the frequency meter, bridge and AF generator resolve contention on the bus, so the bridge unit is guaranteed to receive messages serially from the CAN bus. It only needs to decode the messages and re-code them in a format that is suitable for the RS232 link and forward them. Likewise, messages received on the RS232 link only need to be decoded and forwarded immediately on to the CAN controller, which resolves possible contention issues.

The RS232 link currently operates at 9600 baud, which is at a far lower speed than the CAN bus. The data throughput, however, is only a few messages per second, maximum. Therefore, only a limited amount of buffering between CAN and RS232 link is required.

PIC programming

Programming PIC16 and PIC18 chips requires concentrating on the data bank and code page selection, which significantly increases the risk of mistakes. A good solution to these problems is the use of the C language, effectively letting the compiler designers and programmers worry about the ins and outs of bank and page switching. Modern C compilers are very efficient and the very slight overheads that remain are amply compensated by the highly increased processing power of the 18C family. In addition, programs can become much clearer due to the better structure of C programs.

After careful study of the 18FXX8 data sheet it is not very difficult to program the CAN controller,

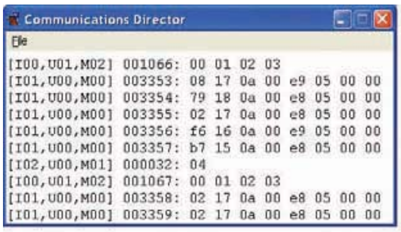


Figure 6: Comms director screenshot

Figure 7: Frequency meter program screenshot

Figure 8: AF generator program screenshot

although it is definitely more complex than the other peripheral devices on the same chip. This project, however, has made use of the CAN routines in 'C', made available by Microchip in AN738.

Comms director

The bridge unit communicates with the PC via a single serial I/O link, carrying all traffic between the PC and the CAN network. Each instrument is a separate unit on the CAN network and has a separate display/control program on the PC. Therefore, the PC needs the equivalent of the bridge unit to route the frequency meter messages to the frequency meter program and to route the AF generator unit messages to and from the AF generator program. This PC program is called "the comms director" and must be running together with the "instrument" programs for the overall system to work.

Each unit has a unique instrument identifier (determined by its software), encoded in the CAN and RS232 message ID: 0 for the bridge, 1 for the frequency meter, 2 for the AF generator. The design makes provision for up to eight units of the same type, e.g. multiple frequency meters. All will have instrument number 1, but they will be distinguished by their unit numbers. Currently, however, this feature is unused. Likewise, the protocol allows for up to eight different message types to be exchanged for each unit.

Essentially, the comms director consists of two parts: One part to handle messages between a program and its instrument and another part to show what is going on the RS232 link (and thus the CAN network).

The message handling of the comms director also consists of two parts, a message store for incoming messages and a queue for outgoing ones. The incoming message store can hold a single message for every instrument on the bus. When a message has been received, the appropriate program is sent a signal, which in turn causes the program to collect the message from the store and deal with it.

The AF generator program can generate commands for the AF generator instrument. These messages are placed in a queue and are sent by the comms director at the earliest possible opportunity, on a FIFO basis. To prevent commands from disappearing into a "black hole" unnoticed, the AF generator echoes each received message, thus indicating to the AF generator program that it is operational and that the communications path is operating correctly.

Running it all together

Connect the bridge unit to the PC via a COM port. Set the COM port number via the comms director file menu. Every five seconds, the comms director sends a diagnostics message to the bridge unit, which is echoed via the RS232 link back to the PC, where it is displayed via the comms director diagnostic window: I00 = instrument 0, U01 = unit 1, M02 = message type 2 (diagnostic message) and four bytes of data: 00 01 02 03. All have been chosen arbitrarily in the design of the comms director, just to display something other than all zeroes.

Connect the frequency meter to the CAN network. This sends a message every second, displayed by the comms director: I01, U00, M00 and eight bytes of data. The data is actually two four byte integer numbers, the measured period in ns and the measured frequency in Hz. For frequencies in excess of 30kHz, the period measurement does definitely not achieve the desired resolution. It does, however, cause a flood of capture port interrupts. To prevent this flood from disrupting other functions, the software disables the period measurement function above 30kHz.

Running the frequency meter PC program will now display the measured value. The program uses the period measurement from the messages for frequencies below 10kHz and calculates the frequency from the period. Above 10kHz, the frequency figure from the message is used and the period is calculated.

There is a risk of undetected failure modes, e.g. CAN network disconnection, power failure, comms director not running, etc. Therefore, the PC display program shows an update indicator, which flashes each time a fresh reading is received. Should this process stop for any reason, the indicator changes to "Stopped" after three seconds and stays so until fresh data is received again.

The AF generator does not send any messages spontaneously, but it is programmed to receive two messages:

- Frequency setpoint: I02, U00, M00 and four bytes of data (floating point value of desired frequency),
- Attenuator setting: I02, U00, M01 and a single data byte (00 – 03 for the range).

Each message is echoed by the unit, allowing the PC program to validate the data path. If no echo is received within two seconds, an error message is displayed.

AF generator evaluation

With an 8 bit DAC (minus 16 codes) and a 25kHz filter, the S/N ratio is predicted at around 50dB (a factor of 316). Without the means of quantifying the noise and various distortion effects more accurately, the oscilloscope display seems to support these figures.

Some interesting effects occur very close to exact divisions of 100kHz, most notably near 25kHz. The amplitude of the signal slowly varies by as much as 10%. Looking at the signal before the filter and after it, it immediately becomes clear what is happening in the time domain. The four samples of the sine wave slowly progress through the entire period of the signal, affecting its average energy content.

Frequency meter evaluation

Connecting the frequency meter to the AF generator confirms that the noise on the signal is significant. The frequency reading is much steadier in the 10V range than in the 1V range, which agrees with the hysteresis of ±100mV. Also, the reading is accurate to 0.01% only.

Using signals from other sources, the instrument gives much more stable read-outs, indicating that the problem of "jitter" lies probably more with the DDS technique used and its implementation than the fundamental operation of the frequency meter.

Where next?

It should be noted that each instrument on the CAN bus needs a corresponding program on the PC. The frequency meter program could be adapted to other display-only uses, whereas the AF generator program could be adapted to other control uses. The comms director is capable of dealing with 31 different instruments, so there is plenty of scope for expansion in this area.

In principle, it would be possible to control the CAN network and its instruments entirely from the PC.

Wireless Networking Technology – How and Why

Gary P. Marrs from Lantronix discusses the benefits of wireless networking and how it can make products and applications more useful through a few design options

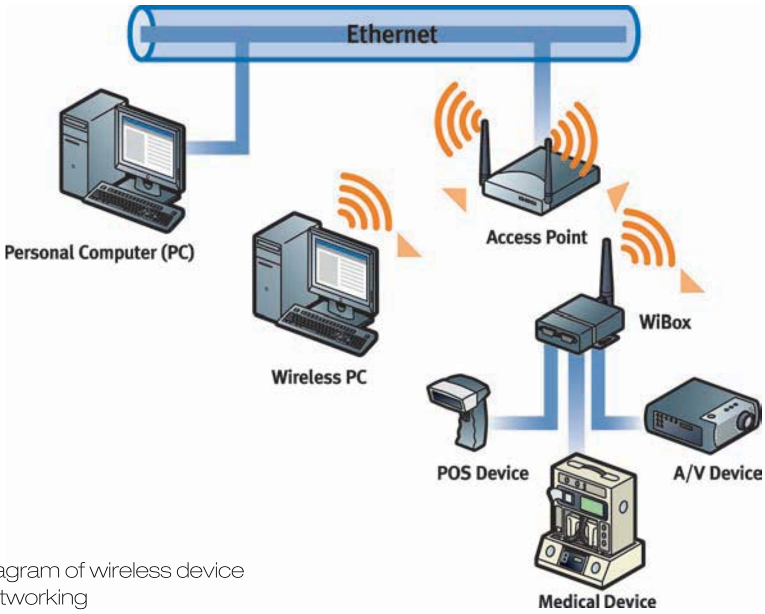


Diagram of wireless device networking

Many industries are realising the benefits of adding wireless technology into an embedded solution that will allow a company to remotely control, monitor and access devices that would otherwise be difficult to put on a network.

For many companies, along with the dream of wireless technology, comes the reality of the challenges associated with its implementation. This is largely due to the list of requirements necessary for creating a true wireless solution. Chipsets and drivers that are difficult to integrate are required, as is a strong understanding of RF and TCP/IP networking among other technologies. In addition, the daunting task of FCC (Federal Communications Commission) certification is required.

Security is another major concern. It has been argued that wireless is not as secure as other networking alternatives. However, it can be just as secure as wired technology with the use of the latest encryption and authentication algorithms. It is important to note that, when implementing wireless technology, each solution will possess individual requirements and the latest security techniques are not yet standardised. These are just a few of the obstacles organisations may face when implementing a wireless solution.

Once convinced that wireless technology is beneficial, the next question is, "How do I add wireless networking to my product?"

Benefits of wireless

There is no question that networking has revolutionised the way we communicate, the way we monitor assets and the way we control equipment. In the last few years wireless computing has exploded because of the mobility it can provide, and the cost of deployment has dropped dramatically.

Wireless device networking is in its infancy but offers many similar benefits. It would, however, be unrealistic to believe that any discussion covering the benefits of wireless device networking would apply to all applications. In most cases, the benefits will differ depending on the ability to do something useful with the content or timeliness of the data. In general, the benefits include:

- Lower cost and ease of deployment
- Greater mobility and flexibility
- Improved data integrity and accuracy
- Enhanced care or service.

Today, the cost of installing wireless is, in many cases, less than the labour costs to string Cat5 cable throughout an office, warehouse or factory environment, especially if remote equipment needs to be connected. In fact, Intel published a study in September 2004 called "*Business Benefits Wireless Computing*", where it reported that the cost savings of installing wireless computing in a building with 3,000 employees is about half as much as installing wired connections.

The cost of installing cable in older buildings is also expensive and time-consuming because many of the walls and ceilings are difficult to wire for traditional local area networks (LAN). In some cases, historic preservation laws make it impossible to run wired LAN connections.

Wireless networks, on the other hand, can be installed and deployed in a few hours, once a site survey has been completed. Also, the price of wireless LAN has plummeted in the last few years.

Mobility and flexibility

Wireless technology can provide the mobility and flexibility needed to gain access to information from devices on the move. It can also allow for devices to be easily relocated, if the work area is being reconfigured for new production equipment or for warehouse space allocation. For example, a wireless solution may be ideal for devices that are connected to a forklift, or even a ventilator attached to a patient who is moving from room to room, without ever losing their network connection. In addition, expanding the network can be easy because the wireless medium is already in place.

By connecting equipment that was previously hard to connect, wireless connectivity provides data integrity and ensures accuracy. In addition, it can bring the advantages of data accessibility and remote management to equipment such as remote controllers, sensors or meters. Wireless data communications can add an unprecedented level of intelligence to business and can eliminate additional labour for manual data entry and in turn minimise human error.

A study conducted by NOP World Technology and Cisco revealed that implementing a wireless LAN can provide greater accuracy in everyday tasks. In the study, called "*2003 WLAN Benefits*" nearly two thirds of end user respondents reported an estimated 41% improvement in the accuracy of data. For respondents from healthcare organisations, 70% felt the improvement in accuracy was noticeable. In this situation, the "anytime, anywhere" aspect of wireless communications helps medical staff ensure patient health and safety by being able to access and record patient information at the point of care.

Wireless device networking can provide enhanced patient care or customer service by utilising real-time monitoring. There are countless examples where field service groups have used wireless monitoring and predictive failure analysis to improve the speed and quality of service calls. Knowing in advance what parts are needed in the truck, preventative maintenance is a benefit that is easy to see and quantify.

Healthcare institutions are requiring patient information faster, if not in real time, to provide better patient care and improve operational efficiencies. For example, after surgery, a patient's blood glucose levels may need to be tested 11 to12 times per day rather than the standard three to four times. This could be a daunting task without the use of a wireless device.

Wireless adoption

Given these benefits, one would expect wireless device networking to mirror the success of wireless computing. But, with the fast evolution of wireless and the achieved freedom, there are some unique concerns and challenges. In addition, embedded designers who are unfamiliar with wireless are plagued with many new questions exclusive to implementing a wireless solution:

- Is the speed/bandwidth of wireless comparable to wired networking?
- Is wireless too complicated for my particular application or environment?
- What security is needed in a wireless implementation and how do I protect data from hackers and eavesdroppers?
- What are the regulatory requirements? Is FCC approval required and how is it obtained?

The early wireless technologies were limited to 1Mbps to 2Mbps and were only half duplex. For many applications, the disparity between wired and wireless throughput was too great to allow wide scale deployment. Today, improved modulation and the additional spectrum in the 2.4GHz and 5GHz bands provide greater wireless bandwidth to burst speeds of 54Mbps. However, as speeds have increased, receiver sensitivity has decreased. With 802.11b/g solutions, the speed of the connection can be selected to allow for slower speeds when the wireless link needs higher receiver sensitivity for more link margin.

In most respects, wireless technology is complex and today's customers require turnkey simplicity. The IEEE 802.11 committee has done a good job of standardising the wireless communication protocol, but the technology has been evolving so rapidly that it is hard for any standards body to keep pace. The most widely used technology today is 802.11b/g. The standard does provide a plug-and-plug like setup when used in Infrastructure Mode with a broadcasted SSID (service set identifier).

The SSID, channel and speed are all configured automatically behind the scenes. For ad-hoc mode, the setup requires selection of the SSID, channel and speed. Some of the off-the-shelf wireless solutions allow an OEM to automatically configure the units via the network or the serial channel.

Security

Wireless security is an important issue and a valid concern. The first attempt at securing the wireless link was Wired Equivalent Privacy (WEP). WEP provided a very light authentication and weak encryption to scramble the data over the air. It was not long before a slew of articles appeared citing successful attempts at breaking the security. The 802.11 committee responded by starting a task group, which attempted to forge a tougher standard and resulted in the creation of the 802.11i standard.

For a lot of reasons, this effort took longer than expected. In the meantime, the Wi-Fi Alliance created an industry standard called Wi-Fi Protected Access (WPA). WPA, which solves many of the problems associated with WEP, is a short-term solution to provide robust wireless security until 802.11i is implemented and widely available.

WPA is designed for use with an 802.1x authentication server, which distributes different keys to each user, however, it can also be used in a less secure "pre-shared key" mode. Data is encrypted using the RC4 stream cipher, with a 128-bit key and a 48-bit initialisation vector (IV).

One major improvement in WPA over WEP is the Temporal Key Integrity Protocol (TKIP), which dynamically changes keys as the system is used. When combined with the much larger IV, it can defeat the well-known key recovery attacks on WEP. At this point, there aren't any known security exploits for WPA.

The 802.11b/g devices use the 2.4GHz license-free spectrum. License free means that this spectrum is allocated for public use provided certain rules are followed. In the US, these rules are enforced by the FCC. The FCC requires any device that radiates RF energy in the license-free bands be tested for compliance to CFR 47 part 15. Once the product reaches a finished prototype form, a test lab can conduct the FCC part 15 compliance testing. In the best case, this process can take 30 days and cost as little as $5,000. If there are problems meeting the requirements, then the costs and approval time can escalate.

In many cases, these are valid concerns, especially when developing a complete wireless design using a chipset. The task of developing a wireless network interface can be long and difficult because it involves integrating RF components with a microprocessor, interfacing to device drivers, porting a TCP/IP stack and running an RTOS to keep it all on track. Once all of this is working, the application must still be written and there is also the task of receiving FCC approval.

Implementing the 802.11b/g interface

There are many options when it comes to developing and implementing an 802.11b/g interface. In each case, the tradeoffs are large. Development costs, time-to-market, bill-of-materials costs, FCC approval and design risk all factor into the final choice. Before selecting and implementing an RF solution, the following should be analysed:

- Forecasting the drain on engineering resources and ensuring that the right engineering skills are there to complete an RF solution.
- Examining annual usage rates to determine return on investment.
- Factoring in design and system integration risks for the hardware and software.
- Obtaining FCC approval – understanding the time involved and potential costs.
- Selecting the correct security algorithms to protect the integrity of the data.

From a practical aspect, there are three options for implementing a WLAN interface for an embedded application:

1. Buy a chipset (usually two or more chips) and integrate the hardware and software into your existing application and microprocessor.
2. Integrate a PCMCIA (also known as a PC Card) with your existing microprocessor and operating system.
3. Buy an off-the-shelf solution that is designed to integrate directly with your existing microprocessor.

The available solutions

There are a few large companies that offer wireless chipset solutions. In general, this approach requires a talented staff of engineers to complete the software and hardware design integration. This choice will require the longest time and largest cost for engineering development. But for high volume applications, a chipset design will, in most cases, provide the lowest bill of material cost. The risk for RF problems or software issues is a large concern with this option. Another very common concern is the risk that the manufacturer will issue an end of life on the chipset. This would force a complete redesign and a new round of FCC compliance testing.

Among its advantages are:

- It can provide a cost-effective solution for high volume applications.
- It allows some customisation through configuration options.

Among its disadvantages are:

- It requires RF technical expertise to complete the hardware design.
- It requires extensive software integration to interface to the existing microprocessor.
- It requires complete FCC testing and approval before the product can be released.
- The time to market is a minimum of 14 to 18 months.

When it comes to the PCMCIA solution, there are several companies that now produce an 802.11b/g interface in such packages. These are popular for use with notebook computers. However, there have been many implementations where a standard PCMCIA-type design has been integrated into an embedded wireless application. This choice will require a fair amount of engineering development to complete the design integration. The biggest issue will be obtaining the right driver from the manufacturer and making sure it works with the application. Also, a PCMCIA solution requires the host CPU to perform a large portion of the data processing prior to sending it the driver.

Among the PCMCIA's advantages are:

- It makes sense if you are going to implement an operating system that already supports that particular card.
- If your application requires it, some cards offer higher output power.

But, disadvantages include that:

- It requires a fair amount of storage and processing on the host CPU.
- It requires software integration to interface to the existing driver, which may be difficult to accomplish.
- It requires FCC testing and approval before a product can be released.
- Some or all of the encryption, or key generation, will be relegated to the host CPU.
- The minimum time to market is 10 to 12 months.

As for off-the-shelf (OTS) WLAN module, this has recently become a very popular option. This is a complete module that takes simple serial data to an 802.11b/g network. All of the RF and networking functionality has already been integrated into the module, so the OEM engineering development time is minimal. The added benefit is that all of the RF and network processing is off-loaded from the host microcontroller. In fact, in many cases, the OTS solution can be added to an existing design with very minimal impact to the existing firmware. This greatly minimises the project development time and risk.

Wireless network security is provided as a configuration option. Most of the manufacturers that provide embedded OTS solutions have already implemented WEP and WPA. This eliminates the need to become a wireless security expert.

In the event that the underlying wireless technology reaches end of life, the OTS manufacturer will redesign the wireless module and handle FCC approval while maintaining the form, fit and function of the module to the OEM.

Most importantly, the OTS wireless module comes with FCC approval. Some OTS modules even come with a modular FCC approval that allows an OEM to leverage that approval in order to get quicker approval on their final product. This can significantly minimise the OEM's time and costs.

The advantages of such a module are:

- It can easily integrate with existing microprocessor firmware. It does not require any changes to existing firmware code if you are already using a serial interface.
- It does not require highly skilled RF hardware and software engineers on staff to implement.
- The OEMs FCC modular compliance can be leveraged to gain approval. In most cases, minor paperwork is needed if the design uses a 3dBi antenna or less.
- Design can be completed in four to eight weeks (quick time-to-market).

But, its main disadvantage is that is has limited options for a customised RF interface.

Implementing an OTS WLAN solution

The OTS solution provides a simple serial interface, which is connected directly to the UART interface on a microcontroller. **Figure 1** depicts an OTS solution connected to a Microchip PIC processor. All that is required is power, TX, RX and a reset signal.

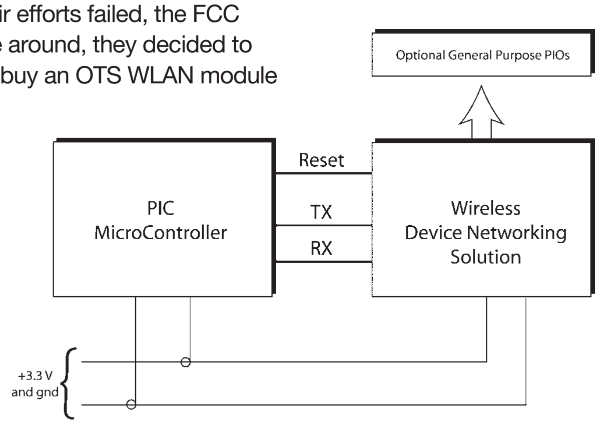
The OTS solution also has general purpose I/O pins (GPIO) that can be configured as inputs or outputs. The GPIO are handy for hardware handshaking to the host processor, detecting sensor signals or turning on buffered relay outputs. The GPIO signals can also be used to trigger e-mails.

In a security door application, an off-the-shelf module simplifies the otherwise complicated configuration and installation, traditionally associated with implementing a network application. If the door's controller was equipped with an industry standard 802.11b wireless protocol, it would make it compatible with virtually any wireless access point on the market. In addition, the integrated module would provide WPA and 128-bit WEP encryption capabilities to ensure secure communications between the IP and the network. The security OEM would only have to develop software to provide its customers with the ability to directly monitor and control an almost unlimited number of security doors enterprise-wide.

In another example, an industrial manufacturer recently took its first stab at building wireless capabilities into one of its products. Engineers there spent two years trying to devise an RF interface that would pass FCC certification tests. They went through several redesigns and spent about a million dollars in the process. When their efforts failed, the FCC hurdle the second time around, they decided to throw in the towel and buy an OTS WLAN module instead.

Given the fast changing nature of wireless technology, obtaining FCC approvals developing and implementing a secure wireless device solution can be challenging.

Figure 1: OTS WLAN solution connected to a Microchip PIC processor



RoHS
WHAT'S ALL THE FUSS ABOUT?

RoHS (the Restriction of the use of certain Hazardous Substances) and WEEE (Waste Electrical and Electronic Equipment) is the equivalent of Y2K for the electronics industry. The upcoming EU environmental directives are the most significant developments in electronics legislation to happen in many years and will completely revolutionise the way electrical and electronic products are designed, sold, recovered and recycled. Worryingly, many design engineers are still not fully aware that the upcoming legislation will affect them. For those who are, many questions remain unanswered. Complicated exemption rules, uncertainty about how the directives will be enforced, obsolescence and component availability has left engineers unsure of what they need to do and when. The clock is ticking. With only several months to go, there's no time to lose in the transition to RoHS. If compliant components aren't already part of the design cycle it could well be too late.

Q: What about hard anodisers? I have heard of hundreds of valuable scope CRTs being smashed into skips before the law comes in.

Ben Duncan, UK

A: *By hard anodising, I assume this is for aluminum, which can be anodised using chromic acid or sulphuric acid. Although this is OK with sulphuric acid it is not with chromic acid as this leaves hexavalent chromium in the coating. Some anodised coatings are sealed with chromates, this is also not OK.*

CRT recycling is a requirement of the WEEE directive, already in force in most EU States although not the UK. Annex II requires all CRTs to be recycled separately. There are no restrictions on re-use, should there be a demand for second hand scope CRTs; in fact, WEEE encourages this.

Q: What is the difference between tin whiskers and dentrites?

A: *Tin whiskers grow outward from a surface; Dentrites grow along a surface.*

Dentrites are fern-like or have a snowflake-like patterns. Tin whiskers are filaments of tin metal surface and can cause short circuits.

Q: As an American manufacturer of industrial equipment for the professional radio broadcasting market, we are finding it increasingly easier to locate RoHS-compliant components, but not sure if we fit into any of the categories of the Directive.

Jim Wood, US

A: *Although category 4 is called "consumer electronics", the authorities view this as "consumer-type" electronics and so does include professional audio etc. Radio broadcasting equipment however is category 3 — transmission of information and so these products should comply with RoHS, although some may be within the scope of the exemption for lead in solders in telecommunications network infrastructure.*

Q: As a foreign manufacturer, exactly what is our obligation, or the obligation of our UK distributor, under WEEE?

Jim Wood, US

A: *There is currently a lot of discussion within EU States about whether non-EU manufacturers can register. This affects US exporters who supply directly to business customers. The US manufacturer may wish to be responsible for WEEE for commercial reasons as otherwise the business user is responsible. This is not currently possible in most EU States but some, including Portugal, are considering changing their approach. Currently, US manufacturers can register in a few countries including Germany, Ireland and Hungary.*

Q: In the case of "consignment stock", where stock is moved from the manufacturer to distributor's warehouse, but not paid for until the distributor sells the stock to its customer, is this deemed as on the market?

A: *Yes, payment is not a requirement of 'being on the market'. The stock is deemed on the market once it is moved from the site of manufacture to another location.*

Q: Why do I need to keep a technical compliance file and what should be included?

A: *Technical compliance files or TCFs, are required to provide evidence of compliance and enforcement authorities, such as National Weights and Measures, will expect to see one. TCFs should be kept for a minimum of four years from the last date of manufacture (six years under the Irish legislation) and include:*

- *Materials declaration*
- *Certificates of compliance*
- *Analytical data – e.g. quality assurance check of incoming parts or accredited third part testing further up the supply chain*
- *Documented procedure on declaration assessment. This should also include evidence that this is being fulfilled*
- *Results of audits from suppliers.*

Q: If a school or college builds its own equipment, is this put onto the market?

A: *In most cases the answer is no. "Products built for own use are, generally, not considered as being placed on the market" (The EU Guide to the Implementation of Directives). So, there is no need to register for WEEE or for it to be RoHS compliant. However, it is important that ownership does not change because then it would be deemed as 'put onto the market' and within scope.*

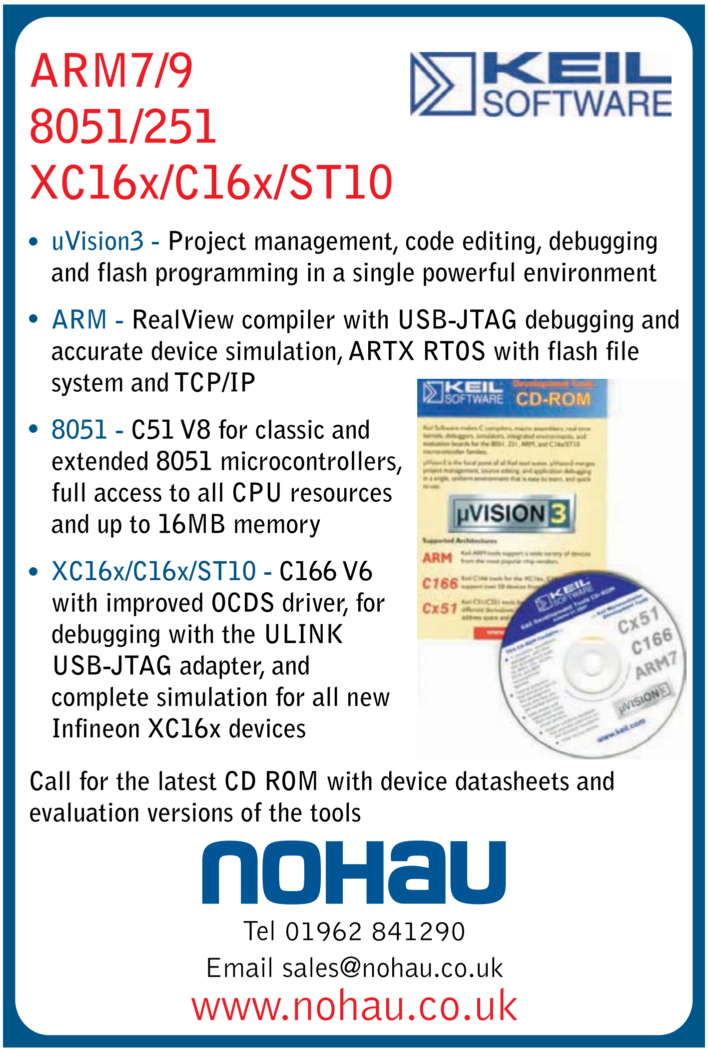
You must remember that equipment purchased by schools or colleges has the same status as it does for any other user and, if it is within one of the eight categories, will need to comply with RoHS.

Q: Can I be sure that the termination coatings of the components that we use in our process development work are now lead-free in readiness for the 1st July deadline?

A: *In short, no. Most component manufacturers have already changed to lead-free terminations but some are still in the process. Lead-free component termination coatings must be used to comply with RoHS and these should be used for process development work. If lead-free components are not yet available, this creates a problem when developing lead-free processes, as tin/lead wetting performance and joint reliability are different to that of lead-free coatings.*

Gary Nevison is chairman of the AFDEC RoHS team, board director at Electronics Yorkshire and head of product market strategy at Farnell InOne. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS and WEEE. Your questions will be published together with Gary's answers in the following issues of Electronics World.

Please email your questions to EWeditor@nexusmedia.com, marking them as RoHS or WEEE.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8051/251
XC16x/C16x/ST10
KEIL SOFTWARE
• uVision3 - Project management, code editing, debugging and flash programming in a single powerful environment
• ARM - RealView compiler with USB-JTAG debugging and accurate device simulation, ARTX RTOS with flash file system and TCP/IP
• 8051 - C51 V8 for classic and extended 8051 microcontrollers, full access to all CPU resources and up to 16MB memory
• XC16x/C16x/ST10 - C166 V6 with improved OCDS driver, for debugging with the ULINK USB-JTAG adapter, and complete simulation for all new Infineon XC16x devices
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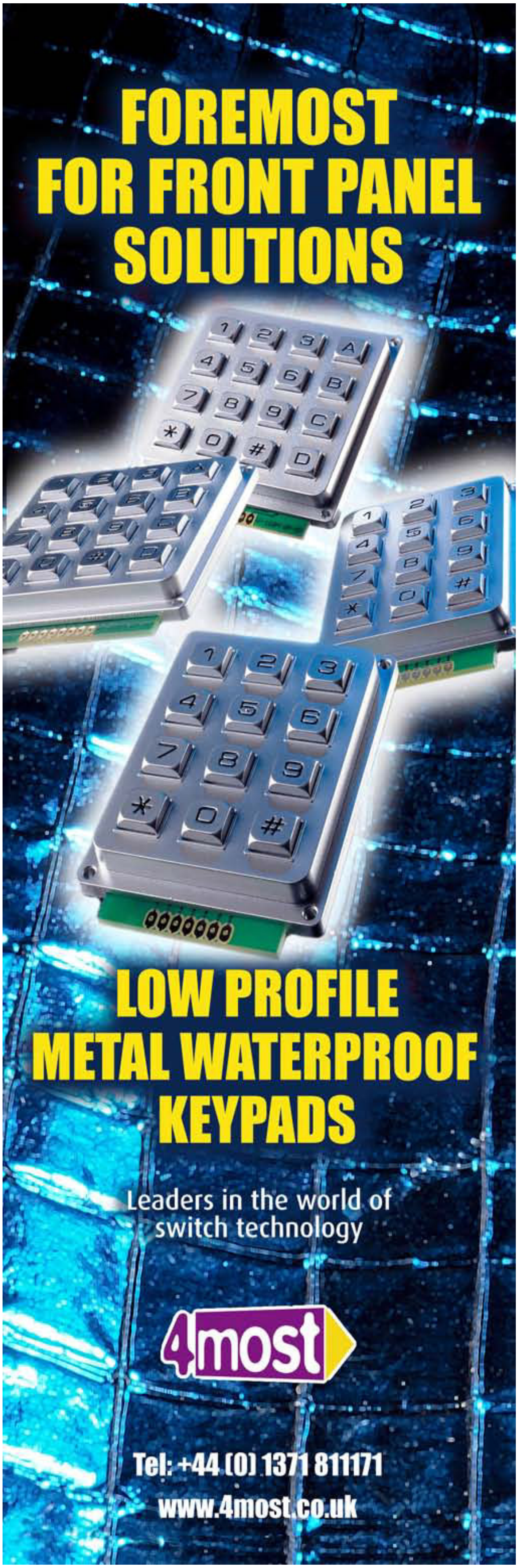
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Novel Voltage-Mode Universal Biquad Filter

Recently, a novel multifunction voltage-mode filter was proposed by Erkan et al. (*Electronics World* June 2005) and shown in **Figure 1**. This proposed circuit, employing only one balanced dual input-dual output current conveyor (BDI-DOCC), two floating capacitors and two floating resistors, offered the following features:

- ➢ use of a single active element;
- ➢ realisation of all-pass, notch, high-pass, band-pass and low-pass signals from the same configuration;
- ➢ no requirements for component-matching conditions; low active and passive sensitivities.

But, both the natural frequency ω_0 and quality factor Q of Figure 1 had mutual dependence.

Here, I present a new voltage-mode filter exhibiting all of the above features but in a new configuration (see **Figure 2**). Furthermore, the proposed new circuit idea can be orthogonal tuning of the natural frequency ω_0 and quality factor Q better than the proposed circuit in Figure 1.

Figure 2 employs a single BDI-DOCC, two capacitors and three resistors. Using standard notation, the input-output relationship of a BDI-DOCC is characterised by $V_{X+}=V_{Y1}$, $V_{X-}=V_{Y2}$, $I_{Z+}=I_{X+}$ and $I_{Z-}=-I_{X-}$. Analysis of the various transfer functions of the configuration of Figure 2 is shown in **Equation 1**:

$$V_{out} = \frac{s^2C_1C_2V_1 + sC_2(G_2+G_3)V_2 + G_1G_2V_3}{s^2C_1C_2 + sC_2(G_2+G_3) + G_1G_2}$$

It is evident from Equation 1 that the natural frequency ω_0 and quality factor Q are shown as **Equation 2**:

$$\omega_o = \sqrt{\frac{1}{R_1R_2C_1C_2}} \qquad Q = \frac{R_3}{R_2+R_3}\sqrt{\frac{C_1R_2}{C_2R_1}}$$

The ω_0 and Q can be properly controlled by R_1 and/or R_2 and R_3, in that order. Note that, the proposed new circuit adding an important advantage: orthogonal control of ω_0 and Q, which was not realising in the recent proposed circuit of Figure 1.

From Equation 1, the five standard biquad filter functions could easily obtained as the same in Figure 1.

To validate the theoretical prediction of Figure 2, we have used H-Spice with TSMC025 process to do the simulation. The supply voltages were $V_{DD}= -V_{SS}=1.25V$, the biasing voltages were $V_{b1}= -V_{b2}=0V$ and the biasing currents were $I_{B1}=I_{B2}=50\mu A$. Figure 2 was designed for $f_0=1MHz$ and Q= 4.95 by choosing $R_1=2k\Omega$, $R_2=10k\Omega$, $R_3=1000k\Omega$, with $C_1=79.5pF$ and $C_2=15.9pF$.

Figure 3 was shown the simulated and theoretical response of low-pass, band-pass, high-pass, notch and all-pass. As can be seen, there is a close agreement between theory and simulation.

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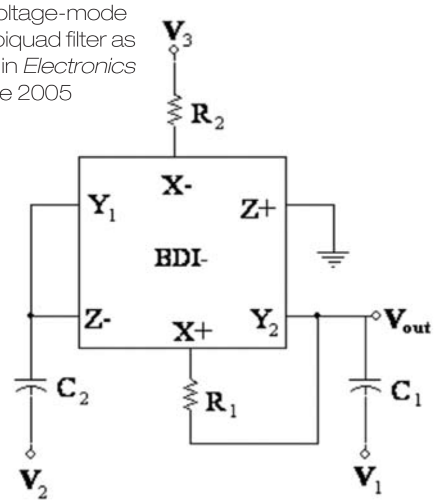
Figure 1: Voltage-mode universal biquad filter as proposed in *Electronics World* June 2005



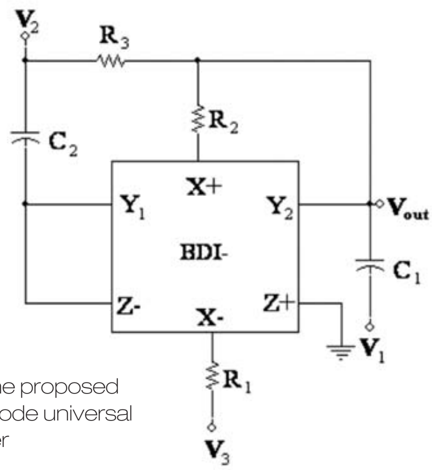
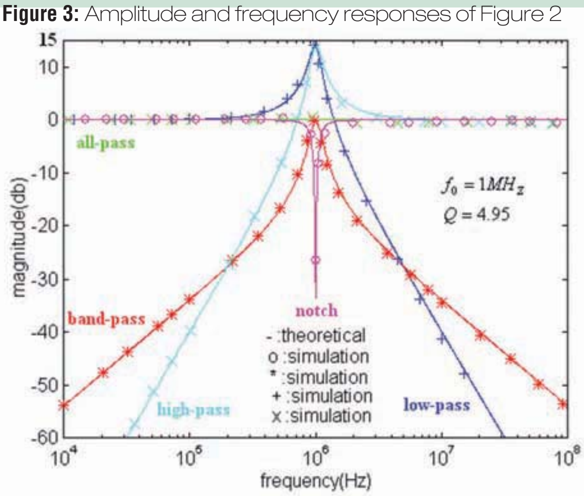


Figure 2: The proposed voltage-mode universal biquad filter

Figure 3: Amplitude and frequency responses of Figure 2



Use Simplorer to Simulate Power Factor Corrected Circuits

Digital control is being incorporated in the control of power converters thanks to the increasing performance and cost reduction of digital signal processors (DSPs) and microcontrollers. This has allowed implementing more sophisticated control techniques like space vector modulation (SVM) for power factor corrected (PFC) circuits and variable-speed drives, among others.

To simulate these circuits, Simplorer of Ansoft (www.simplorer.com) is a good candidate as it combines the benefits of a fast and numerically stable circuit simulator, a block diagram system simulator for control purpose and a state-machine simulator for discontinuous processes.

This design idea is related on the simulation of a three-phase boost rectifier (**Figure 1**) with Simplorer v7 SV, where the SVM technique is applied for power factor correction at the input.

The SVM technique is based on the representation of any three-phase quantity ($\chi_R(t) + \chi_S(t) + \chi_T(t) = 0$) into a rotating space vector $X(t)$:

$$X(t) = \frac{2}{3} \cdot \left(x_R(t) + x_S(t) e^{j\frac{2\pi}{3}} + x_T(t) e^{-j\frac{2\pi}{3}} \right) = X_m \cdot e^{j\omega t} \tag{1}$$

The circuit in Figure 1 provides eight possible switching combinations, made up of six active and two zero switching states (SSVs), which are represented in **Figure 2** by using **Equation 1**. Active vectors divide the plane into six sectors. The idea of the SVM algorithm is to synthesise a rotating space vector V(t) at the rectifier input that gives an input current with low total harmonic distortion and in phase with the corresponding input voltage (power factor correction). The space vector V(t) can be synthesised at any given instant by PWM of the two adjacent SSVs and null vectors (Figure 2), with duty cycles proportional to each projection and given by:

$$\begin{aligned} d_\alpha &= m \cdot \sin\left(\frac{\pi}{3} - \phi\right) \\ d_\beta &= m \cdot \sin(\phi) \\ d_o &= 1 - d_\alpha - d_\beta \end{aligned} \tag{2}$$

where $m \in [0,1]$ is named modulation index and controls the output voltage and $\phi \in [0,\pi/3]$ is the angle between $V(t)$ and the lower SSV.

The duty cycles in **Equation 2** indicates the time each SSV has to be applied in the PWM pattern; however, the distribution of the adjacent vectors and the null vectors in a switching period is free. One possible distribution, which

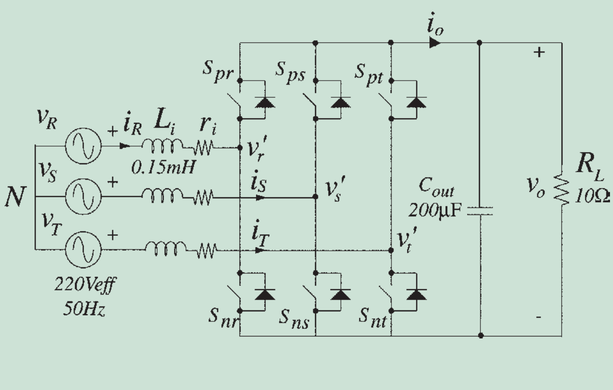


Figure 1

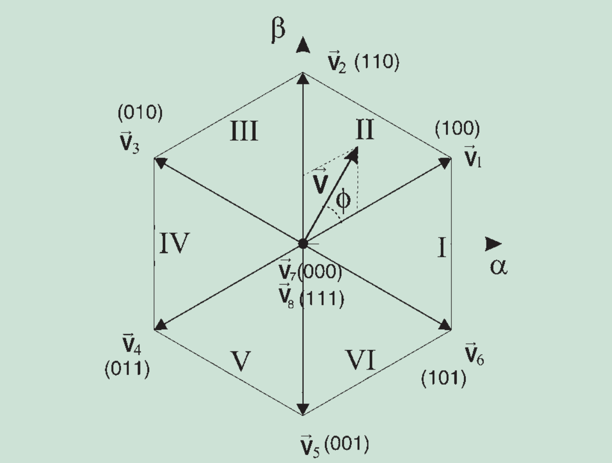


Figure 2

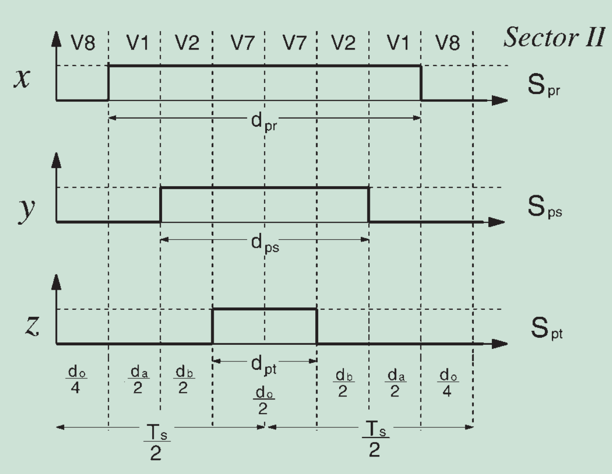


Figure 3

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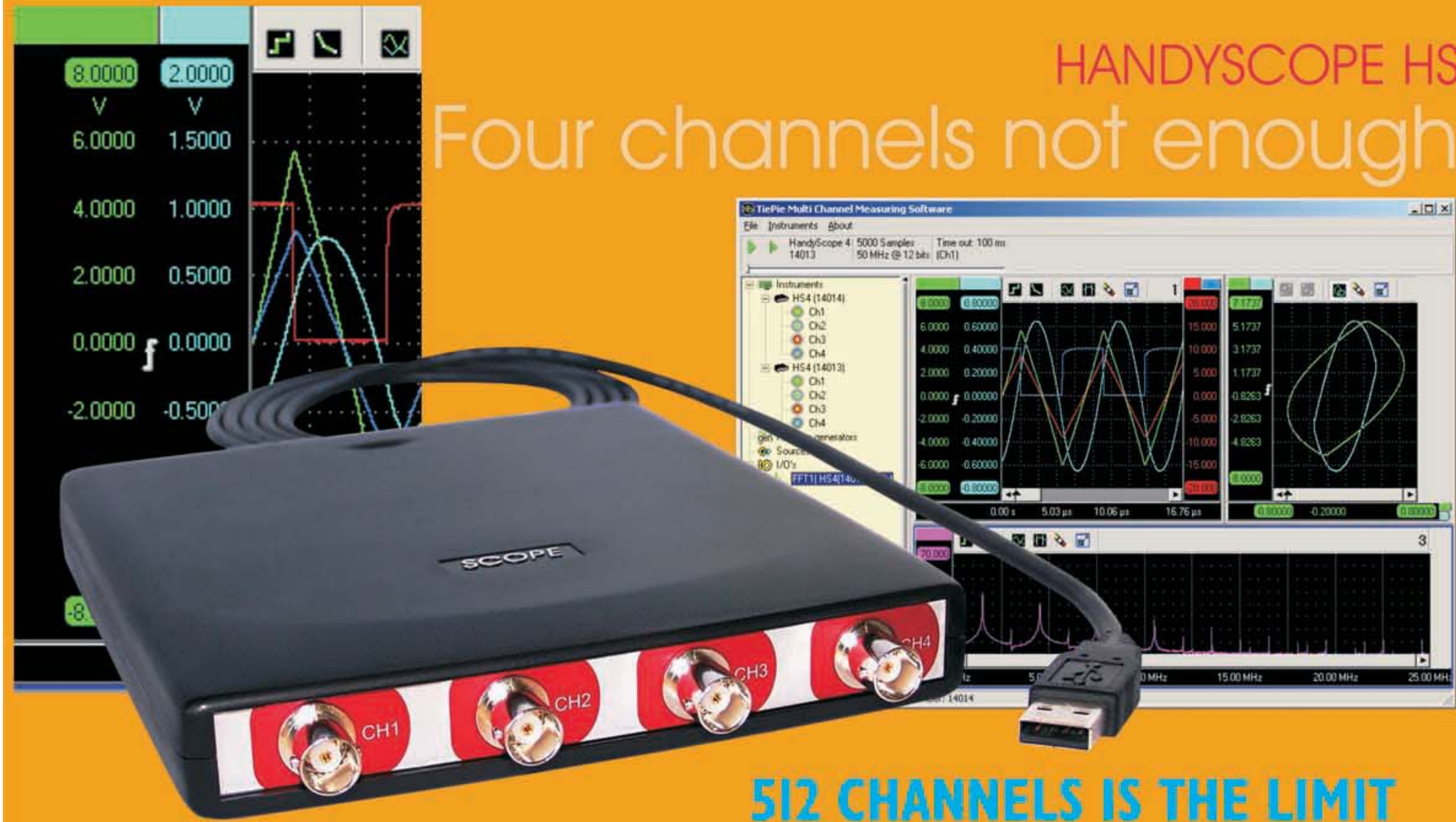

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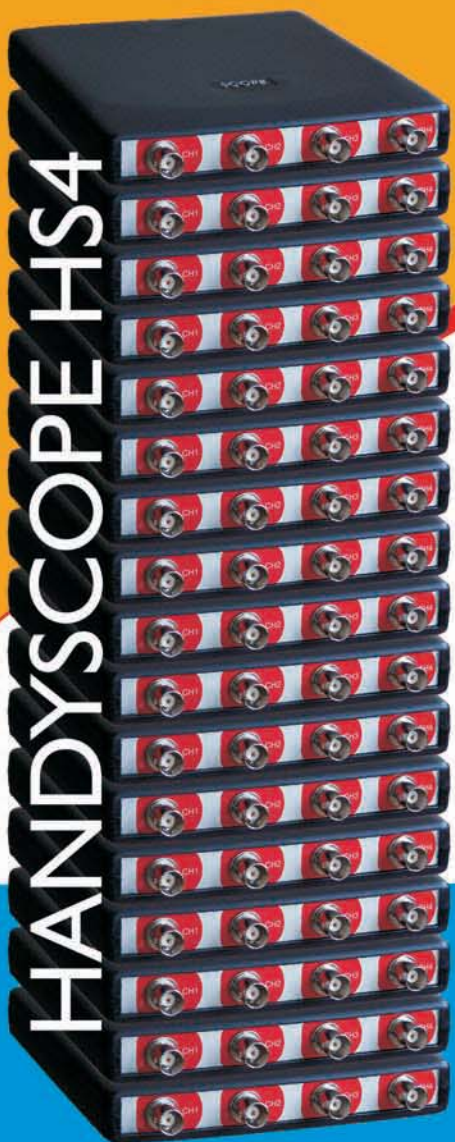

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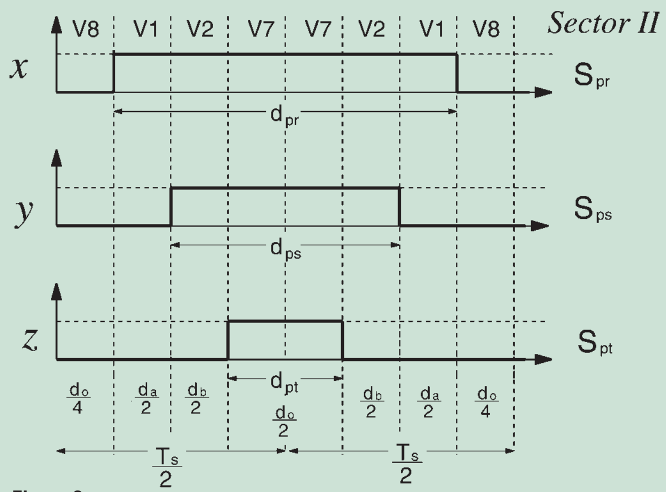


Figure 3

will be used in the present note, is shown in **Figure 3** for sector II. These signals can be applied for the remaining sectors by defining three auxiliary signals named x, y, z which are differently distributed to the transistor gates according to **Table 1**.

For the simulation with Simplorer of the circuit in Figure 1 with the SVM algorithm, two state-machines are used. The first one (**Figure 4a**) implements the auxiliary signals according to the PWM pattern of Figure 3, by dividing the switching period in so many PWM signals as used SSVs, except one. State-machines transition are generated as mod$(t \cdot f_s, 1) \geq$ *desired duty cycle* calculated with Equation 2, with t the simulation time and f_s the switching frequency (20kHz). **Figure 4b** implements Table 1, where transition are generated each 60°. The sinus functions of Equation 2 are also calculated and initialised at the beginning of each 60° sector

Figure 4b

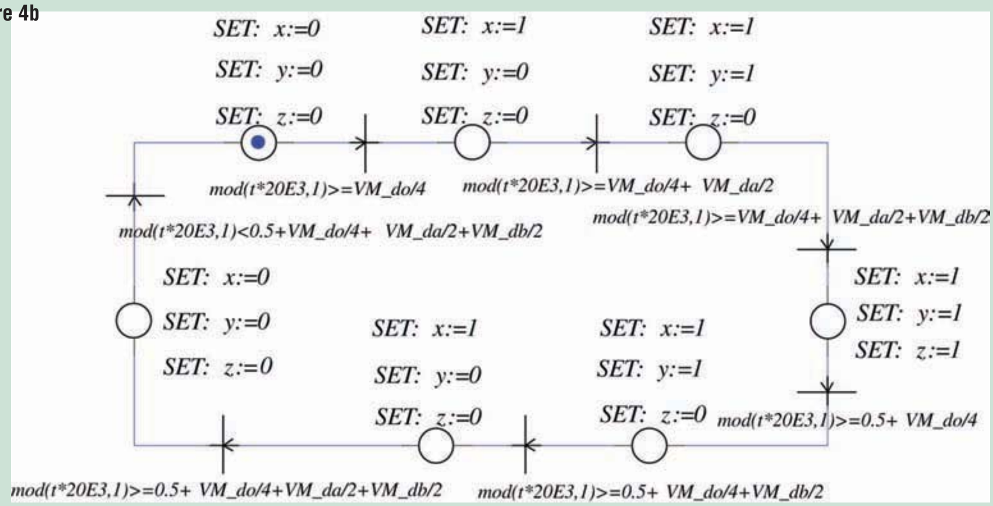
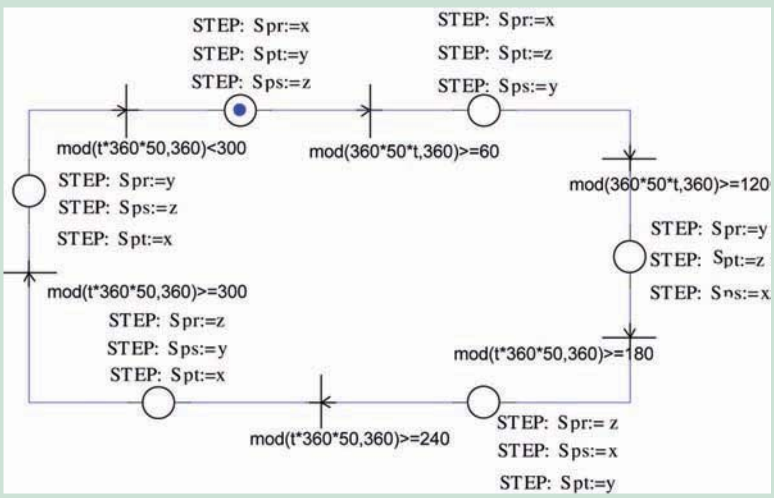


Figure 4a



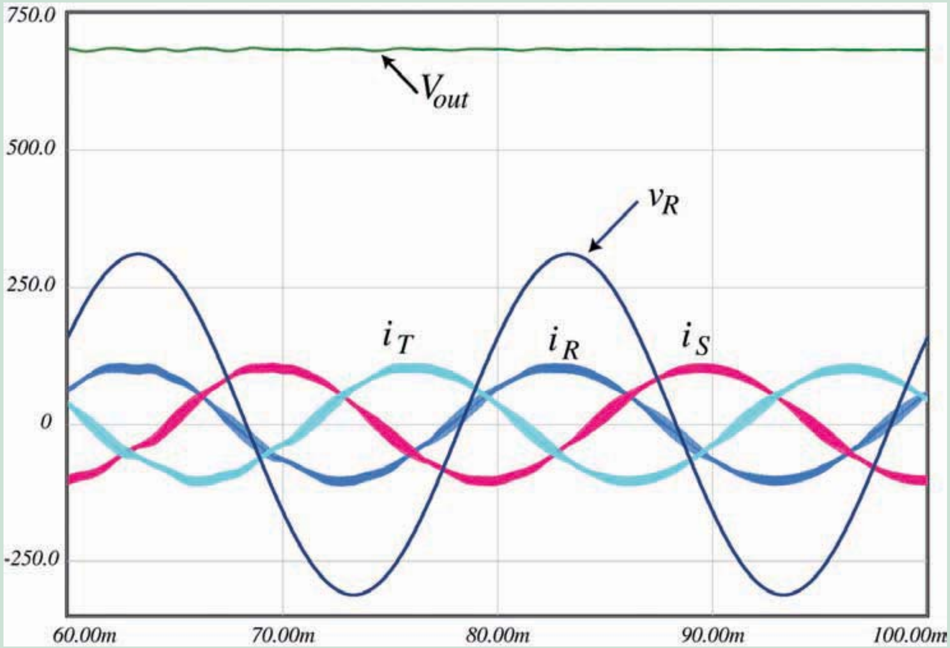


Figure 5

SECTOR	S_{pr}	S_{ps}	S_{pt}
I	x	z	y
II	x	y	z
III	y	x	z
IV	z	x	y
V	z	y	x
VI	y	z	x

Table 1

The simulation is initialised at the beginning of the sector I, which means that input phases v_R, v_S, v_T must be taken with a phase-shift of 30^o, -90^o and 150^o, respectively (Figure 2 is referred to the phase-to-phase voltages). Moreover, due to the input inductor L_i, the space vector $V(t)$ must be delayed an angle ψ respect to the space vector of the input voltages $Vi(t)$ given by,

$$tag(\varphi) \approx -\frac{2P_i L_i \omega}{V_{RS}^{\ 2}} \qquad (3)$$

This angle, which depends on the input power P_i, is added to the initial phase-shift of the input voltages to obtain a unity displacement factor (input voltages and currents in phase). In addition, to omit the transient time during simulation, the output capacitor C_{out} has been initialised with the final value of V_o. **Figure 5** shows the simulation results with $m = 0.8;\ \psi \sim 0.5^o$ (calculated by **Equation 3**) and $V_o = 685V$, which gives an input phase current i_R in phase with the corresponding phase voltage v_R (power factor correction near the unity).

R. García-Gil, J. M. Espí and J. Castelló,
Department of Electronic Engineering,
University of Valencia, Spain

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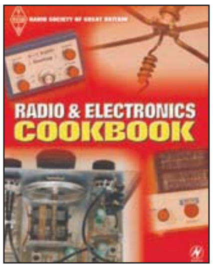

I have numerous electronics cookbooks on my bookshelf, in a range of different formats. This cookbook takes the form of a large number of separate electronics construction projects, along with a number of articles on electronics theory. These construction projects and theory articles appear to be targeted at the beginner to intermediate hobbyist.

Although published by the Radio Society of Great Britain, it is not exclusively for amateur radio enthusiasts. In addition to articles related to general radio topics, amateur radio and antennas, there are many articles on audio, test equipment, power supply, electronics theory and general interest circuits. Of the radio-related articles, many are not specifically targeted at amateur radio but are more general in nature.

In general, the level of skill required to construct each circuit increases as you progress through the book. Some of the final articles (Grid Dip oscillator, CW transmitter for 160M to 20M) are definitely not for the beginner.

The theory articles are all fairly basic and suitable for the electronics beginner. They cover such topics as descriptions of basic electronic components, radio waves, transmission line standing waves, radio frequency mixers, digital electronics and other similar topics.

The audio projects are all at the beginner level also and include simple oscillators (for Morse code practice and signal injectors), a couple of simple amplifiers, a simple audio filter and the construction of a desk microphone.

The test equipment category of articles can be split into general test equipment and radio testing equipment. The general test equipment projects include a couple of simple transistor testers, a capacitance bridge, a continuity tester and an audio signal injector. The radio test equipment is both general (such as an RF signal probe and a crystal calibrator) and amateur radio specific (such as a Grid Dip oscillator, a couple of absorption wavemeters, a 1.8MHz to 50MHz standing wave indicator and an RF field strength meter).

There are only two power supply related construction projects, a NiCad battery charger and voltage monitor for a 12-volt power supply.

Most of the articles are devoted to radio related construction projects. There are numerous receiver projects, ranging from a couple of simple crystal radios, to regenerative detectors, to direct conversion receivers to quite sophisticated superheterodyne amateur radio receivers. These receivers cover the broadcast band and the 40-meter and 80-meter amateur radio bands. There is even a 2-meter (144MHz) receiver pre-amplifier project. These latter projects are definitely targeted at the more experienced constructor.

There are also several transmitter construction projects. Three of these are for very simple low power 80M CW (Continuos Wave) transmitter. The fourth transmitter project is again very low power but it covers the 20M to 160M amateur radio bands. It should be noted that these projects require an amateur radio license to operate.

Throughout the book you will find numerous antenna or antenna related construction projects. These cover the frequency range from long wire, low frequency receiving aerials to a couple of 70cm band antennas and a UHF corner reflector antenna. There are several antenna tuners including a 1.8MHz to 30MHz simple antenna matching unit for random length antennas, a 40W dummy load and a RF changeover relay circuit to automatically switch an antenna from receive to transmit.

The more general interest construction project that don't fit into any of the above categories include such things as a light meter, a moisture meter, a water level alarm, an electronic dice, a simple electronic organ, a metronome and a couple of LED flasher circuits.

While the circuits in this book range from the very simple to the reasonably complex, even the simple ones offer the more experienced hobbyist the opportunity for modification to extend their capabilities.

Unlike a lot of cookbooks, many of the articles in this book include a description of how the circuits operate. Most of the articles indicate that the required components may be sourced in the UK from Maplins, but these parts are not very exotic and should be readily available from North American suppliers like Digi-Key and Newark, or other international sources. Many of the articles also provide references for obtaining complete kits of parts.

Doug Oddy

LCD PICmicro Microcontrollers

Using an LCD PICmicro microcontroller for any embedded application can provide the benefits of system control and human interface via an LCD. Design practices for LCD applications can be further enhanced through the implementation of these suggested Tips 'n' Tricks. These tips describe basic circuits and software building blocks commonly used for driving LCD displays.

➲TIP 1: Contrast control with a buck regulator

Contrast control in any of the LCD PICmicro microcontrollers is accomplished by controlling the voltages applied to the VLCD voltage inputs. The simplest contrast voltage generator is to place a resistor divider across the three pins. The resistor ladder method is good for many applications, but the resistor ladder does not work in an application where the contrast must remain constant over a range of VDDs. The solution is to use a voltage regulator. The voltage regulator can be external to the device or it can be built using a comparator internal to the LCD PIC microcontroller.

The PIC16F917/916/914/913 devices have a special comparator mode that provides a fixed 0.6V reference. The circuit shown in **Figure 1** makes use of this reference to provide a regulated contrast voltage. In this circuit, R1, R2 and R3 provide the contrast control voltages. The voltage on VLCD3 is compared to the internal voltage reference by dividing the voltage at VLCD3 at R4 and R5 and applying the reduced voltage to the internal comparator. When the voltage at VLCD3 is close to the desired voltage, the output of the comparator will begin to oscillate. The oscillations are filtered into a DC voltage by R6 and C1. Capacitor C2 ensures that the voltages at VLCD1 and VLCD2 are steady.

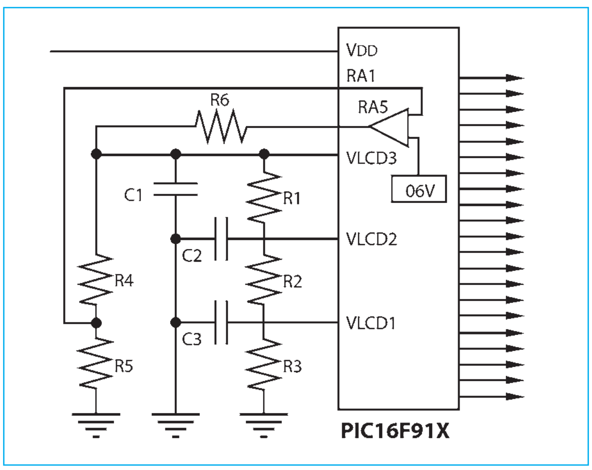

Figure 1: Voltage generator with resistor divider

➲TIP 2: Contrast control using a boost regulator

In Tip 1, a buck converter was created using a comparator. This circuit works great when VDD is greater than the LCD voltage. The PIC microcontroller can operate all the way down to 2.0V, whereas most low voltage LCD glass only operates down to 3V. In a battery application, it is important to stay operational as long as possible. Therefore, a boost converter is required to boost 2.0V up to 3.0V for the LCD (see **Figure 2**).

In the circuit of Figure 2, both comparators are used. The voltage set point is determined by the value of Zener diode D3 and the voltage at R6:R7. The rest of the circuit creates a simple multivibrator to stimulate a boost circuit. The boost circuit can be inductor or capacitor based. When the output voltage is too low, the multivibrator oscillates and causes charge to build up in C2. As the voltage at C2 increases, the multivibrator will begin to operate sporadically to maintain the desired voltage at C2.

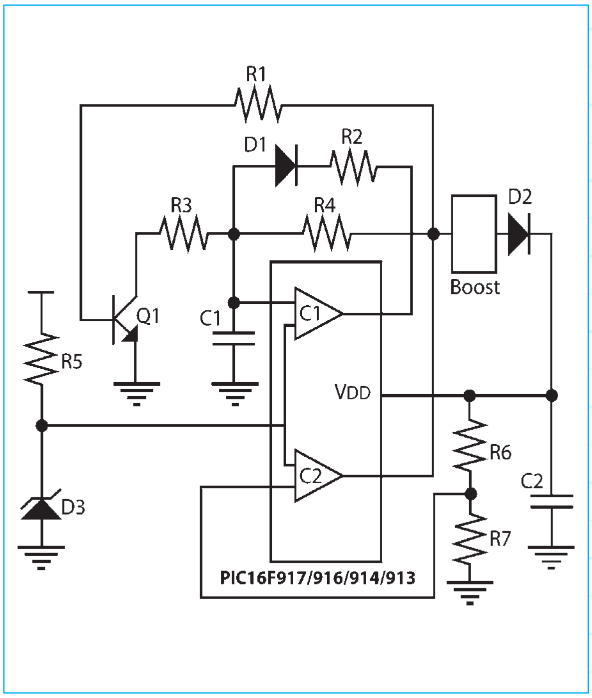

Figure 2: Boost converter

The two methods of producing a boost converter are shown in **Figure 3**. The first circuit is simply a switched capacitor type of circuit. The second circuit is a standard inductor boost circuit. These circuits work by raising VDD. This allows the voltage at VLCD to exceed VDD.

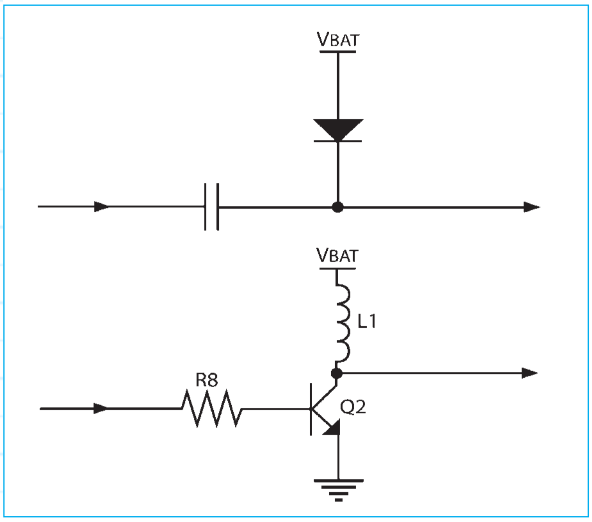

Figure 3: Two types of boost converters

➲TIP 3: Software-controlled contrast with PWM for LCD contrast control

In the previous contrast control circuits, the voltage output was set by a fixed reference. In some cases, the contrast must be variable to account for different operating conditions. The CCP module, available in the LCD controller devices, allows a PWM signal to be used for contrast control. In Figure 4, the buck contrast circuit is modified by connecting the input to RA6 to a CCP pin. The resistor divider created by R4 and R5 in the previous design are no longer required. An input to the ADC is used to provide feedback but this can be considered optional. If the ADC feedback is used, notice that it is used to monitor the VDD supply. The PWM will then be used to compensate for variations in the supply voltage.

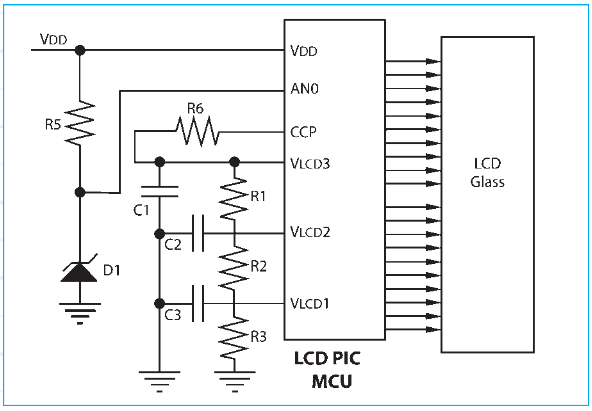

Figure 4: Software-controlled voltage generator

➲TIP 4: Driving common backlights

Any application that operates in a low-light condition requires a backlight. Most low-cost applications use one of the following backlights:

1) Electroluminescent (EL)
2) LEDs in series
3) LEDs in parallel

Other backlight technologies, such as CCFL, are more commonly used in high brightness graphical panels, such as those found in laptop computers. The use of white LEDs is also more common in colour LCDs, where a white light source is required to generate the colours. Driving an Electroluminescent (EL) panel simply requires an AC signal. You may be able to generate this signal simply by using an unused segment on the LCD controller.

The signal can also be generated by a CCP module or through software. The AC signal will need to pass through a transformer for voltage gain to generate the required voltage across the panel. LEDs in series can be easily driven with a boost power supply. Figure 5 depicts a simple boost supply with a pulse applied to the transistor. The pulse duration is controlled by current through R2. When the pulse is turned off, the current stored in the inductor will be transferred to the LEDs. The voltage will rise to the level required to drive the current through the LEDs. The breakdown voltage of the transistor must be equal to the forward voltage of the LEDs multiplied by the number of LEDs. The comparator voltage reference can be adjusted in the software to change the output level of the LEDs.

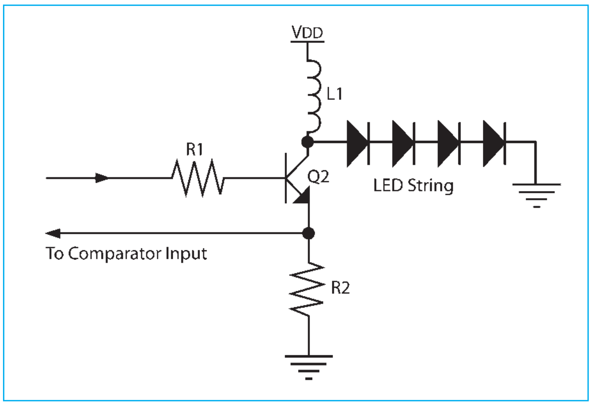

Figure 5: Simple boost supply

If the LEDs are in parallel (Figure 6), the drive is much simpler. In this case, a single transistor can be used to sink the current of many LEDs in parallel. The transistor can be modulated by PWM to achieve the desired output level. If VDD is higher than the maximum forward voltage, a resistor can be added to control the current, or the transistor PWM duty cycle can be adjusted to assure that the LEDs are operating within their specification.

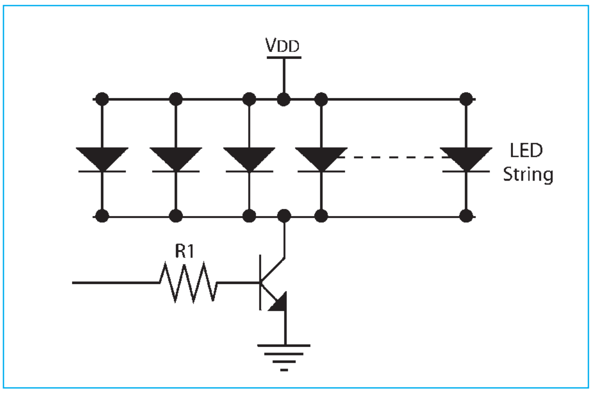

Figure 6: LEDs in parallel

Win a Microchip rfPIC Development Tool

Electronics World is offering its readers the chance to win a Microchip rfPIC Development Kit. The kit provides an easy way to evaluate low-power RF communication links for embedded control applications. Designed to work in tandem with the PICkit 1 Flash Starter Kit, the rfPIC Development Kit 1 includes transmitter and receiver modules supporting frequencies of 315MHz and 433MHz.

The receiver modules feature an rfRXD0420 device that plug directly into the PICkit 1 development board. The modules are available separately so designers can create several prototypes based on the same module, without having to develop an actual RF design. All the design files are available, offering users the ability to migrate their module design into the application for lower cost volume production. Target applications for the rfPIC family include remote control, wireless sensors, automotive and home security.

The self-contained rfPIC12F675 transmitter modules are based on a PICmicro 20-pin Flash microcontroller that features an integrated UHF RF transmitter. The transmitter modules feature button inputs for remote control functions and analogue input that can be used for the evaluation of the microcontroller A/D converter peripherals. Code can be developed using Microchip's MPLAB Integrated Development Environment. Programming the microcontroller is easily accomplished by plugging the modules into the PICkit 1 Flash Starter Kit.

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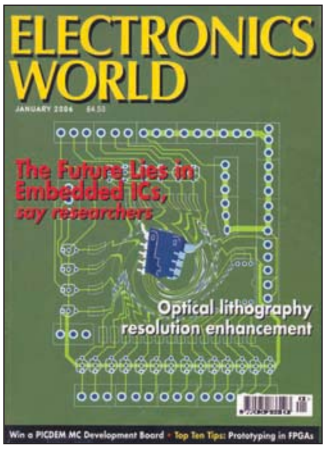

Particular likes

I have been a regular reader of Electronics World for a long time. I liked the January 2006 issue of your magazine in general and “PC-to-PC Communication via RS-232 Serial Port Using C” in particular. The author Varun Jindal has done a nice job in presenting the guidelines for establishing serial communication.

Sumedha Goel
India

Rise of the machines

A report by the International Telecommunications Union (ITU) indicates that machines are to overtake humans as the main users of the Internet. There would be an ‘Internet of Things’, where tens of billions of electronic sensors, control everything from our energy use to groceries.

Many would worry about a potential ‘rise of the machines’ scenario, however, I see this as a great opportunity.

In the 21st century we all lead ever more hectic lives and there are many demands on our time. This could all now change. Our refrigerators could independently communicate with grocery stores, making the weekly shop a thing of the past. There are already innovations that enable sophisticated control equipment to be accessed via the Internet from anywhere — machines truly using the web! The scenario where machines become a majority on the Internet can only lead to easier lives for the rest of us. People always fear change. Science fiction has taught us fear of technology, but practicality unveils a different vista. With time though, people will come to accept their silicon masters.

Andy Parker-Bates
Customer Marketing Manager
Schneider Electric

Going backwards with technology?

I read with interest a reader in February’s edition commenting on receiving mild electric shocks from an LNA while being at the top of a ladder and whether it seems we may be going backwards with technology.

In the same way that EMC compliance pass can be legally attained by applying spread-spectrum to the system clock, so as to fool EMC measuring equipment into being unresponsive, it is also legal to allow an amount of leakage from mains supply to the ground/chassis of consumer electronics under the guise of common-mode emissions, where such equipment is double-insulated and, therefore, not requiring an earth.

What the reader was observing is the allowable primary/secondary leakage via the ‘Y’ capacitor. To some, receiving even a very mild shock in such circumstances would be catastrophic but, of course, you find in the user manual they demand that you unplug from the supply when even so much as plugging in a SCART cable.

Indeed, in days past, adjustments to antenna pointing would best be done while the TV is operating in real time and the earthing of antenna feeds was a legal requirement. So, yes, we are in some ways going backwards in real terms when it comes to technology. Unfortunately, the public at large is very easily blinded by ‘digital science’. As long as it’s got more gigabytes or megapixels and, God forbid, it’s not the dreaded hippy-culture ‘analogue’, it’s always perceived automatically better just because the simple fact that it’s ‘digital’.

But in real terms, are the masses getting better mobile call quality, TV pictures and radio reception? When compared to budget electronics that dominated before the digital revolution it may be the case, but just step back from the ‘digital is better’ hype a minute and take a look again—digital TV receivers of all types exhibit picture movement that is smeary and smudgy (with LCDs especially); because of compression the lip-sync is often poor and slowly moving parts of the picture cannot make up their mind whether they are supposed to be moving or remain part of the still image background. What you are seeing is locally-generated computer graphics animated by the vector movements of live performers, rather than the analogue TV way of transmitting every screen point equally through the media which behaves as a virtual lens, this being almost as it occurs in the real world that we perceive through the lens of the eye to the retina.

The viewer now is faced with 500 diluted channels of ‘nothing on’ and having to constantly channel-hop to avoid adverts, one wonders if all that bandwidth spread over so many channels was a good thing? Consumers, sadly, only seem to judge the picture quality solely by its width and the absence of snow on the screen. Even cinemas now are showing compressed digital screens and films of which the whole picture dissolves into a complete blur of a substance like mixed together plasticine, whenever the camera is panned, which is certainly not what the director intended.

Then, of course, there’re mobile phones that had reached their performance peak in the early 90s before cloning became a problem. The dominant business sector of the market had always demanded clear and intelligible call quality foremost, rather than pay-per-play Tetris or being able to GPS-navigate their way to and from the local supermarket. Anyone who had the past fortune to use a good analogue mobile phone will remember calls were so clear that you could actually hear music through them. Business calls and discussions would be shorter and more efficient, because the absence of the delay allowed each other to ‘cut in’ mid-sentence, in real time, rather than nowadays digital offering which is effectively hearing each other through a codec robot interpreter impersonating the voices, breaking up the natural flow in verbal communication that analogue phones preserved. Again, the consumer only judges call quality by how loud it is, the signal strength indicator and whether it has a reserve of volume adjustment.

When the Philips audio Compact Disc (CD) arrived over 20 years ago, it was a pinnacle of audio sound quality. It had to be, in order to compete with the high-end consumer hi-fi equipment of the day. At last, here was a cheap mass-produced technology that approached the dynamic range and frequency response the typical 2-inch wide tape, 24-track tape and similar width stereo master tape that had sourced the music. Though it was 16-bit in its basic form, there was absolutely no compression or other encoding apart from the A-D-A and error-correction using redundant data to reconstruct natural data dropouts in the media. One might argue that the CD is not actually 'digital' at all in today's sense and the only digital thing about it is the form the sequential recorded DVM readings that make up the analogue waveform take when in the digital domain. Now, that MP3 with its characteristic tonal distortion is often heard on commercial radio stations, begs the question what has happened to all the hi-fi buffs who could tell the difference between different types of copper in speaker cable? We need you.

Digital technology today attracts data compression because the higher the compression, the less media is used, this being the one thing where the most savings can be made, whether the media is EM signal bandwidth, a mini-disk or whether carrying just a mobile ring-tone data, the ultimate in compression to selling-price ratio. It seems, at the present time, the tradeoffs that drive consumer technology are over-influenced by accountants seeking to maximise bums-on-seats in the name of consumer choice and cram everything into the available bandwidth to sell more product and not enough by the artists, performers, producers and directors often in the business out of love rather than money, who would rather not see their work mutilated by poorly-performing decompression algorithms, largely going unnoticed by an indifferent public easily blinded by digital science.

Mark Barker
UK

Problem solving challenge

I am an Electronics and Communication engineering student studying at the CIT in Karnataka. I have started working on a project that I hope you will be able to help me with.

Part of it includes a transmitter, which sends a simple but continuous message within a range of 300-500 meters, and a receiver. The received message is then input into a microcontroller (8051) to be display on a screen. The circuit must be very low cost.

I hope you can give an idea of what techniques, modulation methods and schematics I should use.

Varunjith.T.K
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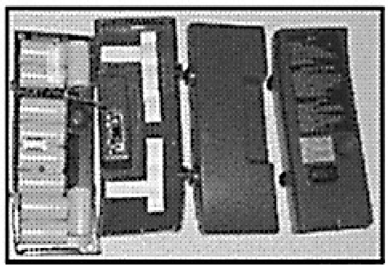
866 battery pack originally intended to be used with an orbitel mobile telephone it contains 10 1.6Ah sub C batteries (42x22dia the size usually used in cordless screwdrivers etc.) the pack is new and unused and can be broken open quite easily £6.46 + VAT = £8.77



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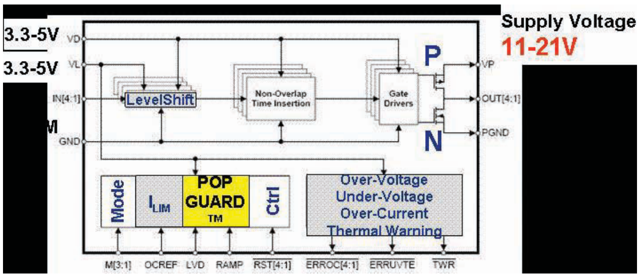
Full Stereo Class-D Amplifier Reference Design



Cirrus Logic has completed its first full production-ready reference design for stereo and 2.1-channel Class D digital amplifier applications.

Central to the Class D reference design is the CS4460 digital amplifier controller and the new CS44130 power stage IC. Because it eliminates the need for an expensive, bulky heatsink on board designs, this reference design is suitable for digital televisions, home theatre systems, DVD receivers and shelf systems, PC sound cards and networked audio systems.

The CS44130 packs up 60W of power and is thermally and electrically self-protecting, making it simple to design digital amplifiers into less than two square inches of board space.

The IC can power subwoofer channels with up to 58W without generating excess heat. The input logic accepts 3.3V as well as 5V control signals, enabling it to also work with other integrated PWM modulators in digital TV and other home theatre applications.

www.cirrus.com

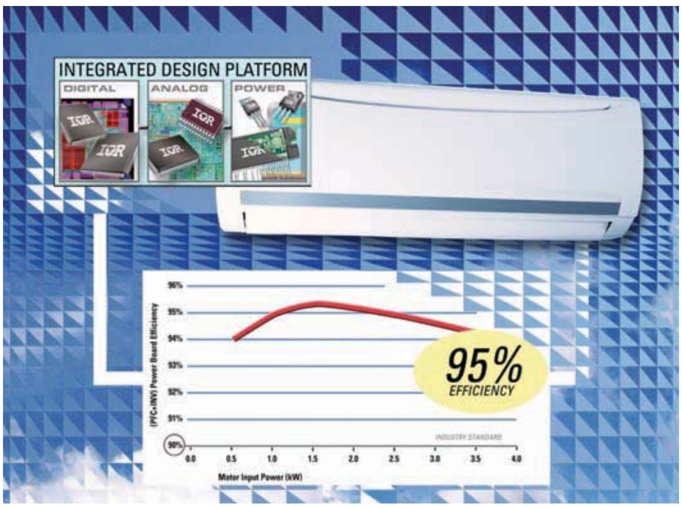
Colour Contact Image Sensor

Pacer, a UK based provider of optoelectronic devices, announces the introduction of the Color contact image sensor (CIS) from Tichawa Vision GmbH. Promising large reading width, high resolution and scan speeds. The rugged, industrial-grade sensor has applications within process and quality inspection for the paper, print and industrial sectors. The scanning width of 530mm is provided by two sensor boards joined end to end. With line rates of up to 40kHz representing a maximum scan speed of 300m/min at a high spatial resolution of 200dpi, productivity and inspection or capture quality is significantly improved and the process speed maximised.

Utilising standard camera link connectivity to frame-grabber chip and having integrated white lighting and optics, the CIS is easy to use as part of PC-based industrial process equipment. Maintenance is decreased and downtime minimised by the provision of a simple alignment mechanism. Pixel binning is employed to reduce read and systemic noise giving the effective resolution of 200dpi and flat field correction is employed to normalise pixel sensitivity. There are three (Red, Green and Blue) detectors per pixel and 4222 of these ‘colour’ pixels. The optimal working distance for the detector is 10mm.

www.pacer-components.co.uk

iMOTION Saves Energy in Airconditioning



International Rectifier (IR) has introduced a motor control platform, optimised for the airconditioning market. The firm claims it offers a 95% efficiency, quieter operation and mechanical simplicity.

The platform, dubbed iMOTION, is based on IR’s proprietary high voltage integrated circuit (HVIC) technology with analogue, digital and power building blocks, along with digital control algorithms. The platform also includes power factor correction (PFC).

The chipset provides sensorless control of Permanent Magnet Synchronous Motors (PMSM) using one dc link current shunt. The digital block consists of the IRMCF3xx family of digital control ICs, which includes the so-called Motion Control Engine (MCE) that implements the complex sensorless PMSM algorithm in hardware, eliminating the need for software coding from the development process.

The analogue section uses the IRS2136D family of three-phase analogue driver and protection ICs. These incorporate three independent 600V half-bridge inverter gate drivers with built-in bootstrap diodes.

With this platform, there’s no need for external active components, and field failures are avoided by eliminating the Hall IC in fan control.

www.irf.com

Motor Drivers/Controllers

Here are just a few of our controller and driver modules for AC, DC, unipolar/bipolar stepper motors and servo motors. See website for full details.

NEW! Bidirectional DC Motor Controller

Controls the speed of most common DC motors (rated up to 32Vdc/5A) in both the forward and reverse direction. The range of control is from fully OFF to fully ON in both directions. The direction and speed are controlled using a single potentiometer. Screw terminal block for connections.
Kit Order Code: 3166KT - **£15.95**
Assembled Order Code: AS3166 - **£25.95**

DC Motor Speed Controller (5A/100V)

Control the speed of almost any common DC motor rated up to 100V/5A. Pulse width modulation output for maximum motor torque at all speeds. Supply: 5-15Vdc. Box supplied. Dimensions (mm): 60Wx100Lx60H.
Kit Order Code: 3067KT - **£12.95**
Assembled Order Code: AS3067 - **£20.95**

NEW! PC / Standalone Unipolar Stepper Motor Driver

Drives any 5, 6 or 8-lead unipolar stepper motor rated up to 6 Amps max. Provides speed and direction control. Operates in stand-alone or PC-controlled mode. Up to six 3179 driver boards can be connected to a single parallel port. Supply: 9Vdc. PCB: 80x50mm.
Kit Order Code: 3179KT - **£11.95**
Assembled Order Code: AS3179 - **£19.95**

NEW! Bi-Polar Stepper Motor Driver

Drive any bi-polar stepper motor using externally supplied 5V levels for stepping and direction control. These usually come from software running on a computer.
Supply: 8-30Vdc. PCB: 75x85mm.
Kit Order Code: 3158KT - **£14.95**
Assembled Order Code: AS3158 - **£29.95**

Most items are available in kit form (KT suffix) or assembled and ready for use (AS prefix).

Controllers & Loggers

Here are just a few of the controller and data acquisition and control units we have. See website for full details. Suitable PSU for all units: Order Code PSU345 £9.95

Rolling Code 4-Channel UHF Remote

State-of-the-Art. High security. 4 channels. Momentary or latching relay output. Range up to 40m. Up to 15 Tx's can be learnt by one Rx (kit includes one Tx but more available separately). 4 indicator LED 's. Rx: PCB 77x85mm, 12Vdc/6mA (standby). *Two and Ten channel versions also available.*
Kit Order Code: 3180KT - **£39.95**
Assembled Order Code: AS3180 - **£47.95**

Computer Temperature Data Logger

4-channel temperature logger for serial port. °C or °F. Continuously logs up to 4 separate sensors located 200m+ from board. Wide range of free software applications for storing/using data. PCB just 38x38mm. Powered by PC. Includes one DS1820 sensor and four header cables.
Kit Order Code: 3145KT - **£17.95**
Assembled Order Code: AS3145 - **£23.95**
Additional DS1820 Sensors - **£3.95 each**

NEW! DTMF Telephone Relay Switcher

Call your phone number using a DTMF phone from anywhere in the world and remotely turn on/off any of the 4 relays as desired. User settable Security Password, Anti-Tamper, Rings to Answer, Auto Hang-up and Lockout. Includes plastic case. Not BT approved. 130x110x30mm. Power: 12Vdc.
Kit Order Code: 3140KT - **£44.95**
Assembled Order Code: AS3140 - **£64.95**

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Kit Order Code: 3108KT - **£54.95**
Assembled Order Code: AS3108 - **£64.95**

Infrared RC Relay Board

Individually control 12 on-board relays with included infrared remote control unit. Toggle or momentary. 15m+ range. 112x122mm. Supply: 12Vdc/0.5A
Kit Order Code: 3142KT - **£42.95**
Assembled Order Code: AS3142 - **£52.95**

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Assembled Order Code: AS3128 - **£39.95**

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Assembled Order Code: AS3117 - **£24.95**

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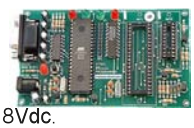

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Kit Order Code: 3123KT - **£24.95**

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Kit Order Code: 3149EKT - **£37.95**
Assembled Order Code: AS3149E - **£52.95**

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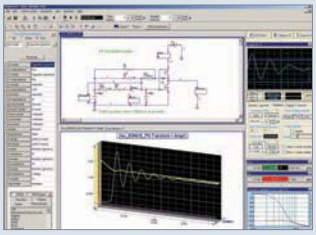

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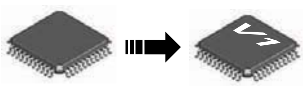

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- Lech Tomawski explains how to use RLC and RCL sections to create resonant circuits
- Profile of Sony – one of the largest consumer companies in the world