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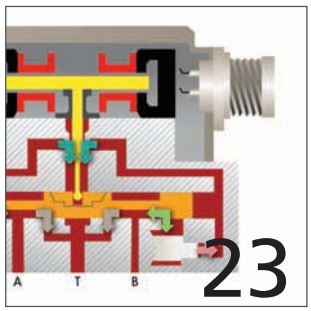

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WHAT'S WRONG WITH THIS PICTURE?

Late last year the UK's industry regulator Ofcom initiated a consultation on its proposals for upgrading Freeview (a free digital service) for High Definition Television (HDTV). Digital TV Group, or DTG, is an industry association for digital TV in the UK, and it is just one of the organisations to comment on that consultation.

While it seems to welcome Ofcom's recognition that HDTV public service broadcasts should be provided for on the digital terrestrial platform (DTT), it also expressed concerns that the regulator's proposals could seriously compromise DTT's long term viability and the platform most adopted by UK viewers and consumers that is Freeview. In turn, DTG is calling for a comprehensive national strategy for HDTV, encompassing all television platforms.

Ofcom proposes that the HDTV service on DTT will be restricted to only between three and four channels. But, this will inevitably threaten the picture quality of HDTV programming, as well as the reach of the existing standard definition channel line-up. If HDTV is broadcast on less number of channels this will save on spectrum (which I assume will then be sold on for a hefty profit to others), but this defies the object of the whole exercise of having HDTV in the first place, which by default should be a lot higher in quality than anything seen to date.

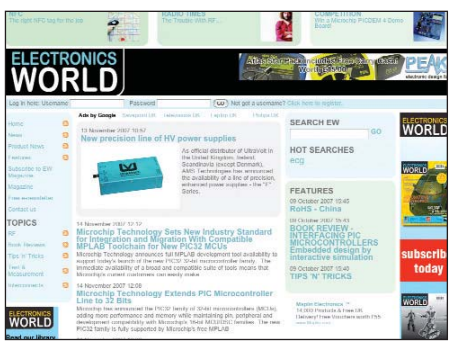
DTT is still the UK's most popular digital television platform with over 14 million units sold and many are led to believe that HDTV will offer unmissable viewing experience. If that experience is no longer to be, then why are millions of viewers shelling out thousands of pounds on 'HD-ready' plasma and LCD screens?

So far there has been heavy promotion of all services digital (radio, TV etc) but why is Ofcom making a U-turn when it comes to the quality of such services. And why is the industry (chip makers, set-top box manufacturers, television set suppliers etc) not kicking up some fuss over this?

Some years ago, the UK (and in particular the BBC), was at the forefront of adopting, testing and promoting new broadcast technologies, but a little under ten years and we are seeing a completely different and, excuse the pun, very fuzzy picture emerging.

It will be disheartening to see the UK which once stood at the helm of new broadcast technologies end up with second class HDTV services.

Svetlana Josifovska
Editor



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Femtocells create buzz but leave questions unanswered

The biggest challenge in femtocell use is who is going to meet the cost of the subscriber box

Mobile operator O2 is starting trials of femtocell technology in the UK with plans for a commercial launch next year. This announcement at the Mobile World Congress in Barcelona created a buzz around the show as exhibitors jostled to display their femtocell offerings.

In a way, this is strange given that the introduction of femtocells is almost an admission of failure by the mobile operators, which for a long time have boasted about how widespread their coverage is.

Users though have known for a long time that, while city centre coverage is normally fine, residential coverage is patchy to say the least. The idea behind femtocells is that each home can buy a box that will boost mobile phone coverage in their own home.

But there are problems. First, and the big headache at the moment, is who will pay? Consumers are not going to be over happy about splashing out between $100 and $200 (rough estimates from different firms at the show) for a box to give them the sort of reception they are meant to be getting anyway.

"The biggest challenge is who is going to meet the cost of the subscriber box," said Rakesh Vij, assistant vice president of communications software company Aricent. "Once the volume goes up, the price will drop, but someone still has to pay."

Some believe that the mobile phone operators themselves will subsidise the cost as a way of keeping subscribers on their network. But what about homes in which different people are on different networks? A single box can handle that and boost the coverage for all the networks it can see, however it is felt that a network operator is unlikely to fund a box that will boost the reception for its rivals and will insist that the boxes are locked to its network. Do not be surprised therefore to see "unlock your box" signs springing up next to the "unlock your phone" signs in shops around the country.

Another option will be mobile virtual network operators (MVNOs) that have roaming agreements with the different main operators and will sell multi-operator boxes.

As to the O2 trial, this is being done in partnership with NEC and Ubiquisys, which is making the boxes.

"The technology is ready," said Will Franks, chief technology officer at Ubiquisys. "We have done our own trials. We have made 1000 boxes so far and they are out there being tested."

Mobile phone jackets for each season

"Tiny, slick and stylish," says Modu about its latest mobile phone

Israeli company Modu believes it has solved the problem of people who like to keep up with the latest mobile phones trends and yet are stuck with upgrading only every 12 to 18 months.

The company was showing at the Mobile World Congress in Barcelona what it claims is the world's smallest and lightest mobile phone (a claim that marketing vice president Tzahi 'Zack' Weisfeld said was verified by the Guinness Book of Records) and that the phone would fit into different jackets to give it different functionalities.

The company was quick to point out that this was not just changing the cover; that is a modular phone that's designed to be slotted into various attachments such as clothing, briefcases or other consumer devices. The device allows message texting, MP3 playback and is Bluetooth enabled among others.

Inserting the phone into a jacket can transform its functionality. City jackets are a good example. If the user is roaming in a city they are not familiar with, they could buy a jacket for that city. The phone would be inserted into it, and then the screen would display maps of the city with information about restaurants and points of interest. Alternatively, the phone could be a business email terminal with qwerty keyboard during the working day. A quick switch of jackets after work and it becomes an MP3 player with high quality speakers.

Each jacket contains an ASIC that controls the interface between the jacket and the phone. For more advanced jackets, such as those with GPS facilities for example, the jacket will contain an extra co-processor to handle that functionality.

"I suspect people will start launching seasonal collections," said Weisfeld. "It takes a lot of time and money to make a phone and certify it. It is a lot less to make a jacket and you don't have to certify it."

The company has already signed deals with some operators and commercial launches are scheduled for October in Brazil, Israel, Italy and Russia, with other countries to follow.

IN BRIEF

● **UK consultancy and engineering firms are among the best to work for, according to a recent survey by the Association for Consultancy and Engineering. These firms are now close to financial services companies as the most successful sector in the 2008. The Association's chief executive Nelson Ogunshakin said: "UK consultancy and engineering firms are world leaders in design, business practices, professionalism, profitability and staff happiness."**
"Those of us in the industry understand that an engineering career is unique. It offers the opportunity to contribute to processes that could affect how people live in hundreds, perhaps thousands of years. It is not surprising that the staff at engineering firms feel so fulfilled," he said.

● **Following the launch of the science and innovation strategy by the UK's government in March, the CBI's Director-General, Richard Lambert said that the government talks the "right kind" of talk but needs to follow it with action.**
"It is important we look at our 'innovation ecosystem' as a whole and don't just think of innovation as 'doing science' or 'inventing things'," said Lambert.
He added that the government can play a big role by harnessing some of its massive £150bn annual spend on goods and services and helping to kick-start new markets for innovative ways of doing things and tackling big issues such as climate change and security.

● **The worldwide market for semiconductor assembly and test services (SATS) grew for the sixth consecutive year in 2007, according to industry analyst firm Gartner. Worldwide SATS revenue was up 7.4% at $20.6bn. For the sixth year in succession, the SATS market continued to outpace the overall semiconductor market by more than 50% (overall semiconductor revenue grew 2.9% in 2007).**
Packaging, assembly and test services have become important in the total semiconductor industry because a growing percentage of the total industry revenue is now attributed to this segment. The outsourcing portion of this back-end manufacturing process, known as SATS, has grown steadily since the recession of 2001.

Mobile phone security keeps in tune

A method of verifying that the person talking on a mobile phone is really who they say they are will be music to the ears of banking and other financial institutions.

The clever technology comes from Yves Eonnet, who was once head of innovations at Schlumberger's smartcard division but now runs Tagattitude, a company he set up to offer a service to let mobile phone users sign transactions securely.

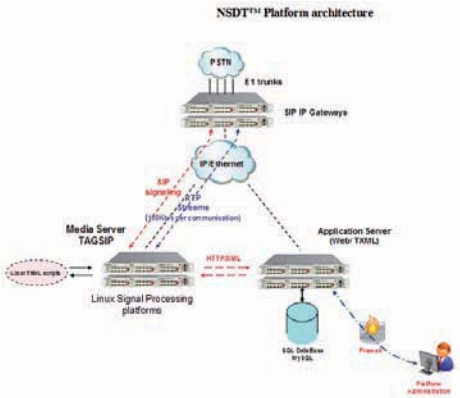
Using audio signal processing, the system combines music and passwords to verify a user's identity. With an online transaction, the user enters a log-in and password onto a web site in the normal way. Two seconds later, the mobile phone rings. The user answers it and the web site then plays music that contains an encrypted one-time password that is heard down the phone line.

"This guarantees that your phone is in front of the web page," said Eonnet.

The system can also be used to authenticate a user in front of a bank ATM money machine and even to authorise a transaction between two users without them even knowing who each other is. One user can enter the amount to pay on his or her phone and the recipient does the same on their phone and then the two phones play a signal to each other to verify the transaction.

"The phone becomes like a bank card for people," said Eonnet. "This is important for developing countries where most people don't have bank accounts. They can use their phone with a prepaid account."

There are pilot schemes running in three countries in Africa, including the Ivory Coast, done through France Telecom's Orange mobile phone subsidiary. French bank Crédit Agricole is also about to implement the technology for online transactions.



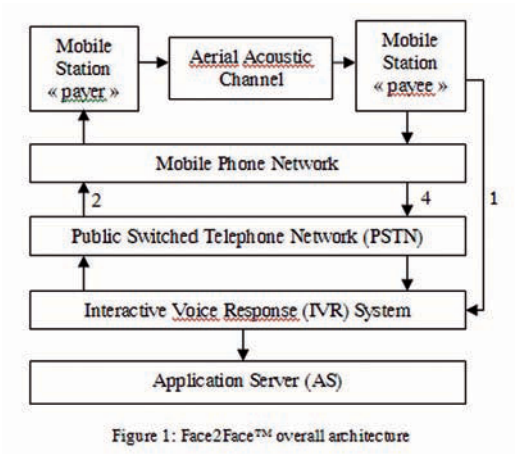


Figure 1: Face2Face™ overall architecture

The platform which allows the mobile phone to become a bank card for users

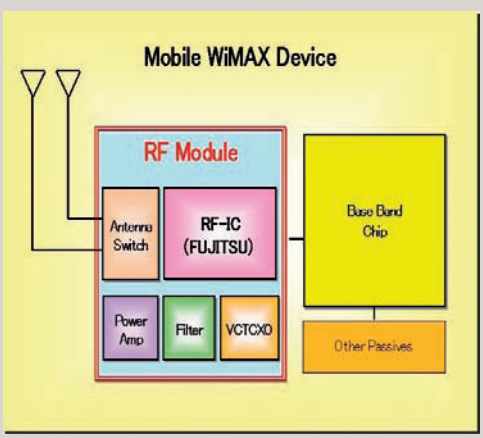
WORLD'S SMALLEST IS ABOUT TO GET SMALLER

Fujitsu was showing off its mobile WiMax baseband chip at Mobile World Congress in Barcelona but was promising more to come before the year is out.

The WiMax RF module fits into a 15x15mm form-factor and is claimed to be the world's smallest to contain all the RF circuits needed for mobile WiMax, including RF IC antenna switches, power amplifier, filters and oscillator circuits.

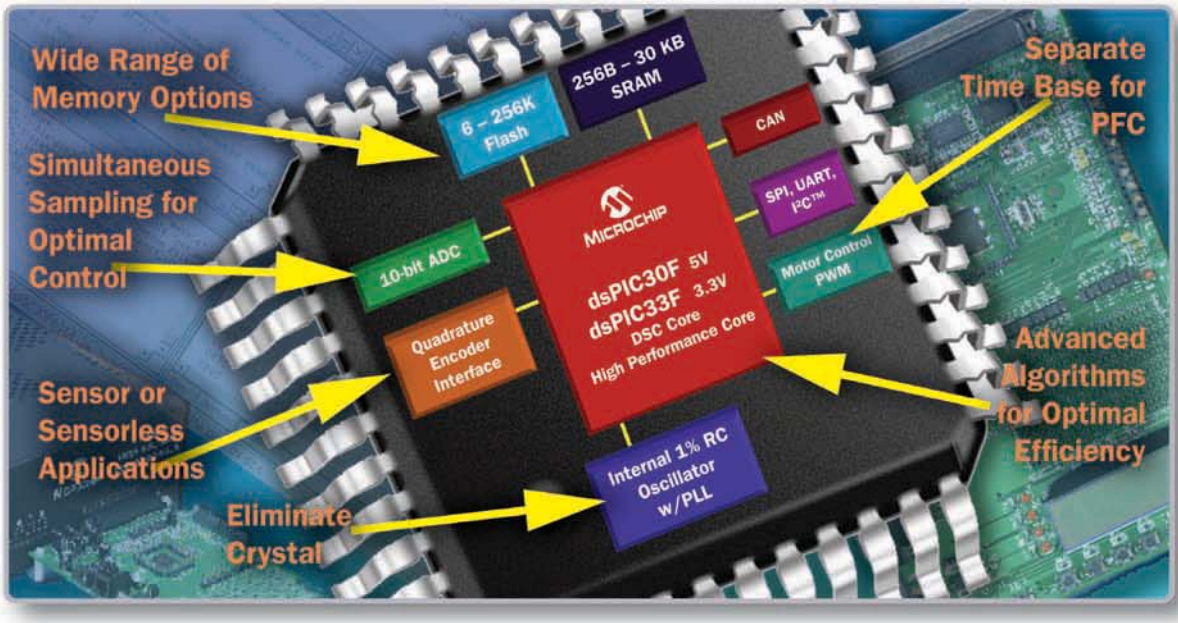
But Manfred Mettendorff, senior marketing manager, said that by July or August this year the firm would have its second generation chip that would combine all that with power management circuitry and memory in the same form-factor. This will be done using 65nm process technology compared with 90nm for the existing chip.

"The current one is targeting PC applications," he said."The new one will target battery-driven mobile devices because of its lower power consumption.



Block diagram of Fujitsu's WiMax IC solution

More Efficient 3-Phase Motor Control



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Top Five Tips

Survival for Communications, Media and Entertainment Companies

01. What business am I actually in?

What exactly is my business offering? Who are my customers today and who will be my customers tomorrow? What do they want?

Telcos need to understand that there is more to the next generation of networks than just technology rollout. Operators are starting to wake up to the fact that 'build it and they will come' is no longer true. Indeed, the ramifications run very deep within the company. As communications technologies begin to converge, companies are starting to compete with organisations that have previously been in complementary markets. This is leading to the question 'who am I?' The confusion is both internal and external and needs to be answered, clearly defined and brand adjusted accordingly.

Sounds simple? Well, no. Some operators are lucky to have been seen more as a conglomerate offering a wide range of communications and have been accepted as such. Most operators aren't so lucky being seen as a media broadcaster or mobile operator leading a very expensive network that isn't being utilised properly.

Never think of a network as just technology rollout but understand that the whole company may need to be augmented behind it, fundamentally changing strategy.

02. Network sharing: Can it really deliver 40% savings on my network running costs?

Most of the business cases that we have seen for network sharing suggest that the long term benefits amount to around 25-35% of total network costs. Of course, the achievable savings depend very much on which elements of the network are shared.

What immediately springs out from these figures is the fact that the higher the share of new build in the overall costs, the greater the ultimate benefits. Intuitively this makes sense as it avoids all the messiness of consolidating legacy infrastructure, however it does raise an important point. The degree of alignment in the plans of the sharing operators for their network deployment will have a very significant impact on the ultimate benefits. Choosing your partner with care and forming the right 'pre-nuptial' agreement is vital to ultimate success. In reality however, few operators have the luxury of ignoring the legacy infrastructure so it is important to strike the right balance between the costs and complexity of consolidating legacy networks with the higher benefits of full sharing. Typically, we find that sharing around 2/3 of the infrastructure is about the best that can be sensibly achieved without agreeing a roaming arrangement, which is not possible everywhere.

03. How can I find a strategy for winning in wireless broadband?

With 3G networks lying largely empty, the industry is asking why 4G will be any different. The industry has learnt its lessons from 3G. It is making sure that the user experience, devices and services are going to be in alignment so that one does not fail the other.

But, there is one final elusive factor: demand. What is going to happen to drive demand for 4G? The answer is sitting in households all over the world, namely the digital native. These are the currently teenage generations who stack their communications using Facebook at the same time as watching TV and accessing YouTube. This is very different to the way anyone uses technology at the moment. When this generation enters the workplace and starts paying the bills then the demand for such user experience anywhere anytime will drive the demand for 4G. With this generation just around the corner, operators need to decide 4G strategy now. The clock is ticking.

04. Should I migrate my mobile customers from 2G to 3G and when?

Over the next five years, mobile operators face the challenge of increasing traffic demand while competitive pressure reduces voice revenues. For many, success will revolve around achieving cost efficiency while seeking new revenues from high speed data. Following a significant investment in 3G, operators are asking: "Is now the time to migrate customers to a network that can leverage more revenue while reducing OPEX?"

05. Do femtocells have a future?

The concept of the femtocell has caused excitement in the 3G infrastructure and operator world as well as with new players. From the concept perspective at least, it is quite revolutionary – equipment volumes of millions provided directly to consumers, short lifetime providing rolling market for manufacturers, connected to a backhaul funded by users, reduced customer churn beyond that provided by attractive handset bundles. It is ideally suited to solve 3G network problems of poor indoor coverage and capacity and to reduce network CAPEX and OPEX.

If it is to become a successful mass market product, a femtocell basestation must have a packed-up factory-gate cost of no more than £50 in volume production. Partitioning the design shows that this leaves only about £20 for the complex processing platform, compared with its macrocell counterpart that typically costs hundreds or thousands of pounds. The question is can a digital processing platform provide the processing needs for the femtocell product and meet this aggressive cost target?

This month's top tips were supplied by Chris Buist, Member of PA's Management Group at the PA Consulting Group. You can find out more by going on PA's website www.paconsulting.com/telecoms

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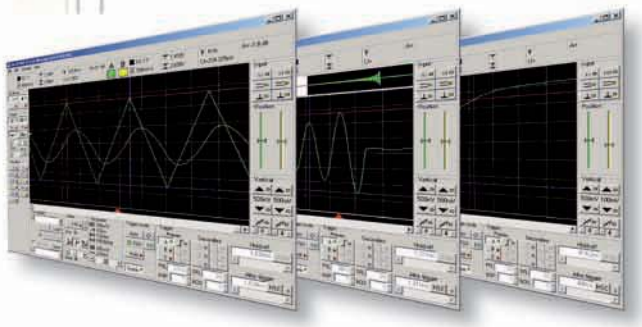

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AT THE HEART OF MODERN COMMUNICATIONS

JUAN PABLO CONTI TALKS TO PICOCHIP, THE BATH-BASED SUPPLIER OF A DSP-TYPE OF ARCHITECTURE SUITABLE FOR DIFFERENT TYPES OF WIRELESS COMMUNICATIONS STANDARDS

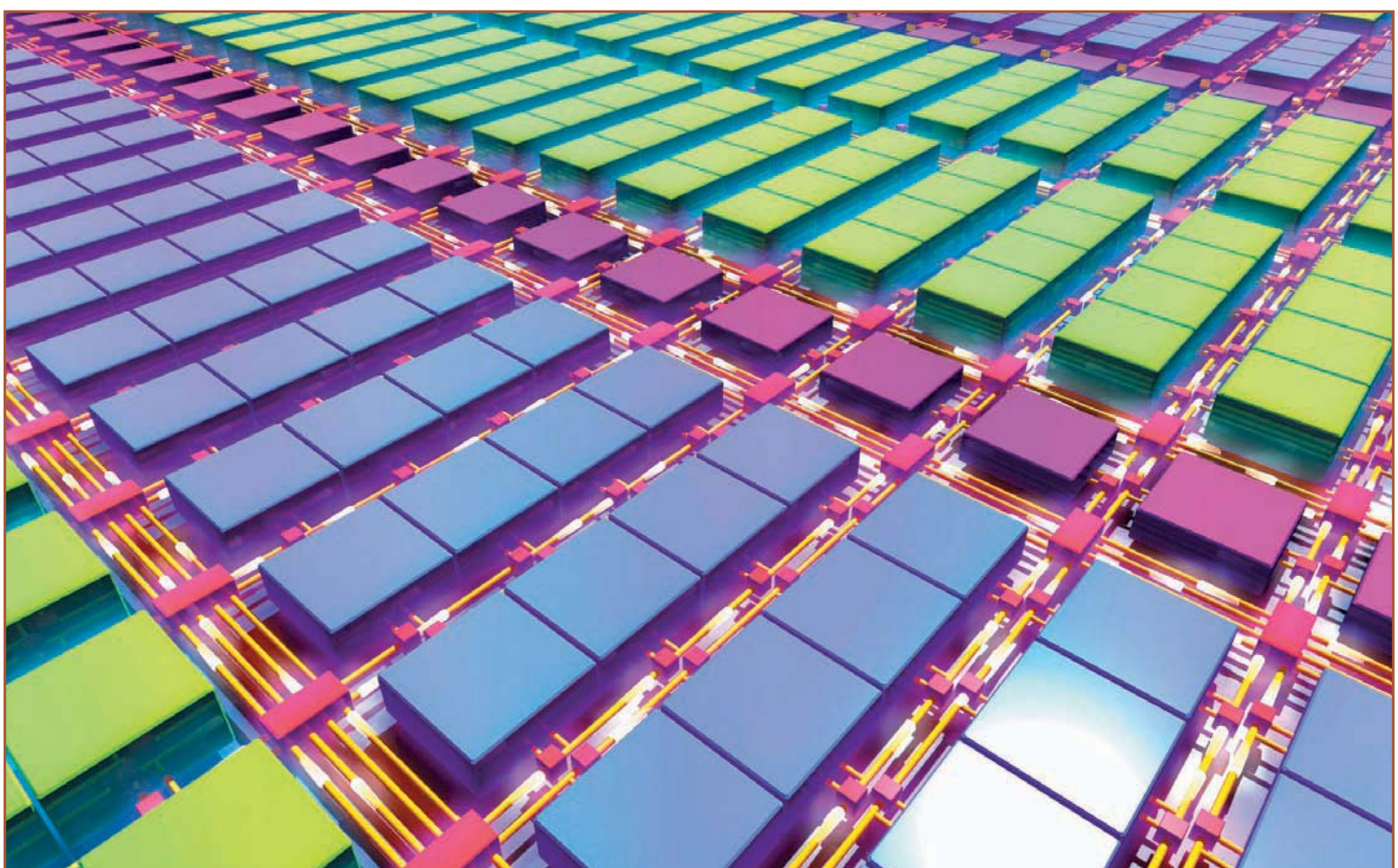
Much in the same style as Formula One broadcasts today include a variety of onboard video shots that show the action from the driver's point of view, come August 2008 TV audiences around the world will be able to enjoy a similar experience during the Beijing Olympics.

Of course, motor racing is not an Olympic sport, but sailing and rowing are. Boats competing in the coastal city of Qingdao and the Shunyi suburb of Beijing will be fitted with tiny cameras and transmitters that will be using a new form of mobile broadband wireless communications technology to relay the live images. Called McWiLL (Multi-carrier Wireless information Local Loop), the radio standard has been developed entirely in China by Xinwei Telecom Technology.

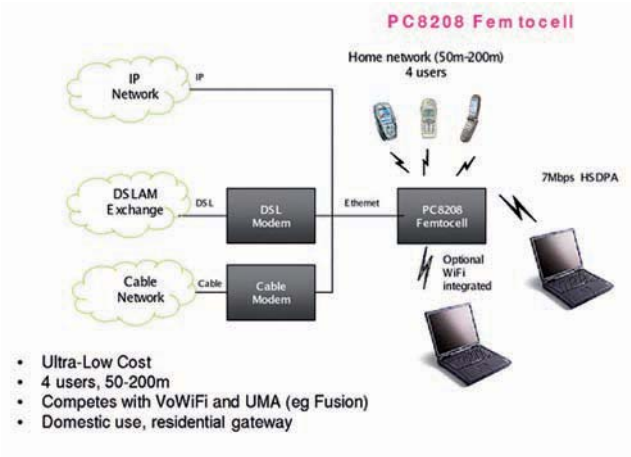
At the heart of each McWiLL base station, silicon developed by Bath, England-based DSP specialist picoChip will be taking care of the baseband processing functions.

Interestingly, it was supposed to be a DSP market leader that was going to be supplying this crucial part of the system. The original design stipulated the use of nine DSPs and two large FPGAs from that firm. However, when in November Xinwei revised the base station's technical specifications, it realised the eleven devices could actually be swapped by just two of picoChip's PC203 ICs, significantly lowering bill of materials and power consumption.

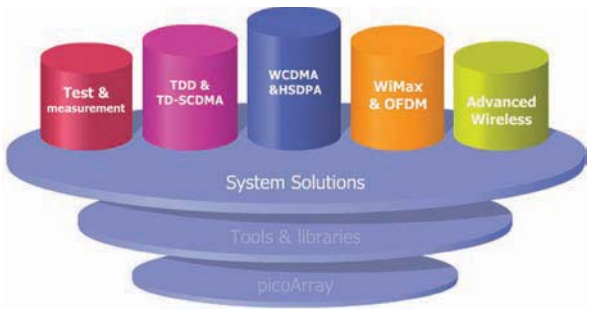
The story – which it must be said comes from picoChip – lends credit to two of the main marketing claims that are helping this fabless company make a name for itself in the semiconductor world: 1) that its massively multi-core chips are powerful enough to handle any wireless standard; and 2) that its package provides a more cost-effective approach than conventional DSP alternatives.



A fourth generation of the picoArray architecture will be unveiled later this year



3G femtocells will change the shape of traditional cellular network configurations



picoChip is initially concentrating on wireless DSP applications only

Radio Focus

The word 'package' is crucial here. The whole company has been built around a tightly knit integration of hard and soft offerings. On the hard side there's the picoArray architecture, an array of programmable elements optimised for high-performance signal processing. On the soft side there's a fairly complete development environment, specifically designed to help programme the family of picoArray-based ICs.

The development environment includes toolchains, libraries and software reference designs for some of the hottest wireless communication standards in town. WiMAX, WiBRO, HSDPA, HSUPA, WCDMA, TD-SCDMA, LTE… if it's radio-based, picoChip will tell you its architecture will tackle it.

In principle, there's nothing that would prevent a picoArray-based chip from addressing other types of DSP applications. However, the company is only interested in wireless, at least for the time being.

"The reason for the focus is purely commercial," says Rupert Baines, the firm's vice president of marketing. "When you're starting out you have to have a focus; you have to be able to focus on particular customers; you have to have application engineers with a deep understanding, because you're trying to break into a market and replace some incumbents, so you really got to focus all your intensity on one point to break through. Once you've got that breakthrough and you're established, you start having reference customers, your credibility builds up, money starts to flow and you can afford to broaden out, which is what we'll do over the next year or so."

Baines says the company has actually already got a few customers in other DSP areas, while he reveals ambitions to target, among others, the video and ultrasound markets in the near future.

There's another reason why picoChip is initially devoted to the wireless sector. Wireless is arguably the most dynamic of all electronic technologies. In some cases, standards change even faster than it takes to design, manufacture and distribute a communications product, based on their specifications. And that's where picoChip claims to have another strong advantage: the necessary flexibility to help OEMs and network operators keep up with constant modifications by deploying first and migrating later, purely by software.

Take WiMAX for example (a technology where, incidentally, picoChip's reference designs have come to be considered the industry standard). With WiMAX roll-outs now gathering pace all over the world, the technology is being improved all the time. The latest approved version (known as 'Wave 2') supports increased mobility and higher data rates using MIMO antenna configurations.

Airspan is using picoChip silicon on its indoor and macro-cell WiMAX base stations

For the average WiMAX subscriber, each of these new technical additions is usually great news. They translate as faster Internet connections, using less wires and accessible from increasingly remote areas. For the average WiMAX equipment manufacturer, though, they mean rushing back to the drawing board to launch a new product family before your competitors do.

Last November, picoChip announced the first single-chip (PHY + MAC) WiMAX base station reference design to support Wave 2 and full IO-MIMO in both downlink and uplink channels. Crucially, it will offer OEMs currently using Wave 1 designs, such as Airspan or Fujitsu, a seamless software upgrade to the new version.

"There are more WiMAX base stations using us [picoChip's products] than using any other single architecture, but without us WiMAX would still be happening," Baines acknowledges. "Some people's base stations would cost a bit more money; some would be a bit less flexible. One probable difference would be that there'd be less competition. Because what we do is we enable Tier-2 [companies] and people with interesting ideas but not huge development teams to use us to get into the market. We reduce the barriers to entry."

But it's not just Tier-2 firms that are turning to picoChip's WiMAX expertise. Intel (apart from being one of the firm's key investors together with Pond Venture Partners, Atlas Venture, Highland Capital Partners, Scottish Equity Partners, Rothschild, AT&T and Samsung) is also a picoChip customer. This may sound somewhat confusing given Intel's much-publicised own WiMAX ambitions.

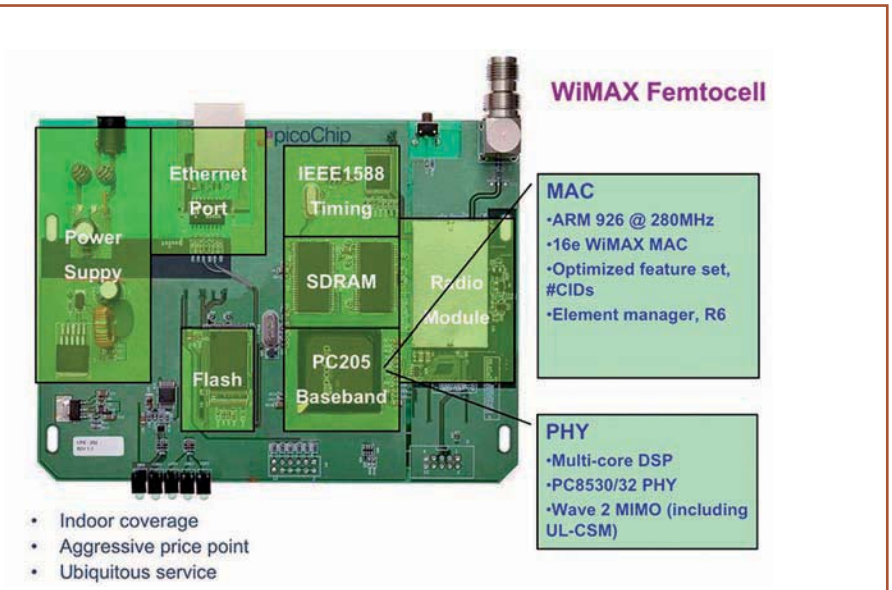
"Intel has got a lot of different WiMAX programmes," Baines clarifies. "Their own product development is focused on chips that go into PCs. But they do also make other products. One of them is a standalone card – effectively a base station card – and they use us for that."

The Femtocells are Coming

Together with WiMAX, the other wireless sector where picoChip is heavily involved in is cellular communications. In particular, the company is seen as one of the driving forces behind what many believe is the next big thing in the mobile phone industry: femtocells.

The femtocell concept is quite simple. As operators migrate an increasing proportion of their customer base from 2G to 3G, the inherently higher frequencies at which 3G networks operate make indoor coverage even patchier than it already is with 2G. This is problematic for various reasons:

Airspan is using picoChip silicon on its indoor and macro-cell WiMAX base stations



The company's femtocell architecture can be applied to both cellular and WiMAX air interfaces

"THE INHERENTLY HIGHER FREQUENCIES AT WHICH 3G NETWORKS OPERATE MAKE INDOOR COVERAGE EVEN PATCHIER THAN IT ALREADY IS WITH 2G"

subscribers use their mobiles mostly when they are indoors; operators are banking on an increasing use of data services on their 3G networks; and competition from voice-over-WiFi providers is intensifying.

Femtocells – which were first demoed by picoChip at the 3GSM 2005 event – not only address these challenges, but they also throw in a few collateral benefits. Essentially a miniature, indoor 3G base-station the size of a paperback book that plugs into the subscriber's broadband line, a typical picoChip femtocell device will support up to four users.

As soon as one of them enters the home, the femtocell will automatically take over from the macrocell network. Users are then guaranteed a wireless data link of up to 7Mbit/s using an HSDPA-enabled laptop or phone.

The novel network architecture opens up a much more efficient way of managing traffic for the operators. Additionally, it helps them offload their two most expensive items in terms of operating expenses: base station backhaul and electricity, both of them now paid by the subscriber. This puts operators in an ideal position to aggressively package and price femtocell-based voice and data services.

"The interesting thing is that this is a market being driven by the operators," says picoChip's Baines. "It's very much people like Vodafone and Telefónica [in Europe], Sprint [US] or SoftBank [Japan] who are pushing it and making it happen, far more than being a technology pushed by suppliers. This is simply because it solves a very big problem for the operators. As soon as they realise this is something that works they're very keen to get it in their networks."

ABI Research is predicting some 70 million femtocells will be installed worldwide by 2012, with 150 million people using them. Considering the direct and indirect financial benefits they will bring, operators will most likely subsidise the roughly €120 cost of each box.

So when can we expect to see femtocells being deployed on a noticeable scale? Baines points out they're already commercially

available in some places. Sprint, for example, has been marketing them in a few of its domestic markets since the second half of 2007. "But it will really be during 2008 that operators will be making their first deployments," he predicts.

He should know. His company's silicon and software are already being integrated into the designs of some of the early OEMs that have started to address the femtocell market, such as ipAccess (which supplies Thomson), Ubiquisys (supplies NEC and Motorola) and Axiom.

The Road Ahead

Ever since it launched the picoArray architecture at the end of 2002, the Bath firm has introduced a new generation of semiconductors approximately every two years, with the second generation launched at the end of 2004 and the third, and so far last, one making its debut in 2006. "Does that mean we're going to be seeing a fourth generation launched at some point in 2008?" I ask. "Yes," Baines replies, and after a short pause he laughs at the forced shortness of his answer.

"And what kind of performance can we expect from it?" I try again. "I'll tell you when we announce it," the predicted response.

But you can certainly expect a jump in processing power, reduced power consumption and more flexibility. With giants TI and Freescale both showing increasing interest in the multi-core DSP space picoChip still dominates, the company can't really afford to rest on its laurels.

"Hmm… yes," Baines replies when I ask him whether that's the main threat picoChip currently faces. "I mean, we compete with some very well-established, very strong players, and we've got to stay ahead of them. Texas Instruments, Freescale, Xilinx are all very good companies with some very smart people. So we have to keep pushing and keep fighting to stay ahead.

"I think we've set a very aggressive pace, addressing a lot of different markets and it's challenging to keep up with that. We're working on many different things, so [what we need] is just the keeping going and not screwing up, in a sense."

They're not the only ones who'll be needing that. The sailing and rowing Olympians in Beijing will also try to "keep going and not screwing up" later this year. While the rest of us will be following their actions attentively, almost as if we were inside their boats with them too. ■

The small fabless semiconductor maker from Bath has developed one of the world's most powerful DSPs

picoChip in brief

Founded: September 2000 by Peter Claydon and Douglas Pulley
Headquarters: Bath, England
CEO: Guillaume d'Eyssautier
Employees: 130
Annual sales: Undisclosed
Net income: Undisclosed
Capital investment funding: $71.5m (four rounds)

Gary Nevison is chairman of the AFDEC RoHS team, and Customer Support Manager, Legislation and Environmental Affairs at Premier Farnell. As such he is our industry expert who will try and answer any questions that you might have relating to the issues of RoHS, WEEE and REACH. Your questions will be published together with Gary's answers in the following issues of Electronics World.

ECO-DESIGN OF ENERGY USING PRODUCTS

The Eco-design of Energy using Products (EuP) Directive will require manufacturers to carefully consider environmental aspects when designing and developing new products. Currently studies are underway to define what measures are required, but the European Commission (EC) has yet to make any firm decisions on the new legislation that will impose eco-design criteria.

Typical examples of products that could be affected include: any mains powered product that has a standby mode – e.g. printers, scanners, etc; any mains powered product that does not have an off-switch that disconnects the mains power; lighting equipment – office, domestic and street (ballasts, bulbs, etc); electric motors rated between 1 and 150kW; some external power supplies and battery chargers; air compressors and vacuum cleaners among others.

The directive mainly affects equipment designers. The EC will impose measures that will place requirements on products that will necessitate on-going improvements in their eco-design. The requirements for each product type will be different, however, some general guidance on eco-friendly new product design is known.

Products with a standby mode are likely to be specified a maximum power consumption level in this mode. Standby mode is typically used where equipment needs to be reactivated remotely (by infra-red for example), or is required to carry out a continuous function such as displaying a clock.

The maximum power consumption in standby mode depends on the equipment's function. The figure being proposed for products that use standby as a re-activation function only, for example televisions, microwave ovens and computer monitors, is 1 watt. It is planned that this figure will be reduced to 0.5 watts after a time. Equipment to which the directive applies will need to be designed to ensure that these values are not exceeded. This requirement has far-reaching implications as every function within a product's circuitry will need to be reviewed in order to determine how the overall standby power consumption can be reduced.

Many products cannot be completely shut down as the off switch disconnects the input power supply from other parts of the equipment but does not disconnect the power supply from the mains. Termed 'off-mode', the EC is proposing to restrict power consumption of equipment in this state to initially 1 watt and then two years later, to 0.5 watts.

The overall power consumption of many products will be controlled either by imposing restrictions with specific consumption limit values or by having to display an energy rating label that is clearly visible to consumers/users.

Energy ratings are already used on light bulbs, washing machines and refrigerators and have proved a great success in making consumers carefully consider energy consumption when they purchase new products.

Most products currently on the market achieve the top rating as a result of improvements already made by manufacturers. This fact is not very useful to consumers and it does not give an incentive to reduce power consumption still further. Therefore, one proposal is to change the criteria used for these ratings so that the power consumption of top rated products is lower than is currently used and so that only the very best products can achieve the top rating. This will give an incentive to manufacturers to make further improvements to their products.

For example, it is proposed that new energy ratings will be developed for fluorescent lamps that will identify the best performing products; currently nearly all have the top 'A' rating. Another proposal is to regulate the energy efficiency of power supplies and battery chargers with obligatory specified minimum efficiency values. This will directly affect power supply design and push forward technical advances in the power electronics sector.

So-called 'active power management' is also being proposed by the EC. This would require equipment to switch itself into standby mode if it is not used for a given period of time. A variety of products are unnecessarily left permanently switched on; good examples are computers, printers and lighting. In some products, switching to standby is impractical but huge power savings can be made by switching off individual functions that are not in use.

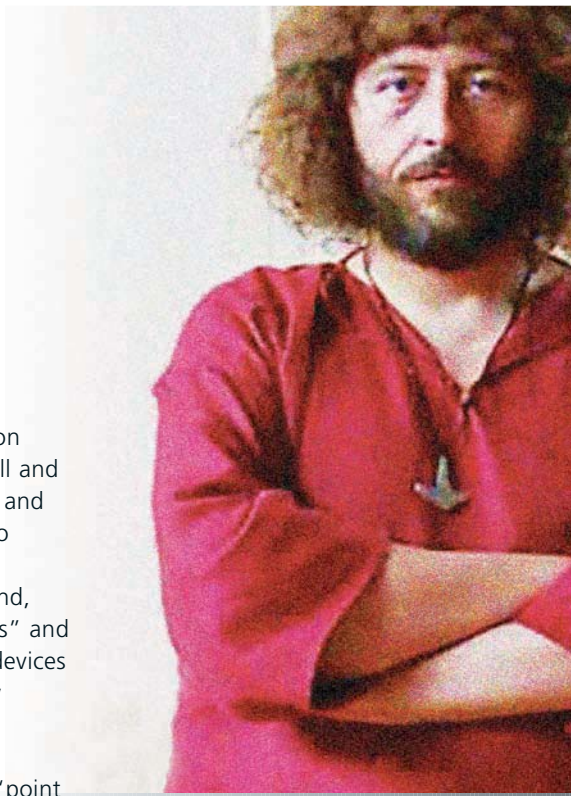
Clearly specified and labelled expected life and other similar information may be required for certain new products. This is being proposed for items such as lamps to encourage designers to make their designs last as long as possible and in so doing have a reduced impact on the environment

Eco-design of EuPs could restrict the use of hazardous materials, for example a recently completed study into office lighting recommended reducing the maximum mercury content of fluorescent lamps below that currently permitted in the RoHS Directive.

Recently, the EC has announced the next batch of product categories for review over the next three years. As we move forward, new EuP implementing measures will target energy consumption but could also affect many other aspects of equipment design. This will make it advisable for designers to carefully consider how their new product developments perform in terms of minimising power consumption, making recycling easier plus reliability and life expectancy. ■

Please email your questions to:
svetlana.josifovska@stjohnpatrick.com
marking them as RoHS or WEEE.

SEEING THROUGH THE WIRELESS TRENDS



by Myk Dormer

Anyone currently working in the low power radio industry cannot be unaware of the arrival on the scene of a new species of "network protocol" radio modules. The most familiar and widely publicised of these are probably the Zigbee devices. Originating with a specification released in 2004 (derived from work begun as early as 1998) by the Zigbee Alliance, a consortium of over a hundred companies of different sizes including some major silicon vendors, these radios have been intensively marketed as, apparently, a universal wireless solution.

THERE IS AN OLD SAYING THAT GOES: "AN ENGINEER CAN DO FOR A PENNY WHAT ANYONE CAN DO FOR A POUND". IT'S STILL TRUE TODAY.

There are a range of vaguely similar imitators (such as Z-wave, Wibree, Insteon and PWN to name only a few), some of which are completely novel while others borrow 802.15.4 radio hardware to run different application firmware stacks. (Strictly speaking, the name "Zigbee" refers to an application and network layer specification, which in turn calls for IEEE 802.15.4 compliant radio hardware. Some applications actually use this type of radio hardware without the full software stack, as simple, conventional short range links.)

With the availability of improved, cheaper RF transceiver devices and increasing levels of advertising, many users are coming to consider such 'famous name' network specification modules as the only solutions for all and any short range wireless functions, and the suppliers of them do nothing to contradict this opinion.

There are many buzzwords abound, including "wireless sensor networks" and "wireless personal area network" devices that are on offer. But what do they actually do, in comparison to a 'traditional' radio system?

The simplest case radio link is a "point to point" application. A device either sends commands to a distant unit (imagine a light switch controlling a light), receives data from it (remote reading of, say, a tide-gauge), or both.

When one 'base unit' communicates with multiple 'out-stations' (consider the monitoring and control of pumps and valves in a water purifying plant) then the radio system has a "star" configuration. Communication can be initiated strictly by the base unit only ('polled' networks) or out-stations can initiate transmissions (either randomly, with retries and possibly 'listen before send' to deal with collisions in 'low duty cycle' systems, or in specifically allocated time slots for 'beacon synchronised' networks).

Star networks (or "point to multi-point" systems) are probably the most common form of low power radio implementations. These are simple to implement and easy to understand techniques. They are typical of customer designed, proprietary ISM band solutions used for many decades. While they hardly fall into the category of wireless networks, they do provide more than adequate facilities for a very large number of applications.

All the above architectures are, however, limited by the range of the basic wireless link: they communicate over only one radio 'hop'. Where the 'master' base unit communicates with one or more distant subordinate bases or 'repeaters', which in turn each communicate with their local group of out-stations, then a "tree" architecture has been formed and we can see the system complexity is significantly increasing.

The simplest version of this network would be a base sending to a repeater, which in turn sends to an out-station. In this case the communication link is over two radio link hops, increasing range, or allowing the placement of the repeater to cover an awkward area where a direct path from the base unit is blocked by terrain.

Even this simple tree network requires extra information to be added to the data burst (so as to prevent multiple responses where the base is in range of both the repeater and the out-station), while particular care is needed in handling 'acknowledge' protocols across the multiple hops. As multiple repeaters and multiple out-stations are added, the complications multiply also and the network protocol must be made more sophisticated.

Methods must be included to prevent 'rings' of repeaters forming (that will pass a single message around for ever), while

traffic synchronisation is needed to stop the collision when two repeaters receive and re-send a burst from the same out-station. Unique 'message identifiers' must be added to the packets and a 're-transmission history' included.

These problems are well understood, as they occur in existing 'packet radio' nets (and in the traffic handling methods used on the internet) but they cannot avoid adding some overhead to the system. Either complex auto-configuring methods are needed (incurring time delays and eating up processing power and bandwidth), or the network must be manually set up, possibly resulting in an inflexible structure, as well as adding to the user's workload.

The final level of complexity is reached in the "mesh" network. In this case the rigidly-defined repeater to out station hierarchy of the tree structure is dispensed with and all out-stations (or "nodes") can communicate with all the other nodes in range. This eliminates the inherent 'brittleness' of a tree network (in that the loss of a single repeater can isolate a whole 'branch' of out-stations) as theoretically, in an ideal ('fully connected') mesh network, there will be multiple communication paths for each hop, so local interference or the loss of a given node ought not disable the network.

Some mesh systems retain a 'master' unit that co-ordinates the network operation and set-up, while other systems go even further and implement the same communication functions in every node (these are referred to as 'peer to peer' networks.)

Simplification can be had by using a mixed approach, with some nodes capable of 'full' communication, while others can receive or originate a data packet, but are incapable of relaying traffic from other nodes. (This is the system adopted by Zigbee, with a base unit 'co-ordinator', communicating to full function 'routers' and reduced function, lower power 'end devices'.)

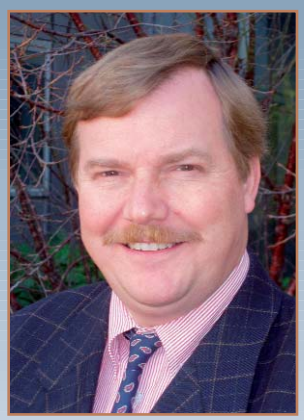
All sounds pretty impressive, doesn't it, but it comes at a cost and that is in complexity. A lot of data traffic, much of it redundant, is passed by the nodes (increasing power and overall bandwidth usage), while the amount of processing required to set up and to operate the network is daunting (a simple, reliable point-to-point link can require only a few hundred bytes of code, on a very low end processor. Full Zigbee stack implementations are quoted as requiring between 30 and 100kbytes of code).

Some applications really do need the facilities that a mesh network offers and assuredly some of those will fall into the area of low power radio. But there are a lot of tasks where only a few bytes worth of information are required to be sent over not-inconsiderable distances, under very tight available power constraints.

These are places where simplicity still wins over complexity and where a little effort taken to implement a good analogue radio link is worth any amount of high level coding.

There is an old saying that goes: "An engineer can do for a penny what anyone can do for a pound". It's still true today.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com



2008: THE YEAR OF POLYMER ELECTRONICS?

DR ALEC READER, DEVELOPMENT DIRECTOR AT INNOS, SAYS THAT THIS YEAR BEGINS THE UPWARD CURVE FOR POLYMER ELECTRONICS; BUT, ARE YOU READY FOR IT?

The physical limitations of silicon have long been a concern for innovators creating groundbreaking intellectual property (IP) for the next generation of electronic devices. Many innovators and early adopters that I speak to have predicted that 2008 will be the year that organic (or polymer) electronics really take off due to their benefits in a number of applications over silicon, but it is crucial that the industry prepares right now.

Advances in organic electronics (based upon semiconducting polymers) have already seen several firms secure pilot line production contracts in 2007, to produce the first devices for eventual sale to market. Polymer electronics' inherent low production cost, portability, aesthetics and, ultimately, the capacity for formable logic and storage circuits whilst staying robust, ensure cheaper devices with a wide range of applications, particularly in the lucrative mobile device market.

In fact, it is the sheer 'flexibility' of polymer electronics that can and will change the market. Semiconducting polymers lend themselves to the fabrication of flexible displays, a market predicted by the electronics industry analysis firm EMSNow, to reach a value of $60m by 2013. Meanwhile, rollable display technology uses many of the same components and characteristics of flexible displays but requires a far greater degree of curvature and resilience than is typically required by a flexible display.

The development of prototype rollable displays designed specifically for use in mobile devices (e.g. telephones) has given way to the signing of commercial deals to produce the first range of product applications in the race to the retailer's shelves. These rollable displays – some able to challenge the circumference of a pencil when completely rolled – have enabled the future production of integrated screens for mobile devices that are physically much larger than the device itself.

Displays of this nature require an appropriate front plane and back plane in order to gain this high flexibility. Developments by innovators so far have been heavily dominated by non-emissive technology, where light is reflected or absorbed as opposed to emitted, with the prime incentive being its low energy consumption. Consumers of mobile devices increasingly expect maximum functionality and longer battery life; non-emissive screens combat this by using low current to generate and, therefore, extend the time before the need to charge the battery.

For example, one of the key front plane technologies is electrophoresis, which allows the separation of black and white particles within individual pixel cells in a display according to their size and charge, using an electric field (specific arrangements of pixel cells will give way to full colour displays). Coupling this with a mature technology such as organic TFT (thin film transistor) for the flexible backplane could see it become one of the most effective methods of creating a rollable display.

There is, of course, huge potential for the growth of emissive front plane technology such as OLED in the future, which unlike non-emissive requires no backlight to view in low light conditions, by using light emitting photons. Typically though, this technology is far more suited to devices or consumer products using a mains power source, such as a television, as it is relatively power-hungry. It is not particularly suitable for mobile devices when compared with non-emissive displays, as the lifetime of some materials and batteries may not sustain intensive everyday use.

The outlook for polymer electronics is indeed an exciting one; Columbia News Service has predicted that the market as a whole will reach $12.5bn in 2012, to double by 2025 according to IDTechEx.

Year 2008 may very well be the one that the technology starts seeing substantial revenues; however, I strongly believe that innovators need to start to exploit applications as soon as possible to ensure their position as a forerunner in the race to market. ■

Rollable display technology uses many of the same components and characteristics of flexible displays but requires a far greater degree of curvature and resilience

BY MATTHEW HAUSE, PRINCIPAL CONSULTANT, ARTISAN SOFTWARE TOOLS

SHOWS HOW OMG SYSML ARTIFACTS CAN BE USED ON MISSION-CRITICAL APPLICATIONS TO SPECIFY THE REQUIREMENTS FOR SOLUTION SPACES SUCH AS SOFTWARE AND HARDWARE TO PROVIDE TRACEABILITY AND HANDOVER

DESIGNING MISSION-CRITICAL SYSTEMS USING OMG SYSML

Back in September 2007, the Object Management Group (OMG) announced that OMG SysML v1.0 had been issued as an Available Specification.

The OMG SysML specification was developed in response to the joint Request for Proposal issued by the OMG and INCOSE (the International Council on Systems Engineering) for a customised version of UML 2 designed to address the specific needs of system engineers. Its customisation for systems engineering supports the modelling of a broad range of systems which may include hardware, software, data, personnel, procedures and facilities.

In developing OMG SysML, the goal was to provide a "standard modelling language for systems engineering to analyse, specify, design and verify complex systems, intended to enhance systems quality, improve the ability to exchange systems engineering information amongst tools and help bridge the semantic gap between systems, software and other engineering disciplines".

Mission-critical applications, in particular, need to take a holistic approach to development. Using Artisan Studio's comprehensive OMG SysML Profile, which makes use of its powerful domain-specific profiling capability, this article shows how OMG SysML artifacts can be used on mission critical applications to specify the requirements for solution spaces such as software and hardware to provide traceability and handover.

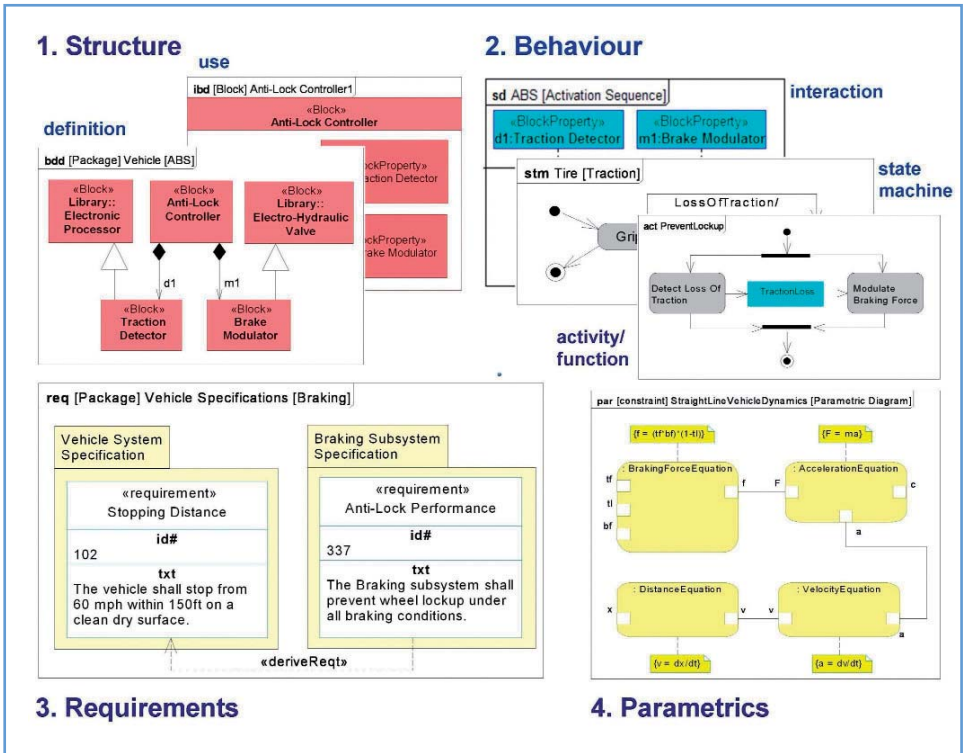


Figure 1: *The four pillars of OMG SysML*

OMG SysML Structure

OMG SysML includes diagrams that can be used to specify system requirements, behaviour, structure and parametric relationships. These are known as the four pillars of OMG SysML. An example of these different diagrams for an automotive ABS system is shown in **Figure 1**.

The system structure is represented by block definition diagrams and internal block diagrams. A block definition diagram describes the system hierarchy and system/component classifications. The internal block diagram describes the internal structure of a system in terms of its parts, ports and connectors. The package diagram is used to organise the model.

The behaviour diagrams include the use case diagram, activity diagram, sequence

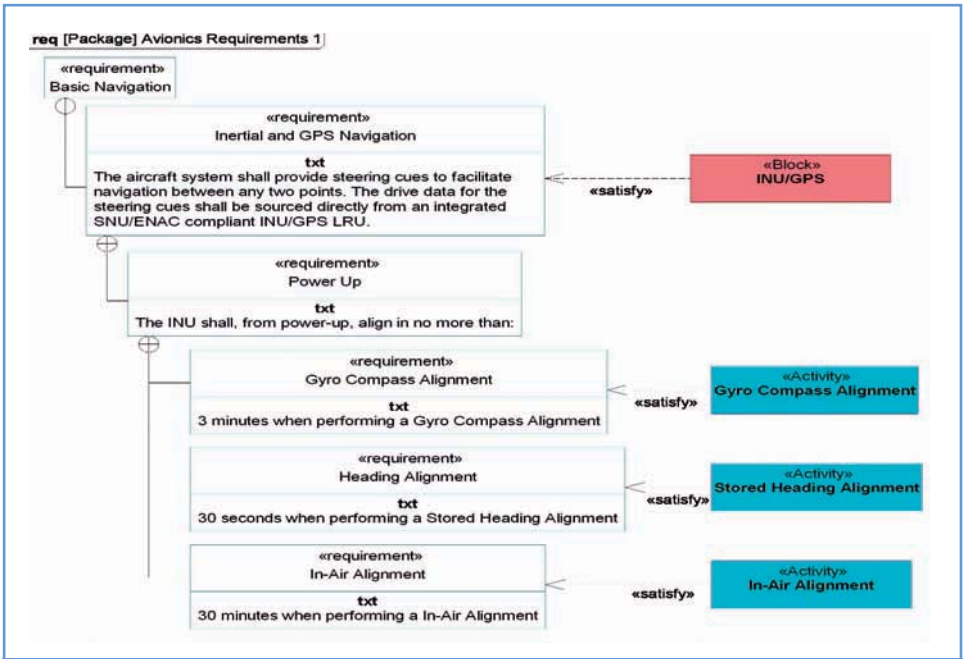


Figure 2: *Requirements diagram*

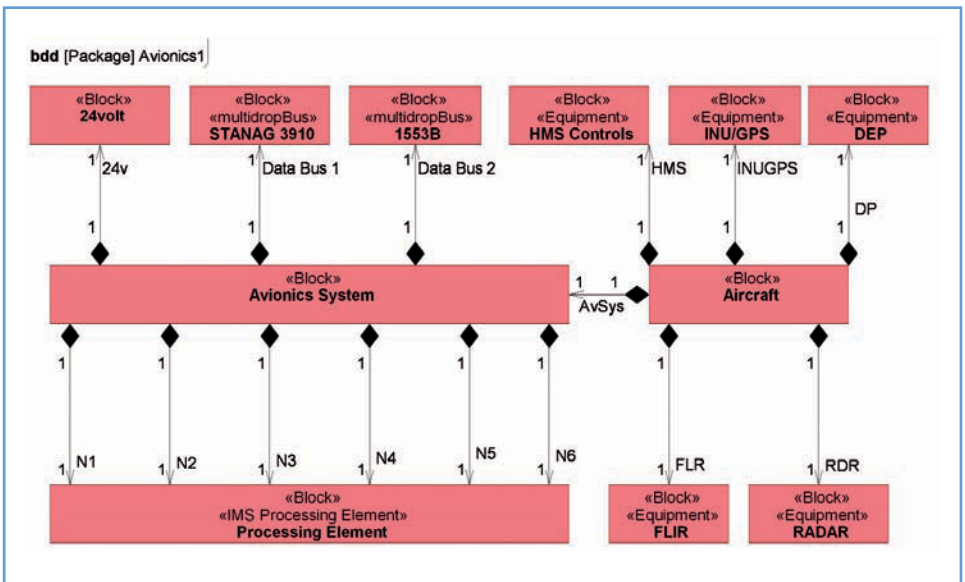


Figure 3: *Block definition diagram*

diagram and state machine diagram. A use-case diagram provides a high-level description of the system functionality. The activity diagram represents the flow of data and control between activities. A sequence diagram represents the interaction between collaborating parts of a system. The state machine diagram describes the state transitions and actions that a system or its parts performs in response to events.

The requirement diagram captures requirements hierarchies and the derivation, satisfaction, verification and refinement relationships. The parametric diagram represents constraints on system parameter values such as performance, reliability and mass properties to support engineering analysis.

Figure 1 makes use of cross-cutting constructs. These apply to both structure and behaviour. Cross-cutting constructs support concerns that cut across the different views and may be addressed by all or disparate parts of the model. These constructs take the form of allocations, requirements and parametrics.

Requirements in OMG SysML

Requirements traceability is an essential part of mission critical applications. For DO-178B, for example, traceability must be provided between system requirements and high-level software requirements, high and low level requirements, low-level requirements and tests, tests and code for structural coverage, and from top down and bottom up.

The requirement diagram is used to integrate the system models with text-based requirements that are typically captured in requirements management tools, to facilitate the required traceability.

The UML containment relationship is used to decompose a requirement into its constituent requirements. The «deriveReqt» and «satisfy» dependencies describe the derivation of requirements from other requirements and the satisfaction of requirements by design, respectively. The «verify» dependency shows the link from a test case to the requirement or requirements it verifies.

In addition, the UML «refine» dependency is used to indicate that an OMG SysML model element is a refinement of a textual requirement, and «a copy» relationship is used to show reuse of a requirement within a different requirement hierarchy.

The «rationale» concept can be used to annotate any model element to identify supporting rationale including analysis and trade studies for a derived requirement, a design or some other decision. **Figure 2** shows the requirements flow down for an INU/GPS component.

More specialised requirement types can be designated using specialisation of the «requirement» stereotype. Each requirement has a unique identifier shown next to the id# tag and the text of the requirement is shown in the compartment labeled "txt" in the lower part of the class box.

The format shown is only one of a number of possibilities and ergonomic profiling can be used to modify the display format to correspond to the needs of the audience. Artisan Studio 6.2 has been used in these examples but the exact capabilities for this type of feature will depend on the actual tool being used. Additionally, requirements and their relationships can be shown on other diagrams.

Tools that provide the functionality to import, export, and synchronise requirements

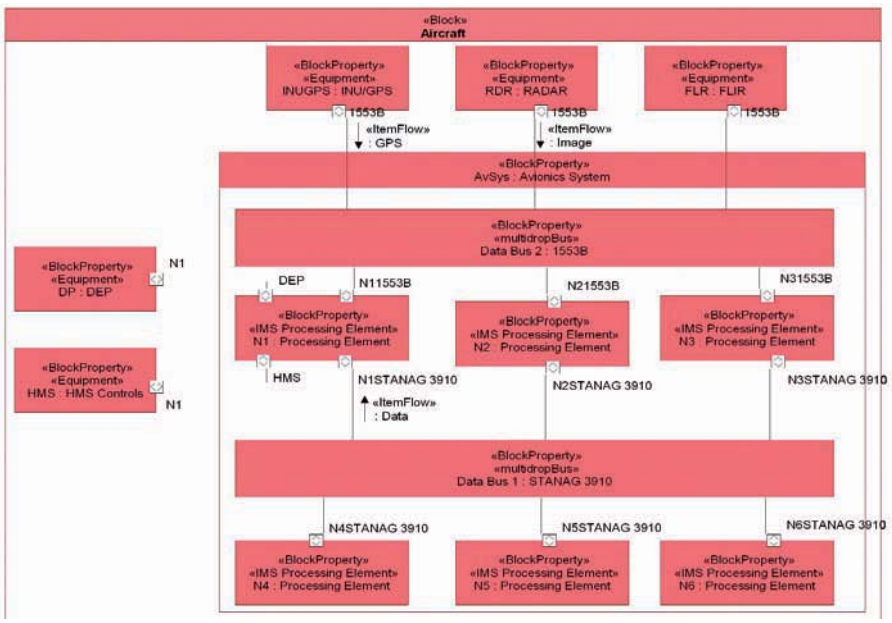


Figure 4: *IBD for an avionics system*

and their relationships between the OMG SysML model and an external requirements management tool will allow developers to perform requirements traceability in the tool while taking advantage of the features provided by specialist requirements management tools. Traceability reports can normally be generated directly from the integrated model in a format compatible with DO-178B.

Structure

A clear description of the system and its environment is essential for mission-critical applications. OMG SysML provides block diagrams to support this. The OMG SysML «block» is a general purpose hierarchical structuring mechanism that abstracts away much of the software-specific detail implicit in UML structured classes.

Blocks can represent any level of the system hierarchy including the top-level system, a subsystem, or logical or physical component of a system or environment. An OMG SysML block describes a system as a collection of parts and connections between them that enable communication and other forms of interaction. Ports provide access to the internal structure of a block for use when the object is used within the context of a larger structure. OMG SysML provides standard ports which support client-server communication (e.g. required and provided interfaces) and FlowPorts that define flows in or out of a block.

* **Structured diagram types**: Two diagrams are used to describe block relationships. The Block Definition Diagram (BDD), similar to a traditional class diagram, is used to describe relationships that exist between blocks. The Internal Block Diagram (IBD) is used to describe block internals.

An example of a block definition diagram is shown in **Figure 3**. The example of an avionics system is represented as a block composed of other blocks, including several processing elements, 24V power and two buses. The role names on the association ends correspond to the parts on the IBD.

The internal structure of an avionics system is shown in **Figure 4**. Each of the components has a number of flow ports that describe what can flow in and out. These are then connected to other compatible ports to enable the required flows in this context. The arrows on the connectors represent item flows that correspond to physical or logical items that actually flow through the system and whose properties can be constrained in parametric models.

*** Allocations**: The OMG SysML allocation relationship is used to allocate one model element to another. Allocation is the term used by systems engineers to denote the organised cross-association (mapping) of elements within the various structures or hierarchies of a user model.

Often this is the allocation of function to form, such as the deployment of software on a hardware platform, or a use case to an organisation or system entity or a logical to a physical entity.

Allocations can be used early in the design as a precursor to more detailed rigorous specifications and implementations. The allocation relationship can provide an effective means for navigating the model by establishing cross relationships and ensuring the various parts of the model are properly integrated. The integration of the software and hardware models means that SIL levels for the various parts can be assigned and verified to ensure a consistent implementation. Hardware/software interfaces can also be verified, as well as architectural constraints, thus ensuring traceability and change analysis.

Additionally, studies are being done to determine if Goal Structuring Notation (GSN) can be integrated into a model in a similar way as requirements described above. GSN provides a graphical means of expressing a safety case. Creating links from the model elements to the GSN safety case elements provides direct traceability and the possibility of modular safety cases, using OMG SysML packages. This creates savings in the time required to build the safety case, and therefore money.

Robust Language for Modelling

The extensions made to UML 2 in the OMG SysML Profile provides systems engineers with a robust language for modelling systems that include models of requirements, behaviour, structure and parametrics.

At the same time, the profile's extensive reuse of UML facilitates a much smoother flow down from systems engineering to software engineering than otherwise possible. ■

References:

A variety of technical papers and a summary of OMG SysML are available from **http://www.artisansw.com.** Further, specific information on the OMG SysML v1.0 specification available at **http://www.omgsysml.org/**.

MODEL-BASED DESIGN FOR MECHATRONIC SYSTEMS

Most engineers are surprised to learn that the term mechatronics is nearly 40 years old. It was first used in1969 by Tetsuro Mori, an engineer at the Yaskawa Company, to describe a system composed of mechanical and electrical elements that is controlled by an embedded system (**Figure 1**).

In today's world it is rare to find electromechanical devices without some kind of embedded system. The intelligence from an embedded system delivers enhanced performance, reduced energy consumption, better reliability and safer operation, which are key differentiators and value drivers for a piece of equipment.

The benefits of an embedded system come at a price. As mechatronic systems take advantage of more powerful microprocessors, which provide the intelligence for embedded systems, the interaction between hardware and software becomes more complex. Managing this complexity can prove challenging to hardware and software engineering teams, who state requirements, describe problems and test and implement solutions in different ways.

In addition, engineers must design closed-loop control strategies to compensate for electromechanical interactions and external disturbances, as well as incorporate open-loop supervisory control for operational requirements, such as start-up and shutdown, personnel and equipment safety, and fault detection and remediation.

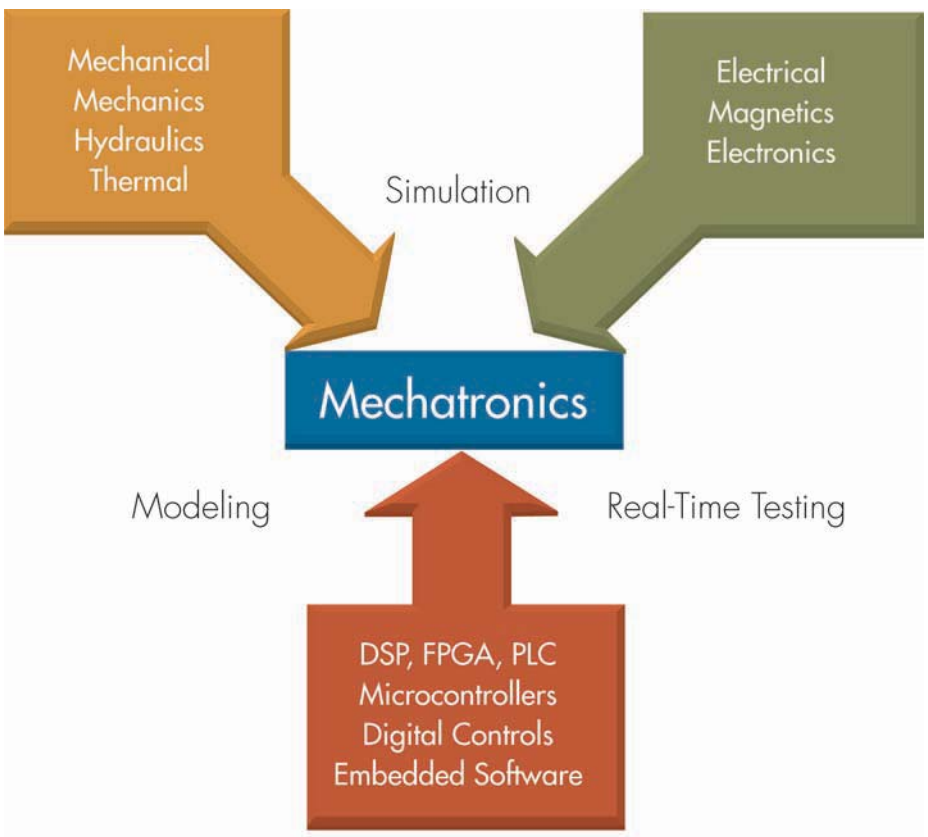


Figure 1: *Mechatronics is a synergy of mechanical and electrical systems controlled by an embedded system.*

TONY LENNON, INDUSTRY MARKETING MANAGER AT THE MATHWORKS EXPLAINS THE BENEFITS AND WHY MODEL-BASED DESIGN IS THE TOOL OF CHOICE FOR SYSTEM-LEVEL DESIGN OF MECHATRONIC SYSTEMS

In most traditional design approaches, engineers test software on hardware prototypes, addressing software validation very late in the development process. Errors found in hardware or software at this stage create costly delays and may be time consuming to trace back to their root cause. Errors related to incomplete, incorrect, or conflicting requirements may even necessitate a fundamental redesign.

Improved Development Using Model-Based Design

Model-Based Design (**Figure 2**) simplifies the development of mechatronic systems by providing a common environment for design and communication across different engineering disciplines. Model-Based Design extends the computer-aided engineering (CAE) world with an additional perspective on system-level design.

Just as computer-aided design (CAD) provides a geometric or static description of

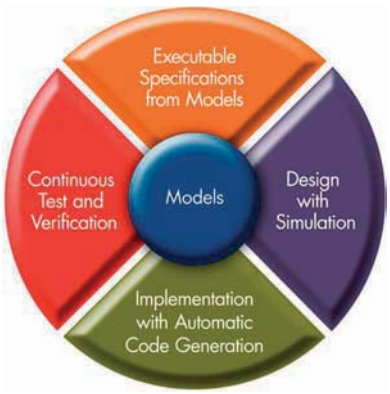


Figure 2: *Model-Based Design places the system-level model at the centre of the development process for mechatronic systems*

equipment, Model-Based Design incorporates the dynamics and performance requirements needed to properly describe the system. Because this approach is software driven, engineers can fluidly investigate competing designs and explore new concepts without the overhead of extensive hardware investment.

Engineers can continuously test the design as it evolves, checking it against requirements and finding mistakes earlier in the development process when they are easier and less costly to correct. In addition, Model-Based Design automates code generation for the embedded system by eliminating the need to hand code the open and closed-loop control algorithms.

Model-Based Design uses a system-level model that defines an executable specification by uniquely describing the natural and controlled behaviour of the equipment in a mathematical form. Engineers can *execute* the model by simulating the actual dynamics and performance of the system. The model *specifies* an unambiguous mathematical definition of the expected performance of the mechatronic system. As an executable specification, the system-level model provides a clear advantage over written documents, which, because they are subject to interpretation, can lead to requirements that are missing, redundant, or in conflict with other requirements.

Written requirements will always exist, but engineers can link their electronic formats to the system-level model and help establish compliance to standards such as ISO 9001 or IEC 61508. Tracing requirements from the written specifications to the system-level model clarifies how the engineer interpreted the requirement. Electronic links between requirements and the model let engineers connect test criteria to test cases used throughout the development process.

Developing the System-Level Model

A block diagram is a natural approach for expressing a system-level model (**Figure 3**). The model has inputs - signals provided by external agencies, and outputs - measures of what the system is actually doing. The inputs and outputs represent real values, such as voltage, temperature and pH.

Inside the model, the blocks represent mathematical operations between the input and output signals of the model. Some blocks, called the plant or process, represent the natural behaviour of the mechatronic system. For example, the model may contain a block representing a motor. The mathematical model of the motor may be fairly simple, just taking a voltage input and converting it to an output torque.

The motor model complexity can increase by adding more inputs to the model, such as noise in the voltage, or by adding more parameters, such as temperature and magnetic saturation affects. A single block or a group of blocks, filtering and processing signals based on output errors or events occurring in the model, can represent the compensation or control in the system.

The basis of a system-level model is a lumped parameter mathematical model that describes the physics of the system. Ordinary differential equations (ODEs) and differential algebraic equations (DAEs) express the input-to-output relationship of the mechatronic systems.

In the motor example, an ODE describes the relationship of the voltage input to the shaft output torque. Differential equations are a computationally efficient way to describe lumped dynamics, as opposed to using a partial differential equation-based modelling tool, such as finite element analysis (FEA). FEA software could be used to solve for the torque-induced stress distribution at a key slot in the motor shaft.

Using ODEs to describe the system-level behaviour of a mechatronic system involving multiple engineering disciplines does not come without challenges. Expressing system behaviour mathematically requires knowledge of the physics underlying the system. The reality of mechatronics is that all systems are nonlinear and you must account for hysteresis, friction and thermal effects exhibited by the real mechatronic equipment.

Improving the System-Level Model

When the mathematics of the system becomes too difficult or time-consuming to develop, engineers can turn to other ways of system-level modelling.

A common method to supplement a first-principles approach is data-driven empirical modelling, such as system identification or neural networks. These black-box approaches use measured input-output data to construct linear or nonlinear ODE forms of the system behaviour for incorporation into the system-level model. These approaches do not give a complete insight into the physics of the system, but can yield accurate descriptions of the system dynamics within the region of the test data.

Measured data can also improve the accuracy of a first principles mathematical model by using parameter estimation techniques. This gray-box modelling involves optimisation techniques to adjust model parameters, such as a friction coefficient, to match the model output with the test data.

Model-Based Design lets engineers start with a less detailed system-level model and incrementally increase its fidelity as development progresses. A proof-of-concept model represented as a lower-order ODE may be all that is required initially to help engineers quickly eliminate concepts with little promise. For stronger ideas, they can add fidelity by incorporating subcomponents provided by suppliers to more quickly evaluate the best combinations of components. Models evolve into a combination of multiple domains, providing only the needed detail to ensure performance under the operational conditions expressed in the requirements documents.

CAD meets Model-Based Design as engineers increase model fidelity by using mass and inertia properties of a mechanical system translated from a three-dimensional CAD assembly file. Engineers can replace

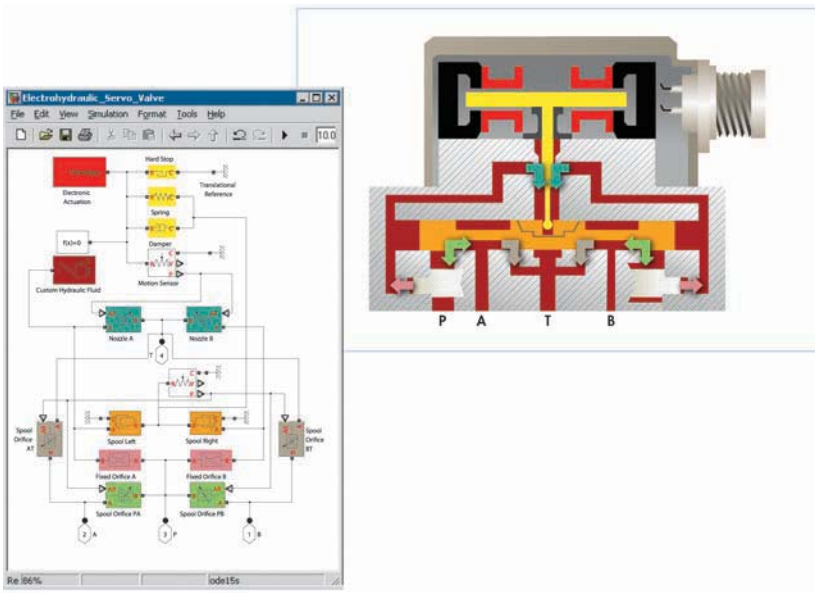


Figure 3: *A block diagram provides an intuitive view of a system-level model*

approximate mathematical representations with blocks that represent the mechanical bodies and linkages translated automatically from the CAD file. In addition to speeding the development of complex mechanical system-level models, this approach ensures that the system designers and the mechanical engineers use an agreed-upon, common-model, behaviour on which to represent the actual mechatronic system when built.

Developing the Control Strategy

After describing the system's natural behaviour, the next step is to develop and evaluate a control strategy, which can incorporate many levels of open and closed-loop control within the mechatronic system. The open-loop control, which includes all interface, mode, logic and supervisory control, is how engineers implement the safe operation, fault detection and recovery features.

The closed-loop control can range in sophistication from algorithms for a basic proportional-integral-derivative (PID) compensator to an implementation of a multivariable linear-quadratic-Gaussian (LQG) controller.

The open-loop control performs supervisory control and mode control within the equipment and addresses the interaction of the operator with equipment. Equipment designers using more powerful microprocessors can develop complex user interfaces that provide greater control over the operation of the equipment. As a result, developers can create increasingly sophisticated self-diagnostics, fault-detection and safety-shutdown systems within the equipment. Model-Based Design helps engineers develop and test the increasingly complex open-loop control system against the system-level model. Simulation lets testing begin early in the design process to improve the ergonomics of the equipment and find any scenarios that may cause equipment damage or create unsafe conditions.

A mechatronic system can employ a number of closed-loop control systems operating over a range of conditions. Using a system-level model helps in designing and tuning the controllers in control loops that exhibit coupled behaviour. Tuning the controllers in hardware is difficult and time-consuming, and often results in detuning the system below expected performance to prevent instability.

A system-level model lets engineers analyse the interaction of the control loops, develop decoupling strategies and tune compensator gains with a variety of approaches that rely on direct and optimisation-based techniques.

At this stage, the system-level model exposes dynamic instabilities that are physically or economically infeasible to eliminate by using closed-loop compensation methods. The model makes it easy to identify and adjust physical parameters, such as mass, length and capacitance that cause instability. As a result, problems can be found during the less expensive software, such as in simulation stage, rather than during testing of physical prototypes.

Model-Based Design helps engineers perform cost trade-off studies within the control system. The system-level model is an analysis tool for deciding whether a less expensive sensor with greater tolerance provide the desired levels of accuracy and performance. Engineers can evaluate practically any component used in mechatronic systems for cost versus impact of the system performance.

Continuous Testing and System Verification

Continuous testing and verification throughout the development process involves defining and using standard tests in conjunction with the control system design process. Using standard tests or a test harness ensures that engineers test the evolving system-level model in a consistent manner and with the same set of measures.

Test criteria such as pass/fail and tolerance bands are associated with a test through electronic links to requirement documents. Continuous testing with a standard test harness immediately exposes the impact of any design change on system outputs and helps quickly trace the change to the cause.

In addition, engineers can use the test harness to determine whether they have full-model coverage, a measure of how completely the test harness exercises all of the operational scenarios of the equipment.

Verifying that the standard tests will completely exercise the system for all operating conditions during the modelling phase assures developers that the tests are complete and correct before testing begins on the physical prototype. Model-Based Design helps engineers create complete tests that they can use during all stages of the development process and into production testing.

System-Level Model Elaboration for Deployment

Once the control design strategy has been developed and tested in simulation, engineers further elaborate the model for deployment. Deployment refers to converting the control algorithms into C code, hardware description language (HDL), or an IEC 61131-3 language, such as structured text (ST), for executing on a real-time system.

This process involves converting the control algorithms from a continuous (analogue) to a discrete (digital), often fixed-point, format. During the continuous testing, engineers test the digital form of the control algorithms against the continuous form of the plant to ascertain whether the digital conversion adversely affects the desired performance to the system.

Model elaboration lets engineers examine other aspects of converting to digital signals.

System designers model the input/output (I/O) device drivers and any A/D and D/A converters to ensure that no corruption or aliasing of signals will occur in the actual implementation of the system.

Mechatronic systems often use a combination of different processors that operate at different speeds and sampling rates. The system-level model lets engineers simulate and test various combinations to assess cost and implementation options, such as using a field-programmable gate array (FPGA) instead of a digital signal processor (DSP), or fixed-point calculations instead of floating-point calculations.

Testing Mechatronic Systems Using a Real-Time System

Testing the system-level model on a real-time system is the next step in Model-Based Design. In this stage, engineers automatically convert the system-level model into C code, HDL or PLC code. Engineers may generate code for the control algorithms, the plant model, or both, depending on how they choose to test the system. In Model-Based Design, automatically converting the system-level model to code eliminates the need for system engineers to be code-writing experts, prevents the introduction of errors, and saves time.

The process of automatic code generation is analogous to generating a tool path for machining a part from a three-dimensional CAD file. If an error is found in the part after machining, the engineer checks and modifies the CAD file and regenerates the code for the tool path. In Model-Based Design, engineers change the code via the system-level model, a natural environment for troubleshooting the system. They update and test the model and regenerate the code.

Using dedicated real-time test systems, real-time testing involves two kinds of testing: rapid prototyping (RP) and hardware-in-the-loop (HIL). During this testing, engineers can collect data in real time and modify parameters in the code as the test runs.

Table 1 shows some of the options for real-time testing and illustrates the testing flexibility that lets engineers catch critical and time-consuming mistakes before actual hardware is available. As stated earlier, tracing mistakes to their source is much easier since the system-level model is the specification, tied directly to the requirements documents.

Testing Type	Control Algorithms	Plant Model
Hardware-in-the-loop	Expressed in code on a target microprocessor	Expressed in code on a real-time system
Rapid prototyping	Expressed in code on a real-time system	Real hardware

Table 1: *Rapid prototyping and hardware-in-the loop testing scenarios*

During rapid prototyping, the real-time system connects to real hardware. Because the control system in the model contains all of the needed I/O in most cases, the system-level model automatically creates the code for these features, eliminating the need for engineers to hand code them.

HIL testing deploys the plant model of the equipment to a real-time system. In this situation, engineers deploy the control algorithms to a real-time test system or to the intended target processor and connect to the plant model, which also runs in real-time. HIL testing can also be accomplished by using the simulated plant model running on the desktop or workstation computer.

Production Quality Code Generation

Model-Based Design lets engineers use the system-level model to deploy the control algorithms in C code, HDL or PLC code, targeting the production processor or other real-time system. The code generation process optimises the production quality code for a specific processor.

It differs from the code used in real-time testing because the process strips out all parameters needed during testing and optimises the code for a minimum footprint to reduce memory overhead and maximize computational speed. Engineers have control over the code generation process to include data objects, user-defined storage classes, types, and aliases.

In addition, customising the code format to conform automatically to a company's software style guide helps make the optimisation complete and simplifies the use of the code by software engineers, usually responsible for integrating the code into a larger code set.

'Staple Diet' Tool

Model-Based Design is CAE for system-level design of mechatronic systems. Engineers develop and test a behavioural model of their equipment in software with these benefits:

1. The capability to inexpensively design and test multiple approaches without a costly commitment to prototype hardware early in the development process.
2. A collaborative design environment using a common executable specification that connects to requirement documents and lets all multiple engineering disciplines communicate in a common language.
3. The ability to reduce development costs by easily finding and correcting errors during an early simulation stage.
4. The capability to develop complex embedded systems that provide greater customer value, product quality and sophistication in mechatronic systems.■

UN-DOCUMENTED CODE AND THE ELECTRONICS INDUSTRY

MARK TOLLIVER, CEO OF PALAMIDA IN THE US, DISCUSSES THE VIRTUES OF OPEN-SOURCE SOFTWARE BUT ALSO THE PITFALLS FOR MODERN FIRMS TRYING TO COMPLY

Customer demand is synonymous with technological innovation. Pushing the boundaries of product design, manufacturers continually look to do more, whether features, functionality and processing power, but in less space and for less money. Fundamental to achieving these goals is the use of open source code. Readily available, cost-effective and outside of the lines of the normal software procurement process, open source code is at the nexus of all of today's software development.

The widespread acceptance of open source continues to grow as an important alternative to commercial software. It is safe to say that open source is everywhere and is being used within your organisation whether or not you are aware of it. In fact, it makes up at least 30% of the total lines of code in all software applications, both internally developed and commercial software applications installed on your network. Even if you implemented policies prohibiting its use in the development process, it is already there by virtue of the operating system you may be using or your word processing application. Often, open source makes up 50% or more of an application's total code base.

The prevalence of open source has thought-provoking implications for the electronics industry in that it introduces new risk from an intellectual property (IP) and security standpoint. Commonly found throughout the electronics industry is embedded open source, which poses greater challenges by virtue of the license that governs its use – the General Public License version 2.0 (GPLv2). The GPLv2 is the legacy open source license that permeates a significant percentage of the embedded market.

The most recognisable embedded open source project is embedded Linux, which denotes the use of Linux OS in an embedded system typically found in mobile phones, personal digital assistants and media players. It can also be found in machine control and industrial automation among other things.

Embedded Linux is different from its cousin, Linux OS, in that it was made specifically for devices with smaller sized RAM and flash-memory based storage and is not appropriate for use with desktop computers. Embedded Linux exists on a large percentage of consumer devices and is covered by the GPLv2.

The DRM Drama

As of June 2007, the GPLv2 was upgraded to version 3, which is not compatible with its predecessor. This effectively puts a halt to the future innovation of retail items using code covered under the GPLv2, primarily due to the Digital Restrictions Mismanagement provisions.

Digital Rights Management (DRM) is most often associated with DVDs and other media. With DRM came laws that prohibited individuals from writing tools to bypass its restrictions such as the Digital Millennium Copyright Act and the European Union Copyright Directive. The GPLv3 provisions ignited a debate about whether or not these laws suppressed the intent and spirit of the GPL. GPLv3 was written with the intent to prevent what Eben Moglen, lawyer for the Free Software Foundation (instigators of the GPLv3) termed "Tivoization".

TiVo, manufacturers of the eponymous TiVo digital recording system, built the software for their device using both the Linux kernel and GNU software, both licensed under the GPLv2, which requires distributors to make their source code available to anyone receiving the software. This would mean everyone purchasing the TiVo device. The intent of this GPLv2 provision was to allow anyone using software under the license to modify it to suit their needs.

The Free Software Foundation believes that TiVo superseded the intent of the license by ensuring that their device would run programs with digital signatures that matched (and were authorised by) their organisation. TiVo did release its source code for modification,

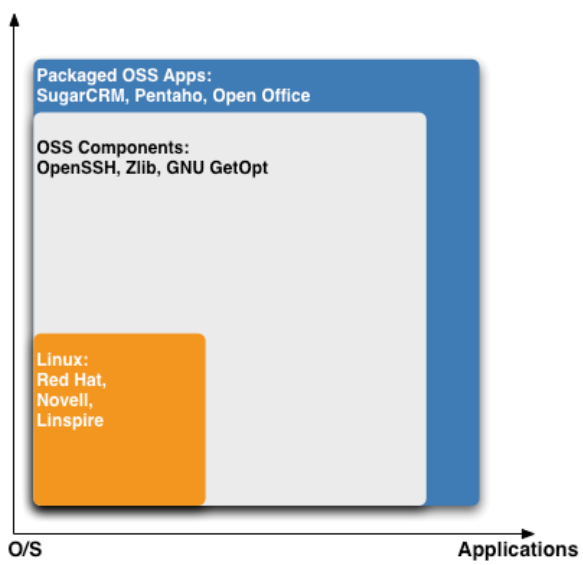


Figure 1: *OSS landscape*

Project	Vulnerability	Vulnerability Type
Apache Geronimo 2.0	CVE-2007-4548	Allows attackers to bypass authentication requirements and deploy arbitrary code
JBoss Application Server 3.2.4 to 4.0.5	CVE-2006-5750	Allows remote users to read or modify arbitrary files.
LibTiff before 3.8.2	CVE-2006-3464	Allows attackers ability to deploy arbitrary code
Net-SNMP 5.2.x before 5.2.2, 5.1.x before 5.1.3, 5.0.x before 5.0.10.2,	CVE-2005-4837	Allows remote attackers ability to cause denial of service
Zlib before 1.2.3	CVE-2005-2096	Allows remote attackers ability to cause denial of service

Source: Palamida, Inc.

Figure 2: *Top five most overlooked open source vulnerabilities, 2007*

as outlined in the provisions of the GPLv2, modified software cannot run on their devices. Therein lies "Tivoization".

Interestingly, Linus Torvalds, the father of the Linux kernel, has said he believes TiVo has a right to use digital signatures to limit what runs on its hardware as private digital signatures are important for software security. He has stated that he believes software licenses, such as the GPLv2, should only relate to software, not on the hardware running it and if the software source code were released for anyone to modify for use on other hardware, he doesn't see it as GPL violation.

According to Moglen, the FSF developed the GPLv3 with the intent of "prohibiting technical means of evasion of its rules, with the same clarity that it prohibits legal evasion of its rules".

In his presentation at the 3rd International GPLv3 Conference, Moglen explained his stance by saying: "Let's say I make a digital video recorder, let's say I call it TiVo, and I sell it on; The GPL software in there, and so is the source code. The only thing is, if you modify this software inside my box I will cut your service off. That would be a straightforward violation of the GPL. You would be adding a condition to the license and you couldn't do it."

"We are saying that the license should prohibit technical means of evasion of its rules, with the same clarity that it prohibits legal evasion of its rules, that's all."

Although it is best to seek qualified legal advice for the proper interpretation of the GPL and how it affects individual business practices, it is safe to assume that the GPLv3 is asking that manufacturers using embedded open source covered under the GPL to release all of their source code and refrain from preventing modification to the hardware that surrounds it. The Google Android project is a perfect example of this model in action.

Unless companies are willing and able to allow open modification of their products, they may want to search for viable alternatives to any embedded open source covered by the GPL.

Where To Go From Here?

The issues pertaining to the GPL matter greatly to organisations shipping products containing the GPL in either of its iterations.

Manufacturers using electronic components are not always aware that they contain embedded open source and thus, would not be aware of the license provisions governing the undocumented code. Without a clear understanding of what open source is being used and where it resides, manufacturers leave themselves open to risk.

The growing complexity of multi-source development environments necessitates transparency in the application development lifecycle. Successful open source management calls for a robust and enforceable software risk management process based on the following best practices:

Policy – setting development guidelines for the procurement and use of open source and third party components.

Education – Ensuring that the development teams understand the importance of and adhere to the open source use policy.

Audit and analysis – Keeping an ongoing inventory of open source and third party components, reporting on their use, detecting known vulnerabilities and alerting the organisation to legal liabilities.

Among the necessary steps for implementing a software risk management policy, code audits are fundamental to its overall success. Thorough code audits enable security and engineering teams to ensure that open source and other third-party components meet the same rigorous security and quality assurance thresholds required of internally developed, proprietary code. They also alert the organisation to the existence of undocumented code, what license governs its use and whether or not it contains a known vulnerability.

All organisations should ensure that they can confidently answer the following questions:

– What open source and third party software components are we using?

– Where are we using them?

– Are they secure? Do they have known vulnerabilities?

– What rights do we have to use them and are we in compliance with any obligations regarding their use?

Enacting best practices for open source use empowers organisations to use it to their best advantage as a solution for driving continual innovation and growth and prevent open source licensing and security issues. ■

OPENING UP OPPORTUNITIES IN SYSTEM DESIGNS

WOLF FRONAUER, MARKETING MANAGER AT JAPANESE FIRM FUJITSU, LOOKS AT WHY FERROELECTRIC RANDOM ACCESS MEMORY (FRAM) IS BECOMING INCREASINGLY POPULAR WITH SYSTEM DESIGNERS

One universal type of memory that combines the features of RAM with non-volatile data retention is ferroelectric random access memory, or FRAM. As a memory type with these features it is fast becoming popular with developers. It saves data at the same time as it is read out and, in addition, the data is saved in a non-volatile manner and retained, even when the computer is switched off.

This combination of the features of RAM and ROM/EEPROM functions, together with higher write/read speed and lower power consumption, opens up new possibilities for system design.

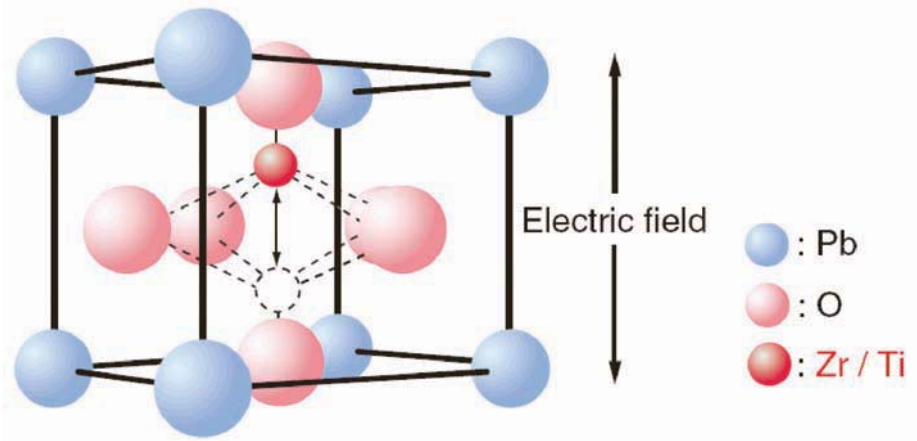


Figure 1: *Crystal structure of ferroelectric material PZT (PB(ZrTi)O3)*

How it Works

The first FRAM was launched on the market in 1988, after successful experiments with ferroelectric materials were performed at Stanford University and published in 1963.

This type of memory is based on a thin film with ferroelectric properties. The ferroelectric material is composed mainly of PZT (Pb (ZrTi)O3). Instead of a conventional condenser, a condenser with ferroelectric dielectric medium is used, meaning the structure of a memory cell is similar to that of a DRAM cell.

By creating an electrical field from outside, the ferroelectric dielectric medium is polarised. This polarisation is retained even if the external electrical field is removed, and it is this that creates non-volatile data storage.

If the direction of the electrical field is changed, the direction of the polarisation of the ferroelectric crystals also changes. The process of polarisation itself is rapid, which leads to short writing times (~ 110ns). In addition, the energy required for polarisation, and hence the current consumption during saving, is extremely low. Integrated circuits read out the state of the electrical polarisation and recognise it as logical "1" or "0".

Comparison with Other Memory Types

With 10^{10} guaranteed write cycles, FRAM offers an almost unlimited write life cycle, so unlike with other non-volatile memories, the early appearance of wear and tear will not be a problem. This is mainly due to the fact that FRAM does not require high voltages in order to be erased. This means that no internal charging pumps are required in order to generate these erase voltages, which explains the low current consumption of FRAM when writing data compared to other non-volatile memories.

FRAM memories are written with 3.3V in 0.35um processes. A typical write cycle lasts only 110ns as the data is overwritten and a dedicated erase cycle is not required. These properties pre-destine FRAM memories for applications involving intensive writing which have to save data frequently and quickly in a non-volatile manner.

In direct comparison with EEPROM, FRAM delivers 100,000 times more writing cycles, consumes only one four hundredth of the power but is 30,000 times quicker.

FRAM Benefits to RFID Applications

These properties make FRAM the preferred memory for applications which have to save high data volumes frequently with low energy.

A typical example of this is a passive re-writeable RFID tag. In this case, the entire supply energy must be more or less provided

through the air. As FRAM has the same low power consumption for writing and reading, the same distances are achieved during reading and writing using FRAM-based RFID tags. Conventional tags based on EEPROM technology must be located much closer to the reading/writing device because of the erase energy which is required and must be transferred during write cycles than for simple read access. Particularly with applications in which the RFID tag contains a lot of data which are often changed, FRAM really comes into its own thanks to its high strength of 10^{10} write cycles.

Thanks to their outstanding properties, FRAMs have already been installed in many industrial tags. These are mainly used in automation engineering in order to save the parameters and properties of the goods to be produced. Particularly in the manufacturing of products on manufacturing slides (e.g. automobile production) where the same slide is used repeatedly, an FRAM-based tag keeps costs low as it can be overwritten an almost unlimited number of times. The high write speed combined with larger distance from the read/write device accelerates the entire process and simplifies process control.

FRAM is often used as a replacement for battery-buffered SRAMs, meaning that the manufacturing process and the servicing of the product becomes cost-effective.

Further typical applications for FRAM memories include data loggers and measuring devices (increasing the write frequency and service life), as well as medical equipment that can benefit from the high resistance of FRAM to radiation (alpha, beta, gamma).

FRAM as MCU Embedded Memory

The implementation of FRAM as an embedded memory in microcontrollers will be the next major step. Internally, the FRAM memory in these components is connected serially and therefore provides the typical benefits of FRAM in comparison with an external EEPROM memory, so it is mainly used for rapid, continuous saving of data such as parameters or failsafe values. Mamory makers are moving from "system in package" technology to monolithic use of FRAM instead of FLASH (and RAM).

In May 2007, Fujitsu gave an insight into how this technology could be used in the future and presented the MB95RV100 to the public at the "10th installed system development technical exhibition (ESEC)". This 8-bit evaluation microcontroller provides 64kbytes of FRAM. It replaces both the RAM memory and the Flash memory that are normally used.

The advantage of this approach is that it abolishes the usual practice of fixed partitioning.

This opens up new opportunities for using it as the area for programming and data can be flexibly changed at any time. The entire memory is essentially treated as a RAM.

Special saving of data (normally in the internal Flash or external EEPROMs) can be completely avoided as all data and program parts are located in the FRAM and are therefore saved in a non-volatile manner at all times. This also opens up entirely new opportunities for power-on handling.

The MB95RV100 is currently used by Fujitsu for evaluation purposes. The first 8-bit microcontrollers with a monolithic FRAM memory are likely to enter mass production this year and to be supplied in dedicated applications such as metering.

As an evaluation chip, the MB95RV100 maps the entire 8FX family of Fujitsu 8-bit microcontrollers. This includes standard derivatives of 28 to 64 pins and derivatives of 48 to 100 pins with an integrated LCD controller in housings.

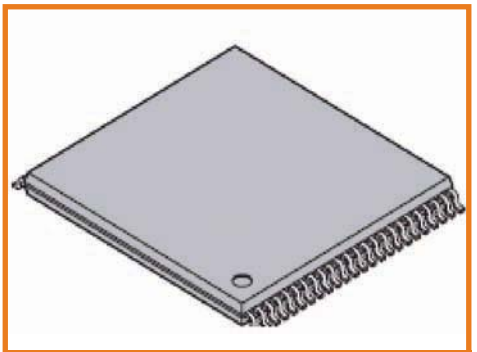


Figure 2: *2Mbit FRAM is currently the largest stand-alone FRAM memory from Fujitsu in mass production*

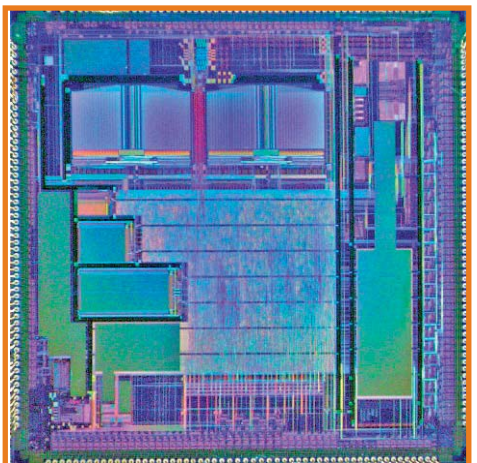


Figure 3: *Silicon of the first FRAM embedded MCU from Fujitsu (MB95RV100)*

	SRAM*1	DRAM*2	EEPROM*3	FLASH*4	FRAM*5
Memory type	Volatile back-up	Volatile	Non-volatile	Non-volatile	Non-volatile
Cell structure	6T	1T/1C	2T	1T	1T/1C 2T/2C
Read cycle (ns)	12	70	200	70	110
Internal write voltage (V)	3.3	3.3	20 (supply voltage 3.3V)	12 (supply voltage 3.3V)	3.3
Write cycle	12ns	70ns	3ms	1 sec.	110ns
Data write	Overwrite	Overwrite	Erase + Write	Erase + Write	Overwrite
Data erase	Unnecessary	Unnecessary	Byte (64 byte page)	Sector (8K/16K/32K/64K)	Unnecessary
Endurance	∞	∞	1E5	1E5	1E10 to 1E12
Stand-by current (µA)	7	1,000	20	5	5
Read operation current (mA)	40	80	5	12	4
Write operation current (mA)	40	80	8	35	4

Notes: *1: 512K × 8bit *2: 2M × 8bit *3: 8K × 8bit *4: 1M × 8bit *5: 8K × 8bit

Table 1: *Comparison of FRAM with other saving technologies*

Fujitsu's FRAM Offerings

Fujitsu has been producing FRAM-based products in large quantities since 1999. To date, more than 500 million FRAM chips have been supplied. Fujitsu offers a series of stand-alone FRAM memories. These allow every system developer to use the valuable benefits of FRAM for his particular application. This means that variants with a parallel 8-bit or 16-bit bus interface with memory sizes of 256kbit, 1Mbit and 2Mbit are available. The new 2Mbit variants MB85R2001 (256k x 8) and MB85R2002 (128k x 16) have been in mass production since early 2007. Components with a larger memory are already in development. The parallel interface is a pseudo SRAM interface, which ensures a simple connection to the target system.

Fujitsu also offers FRAM with a serial SPI interface specifically to allow rapid saving of parameters. The MB85RS256 with a 256kbit memory offers the FRAM-typical 1010 write cycles, can be cycled with up to 15MHz and comes in a compact SOP8 housing. It can be used as a replacement EEPROM, wherever the number of write cycles required during the product's life cycle cannot be guaranteed with EEPROM or the write times of EEPROM are simply too long.

In addition, there are RFID tag ICs with a 256-byte FRAM memory (MB89R119), and even with a 2048-byte FRAM memory (MB89R118), both in accordance with the ISO15693 standard.

In order to fully exploit the rapid writing to the FRAM RFID tags, Fujitsu has integrated special "fast write" commands into the components. These allow speeds which vastly exceed those of the standard commands.

Name	Memory size	Organisation	Interface	Housing
MB85R256H	256kbits	32k x 8	Parallel	SOP/TSOP28
MB85RS256	256kbits	32k x 8	Serial SPI	SOP8
MB85R1001	1Mbits	128k x 8	Parallel	TSOP48
MB85R1002	1Mbits	64k x 16	Parallel	TSOP48
MB85R2001	2Mbits	256k x 8	Parallel	TSOP48
MB85R2002	2Mbits	128k x 16	Parallel	TSOP48

Table 2: *Overview of stand-alone FRAM memory from Fujitsu*

UNDERSTANDING THE FPGA DESIGN FLOW

There is a plethora of field programmable gate array (FPGA) design tools available on the market, ranging from free software that is readily available on the Internet, to high-end software from major EDA companies that may cost tens of thousands of pounds, and while this article is not a review of those tools, hopefully it will give some insight into the processes that need to be carried out by designers. This, of course, will then influence the choices that individual designers make based on their own requirements.

If we start with a simplified version of the standard FPGA design flow, shown in **Figure 1**, we can see the key steps involved in the process of taking our design and turning it into a form that can be used to successfully program an FPGA device.

You can see from Figure 1 that simulation plays a key role in the overall process as it is used several times, but for subtly different reasons. In the early stage of the process the role of simulation is to ensure that the design will meet the specification. This is essentially a "functional" *validation* step, i.e. "doing the right thing". It is also the time to carry out some functional *verification* where the aim is to ensure that the design is "doing the right thing *right*". A key aspect if successfully simulating any design is being effective in the use of VHDL test benches.

Test Benches

The overall goal of any hardware design is to ensure that the design meets the requirements of the design specification. In order to measure this is indeed the case we need to not only simulate the design representation in a hardware description language (such as VHDL), but also to ensure that whatever tests we undertake are appropriate and demonstrate that the specification has been met.

The way that designers can test their designs in a simulator is by creating a "test bench". This is directly analogous to a real experimental test bench, in the sense that stimuli are defined and the responses of the circuit measured to ensure that they meet the specification. In practice, the test bench is simply a VHDL model that generates the required stimuli and checks the responses. This can be in such a way that the designer can view the waveforms and manually check them, or by using VHDL constructs to check the design responses automatically.

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Simple Test Bench – Instantiating Components

Consider a simple combinatorial VHDL model given in the listing below. This simple model is clearly a two-input AND gate, and to test the operation of the component we need to do several things to ensure the correct operation of the device including connectivity, functionality and timing.

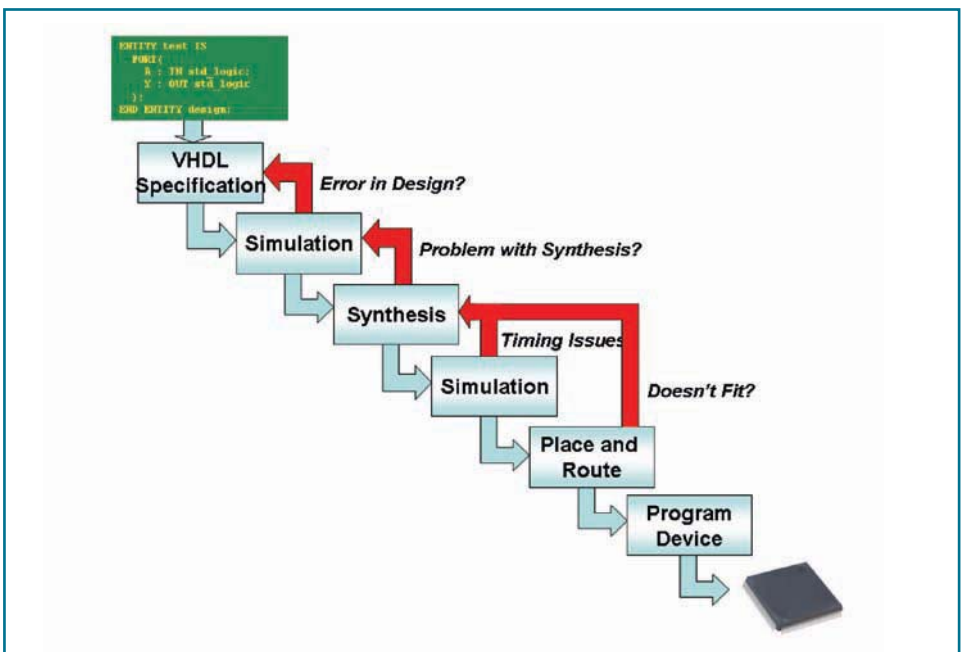

Figure 1: *Outline FPGA design flow*

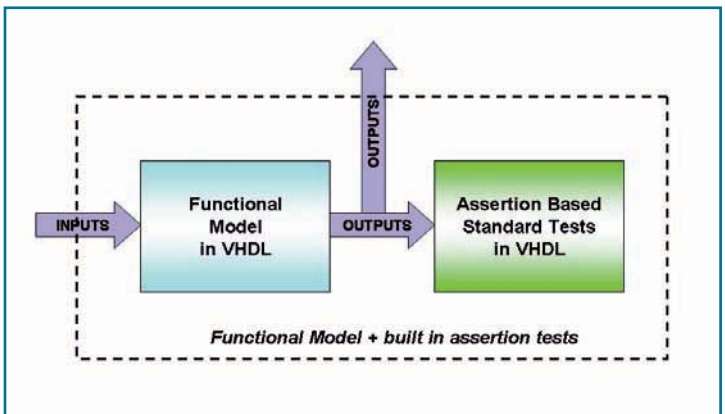

Figure 2: *Extending model behaviour using assertions*

```
library ieee;
use ieee.std_logic_1164.all;
entity cct is
        port (     in0, in1 : in std_logic;
                           out1 : out std_logic
        );
end;

architecture simple of cct is
begin
        out1 <= in0 AND in1 ;
end;
```

First, we must include the component in a new VHDL design. So we need to create a basic test bench. The listing below shows how a basic entity (with no connections) is created and then the architecture contains both the component declaration and the signals to test the design.

```
— library declarations
library ieee;
use ieee.std_logic_1164.all;

— empty entity declaration
entity test is
end;

— test bench architecture
architecture testbench of test is
        — component declaration
        component cct
                port (     in0, in1 : in std_logic;
                           out1 : out std_logic );
        end component;
        — test bench signal declarations
        signal in0, in1, out1 : std_logic;
— architecture body
Begin
        — declare the Circuit Under Test (CUT)
        CUT : cct port map ( in0, in1, out1 );
end;
```

This test bench will compile in a VHDL simulator, but is not particularly useful as there are no definitions of the input stimuli (signals in0 and in1) that will exercise the circuit under test (CUT). If we wish to add stimuli to our test bench we have some significant advantages over our design VHDL – the most appealing is that we generally don't need to adhere to any design rules or even make the code synthesisable. Test bench code is generally designed to be "off chip" and therefore we can make the code as abstract or behavioural as we like and it will still be fit for purpose. We can use wait statements, file read and write, assertions and other non-synthesisable code options.

Adding Stimuli

In order to add a basic set of stimuli to our test bench, we could simply define the values of the input signals in0 and in1 with a simple signal assignment:

```
        begin
                CUT : cct port map ( in0, in1, out1 );

                in0 <= '0';
                in1 <= '1';
        end;
```

Clearly this is not very complex or dynamic test bench, so to add a sequence of events we can modify the signal assignments to include numerous value,time pairs defining a sequence of values.

```
        begin
                CUT : cct port map ( in0, in1, out1 );

                in0 <= '0' after 0 ns, '1' after 10 ns, '0' after
        20 ns;
                in1 <= '0' after 0 ns, '1' after 15 ns, '0' after
        25 ns;
          end;
```

While this method is useful for small circuits, clearly for more complex realistic designs it is of limited value. Another approach is to define a constant array of values that allow a number of tests to be carried out with a relatively simple test bench and applying a different set of stimuli and responses in turn.

For example, we can exhaustively test our simple two input logic design using a set of data in a **record**. A VHDL record is simply a collection of types grouped together defined as a new type.

```
type testdata is record
        in0 : std_logic;
        in1 : std_logic;
end;
```

With a new composite type, such as a record, we can then create an array, just as in any standard VHDL type. This requires another type declaration, of the array type itself.

type data_array is array (natural range <>) of data_array

With these two new types we can simply declare a constant (of type data_array) that is an array of record values (of type testdata) that fully describe the data set to be used to test the design. Notice that the type data_array does not have a default range, but that this is defined by the declaration in this particular test bench.

```
constant test_data : data_array := ( ('0', '0'), ('0', '1'), ('1', '0'),
('1', '1') );
```

The beauty of this approach is that we can change from a system that requires every test stimulus to be defined explicitly, to one where a generic test data process will read values from pre-defined arrays of data. In the simple test example presented here, an example process to apply each set of test data in turn could be implemented as follows:

```
process
begin
        for i in test_data'range loop
                in0 <= test_data(i).in0;
                in1 <= test_data(i).in1;
                wait for 100 ns;
        end loop
        wait;
end process;
```

There are several interesting aspects to this piece of test bench VHDL. The first is that we can use behavioural VHDL (wait for 100ns) as we are not constrained to synthesise this to hardware. Secondly, the test bench becomes unconstrained by the size of the data set by using the 'range operator'. Finally, the individual record elements are accessed using the hierarchical construct test_data(i).in0 or test_data(i).in1 respectively.

Assertions

Assertions are used to check if certain conditions have been met in the model and are extremely useful in debugging models. Some examples show how not only values can be tested, but also how timing conditions can be tested.

```
assert value <= max_value
 report "Value too large";
assert clock_width >= 100 ns
 report "clock width too small"
 severity failure;
```

While this looks on the surface to be just another form of test bench statement, the power of using assertions comes in the development of hierarchical blocks that can be used as a standard test alongside the functional block of VHDL, re-usable standard assertion blocks and also by linking up with stimulus blocks to ensure correct operation.

For example, say that the function being developed is an ALU (Arithmetic Logic Unit) for a processor. Clearly, to define each individual assertion test from scratch is going to be a laborious and time-consuming task. However, if we define a standard test, for say one bit at a time, then extend this to n bits, then we can develop a simple, single test that can be applied in all contexts, to validate the design.

This is shown in **Figure 2**, where we have extended the functional model to include the testing we need to ensure that the model can be debugged adequately under test conditions and the correct behaviour validated.

Synthesis

As can be seen from Figure 1, synthesis is the key stage between high-level design and the physical place-and-route which is the final product of the design flow. There are several different types of synthesis ranging from behavioural, to RTL and finally physical synthesis.

Behavioural synthesis is the mechanism by which high level abstract models are synthesised to an intermediate model that is physically realisable. Behavioural models can be written in VHDL that are not directly synthesisable and, so, care must be taken with high level models to ensure that this can take place, in fact.

There are a limited number of tools that can synthesise behavioural VHDL and these include the Behavioural Compiler from Synopsys and MOODS, a research synthesis platform from the University of Southampton.

RTL (Register Transfer Level) synthesis is what most designers call synthesis, which is the mechanism whereby a direct translation of structural and register level VHDL can be synthesised to individual gates targeted at a specific FPGA platform. At this stage, detailed timing analysis can be carried out and an estimate of power consumption obtained.

There are many commercial synthesis software packages including Design Compiler (Synopsys), Leonardo Spectrum (Mentor Graphics) and Synplify (Synplicity), available at a variety of prices (even though this is not an exhaustive list).

Synthesis Issues

Synthesis basically transforms program-like VHDL into a true hardware design (netlist). It requires a set of inputs, a VHDL description, timing constraints (when outputs need to be ready, when inputs will be ready, data to estimate wire delay), a technology to map to (list of available blocks and their size/timing information) and information about design priorities (area vs speed)

For big designs, the VHDL will typically be broken into modules and then synthesised separately. 10K gates per module was a reasonable size in the 1990s, however tools can handle a lot more now.

RTL as an Input Format

Register Transfer Level (RTL) VHDL is the input to most standard synthesis software tools. The VHDL must be written in a form that contains Registers, State Machines (FSM) and combinational logic functions.

The synthesis software translates these blocks and functions into gates and library cells from the FPGA library. Using RTL VHDL restricts the scope of the designer as it precludes algorithmic design, as we will see later. This approach forces the

designer to think at quite a low level, making the resulting code sometimes verbose and cumbersome. It also forces structural decisions early in the design process – restrictive and not always advisable, or helpful.

Physical Design Flow (Place and Route)

Synthesis generates a netlist of devices plus interconnections. The "place and route" software figures out where the devices go and how to connect them. The results are not as good as you'd like; a 40-60% utilisation of devices and wires is typical. The designer can trade off run time against greater utilisation to some degree, but there are serious limits. Typically, the FPGA vendor will provide a software toolkit (such as the Xilinx Design Navigator, or Altera's Quartus tools) that manages the steps involved in physical design.

Regardless of the particular physical synthesis flow chosen, the steps required to translate the VHDL or EDIF output from an RTL synthesis software programme into a physically downloadable bit file are essentially the same and are listed below:

1. Translate
2. Map
3. Place
4. Route
5. Generate Accurate timing models and reports
6. Create binary files for download to device

Place and Route

The basic goal of place-and-route is to first take the netlist of fundamental cells obtained from synthesis and establish the most efficient placement of those cells on the target FPGA. This is not just as simple as randomly placing cells across the device, as timing is affected fundamentally by the distance between cells, so the placement needs to be "timing aware".

There are a variety of techniques to measure this, which basically take the form of a correlation between routing and raw distance between cells. The second task is then to establish the optimum connections between the individual cells (routing). Once the routing has been completed, various forms of timing analysis need to be carried out to ensure that the device will still work when it is programmed onto the device, *and* how fast the device can operate.

Timing Analysis

Static timing analysis is the most commonly-used approach. In Static Timing Analysis, we calculate the delay from each input to each output of all devices. The delays are added up along each path through circuit to get the critical path through the design and hence the fastest design speed.

This works as long as there are no cycles in the circuit, however in these cases the analysis becomes less easy. Design software allows you to break cycles at registers to handle feedback if this is the case.

As in any timing analysis, the designer can trade off some accuracy for run time. Digital simulation software such as Modelsim or Verilog will give fast results, but will use approximate models of timing, whereas analogue simulation tools like SPICE will give more accurate numbers, but take much longer to run.

Design Pitfalls

The most common mistake that inexperienced designers make is simply making things too complex. The best approach to successful design is to keep the design elements simple, and the easiest way to manage that is efficient use of hierarchy.

The second mistake that is closely related to design complexity is not testing enough. It is vital to ensure that all aspects of the design are adequately tested. This means not only carrying out basic functional testing, but also systematic testing and checking for redundant states and potential error states.

Another common pitfall is to use multiple clocks unnecessarily. Multiple clocks can create timing related bugs that are transient or hardware dependent. They can also occur in hardware and yet be missed by simulation.

VHDL Issues for FPGA Design

Initialisation

Any default values of signals and variables are ignored. This means that you must ensure that synchronous (or asynchronous) sets and resets must be used on all flip-flops to ensure a stable starting condition. Remember that synthesis tools are basically stupid and follow a basic set of rules that may not always result in the hardware that you expect.

Floating Point Numbers and Operations

Data types using floating point are currently not supported by synthesis software tools. They generally require 32 bits and the requisite hardware is just too large for most FPGA and ASIC platforms.

Practical Aspects

This article has introduced the practical aspect of developing test benches and validating VHDL models using simulation. This is an often overlooked skill in VHDL (or any hardware description language) and is vital to ensuring correct behaviour of the final implemented design.

We have also introduced the concept of design synthesis and highlighted the problem of not only ensuring that a design simulates correctly, but also how we can make sure that the design will synthesise to the target technology and still operate correctly with practical delays and parasitics. Finally, we have raised some of the practical implementation issues and potential problems that can occur with real designs.

An important concept useful to define here is the difference between validation and verification. The terms are often confused leading to problems in the final design and meeting a specification. Validation is the task of ensuring that the design is "doing the right thing". If the specification asks for a low pass filter, then we must implement a low pass filter to have a valid design. We can even be more specific and state that the design must perform within a constraint. Verification, on the other hand, is much more specific and can be stated as "doing the right thing *right*". In other words, verification is ensuring that not only does our design do what is required functionally, but in addition it must meet all the criteria defined by the specification, preferably with some headroom to ensure that the design will operate to the specification under all possible operating conditions. ■

To find out more on the subject of practical FPGA design, check out Dr Peter R. Wilson's recently published book "Design Recipes for FPGAs".

PAUL DODDS, SENIOR ENGINEER AT CLARITYCAP, SUPPLIER OF AUDIO CAPACITORS TO THE HI-FI MARKET, GOES OVER THE FINDINGS OF A RECENT RESEARCH THAT ESTABLISHED THE EFFECT OF THE CAPACITOR'S PROPERTIES ON THE QUALITY OF SOUND

THE EFFECTS OF AUDIO CAPACITORS ON SOUND QUALITY

During recent years it has become clear that to stay ahead of the competition and keep producing audio capacitors of the highest quality we at ClarityCap, suppliers of high-quality audio capacitors, needed a detailed understanding of what properties of capacitors affected the audio quality in hi-fi systems. Specifically, we wanted to understand the underlying technology of our capacitors, without looking at exotic materials and strange assemblies.

We therefore set up a two-year project with the Acoustics Research Centre (ARC) at the University of Salford, known for their expertise in the field of audio and acoustics, to investigate the material properties of audio capacitors.

This research programme was undertaken as part of the UK Department of Industry Knowledge Transfer Partnership programme. The research is partly funded by the British government and partly by the company with the University offering its research facilities as part of the arrangement. As part of the programme, the research team had to survey many of world renowned loudspeaker engineers, gathering their thoughts on capacitor performance and the effects that the components had within their finished products.

During the course of such an in-depth investigation, we also measured many of our components as well as that of competitor products in great detail.

Initial Investigations

Well over 300,000 individual measurements were taken on a huge range of capacitors using all available voltage ratings and aspect ratios. A state-of-the-art component analyser and automation system was used to gather an enormous amount of data.

Metallised film capacitors have excellent electrical properties that make them ideal for use as audio capacitors. They have an inherently low Equivalent Series Resistance (ESR) in the order of milliohms.

One criticism levelled at many types of capacitor wound from film is the stray inductance found inside the component. **Figure 1** shows a basic equivalent circuit of a capacitor, where L is the stray inductance of the capacitor including that of the leads, C is the capacitance and R is the ESR. The phasor diagram of this system is shown in **Figure 2**.

When multiplying through by the current, i.e. to obtain impedances for each individual element, the following transformations occur:

$$V_L \rightarrow \omega L, \quad V_R \rightarrow R, \quad V_C \rightarrow 1/\omega C$$

The impedance of the capacitor's equivalent circuit can be found using:

$$|Z| = \sqrt{R^2 + \left(\frac{1}{\omega C} - \omega L\right)^2}$$

where: Z is impedance (ohms)
R is ESR (ohms)
ω is frequency (rad/s)
C is capacitance (F)
L is inductance (H)

This implies that any stray inductance gives rise to a capacitance that increases sharply with frequency. It is easy to understand why that would be a problem in audio systems, where several octaves will be covered by a single driver.

When ClarityCap makes capacitors, we short all of the turns out by spraying the end of the capacitor with metal. This has several benefits. The first is that it provides an excellent end connection with low resistance and high mechanical strength (see N. Williams's ***"Metallised Film Capacitors for High Frequency High Current Applications"***, IEE Colloquium on Capacitors & Inductors for Power Electronics, 7th March 1996). Importantly, it virtually eliminates all of

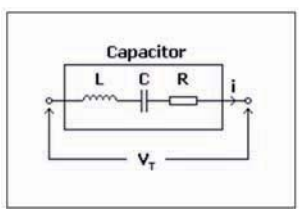

Figure 1: *Basic equivalent circuit of capacitor*

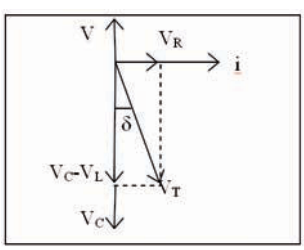

Figure 2: *Phasor diagram of capacitor equivalent circuit*

the stray inductance due to the winding of turns. The result is a capacitor with stable electrical properties and a smooth frequency characteristic.

However, after all of the electrical measurements were taken, we drew a blank when it came to explaining the audible differences between capacitors – as expected, there were small variations in terms of ESR but nothing that explained the differences we could hear when listening to the capacitors.

Mechanical Resonances

Then, we began to investigate a key feature of audio capacitors: the mechanical resonance. This is a physical deformation of the capacitor walls which occurs as a result of the audio signal passing through the component – much like an electrostatic speaker. This resonance is dependent on the size, shape, materials and manufacturing parameters of the capacitors.

This effect has been known about for years as it plays a part in the impulse strength of capacitors. However, the effect has never been considered to be significant enough to affect a hi-fi system's audio reproduction due to the low energy involved.

In order to investigate it properly, we developed two new and innovative excitation and measurement techniques. The first was based upon a continuous swept sine wave being applied to the component. The second, using unique in-house designed equipment, determined an impulse response for the capacitor.

However, the key moment was when we found that these two traces aligned almost perfectly. When further research showed a phase change at the peak frequency, we knew we had identified a resonance in the capacitor.

Analysis of the vibrations generated by both of these methods yielded several interesting features. For instance, a lot of detail can be obtained about the manufacturing process.

The resonances always occurred between 5 and 25kHz – exactly the range of frequencies where the capacitors would be used. We characterised the resonances for a huge variety of capacitor types, values, sizes and shapes, and examined many competitor products too. All, without exception, followed this pattern.

These resonances have been examined and measured at the micron level using laser vibrometry at ARC. The discovery and characterisation of these mechanical resonances was outlined in our paper entitled ***"Assessing The Effects Of Loudspeaker Crossover Components On Sound Quality"*** by P.S. Dodds, P.J. Duncan and N. Williams, given at the Institute of Acoustics conference on Reproduced Sound in November 2006

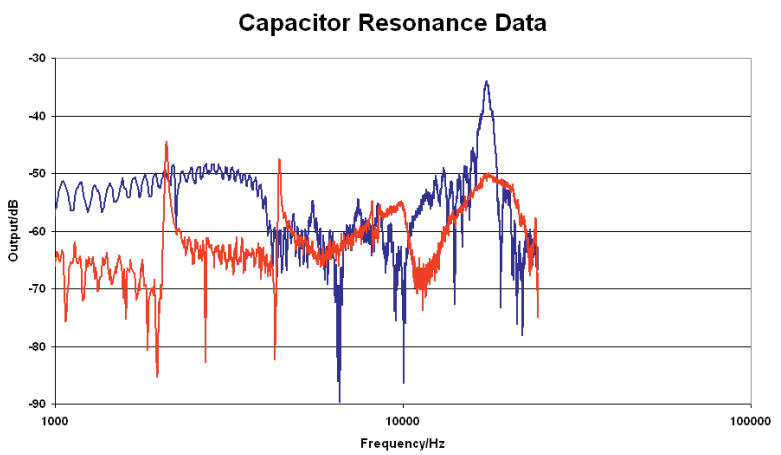

Figure 3: *Capacitor resonance data*

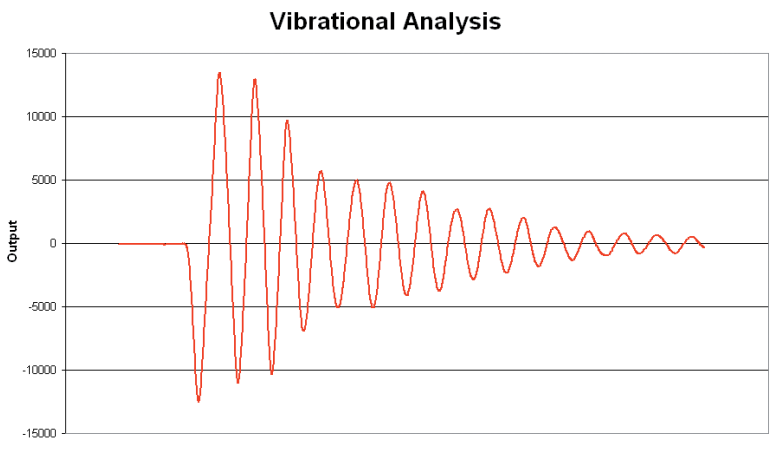

Figure 4: *Impulse response analysis*

The Effect on Sound Quality

The next challenge was to identify whether these resonances had an effect on the sound quality of a system and on what aspects of the sound.

We conducted listening tests in the specialist listening facilities at the University of Salford which have shown conclusively the effect these resonances have on sound quality. We designed capacitors with differing resonances and asked the panel to compare them to each other. The tests were blind and based on the ITU-R BS 1116-1 standard; they involved an independent panel of over 30 listeners.

The listeners were asked for their opinions on the sonic differences between the capacitors and to identify the characteristics of the sound that had been affected. They were also asked to state a preference, if possible, between the capacitors.

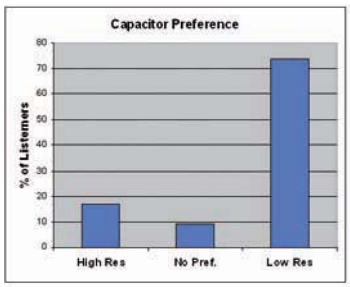

Figure 5: *Capacitor Preference*

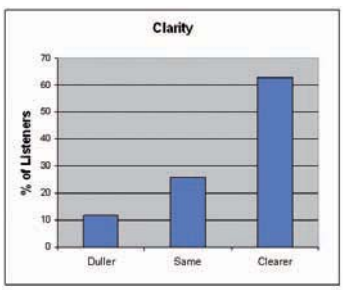

Figure 6: *Clarity*

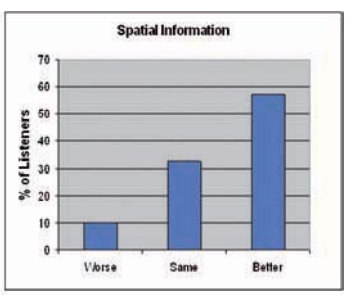

Figure 7: *Spatial Information*

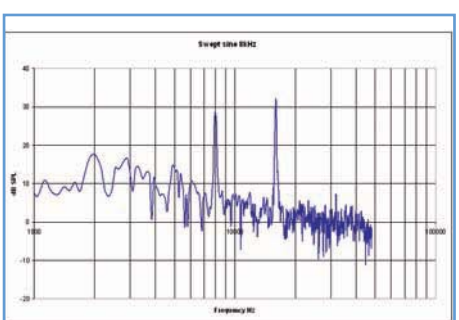

Figure 8 *The results of a 'frequency doubling' effect*

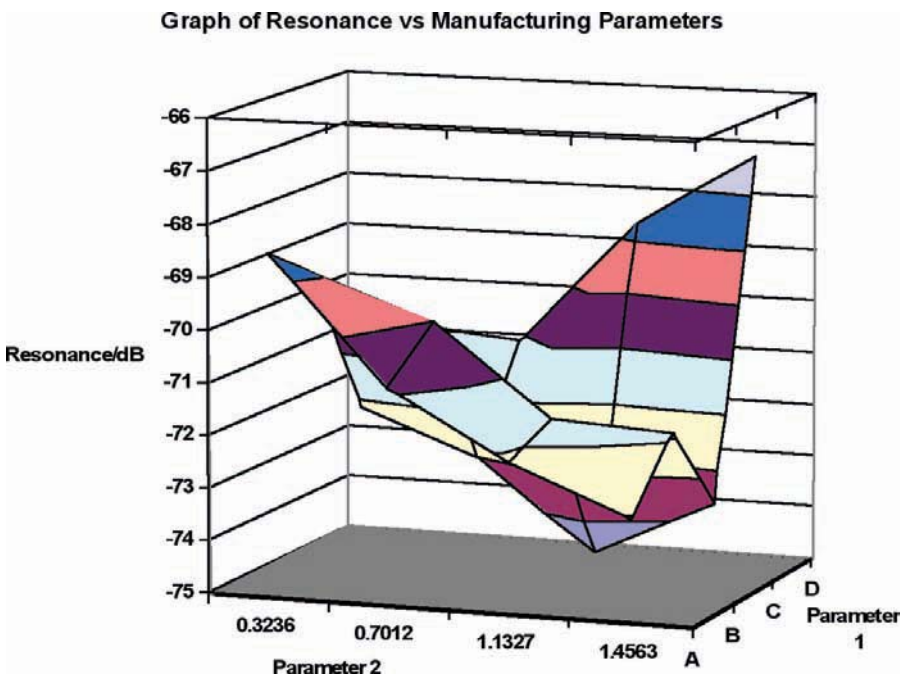

Figure 9: *Graph of resonance vs manufacturing parameters*

The results were dramatic: over 70% stated a clear preference for the capacitors with lower mechanical resonances.

Most importantly, the tests helped us to identify how different properties of the capacitors affected different properties of the reproduced sound. We were able to identify the manufacturing factors which affect the clarity and spatial detail in our audio capacitors.

The Mechanism

The answer to how these resonances occur requires some background in capacitor technology. Metallised film capacitors are effectively multi-layered devices: a laminated structure, consisting of the interleaved plates of the capacitor.

When charged, the capacitor plates are attracted to each other, forming a compressive force across the body of the capacitor. During discharge, this force is released and the plates return to their resting position.

Since the force between the plates of a charged capacitor is always attractive, driving with a sine wave, like an audio signal, will produce a mechanical force at twice the driving frequency; an example of this 'frequency doubling' effect is shown in **Figure 8**. This raises the issue of the capacitor being a possible source of intermodulation distortion products at double the frequency of any audio signals present.

The Perfect Capacitor?

Armed with this knowledge, we set about designing a capacitor with the lowest possible resonances. We examined the manufacturing process in fine detail and identified the key processes that determine the mechanical resonance of a capacitor. We developed a matrix of the parameters and tested every combination to find the optimum solution. The graph in **Figure 9** shows how we arrived at the lowest possible resonance capacitor.

We are now working on bringing a product utilising this knowledge to market. ■

Debate is Alive and Well in EW

It's good to see letters in Electronics World, especially Mike Hall's letter in the February issue, which expresses sentiments similar to those of several readers over the last few years as well as your own [*'Power on the menu'*, Electronics World, December 2007].

Chris Williams might like to see an article by Tom Stockdale which describes and analyses the effects of using CFLs in bedrooms in an article titled *'Angina can be induced by electromagnetic fields'* published by The McCarrison Society, 41/3 pp 18-21

Tony Callegari

Those Dogging CFL Issues

Chris Williams in his article *'Looking at Light bulbs'* [Electronics World, March 2008, p43] gave us many interesting facts about the new compact fluorescent lamps that are now so popular (and cheap – so cheap that my local Waitrose supermarket was giving them away free when I last visited there).

However, some of Chris's statements should not go unchallenged.

– The old incandescent bulbs contributed heat, which is not produced with low-energy lamps, and has to be supplied by the central heating instead. Well, yes, but hot air produced at ceiling level tends to stay there, warming the ceiling, but not the room, so its loss is unlikely to be noticed in practice.

– The luminaires in which the new compact fluorescent lamps are mounted lose quite a lot of the light. True, but exactly the same is true of the luminaries for the old-style incandescent lamps, so we still get the benefit of the higher efficiency of the new CFLs.

– CFLs contain mercury. This is true, but I've heard (though not been able to confirm) that the amount of mercury in a modern CFL is less than the extra mercury that would have been emitted into the environment by the power stations powering an equivalent incandescent lamp over the lifetime of the CFL.

All this goes to show that, in the words of Oscar Wilde, "the truth is rarely plain and never simple".

It does seem surprising that the quality of lamps is not controlled by an EC directive, so we are at the mercy of low-energy lamp suppliers as regards colour and warm-up time, and now Chris Williams tells us that the new cheap lamps radiate non-trivial levels of UV light.

Never mind, we are now being told that LED lighting is just around the corner…

Brian Pollard

Chris Williams from the UK Displays & Lighting (UKDL) Knowledge Transfer Network replies:

Thanks for reading my article and responding to it at length. I'd like to address your comments in turn:

1. Incandescent bulbs generate heat, but this is at ceiling level so not usable for room heating? This is a two-edged argument for discussion over a beer or two around the fireside.

Heat from bulbs in ground floor rooms – usually on for several hours – will gradually percolate upwards to higher levels, if possible. These are often the bedrooms, so there is likely to be some benefit, even if it is small. The anecdotal information from my colleagues in industry is that the electrical energy saving by moving from incandescents to CFLs is lost by even the slightest nudge upwards in the temperature controller of the central heating system. Since most heating is by gas or oil, the savings in the electricity bill will be seen separately to the cost of the heating bill and any cross-connection may not be realised.

2. Luminaires lose light. Yes – just about all common designs of luminaires will absorb much of the light created from the bulbs they contain. One of our UKDL member companies was shocked to realise that the very attractive luminaires they made for their T5 fluorescent lamps cut the efficiency of the delivered light from 104 lumens per watt at the lamp itself down to just 38 lumens per watt outside the luminaire.

Perhaps the measure of efficiency we adopt to compare all different types of lighting should be from the "wallsocket supply" (240V ac in the UK) to the light measured in the area we want to use it. That would give us a true "delivered lumens per watt" measure to compare LEDs, CFLs, fluorescents, OLEDs and any other type of light source.

3. CFLs contain mercury. This is another "smoke and mirrors" topic. Electrical power stations emit mercury as a tiny constituent of their exhaust gases. This emission is generally in the high velocity plume that will be dispersed at high levels in our atmosphere.

If we accidentally break, or improperly dispose of, our CFL lamps and fluorescent tubes, we are discharging mercury at ground level. This will locally pollute landfill and our own houses, and will certainly migrate downwards towards the watercourse over an extended period of time.

In an ideal world we would see no mercury (or any other heavy metal) discharged at any level into the environment, but as a matter of personal preference, I feel easier about it being widely dispersed at 10-20,000 feet rather than in a more localised form in my immediate vicinity.

As Brian concludes so correctly, "the truth is rarely plain, and never simple!"

CURRENT LIMITERS USING SINGLE CDTA AND APPLICATIONS

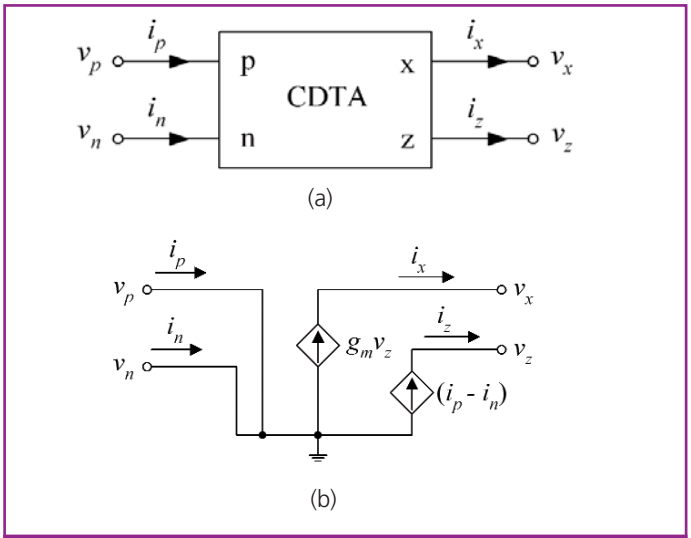

***Figure 1**: CDTA (a) circuit symbol (b) equivalent circuit*

Generally, the current limiter (CL) is an alternative way to handle non-linear problems. In the area of analogue signal processing applications, it can be widely found as the basic element in the design of non-linear components and networks, such as non-linear resistors, chaotic oscillators, precision rectifiers and piecewise-linear function approximation generators.

Recently, a new current-mode active element with two current inputs and two kinds of current output, which is called a Current Differencing Transconductance Amplifier (CDTA), has been introduced (see D. Biolek's ***"CDTA-Building block for current-mode analogue signal processing"***, Proceeding of the ECCTD'03, vol. III, Krakow, Poland; pp.397-400, 2003). This device is synthesised using the current differencing nature of the modified differential current conveyor (MDCC) and a multiple-output transconductance amplifier to facilitate the implementation of current-mode analogue signal processing. As a result, several implementations have emerged, such as active filters, oscillator and amplifiers using CDTAs as active components.

Non-linear CDTA applications are also expected, in particular precision rectifiers, current-mode Schmitt triggers and current-mode multipliers. Unfortunately, not much is being reported in literature on the use of CDTAs for synthesising current limiter circuits.

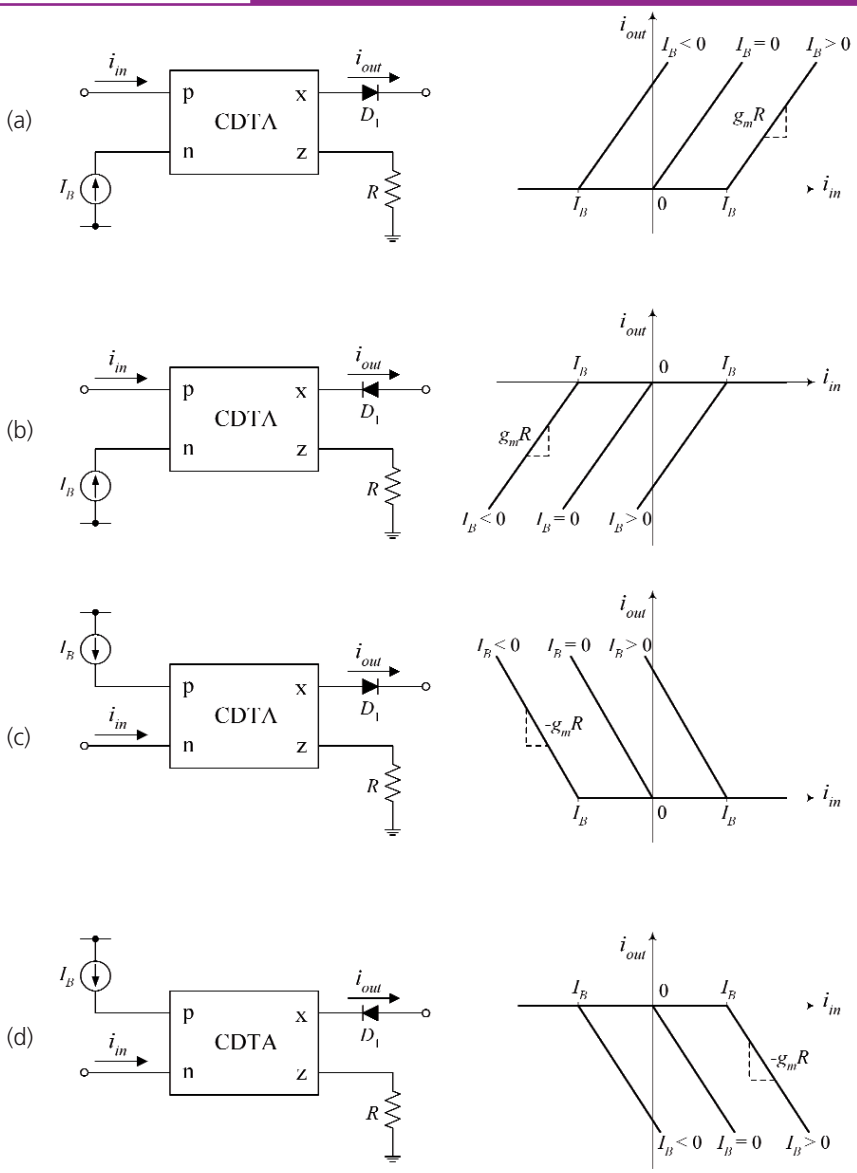

***Figure 2**: Proposed CDTA-based current limiter building blocks*

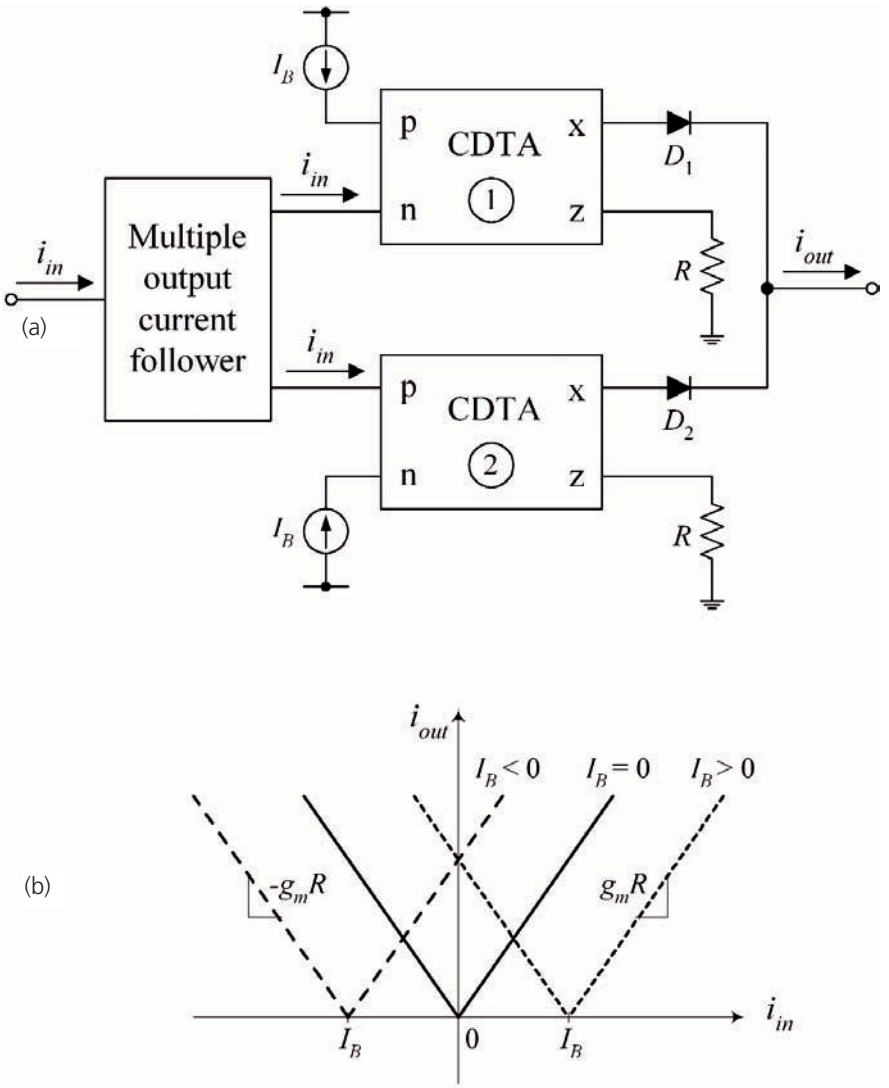

***Figure 3**: Positive current-mode full-wave rectifier (a) circuit implementation (b) transfer characteristic curve*

Here, we propose the applicability of CDTAs as the fundamental active elements for designing the simple CL building blocks. The breakpoints and slopes of the realised transfer curves can be electronically programmed by the transconductance gain (g_m) of the CDTA. To demonstrate versatility of the proposed electronically tunable CLs, some non-linear applications to programmable current-mode precision full-wave rectifiers and piecewise-linear function approximation generator are also presented.

Circuit Description and Operation

The circuit representation and the equivalent circuit of the CDTA are shown in **Figure 1**. The terminal relation of the CDTA can be characterised by the following set of equations:

$v_p = v_n = 0$, $i_z = i_p - i_n$ and $i_x = g_m v_z = g_m Z_z i_z$ (1)

where Z_z is an external impedance connected at the terminal z. In general, the g_m value is linearly adjustable over several decades by a supplied bias current/voltage, which lends electronic controllability to design circuit parameters. It may also be emphasised that the electronic controllability becomes very important when the circuit is in a variety of design specifications and in the integrated circuit (IC) form.

Figure 2 shows the basic building blocks of the proposed CDTA-based CLs and their corresponding transfer characteristic curves. First, consider the proposed circuit depicted in Figure 2a, where i_{in} is an input current and I_B is the breakpoint current. If $i_{in} \le I_B$, the diode is cut-off. Since no current flows through the diode D_1 ($I_{D1} = 0$), the output current becomes zero ($i_{out} = 0$). For the case of $i_{in} > I_B$, the output current i_{out} will flow through the diode D_1. Therefore, the output current i_{out} of the circuit related to the breakpoint current I_B and the gain g_m can be given as :

$$i_{out} = \begin{cases} 0 & \text{for } i_{in} \le I_B \\ g_m R(i_{in} - I_B) & \text{for } i_{in} > I_B \end{cases} \quad (2)$$

From **Equation 2**, we will simply state that both breakpoint and slope of the transfer characteristic curve can be electronically controlled by tuning the values of the current I_B and the gain g_m, which gives an additional flexibility in the non-linear function approximation design problem. In addition, by the same principle, the remaining proposed circuits shown in Figures 2b-d will give similar transfer characteristics to Equation 2, depending on the terminal connection of the CDTA and the diode.

Applications

The proposed CLs of Figure 2 can be effectively used to implement current-

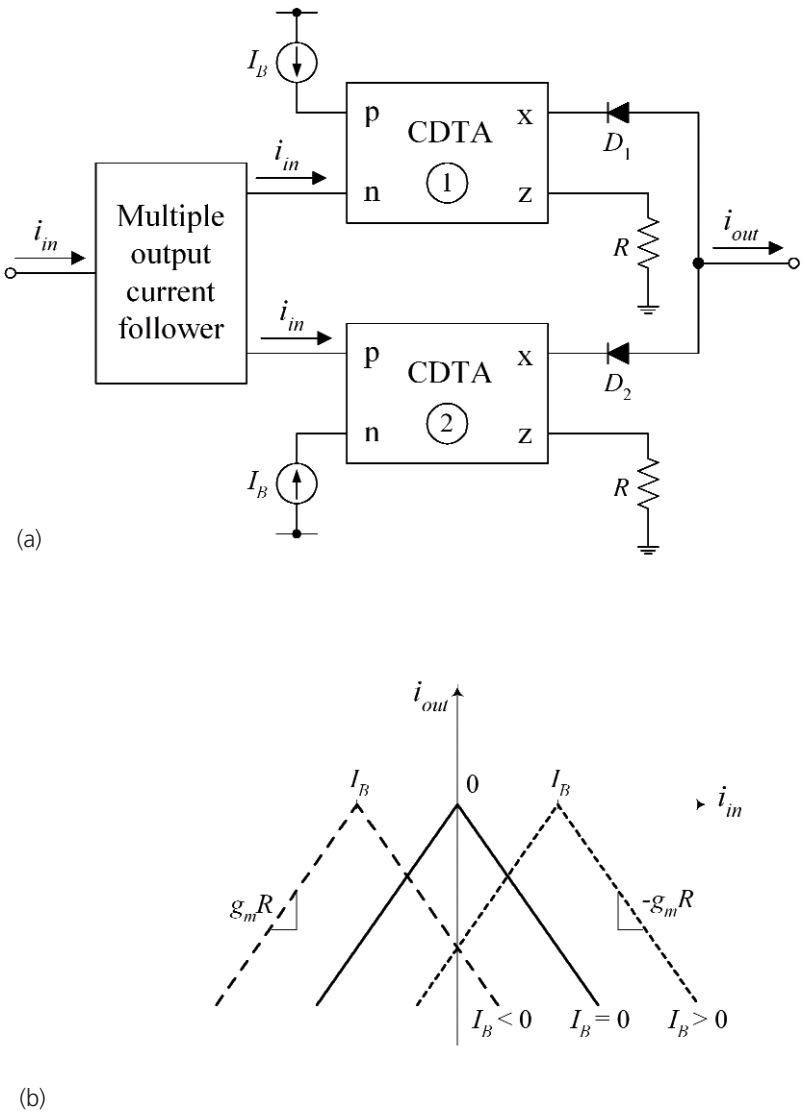

***Figure 4**: Negative current-mode full-wave rectifier (a) circuit implementation (b) transfer characteristic curve*

mode precision full-wave rectifiers as shown in **Figures 3** and **4**. The multiple-output current follower stage is the circuit that generates, from the input current (i_{in}), multiple output currents in the same direction. It can be realised by using the basic current mirror with multi-output terminals. From the operation of the proposed CDTA-based CLs described above and by setting $g_{m1} = g_{m2} = g_m$, the relations between the input and the output currents of the two new circuits can be expressed as follows.

$$i_{out} = |g_m R(i_{in} - I_B)| \qquad (3)$$

$$-i_{out} = |g_m R(i_{in} - I_B)| \qquad (4)$$

This means that the circuits of Figures 3 and 4 operate as the positive and negative current-mode full-wave rectifiers, respectively. It is worth nothing that the slopes of the transfer curves can still be continuously controlled by tuning g_{m1} of the CDTA1 for the negative slope and by tuning g_{m2} of the CDTA2 for the positive slope.

The applications of the proposed CLs for implementing the piecewise-linear (PWL) function approximation circuits can also be realised. As an example, the desired transfer characteristic is shown in **Figure 5a** (see next page) which is composed of three linear segments. The required individual slopes due to each CDTA-based CL of Figure 2 are indicated in the lower part of Figure 5a, and the actual circuit implementation can be shown in **Figure 5b.**

It should be noted that the slopes S_0, S_1 and S_2 of the composed resulting transfer characteristics can be easily determined by adjusting the values of $g_{m1}R_1$, $g_{m2}R_2$ and $g_{m3}R_3$, respectively. From the above discussions, it is further apparent that a class of arbitrary non-linear current generators can be synthesised.

Conclusion

A simple approach for the syntheses of the current limiters using the CDTA as an active element is proposed. The proposed CDTA-based CLs were then used as fundamental circuit building blocks to implement integrable non-linear function circuits, such as current-mode precision full-wave rectifiers and a piecewise-linear function approximation circuit. All the resulting synthetic building blocks will also posses several desirable properties, namely, the positive and negative slopes of the linear segments and breakpoints can be electronically tunable through the g_m-value of the CDTA.

Worapong Tangsrirat
Faculty of Engineering and Research Center for Communications and Information Technology (ReCCIT)
Thailand

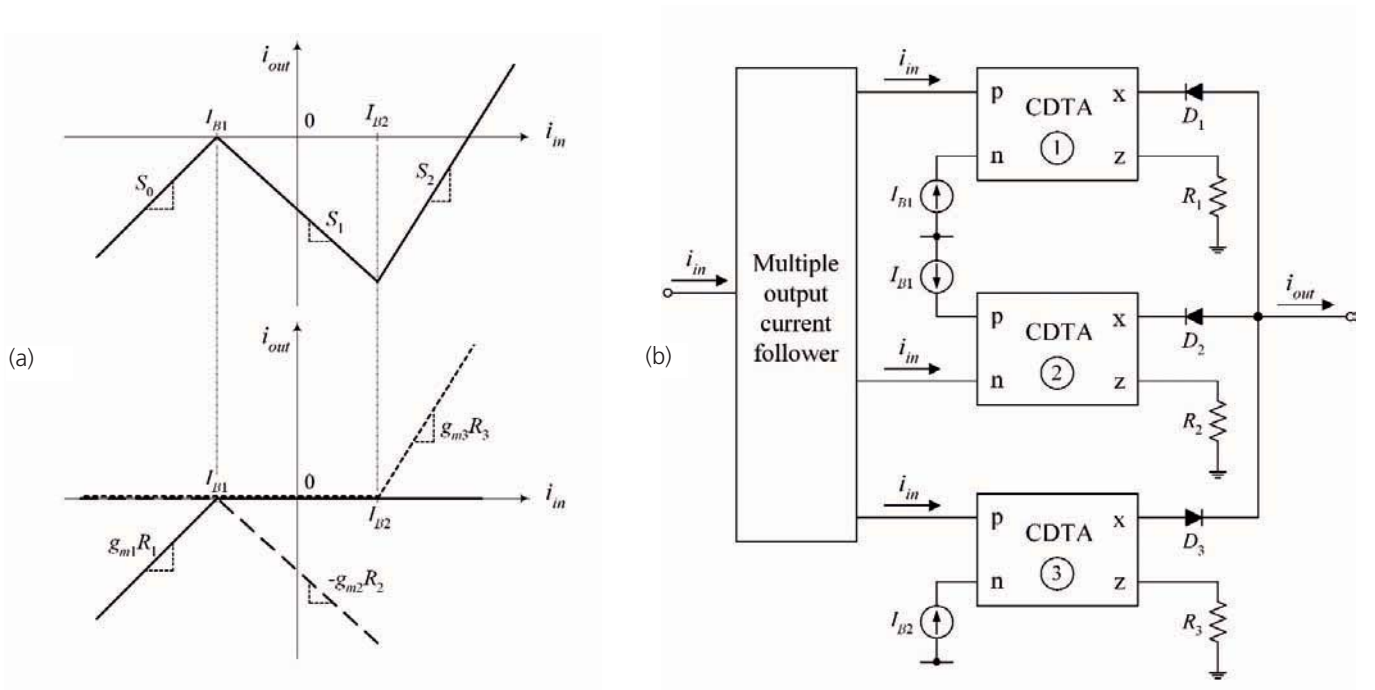

***Figure 5**: Piecewise-linear (PWL) function approximation function (a) desired transfer characteristic curve (b) circuit implementation*

IS 3-D FINALLY ON ITS WAY TO A SHOP NEAR YOU? DO YOU WANT IT IF IT IS?

By Chris Williams, UKDL

For all the time that I have been working in the displays industry (33 years and counting…), display engineers have been experimenting with techniques to deliver a true three-dimensional (3-D) image to viewers using their display systems. They have been promising to deliver extraordinary real-world experiences to viewers using only 2-D displays, except for the extra few who promise to deliver volumetric 3-D imagery, which we can best relate to by thinking of the Star Trek Holodeck system!

The most common types of 3-D display are based on enhanced variants of conventional 2-D displays. The volumetric 3-D is completely different and worthy of its own comments in a future column.

The argument "for" from the 3-D community starts from the basic premise that what we 'see' on our two-dimensional displays today simply isn't good enough compared to the original image from which the source data is derived. The limited number of pixels in the display, together with the limited dynamic range of brightness and colour, results in images being presented (they say) that have insufficient depth cues for us to believe that the images on the screen are real. We must have (they say) additional data to allow two real-time images to be displayed – one that is targeted at the viewer's left eye and one that is targeted at the right eye. With this additional data the brain can now interpret more depth cues and can interpolate more accurately the shape and position of objects on the display screen, giving us an accurate mental image of the original source material.

Who would benefit from more accuracy? Well, I can concede immediately that a neurosurgeon operating on a patient using remotely controlled micro-surgical instruments will have greater chance of success if the image he is using to plan his dicing and splicing is as accurate as possible. Seeing the exact shape of an artery and its exact location with regard to adjacent veins and organs is crucial if you are about to go cutting around without a direct line of sight. I can further accept that such 3-D imagery is vitally important for the technican to remove, using remote forceps, the spanner that the engineer dropped into the works of the shuttle engine under repair in orbit.

Figure 1: *The reason for using 3-D is to deliver depth information that makes object look convincingly real, but can this be done just as well by using high resolution displays with good colour depth?*

But is it really necessary for you and me? Will the quality of our lives be seriously improved by the mass adoption of yet more technology?

The technical press is now reporting that 3-D display systems are becoming more available; for example, all Mitsubishi and Samsung rear Projection TVs built using the Texas Instruments DLP (Digital Light Processor) chipset are now "3-D enabled". Or, as is more correctly the case, if the source material you want to watch (broadcast TV, DVD, games, etc) is available as a 3-D transmission, these sets would be able to decode the extra data and allow you to see a 3-D image on the television set, although you would need to wear special glasses to see it. Viewers without the glasses would see the normal 2-D image and be blissfully unaware that anything different was going on in the background.

This is where I step in and say that although I evangelise the use of current and future technology whenever I can, I do this where I see a clear reason to do so and a benefit to be gained from doing so. Change for change's sake is *not* a good mantra.

My personal view is that 3-D for personal consumer electronic use is for the most part a waste of time and the "need" for it – poor displays with inadequate dynamic range have been already addressed by the full availability of high definition television (HDTV) and multiple sources of material. (Let's not raise the matter of the demise of HD DVD against Blu-Ray just yet!)

A crucial problem is that there really is not much 3-D source material available today. However, I remain at heart skeptical of the whole matter, particularly with

regard to its use with consumer electronic devices and domestic TV. My home TV is now an HD plasma TV and the quality of the imagery when playing HD DVD discs is just mind-blowing. The rendition of colours and accuracy of detail is fantastic. I don't see how changing this to implement 3-D would improve my 'personal viewing experience' any further.

What is the point of 3-D vision in the first place?

In the real world all objects have three dimensions: height, width and depth. When we look at anything around us, provided we still have use of both eyes, we are receiving information into the eyes that is processed by the brain to interpret the various positions and relative sizes of the objects in our view. With each eye receiving a slightly different view because of the difference in position of the eyes in our head, the brain receives different inputs from each eye. The brain automatically processes that data and feeds the information back to parts of the body that might need it. For example, if you are lifting a hot cup of tea towards your mouth, your brain will process the series of images it receives as you watch the cup approaching your mouth and the data from this will be used to help guide your hand properly. Do it right, all is well, but do it wrongly and the results will be painful.

So, we use three-dimensional data in every day life. It stops us bumping into things and other people, and it allows us to enjoy a wide range of activities. Of course, if you lose one eye, you lose 3-D vision, but that doesn't destroy a person's quality of life totally, nor does it completely imprison anyone as a disability. Having monocular vision simply restricts activity and requires the brain to be retrained to work on a single vision input rather than two, and for the person involved to take much more care in activities that take place in their immediate vicinity. The brain automatically adapts to fewer depth cues.

Here is the nub of my argument: I *need* 3-D vision when I am handling activities that occur within what I would call my near-field personal space – generally within an arm's length all round. I need full height, width and depth data of objects (both static and moving) in this space to avoid personal injury. Beyond this near-field space and out to an arbitrary more distant space, which I will call my far-field personal space, which is probably about 5-10 metres away, 3-D is an advantage, but is not essential to my safety. Beyond this personal space limit and off to the far distance, 3-D doesn't particularly do anything for me.

Try this for a simple experiment to see what I mean.

Put one cup on a shelf about 300mm from you. Put a second cup on a wall about 10 metres away. Put a third cup on a fence about 30 metres away. Look at each of them with one eye open, then the other, then both. The impact of binocular vision (two eyes open giving you 3-D) is acute for the first cup, considerably lessened for the second and has next to no impact on the third.

Now consider what makes you "understand" the vision cues you are receiving from these real-world objects.

TO CREATE AN IMAGE THAT IS AS CLOSE AS POSSIBLE TO THE REAL WORLD FROM WHICH THE ORIGINAL SOURCE DATA HAS COME FROM, THE DISPLAY MUST SHOW A VERY WIDE DYNAMIC RANGE IN COLOUR AND BRIGHTNESS

They have a perceived height and width, and you see them relative to other items in your vision. Your experience lets you interpolate the relative sizes: a cup will appear much larger at 300mm than at 10 meters and larger at 10 than at 30 metres. Your brain automatically reacts to the data and assesses relative distances accordingly.

There is also the receipt of colour information and colour depth, or in other words, how many colour hues can you discern on an object. The eye is a passive receiver. It does not transmit signals like a bat's sonar system; it can only respond to incoming light reflected off the objects in the visual path. Therefore, the more colour information that is received, the more additional data there is for processing by the brain.

We can generally tell by the gradient of colours across an object what the three-dimensional shape of that object is. Here's a simple test: put a ball, a box and a waste paper basket in a large room at one end. Light them well with standard overhead white lighting or some similar arrangement. Stand close to them and see what shape they are. Now walk to the far end of the room, and see how well you can tell what shape they are – has the ball become a disc or is it still a ball? Is the waste paper basket still a basket shape or has it become a rectangular shape? I am willing to bet that if you try this, you will agree that your brain can still determine the ball shape of the ball and the basket shape of the waste paper basket. This is because the colour rendering of the objects allow our brain to interpret the information and "guess" what the shape is, even if we are too far away to see the object fully.

So, my point – at last I am getting to it – is that in the real world, we have excellent colour rendering, with colour resolution that is limited only by our individual visual capability, coupled with limitations based on the intensity and colour temperature of the ambient light. Try the above test in a darkened room and it might be just a bit more difficult.

You get what you pay for!

When trying to simulate the real world by presenting images on an electronic display, we run into real difficulties. An electronic display is a two-dimensional unit. It can only present electronic images constructed from a matrix of pixels that vary in colour and brightness, from which our brain must interpolate the necessary information to understand the content of the image. To create an image that is as close as possible to the real world from which the original source data has come from, the display must show a very wide dynamic range in colour and brightness.

This is where we run into the nasty world of commercial manufacturing costs. Information in an image (colour depth and brightness) requires digital data and processing data through a consumer device costs money. To get high quality colour rendering in a display will require at least 24-bit colour (8 bits of red, 8 bits of green and 8 bits of blue). To match the highest quality that can be achieved in source material would require even more. But, the electronics required to transmit, decode and distribute this much data costs money. A very large number of consumer

electronic devices – laptop computers, PDAs and even many domestic TVs – only have 6 bits of data per colour channel, so 18 bits of colour data altogether. These lower cost display devices simply do not have the dynamic range and cannot render the images of any object sufficiently well to accurately represent real world images.

That is why the TV image on a full 1080p HD screen looks so much better than the same image on a conventional TV, or even worse, on most laptop computers.

But there are "dangers" associated with 3-D too.

Many 3-D systems for gaming applications are based on stand-alone headmounted displays rather than accessories attached to the conventional TV set, and are designed to deliver an "immersive experience". In other words, when you use the system, your brain is fooled into thinking you really are in the location and the game you are playing is the real thing.

That's all very well and the gaming market is a booming multi-billion pound industry as a result of the increasing usage of these devices, but we need to remember that the brain is part of a complex biological system. When it processes data from the eyes, it also processes data it receives from your ears. This data is not just "sound", but also includes "virtual position". Real-time feedback of the responses of the ventricular canals in the ears helps the brain determine exactly what orientation your head is in compared to the rest of the world around it.

The danger comes when the "eyes" tell the brain that there is rapid motion taking place, based on visual input from the screen images being delivered to the brain, but the "ears" tell the brain that there is no rapid motion and, in fact, the head is still. This can lead to sensory disorientation, which has the wonderful name of "vestibular conflict", and has the common outcome of the viewer not only feeling nauseous, but very often actually throwing up. About 45% of the population will suffer from vestibular conflict when trying to watch 3-D action activities, particularly if the event is immersive.

There was a major project undertaken at Abertay University a while ago that needed to evaluate the general public's response to using 3-D displays to perform simple tasks. The length of the project had to be extended because half of the people taking part in the activities had to drop out – they just got too sick to be able to complete their tasks.

Chris Williams is Network Director at the UK Display & Lighting Knowledge Transfer Network (UKDL KTN)

PIC microcontrollers (MCUs) are used in a wide range of everyday products from washing machines, garage door openers and television remotes to industrial, automotive and medical products. While some designs such as Switch Mode Power Supplies (SMPS) are traditionally implemented using a purely analogue control scheme, these designs can benefit from the configurability and intelligence that can only be realised by adding a microcontroller.

NOTE: The tips 'n' tricks presented here assume a 3.3V supply. However, the techniques work equally well for other supply voltages with the appropriate modifications.

TIP 1: DRIVING HIGH SIDE FETS

In applications where high side N-channel FETs are to be driven, there are several means for generating an elevated driving voltage. One very simple method is to use a voltage doubling charge pump as shown in **Figure 1**.

Method 1:

The PIC MCUs CLKOUT pin toggles at 1/4 of the oscillator frequency. When CLKOUT is low, D1 is forward biased and conducts current, thereby charging CPUMP. After CLKOUT is high, D2 is forward biased, moving the charge to CFILTER. The result is a voltage equal to twice the VDD minus two diode drops. This can be used with a PWM or any other I/O pin that toggles.

In **Figure 2**, a standard FET driver is used to drive both the high and low side FETs by using the diode and capacitor arrangement.

Method 2:

The +5V is used for powering the microcontroller. Using this arrangement, the FET driver would have approximately 12 + (5 – VDIODE) – VDIODE volts as a supply and is able to drive both the high and low side FETs.

The circuit in Figure 2 works by charging C1 through D1 to (5V – VDIODE) while M2 is on, effectively connecting C1 to ground. When M2 turns off and M1 turns on, one side of C1 is now at 12V and the other side is at 12V + (5V –VDIODE). The D2 turns on and the voltage supplied to the FET driver is 12V + (5V – VDIODE) – VDIODE.

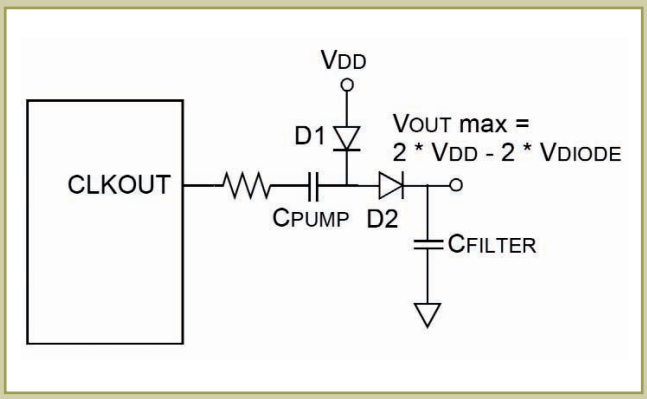

Figure 1: *Typical charge pump*

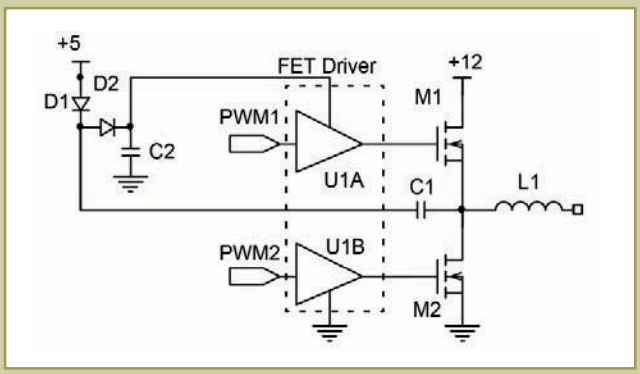

Figure 2: *Schematic*

TIP 2: GENERATING A REFERENCE VOLTAGE WITH A PWM OUTPUT

A PWM signal can be used to create a Digital-to-Analogue Converter (DAC) with only a few external components. Conversion of PWM waveforms to analogue signals involves the use of an analogue lowpass filter.

In order to eliminate unwanted harmonics caused by a PWM signal, the PWM frequency (FPWM) should be significantly higher than the bandwidth (FBW) of the desired analogue signal. **Equation 1** shows this relation.

$$F_{PWM} = K \cdot F_{BW}$$

Where harmonics decrease as K increases

R and C are chosen based on the following equation:

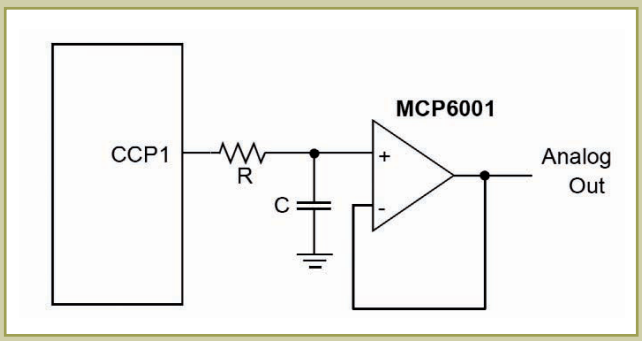

Figure 3: *Low-pass filter*

$$RC = 1/(2 \cdot \pi \cdot FBW)$$

Where harmonics decrease as K increases

Choose the R value based on drive capability and then calculate the required C value. The attenuation of the PWM frequency for a given RC filter is shown in **Equation 2** (above).

$$Att(dB) = -10 \cdot \log [1 + (2\pi \cdot FPWM \cdot RC)^2]$$

If the attenuation calculated in **Equation 3** is not sufficient, then K must be increased in Equation 2.

In order to sufficiently attenuate the harmonics, it may be necessary to use small capacitor values or large resistor values. Any current draw will affect the voltage across the capacitor. Adding an op-amp allows the analogue voltage to be buffered and because of this any current drawn will be supplied by the op-amp and not the filter capacitor.

TIP 3: USING AUTO-SHUTDOWN

CCP PWM AUTO-SHUTDOWN

Several of Microchip's PIC MCUs, such as the PIC16F684, PIC16F685 and PIC16F690, have a PWM auto-shutdown feature. When auto-shutdown is enabled, an event can terminate the current PWM pulse and prevent subsequent pulses, unless the event is cleared. The ECCP can be set up to automatically start generating pulses again once the event clears.

Figure 4 shows an example timing for the PWM auto-shutdown. When the shutdown event occurs, the current pulse is immediately terminated. In this example, the next two pulses are also terminated because the shutdown event had not been cleared by the beginning of the pulse period. After the event has cleared, pulses are allowed to resume, but only at the beginning of a pulse period.

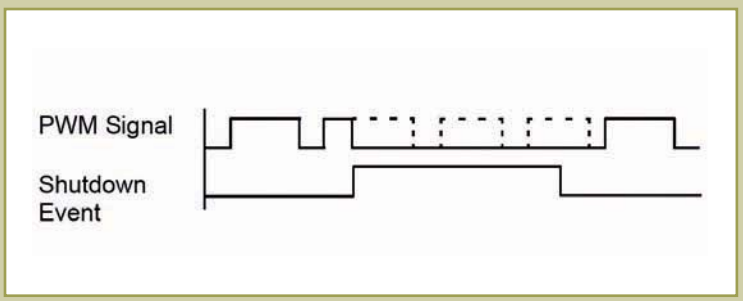

***Figure 4:** PWM auto-shutdown timing*

Using Auto-Shutdown to Create a Boost Supply

By using the auto-shutdown feature, a very simple SMPS can be created. **Figure 5** shows an example boost power supply.

This power supply configuration has several unique features:

1. The switching frequency is determined by the PWM frequency and, therefore, can be changed at any time.
2. The maximum on-time is determined by the PWM duty cycle and, therefore, can be changed any time. This provides a very easy way to implement soft-start.
3. On PIC MCUs that have a programmable reference module, the output voltage can be configured and changed at any time.

The topology can also be re-arranged to create other types of power supplies.

Example software is provided for the PIC16F685 (but can be adapted to any PIC MCU with the ECCP module). The software configures the PWM and comparator modules as shown in Figure 5. The software and referenced documents can be found on the Microchip Technology web site at **www.microchip.com.**

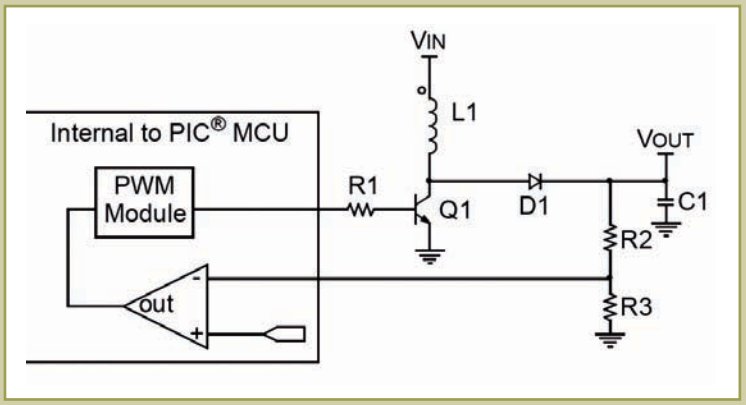

***Figure 5:** Boost power supply*

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TIP: USING BOOTSTRAP CELL CIRCUITS IN DC/DC CONVERTERS

By George Yu and Tom Gross, Power Applications Engineers, Linear Technology

Bootstrap circuits are widely used in DC/DC converters to serve as top side bias voltage supplies. **Figure 6** shows one typical bootstrap circuit for the LTC3728 high-side driver.

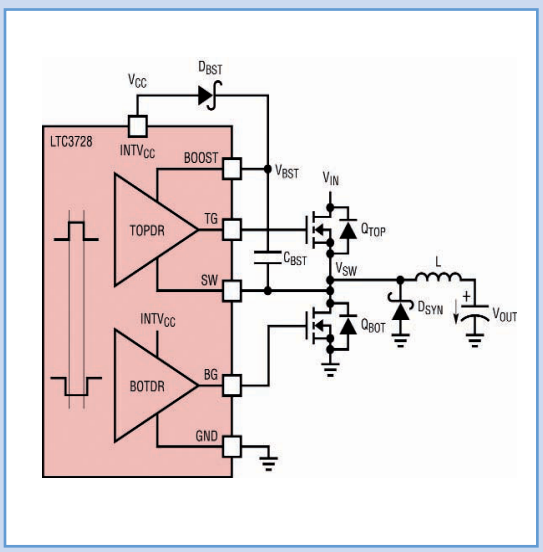


***Figure 6:** A typical bootstrap circuit for the LTC3728 synchronous buck high-side driver*

The bias voltage for the high-side driver is produced by the bootstrap supply circuit between the BOOST, INTVcc and SW pins. At the beginning of the initial cycle during start-up, the SW pin is at zero voltage. The bootstrap capacitor is charged up to $INTV_{CC}$ through diode D_{BST}.

When the high side PWM signal is enabled, the top MOSFET switch, $Q_{TOP,}$ is turned on and the SW pin will rise up to $V_{IN.}$ The BOOST pin voltage, $V_{BST,}$ will be V_{IN} + $INTV_{CC}$. When Q_{TOP} is switched off and the bottom side MOSFET switch, $Q_{BOT,}$ is turned on, the SW pin is pulled down to ground and bootstrap capacitor C_{BST} is recharged to $INTV_{CC}$ level.

When the switching frequency is sufficiently high, it can be guaranteed that the voltage across the bootstrap capacitor can be maintained at a level of $INTV_{CC}$ to ensure proper switching of the high side switch.

The bootstrap circuit in Figure 6 can be redrawn in **Figure 7a** to get a better understanding of the circuit. The bootstrap circuit can be divided into four required elements:

1. Dimming voltage source V_{DIM};
2. Bootstrap diode D_{BST};
3. Bootstrap capacitor C_{BST};
4. Charging voltage source V_S.

The dimming voltage source is a voltage source that will fluctuate between V_{DIM} and ground.

In Figure 1, a LTC3728 synchronous buck regulator application, the voltage at the switch node, V_{SW}, acts as the dimming voltage source. When Q_{TOP} is on, V_{DIM} is equal to the input voltage, V_{IN}, and when the Q_{BOT} is on, V_{DIM} is set to ground. The $INTV_{cc}$ serves as the charging voltage source V_S.

Figure 7b shows the typical waveforms on the switch node $V_{SW,}$ or V_{DIM}, and the bootstrap capacitor voltage, V_{BST}. The peak

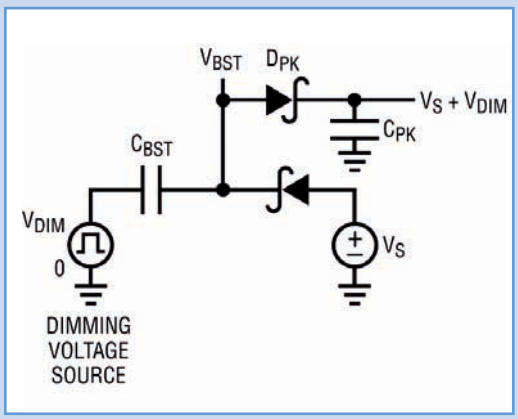


***Figure 7a:** Basic cell of bootstrap circuit*

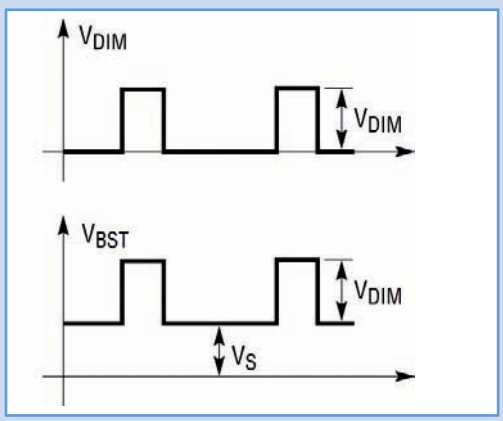


***Figure 7b:** Key waveforms of bootstrap circuit*

V_{dim} (dimming source)	V_s (charging source)	V_{bst}
V_{sw} (switch node)	INV_{CC}	$V_{in}+INV_{CC}$
V_{sw}	V_{in}	$V_{in}+V_{in}$
V_{sw}	V_{out}	$V_{in}+V_{out}$
V_{sw}	$V_{in}+INV_{CC}$	$2*V_{in}+INV_{CC}$ (fig. 3)
V_{out}	V_{out}	$V_{out}+V_{out}$ (fig. 4)

***Table 1:** The combinations of using a bootstrap circuit for the LTC3728 synchronous buck*

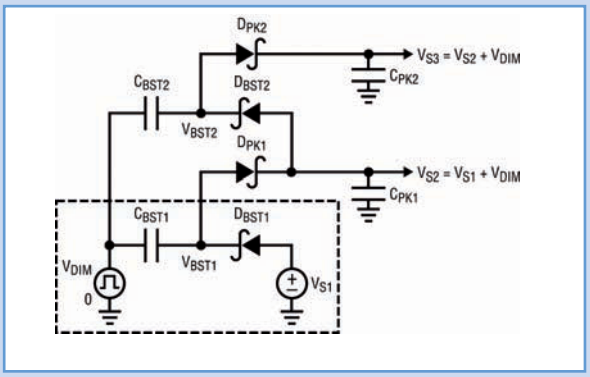


Figure 8: A voltage multiplier circuit based on basic bootstrap cell

voltage on bootstrap capacitor V_{BST} is the sum of V_{DIM} and V_S, or in the LTC3728 buck application example, $INTV_{CC}+V_{IN}$. By adding one more diode and capacitor, a peak detector circuit can provide a voltage source equal to V_S+V_{DIM}.

By using different sources for V_{DIM} and V_S, various DC voltages can be generated. **Table 1** shows some possible combinations that can be achieved by the LTC3728 synchronous buck regulator ckt.

Figure 8 shows a voltage multiplier circuit based on the basic boostrap cell and a simple peak detector circuit. Without considering the voltage drops on the boost diode, $D_{BST,}$ and the peak detector diode, D_{PK}, the voltage V_{S3}, will be $V_{S1} + 2V_{DIM}$; 2 being the number of stacked stages of the basic boostrap cell.

In general, a DC voltage of $V_{S1} + NV_{DIM}$ can be generated by a N number of stages of the basic boostrap cell and a peak detector circuit. Considering the LTC3728 application, a voltage of $INTV_{CC}$ + $2V_{IN}$ can be produced using two bootstrap cell stages.

Figure 9 shows the implementation of the varying voltage sources to generate a stable DC voltage. A dimming source switching from V_{OUT} to GND is formed by a switch, the VN2222LL, three diodes and two capacitors, and it creates an $EXTV_{CC}$ voltage source that is equal to twice the output voltage.

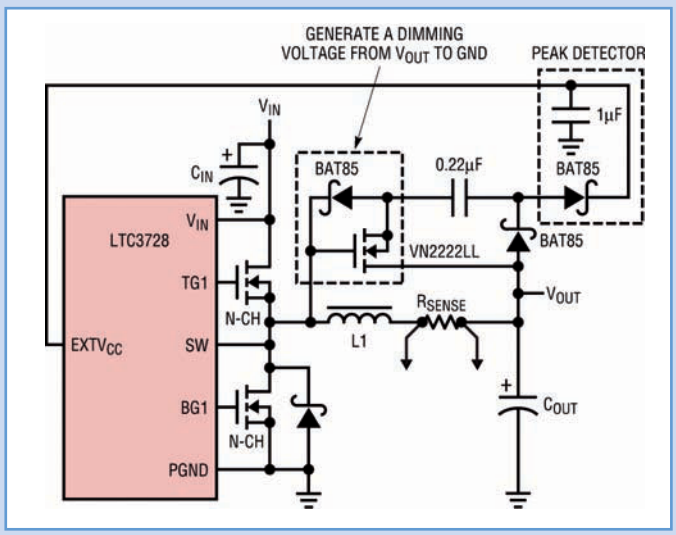


Figure 9: A capacitive charge pump circuit derived from a basic bootstrap cell

Win a Microchip PICDEM FS-USB Demonstration and Evaluation Board plus an MPLAB ICD2!

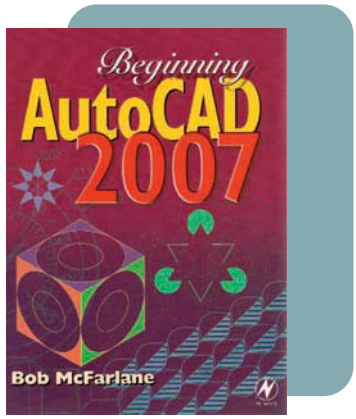
Electronics World is offering its readers the chance to win a PICDEM FS-USB demonstration and evaluation board and an MPLAB ICD2.

The PICDEM FS-USB is a demonstration and evaluation board for the PIC18F4550 family of Flash microcontrollers with full speed USB 2.0 interface. The board contains a PIC18F4550 microcontroller in a 44-pin TQFP package, representing the superset of the entire family of devices offering the following features:
48MHz maximum operating speed (12 MIPS), 32Kbytes of Enhanced Flash memory, 2Kbytes of RAM (of which 1 Kbyte dual port), 256bytes of data EEPROM, Full Speed USB 2.0 interface (capable of 12Mbit/s data tranfers), including FS-USB transceiver and voltage regulator.
The demonstration board provides the following functions:
20MHz crystal, serial port connector/interface (for demonstration of migration from legacy applications), connection to the MPLAB ICD 2 In Circuit Debugger, voltage regulation, with the ability to switch from external power supply to USB bus supply, expansion connector, compatible with the PICtail daughter boards standard, temperature sensor TC77 (connected to the SPI bus), potentiometer (connected to RA0 input) for A/D conversion demonstrations, 2 LEDs for status display, 2 input switches, reset button
The board comes pre-loaded with a USB bootloader that demonstrates the Enhanced Flash memory capabilities of the device. The PIC18F4550 can be re-programmed in circuit without an external programmer.
A CD-ROM is also included in the kit which contains full documentation about the board, application notes and software libraries for support of the HID, CDC and custom classes. Microchip is also giving away a MPLAB ICD2 to use with the PICDEM FS-USB Demo Board.
For the chance to win these development kits, please log onto **www.microchip-comp.com/ew-fsusb08**

BEGINNING AUTOCAD 2007

BOB MCFARLANE

NEWNES



I currently use AutoCAD 2004, but have used various versions of AutoCAD over the years.

Never having being formally taught AutoCAD, the way that McFarlane has laid out the format for beginners and self-taught users is very friendly, easy to follow and understand.

The step by step guide and structured approach (i.e. "don't skip ahead"; "does this *before* you go ahead" etc) allow the user to clearly see what he/she has done. This assist the reader - me especially - to sink in the concept of what McFarlane is trying to explain.

The way McFarlane has laid out the print is good, and allows a person to clearly follow each step of a required process. I especially like the way he has included error examples and explanation for those particular errors.

When doing the examples, I found the method of explanation very useful, as, even though I have used AutoCAD for many years, it is brain-drain intensive trying to remember each and every option available for each command. (And yes, some can have many depths of options!). The additional exercises at the end of each chapter allowed you to proof what you had just read and practiced.

My only comment would be to have a dedicated section on commonly used icons, i.e. 'End of Line', or 'Centre of Circle', 'Mid Line' etc, for reference.

The book got rid of some of my bad habits, and showed me that using the command line should be used in conjunction with all the convenient shortcuts available. It also showed me some excellent tips on shortening the time it takes to draw some complex drawings.

I would recommend this book as a good teaching aid to school students too. For example, my eldest son is currently doing graphics in year 11 in school. He had a brief look at McFarlane's book and found that it cemented some of the concepts he had learned over the past few months into place. He now even assists his teacher in teaching the rest of his class thanks to this book.

I would also recommend this book to the experienced users to iron out some taunting questions they may have had over the years.

Happy drawing!

Peter Krause

THE BOOK GOT RID OF SOME OF MY BAD HABITS, AND SHOWED ME THAT USING THE COMMAND LINE SHOULD BE USED IN CONJUNCTION WITH ALL THE CONVENIENT SHORTCUTS AVAILABLE. IT ALSO SHOWED ME SOME EXCELLENT TIPS ON SHORTENING THE TIME IT TAKES TO DRAW SOME COMPLEX DRAWINGS

KISS 4U Server with 775 Embedded Socket

With a 64-bit multi-core performance and ultra quiet operation (<35dB), the Kontron KISS 4U KT965 is not only perfect for data-intensive applications, such as those found in test and measurement or industrial and medical image processing, but is also the ideal server for control rooms and engineering offices.

The KISS 4U industrial server is based on the Intel Q965 chipset with up to 1066MHz front side bus and the Intel ICH8 DO I/O controller hub. The Intel LGA 775 socket provides scalable processor performance from the Intel Core2 Duo E4300 Embedded and Intel Core2 Duo E6400 Embedded processors up to the Intel Core2 Quad Q6x00 processor. Performance is boosted even further by up to 8 Gigabytes of DDR2 Dual-Channel RAM. 1x PCI Express x16 (PEG) and 6 x PCI interfaces offer plenty of options for application-specific expansions.

In terms of standard data interfaces, the Kontron KISS 4U industrial server offers 2 x Gigabit Ethernet, 10 x USB 2.0 ports (2 on the front) and 1 x COM. Data storage media are connected via 6 x SATA 150/300 with an onboard RAID 0/1/5/10 functionality and an ATA 100 interface.

www.kontron.com/KISS-4U

Certified Wireless USB Native Device Development Kit

Staccato Communications announced the availability of the Ripcord1 Development Kit (DVK). Staccato's Ripcord1 DVK is a completely integrated development environment that accelerates native Wireless USB device designs based on the Ripcord1 family of single-chip, all-CMOS Certified Wireless USB solutions.

At the core of the Ripcord1 DVK is the Ripcord Control Library (RCL). This fully abstracted software library provides services to simplify the interface to the Ripcord1 IC and enables easy integration on a wide variety of platforms.

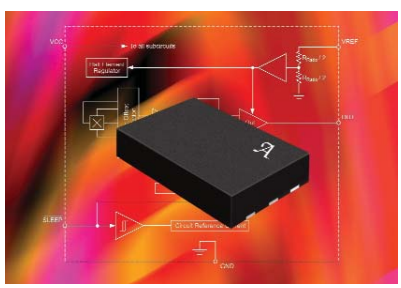
The software compatibility of the RCL with all of Staccato's Ripcord ICs allows for the seamless migration of designs that will work with the next-generation of devices on Staccato's product roadmap. The integration of the Ripcord Control Library in the development kit reduces overall design complexity in a variety of applications including mobile handsets, digital cameras, printers, portable media players, mass storage and wireless audio/video. Inherent benefits afforded by the Staccato's single-chip, all-CMOS solutions include low power, small form-factor and reduced system-cost.

The Ripcord1 DVK features an Xscale PXA270-based Single-Board Computer (SBC) running embedded Linux and allows developers to access and evaluate WiMedia MAC and PHY characteristics.

www.staccatocommunications.com

Micropower Linear Hall-Effect Sensors

The A139x family of linear Hall-effect sensor integrated circuits from Allegro MicroSystems Europe combines micropower operation, a tri-state output and a user-selectable 'sleep' mode.



The new sensor ICs provide a voltage output that is directly proportional to an applied magnetic field. The 'sleep' mode allows the devices to operate at a current consumption of less than 25µA, which contrasts with typical Hall-effect ICs whose sensitivity before amplification is directly proportional to the current flowing through the transducer element. As a result, it is difficult to achieve sufficient sensitivity levels with traditional Hall-effect sensor ICs without consuming more than 3mA of current.

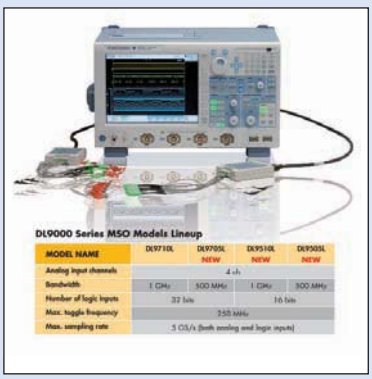
This low-current operation and the resulting power consumption of less than 10mW make these devices perfect for battery-operated applications such as mobile telephones, digital cameras, and portable tools. The operating voltage of 3 V makes them compatible with 2.5-3.5V supplies.

There are four devices in the family, differentiated only by sensitivity: A1391, 1.25mV/Gs; A1392, 2.5mV/Gs; A1393, 5mV/Gs and A1395, 10mV/Gs.

Despite the low power consumption of the circuitry in the A139x family, the features required to produce a highly accurate linear Hall-effect IC have not been compromised.

www.allegromicro.com

Three New Mixed-Signal Oscilloscope Models



Three new models have been added to the Yokogawa DL9000 Series of mixed-signal oscilloscopes (MSOs). The DL9705L, DL9510L and DL9505L complement the DL9710L model released in 2007.

The DL9705L is a 32-channel instrument with a bandwidth of 500MHz and a sampling rate of 5GS/s. The DL9510L has 16 channels, a bandwidth of 1GHz and a sampling rate of 5GS/s. Whereas the DL9505L has 16 channels, a bandwidth of 500MHz and a sampling rate of 5GS/s.

The DL9000 Series MSO models allow for simultaneous multi-channel monitoring of devices and electronic circuits that handle both digital and analogue signals. Together with the DL9710L (32 channels, 1GHz, 5GS/s), these new models give users more choice and enable them to select an instrument tailored to their application needs.

Unlike existing mixed-signal oscilloscope which offer limited display and analysis capabilities for logic signals, the Yokogawa MSO family is optimised for users who wish to analyse logic signals as well as analogue waveforms. The instruments feature the full state display and bus display functions typically found on logic analysers, allowing co-ordinated analysis of analogue and logic signals.

www.yokogawa.com

Raising Alarms and Protecting Equipment

Monitran has launched the VS0004, a complete condition monitoring and alarm module.

Fixed to a piece of plant machinery, the VS0004 can respond to a rise in vibration levels in a number of user-definable ways. The unit has two alarm levels, with the user able to set Alarm 1 between 1 and 50mm/s and with Alarm 2 capable of being set as a multiple of Alarm 1, either 1.5, 2, 3 or 5x. Also, the unit has a 4-20mA output scaled to Alarm 2 and, so, can be interfaced with PLCs or other control circuitry.

The VS0004 contains a double-pole double-throw relay for each Alarm Level and the user effectively wires to the normally open (NO) or normally closed (NC) contacts, depending on what action is to be taken when an alarm limit is reached. The switching capability of each relay is 8A at 240V AC or 30V DC.

The switch module also features a 10 second Alarm ON time constant and a 30 second start-up delay. The VS0004 is available with latching or non-latching indicators.

Sealed in a die-cast aluminium enclosure, the VS0004 weighs approximately 0.8kg and measures 80 x 125 x 82mm (depth, width and height, including connectors, respectively). Its frequency response is 5Hz-1kHz and its operational temperature range is -10 to 85ºC.

www.monitran.com

IECEx certification for Intrinsically Safe Vibration Sensors

Monitran has been awarded IECEx certification on all 18 of its intrinsically safe vibration sensors.

IECEx is an international standard under which a product's certification approves its suitability for use in hazardous atmospheres, where flammable liquids, vapours, gases or combustible dusts are likely to occur and risk fire or explosion through sparks or contact with hot surfaces.

These intrinsically safe vibration sensors are designed with the same performance as Monitran's standard range but with enhanced safety circuitry. They may be used in mining and underground environments (Group I) and petrochemical and dust environments (Group II). They are available with AC outputs for vibration analysis with portable or on-line analysers and DC outputs for connection to PLC and other control systems giving 24/7 monitoring and control of vital machinery.

All products are detailed in Monitran's General and Special Purpose Vibration Sensors guide.

In addition, Monitran already has the KOSHA (the Korean safety certification) certificate for its MTN/1185I sensor.

www.monitran.com

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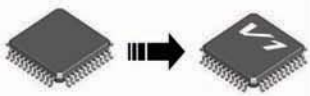

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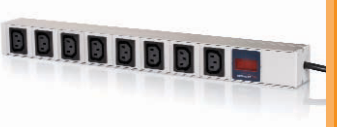
Infratec's SpeedUp Partnerprogramme

Infratec AG, a supplier of Rack Monitoring Systems for the control and management of EDP and telecommunication systems, has launched a new SpeedUp Partnerprogramme. The programme offers potentially lucrative conditions and services, but above all it offers the SMS Alarm System which controls both PCs and servers; for instance, in case of damage, an alarm is sent via SMS or via email.

The SpeedUp Partnerprogramme has three categories: Partner, Silver Partner and Gold Partner. Certification depends essentially on training courses relating to the products. In order to achieve the Silver Partner status, training on the Remote Monitoring System and on Power Monitoring Products is required. The Gold Partner status can be obtained once training on NMS 1000 software for general control is undertaken.

Competent Partners can give suitable advice to their clients and thus sell Infratec products.

Infratec range of products includes individual components and complete solutions for the range of KVM switches, KVM extender, cabinet monitors and even power distribution units and serial console servers.



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