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ELECTRONICS WORLD

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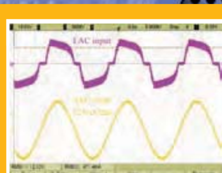
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

- SMART METERING ON THE CARDS FOR THE UK
- SHOULD SOFTWARE COME WITH IP CLEANLINESS CERTIFICATE?
- THE ROLE OF LASERS IN DISPLAYS MANUFACTURE

POE+ DESIGNS MADE EASY

WITH AN INDUSTRY-STANDARD PSE MODULE

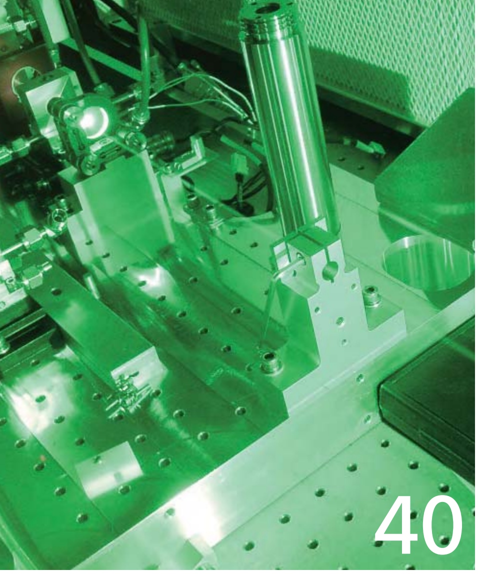
SPECIAL REPORT: DESIGNING WITH POWER IN MIND



TIPS 'N' TRICKS LED DRIVER POWERS HALOGEN REPLACEMENT

PRODUCTS LATEST SELECTION OF AVAILABLE PRODUCTS

ALSO IN THIS ISSUE: NEW COLUMN: "BUG-HUNTER'S LIFE"



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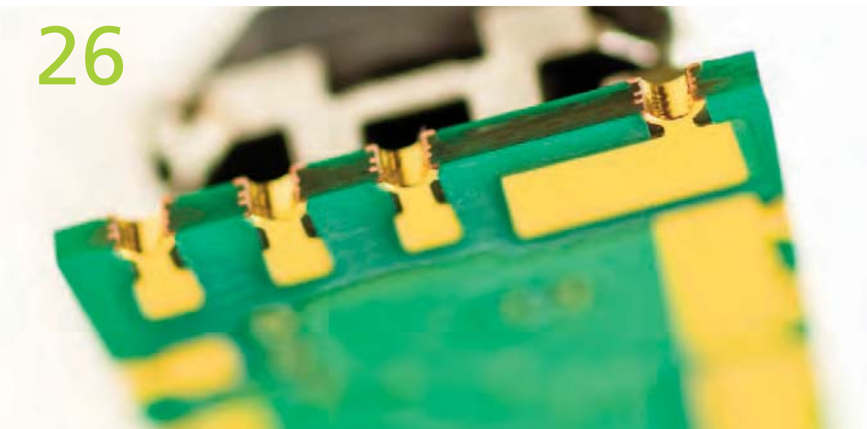

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REGULARS

FEATURES

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ELECTRONICS WORLD

EDITOR: Svetlana Josifovska
Email: svetlanaj@stjohnpatrick.com

PRODUCTION MANAGER: Tania King
Email: taniak@stjohnpatrick.com

DISPLAY SALES: Matthew Dawe
Tel: +44 (0) 20 7933 8999
Email: matthewd@stjohnpatrick.com

SALES DIRECTOR: Chris Cooke

PUBLISHER: John Owen

SUBSCRIPTIONS:
Saint John Patrick Publishers
c/o Circulation Data Services Ltd
The Coach House, Turners Drive
Thatcham, Berkshire, RG19 4QB
Tel: 01635 879361
Fax: 01635 868594
Email: electronicsworld@circdata.com

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End of an Era?

I am not sure if I should call it 'end of an era' or 'the beginning of a new one', as the government lays out plans to equip every home in the UK with smart utility meters by 2020.

Many will not be sorry to see the end of obsolete ways of reading old meter types (gas/electricity man going door-to-door) or the way they've been billed (largely by estimation) and charged (many questioned their overestimated charges).

Sensor and wireless technologies have advanced so much over the past decade, so it is surprising to have not seen the trend for smart metering appear sooner.

And the new era ushered by smart metering can only be a good thing: suppliers can remotely record customers' gas and electricity use, making the use of energy more transparent. In addition, smart metering could help reduce the UK's energy use, cut carbon emissions and save customers money. The savings come in the form of new meters being able to 'translate' the energy use into how much has been spent in 'exact' money, what that means in 'carbon footprint' terms, but will also come with an 'analysis' display unit, which will not only show how much energy has been used per day, but also compare this use either on a daily, weekly or monthly basis.

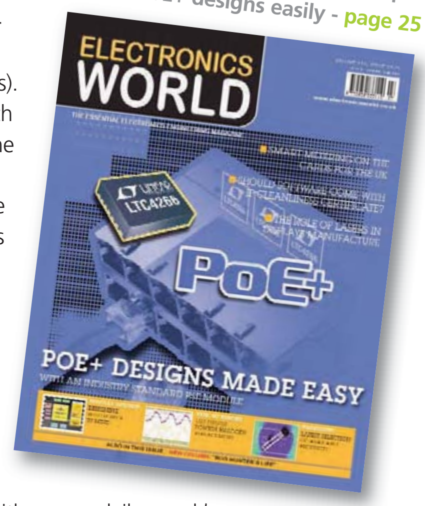
The meter would also be capable of providing information on which appliances are used the most, allowing companies to subsequently offer energy saving tips via the meter and its display device or introduce new tariffs to encourage off-peak energy use.

In addition, there's the 'fun' part to smart metering that will lead to different types of appliances being linked to communicate and cooperate inside the home, as well as with various utility providers and their electronic systems. Apart from benefits to consumers and environment, just think of the benefits this could bring to our industry – the smart metering technology is electronics and communications-based.

The installment of new meters in the UK is estimated to cost £7bn, but it'll be money well spent. It's good to see that the 'future' has arrived in this field!

Editor
Svetlana Josifovska

Linear Technology's modules help create PoE+ designs easily - page 25



■ Software integrity company Coverity announced the availability of its Integrity Center. The Center has been designed so that companies that want to reduce product failures and recalls caused by software problems can make software changes faster and with less risk, and can achieve breakthroughs in product innovation through highly efficient development.

"We live in a world where the integrity of your business and competitive advantage is directly dependent on the integrity of your software," said Seth Hallem, Coverity CEO. "The launch of Coverity Integrity Center enables customers to leverage the full power of all our software analysis capabilities."

■ Agilent Technologies and the University of Leeds have opened a new wireless communications laboratory at the School of Electronic and Electrical Engineering at the University. The lab will support teaching of undergraduate and postgraduate degree courses in broadband wireless networks, RFID and sensor networks. It is equipped with Agilent instruments.

"The University of Leeds has a world-class reputation in RF, microwave and wireless research, and it is a pleasure to be able to assist them in this way," said Ueli Nussbaumer, Agilent's European Business Manager.

Agilent equipment donation to the lab includes six Digital Modulation Workstations for generation and analysis of IQ modulated signals up to 3GHz; six RF network analysers; and vector signal generation and analysis instruments used to validate conformance to a wide range of modern digital communications standards.

SMART METERS ON THE CARDS FOR THE UK

The UK government plans a smart utility meter for every home in the country by the end of 2020, an effort that is touted to bring reductions in energy use, cuts in carbon emissions and savings to customers. Nearly 50 million meters will need to be fitted, at an expected cost of £7bn.

Smart meters use a combination of technologies to allow utility companies to remotely record customers' gas and electricity use, as well as let consumers see how much energy they are using.

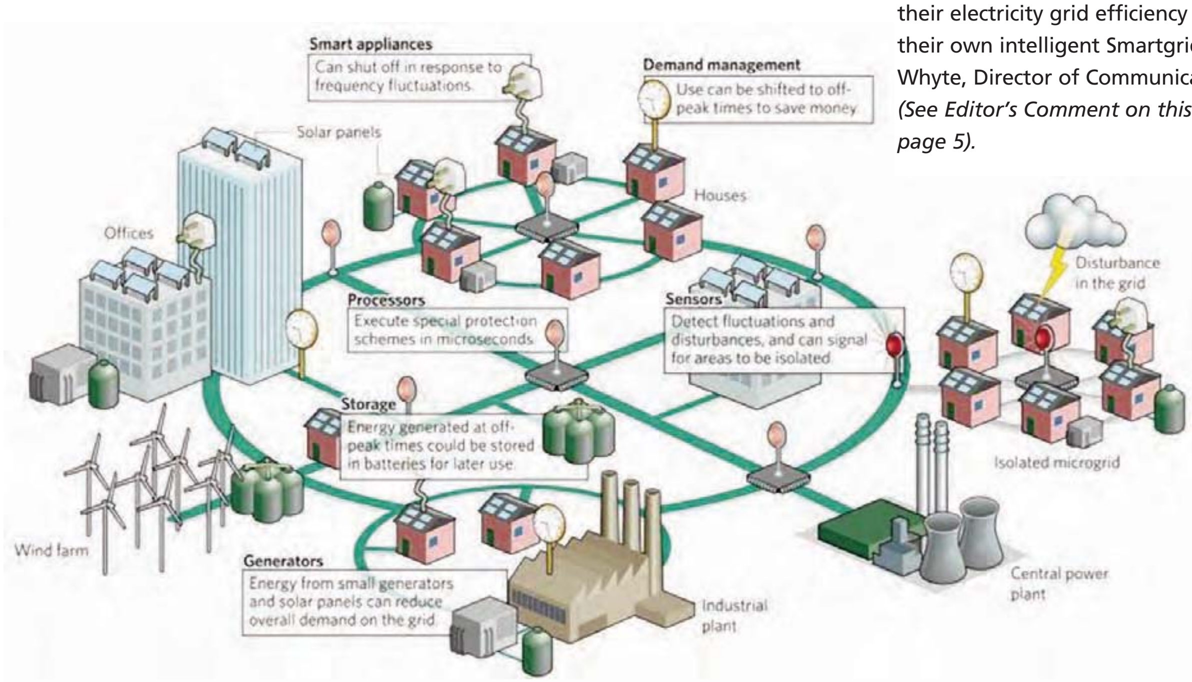
The UK government believes smart meters will help users reduce energy consumption by 2%, equating to £100m in cuts from bills by 2020. In addition, it expects a reduction in the country's C02 emissions by 2.6m tonnes.

Many have welcomed the rollout of smart meters in the UK, including Sentec, an energy management consultancy. Mark England, its managing director, said: "Smart metering is a key enabler in the government's push towards reducing carbon emissions in line with EU targets, and has the potential to transform the way we all produce, consume and pay for our energy: It would be difficult to underestimate the impact of the national rollout programme on the energy industry and its stakeholders."

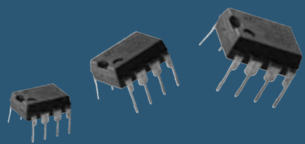
However, Sentec also believes that encouraging competition in this field now will take advantage of all that smart meters can offer.

"Smart meters are, in effect, a gateway to a huge range of possibilities, including increased micro-generation, greater use of renewables and a whole range of home management options. These opportunities will only be realised if sufficient room for competition and innovation is built into the market design," said England.

Asia and the US have already started deployment of the so-called Smartgrids. In the US, energy companies are looking into powerline technology as a reliable, stable and practical method to support the application of Smartgrids. According to DS2, a supplier of powerline technology, at this time it is critical to choose a technology that supports two-way digital communications as a cornerstone of future intelligent Smartgrids. "Intelligent Smartgrids will reduce energy companies' running costs by providing real-time network planning and management, avoiding outages, anticipating demand and even eliminating customer services time spent on dealing with estimated bills. Increasingly, utility companies across Europe and the US are realising the benefits that powerline technology can bring to improve their electricity grid efficiency and build their own intelligent Smartgrids," said Ann Whyte, Director of Communications at DS2. *(See Editor's Comment on this subject, on page 5).*



Smartgrid is a vision for the future – a network of integrated microgrids that can monitor and heal itself



ZEN AND THE ART

Vicky Larmour from Cambridge Consultants, with thanks to **Colin Clark** and **Andy Cleland**, goes on the ultimate bug hunt in software

ASK ANY software engineer about bugs and they'll have a story: the one that affected millions of customers but could not be reproduced by the developers, or the one that ground the entire system to a halt due to a single misplaced comma.

The vast majority of bugs are easily tracked down and fixed, but as systems get more advanced and complex, bug hunting becomes much more of a skill.

Through years of experience developing complex wireless embedded systems, we have refined these techniques to improve the efficiency of the debugging process. We hope they will be useful to others.

Structured debugging process: small, structured meetings can bring quick results

Understand the Problem

The first step must always be to understand the problem and reproduce the erroneous behaviour.

Bug reports are often vague or misleading, so ask for clarification if necessary. You need to understand:

- Exactly what is the erroneous behaviour?
- Is there a particular action that provokes the problem?
- Is it linked to a particular context or environment such as a busy network or high temperatures?
- If it has worked before, what has changed?

Once you have answers to these, you need to gather as much information from the system and its interfaces as possible. What data is going over the air or on the wire? What signals are on what pins, lines, or test pads on the board? Use scopes, sniffers and protocol analysers to capture raw data, control signals and timing information.

A debug build can provide extra checking and/or logging. Look at a known good case, as well as the problem case and identify differences.

Keep everything! At this stage you will be accumulating log files and test results. The golden rule is to keep everything.

As you try each test, record the details and note a test number; save all the test output into a folder named with the test number. Also save any special code builds or scripts used. Note the result in a summary table as you go.

Later, this summary will provide an overview of what has been tried: even if

OF BUG-HUNTING

each experiment in isolation doesn't help, a pattern may emerge. You still have the original raw logs to go back to if needed, and if you want to run a test again, perhaps collecting different outputs, you still have the code used for that particular test. When you have found the bug, you can go back to the summary and verify that it explains all the behaviour seen.

Strike the Right Balance of Trust

Don't necessarily trust source code comments or documentation. In an ideal world it will all be up to date and accurate, but in any case the code is definitive, so it is useful to learn to read it. Notice where the code and comments diverge – is there a cut-and-paste issue, or a change to fix an earlier bug which has introduced another bug?

On embedded devices or custom hardware in particular, don't necessarily trust the hardware. There may be individual board or connector issues, or a wider design issue; hardware datasheets may not be complete or accurate.

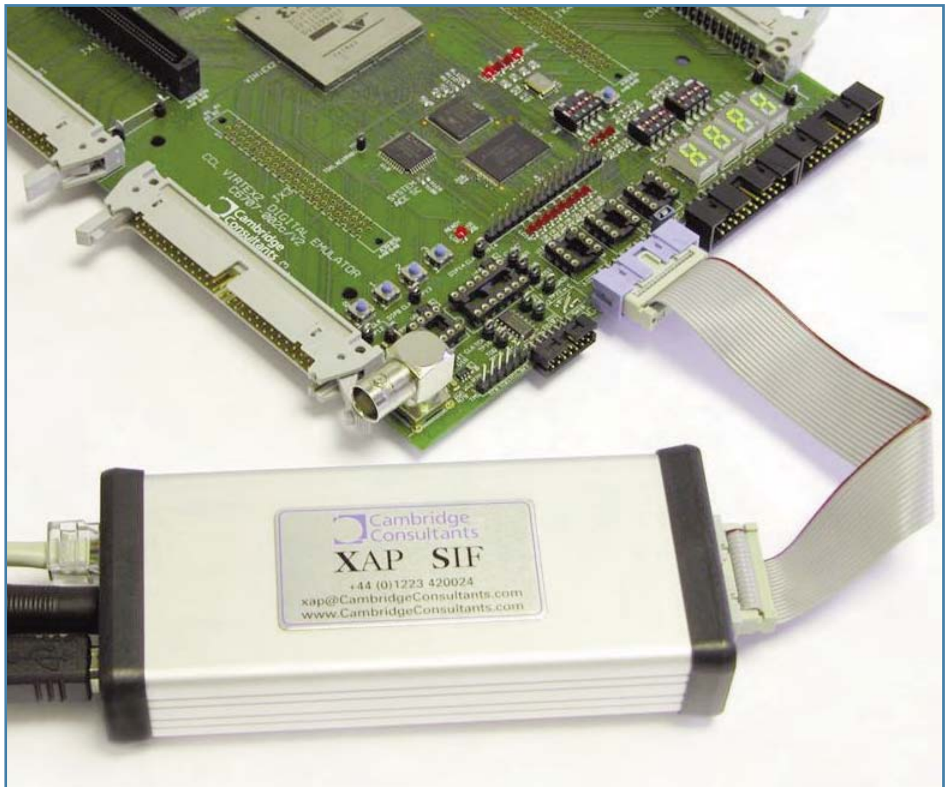
Don't necessarily trust the tools or build system. Rarely used or customised components will inevitably be less thoroughly tested, so focus on those first if there does seem to be a build issue.

Enabling compiler optimisation sometimes introduces bugs; testing with a lower optimisation level can be helpful.

This litany of "don't necessarily trust..." doesn't mean blame the problem on someone else – there's a balance to be struck! If you think the problem really is outside your control, try to prove it with a minimal test case, and follow the bug reporting guidelines mentioned earlier to give a clear problem report to the relevant person.

Common Problem Areas

Dynamic memory allocation is a potential source of many hard-to-trace bugs:



Prevention is better than cure: take the time to understand the platform's features and limitations

- Memory leaks (allocating a block and then failing to free it before all references to the block have been lost);
- Re-using freed memory (reading/writing a block that has already been freed, or attempting to free it again);
- Buffer overruns (reading/writing past the end of an allocated block).

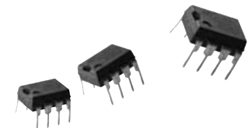
These lead to memory corruption and the symptoms can be wide ranging. Embedded systems often cannot afford the overhead of memory debugging features in normal use, though you may be able to turn them on (or add some) in your memory management library; for example guard blocks around allocated memory, tracking allocations and frees, or monitoring memory usage in real time or at set points in the code. Some debugging tools also provide watch-points to break execution when the data at a particular address changes.

Call stack overflow is another culprit that can cause just about any symptom. If the per-task stack of function calls, associated return addresses and context data becomes too large for the space allocated for it, you may get execution jumping to a random address or executing data rather than code. Many debugging tools allow you to monitor stack usage per task, to catch any overflows as they happen.

Timing issues can be caused by a software task not waiting long enough for a hardware event to occur, or by a race condition (if tasks or interrupt routines are not thread-safe, they may access the same data simultaneously). Check whether all shared data is properly mutex-protected, all state machines handle events out of the usual order and all hardware timings are respected. With timing issues the behaviour often changes when you turn on debug logging.

ON THE BUG HUNT

Turn debugging from a time-consuming chore into a structured process with reliable results



Structured Debugging Process

Sometimes a bug will be particularly hard to track down; you have several promising leads that come to nothing and in-house experts are stumped. The issue itself is complex, involving multiple software modules, and experiments present seemingly contradictory evidence.

It is tempting, especially for detail-oriented software engineers, to spend time collecting more and more detailed evidence. However, you run the risk of going vastly over schedule, demoralising yourself and still not finding the bug.

Set up a meeting, in a space with lots of whiteboards, for no more than eight people. Include engineers with experience in areas that relate to the bug, as well as at least one person who has not been involved in this bug or even the project.

1. The first stage is to agree on a single-sentence statement of the problem, aiming for clarity without getting bogged down in details. It may take five or ten minutes to achieve this. When everyone agrees, write it up on the board.
2. Next, state what is known about the problem. At this point you want only pure hard facts; write them up and encourage the group to challenge them (for example, "only occurs on revision G hardware" may be challenged by asking whether all other hardware revisions have been tested, and then revised to say "occurs on revision G, not E or F").
3. The third stage is speculation as to the cause. In line with general brainstorming techniques, as many ideas, theories and wild speculations as possible should be added to the board – no criticism or nay-saying allowed!
4. Finally, filter and prioritise the ideas. Some of the ideas might be testable with a very simple experiment; others might need more detailed investigation. Pick the top approaches according to what is considered the most likely culprit and what is easy to test, and divide up the relevant actions within the group.
5. Schedule a follow up meeting for the next day so everyone can report back, and repeat the process if necessary. In our experience of using this structured process, we have found that it brings results extremely quickly.

Fixing What You Have Found

If you've found the cause of a problem and the fix is "obvious", it doesn't necessarily make it right. For example, you've found a double free in one code path – is there another path that was relying on the free you've just removed?

Ideally, look at:

- All calls to the function you are changing, especially if it's used by several different subsystems;
- Anything that uses data affected by your change;
- Anything you have a gut feel might be related (intuition is invaluable!).

Regression testing should cover not just the specific bug you've fixed but any other related functionality.

Prevention Is Better Than Cure

It's well known that the earlier a problem is caught, the less it costs to fix. So:

- Take the time to understand the platform's features, limitations, debugging facilities; read all documentation and talk to others who have used it.
- Provide a system for enabling debug support (assertions, logging etc) selectively.
- Handle memory/resource allocation failures coherently; propagate errors upwards until they can be handled, or panic if even the most basic operation can't continue.
- Run nightly builds and investigate any compiler warnings that are generated.
- Develop code defensively; use a coding standard to help with this.
- Keep comments up-to-date, accurate and informative.
- Code often evolves; if a module starts to feel too complicated, consider rewriting it from scratch, re-partitioning it or breaking it down further.
- Make use of memory allocation and stack usage monitoring tools during development.
- Monitor hardware signals; drivers may appear to work but monitoring can show up problems such as unhandled interrupts, marginal timings, or excessive retries.

I hope these ideas will help you turn debugging from a frustrating and time-consuming chore into a structured process leading to reliable results. ■

Cambridge Consultants is a technology and innovation company, renowned for its ability to solve technical problems and provide creative, practical solutions to business issues.
www.cambridgeconsultants.com


Myk Dormer

There's more in there than you **REALISE**

TO MOST USERS, a low power wireless module is considered as little more than a – sometimes rather temperamental – replacement for a wired data connection, which, for the most part, is true.

On the other hand, a closer inspection of the circuitry built into the module can yield dividends, as there are functions and possibilities inherent in these little components that even the manufacturers might not have considered.

Modern radio designs routinely include a small microcontroller, used to either format and code the data stream, control the PLL frequency synthesizer circuits (and other programmable circuit elements), or both. This is rarely a particularly powerful or capable unit, but to an innovative user it can be very helpful.

Low power radio applications frequently consist of control or monitoring tasks, requiring the radio data link to control peripheral devices, or accept inputs from external sensors. To do so, it is usual for the user to include a microcontroller in his product, connecting the external inputs and outputs to the wireless module.

If the module already has a microcontroller, why not make use of that instead? It is already mounted in the module, supplied with power and clock circuitry and connected intimately with the radio hardware and it always has a few of its pins linked to the module's user interface (as control, programming or frequency select signals).

So how is it possible to get access to this device? Firstly, it is necessary to get the assistance, or at least permission, of the module manufacturer. As a minimum, a description of the function of each of the module internal control signals will be needed, along with a general briefing on how to 'drive' the radio hardware. Some makers will be happy to provide either high-level function routines (for inclusion directly into your code) or examples of the assembler functions necessary, while others may prefer to analyze your requirement – and your algorithms – and write the necessary code themselves, as a semi-custom version.

Then, the module will need to be programmed with the new firmware. Often this is possible in-circuit, via the user interface pins, or by connecting via a 'bed of nails' jig to pads on the module (this facility is often included by the designers to do the updating of the internal firmware in production). In the worst case, the code may have to be included at the initial build stage, requiring more intervention from the manufacturer.

Lastly, testing is required. Obviously, full functional testing by the customer is necessary, but the module supplier will also need to conduct RF approval confirmation tests, to ensure the new code doesn't cause any unexpected radio misbehavior.

As can be seen, the process is far from trivial, but compared to the steps necessary if the application was written in a standard external processor, there is relatively little extra to be done; especially if the module manufacturer is willing to co-operate.

Results can be well worth the effort: a module that does exactly what the customer needs.

As always, test everything.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd ***www.radiometrix.com***

AIMING TO BE IN POLE POSITION

While the UK manufacturing sector battens down its hatches as the global downturn continues to wreak havoc on worldwide markets, **Hans de Haas**, CEO of Bianor, argues that there has never been a more important time to revise the supply chain strategy and keep a tighter rein on logistics

SOMEONE ONCE SAID that drastic times call for drastic measures and while these are certainly unprecedented economic times, now is not the time to make knee-jerk reactions but rather to take a considered approach to optimising supply chain processes and improving cost efficiencies.

According to a recent international study by Capgemini Consulting, the global financial crisis leads the list of most influencing factors for the supply chain agenda in 2009. In fact, almost two thirds (65%) of managers involved in the supply chain argue that the worldwide economic slowdown will be the biggest issue they face this year.

With the crunch continuing to sink its teeth into the global economy, the vast manufacturing powerhouses of the Far East are no longer the viable, cost effective, attractive option they once were. Outsourcing production to far-flung destinations such as China and India just cannot afford UK businesses the flexibility they require, particularly in these tough trading times when satisfying customer demand quickly and effectively is a must.

Looking closer to home and considering outsourcing options in Europe are a sure fire way for British firms to combat the cost and time impact of lengthy overseas inspections helping to cut down order lead times.

Despite making UK exports more competitive, the weak pound has so far failed to lift the fortunes of manufacturers as global demand stalls. With Poland firmly outside the eurozone, it represents a haven for British outsourcing.

EU enlargement has seen growing trade with new member countries in Central and Eastern Europe and as one of the most 'western-looking' of the former Eastern Block countries, Poland serves as a useful gateway to the East and West.

This year, the Polish economy is expected to outperform most of the emerging European economies and to make a quicker recovery. It looks set to fare better than its regional peers the Czech Republic and Hungary, which are forecast to contract by 2.1% and 3.4% respectively this year.

According to UK Trade & Investment (UKTI) in 2008, the UK retained its position as Poland's fourth largest trading partner and Poland remained the UK's largest export market in Central and Eastern Europe. UK exports to Poland in 2008 exceeded £2.9bn – some 24% up on the previous year. And 15% of Polish exports worth £ 4.2bn went to the UK with total value of trade amounting to £7.1bn, up 19% against 2007.

If the relative strength of the Polish economy compared to its other European counterparts is not convincing enough, the quality of the Polish workforce is a further key strength. Poland has one of the best-educated societies in Europe, with a highly-skilled, multi-lingual workforce and English widely spoken throughout the country.

Furthermore, Poland is hosting the European Football Championships in 2012, along with the Ukraine. Preparation for EURO 2012 is a huge long-term project for Poland, generating numerous opportunities across a number of sectors and triggering significant investment in the country's infrastructure.

The decision to eschew the Far East in favour of more local opportunities is complex and not an easy decision to make. In order to maintain competitiveness, businesses need to pay due consideration to the total acquisition cost, time constraints on staff and lead times and not just focus on the more cost-effective labour rates.

A European location provides many commercial benefits for businesses compared to more far-flung countries such as China, where site inspections can take up to two weeks when flights, jet lag, transfers to production centres and problems with communication are factored in. For example, a quality controller may visit a factory like Bianor in Eastern Poland in just one day at manageable costs compared to an extended trip and the high associated travel costs to Asia.

Quality of output, cost of production and time requirements to inspect and ship tend to represent the 'big three' for businesses seeking to outsource production. Considering working with businesses closer to your domestic market and partnering with near-by firms offers a real alternative in all three arenas allowing companies to reinvest time and save money that can be ploughed back into the business.

As a multitude of businesses put the brakes on advertising, recruitment and expansion plans in a bid to ride out the economic storm, it is vital that manufacturers resist the temptation to retreat into

OUTSOURCING PRODUCTION TO FAR-FLUNG DESTINATIONS SUCH AS CHINA AND INDIA CANNOT AFFORD UK BUSINESSES THE FLEXIBILITY THEY REQUIRE, PARTICULARLY IN THESE TOUGH TRADING TIMES WHEN SATISFYING CUSTOMER DEMAND QUICKLY AND EFFECTIVELY IS A MUST

a corner to lick their wounds and instead look at ways to buck the downward trend. It goes without saying that doing nothing is just not an option for manufacturers in the current economic climate.

The supply chain manager's challenge is to actualise cost reduction through innovation and optimised supply chain processes, in order to improve cost efficiency. This will result in a supply chain that provides a significant competitive advantage when the recession is over.

Hans de Haas is CEO of Bianor, an injection moulding company established in 1997 as a Polish-Dutch joint venture. Bianor specialises in the manufacture of household appliances for well-known companies such as Bosch-Siemens Hausgeräte, Senseo and Philips. ■

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Lonne Mays, systems and applications engineer for Freescale's Sensors and Analog Products Division, explains why battery charger design has to be application-specific

Advanced ICs Facilitate APPLICATION-SPECIFIC Configuration of Li-ion Battery Chargers

LITHIUM-ION BATTERIES are emerging as the power source of choice for advanced consumer portable applications. They are lightweight, have excellent energy-to-weight ratio, can be created in a wide variety of shapes and sizes, and have low self-discharge rates.

However, charging Li-ion batteries can be problematic. Over-current charging can cause cell over-heating and lead to safety issues, and over-voltage charging (even at a very low trickle current) can damage batteries and shorten their cycle life. Consequently, manufacturers of Li-ion and Lithium-polymer cells typically recommend that the target cell charging voltage be accurately maintained within ±50mV, and that charging currents be tightly controlled as they approach the specified maximum. In addition, if a cell has been allowed to deeply discharge, charging without first pre-conditioning it can cause damage and jeopardize battery safety.

Fortunately, advanced charger ICs are now available that address Li-ion chemistry's unique charging algorithms, as well as supporting application-specific tailoring of the charger's operating parameters.

Lithium-Ion Batteries – Evolving and Improving

Lithium-ion battery technology is still evolving and improving. This evolution and improvement includes the development of Lithium-ion polymer batteries, so-called because of their use of a dry plastic electrolyte laminated between anode and cathode layers.

Lithium-ion polymer batteries, also known as Li-polymer and Li-poly batteries, have a unique advantage over wet electrolyte Li-ion, in that the battery can be shaped into any form from wafer thin to form-factors taking advantage of irregular spaces available within portable devices like cell phones, laptops, PDAs and MP3 players and so on. Nevertheless, gel/wet cell Li-ion batteries are also gaining ground and finding application in the latest generation of cordless power tools, due to their exceptionally low internal resistance and ability to support the very high currents demanded by power tool applications.

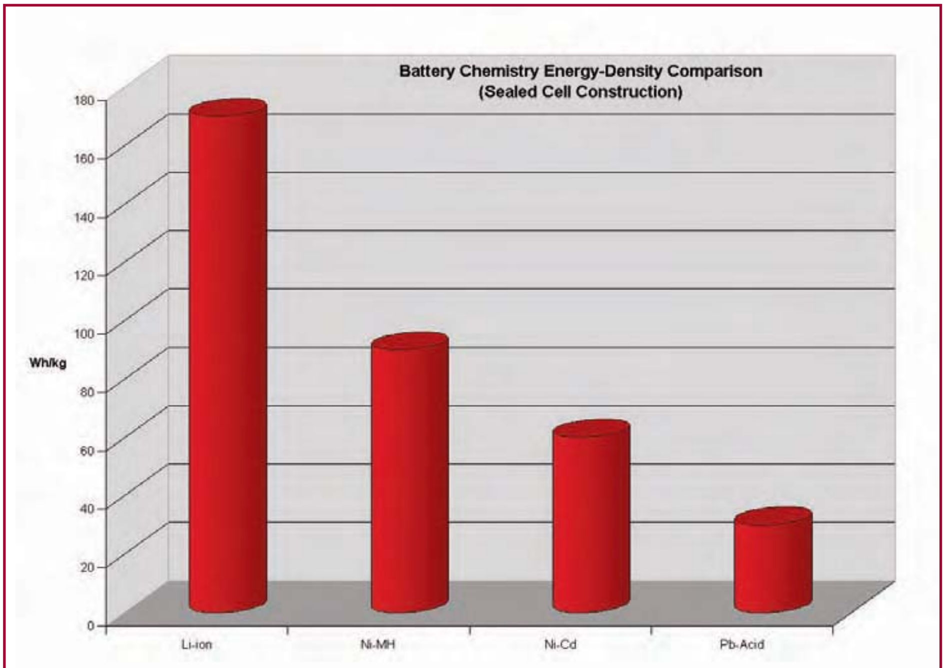


Figure 1: Cell chemistry energy-density comparison

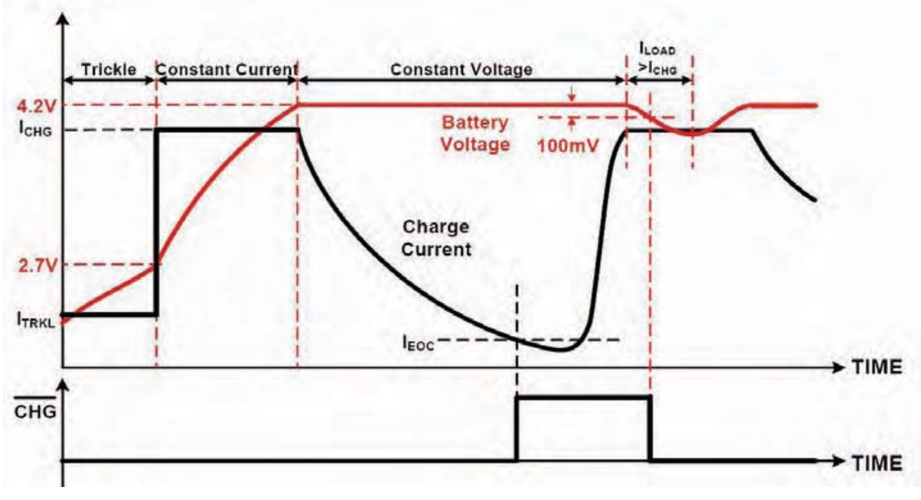


Figure 2: *A practical Li-ion/Li-polymer battery charging profile*

Li-ion/Li-polymer batteries are a significant improvement over competing rechargeable battery technologies in terms of their energy density. For a given battery size/weight this, of course, translates into longer use of the consumer appliance before recharging is required. The graph in **Figure 1** gives a general approximation of the different cell chemistries' relative energy densities.

Within the category of Li-ion/Li-polymer battery chemistry there are actually sub-sets of competing and evolving chemistries, primarily differing by the composition of the cathode. These presently include Cobalt-based cathodes, Manganese-based cathodes, Nickel-Cobalt-Manganese cathodes and Phosphate-based cathodes. All have the same basic cell voltage of the Lithium-ion chemistry, but vary in their charge/discharge rates, energy density and recharge cycle life. As well, there are differences in the construction of the electrolyte separator medium (e.g., wet/gel electrolyte in a porous medium, solid polymer electrolyte medium and semi-porous solid polymer electrolyte infused with gelled electrolyte).

Charging Algorithms

So what does a Li-ion/Li-polymer charge profile look like? In simplest terms, it can be graphed relative to time as a constant-current charging period followed by a constant-voltage charging period. In practice, the charger should also address the possible states of the cell, e.g. the possibility that the cell had been deeply discharged, or is already fully charged. **Figure 2** shows a practical charge profile.

Note that there are three distinct phases:

- Trickle Charge Phase – implemented when the cell voltage indicates a state of deep discharge. (Charging a deeply discharged cell with the normal charge current would result in damage to the battery and possibly cause unsafe overheating. Therefore the cell is pre-conditioned with a low "trickle current" before proceeding into the normal charge profile.) During this phase the cell voltage is allowed to float and is monitored while a predetermined trickle-value of constant-current is applied.
- Constant Current (CC) Phase – implemented when the cell voltage indicates that it is below a full charge but above a deep-discharge state. This is when the cell chemistry is able to absorb a maximum number of Coulombs in the ion exchange. During this phase the cell voltage is allowed to float and is monitored while a predetermined fast-charge value of constant-current is applied.
- Constant Voltage (CV) Phase – implemented when the cell voltage reaches a maximum predetermined value. Upon detecting that the cell voltage has risen to the predetermined maximum, the charging method is switched over to a regulated voltage (constant voltage) and the current is allowed to float. During this phase the cell chemistry is able to absorb ever fewer Coulombs and, consequently, the current decays until the charging circuitry detects the predetermined End-of-Charge (EOC) current, at which point the charging cycle can be terminated. Depending on the end application, it may be desirable to have the charge circuitry continue to provide a regulated output to power a load in parallel with the battery. In this case the battery voltage would be monitored and should the battery voltage drop 100mV, the charge circuitry would repeat the CC/CV phases.

Charger Design is Application-Specific

The charger must be designed for a specific application's battery and, therefore, has predetermined targets for the currents levels for trickle, CC and IEOC, as well as specific voltage thresholds for the CV charge phase and detecting a deeply discharged cell. The maximum time periods allowed for each phase of charging can also be specific to the particular application. A practical charger might also include the ability to detect a battery's temperature and prevent charging when the battery is either too cold or too hot to safely charge.

Another reason the charger design must be configured for the particular application, is to ensure the trickle charge current level compensates for the system's standby current with all the circuits powered by the battery. (If the trickle charge current is insufficient, all the trickle charge current from the charger will be absorbed by the system, leaving none to flow into the battery and the system will never be able to start up.)

The circuitry to address all these factors, although complex, can be contained in a single monolithic power management IC. **Figure 3** shows a block diagram representative of such an application specific integrated circuit (ASIC).

Advanced charging ICs like those from Freescale Semiconductor's MC3467X family of single-cell Li-ion battery charger devices address all of the requirements discussed here, including the ability to be configured for various applications. By means of a proprietary digital interface, Freescale is able to pre-configure certain parameters of the IC for the OEM customer prior to shipment. The designer's task is further simplified in space-restricted applications, because these devices are available in near chip-scale packages.

Other parameters can be tailored to the specific application by means of fixed external resistors, for example setting the CC mode current regulation point. Also available from this family are devices, such as the MC34674, that offer the designer the ability to control the charger in response to battery pack temperature via interface to an external NTC thermistor (see **Figure 4**). This would be a key feature for applications where the battery may be exposed to extreme outdoor temperatures, providing the means to prevent the battery cell from being charged when the electrolyte is too cold to charge without damage, or too hot to safely charge.

Emerging Power Source of Choice

In summary, as Lithium-ion/Li-polymer batteries emerge as the power source of choice for advanced consumer portable applications, the systems design engineer of those advanced portable consumer appliances can enhance system performance, improving run-time and battery life, by tailoring the charger parameters to the specific application's system requirements.

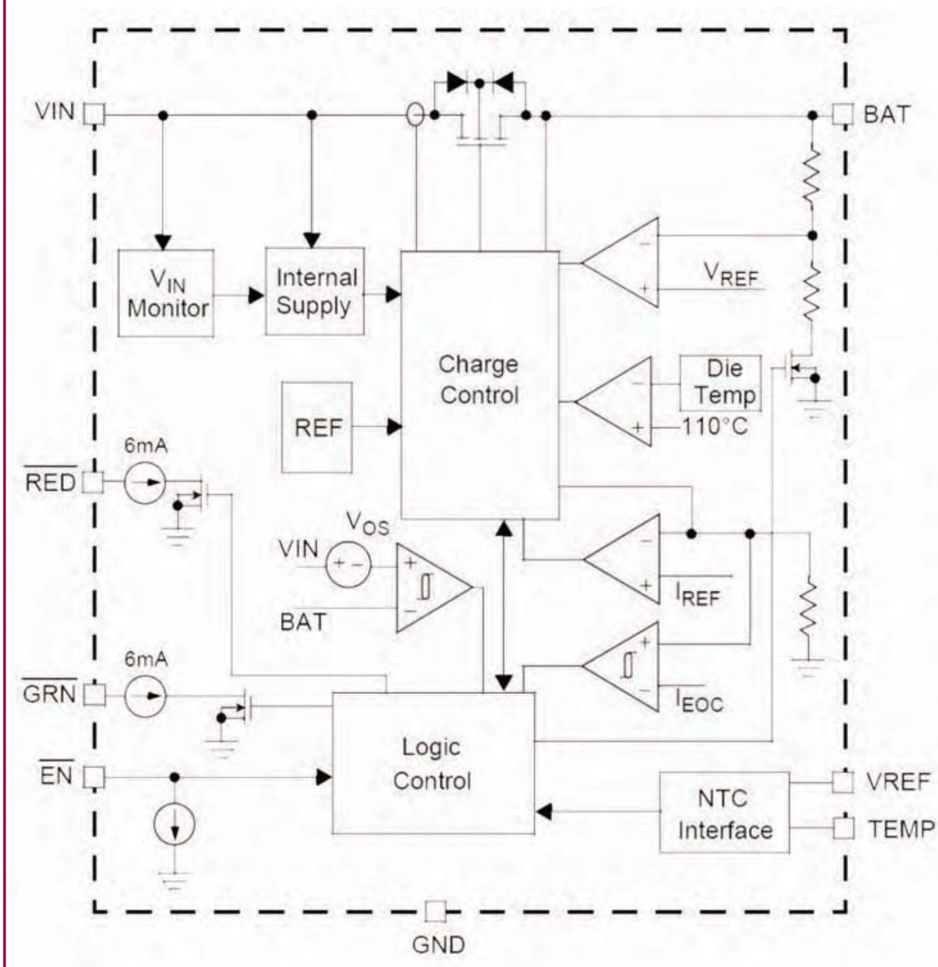


Figure 3: *Li-ion/Li-polymer battery charging IC block diagram*

Choosing a charger IC that can be easily configured and custom-tailored directly from the manufacturer will speed the product's time-to-market and help ensure the safety and performance of the product's battery system. ■

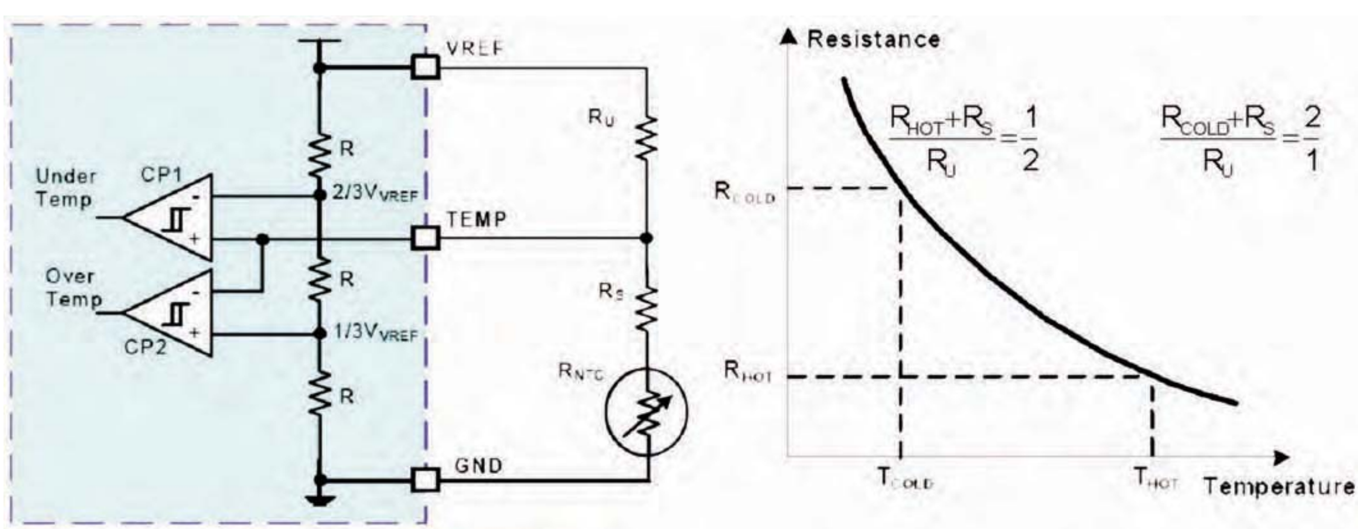


Figure 4: *NTC thermistor interface circuit*

Digital Signal Controllers are replacing analogue PWM controllers to bring new levels of flexibility and cost reductions for intelligent power supplies. Microchip Technology's **Bryan Kris** explains why

INTELLIGENT Power with Digital Feedback Loops

MARKET FACTORS are driving the development of intelligent power supplies that involve external control of the power supply and soft configuration in production. One way to achieve this is with digital feedback control of the power-conversion loop.

Power-supply designers have employed microcontrollers (MCUs) in intelligent power supplies for communications, monitoring, control and deterministic functions, such as power sequencing, soft start and topology control. However, until recently, complete digital control of the power-conversion loop has been impractical, due to the lack of suitable cost-effective technology. With the advent of Digital Signal Controllers (DSCs) that contain specialised peripherals, complete digital control is now practical.

DSCs Enable Digital Feedback Loop

There are so many inexpensive, dedicated analogue Pulse Width Modulation (PWM) controllers available, so why should designers opt for digital feedback control using DSCs?

DSCs provide the capability to implement new control methodologies and power-conversion topologies that are impractical or impossible with conventional analogue power-conversion controllers. The operating modes of voltage versus current, or continuous versus discontinuous, can be changed during operation, to meet changing input or load conditions.

Digital control loops implemented in DSCs can take advantage of Flash-based technology that permit systems to be configured and calibrated for different customers using standard platform designs, which reduces inventories, time to market and NRE costs.

Figure 1 shows a synchronous buck converter SMPS control system based on a typical DSC architecture that combines fast arithmetic operations and control peripherals, such as counter-based PWM modules, with analogue comparator-based feedback and coordinated ADC sampling.

Digital Feedback Loop Benefits

The digital nature of a DSC eliminates the thermal drift and much of the analogue component variations in a typical design, therefore design tolerances can be minimized, reducing the size and cost of components, such as transformers and inductors. If the product requires the design to become adaptive to changing environments, parameters in DSCs can be reprogrammed during run-time. This capability is impossible with analogue designs.

A single DSC can replace multiple analogue controllers, such as PFC and DC/DC, providing tight coordination among the power-conversion stages, or individual power control for multiple outputs. The ability to implement multiple independent power-control loops can provide tighter output regulation than is possible with conventional controllers.

The ability to implement multiple control loops also provides for very adaptable system designs. Consider a standard multi-phase buck converter, implemented with an analogue controller. The relationship between the phases is fixed by design, and the functionality is also fixed at a specific voltage. By implementing the same multi-phase buck converter with digital control loops in a DSC, the phase relationship can change on-the-fly to meet changing load conditions; phases can be disabled as the load drops, to reduce switching losses; and the remaining phases can continue to operate in continuous-current mode. This is comparable to modern V8 engine deactivating cylinders as the horsepower requirement drops.

Now, imagine the same digitally-controlled multi-phase buck converter. Another customer may not require 1.8 volts at 100 amps, but may instead need 4 outputs at, for example, 1.2V @ 20A, 1.8V@ 20A, 2.5V @ 15A and 3.3V @ 10A. The digital controller is easily adaptable to treating the PWM phases as related or independent. Updating the DSC's Flash memory with revised parameters can enable a basic power-conversion block to provide different functionality.

DSCs enable the power-supply designer to develop new power-conversion topologies and control strategies that are not possible with standard, off-the-shelf analogue PWM controllers, unless or until, an analogue device vendor designs and markets a controller specific to the design's specific requirements.

Analogue PWM controllers require resistors and multiple pins to set options; DSCs use code, making the chip smaller. Analogue PWMs only give you a few options, whilst DSCs can be completely reconfigured. Also, analogue PWMs are typically locked into one mode on power-up, but DSCs can reconfigure dynamically in response to changing conditions.

If a product requires the design to become adaptive to changing requirements, a DSC can be reprogrammed, whilst analogue-based designs need to resort to replacing the module. Through on-chip Flash, DSCs can enable a simplified power-supply production assembly line, allowing a single hardware design to be configured for customer voltage and/or current requirements. Power-supply trimming and calibration can be performed by programming the Flash memory, thereby eliminating trim pots or laser trimming of resistors.

Additional Digital-Control Benefits

With a DSC implementation of a digital

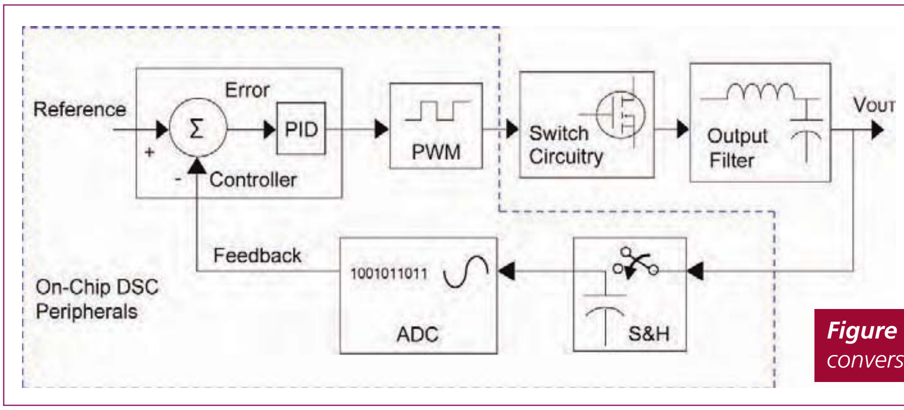


Figure 1: *Digital power-conversion system using a DSC*

power controller, many additional features can be added to a system without incurring additional cost.

If a design requires the coordination of multiple output voltages during start-up and shut-down, a DSC can provide this functionality at no added cost. By contrast, deploying analogue supply sequencing and tracking devices can be very expensive. During fault conditions, many products require the coordination of multiple output voltages. This is because if one output voltage experiences a fault, the other output voltages usually must be reduced or turned off to prevent the load circuitry (such as a motherboard) from experiencing a latch-up condition.

If the power-conversion process needs to be synchronised to external events or other devices, DSCs can provide this capability at no additional cost. Standard analogue PWM controllers which integrate this capability are significantly more expensive than 'jelly bean' analogue PWM controllers. DSCs can also be daisy-chained together to provide additional coordinated resources.

In certain applications, such as those in fan control and failure detection, and temperature monitoring, sensor information needs to be collated and monitored. A DSC can handle these additional tasks with processor resources not utilized by the digital control loops.

In telecommunications and other critical applications, the system power supply is typically implemented with multiple independent power modules that provide more total power capability than the system requires. This is done so that, if a particular power module fails, the remaining modules can continue to power the system. These collections of power modules are physically wired together, so it is imperative that each power module equally provides its fair share of the total power required. This is called load sharing. A DSC can implement load sharing at no added cost. Analogue load-sharing interface devices can cost more than many analogue PWM controllers.

Associated with load sharing is the hot-swap function. When a failure occurs in a power module within a load-sharing application, it is often desirable to enable a service technician to replace the defective power module with a new module while the system is operating. Hot-swap requires that the power modules are able to disable and enable themselves in an orderly manner, and control their behaviour as not to interfere with the operation of the other power modules. With analogue parts, implementing hot-swap capability can become very expensive.

If a system already requires a microprocessor for other tasks, a DSC may be capable of performing that task as well as controlling the power supply, thereby reducing component count and costs.

If a system requires error logging or communications capability, a DSC can provide this capability, which is not possible with an analogue controller. DSCs give power supply designers the ability to measure complex metrics, such as power and efficiency. DSCs can also use this information to help them adapt their response characteristics to any changing load conditions.

Another feature of digital-loop control is the potential to save time and money during the development of new products by eliminating the need for an expensive multi-layer board spin, because the fix can be made in software. The ability to load test-friendly software for board test, or the ability to make multiple custom products based on a single piece of hardware, can further reduce product development costs.

Digital Loop Control Considerations

There may be a learning curve for topics such as embedded systems design and MCU programming, especially for designers used to stand-alone analogue power solutions. Fortunately, there are software tools, reference designs and software libraries that can ease this transition. Choosing the correct DSC for the particular application is critical for the success of the design, and careful consideration of the required DSC features is an important step. A key factor to consider in DSC selection is to ensure that the on-board PWM module provides adequate resolution for the power-supply design. The resolution and speed of the ADC on-board a DSC provides the system with status, or feedback, to the control loop and should also have adequate resolution. Therefore, it is necessary to choose DSCs with on-board PWMs and ADCs suitable for power-supply applications.

Also, DSCs that offer analogue comparators, or ADCs, can continuously monitor signals and process the samples up to their mega-samples-per-second (MSPS) rating. However, this is a waste of processing power if the signal being monitored is just being compared to a fixed limit. On-board analogue comparators free the processor and ADC to perform other, more valuable, tasks while still allowing the DSC to support fast power-supply fault- and current-limiting functions.

The correct choice of a controller-centric

DSC such as that shown in **Figure 2** can ease the task of implementing the control algorithm. Often, digital control loops are implemented with a Proportional, Integral and Derivative (PID) algorithm. However, complex DSP programming skills are not needed to handle the DSP features of controller-centric DSCs.

Modern DSCs also provide supervisory functions, such as Watch-Dog Timers (WDTs), which can reset the system software and hardware in the event of a failure. WDTs enhance system reliability by enabling the digital-control system to recover, or at least enter a safe state.

Design Advantages

Here we discussed the advantages that a digital feedback loop brings to power-supply designers and their designs. Analogue PWM controllers are basically reactive devices, although a few have some limited feed-forward capability. This means that they can never provide optimal behavior under widely changing conditions.

In contrast, implementing a digital feedback loop in power supplies enables the designer to model the power-conversion process, as well as the load process. This offers advantages, such as increased reliability, reduced component count, better transient response, and the ability to change topologies and from single- to multi-phase on-the-fly. It also allows design customization toward the end of production through software rather than hardware. ■

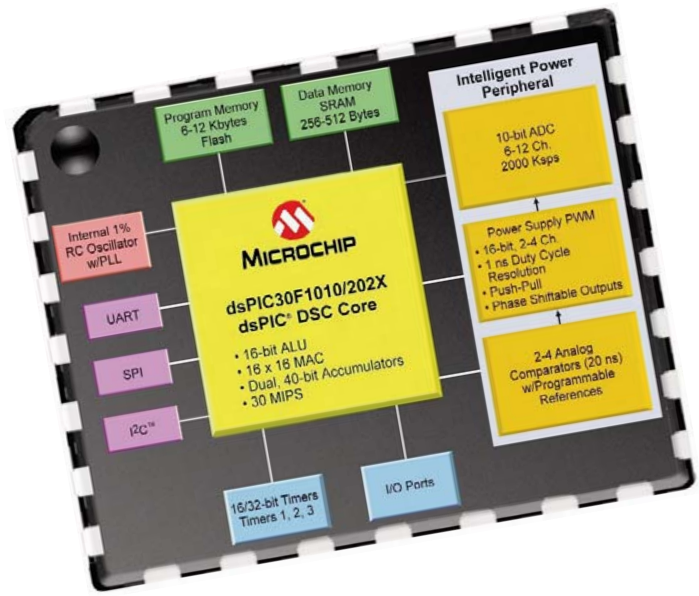


Figure 2: *Controller-centric DSCs with specialised peripherals, such as Microchip's dsPIC30F1010/202X, make digital control of the power-conversion loop practical*

Standardized PSE Module Simplifies Switch Design

The IEEE is close to completing the PoE+ (Power over Ethernet+) standard and network equipment makers are rushing to upgrade their designs. Making the transition can be challenging, so **Alison Steer**, product Marketing Manager in Mixed Signal Products of Linear Technology, discusses a new industry-standard PSE module that can make the job a lot easier

THE POWER OVER Ethernet (PoE) market has grown tremendously over the past few years. PoE has become almost ubiquitous, with millions of PoE-enabled switches installed all over the world.

The primary application of PoE is still to remotely power IP telephones and wireless access points. Engineers have dreamed of using PoE for many other applications, but too often these dreams have been frustrated by the small amount of available power. Under the original IEEE 802.3af standard, a Powered Device (PD) could only draw up to 12.95W.

The IEEE is about to improve the situation with the eagerly anticipated 802.3at revision (sometimes called PoE+) that is nearing completion. This latest revision will increase the power limit, allowing a PD to draw up to 25.5W, and will open the door to a host of high volume applications such as Pan-Zoom-Tilt (PZT) cameras, multimedia kiosks, industrial controllers and laptop battery chargers.

Going to PoE+

The challenge now is for Power Sourcing Equipment (PSE) manufacturers to get those high-power PoE+ ports into the field rapidly. High-power PDs won't become commonplace until high-power PSE ports are widely available.

Upgrading an existing PSE design for PoE+ requires:

- Improved Ethernet magnetics that can take more bias current without increased bit error rates at full gigabit line rate.
- New PSE controller chips with higher cutoff current thresholds.
- Depending on which controller chip is used, larger MOSFETs with larger Safe Operating Areas (SOA) may be needed.
- Larger main power supply.
- Miscellaneous components such as connectors, fuses, common-mode chokes, transient voltage suppressor diodes, current-sense resistors and EMI filters may need to be upgraded for higher currents.

These components are already available and vendors have tried to make their new PoE+ magnetics and chips simple drop-in replacements for 802.3af components as much as practical. But unfortunately, upgrading a PSE design for PoE+ will rarely be as simple as changing the bill of materials; usually, significant PCB layout changes are needed.

For example, designs that use discrete Ethernet magnetics may need layout changes. The traces that carry gigabit Ethernet data and power from the RJ45 connectors to the transformers must have controlled impedances, but also must be heavy enough to carry the increased current. Many existing designs use single-ended 50Ω traces on inner layers which are typically 6mils wide in 0.5oz copper; some designs use closely coupled differential traces where the widths are even narrower. While these layouts may have worked at 400mA for 802.3af, there could be a serious risk of overheating at 600mA for 802.3at. Therefore, a PoE+ switch may need to route these traces on the outer layers where 50Ω line widths are typically 8 to 10mils. What is more, surface layers are typically 1.5oz after plating.

But the list of headaches for the switch designer is even longer: the increased heat dissipation may require additional or stronger fans; the whole industry is under pressure to make network equipment more energy efficient; and the upgraded PSE design will have to repeat qualification and

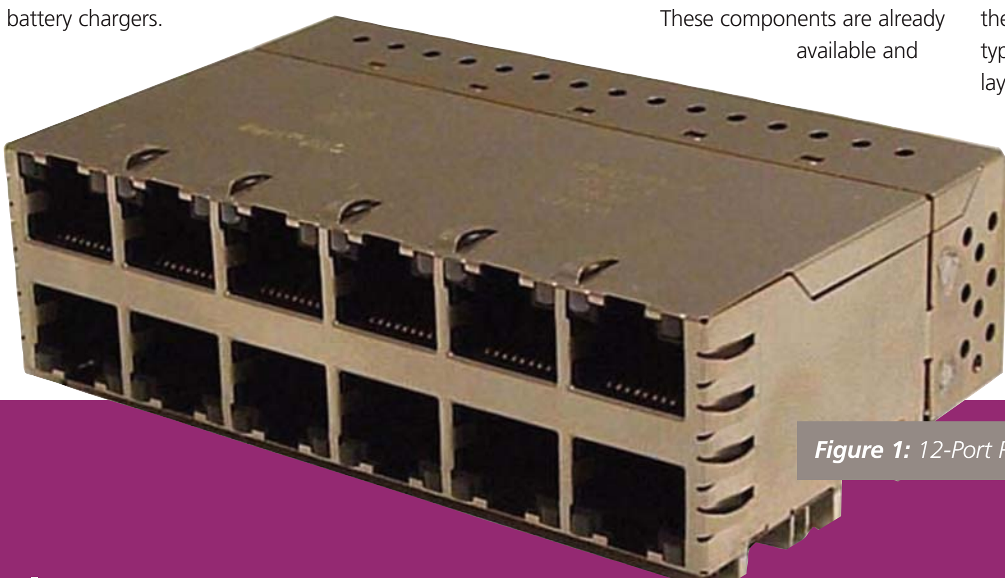


Figure 1: *12-Port PSE-ICM, courtesy of Tyco Electronics*

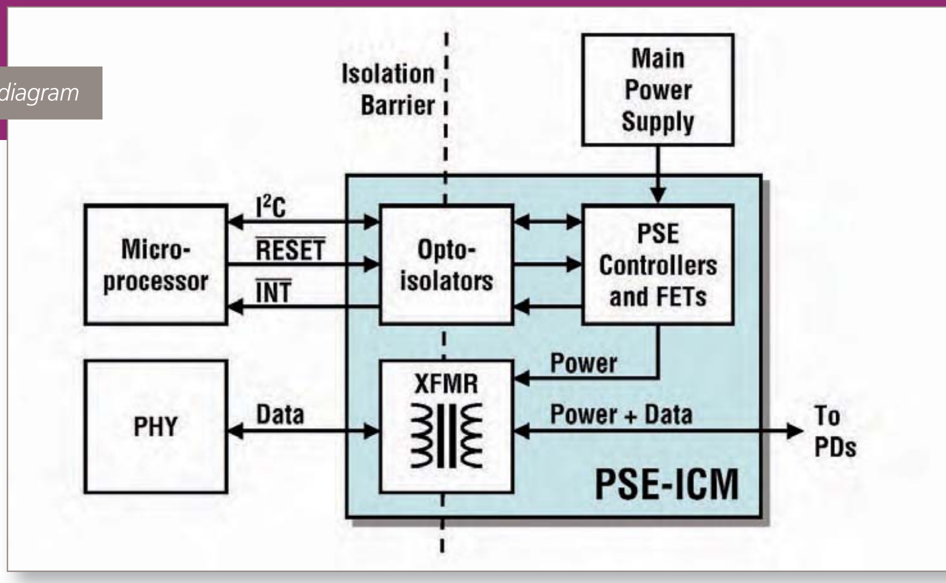


Figure 2: *Block diagram*

certification testing. All of the above mentioned tasks can put a significant burden on switch designers who, in many cases, are already overburdened.

Solutions

One solution is to use a multiport PSE module. There have been some module assemblies available for 802.3af PSE in the form of DIMM cards, or power supplies with PSE port circuitry built in. But these types of modules leave the designer some significant challenges because they don't include the Ethernet magnetics or RJ45 connectors. The Ethernet signals must be carefully routed from the connectors through the magnetics to the PHY chips, and power must be routed from the transformer centre-taps to the PSE port circuits. As mentioned before, this can be tricky: maintaining controlled impedances, maintaining clearances for high potential (hipot) and making the traces heavy enough to carry maximum current under worst-case thermal conditions is not trivial.

Probably the most elegant approach is to put all of the PSE circuitry and Ethernet magnetics inside a ganged connector assembly. This really simplifies the task of laying out a board, because all of the Ethernet signal pins are on the PHY side of the transformers; they don't carry DC currents, so you don't have to worry about the ohms-per-square of the traces, and you don't have to worry about maintaining clearances for hipot. Just route these signals directly to the PHY chips as normal impedance-controlled traces.

Some PSE modules like this have been available for 802.3af switches, but one of their main drawbacks has been a lack of standardization. Each vendor has a specific footprint and electrical characteristics. Once you pick a vendor you're locked into its design.

But that's changed now, thanks to PoETec. PoETec is a consortium of leading manufacturers of network equipment and components, dedicated to advancing and promoting PoE technology.

PoETec has developed and will soon publish a specification for the industry's first standardized PSE module, which it calls the PSE Integrated Connector Module (PSE-ICM). The specification defines all aspects of the PSE-ICM characteristics including footprint, signal functions and the internal register set. So a PSE design that uses one brand of PSE-ICM can simply drop in another brand without changing the board layout or the system software.

Figure 1 shows a 12-port PSE-ICM from one vendor. At the time of this writing, two PoETec member companies (Molex and Tyco Electronics) are shipping PSE-ICMs, and two more companies are about to start shipping. Presently, there are 12-port and 8-port PSE-ICMs available; 16-port PSE-ICMs may be coming in the near future. There are also versions with and without LEDs. Passive modules without the PSE circuitry, just the magnetics, are also available.

Figure 2 shows a simplified block diagram of a 12-port PSE-ICM. It includes an isolated I2C interface for control and monitoring of PSE functions. Also included, but not shown, are common-mode chokes and terminations. All that's needed is the main power supply and an external microprocessor to run the power management software. The PSE-ICM can also be configured for AUTO mode in which standalone operation is achieved. In this mode, the external microprocessor is not required.

The PSE-ICMs were made practical by some pretty advanced technology, and probably couldn't have been built at a reasonable cost just a year ago. One key enabling technology is the new LTC4266 quad PSE controller chip from Linear Technology. The LTC4266 has the smallest package (5x7mm QFN) and lowest power dissipation of any quad PSE controller in the industry: just 165mW/port at 600mA, including current-sense resistors and MOSFET on-resistance. The LTC4266 also has a unique non-linear foldback feature that protects the module from short circuit faults; without this feature, larger MOSFETs with bigger Safe Operating Area (SOA) would be needed to support the higher current levels reliably.

PSE-ICM Advantages

These days, switch designers face many tough engineering challenges. All of the digital and software tasks are difficult enough, without having to worry about analogue issues. For example, hipot, EMI, UL certification, lightning surge protection and heat dissipation are several areas where problems often crop up near the end of a project, when it's most costly and time-consuming to fix them. In fact, these are probably the most common reasons why products miss their launch dates.

The primary advantage of the PSE-ICM is that it's already been through all these tests. Therefore, it not only reduces the switch designer's workload, but also reduces the risks of last minute problems. Of course, it's still possible for a switch to fail hipot or EMI because of layout issues outside the PSE-ICM, but the chances of that happening are reduced.

The PSE-ICM also reduces risk because there are multiple sources. This not only creates price competition, but reduces the risk of late delivery that sometimes occurs when using sole sources for components.

Poor technical support can also lead to project delays and cost overruns. Suppose you're testing a new PSE prototype and one of the MOSFETs overheats. Was the failure due to a bad MOSFET or a bad controller chip? The two vendors will likely point their fingers at each other, while your project slips further behind schedule. But with the PSE-ICM there is no finger pointing; if one PSE-ICM brand seems unreliable, you can simply switch to one of the others with no changes to your board layout or software.

The Cost Issue

Of course cost is king in the network equipment industry. Some designers may take one look at the PSE-ICM and say it's too expensive, but a smart designer won't be so hasty. The real objective is to reduce overall costs; that's rarely as simple as picking the cheapest parts.

Figure 3 shows a qualitative cost comparison between a discrete design – where the designer places all the PSE components (controller chips, FETs, magnetics, etc) on the main board – and a design that uses the PSE-ICM. The graph is intended to illustrate three points:

1. The costs of both alternatives decrease over time.

2. There are sudden drops in cost when new technologies are introduced.

3. The material cost of the discrete approach will always be slightly lower.

Think about the second point. One of the advantages of the PSE-ICM is it allows you to more easily keep up with advancing technology and take advantage of the savings. For example, when a new chip that reduces cost is introduced, it may be difficult to use that chip in the discrete design because a new PCB layout would be needed. But when that chip is incorporated into a new PSE-ICM, you can just drop it on your board because the PSE-ICM footprint hasn't changed.

Now think about the third point. The discrete approach has a slightly lower material cost, but the PSE-ICM offers a lot of added value that makes up the difference. For example:

- Shorter time to market. Some products have market windows only 8 to 12 months before they're obsolete. If the launch of such a product were delayed just two months, due to PCB layout problems for example, then the overall revenue from that product would be severely reduced. The PSE-ICM can greatly reduce the risk of these delays and that has economic value that should be counted.

- Lower assembly and test costs. The PSE-ICM obviously reduces assembly cost, but its benefit of reducing test costs should not be overlooked. A designer who goes with the discrete approach must develop test setups and software sufficient to catch all the defects that might occur during the assembly process: at a minimum one would need to verify basic functions such as detection, classification and disconnect sensing. All these functions are pre-tested in the PSE-ICM; the only testing required would be to verify there are no bent pins or bad solder joints when the PSE-ICM is stuffed on the board. You get almost complete coverage just by running Ethernet traffic on all the ports and verifying the PSE-ICM acknowledges when it is addressed via the I2C bus.

- Lower configuration management costs. For example, PSE-ICMs are available without the PSE electronics in the same footprint. This means a switch maker can design two products (a PoE-enabled switch and a switch without PoE) that use the same main board; the only difference being which type of PSE-ICM is used.

POE+ Products Launches

As the new IEEE 802.3at standard nears completion, many companies are preparing to launch their new PoE+ products. In this environment, where designers have a long list of technical challenges and a wave of competing products is imminent, shortening the design cycle time can be critical for success.

The PSE-ICM can greatly reduce time to market, but offers many other advantages described here. The two main drawbacks of previous modules were lack of standardization and high cost, but both of these are addressed by the new PoETec industry standard: Multiple sources are already on line, with more coming. The new PSE-ICMs are already lower cost than their predecessors and, over time, competition and technological advances will drive costs down even further. ■

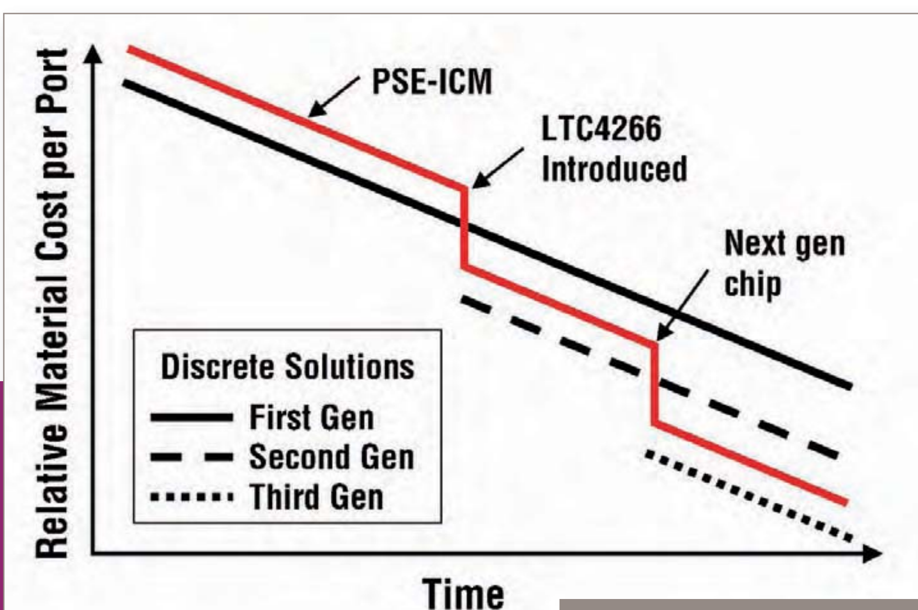


Figure 3: *PSE cost vs time*

Point-of-Load POWER MODULES Can Be More Beneficial Than Discrete Solutions

Henry Lee, Product Marketing Manager at Murata Power Solutions, argues the case for using PoL modules versus discrete solutions in the demanding high density circuit design

THE SEMICONDUCTOR industry continues to move to smaller geometries; there is a corresponding growth in the demand for lower voltage power converters. Linked to this, there is a growing trend in both the data communications and industrial markets toward the use of a distributed power architecture that utilizes either an AC to 12VDC power supply or one or more single output, isolated brick-type converters to distribute a 5V or 12V bus voltage. From this bus voltage, individual non-isolated Point-of-Load (PoL) converters take their feed.

Equipment designers now have more products and suppliers to choose from as they decide whether a discrete or modular solution is best for their power requirements.

The Shift in Power

The use of PoL modules has grown steadily over the past several years as there are now

Figure 1: *The Murata Power Solutions Okami OKL PoL DC/DC power converter*

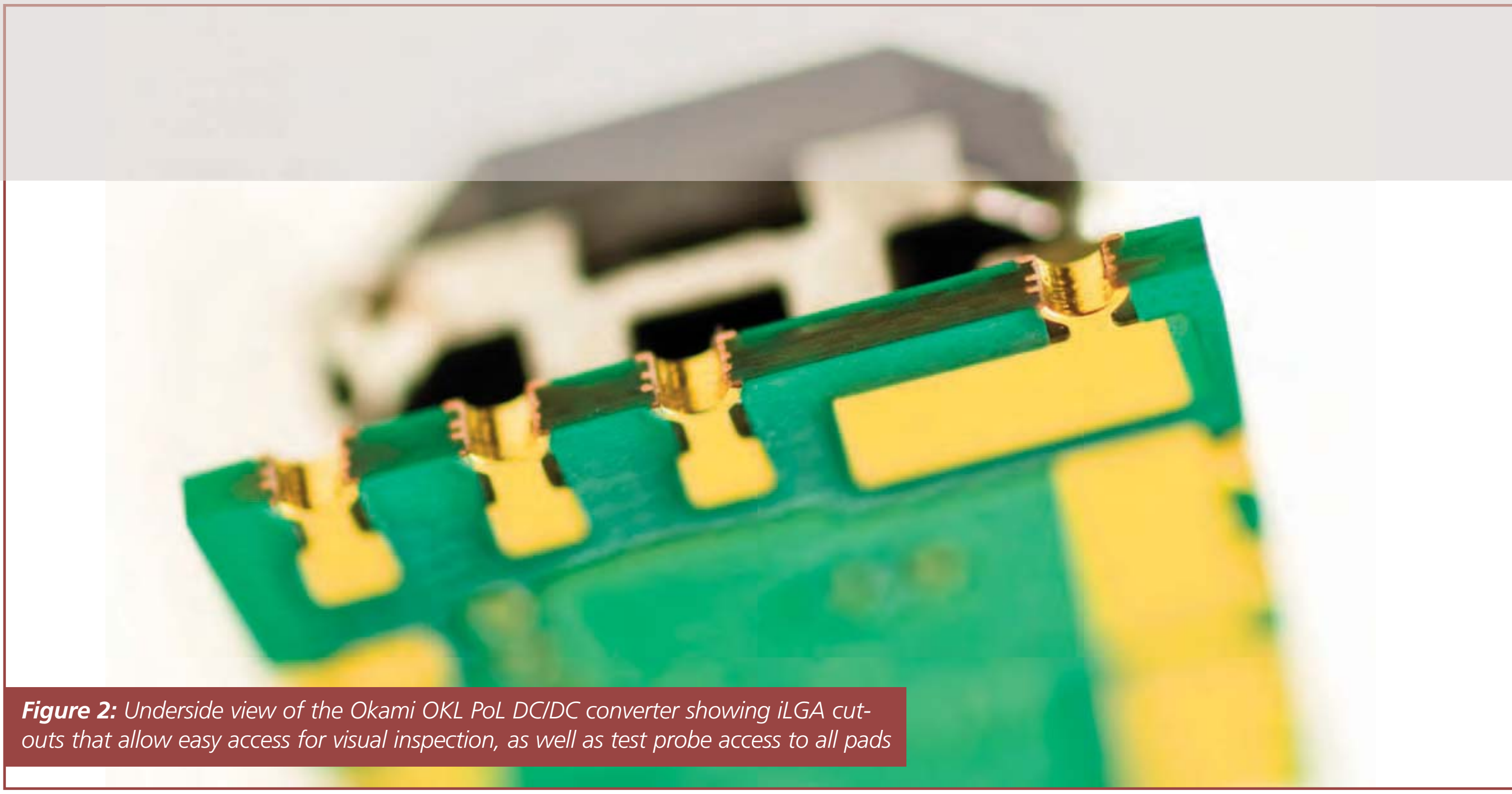


Figure 2: *Underside view of the Okami OKL PoL DC/DC converter showing iLGA cut-outs that allow easy access for visual inspection, as well as test probe access to all pads*

more suppliers who can offer industry-standard products that meet customers' power requirements at competitive prices.

There is more behind the transition in preferred approach from discrete to modular PoL power than just the increase in choice and availability. Today the ratio of analogue to digital engineering know-how within most companies designing and manufacturing electronic equipment is heavily weighted towards digital, even to the point where smaller businesses have no in-house power engineering 'specialists'. This situation has been reached due to the fact that digital has become the driving force behind the delivery of functionality in end products and power generally plays the supporting role – providing the power to allow digital components to perform their increasingly comprehensive set of tasks.

The growing availability of modular power has helped make the outsourcing of power design possible and has seen a shift in power knowledge and capability from OEM customers to power specialist suppliers, where experienced power experts are designing products with higher power conversion efficiencies in smaller form-factors.

Benefits of Discrete PoL Power

In order to maximize ease-of-implementation and offset sometimes limited power engineering knowledge within the customer's business, suppliers of the primary components within a discrete PoL power solution typically offer a schematic of the complete PoL circuit and a Bill of Materials (BOM).

This is, of course, a great help to the customer when acquiring the various parts and implementing the design on a PCB. Until recently the total cost of the individual components needed to achieve a discrete PoL solution was often less than that of a finished module. However, PoL module prices have become very competitive over the past few years. In addition to the board space savings they can bring, PoL modules can now be at par – or even lower cost – when looking at a straight BOM cost comparison to discrete solutions.

Ease of Use and Flexibility

Designing in a PoL power module is now as simple as the placement of an industry-standard modular pad layout; customers only need provide the appropriate physical space and interconnects on their PCB.

For a discrete approach the scenario is far more complex as the placement of the multiple components required can be challenging, depending on the size and shape of the space available on the board. In many cases a discrete approach requires the provision of more board area than a PoL module. This presents obvious issues for designers who are tasked with producing smaller equipment designs, leaving less room for the implementation of a power solution.

Power requirements can often change late in the system design. With a discrete design, the system board may need to be redesigned to accommodate an increase (or decrease) in system power requirements. With a PoL module solution, multiple power levels are often available within the same package outline and pinout, giving system designers the flexibility to easily accommodate such changes with a simple change of the supplier part number on the BOM as opposed to having to re-spin their PCB.

In high density circuits, where digital and analogue devices are often in close proximity, the issues of EMI/RFI and thermal management must also be carefully addressed. When implementing a discrete solution, these can be time consuming and problematic to overcome with the problem and the risk falling upon the equipment designer. With a PoL module, great consideration has been paid to the design, layout and construction of the module in order to minimise the effects of EMI/RFI on nearby components.

Industry Standard PoL Solutions

In the isolated and non-isolated PoL power sector the prevailing standard is the Distributed-power Open Standards Alliance (DOSA). DOSA was established by leading DC/DC converter manufacturers to ensure future product compatibility and standardisation within what was becoming an increasingly fragmented power converter market. The goal of the alliance is to establish standards over a broad range of power converter form-factors, footprints, feature sets and functionality to help drive product development and facilitate alternate product sources.

DOSA has been very effective in that it defines certain criteria that make second sourcing easily achievable whilst still giving a fast moving sector of the electronics market the freedom to evolve and meet the changing needs of the end applications. Murata's new Okami range of DOSA compliant, non-isolated PoL converters is a testament to this.

New Generation PoL Modules

Some examples of useful features seen on latest generation modules include wide range input voltages and programmable single output voltages that make selection and implementation into a customer application more straightforward. Efficiency levels, often in the region of 93%, plus high power densities that allow designers to implement a PoL solution in a remarkably small area with excellent thermal derating performance, add to the appeal of a PoL module.

A further consideration is that as the majority of components become available in surface mount (SMT) formats, it is advantageous for equipment designers to either eliminate through-hole components from their PCB designs or keep their use to a minimum. This enables the number of secondary PCB assembly processes to be kept to a minimum. In line with this, the latest PoL power modules are very often available in SMT, as well as more traditional formats such as single-inline packages (SIP).

In a further evolution of the SMT format, several of the Okami PoL DC/DCs utilize an innovative, inspectable land grid array package (known as iLGA). The conventional LGA interconnect package provides space savings and an excellent conduction path from the PoL module to the larger heat dissipating copper areas of the host PCB. However, they prevent easy visual inspection of the solder connection between module and PCB. To date, the only real way to overcome this was by expensive X-ray inspection methods or by destructive cross-sectioning to allow inspection of the solder joint. Murata developed the inspectable LGA (iLGA) package to overcome this problem. It features small, plated cut-outs (castellations) that allow easy access for visual inspection as well as test probe access to all pads.

Higher Value Add Enabled

Modular PoL power is becoming more accepted as a way to supply the power needs of devices such as ASICs, FPGAs, DSPs, microprocessors and communications ICs in a wide range of applications. With the emergence of standards such as DOSA, designers and buyers have the option to choose industry standard modular PoL solutions from multiple suppliers.

The PoL modules described herein offer system designers the potential to spend their time on higher value-add activities such increasing system functionality and performance. ■

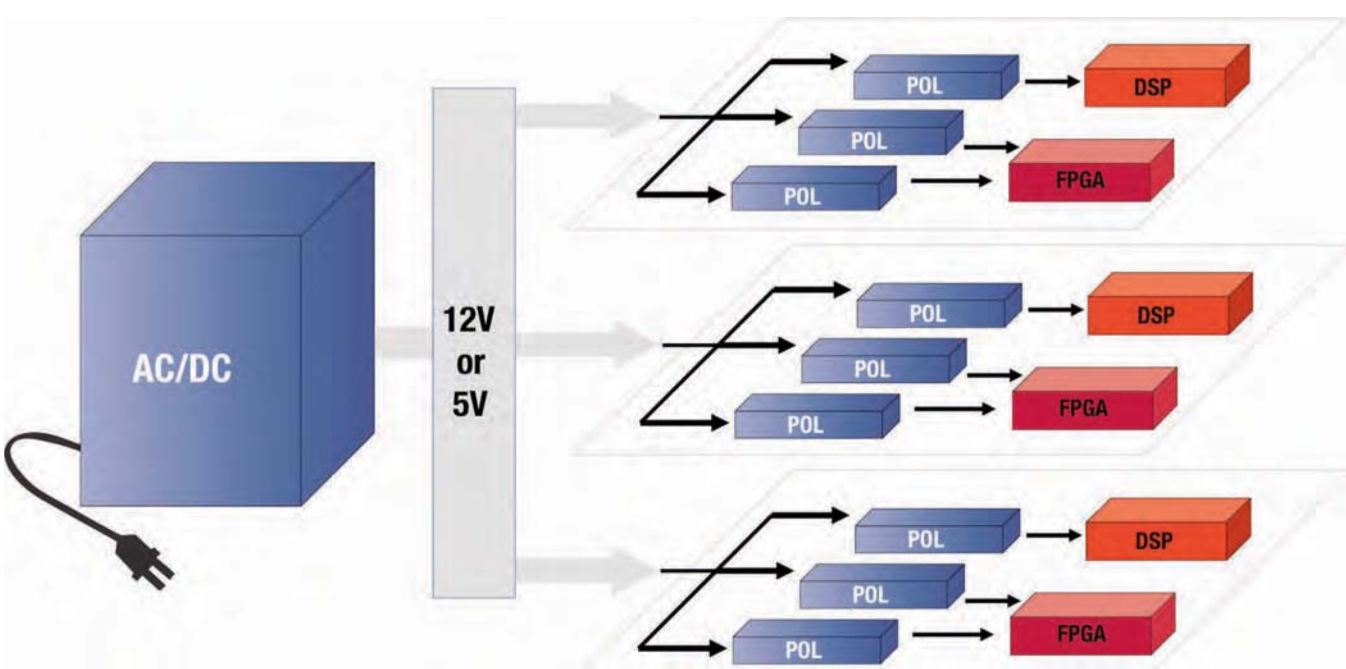


Figure 3: *Block diagram of a typical distributed power architecture*

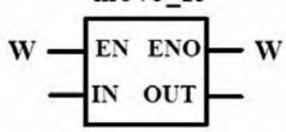
Associate Professor **Dr Murat Uzam** from Nigde University in Turkey presents a series of articles on a project that focuses on a microcontroller-based PLC. This is the ninth article in the series describing comparison macros

PLC with PIC16F648A Microcontroller – Part 9

IN THIS ARTICLE, the following are described: The contents of two registers (R1 and R2) are compared according to the following: GT (Greater Than – ">"), GE (Greater than or Equal to – "≥", in the article represented by ">="), EQ (EQual to – "="), LT (Less Than – "<"), LE (Less than or Equal to – "≤", in the article represented by "<="), NE (Not Equal to – "≠", in the article represented by "<>").

Similar comparison macros are also described for comparing the content of an 8-bit register (R) with an 8-bit constant (K). In addition two macros, namely "move_R" and "load_R", are described for data transfer.

The algorithm	Macro	Symbol

if EN = 1 then
OUT = IN;
ENO = 1;
else ENO = 0;
end if;
	`move_R macro in,out`
	`local L1`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw in`
	`movwf out`
	`movfw Temp_1`
	`L1`
	`endm`
		move_R
		
		IN, OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

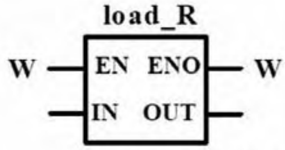
if EN = 1 then
OUT = IN;
ENO = 1;
else ENO = 0;
end if;
	`load_R macro in,out`
	`local L1`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movlw in`
	`movwf out`
	`movfw Temp_1`
	`L1`
	`endm`
		load_R
		
		IN (8 bit constant)
		OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

Table 1: *The macros "move_R" and "load_R", together with their algorithms and symbols*

Move and Load Macros

In a PLC, numbers are often required to be moved from one location to another; a timer preset value may be required to be changed according to plant conditions, or the result of some calculations may be used in another part of a program.

To satisfy this need for 8-bit variables, in UZAM_PLC we define the macro "move_R". Similarly, the macro "load_R" is also described to load an 8-bit number into an 8-bit variable. These macros are shown in **Table 1**, together with their algorithms and symbols.

In these macros, EN is a Boolean input variable taken into the macro through W, and ENO is a Boolean output variable sent out from the macro through W. Output ENO follows the input EN. This means that when EN=0, ENO is forced to be 0 and when EN=1, ENO is forced to be 1. This is especially useful if we want to carry out more than one move or load operations based on a single input condition. When EN=1, the macro "move_R" transfers the data from the 8-bit input variable IN, to

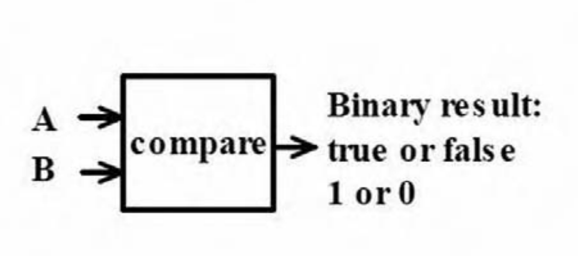


***Figure 1:** The generalized form of data comparison*

the 8-bit output variable OUT. Similarly, when EN=1, the macro "load_R" transfers the 8-bit constant data IN, within the 8-bit output variable OUT.

The file "mv_ld_mcr_def.inc" including the macros "move_R" and "load_R", can be downloaded from http://host.nigde.edu.tr/muzam/.

Comparison Macros

Numerical values often need to be compared in PLC programs; typical examples are a batch counter stating the required number of items that has been delivered, or alarm circuits indicating, for example, a temperature has gone above some safety level. These comparisons are performed by elements which have the generalized form of **Figure 1**, with two numerical inputs A and B corresponding to the values to be compared, and a Boolean (on/off) output which is true if the specified condition is met. The comparisons provided in this article are as follows:

A greater than B	**(A > B)**
A greater than or equal to B	**(A >= B)**
A equal to B	**(A = B)**
A less than B	**(A < B)**
A less than or equal to B	**(A <= B)**
A not equal to B	**(A <> B)**

where A and B are 8-bit numerical data.

In this article, two groups of comparison macros are described for UZAM_PLC. In the former, the contents of two registers (R1 and R2) are compared according to the following: GT (Greater Than – ">"), GE (Greater than or Equal to – ">="), EQ (EQual to – "="), LT (Less Than – "<"), LE (Less than or Equal to – "<="), NE (Not Equal to – "<>"). These six macros are shown in **Table 2**, together with their descriptions, algorithms and symbols.

In the latter, similar comparison macros are also described for comparing the contents of an 8-bit register (R) with an 8-bit constant (K). The six macros comparing the contents of an 8-bit register (R) with an 8-bit constant (K) are shown in **Table 3**, together with their descriptions, algorithms and symbols. The file "cmpr_mcr_def.inc" including the 16 comparison macros shown in Table 2 and Table 3 can be downloaded from http://host.nigde.edu.tr/muzam/.

Comparison Macros Examples

We will consider two examples, namely UZAM_plc_8i8o_exN.asm, N = 13, 14 to show the usage of comparison macros. In order to test the respected example please download the files from http://host.nigde.edu.tr/muzam/ and then open the UZAM_plc_8i8o_exN.asm program, N = 13, 14 by MPLAB IDE and compile it.

Following that, by using the PIC programmer software, take the compiled file "UZAM_PLC_8i8o_exN.hex" and with your PIC programmer hardware send it to the program memory of PIC16F648A microcontroller within the UZAM_PLC. After loading the "UZAM_PLC_8i8o _exN.hex", switch the 4PDT in "RUN" and the power switch in "ON" position. Finally, you are ready to test this program example.

To check the correctness of each program you are referred to the related information for each comparison function provided in Table 2 and Table 3. When studying these two examples, note that the input register I0 is made up of the 8 bits: I0.7, I0.6…I0.0 and that I0.7 is the most significant bit (MSB), while I0.0 is the least significant bit (LSB).

The first example program, "UZAM_plc_8i8o_ex13.asm" is shown in **Figure 2**. It shows the usage of all six comparison macros for comparing the contents of two registers as described in Table 2. The schematic and ladder diagrams of the user program of "UZAM_plc_8i8o_ex13.asm" shown in Figure 2 are depicted in **Figure 3a** and **3b**.

In the first rung, 8-bit numerical data "0Fh" is loaded to 8-bit variable M3, (for M3 you should go back to the second part of this article series), by using both the macros "move_R" and "load_R". This process is carried out only once at the first program scan by using the "FRSTSCN" NO contact.

In the rest of the PLC rungs, namely rungs 2, 3…7, we use six different comparison macros as described in Table 2 to compare the contents of two 8-bit variables M3 and I0. As we have M3 loaded with the numerical 8-bit data "0Fh" the outputs Q0.0, Q0.1…Q0.5 will be true or false based on the input data entered from the input bits I0.7, I0.6…I0.0.

The second example program, "UZAM_plc_8i8o_ex14.asm" is shown in **Figure 4**. It shows the usage of all six comparison macros for comparing the content of an 8-bit register (R) with an 8-bit constant (K) as described in Table 3. The schematic and ladder diagrams of the user program of "UZAM_plc_8i8o_ex14.asm" shown in Figure 4 are depicted in **Figure 5a** and **5b**.

There are six PLC rungs 1, 3…6, each of which is dedicated to one comparison macro of Table 3. In these macros, the 8-bit register (R) is I0 and the 8-bit constant (K) is "0Fh". As in the previous example, the PLC outputs Q0.0, Q0.1…Q0.5 will be true or false based on the input data entered from the input bits I0.7, I0.6…I0.0. (See the rest of the tables and figures on the next few pages). ■

Description	Macro	Ladder logic symbol	Schematic symbol and the algorithm

is the content of register **R1** **G**reater **T**han the content of register **R2**?	`R1_GT_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r1`
	`subwf r2,W`
	`skpnc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 > R2 ├ W	W – EN, R1, R2 [>] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 > R2 then Q = 1;
			else Q = 0;
			end if;

is the content of register **R1** **G**reater than or **E**qual to the content of register **R2**?	`R1_GE_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r2`
	`subwf r1,W`
	`skpc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 >= R2 ├ W	W – EN, R1, R2 [>=] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 >= R2 then Q = 1;
			else Q = 0;
			end if;

is the content of register **R1** **EQ**ual to the content of register **R2**?	`R1_EQ_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r1`
	`subwf r2,W`
	`skpz`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 = R2 ├ W	W – EN, R1, R2 [=] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 = R2 then Q = 1;
			else Q = 0;
			end if;

is the content of register **R1** **L**ess **T**han the content of register **R2**?	`R1_LT_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r2`
	`subwf r1,W`
	`skpnc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 < R2 ├ W	W – EN, R1, R2 [<] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 < R2 then Q = 1;
			else Q = 0;
			end if;

is the contents of register **R1** **L**ess than or **E**qual to the content of register **R2**?	`R1_LE_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r1`
	`subwf r2,W`
	`skpc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 <= R2 ├ W	W – EN, R1, R2 [<=] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 <= R2 then Q = 1;
			else Q = 0;
			end if;

is the content of register **R1** **N**ot **E**qual to the content of register **R2**?	`R1_NE_R2 macro r1,r2`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw r1`
	`subwf r2,W`
	`skpnz`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R1 <> R2 ├ W	W – EN, R1, R2 [<>] Q – W
			R1, R2 (8 bit register)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			
			if EN = 1 then
			if R1 ≠ R2 then Q = 1;
			else Q = 0;
			end if;

Table 2: *The comparison macros described for comparing the contents of two 8-bit registers R1 and R2, together with their descriptions, algorithms and symbols*

Description	Macro	Ladder logic symbol	Schematic symbol and the algorithm	Description	Macro	Ladder logic symbol	Schematic symbol and the algorithm

is the content of register **R** Greater Than the constant **K**?	`R_GT_K macro R,K`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw R`
	`sublw K`
	`skpnc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R > K ├ W	W — EN Q — W; R; K; >
			R (8 bit register)
			K (8 bit constant)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			if EN = 1 then
			if R > K then Q = 1;
			else Q = 0;
			end if;
				is the content of register **R** Less Than the constant **K**?	`R_LT_K macro R,K`
					`local L1,L2`
					`movwf Temp_1`
					`btfss Temp_1,0`
					`goto L1`
					`movlw K`
					`subwf R,W`
					`skpnc`
					`goto L1`
					`movlw D'1'`
					`goto L2`
					`L1 movlw D'0'`
					`L2`
					`endm`
						W ┤ R < K ├ W	W — EN Q — W; R; K; <
							R (8 bit register)
							K (8 bit constant)
							EN (through W) = 0 or 1
							Q (through W) = 0 or 1
							if EN = 1 then
							if R < K then Q = 1;
							else Q = 0;
							end if;

is the content of register **R** Greater than or Equal to the constant **K**?	`R_GE_K macro R,K`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movlw K`
	`subwf R,W`
	`skpc`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R >= K ├ W	W — EN Q — W; R; K; >=
			R (8 bit register)
			K (8 bit constant)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			if EN = 1 then
			if R >= K then Q = 1;
			else Q = 0;
			end if;
				is the content of register **R** Less than or Equal to the constant **K**?	`R_LE_K macro R,K`
					`local L1,L2`
					`movwf Temp_1`
					`btfss Temp_1,0`
					`goto L1`
					`movfw R`
					`sublw K`
					`skpc`
					`goto L1`
					`movlw D'1'`
					`goto L2`
					`L1 movlw D'0'`
					`L2`
					`endm`
						W ┤ R <= K ├ W	W — EN Q — W; R; K; <=
							R (8 bit register)
							K (8 bit constant)
							EN (through W) = 0 or 1
							Q (through W) = 0 or 1
							if EN = 1 then
							if R <= K then Q = 1;
							else Q = 0;
							end if;

is the content of register **R** **EQ**ual to the constant **K**?	`R_EQ_K macro R,K`
	`local L1,L2`
	`movwf Temp_1`
	`btfss Temp_1,0`
	`goto L1`
	`movfw R`
	`sublw K`
	`skpz`
	`goto L1`
	`movlw D'1'`
	`goto L2`
	`L1 movlw D'0'`
	`L2`
	`endm`
		W ┤ R = K ├ W	W — EN Q — W; R; K; =
			R (8 bit register)
			K (8 bit constant)
			EN (through W) = 0 or 1
			Q (through W) = 0 or 1
			if EN = 1 then
			if R = K then Q = 1;
			else Q = 0;
			end if;
				is the content of register **R** Not Equal to the constant **K**?	`R_NE_K macro R,K`
					`local L1,L2`
					`movwf Temp_1`
					`btfss Temp_1,0`
					`goto L1`
					`movfw R`
					`sublw K`
					`skpnz`
					`goto L1`
					`movlw D'1'`
					`goto L2`
					`L1 movlw D'0'`
					`L2`
					`endm`
						W ┤ R <> K ├ W	W — EN Q — W; R; K; <>
							R (8 bit register)
							K (8 bit constant)
							EN (through W) = 0 or 1
							Q (through W) = 0 or 1
							if EN = 1 then
							if R ≠ K then Q = 1;
							else Q = 0;
							end if;

***Table 3:** The comparison macros described for comparing the contents of two 8-bit registers R1 and R2, together with their descriptions, algorithms and symbols*

```
.
      #include <definitions.inc>    ;basic PLC definitions, macros, etc.
      #include <cntct_mcr_def.inc>  ;Contact & Relay based macros
      #include <cmpr_mcr_def.inc>   ;Comparison macros
      #include <mv_ld_mcr_def.inc>  ;move_R and load_R macros
.
;--------------- user program starts here ------------------------
      ld          FRSTSCN           ;rung 1
      load_R      0Fh,Temp_1
      move_R      Temp_1,M3

      ld          LOGIC1            ;rung 2
      R1_GT_R2    I0,M3
      out         Q0.0

      ld          LOGIC1            ;rung 3
      R1_GE_R2    I0,M3
      out         Q0.1

      ld          LOGIC1            ;rung 4
      R1_EQ_R2    I0,M3
      out         Q0.2

      ld          LOGIC1            ;rung 5
      R1_LT_R2    I0,M3
      out         Q0.3

      ld          LOGIC1            ;rung 6
      R1_LE_R2    I0,M3
      out         Q0.4

      ld          LOGIC1            ;rung 7
      R1_NE_R2    I0,M3
      out         Q0.5
;--------------- user program ends here -------------------------
.
```

Figure 2: *The user program UZAM_plc_8i8o_ex13.asm*

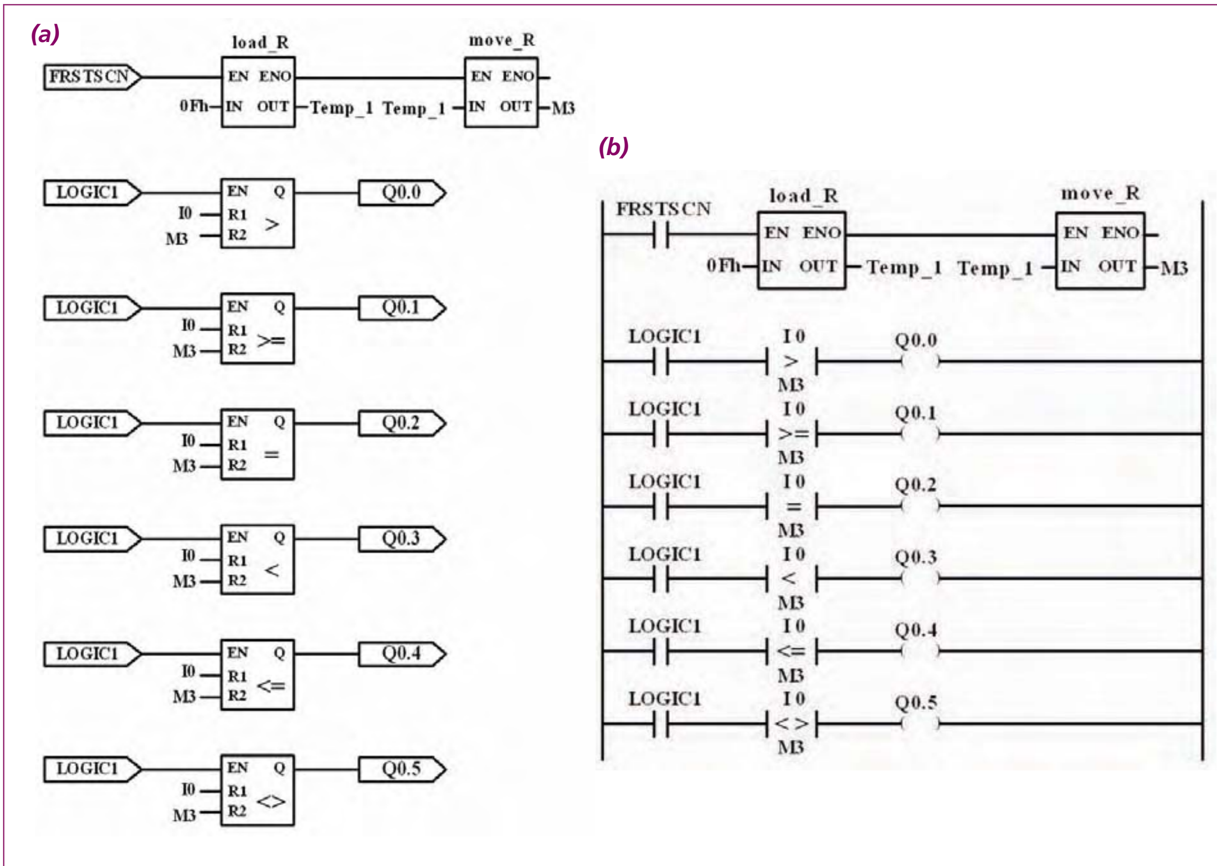


Figure 3: (a) *Schematic diagram and* ***(b)*** *Ladder diagram for the user program UZAM_plc_8i8o_ex13.asm*

```
.
      #include <definitions.inc>    ;basic PLC definitions, macros, etc.
      #include <cntct_mcr_def.inc>  ;Contact & Relay based macros
      #include <cmpr_mcr_def.inc>   ;Comparison macros
.
;--------------- user program starts here ------------------------
      ld          LOGIC1            ;rung 1
      R_GT_K      I0,0Fh
      out         Q0.0

      ld          LOGIC1            ;rung 2
      R_GE_K      I0,0Fh
      out         Q0.1

      ld          LOGIC1            ;rung 3
      R_EQ_K      I0,0Fh
      out         Q0.2

      ld          LOGIC1            ;rung 4
      R_LT_K      I0,0Fh
      out         Q0.3

      ld          LOGIC1            ;rung 5
      R_LE_K      I0,0Fh
      out         Q0.4

      ld          LOGIC1            ;rung 6
      R_NE_K      I0,0Fh
      out         Q0.5
;--------------- user program ends here --------------------------
.
```

Figure 4: *The user program UZAM_plc_8i8o_ex14.asm*

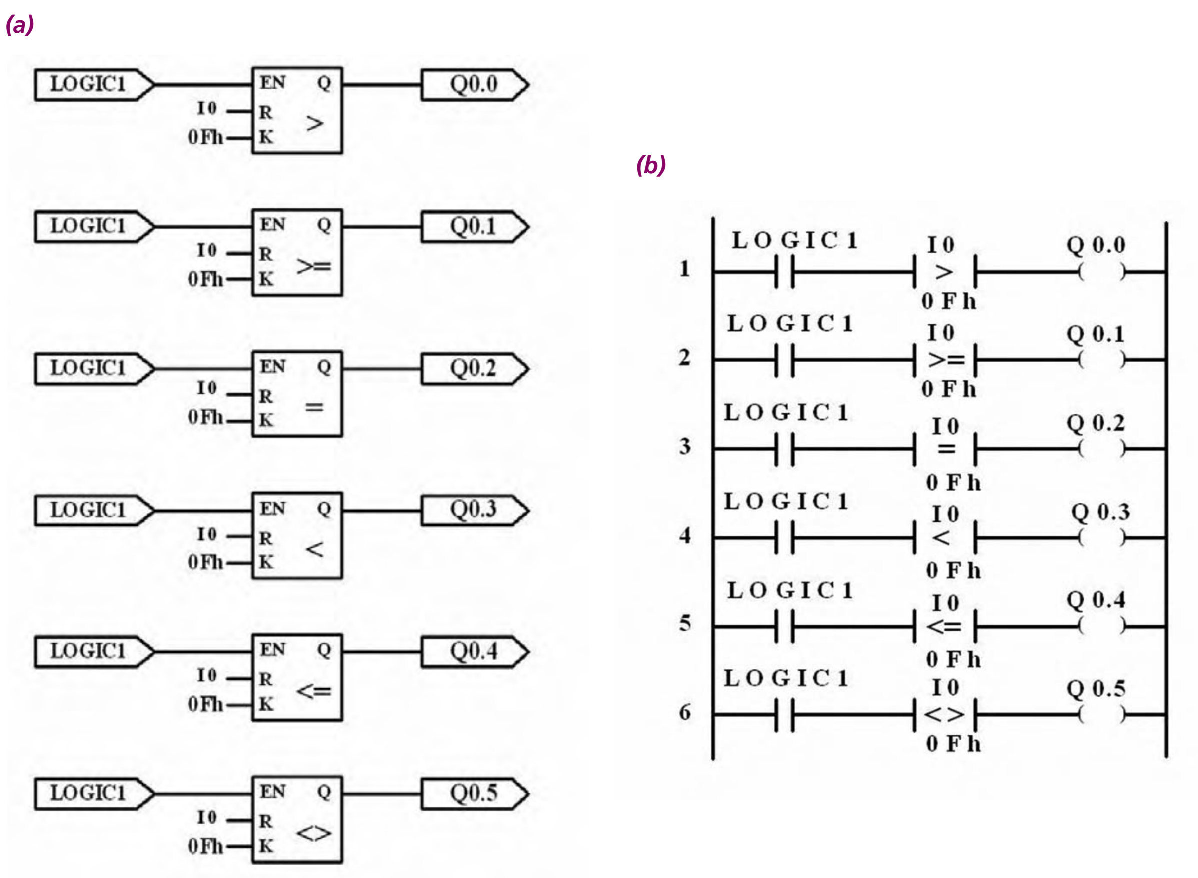


Figure 5: (a) *Schematic diagram and* ***(b)*** *Ladder diagram for the user program UZAM_plc_8i8o_ex14.asm*

Should SOFTWARE Come with Certificates of IP Cleanliness?

REMEMBER the troubles Cisco had with the software licensing issues in one of its products?

Cisco was not guilty of any premeditated infringement of software licensing obligations as it acquired Linksys in good faith and proceeded to distribute its products. Alas, Linksys had used a chip from a supplier who had used some outsource contractors to develop associated software. These sub-sub-contractors had used a piece of open source software that had a GPL license, which obliges the user to make all derivative software available by itself as an open source item under the same GPL license. Nobody in the Cisco-Linksys-chip supplier chain was aware of this piece of code, but when legally challenged, Cisco had only two options to pursue: withdraw the product from the market or make all the product source code available as open source.

To the market delight, Cisco chose the second option for that specific product, but then went ahead and re-engineered the follow-on product line to eliminate the troublesome piece of code. This was a rather expensive lesson for Cisco, but it served well for all of the industry to see the consequences of not making sure of the intellectual property (IP) licensing and copyright obligations in their software.

Ascertaining IP Cleanliness is Key

So, how should one go about ascertaining the IP cleanliness of bought-in software or of software that's just about to be acquired?

Software is a pervasive element in most industrial products and processes nowadays. It comes from internal developments, from suppliers of sub-systems and chips, from outsourced development contractors, from open source repositories or simply from the previous work of the developers themselves. Software, unlike hardware, is easily replicable, accessed, copied and re-used.

In many cases software appears to be cost free. But that is not completely true, as it comes laden with licensing and copyright obligations that are enforceable by law – sometimes with dire consequences for the hapless manufacturer who was not careful to validate the pedigree of the code in its products; i.e. the provenance and the associated obligations of all software components.

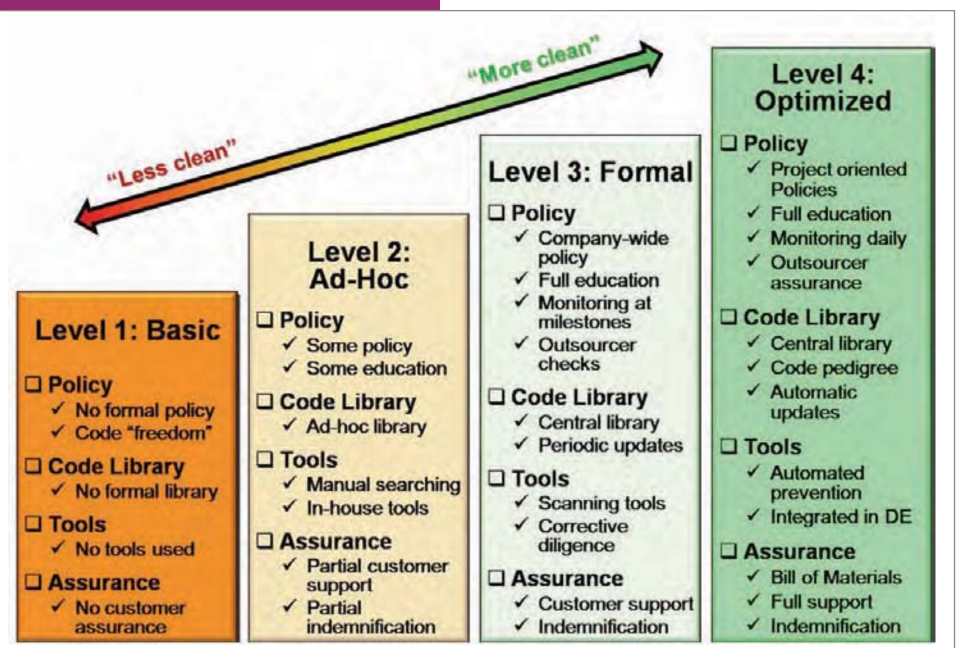


Figure 1: *Status of IP management – the four levels of the spectrum*

This does not mean that outsourcing or the use of open source software is to be avoided. No, not at all. Open source is very valuable and its use has grown tremendously, thanks to the wealth of source code available and its high degree of stability and security. The issue is not with the use of open source, but with the unmanaged adoption without proper care to the copyright and licensing obligations it entails.

The situation is exacerbated in a down economy as many businesses are forced to reduce costs and shorten time to market, which is leading to more use of external contractors and open source software. This makes it paramount for industrial managers to validate the IP cleanliness of their products and services before they reach the market.

Like most hardware products, software products need to have an associated Bill of Materials (BoM) that fully records the components in the product, their provenance and the licensing and copyright obligations each of them entail, making sure that there are no incompatibilities or violations. An adequate software BoM is instrumental in certifying the IP cleanliness of the software and provides the necessary assurance to customers. As such, it can minimize the cost of indemnification and other associated legal obligations.

Traditionally, IP cleanliness was done manually through rather expensive expert analyses and due diligence processes, mostly undertaken in advance of important financial transactions – a merger, an acquisition or a major commercial undertaking. Manual analyses are prone to error, consume expert resources, take long time and are becoming prohibitively expensive nowadays, when software is so pervasive and the use of open

Mahshad Koohgoli, CEO of Ottawa-based Protecode, and **Sorin Cohn-Sfetcu** discuss how to go about ascertaining the IP cleanliness of newly acquired software for your design

source and outsourcing so prevalent.

Fortunately, nowadays there are tools at our disposal to do such pedigree analyses automatically – on demand, on schedule, or even in real-time within the development process. Some of these tools allow the analyses to be done in accordance with corporate IP policies and lend themselves well to an institutionalization of proper record-keeping and safe software development practices.

Corporate IP policies must be based on the organizations' business goals and they should be clear and enforceable. They need to show the acceptable licenses, the approved vendors, what is restricted, and what should be done if unknown or unacceptable code is being brought into the organization's software.

As the critical factors driving the economics of software management are the efforts to fix the software IP issues and the associated delays in product introduction to market, everything should be done to catch IP issues as soon as possible in the development process rather than wait until the product is finished.

Major Aspects of Software IP Management

The major aspects of software IP management in an organization are:

- The existence of an IP policy and a process to disseminate and apply it. This includes the adequate education of personnel involved.
- The availability of a central code library, which includes the legacy code in the organization, together with a process for updating it.
- The processes and tools for ascertaining the legal obligations and managing the IP of software created and/or used in the organization.
- The customer assurance and support concerning the quality and IP cleanliness of the software provided.

Organizations can use the above aspects of software IP management as the criteria for determining their status (level) of performance. Basically, there are four distinct levels (see **Figure 1**)

- Level 1. This is the stage of "avoidance". There is no IP policy and developers have full "freedom" to use whichever code components. There is no code library or any process to ascertain the IP cleanliness of the software produced. Therefore, no customer assurance is provided.
- Level 2. This is the "ad-hoc" stage. There is some IP policy and some training is provided as well. An ad-hoc code library exists and manual techniques or in-house tools are used to manage the software IP issues. Customer assurance is provided through partial indemnification.
- Level 3. This is the "formal" stage. There is a company-wide IP policy and full training is provided. A central code library is established and periodic updates are performed. Automatic scanning tools are used for due diligence at the end of software projects or at major milestones. Customer indemnification and support is available.
- Level 4. This is the "optimized" stage. IP policies are in place and are enforced

Figure 2: *The IP management flow process*

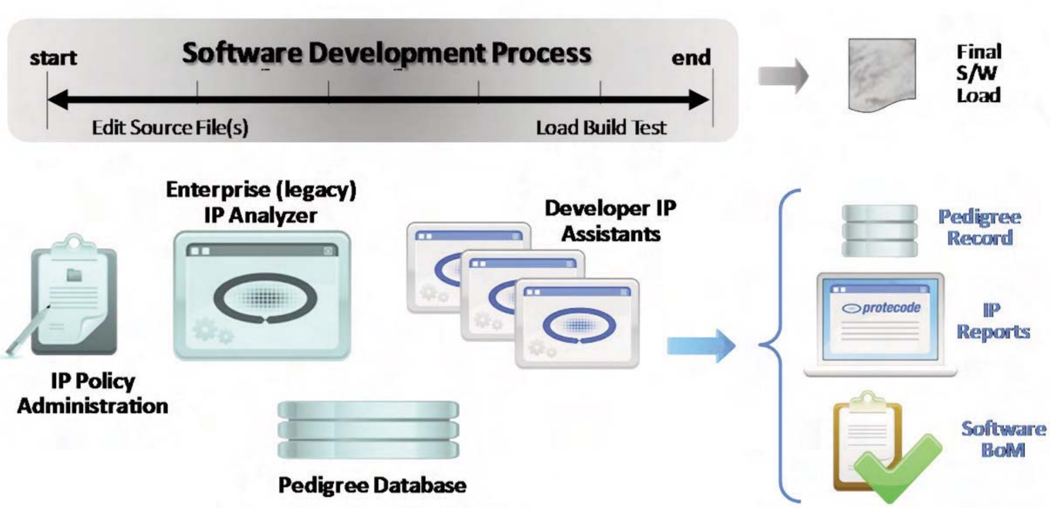


Figure 3: *IP management integration in a development process*

automatically through continuous monitoring. The central code library has an associated pedigree database and automatic updates are done every time new code is acquired. Software record-keeping and pedigree vetting is performed in real-time, thus preventing any code with undesired or unknown legal obligations. Customers benefit from full support and assurance on the IP cleanliness of software provided.

The best results are obtained when record keeping and IP management are treated as integral parts of the software development and quality assurance process (see **Figure 2**):

- The establishment and enforcement of an organization software IP policy commensurate with the corporate business goals. Large organizations may choose to establish IP policies appropriate for each class of project (software) they are undertaking.
- The creation of a central (legacy) code library for the enterprise (organization) and its subsequent analysis for the establishment of an associated pedigree database, which should capture the provenance and legal obligations associated with each code component in the enterprise (organization) code portfolio.
- The intellectual property audit and interpretation of the existing software status vis-à-vis the organization's IP policy, with adequate follow-up actions to remedy any policy violations.
- The enforcement of IP cleanliness assurance for any software acquired from outsourced development partners.
- The real-time gathering of software records for all new source code created or brought into the organization by its developers.
- Preventive analysis of each new software component to ensure that it meets the corporate IP policy;
- Alerting developers if code brought into the project does not meet corporate IP policy, together with instructions on what to do in order to alleviate the situation in real time.
- The completion of a software BoM which contains information on all components, including their origin, licensing obligations, supplier history, version, and all other pertinent information for proper life-time management.

Done properly, software IP management should be unobtrusive to the developers, requiring their attention only when code of unknown or unacceptable pedigree is brought into the software. Equally important, preventive application of automatic software IP management results in the delivery of a software BoM which can be used to certify the IP cleanliness of the software and alleviate risks associated with its licensing and copyright obligations.

Several automatic tools for record keeping and source code portfolio management have been made available recently to help companies lower development and legal costs, reduce time-to-market and lower business risks. Some of the more advanced tools have been designed from the beginning for easy adoption and application, do not require any special training of developers, are truly affordable even for small companies and provide automatically the desired "certificate of IP cleanliness". ■

FROM PLASMA TO CRYSTAL: The role of lasers in display manufacture

Mike Mason, VP Technology at Powerlase, discusses the evolution of the display manufacturing sector and how laser-based manufacturing technologies are changing the market landscape

HIGH QUALITY performance and an attractive appearance have made Flat Panel Display (FPD) televisions very popular across both consumer and business markets. Initial uptake of the units was slow compared to CRT counterparts, due to a high cost of production and subsequent retail price point. It was not uncommon to pay up to £4000 for a 42-inch FPD ten years ago. Now the same screen costs hundreds of pounds, rather than thousands.

Liquid crystal display (LCD) screens are now the technology of choice for smaller displays (42 inch and below). Plasma display panels (PDPs) are the superior technology for screens over 42 inches, as they present a better picture quality at the larger size.

The FPD market is increasingly competitive, as manufacturers continue to be under huge pressure to reduce the cost of FPDs to the consumer as products become commoditized. Improvements in the efficiency of manufacturing common displays, such as PDPs and LCDs, have helped drive the price of production down. This article examines how manufacturers have adopted new techniques to ensure PDP production is more efficient and, as such, cost effective.

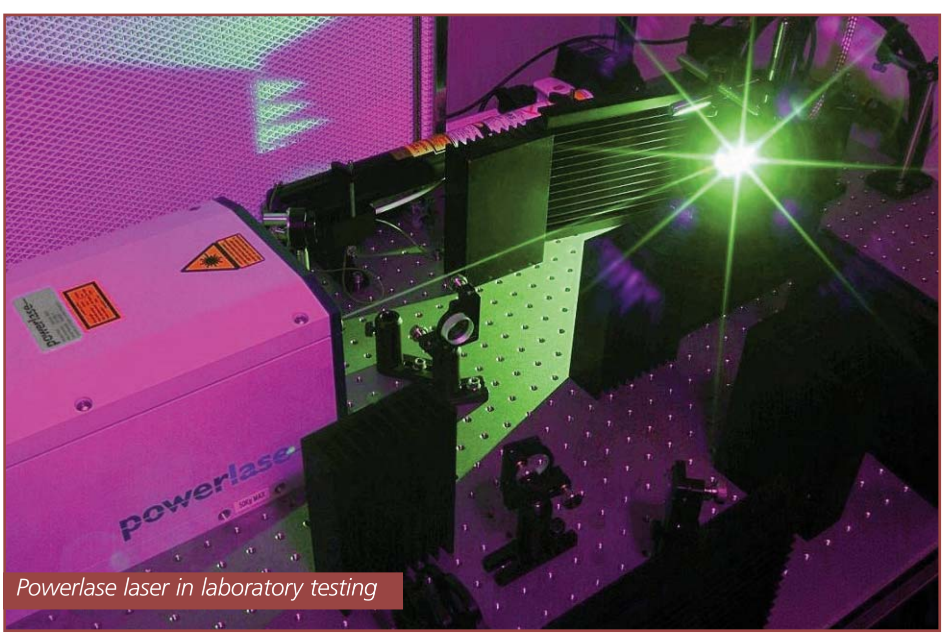
Patterning the PDP

In large screen production, manufacturers' cost reduction is achieved by continuously examining and improving PDP production methods. By employing new technologies to streamline manufacturing costs, PDP manufacturers can reduce their operational costs, allowing them to lower the cost of the end product in order to be as attractive as possible to consumers.

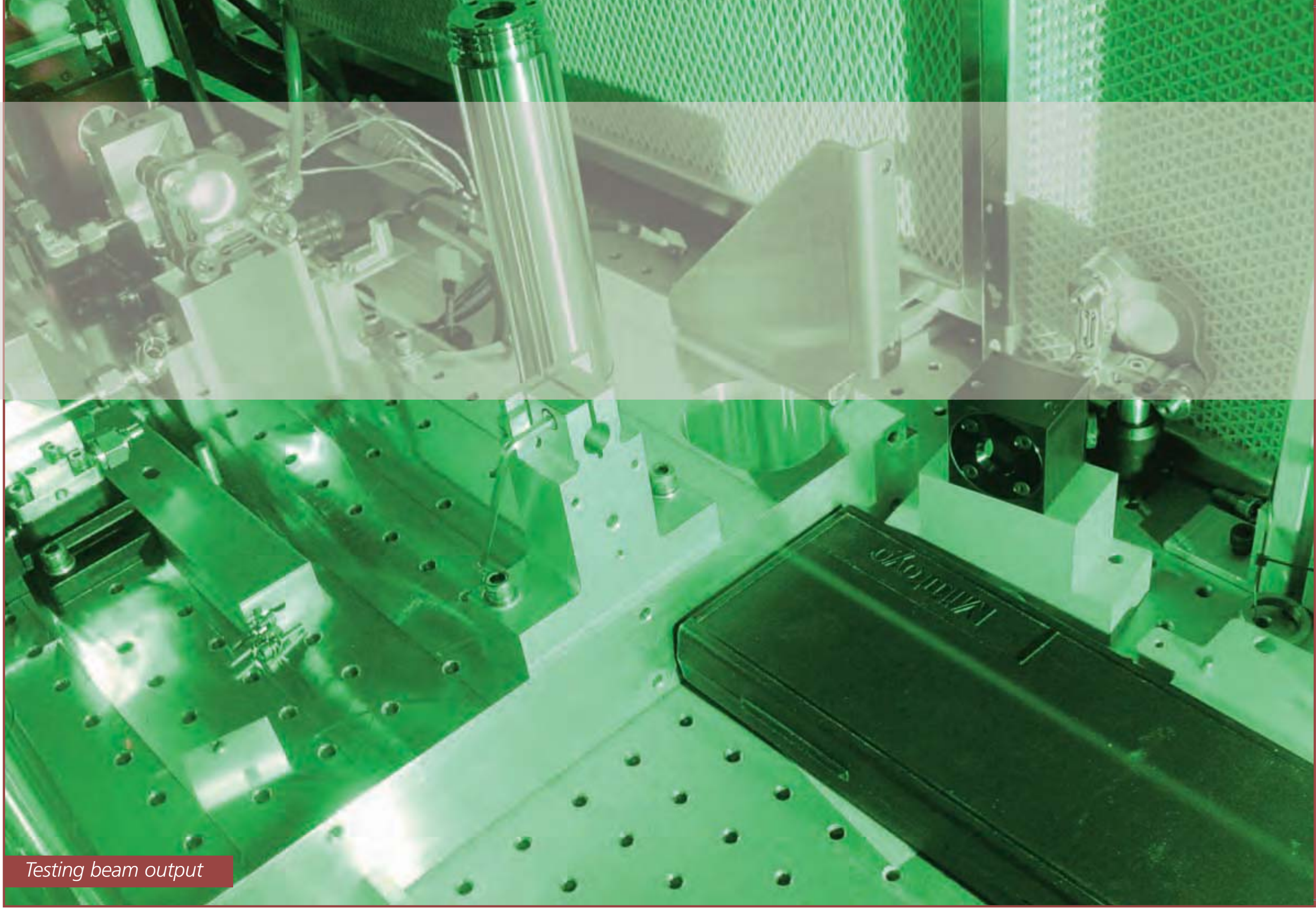
In PDP manufacture, thin film layers of Transparent Conductive Oxides are coated on the glass substrates that make up the display screen. This film layer is 'patterned' to create the pixels that display the picture. Previously, manufacturing PDP screens required large-scale lithography tools to pattern the large area of glass substrates. Each substrate ultimately makes up as many as eight PDP screens, and patterning such a large area of thin film presented a significant challenge. The lithography tools were used to conduct multi-step patterning via a wet-etch technique. Wet-etch lithography involves chemical material removal to pattern the transparent oxide coatings that define the pixel structure.

The wet-etch process has proved to be cost-intensive for manufacturers, with high operational expenditure on a 24/7 production line. The introduction of laser-based patterning techniques has now successfully displaced wet-etch technology in PDP production. A technique dubbed Rapid Laser Patterning (RLP) has been adopted in place of traditional wet-etch lithography.

RLP offers several advantages over traditional patterning techniques, including an overall reduction in operational expenditure. In wet-etch lithography, the chemicals used represent a significant expense as they can only be used once before becoming contaminated with thin-film material from the ablation process. Additional expenditure is also required to



Powerlase laser in laboratory testing



Testing beam output

safely dispose of these chemicals. With RLP, there are few waste products, and thus little to dispose of, offering manufacturers a less costly and more environmentally sound alternative to the use of chemicals.

With RLP, the lack of a need to replenish chemicals means that while the initial capital investment is high, it is significantly more cost-effective to purchase RLP equipment once than continuously replenishing the supply of chemicals needed for wet-etch lithography.

Efficiency is improved with RLP as it produces a higher yield than wet-etch lithography. Of the screens processed via wet-etch, around 80-85% meet the standard for use in PDP manufacture. By comparison, the RLP technique achieves a yield of more than a 99% in creating patterned screens, reducing waste in the manufacturing process.

RLP in Action

In PDP manufacture, positional accuracy is required on the order of microns, with feature sizes being approximately 1x1 mm with an edge resolution of 1μm. This is ideally suited to RLP, as the technique is able to remain highly accurate while covering the large areas of PDPs at a high-speed manufacturing rate.

Diode pumped solid state lasers are favoured for RLP because they offer average power levels up to 1600W, at kilohertz repetition rates, with nanosecond pulse durations and pulse energies of greater than 250mJ. The lasers operate with medium beam quality, allowing the laser beam to be homogenized, imaged onto a mask and re-imaged on to the glass substrate. The high pulse energies allow sufficient energy density to ablate large pixels (approximately $1mm^2$) with a single pulse. Kilohertz repetition rates mean thousands of pixels can be ablated per second, and by 'stitching' the pixels together large areas of active Transparent Oxide electrode structure can be created very rapidly. To further improve the throughput of industrial systems, multiple lasers can be employed on a single machine.

RLP technology has now been adopted in multiple global sites, replacing lithography systems, by market-leading FPD manufacturers Samsung and LG Electronics, in full 24/7 mass production of PDPs.

Next Generation Screens

The RLP technique has greatly reduced the cost and increased the efficiency of PDP manufacture, allowing manufacturers to reduce end unit costs and remain competitive in the market. While analysts are predicting PDP sales have reached a plateau and will begin to decline in coming years, sales still remain strong in emerging markets in Asia.

Despite this, new display technologies continue to emerge, with organic light emitting diode (OLED) screens widely billed as the next generation television of choice. Active matrix (AMOLED) technology is already used for small displays, such as those in mobile devices, and improvements to the technology are making it increasingly viable for larger displays, such as domestic televisions. AMOLED screens are appealing due to their high quality picture and a wider viewing angle, combined with lower power requirements and a thinner design. However, as with PDPs before them, AMOLED screens are currently costly to manufacture and have not yet proved a viable alternative to LCD or PDP display for the mass market.

Growing Crystals

In AMOLED screens, each pixel uses a number of small transistors in order to activate and deactivate it. These transistors are located next to each pixel within the display. In order to produce a display with a fast response time and refresh rate, high quality silicon crystals are required to form these transistors.

Normally, silicon is layered onto the glass substrate screen in an amorphous (non-crystalline) layer during the manufacturing process. In order to convert this amorphous silicon into crystalline silicon, an annealing process is used to stimulate crystal growth. The larger the crystals are the better picture they produce as they form transistors with the ability to refresh at a faster rate.

For this, an annealing process using green lasers, dubbed Green Laser Annealing (GLA), has been developed. This process uses a laser to heat the silicon, causing it to melt. As the melted silicon slowly cools, long, high quality silicon crystals are formed.

Prior to the development of GLA, a similar manufacturing technique known as Excimer Laser Annealing (ELA) was used to process amorphous silicon. The key difference between ELA and the new GLA technique is the laser used. Excimer lasers produce light by using non-environmentally friendly gases, such as chlorine and fluorine. These gases erode components in the laser, meaning Excimer lasers need to be frequently serviced, increasing operational costs incurred by the manufacturers in AMOLED production. By comparison, the 532nm lasers used in GLA produce light through the use of solid-state crystals rather than gases, so do not require the intense maintenance associated with Excimer lasers.

The reduction in cost of ownership and improved results with crystal growth lowers the production cost of AMOLED screens in a similar regard to RLP, lowering the cost of PDP production. In turn, this provides manufacturers with the opportunity to lower overall costs bringing an emerging technology to the wider mass market.

Continuing Evolution

By investing in new production methods, display manufacturers are able to reduce the production cost of both established and emerging technologies. Cost reduction allows manufacturers to remain competitive in the market place and meet the ever increasing demand to drive down cost for the end user. Laser-based manufacturing has proven highly effective in this regard and will continue to evolve and adapt as new display technologies emerge. ■

CONNECTING 120V MAINS ADAPTERS (NON-SMPS) TO A 240V GRID

I GOT SEVERAL US mains adapters, which are unusable with 240V. Since I do not want to waste good material, I've put them together as shown in **Figure 1**. This works well: no warming up at rather high load, and is supported by basic transformer theory.

Note that the device's enclosures are kept closed, making it safer. Also note that the adapters I used are of the old-fashioned type and are bulky devices: transformer, diodes and a buffer capacitor; so no SMPS-based adapters.

The basic 'design' considerations are (stated for three similar adapters):

1. By connecting the three outputs in parallel, the 240V is distributed equally over the three inputs: 80V per adapter.
2. By connecting the three inputs in series, the total output current is distributed equally over the three outputs.

Output voltage for Figure 1 is 80V/20 = 4V (ignoring the increased contribution of the rectifier voltage drops). The available output current is 6A from three 2A adapters.

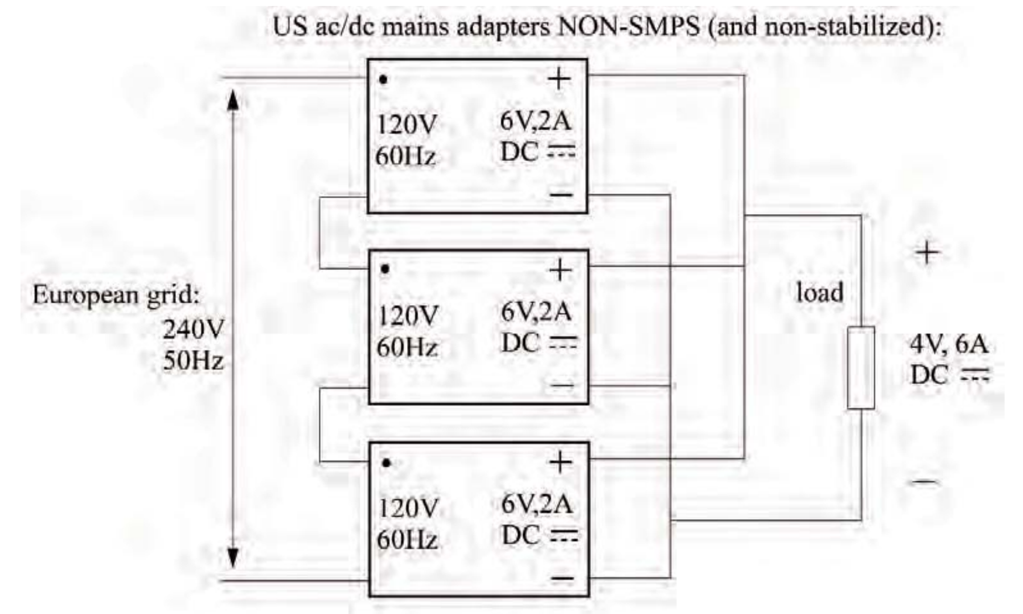


Figure 1: *Practical power supply*

Why use more than two adapters? Because the devices are operated at 50Hz, while the transformers are designed for 60Hz. The rated 120V, 60Hz is equivalent to 100V, 50Hz for the same maximum level of magnetization in the transformer core. So the construction as in Figure 1 can handle up to 300V (for equal adapters). In case adapters of different output voltages are combined, this frequency effect must be taken into account carefully.

Since the adapters are used derated (80V vs 100V rated: thus at 80% voltage level), the continuous maximum available output current will be > 6A, for the rated dissipation. Further, this derated usage makes the circuit tolerant for variability between the devices.

The theory in **Figure 2** tells us "simplified for a transformer only":

ad 1: $(n_1+n_2+n_3)\ V_b = V_{mains.}$

or: $n_1V_b= [\ n_1\ /\ (n_1+n_2+n_3)\ ]$ V_{mains} is 1/3 if $n_i= n$

ad 2: $(n_1+n_2+n_3)\ I_a = I_b$

or: $n_1I_a= [\ n_1\ /\ (n_1+n_2+n_3)\ ]\ I_b$; is 1/3 if $n_i= n$

For the practical construction, the pins can be interconnected by bolt (long) and nut.

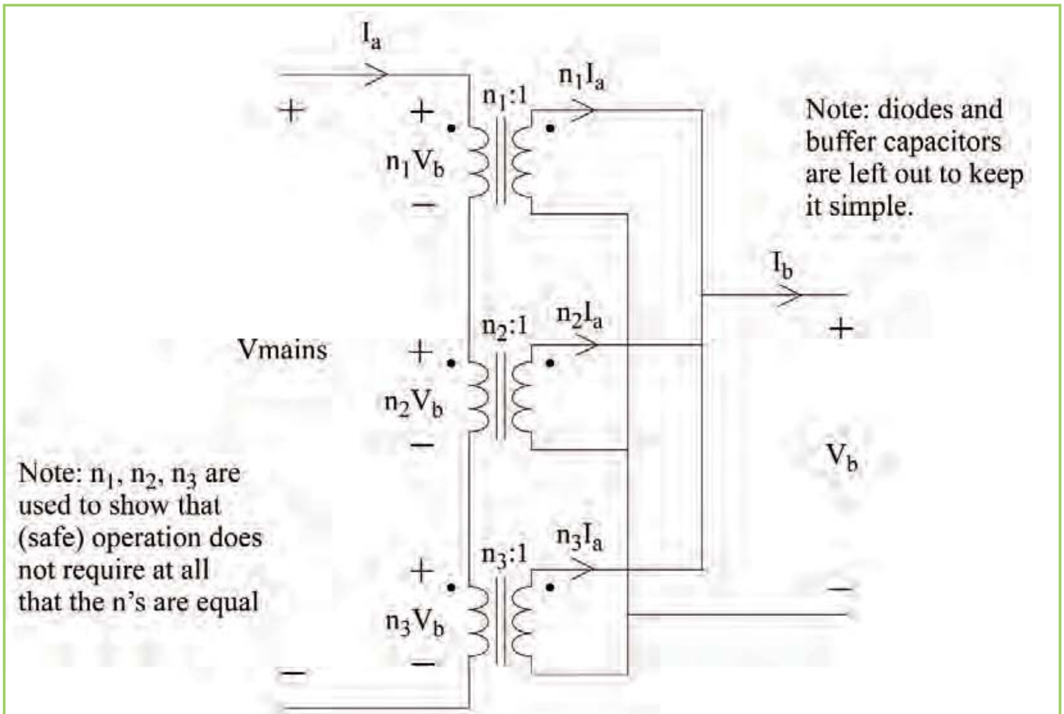


Figure 2: *Theory: V,I distribution: equal if* $n_1=n_2=n_3=n$

Bram Melse
Netherlands

TIP 1: LED DRIVER POWERS HALOGEN REPLACEMENT

By Keith Szolusha, Senior Applications Engineer, Linear Technology Corporation

HIGH BRIGHTNESS LEDs are an inexpensive, robust and green replacement to halogen light bulbs. The tungsten filament base to the halogen bulb has a short lifetime compared to the robust LED. The safety hazards of the inert gas, the expense of the UV filter encasement and the handling sensitivity of halogens are all downsides that an LED light bulb does not have.

Since halogen bulbs are typically driven with 12V or 24V due to their excellent efficacy at that voltage, buildings have been hardwired with 12VAC and 24VAC transformers for powering the halogen lighting. Replacing existing halogen lighting without starting over from scratch requires an LED that can be powered from a 12VAC or 24VAC source.

Replacing AC-driven halogen lighting with LEDs can be done with a switch mode regulator LED driver designed for AC lighting with high power factor. Although switch mode LED drivers are often used to regulate a constant LED current through a string of LEDs from a DC voltage source, such as a computer battery, a car battery, or a regulated system voltage, halogen replacements run off of 12VACrms and require high power factor.

The ideal load with 100% power factor (PF) is a pure resistor. When used with a 12VACrms source and a rectifier bridge (to create 120Hz from 60Hz), the power factor is slightly under 100% using a resistive load such as a halogen or incandescent bulb.

An LED driver with constant (DC) LED current has very poor power factor when used with an AC source in contrast to the resistive load. A constant DC load requires DC power from the input. With an AC source, DC power creates the highest input current when the input voltage is lowest and vice versa. This creates voltage and current input waveforms with a large phase shift and very low power factor. The goal is to create an LED driver with input current in phase with the input voltage. In order to do this, a 120Hz LED current waveform is created to demand the highest input current when the input voltage is the highest and vice versa.

The circuit in **Figure 1** is an LT3755 AC LED driver with 98.1% power factor. The topology is buck-boost mode since the wide-ranging input of 0V to 18V (12Vrms) and the wide ranging 4-LED string voltage of 9V to 14V crossover each other. The 12VACrms input is first rectified by D3-D6 to create a 120Hz 0V to 18V PVIN supply. The PVIN and VIN nodes are separated by a diode since the LT3755 works best when the VIN pin is held above 7V, maintaining 7V on INTVcc and driving the power MOSFET M1 with proper gate voltage. The diode allows peak charging of the VIN cap CVIN, which is big enough to maintain charge when PVIN drops down to 0V.

LED current foldback with the CTRL pin voltage is used to create a high power factor LED driver. The maximum LED current is set by RS2 at 680mA, but the CTRL pin monitors the PVIN voltage and shapes the LED current waveform to match PVIN. When PVIN drops below the shutdown pin threshold, the IC goes into shutdown, switching stops and the soft-start feature is reset.

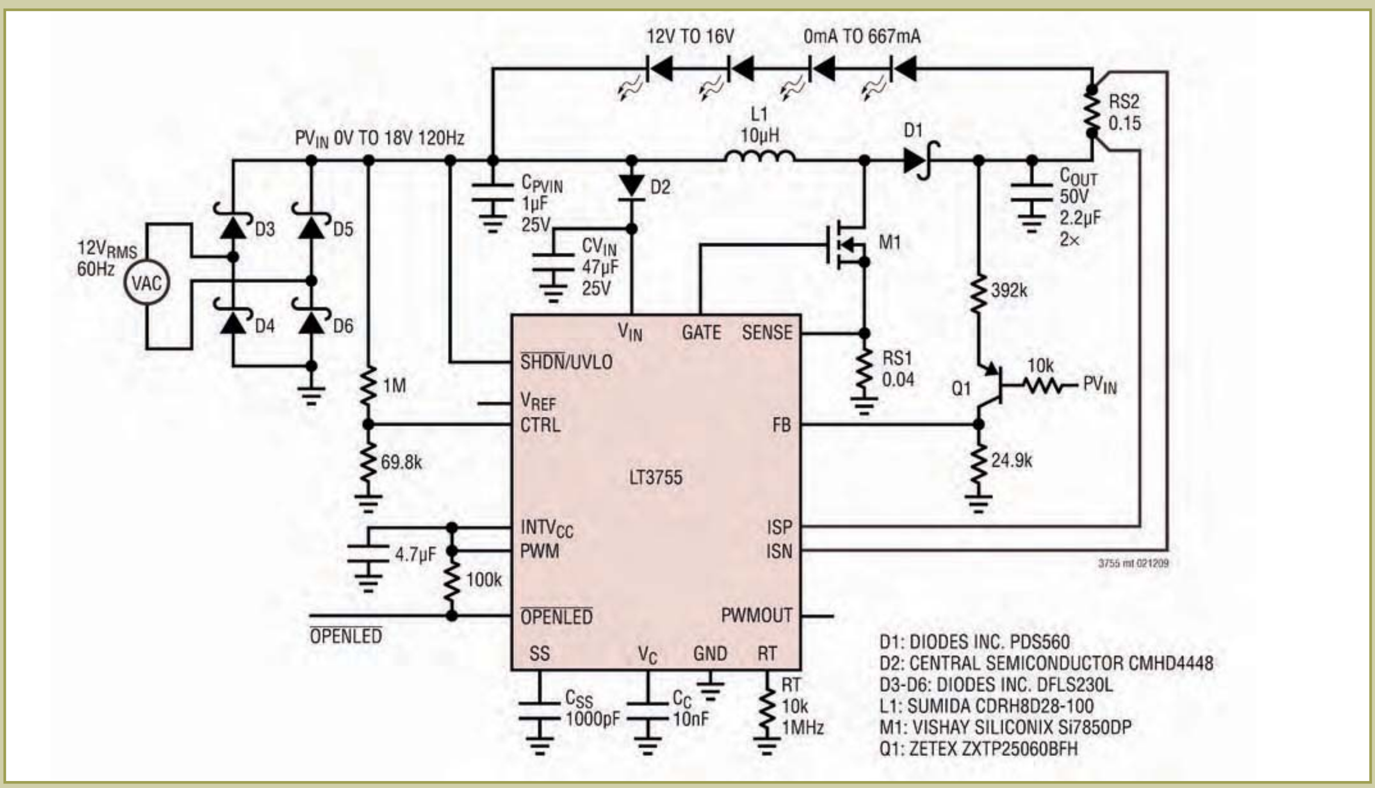


***Figure 1:** LT3755 AC buck-boost mode LED driver with 98.1% power factor schematic*

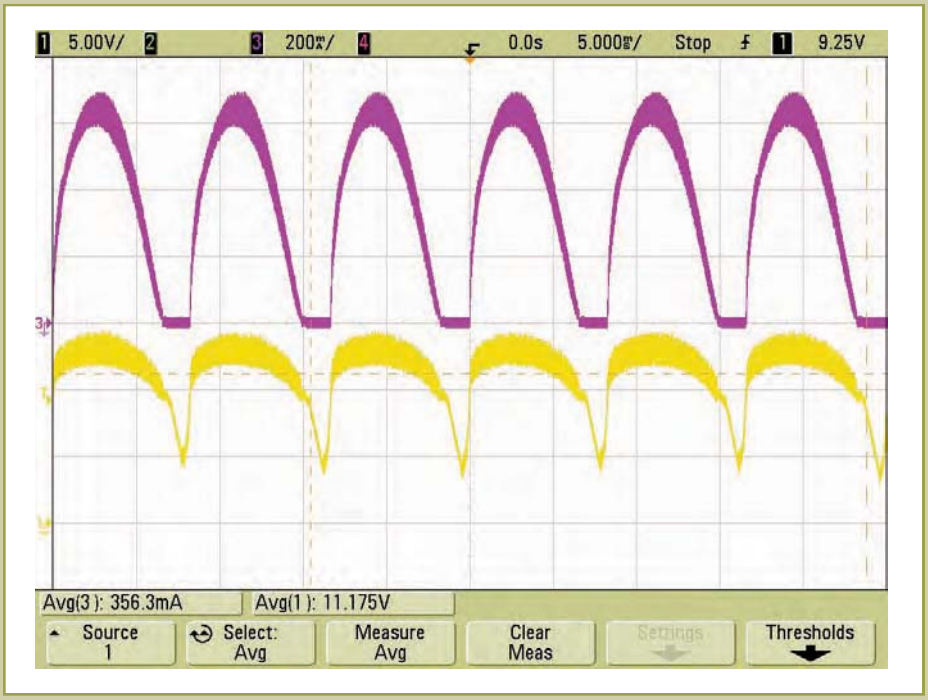


__Figure 2:__ 120Hz AC LED current and voltage waveforms delivering ~ 4W of LED power

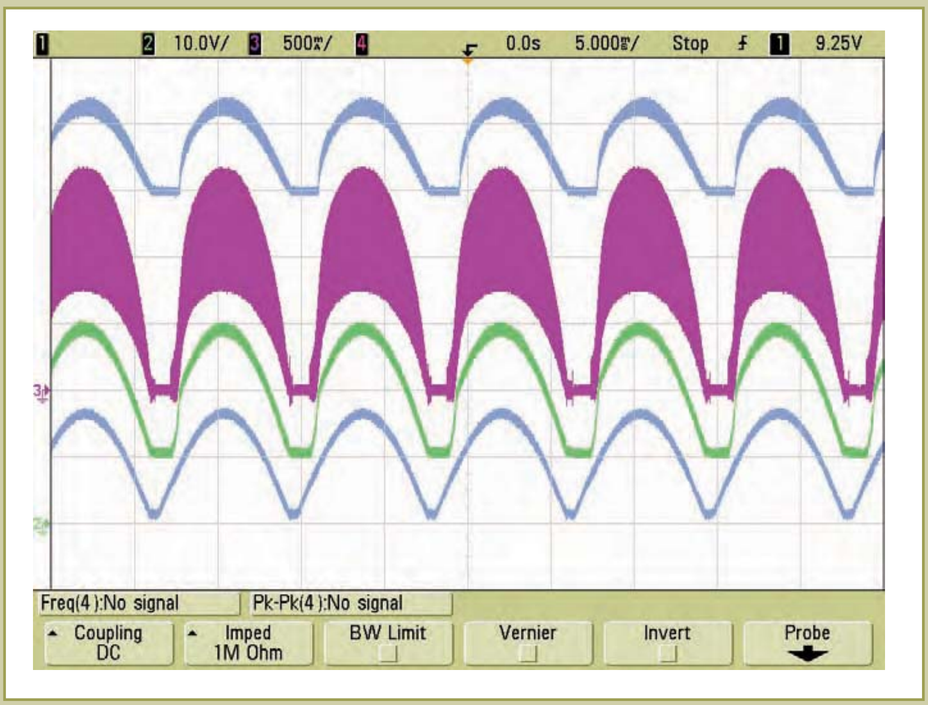


__Figure 3:__ 120Hz AC LED driver waveforms derived from the rectified 12VACrms PVIN

The LED current trails off as the output capacitors are discharged and soon enough, PVIN rises above the shutdown pin threshold voltage and the LT3755 starts back up.

A light soft-start capacitor allows the LT3755 to get started up quickly and keep the power factor high. With the CTRL pin folding back the LED current at low PVIN, startup is not harsh and inrush currents do not affect the high power factor.

Figure 2 shows the LED string current and voltage waveforms at 120Hz. The scope was used to measure the average LED current and the average LED voltage. Multiplying the two is an approximate method for calculating the LED power. 356mA * 11.175V gives about 4W of LED power, enough for an efficient light bulb replacement.

Figure 3 shows the 120Hz waveforms generated by the LT3755 buck-boost mode AC LED driver in Figure 1. PVIN, VLED, IL1 and ILED are shown – all at 120Hz. 120Hz is a high enough frequency to not be perceived by the human eye.

The power factor in this circuit is measured using an Agilent 6811B AC power source/analyzer. The 60Hz AC line voltage and current measurements are shown in **Figure 4** (page 46).

The LT3755 buck-boost mode AC LED driver delivers 4W of high efficiency LED power at 120Hz with 98.1% power factor. This circuit can be used to replace 12VAC halogen lighting with more robust LEDs. This high power factor of this AC LED driver rivals the high power factor of an incandescent filament-based bulb with purely resistive load properties. ■

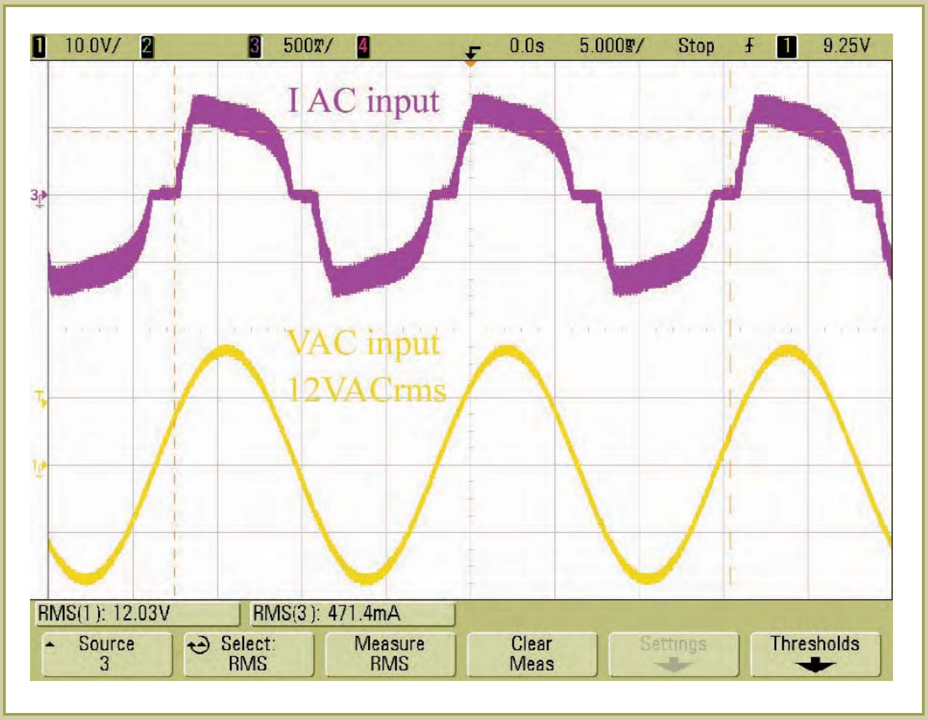


Figure 4: *12VACrms pre-rectifier line voltage and current waveforms with 98.1% power factor*

WEBSITE DIRECTORY

LED ILLUMINATED PUSHBUTTON SWITCHES FROM KNITTER-SWITCH GIVE USERS A POSITIVE "FEEL"

Switch manufacturer, knitter-switch, has announced a new series of pushbutton switches that will find wide interest among manufacturers of test and measurement instruments, multimedia devices and industrial automation systems.

Because the MPLS 12 series has a long travel of > 5mm, users get what knitter-switch calls "a distinctive switch feeling" when using the new switch. This positive actuation response gives users tactile reassurance that the switch has activated. This can be very useful in noisy environments such as factories and control rooms.

The switches are offered in white, red, amber, green, blue and with amber/green or red/green Dual-LED. Thanks to the use of gold-plated contacts and terminals, switching current is a minimum of 10µA

The MPLS 12 series of pushbutton switches are surface mount products suitable for 260°C reflow soldering and feature a mechanical lifetime of at least 30,000 operations. Both latching and momentary types are offered.

The new switches are available from a number of distributors throughout Europe. Samples are usually available on next day delivery.

www.knitter-switch.com

NEW UPCONVERTER SUPPORTS TRANSCEIVER TEST AND SIMPLIFIES TEST SYSTEM DESIGN

Keithley Instruments has introduced its Model 2891-IQ Upconverter, which provides comprehensive support for transceiver testing by processing analogue I and Q baseband signals for testing a transceiver's transmitter, as well as processing analogue I and Q output signals for testing a transceiver's receiver.

This model converts single-ended baseband analogue I and Q signals from a signal generator into differential output signals to provide input signals for testing transceivers with differential baseband IQ inputs. On the receiver side, it converts the receiver's down-converted differential I and Q signals into a modulated, up-converted signal for receiver performance testing by an RF signal analyzer. It speeds and simplifies designing transceiver test systems because it interfaces easily with both RF transceivers and with Keithley's Series 2900 RF vector signal generators and Series 2800 RF vector signal analyzers.

The combination of the Model 2891-IQ with the Model 2920 vector signal generator and the Model 2820A vector signal analyzer makes it easy to create a small, simple and cost-effective RF transceiver test system. The Model 2891-IQ contains gain adjustments so that it can interface with a wide variety of wireless chipsets and devices. Furthermore, the Model 2891-IQ can interface with RF transceivers with either single-ended or differential inputs. Its EVM floor of 41dB, even for wideband 40MHz-bandwidth 802.11n signals, makes it possible to use the Model 2891-IQ when making high quality modulation measurements.

www.keithley.com

MODULAR & VERSATILE – THE AXIOHM KMGA KIOSK PRINTER FROM DED

Expanding on its already comprehensive range of kiosk printers, DED introduces the heavy duty Axiohm KMGA thermal kiosk printer. A modular printer designed to fit an array of self-service applications, the KMGA brings superior performance and low maintenance to the world of kiosk printers.

The versatile KMGA offers a wealth of possibilities combined into one printer. Printing at 180mm per second, the KMGA features an adjustable print width of between 58 and 82.5mm and paper diameter of up to 250mm, making it the ideal printer for unattended kiosks. The ability to take thicker paper stock makes the KMGA particularly suited to ticket printing applications; using regular weight paper it is, of course, suitable for a variety of self-service and information kiosks.

The adjustable paper holder on the KMGA offers up to four possible configurations and six positions from +75 degrees C to -60 degrees C, offering superb flexibility for integration into kiosks. The operating temperature on the KMGA is between -20 degrees C to +60 degrees C, making it suitable for either indoor or outdoor use.

Other features on the KMGA include an anti paper-jam system to provide trouble-free receipt delivery, a paper out/low sensor to monitor paper supply levels, and a full or partial jam-free cutter.

www.ded.co.uk

KONTRON MICROETXEXPRESS COMPUTER-ON-MODULES FEATURE INTEL ATOM PROCESSOR N270 AND S5 ECO STATE

Kontron's new microETXexpress-DC Computer-on-Module offers a host of features coupled with superior graphic performance for the development of mini devices. The energy-efficient Kontron microETXexpress-DC is equipped with the Intel Atom processor N270 (1.6GHz) with Hyperthreading, Intel 945GSE and Intel ICH7M chipset as well as Kontron's new S5 Eco State.

With its great 3D graphic power and dual independent display support via SVDO, LVDS, VGA and TV-out, the new Computer-on-Module is ideal for a wide range of embedded applications, extending from embedded netbooks, to in-vehicle and solar-operated devices right up to classic, stationary embedded systems, especially taking into account its low power consumption too.

Kontron's microETXexpress-DC Computer-on-Module is also the ideal choice for graphics and interface demanding applications in market segments such as medical equipment, test and measurement, maintenance, transportation, HMIs for the energy and automation sector, as well as kiosk and digital signage solutions for POS/POI.

The Kontron microETXexpress-DC Computer-on-Module has dimensions of just 95mm x 95mm and due to the fact that it is 100% compatible to the type 2 pin-out of the COM Express specification in regards to pin-out and position of the connectors, for which recently an official PICMG carrier board design guide was published, it offers design security and scalability of the highest level plus long-term availability.

www.kontron.com

COMPREHENSIVE RANGE OF BAYONET COUPLING CONNECTORS ANNOUNCED BY LANE ELECTRONICS

Lane Electronics, supplier of electrical and electronic interconnection products, announced a comprehensive range of Bayonet Coupling Connectors manufactured by fellow Lodge Group company, Weald Electronics.

The LMH Series has been designed to perform to the requirements of MIL-C-26482 Series 1 and Patt 105. The connectors are also approved to IECQ-CECC spec BS/CECC 75201-003 and BS 9522 F0017.

Available in nine shell sizes and 33 shell styles, the LMH Series connectors can be supplied from stock with 2 to 61 contacts in 20 contact arrangements. They can also be specified in a RoHS compliant olive drab finish.

Peak working voltages can be as high as 1200V, DC or AC. A 360°C screen termination option provides full EMC protection. Free shells with grounding fingers and PCB contacts for fixed styles are also part of the LMH Series.

Lane can provide a wide selection of accessories including J sealing glands and protective caps.

Lane is also a source of other key connector types including circular, filtered, RF, coaxial, sub – miniature, backshells and adaptors, D connectors, aerospace, test and measurement, IDC, PCB connectors, edge connectors and connectors for rack and panel applications.

www.fclane.com

NEW CAPACITIVE SENSOR TECHNOLOGY ALLOWS FOR CONTINUOUS AND CONTACT-FREE LEVEL MEASUREMENT

Sensortechnics's CLC series uses a new contact-free capacitive sensor technology to continuously measure the fill level of liquids, as well as granular or pulverized materials. The miniature sensor can be easily mounted to the outside of a container or vessel and is able to measure through almost any non-metallic wall material. The level sensing range of the standard device is up to 10cm, which can be enlarged in special multi-sensor configurations.

The non-invasive design, with no contact between the sensor and the fluid, eliminates all media compatibility and sterility issues. The device is highly flexible and the user can easily calibrate the sensor to measure to the desired levels, media and application set-up. The CLC series achieves a very high accuracy and reliability due to an additional reference electrode that compensates for all changes in ambient environmental conditions such as temperature and humidity. As an optional safety feature the sensor can be supplied with an extra sensing pad to detect if a container is actually present or not.

The CLC sensor offers an analogue voltage output, as well as a digital interface. Sensortechnics can also provide modifications of its capacitive level sensor based on customer specific requirements.

Due to its new, continuous and contact-free technology Sensortechnics's CLC capacitive sensor can be used in many level monitoring applications within medical technology, chemical and pharmaceutical industries, also biotechnology as well as food and beverage.

www.sensortechnics.com

RIELLO MULTI PLUS PROVIDES ENERGY SAVING POWER PROTECTION

The Riello Multi Plus UPS sets the specification for energy saving, flexibility and electrical performance. The latest 30kVA and 40kVA modules are designed to power mini data centres (running 80 to 100 servers) but can be scaled using a decentralised parallel architecture for larger installations.

Within a data centre environment, energy management is critical. Running costs need to be minimized and environmental concerns addressed, while still offering optimum resilience and power protection. Ideal for the protection of critical information and telecommunication networks, the Multi Plus is designed to meet the specific energy demands of this high-pressure environment. The exceptional quality of the components and technology used by Riello allows the Multi Plus UPS to operate with an industry-leading on-line efficiency of up to 96.5%. This can provide up to a 50% saving in energy usage per annum compared to traditional UPS.

Independently tested, and rated as a Level 6 product on Riello's unique Eco Energy Level Scale, the Multi Plus range achieves high performance with a surprisingly small footprint, freeing up valuable floor-space. Multi Plus also has a range of advanced battery optimisation features; extending the average working life of a battery set and reducing lifetime management costs.

www.riello-ups.co.uk

RF VECTOR SIGNAL ANALYZER OFFERS IMPROVED SPEED AND ENHANCED MEASUREMENT PERFORMANCE

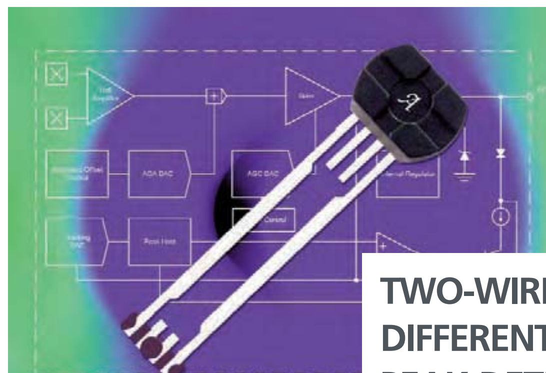
Keithley Instruments announced that it has upgraded its popular RF Vector Signal Analyzer line with new capabilities that reduce signal acquisition and measurement times. The new Model 2820A RF Vector Signal Analyzer, which provides a 40MHz signal acquisition bandwidth with a frequency range of either 400MHz-4GHz or 400MHz-6GHz, builds on the capabilities of Keithley's Series 2800 signal analyzer line. It expands the line's applications for testing wireless devices to today's high throughput, complex modulation and wide bandwidth wireless telecom standards.

The Model 2820's combination of fast frequency tuning, a desktop control panel, high speed USB interface and fast sequence testing makes it the industry's fastest transmitter calibrator and substantially reduces production test time and test costs.

In addition to the existing demodulation and signal analysis options for GSM, EDGE, EDGE Evolution, WCDMA, HSDPA, cdma2000, WLAN and WiMAX transmissions, the Model 2820A can now analyze 3GPP Release 7, HSPA+ signals with a new optional personality. Each preconfigured personality provides a robust set of measurements, instrument settings, and test limits customized for the various standards. These personalities save configuration time and minimize the potential for operator error.

This model is among the latest additions to Keithley's MIMO (Multiple-Input, Multiple-Output) testing system solutions. The new 100Mb/sec data transfer rate allows researchers to conduct advanced MIMO studies in such areas as channel sounding and beam forming.

www.keithley.com



TWO-WIRE DIFFERENTIAL PEAK-DETECTING HALL SENSOR OFFERS TRUE ZERO-SPEED OPERATION

The new ATS682LSH from Allegro MicroSystems Europe is a Hall-effect sensing integrated circuit and magnet combination that provides a flexible, easy-to-use solution for true zero-speed sensing of ferrous targets in two-wire applications.

The new device is particularly suited to gear-tooth sensing in automotive applications, for example in wheel-speed sensing in anti-lock braking systems, and can be used in conjunction with a wide variety of gear shapes and sizes.

The ATS682LSH incorporates a dual-element Hall-effect sensor and signal-processing circuitry that switches in response to differential magnetic signals created by a ferrous target. The device contains sophisticated electronics that reduces magnet and system offsets, calibrates the gain for air-gap independent switch points and provides true zero-speed operation.

Signal optimisation occurs at power-up through the combination of offset and gain adjustment and is maintained throughout operation with the use of a running-mode calibration that allows immunity to environmental effects such as micro-oscillations of the sensed target at start-up or sudden air-gap changes.

The digital peak-detecting algorithm is capable of tracking harsh magnetic profiles resulting from target design and/or applications conditions such as ferrous contamination, damaged teeth or 'pot-holes'.

The regulated current output is configured for two-wire interface circuitry and is ideally suited for obtaining speed information in wheel speed applications. The Hall element spacing is optimised for use with high-resolution, small-diameter targets.

www.allegromicro.com

VICOR 'POWERTECHTORIALS' ON CD

Vicor has launched a new educational initiative for power design engineers to provide support throughout the power systems design process from selecting the optimum architecture to meeting EMI regulations.

A series of 'PowerTechtorials' is the first phase and is now available on CD. Each CD serves as a one-on-one tutorial, containing technical presentations and lab demos, that can be revisited as needed. The tutorials address everyday technical issues and answer real-world questions on power system design topics, providing engineers with practical advice for solving design challenges that arise in a broad range of different applications. In addition, the interactive CD contains useful links to the Internet for easy access to product datasheets, related articles, application notes and more.

Volume 1 contains three videos covering the following topics: 'Vicor DC-DC Converter Theory Overview'; 'Improving Output Filtering' and 'Input Overvoltage Protection'. Engineers who sign up to receive their free 'PowerTechtorial' CD Volume 1 will be able to suggest topics to be covered in future editions and will also have the opportunity to ask presenters a question.

Volume 2 will be available in the second half of the year and will include topics such as 'Improving EMI filtering' and 'Thermal considerations'.

www.vicoreurope.com/techtorial1

AWS GROUP INCREASES CAPABILITY OF SMT LINE

AWS Cemgraft, part of the AWS Group, one of the UK's independent Electronic Manufacturing Solutions (EMS) providers, has invested in an upgrade of its surface mount production line to handle large boards.

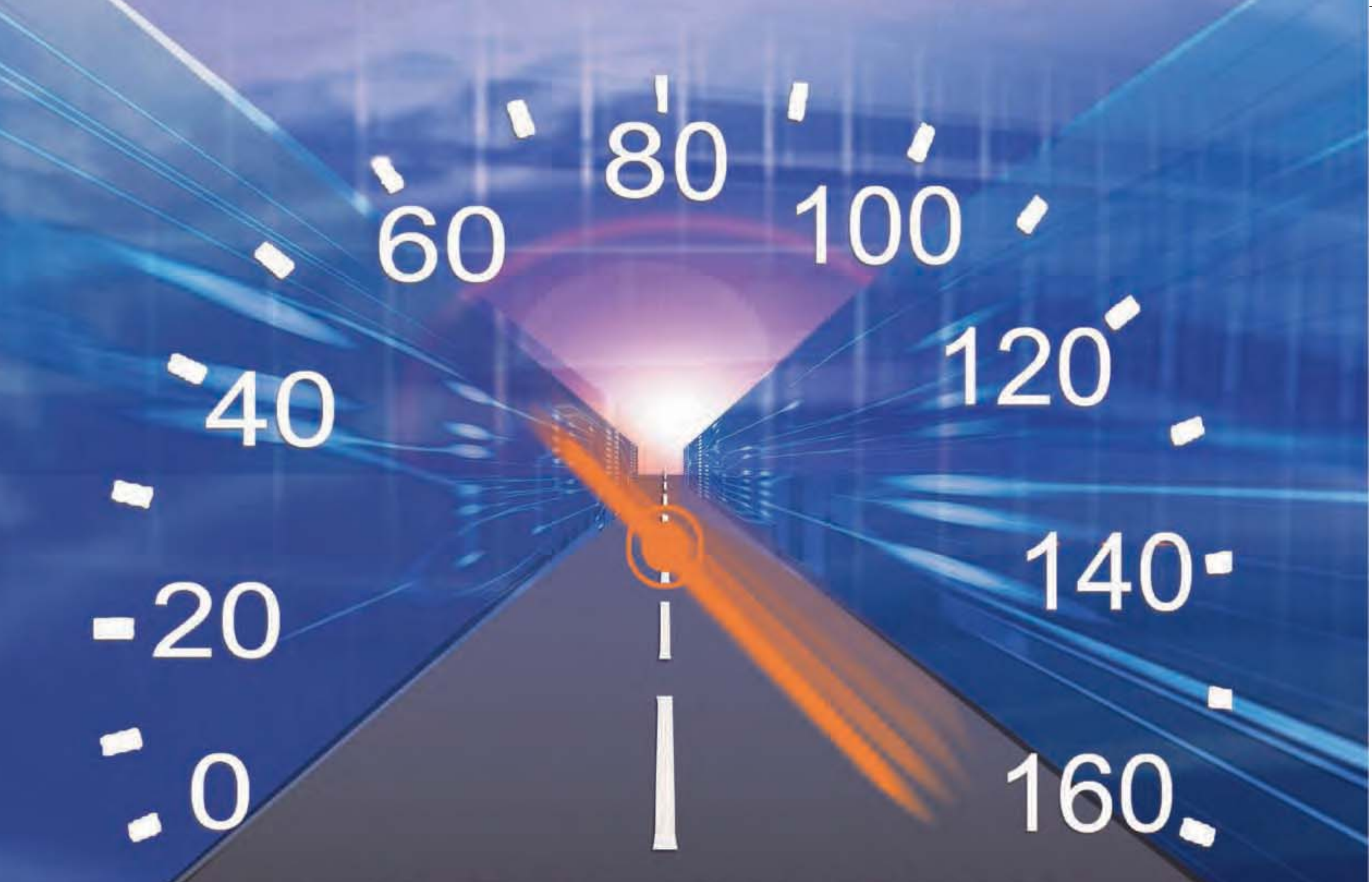
Cemgraft worked with surface mount assembly equipment maker, Juki Automation Systems, and reflow oven manufacturer, Heller Industries, to develop its automated line to handle boards measuring 663 x 145mm. The longest board that could be handled previously was 510mm.

"We try to work with our customers to ensure that their boards can be made on our automated production lines, rather than using batch production, which is slower and more expensive," said Jamie Maughan, Cemgraft Operations Director. "Sometimes, large boards can be accommodated by grouping all the surface mount components at one end of the board. However, in this case there was a high concentration of SMDs – BGAs, QFPs etc – all across the length of the board."

By changing the software and altering some mechanical hard stops, Juki modified its KE-2060RE high-speed, fine-pitch, assembly machine to enable it to handle boards up to 680mm in length. The Heller reflow ovens were also able to be profiled with a suitable temperature profile, and screen printing equipment enhanced ensuring that Cemgraft can offer a full production process.

Equally important is changeover time, which has been kept to just 20 minutes.

www.awselectronicsgroup.com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