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ELECTRONICS WORLD

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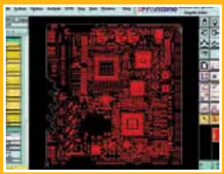
■ DESIGNING DEPENDABLE PRODUCTS WITH PPTC DEVICES

ENERGY STAR

POWERSOLVE'S NEW ENERGY STAR AC-DC POWER SUPPLIES

INSIGHT: REDEFINING DESIGN FOR CON-NECTIVITY



FOCUS NEW FPGA PACKAGES NEED INDUSTRY CULTURE CHANGE

PRODUCTS TRANSMITTERS, EMITTERS AND RADIO MODULES

ALSO IN THIS ISSUE: ON THE BUG HUNT • THE TROUBLE WITH RF • LETTERS

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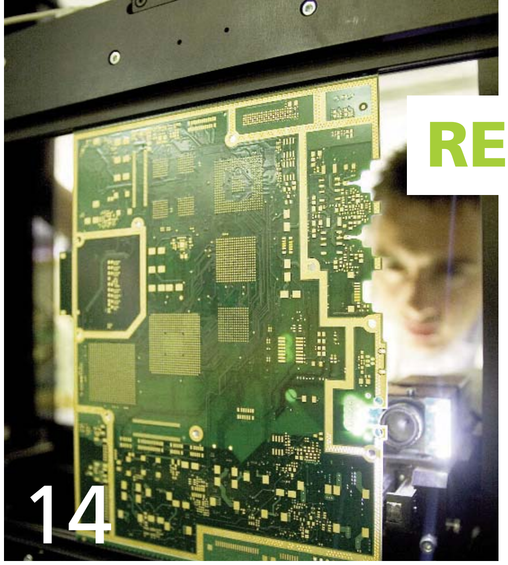

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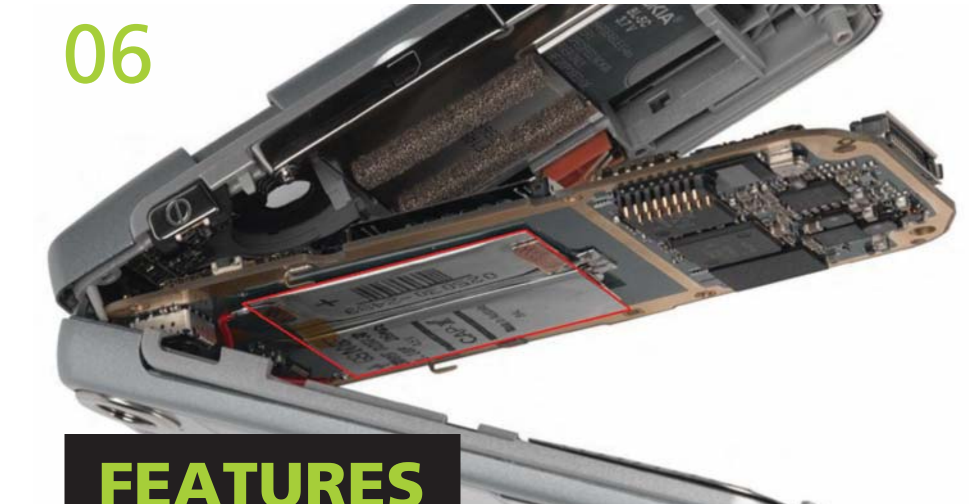

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Welcomed VC Fund for UK High-Tech Start-Ups

Discover **Powersolve**'s Energy Star AC-DC power supplies page 10

The UK's Prime Minister, Gordon Brown, last month announced the creation of a so-called 'UK Innovation Investment Fund' allocated for technology-based businesses with high growth potential. It is planned for the new fund to help grow small businesses, start-ups and spin-outs, in digital and life sciences, clean technology and advanced manufacturing.

Various departments, including the Department for Business, Innovation and Skills, the Department of Energy and Climate Change and the Department of Health, will invest £150m alongside private sector investment on an equal basis. It is the government's belief that this could lead to a private investment fund of up to £1bn over the next 10 years.

So, the government is trying to 'put money where its mouth is' and this is laudable. The UK needs to continue to be innovative and most importantly competitive, especially in certain sectors that are expected to prove lucrative in the near future. Venture capital finance has always been the lifeblood of innovation and crucial to ensuring the commercialisation of the discoveries coming out of a research base.

The US had always helped its own small businesses; more recently Taiwan, Korea and even China have been trying to support their own fledgling high-tech companies too, so it's high time that the UK did the same on a larger scale.

The action has been praised by many including Simon Walker, CEO of the British Venture Capital Association (BVCA), who said: "The BVCA is immensely encouraged by this venture capital initiative. The UK Innovation Investment Fund offers an exciting economic incentive for more than a thousand young venture-backed companies and the ideas and jobs which they represent."

It is also very apt to have such an initiative come at a crucial time such as now. Equally, it has been a difficult time for the VC industry so this fund is expected to underpin a next round of critically important fundraising for fund managers.

It is explained that the UK Innovation Investment Fund will operate on a so-called 'fund of funds' structure; this means that it will not invest directly in companies, but rather invest in a small number of specialist technology funds that have the expertise and track record to invest directly in companies.

All of this sounds very good and encouraging. We can only hope that for a small high-tech start-up it'll be easier to get money out of this fund than it is getting it out of a bank.

Editor
Svetlana Josifovska

CAP-XX CREATES AN SMT VERSION OF SUPERCAPACITORS

CAP-XX, developer of thin-form supercapacitors which deliver burst and back-up power in space-constrained electronic devices, has demonstrated prototypes of surface-mountable supercapacitors at its Lane Cove manufacturing facility in Australia. The company developed the SMT (surface-mount technology) devices to meet customer requests for supercapacitors capable of mass production assembly using standard reflow soldering techniques.

CAP-XX engineers sent several working prototypes of the SMT supercapacitors though a reflow oven at 260ºC. Before reflow, the thin, prismatic prototypes had ESRs (equivalent-series resistance) of 60 and 100 milliohms, capacitances of 1.0 and 0.5 Farads, and voltage ratings of 2.75 and 5.5V, respectively. The process had only minimal impact on performance, changing the ESR and capacitance by less than 10%.

"A high-power, surface-mountable supercapacitor with the CAP-XX characteristics of a thin, small form-factor has been the holy grail for the portable electronics industry, particularly mobile handsets," said Anthony Kongats, CAP-XX CEO. "The preservation of performance demonstrated in this trial meets the requirements of these customer groups."

CAP-XX is developing SMT devices to ease the adoption of supercapacitor-enabled power architectures in high-end feature phones and other consumer electronics devices. Current CAP-XX devices are manually soldered onto the PCB (printed-circuit board).

"Supercapacitors will soon become a key component in mobile computing products," said Craig Mathias, a principal with Farpoint Group, an advisory firm specializing in wireless networking and mobile computing. "A supercapacitor handles the large instantaneous power demands of flash photos, audio, video and wireless transmissions, maximizing battery life and enabling the use of smaller batteries. Given ever-increasing demands on battery power from higher clock rates and greater functionality, the supercapacitor is about to take centre stage in mobile-power applications."

This phone has 1.2mm thick dual-cell supercapacitor to enable the BrightFlash feature; soon mobile phones will carry SMT supercapacitors too

Mathias continued, "CAP-XX's SMT capability is an impressive development from a leader in the supercapacitor space."

CAP-XX supercapacitors store charge on nanoporous carbon electrodes on aluminum foil, arranged in multiple layers and connected in parallel to minimize resistance and maximize capacitance. This packs the highest energy and power densities possible into thin (0.9 to 3.8mm), prismatic packages.

The company did not disclose expected availability for its SMT devices.

Transatlantic Co-Operation Leads to Major Scientific CMOS (sCMOS) Technology Breakthrough

Scientists from Andor Technology (Northern Ireland), Fairchild Imaging (United States) and PCO (Germany) pooled their resources and expertise in developing Scientific CMOS (sCMOS), a breakthrough technology based on next-generation CIS design and fabrication techniques.

"This announcement is a great moment for all three companies, who have come together in a true spirit of commitment to reach a shared goal," said Fairchild Imaging's Colin Earle.

sCMOS is poised for widespread recognition as a true scientific grade CMOS image sensor (CIS) technology, capable of out-performing most scientific imaging devices on the market today. As such, CIS technology may become the global detector platform of choice for scientific photonics applications that require world class performance in the fields of sensitivity, speed, dynamic range, resolution and field of view.

"We have reached a 'leap forward' point, where we can confidently claim that the next significant wave of advancement in high-performance scientific imaging capability has come from the CIS technology stable," said Dr Colin Coates of Andor Technology.

Unlike previous generations of CMOS and CCD-based sensors, sCMOS simultaneously offers extremely low noise, rapid frame rates, wide dynamic range, high quantum efficiency (QE), high resolution and a large field of view.

Dr Gerhard Holst, PCO, said: "Scientific CMOS (sCMOS) technology stands to gain widespread recognition across a broad gamut of demanding imaging applications, carrying an advanced set of performance features that renders it entirely suitable to high fidelity, quantitative scientific measurement."

Current scientific imaging technology standards suffer limitations in relation to a strong element of 'mutual exclusivity' between performance parameters, where one can be optimized at the expense of others. sCMOS can be considered unique in its ability to concurrently deliver on many key parameters, whilst eradicating the performance drawbacks that have traditionally been associated with conventional CMOS imagers.

'Digital Britain' Meets Mixed Reaction from Companies

On 16 June the UK government published the 'Digital Britain' Report, in which it outlines its strategic vision for ensuring that the UK is at the leading edge of the global digital economy.

The report provides actions and recommendations for the Internet, radio, television, local media and broadband for the forseeable future.

It's been a mixed bag of reactions by various firms. For example, Imagination Technologies, a UK-based provider of digital radio technology, confirmed its support for the digital migration of radio by 2015.

"Digital Britain confirms a strong and clear future for digital radio in the UK and, critically, provides the industry with the concrete timetable necessary for planning technology and product roadmaps with confidence," said Hossein Yassaie, Imagination Technologies's CEO.

Frontier Silicon, a supplier of DAB digital radio semiconductor solutions, also welcomed the digital migration of radio. The company, which supplies the technology for the majority of digital radios sold in Britain, anticipates a three-fold business increase in annual shipments or sales over the next three years as a result of the proposals contained in this report, which favours DAB as the preferred platform for future radio broadcasting in the UK and calls on a commitment from the car industry to facilitate digital switchover by means of a five-point plan.

In the UK, around a third of all households already have digital radios. In-car adaptors alone have increased the in-car digital radio market by 300% to date.

Recent announcements from France, Germany, Denmark and Eastern Europe, and the formal launch of DAB digital radio in Australia, mean that the global market for digital radios and digital radio technology is due to take off. Anthony Sethill, Chief Executive of Frontier Silicon, said: "The recommendations contained in the final Digital Britain report come as the digital radio industry continues to grow apace, with digital radio now accounting for over 20% of all listening, DAB volume share now at 25% of sales for the first time and with UK DAB radio ownership – up 17% year-on-year during the first quarter of this year – now at one third. We expect that the UK lead in digital migration will act as a catalyst for other European markets to follow suit".

However, some criticised the 'Digital Britain' Report, which holds plans that will see the UK stuck in the past, according to Richard Heap, Head of Telecoms at BDO Stoy Hayward.

Confusing state of the Digital Britain report?

"Despite being widely criticised in January for only committing to a broadband network speed of 2Mbps by 2012, Lord Carter has gone ahead with plans to provide Britain with outdated technology at a speed akin to a snail's pace. This is even more frustrating when other countries, such as South Korea, are committing to universal speeds of up to 1Gbps by 2012, which is 500 times faster," said Heap.

"To add insult to injury, Carter has said he's going to tax every phone line in the country £6 per annum to fund this inaptly named "next generation" network. Especially as an Ipsos Mori poll has shown that 43% of people wouldn't use broadband even if they had access to it. This clearly begs the question of where resources should be allocated – surely in quicker broadband rather than trying to meet the Universal Service Commitment?"

■ DuPont Displays has developed a third generation (Gen 3) organic light emitting diode (OLED) technology, which has led to substantial performance gains for printable OLED light-emitting materials. A DuPont Gen 3 green OLED material achieved a record lifetime of over 1,000,000 hours, while two new Gen 3 blue materials have been developed that set new standards for longevity and colour. Gen 3 OLED materials can meet or exceed the performance of today's vapour deposited materials and are paving the way for lower cost solution process OLED displays.

"With lifetime five times better than just two years ago, these new materials will allow solution OLEDs to be used in mobile displays, and also to begin to penetrate the television and general lighting markets at a lower cost than today's evaporated OLED technology," said William Feehery, global business director at DuPont OLED Displays.

■ RTX and SiTel have jointly created a new innovative Ultra Low Power (ULP) technology based on CAT-iq, opening doors to new applications for DECT/CAT-iq.

The firms developed an innovative battery management algorithm to obtain a considerable reduction in power consumption. ULP technology targets not only cordless phones but battery-powered devices in general.

A central feature in the ULP technology is interoperability with the existing DECT/CAT-iq infrastructure, since this will open up a completely new world of opportunities in which ULP devices can be connected to the Internet or LAN through for example a CAT-iq enabled gateway or IAD. Among the new applications are door bells, smoke alarms and point-of-sale terminals among others.

■ Five countries engaged with Digital Multimedia Broadcasting (DMB) have established an organization that will support mobile TV services via DMB and related services. International DMB Advancement Group (IDAG) currently has members from the Netherlands, Norway, Great Britain, Malta and Italy.

IDAGs goal is to promote TV, radio and data services via DMB, DAB and DAB+, but also enhanced functionality via other networks, such as 3G and WLAN. The group focuses on creating a bigger pan-European market for DMB terminals through purchasing partnerships, collaborations with other companies and organizations, coordination of technical solutions and creating successful business models.

GREEN SHOOTS OR A DESERT?

Malcolm Penn is CEO and chairman of market analyst firm Future Horizons, based in the UK

WHILST MUCH of the current industry tittle-tattle focuses on the ‘green shoots of recovery’ debate (‘are there/aren’t there green shoots?’), as well as the ‘shape of the downturn’ – V, U, W, sharp, stretched, extended, etc – we prefer to take a more sober look at the underlying trends.

As mentioned in our May Global Semiconductor Report, at -24.2% growth Q4-08 was a little worse than our 22.5% January IFS forecast, whereas Q1-09’s 15.5% fall was slightly better than our -18% number. The counterbalancing overall effect of the two was to put the 2009 market slightly ahead of our official -28% forecast, to -25.3%. In our book, this does not constitute a forecast revision, given that the basic forecast assumptions and analysis had not changed; it was merely fine-tuning the number. So far, so good!

However, Q2-09 might well be different in that it now looks to be coming in with growth in the 4-5% range versus our -2% January estimate. If true, this would represent a material change to our 2009 forecast, improving it from -28% to -21.3%, assuming that the second half of the year rolled out as planned and removing most of the downside risk potentials.

But what is actually going on in the markets? The first quarter was clearly a difficult time for the industry with the combined effect of the global recession on top of the normal Q1 seasonality weakness. Not quite a knockout punch, but a real double-whammy. Based on a reasonable cross-industry sampling, the overall result was a net 12% fall in electronic equipment sales versus Q1-08.

Aside from government/military, which was the only sector to grow, every market and geographic region was negatively impacted, with Japan and Taiwan/China the worst hit, even though the latter is the first to show a rebound.

Looking at the key mobile and PC industry sectors, both of these have been hit badly by the discretional consumer spending slowdown, with Q1-09 phone and PC unit sales down 16% and 20% respectively, versus Q1-08. Given the magnitude of these declines (all markets, sectors, regions, customers, consumers and enterprise), the industry and chip market exited the first quarter in remarkably good shape, relatively speaking. That is not to say it will be plain sailing hereon out, far from it, but that the industry has clearly weathered the worst of the storm, bloodied but (mostly) not beaten.

The 12%, 16% and 20% OEM, mobile and PC sales declines are key industry benchmarks in that they represent the absolute worst-case full-year scenarios. Our January 2009 forecast called for 8.2%, 15% and 22% declines here respectively, which are all well in line with the way the market is unwinding. Given we expect the Q1-09 12:12 declines to improve as the year rolls out, the downside risks to our forecast are clearly diminishing.

From an economic perspective, our 8.2% electronic equipment industry decline was based on the then IMF’s World GDP growth forecast of +1.8%. This, however, has been subsequently revised down three times, first to +0.5% on January 28, then to -0.5 to -1.0% on March 13, to the current forecast of -1.3% in the April 2009 World Economic Output Report. Intuitively one would worry that these downward revisions ought to force a corresponding revision to the electronics equipment market; in reality this does not seem to be the case. This in turn begs the big unanswerable questions: “To what extent are these downward revisions to world GDP growth the cause or effect of the electronic equipment industry decline, and what impact will their downward revision (and for that matter subsequent recovery) have on the 2009 and beyond electronic equipment industry absolute growth number?”

“ASIDE FROM GOVERNMENT/ MILITARY, WHICH WAS THE ONLY SECTOR TO GROW, EVERY MARKET AND GEOGRAPHIC REGION WAS NEGATIVELY IMPACTED”

The bottom-line answer? No one actually has the faintest idea; furthermore, it is impossible to calculate. Whilst anecdotally and intellectually there is an obvious link between GDP and the electronic equipment industry growth rates, the electronic equipment industry represents only 2-3% of total world GPD. In contrast, at their peak, the financial derivatives markets totalled 120% of world GDP.

With recession, cutbacks clearly hit the electronic equipment industry early, as both enterprises and consumers hit the 'stop spending' button relatively quickly. In the case of the 2008 downturn, for 'relatively quickly' read 'instantaneously fast'. The impact on the chip market is immediate, aggravated by the associated component and WIP inventory burn, with overshoot inevitable.

Inventory levels clearly stabilised during Q1-09 and are being rebuilt in Q2, most probably targeting an electronics equipment production level 12% down on this time last year, i.e. in line with first quarter actual. This being the case, the industry will have adjusted much faster than in previous cycles, with today's inventory imbalance levels already peaked and much more in line with the 2H-06 'course-adjusting' excess than the post dotcom bubble burst 2001 flood.

To summarise, the downside risks to the 2009 market are clearly abating with our 13% third quarter growth forecast still looking reasonably robust, given the current inventory rebuild plus a touch of seasonal strength. Likewise, it is still credible for this to be followed by a seasonally weak 3% forth quarter growth, given the normal end-of-year inventory clean-out.

With the global economic recovery then starting to gain traction in 2010, a 'normal' quarterly (-2%, +2%, +14%, +3%) 2010 growth pattern would be reasonable, yielding a 2010 annual growth of around 17%, well in-line with our '15% with lots of upside potential' January 2009 forecast.

Whilst the slightly revised 2009 quarterly growth pattern would call for an (upwards) formal forecast revision to the actual 'growth number', the underlying market analysis and assessment presented at our January 2009 Forecast Seminar will not have materially changed, either for 2009 or 2010.

Malcolm Penn and his colleagues will be presenting the Future Horizons's Mid-Term Industry Forecast Seminar in London on the 21st of July.

Malcolm Penn can be contacted at mail@futurehorizons.com. Future Horizon's website can be found at www.futurehorizons.com

Energy Star AC-DC power supplies meet growing demand

Responding to the growing demand for power supplies that have low power consumption when connected to the mains supply, but not in use, Newbury based Powersolve Electronics has just announced the introduction of a very wide range of Energy Star power supplies. The PSG40-60ES Series, as shown on the front cover, are low cost external AC-DC power adaptors that are available in power ratings of 40 Watts to 60 Watts with single output voltages from 9V up to 30V DC. Input is universal 90-264VAC 50/60Hz, which enables them to be used with any worldwide domestic mains supply. Their standby power consumption of less than 0.5 Watts meets Energy Star and CEC requirements. Efficiency is around 85% and the power supplies are housed in compact, sealed, desk top plastic cases with 3 pin IEC320 C14 input connectors. Output is via a 1.2 metre flying lead with 2.5 x 5.5 x 11mm DC power connector, though other types of connectors are available on request. All versions have full UL, cUL, TUV EN60950 & Chinese CCC safety approvals and conform to EN55022'B', CISPR22'B' and FCC Part 15 B for conducted and radiated emissions.

Other external, desk top Energy Star and CEC rated power supplies are the PSE Series which are available in power ratings from 15 Watts to 130 Watts and with DC outputs from 5V up to 48V DC.

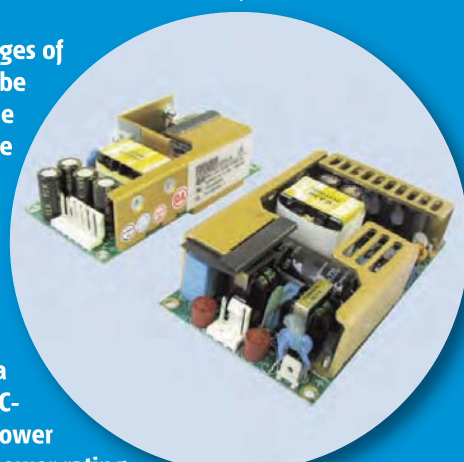
Again all models have universal 90-264VAC 50/60Hz input and models up to 25W can have optional IEC320 C8 2 pin input connectors as well as the standard IEC320 C14 3 pin versions. All models have full safety approvals (some models also with medical approval) and conform to current conducted and radiated emissions requirements.

Also available in the very near future is a new range of 24 Watt wall mount plug top power supplies that also conform to Energy Star and CEC requirements. These products have interchangeable AC plugs for use in UK, Europe, America and various other countries. Inputs are universal 90-264VAC 50/60Hz and outputs are available from 3V to 24V DC. These products also carry full safety approvals for both ITE and Medical safety requirements.

On the horizon are a range of single output 60 Watt, 100 Watt and 200 Watt open frame power supplies for use internally within customers' equipment, which will also conform to Energy Star & CEC. These have been designed because we are seeing a demand for low standby energy not only in external power supplies, but also with customers wanting to design this feature into their next generation of products.

The 60 Watt versions are on a standard 2 x 4 footprint and these will have both ITE and Medical approvals and the 100 Watt and 200 Watt versions will be on an industry standard 3 x 5 inch footprint.

Single output voltages of 5V up to 48V DC will be available and as is the norm they will feature 90-264 VAC input, with Power Factor Correction as standard on the 200W version.



Powersolve provide a very wide range of AC-DC, DC-DC & DC-AC power products ranging in power rating from 1 Watt right up to 22 kWatts. In addition we supply on-line, true sine wave UPS Systems from 1kVA up to 6kVA. We hold around £1.5 million of stock in our warehouse in the UK and have manufacturing facilities in China. With over 20 years experience of supplying power products to the UK market there is rarely a requirement that we cannot find a power supply for. For details of our vast product range please go to www.powersolve.co.uk.

Why STOP at One?

Myk Dormer

TO START THIS article I must declare a preference: I like simple microcontrollers. I like low pin-count, unsophisticated low power devices. Processors with no more than a few thousand words of code space that you can program in assembler and hold the whole algorithm in your head at once, without your brains leaking out.

I appreciate that there is an absolute need for highly complex, high performance devices with hundreds of pins and GHz clocks. After all, I'm writing this article on a desktop PC, and I'll soon be sending it as an email attachment, but in the niche area of low power radio design, the simpler part is usually sufficient.

In the design of a wireless module, the firmware is only required to perform some very limited tasks, such as frequency synthesizer PLL programming, transmitter power on ramp generation, maybe some data formatting and so on. Things get more "interesting" however, when the job extends into the 'user application' arena.

"EFFICIENT DECODING OF A BASEBAND DATA STREAM REQUIRES CONSIDERABLE CPU EFFORT, ESPECIALLY IF A BI PHASE RATHER THAN EDGE DETECTING DECODER IS USED"

At this point things can become very much more complex, very fast. Low power radio applications cover a vast array of different tasks, and the 'user processor' can be called on to perform many different operations: data stream coding, decoding and buffering – effectively 'modem' functions; power switching; analogue or digital input handling, from a variety of possible sensors and transducers; motor control tasks; battery maintenance tasks … the list goes on.

To take a simple example, consider a radio controlled 'toy' tank chassis. In the simplest case this is just the remote control of two DC motors. To give smooth handling and realistic maneuvering, the motor control will need to be proportional. At the transmitter, input from a joystick will need to be interpreted.

Conventionally, one might consider lumping all the control functions together in a single processor. At the transmit end, this is reasonable: two A/D channels and a simple data burst formatter is no great strain on even a simple processors. At the receiver, however, things are more problematical. There are several processor-intensive tasks required simultaneously. Efficient decoding of a baseband data stream requires considerable CPU effort, especially if a bi phase rather than edge detecting decoder is used, while the PWM control of a DC motor is another processor effort-hog.

To realise these functions in a single processor will either require specific peripherals (some controllers include hardware motor control, or data interface, hardware), which limits choice of processor type, or will require considerably more processing power to be able to fulfill the decoder and PWM control tasks in parallel, which in turn will push clock speed up.

Sharing processor resources between multiple tasks is, in itself, a potentially difficult task. It requires complex coding, multiple interrupts and, possibly, the use of an RTOS (real time operating system) to support the multiple concurrent tasks, which by then will be complex enough to need to be coded in a high level language. This, in turn, requires yet more processing power and memory space.

The alternative is to identify the individual tasks (decode baseband data output from radio receiver, PWM control of left track-motor, PWM control of right track-motor) and dedicate a very simple processor to each task. The result is a three processor design, but one where each of the individual firmware functions is much, much simpler.

This is admittedly a very simple example, which a competent software engineer could actually code into a single processor without too much sweat, but it serves to illustrate the problem. With the addition of multiple control functions, the software complexity of a control processor can very rapidly spiral out of control, and a cost and power critical task can start to look as if it needs an industrial PC.

The alternative to a complex single master CPU is a multiple processor system. This is not a new idea and is implemented in many industrial control applications already, most particularly in the automotive and aviation industries.

What I am specifically proposing is to divide the task up between a larger number of very simple processors at a much lower level than is usually done, before any one processor is required to handle more than a single job, or needs more than a few hundred words of assembly code.

As individual processor tasks are simpler, the data flow needed to any particular device ought to be proportionally lower, so allowing a simple low speed serial inter-processor bus (I favour simple asynchronous serial protocols, but synchronous methods like I2C are just as applicable) with dedicated higher speed data-links to especially data-hungry sub functions if required.

The processors indicated for these distributed tasks are parts with between eight and twenty pins, and unit costs of around £1 or less. Beyond the basic CPU and memory, only a hardware communications device (UART, SPI or similar) is really vital, and that is only to relieve the firmware of the need to handle concurrent communication and primary function tasks. Typical control functions such as PWM motor control or pulse-coded servo handling can be easily coded in simple assembler routines, keeping one function per processor to minimise software complexity.

This approach goes against the current trend towards high level software applications, running on increasingly powerful platforms. By comparison this method can seem primitive, but it has some significant advantages:

1. By running each control function on its own processor (once the inter processor communication bus has been defined), it is easy to develop and test the functions in isolation. In a large project, the tasks can be efficiently split up between team members.
2. Each individual task is, in software terms, very simple. Extensive debugging with expensive tools should be unnecessary, and the likelihood of a hidden bugs cropping up is reduced.
3. Functions are re-useable in future projects. A developed control task and its processor can be treated as a component for new designs. Expanding an existing design is also simpler, as it's easier to add another device to the bus than to modify an already complex 'master processor' design.
4. Each individual processor is a low power, low-speed device. RF interference issues are minimised and power consumption is kept low (processors can even be switched completely off until needed).
5. In a physically large project, the interconnection between different elements is reduced to power supplies and the low-speed bus signal; this is much easier than trying to route multiple transducer inputs and control output cable skeins to and from a main processor card.

This method is not a panacea and it has obvious limitations as the volume of control data increases or response time requirements become more critical, but it is well worth considering as a simpler, less expensive, greener alternative to the obvious "wire everything to an industrial PC card and write the application software in C+" solution.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd ***www.radiometrix.com***

REDEFINING DESIGN FOR CONNECTIVITY

Marcelle Douglas, technical editor at Altium, points out that it's time to shape the tools used in design with a unified approach to create a level of support needed for the emerging trends in electronics systems

WHAT WAS ONCE reserved ten years ago for mission critical applications and science fiction is now an essential part of many consumer and industrial applications. Digital communications and computing power are quickly expanding connectivity in the world, exploding past conventional technology boundaries. Our engineering challenge now is how to create device intelligence with this forward view to connectivity in mind.

What does this type of development mean for designers who want to innovate and edge ahead of the competition? Finding new ways of designing electronic products, sub-systems and embedded systems that go into machines or devices that are then connected to larger eco-systems needs to be the primary focus of development teams. An implied requirement of being able to deliver these kinds of systems is to use state-of-the-art design solutions that unify the development process instead of just focusing on managing complexity.

Such development environments must be strategically designed for the device intelligence and connectivity to offer the most advantages for engineers. Redefining how we view the design process as a whole for real collaboration is the crux move.

Designing electronics isn't straightforward anymore. Unfortunately, most design solutions are static, antiquated collections of point tools. Ironically, they haven't experienced the same unprecedented rate of change as the designs they are used to create. Yesterday's solutions aren't enough and the benefits of using current design methodologies are reaching the point of diminishing returns. More is needed than just adding feature sets and vendor-specific approaches that just push the details around.

Let's face it: engineers now should have to think less about low-level details they don't need to see so they can focus more on core functional intelligence and connectivity. This is where the real value is. For example, being able to create device intelligence and connectivity would be better served with a raised level of abstraction in the design environment. Larger systems can then be tackled in new ways without extending development time. Added technologies then, such as real-time concept exploration and modelling, would be more effective.

And it doesn't stop there. Today's designs require implementation flexibility down to the lowest levels of detail. An environment that offers reconfigurable programming linked down to the hardware implementation would be a huge advantage. This would allow algorithmic exploration at the physical level for even the most challenging system architectures. Higher level abstraction and design automation can be harnessed because designers can mix their approach to hardware and software. They won't need to fabricate hardware to support the design functionality or think about it as much. There is no longer a need to 'fix' the design of a hardware platform before the software development can begin. Workflow analysis to identify where bottlenecks occur and design reuse can be performed easier because instant validation is always available.

DESIGNING ELECTRONICS ISN'T STRAIGHTFORWARD ANYMORE; UNFORTUNATELY, MOST DESIGN SOLUTIONS ARE STATIC, ANTIQUATED COLLECTIONS OF POINT TOOLS

The end result is real-time design collaboration with the mechanical and physical world. Designers can interactively adjust board layout, component placement and even component package choice to suit proposed enclosure designs. They can ensure that the PCB complies with mechanical clearance constraints – tested directly against the real enclosure design – all before the board is sent for prototyping or manufacture. Collaboration with team members is also easier because everyone has a singular view of the design's data model.

Hardware and software co-design then plays a fundamental part in gaining the upper hand with today's complexity. While many tools focus on improving capacity and engine performance, they miss the mark on unifying all the various domains of electronic design. There often isn't a built-in detection for a wider range of design issues. This is a symptomatic solution when what is really needed is a systematic one.

There is a correlation between the ease of being able to specify, implement and verify the aggressive intelligence and connectivity requirements of high speed designs and having a unified approach. Only when the barriers are removed and the design approach is unified is it possible to create the level of support needed for emerging trends like intelligence and connectivity. It's time we shape the tools we use rather than be shaped by them. ■

BRAVE NEW WORLD

While the more widespread adoption of complex FPGA packages is one of the most exciting developments in the electronics market, an industry culture change is needed to deliver new generation FPGA packages, says Mike Devine, NPI technical manager at Exception PCB

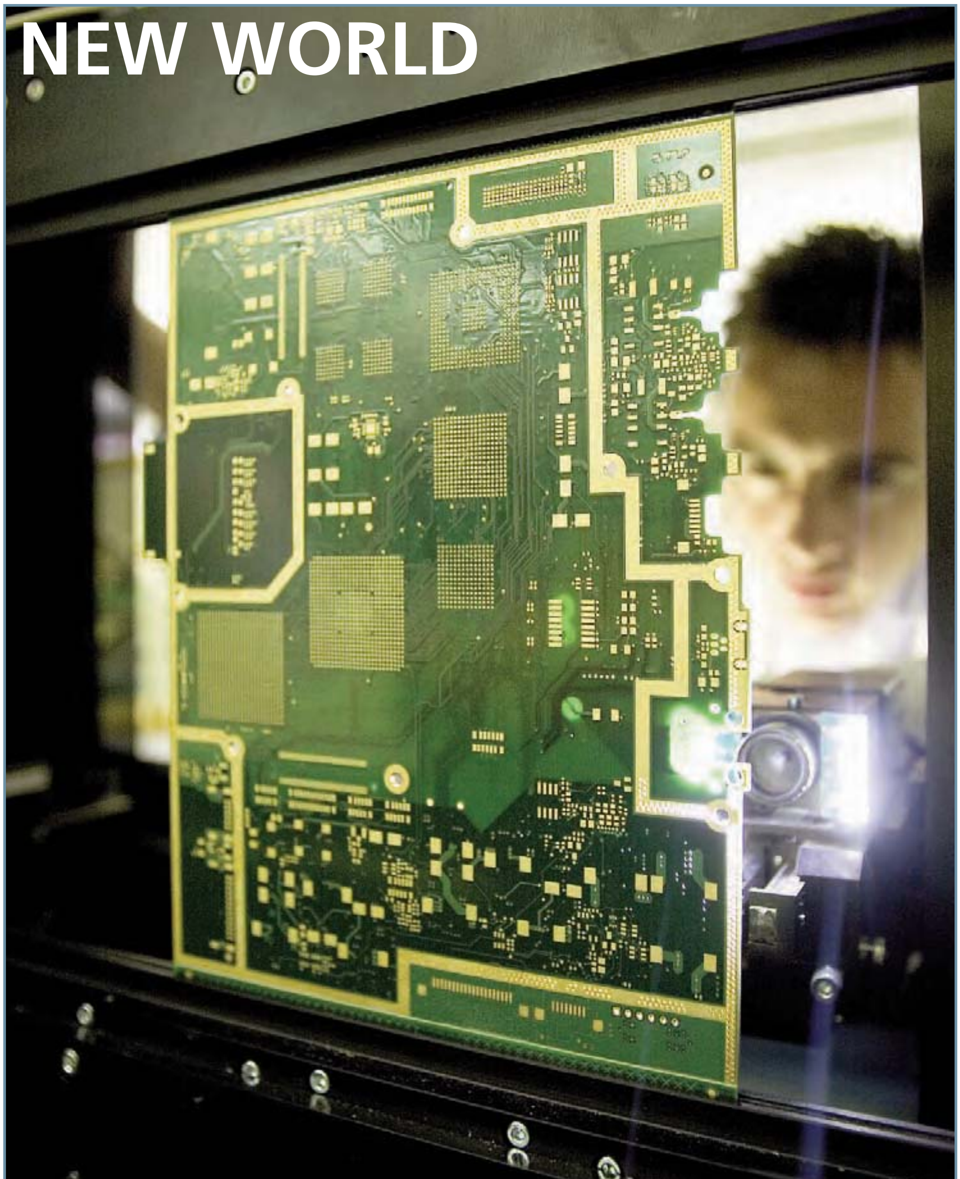


***Figure 1:** Exception has invested significantly in test equipment to keep up with the demands of FPGA development*

THE MANUFACTURE of micro BGA (ball grid arrays) with a higher number of interconnections per board has been a trend in electronics manufacture for some years and the use of such devices on a large scale – with components such as FPGAs (Field Programmable Grid Arrays) – continues to increase in popularity due to their performance. While this development creates exciting opportunities for designers and manufacturers, it also presents the electronics industry with several serious issues, specifically in the areas of skills development, liaison between designers and fabricators and emerging technological processes.

Not so long ago, the development of one FPGA per board was a major challenge. Companies like Exception are now increasingly asked by chip manufacturers for several high density FPGAs per board. "The big challenge in the sector at the moment is being able to consistently produce complex products utilising ever decreasing features and real estate on a scale never seen before," says Mike Devine, NPI technical manager at Exception PCB. "Clearly, the adoption of this new generation of PCBs to create truly flexible FPGAs that bring even greater processing power is a big challenge."

There are a number of issues of a technical, design and commercial nature that must not be ignored. While PCBs have previously been seen merely as a way of connecting electronic components together, within the FPGA environment they play a much more active role as an electronic function. Functional integrity is of great importance here. "This flexibility is at the very heart of what makes FPGAs so attractive to OEMs – the fact that they can be taken to market quickly and programmed at low cost after the manufacturing stage is finished," said Devine. "This new generation of highly sophisticated PCBs is bringing about function integrity and bringing even greater power to FPGAs."

Devine is confident that the manufacturing capability now exists – through the use of tried and tested HDI, flat pad and microvia tower processes – to manufacture a new generation of PCBs that will surpass the expectations of the major chip makers. For example, in the last few weeks Exception has taken delivery of a state-of-the-art laser drill machine, a Process Photonics, ProVia H, which provides the capability to laser ablate down to between 30 and 50 microns in size. Previously, the company was able to go down to between 50 and 150 microns, so this is a major development in technical capability for Exception.

"To complement the new machine we are using much thinner dialectic pre-preg – basically the bonding agent between layers – which is a thinner and flatter weaved material that is used in conjunction with thin copper foils of between 5 and 12 microns," said Devine.

Companies are also beginning to use megasonic plating to achieve even deeper and smaller microvias, which are central to the development of robust and efficient FPGAs. Exception is one of them and it is currently working closely with a number of universities to perfect the plating process that can reduce the number of sequential bonds required, thus cutting out some of the processes to reduce the cost and lead time of production.

Although technical excellence is central to the successful delivery of FPGAs, that's not the whole story, according to Devine, who believes that better integration with software developers is crucial.

"There are now software developers that are now creating programmes that simulate hardware performance through PCBs, which brings about a whole new function for the once humble PCB," he said.

Increasingly, this means that design engineers need to think about the specific PCB requirements far earlier in the planning process than ever before. "In the past, PCBs were seen as an off-the-shelf item that could be added into a design towards the end of the process. These new developments change the rules of the game, so that design engineers must now introduce PCB architecture in their design, which is a major cultural shift for them," added Devine.

"The problem we face is that technology has once again moved more quickly than PCB design software and the way design teams work. Also as there are no university or college modules looking at this topic, there is little real understanding of PCB design within the electronics manufacturing community and no immediate prospect of students coming into the jobs market with knowledge of this specialist area."

With greater sophistication also comes greater cost, which is another key issue that needs to be hot wired into OEMs' planning before the silicon package is developed on a larger scale. It has to be ensured that as an industry each party is talking to the other at every stage of the development chain to ensure functionality and a technology that is affordable. With this knowledge and understanding of the FPGA package size (and available real estate) firms can make strategic decisions on the most practical fabrication process from the outset.

Equally, cost analysis needs to become a more commonplace topic in design departments, with design engineers working far more closely with marketing departments to agree budgets to ensure the ends product brings both performance and value.

"To achieve a lower cost that helps to secure more market share, PCB designers are

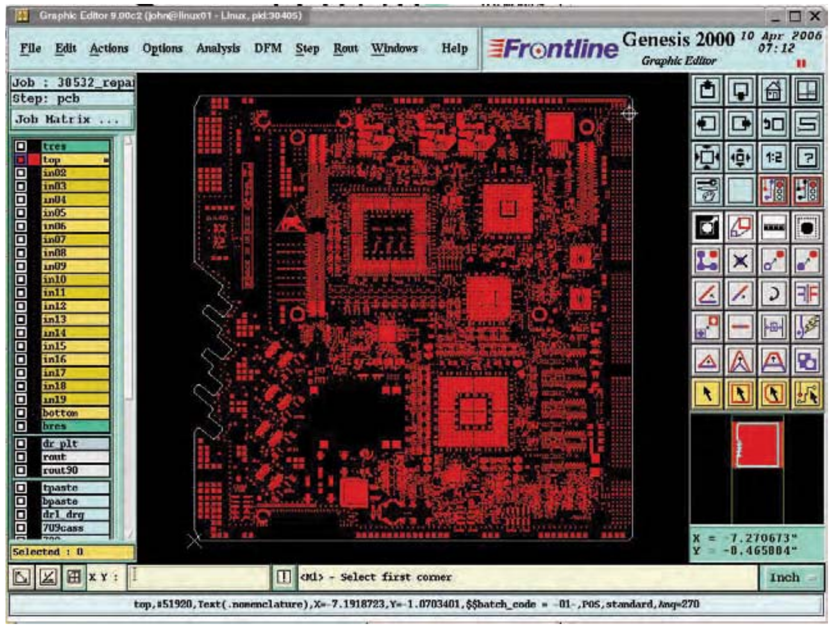


Figure 2: *Software designers and fabricators need to work more closely to deliver the full potential of FPGAs*

under pressure to develop boards using traditional 'fan-out' techniques. As FPGAs are growing in size, with more and more interconnects, the challenge is to achieve performance of the board, at a lower total cost," said Devine. "It's all about getting the balance between relevant technology options and finished product cost.

While the use of HDI techniques has been

DESIGN ENGINEERS NEED TO THINK ABOUT THE SPECIFIC PCB REQUIREMENTS FAR EARLIER IN THE PLANNING PROCESS THAN EVER BEFORE

pioneered by Exception to accommodate the fan-out of multiple devices, its innovative use at its Tewkesbury plant has also seen the support of hardware to functionally test to evaluate micro-BGAs. This is a technique that was never previously considered possible in the manufacture of larger I/O packages such as FPGAs.

Exception has invested in flying probe test equipment, which is seen as a vital part of the quality process. Typically when testing a finished PCB, the traditional way was to use what is known as a 'bed of nails', a tried and tested quality process. But as devices are becoming so small, flying probe machines are increasingly used to take testing down to the 0.4 pitch BGA level. The latest ATG Soft Touch test machines enable firms like Exception to take geometries down to 0.2 pitch BGA.

In addition, track and gap test technology that can do down to sub 50 microns as some wire bonded boards are on geometries of 50-75 microns, containing tracks that cannot be tested by more traditional test equipment.

New developments in the areas of silicon etching within the silicon fab world continue to push density, with packages being talked about as small as 40nm. This also makes it possible to transfer PCB thinking across into FPGA design.

Despite the constraints that the electronics sector faces at the moment, in terms of global demand for products, the skills gap and the technical challenges facing PCB manufacturers, Devine is confident that the growing sophistication of FPGAs is a trend that will continue.

"Even in the teeth of a recession, this new generation of PCBs will continue to find new applications. The potential use of this essentially different nature of PCB is significant. We see significant growth prospects for this technology in the next five years, especially from the communications, medical and defence sector," he added. ■

Adaptive Differential Pulse Code Modulation Using An AVR MICROCONTROLLER

Muhammad Yasir discusses the Adaptive Differential Pulse Code Modulation (ADPCM) compression and decompression algorithms, their performance and practical implementation using an 8-bit ATmega8535 AVR microcontroller

EFFICIENT AND simplified speech processing algorithms like Adaptive Differential Pulse Code Modulation (ADPCM) and enhanced features of microcontrollers have made it possible to add sophisticated and complex speech processing capabilities to any 8-bit AVR microcontroller.

Analysis of speech samples, obtained from an analogue-to-digital conversion process, reveals that a high correlation is found between consecutive speech samples. The ADPCM algorithm takes advantage of this high correlation property of speech data. This algorithm does not encode the actual speech samples. This algorithm actually encodes the difference between a predicted speech sample and the actual speech sample. This speech encoding provides an efficient compression with a significant reduction in the number of bits per sample.

The quality of speech signal is also significantly preserved by this speech processing algorithm. The practical implementation of ADPCM algorithm discussed in this article is based upon Interactive Multimedia Associations (IMA) recommended practices for enhancing digital audio capability in multimedia systems revision 3.00.

The IMA ADPCM Reference algorithm, upon which this article is based, has significantly reduced the mathematical complexity of the original International Telecommunication Union (ITU) Family G.721 ADPCM algorithm, by simplifying many operations and using the lookup tables where appropriate. The IMA, the Digital Audio Technical Working Group, is a trade association which includes technical representatives from different companies like Compaq, Apple Computer, Hewlett-Packard, Intel, Microsoft, Sony, Texas Instruments and others. This association is working towards developing standards for high-quality audio data exchange between computing machines. The speech compression and decompression algorithms discussed in this article were implemented by Rodger Richey of Microchip Technology on an 8-bit PIC microcontroller. The algorithms and idea have been taken from an article by Rodger Richey of Microchip Technology. Unlike Rodger Richey's article however, this article discusses implementation of speech compression algorithm on 8-bit AVR microcontroller, while decompression algorithm is implemented in Turbo C on PC side.

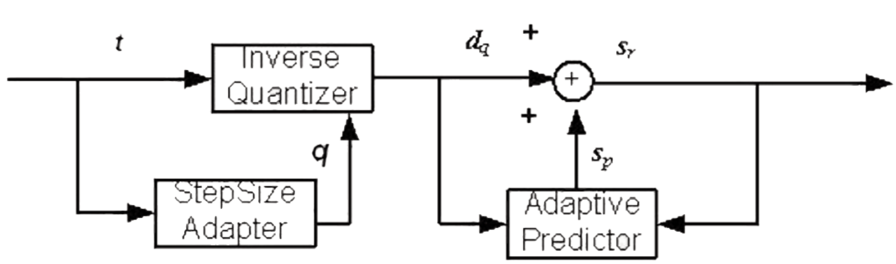


***Figure 1:** ADPCM encoder block diagram*

Compression

The input signal s_i to the speech encoder is supposed to be the 16-bit 2's complement speech sample. For a 16-bit speech sample the range of available values is -32768 to +32767. **Figure 1** shows the block diagram for ADPCM compression algorithm.

For the next iteration of the encoder, the predicted sample s_p and the quantizer step size index are saved in a structure. For this iterative process, the quantization step size index and the predicted sample s_p are initially set to zero. The input s_i to the speech encoder is supposed to be a 16-bit 2's complement speech sample, while the value returned by the speech encoder is an 8-bit number which contains the 4-bit sign magnitude ADPCM code.

The difference d is produced by subtracting the predicted sample s_p from the input signal s_i. The 4-bit ADPCM value t is obtained by performing adaptive quantization on the difference obtained in

01. ADPCM Encoder takes a 16-bit signed number (speech sample, -32768 to +32767) and returns an 8-bit number containing the 4-bit ADPCM Code (0-15).
02. Restore the previous values of predicted sample (s_p) and the quantizer step size index Find the quantizer step size (q) from a lookup table using the quantizer step size index.
03. Compute the difference (d) between the actual sample (s_i) and the predicted sample (s_p).
04. Set the sign bit of the ADPCM code (t) if necessary and find the absolute value of difference (d).
05. Save quantizer step size (q) in a temporary variable.
06. Quantize the difference (d) into the ADPCM code (t) using the quantizer step size (q).
07. Inverse quantize the ADPCM code (t) into a predicted difference (d_q) using the quantizer step size (q).
08. Fixed predictor computes new predicted sample (s_r) by adding the old predicted sample (s_p) to the predicted difference (d_q).
09. Check for overflow of the new predicted sample (s_r). s_r, which is a signed 16-bit sample, must be in the range of -32768 to +32767.
10. Find the new quantizer step size index (q) by adding the previous index and a lookup table using the ADPCM code (t).
11. Check for overflow of the new quantizer step size index.
12. Save the new predicted sample (s_r) and quantizer step size index for next iteration.
13. Return the ADPCM code (t).

Algorithm 1: *ADPCM encoder algorithm step-by-step*

the previous step. Using that ADPCM value the encoder and decoder update their internal variables.

The encoder actually contains a full decoder embedded inside it. This ensures synchronization between encoder and decoder without requiring any additional data. The dotted lines in Figure 1 depict the block comprising the embedded decoder. The ADPCM value is used by the embedded decoder to update the inverse quantizer, which in turn produces a dequantized version d_q of the difference d.

To simplify the speech compression process a fixed predictor has been used instead of an adaptive predictor, which significantly reduces the amount of data memory and instruction cycles required. A weighted average of the last six dequantized difference values and the last two predicted values are used by the adaptive predictor of ITU G.721 for its adjustment and updating according to the value of each input sample. At this point, new predicted sample sr is obtained by adding the dequantized difference d_q to the predicted sample s_p. Finally, the new predicted sample s_r is saved in s_p.

Algorithm 1 is a step-by-step description of the ADPCM Encoder function. This function requires five 16-bit variables and two 8-bit variables. Some optimizations can be made in this code by combining steps 7 and 8.

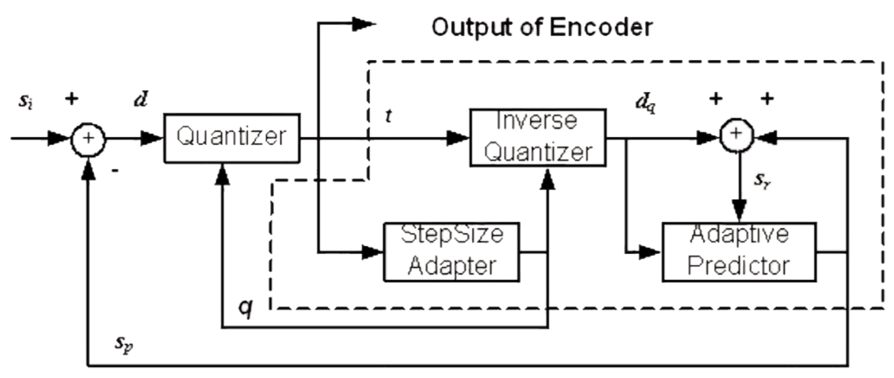


Figure 2: *ADPCM decoder block diagram*

Decompression

The input to the speech decoder is supposed to be an 8-bit number containing the 4-bit ADPCM data in sign magnitude format. The allowable values for t range from 0 to 15, where 7 = 0 x 07 and -7 = 0 x 0F.

The block diagram of the ADPCM decompression is shown in **Figure 2**. For the next iteration of the decoder, the predicted sample value s_p and the quantizer step size index are saved in a structure. The quantizer step size index and the predicted sample (s_p) are initially set to zero. A 4-bit sign magnitude ADPCM code is fed as an input to the ADPCM Decoder() function, which in turn produces a 16-bit 2's complement speech sample. The decoder is same as the one used by the encoder routine.

For updating the inverse quantizer it uses the ADPCM value, which in turn produces the difference d_q. The output sample sr is produced by adding the difference d_q to the predicted sample s_p. For next iteration of the decoder the output sample s_r is saved into the predicted sample.

The function ADPCM Decoder function is listed in **Algorithm 2**. This function requires three 16-bit variables and one 8-bit variable.

Performance

In this article we have used AVR ATmega8535 microcontroller. The ATmega8535 is a low-power CMOS 8-bit microcontroller, based on the AVR enhanced RISC architecture. By executing instructions in a single clock cycle, the

ATmega8535 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed.

The external oscillator frequency that we have chosen is 7.3728MHz. This oscillator generates a baud rate for serial communication with PC with very little error in baud rate. The sampling rate chosen for analogue-to-digital conversion (ADC) process is 8kHz per sample. With this sampling rate the microcontroller has a time span of 125µs seconds between two consecutive samples taken from ADC. So, during this time span of 125µs, considering the maximum code size, the microcontroller is not only required to compress and pack two speech data samples but, also, it has to transmit the compressed speech samples to the PC through serial port.

The maximum instruction cycles taken by all the routines, including speech compression (281 instruction cycles), packing two compressed speech data sample in a single byte (5 instruction cycles), ISR for Timer0 over flow (5 instruction cycles), ISR for ADC (105 instruction cycles) and ISR for serial communication (40 instruction cycles) are approximately 473 instruction cycles.

Considering single-clock cycle execution per instruction and 7.3728MHz operating frequency, it may be noted that single instruction cycle takes 0.1356µs and 473 instruction cycles would take approximately 64.1547µs. A single instruction cycle for AVR 8535 takes one clock cycle of external oscillator, this external oscillator frequency not only generates a good error free baud rate for serial communication with PC, but it is also more than sufficient for implementing ADPCM speech compression algorithm.

Application

The hardware for this application article implements only the compression algorithm, while the decompression algorithm is implemented in PC using Turbo C. In order to implement the audio recording, the following components need to be added to the application hardware:

- A microphone with anti-aliasing filter;
- Amplifier with adjustable gain;
- Built-in A/D converter and timer of AVR 8535 microcontroller.

The conversion time for this application has been chosen to be 52µs.The sampling rate used by A/D converter is 8kHz, which takes input sample every 125µs. In this way the effective bandwidth of the input speech data is 4kHz, which is sufficient enough for human speech recording.

The compiler used for this data compression and decompression application is ICCAVR version 7.14. For simulation of the speech compression code AVR Studio4 has been used. AVR Studio is an Integrated Development Environment (IDE) for writing and debugging AVR applications in Windows.

The audio data is fed as input to the built-in ADC of the AVR microcontroller from microphone after filtering and amplification. The microcontroller generates the digital samples from analogue audio input through an analogue-to-digital conversion process, compresses the speech samples, and then serially transmits the two compressed speech samples per byte. The speech data is recorded on a PC in a binary file through a Hyper Terminal. The binary file is used by the ADPCM speech decompression algorithm implemented in Turbo C. A program written in Visual C++ is used on the PC side for converting the recorded and decompressed speech data to audio file.

Results

The final results of the application hardware using the ATmega8535 are:

Compression

- The ADPCM compression routine compresses 10 bits of uncompressed data sample to 4 bits of compressed data. This ADPCM compression routine actually takes 16-bit input and generates a 4-bit ADPCM code. In this way, it gives almost 60% compression of single input speech sample.
- 281 instruction cycles to encode single data sample to ADPCM compressed sample.

01. ADPCM Decoder takes an 8-bit number containing the 4-bit ADPCM code (0-15) and returns a 16-bit signed number (speech sample, -32768 to +32767).
02. Restore the previous values of predicted sample (s_p) and quantizer step size index.
03. Find the quantizer step size (q) from a lookup table using the quantizer step size index.
04. Inverse quantize the ADPCM code (t) into a predicted difference (d_q) using the quantizer step size (q).
05. Fixed predictor computes new predicted sample (s_r) by adding the old predicted sample (s_p) to the predicted difference (d_q).
06. Check for overflow of the new predicted sample (s_r). s_r, which is a signed 16-bit sample, must be in the range of -32768 to +32767
07. Find the new quantizer step size (q) by adding the previous index and a lookup table using the ADPCM code (t).
08. Check for overflow of the new quantizer step size index.
09. Save the new predicted sample (s_r) and quantizer step size index for next iteration.
10. Return the new sample (s_r)

Algorithm 2: *ADPCM decoder algorithm step-by-step*

- Upon compiling the compression code in ICCAVR7.14 compiler, the compiler shows the device to be 15% full.

Decompression

- It has been implemented on a PC using Turbo C which receives compressed data bytes through serial port, decompresses the received data and writes the decompressed data in a binary file.
- Visual C++ program is used for transforming the binary file to a wave file.
- Baud rate used for receiving data at serial port is 115200bps.
- Data format used for serial communication is: 8 bits per sample, 1 start bit, 1 stop bit and no parity. ■

Microcontroller DEBUGGING and TESTING tools

Professor Dr Dogan Ibrahim, lecturer at the Near East University of Nicosia in Cyprus, describes some of the currently available tools for microcontroller debugging and testing

DESIGNING A microcontroller-based system is a complex activity that involves hardware and software interfacing with the external world and many engineers find it difficult the first time.

Successful design of a microcontroller-based system requires skills to use the various debugging and testing tools available. A program may seem to be running but may not be effective, or it might give the wrong results when operated in real-time, so debugging may be the only tool to help eliminate the problems.

Tools for debugging and testing microcontroller-based systems can be divided into two groups: software-only tools and software-hardware tools. Software-only tools come in the form of monitors and simulators, which are independent of the hardware under development. Software-hardware tools are usually hardware dependent, are more expensive and range from in-circuit emulators and in-circuit simulators to in-circuit debuggers. In general, the higher the level of integration with the target hardware, the greater the benefit of a tool, resulting in a shorter development time, but the greater the cost as well.

This article describes very briefly some of the commercially available tools for debugging and testing microcontroller-based systems. The factors to consider when choosing a debugging tool are cost, ease of use and the features offered during the debugging process.

In this article I will describe the details of one of the popular low-cost debugging tools, with an example showing how an in-circuit debugger can be used in a real design. I've used the PIC microcontroller family as the basis for this article.

Software Simulators

A software simulator is basically a computer program running on an independent hardware and it simulates the CPU, the instruction set and the I/O of the target microcontroller. Simulators offer the lowest-cost development tools for microcontroller-based systems and most companies offer their simulator programs free of charge.

Basically, the user program can be operated in a simulation environment where the user can insert breakpoints within the code to stop the code and then analyze the internal registers and memory, display and change the values of program variables and so on.

Incorrect logic or errors in computations can be analyzed by stepping through the code in simulation. Simulators run at speeds 100 to 1000 times slower than the actual microcontroller hardware and, thus, long time delays should be avoided when simulating a program.

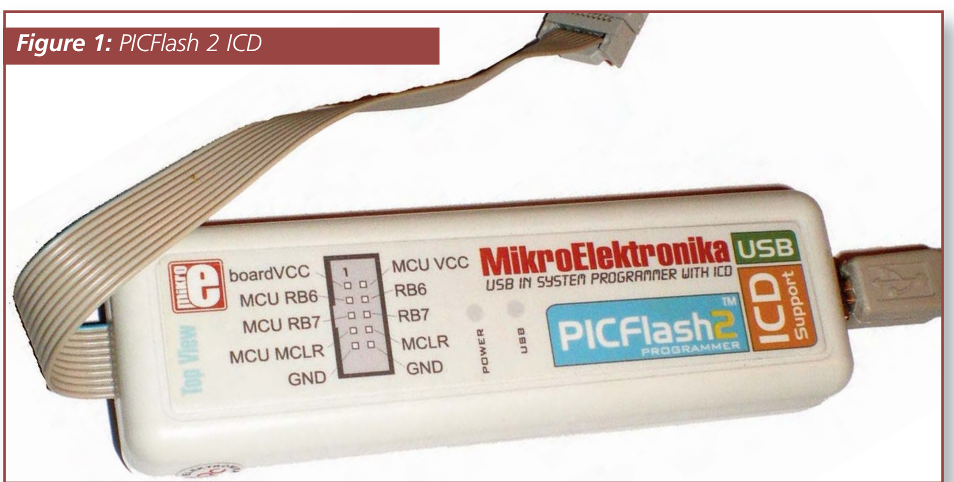
Microcontroller-based systems usually have interfaces to various external devices such as motors, I/O ports, timers, A/D converters, displays, push-buttons, sensors and signal generators, which are usually difficult to simulate. Some advanced simulators, such as the Proteus from Labcenter Electronics (**www.labcenter.co.uk**) for example, allow the simulation of various peripheral devices such as motors, LCDs, 7-segment displays and keyboards, and users can, in general, create new peripheral devices. Inputs to the simulator can come from files that may store complex digital I/O signals and waveforms. Outputs can be in the form of digital data or waveforms, usually stored in a file, or displayed on a screen. Some simulators accept only the assembly language of the target microcontroller.

Most microcontroller software is nowadays written using a high-level language such as C, Pascal or Basic, and it has become a necessity to simulate a program written in a high-level language. Some simulators – the microC, developed by mikroElektronika (**www.mikroe.com**) – can perform simulation using high-level languages. Oshon Software simulators (**www.oshonsoft.com**) are powerful low-cost high-level language simulators enabling the user to set breakpoints and display and modify registers and program variables.

Monitors

Monitors are software tools that usually run on the target microcontroller system. A monitor program usually resides in the bottom or top

Figure 1: *PICFlash 2 ICD*



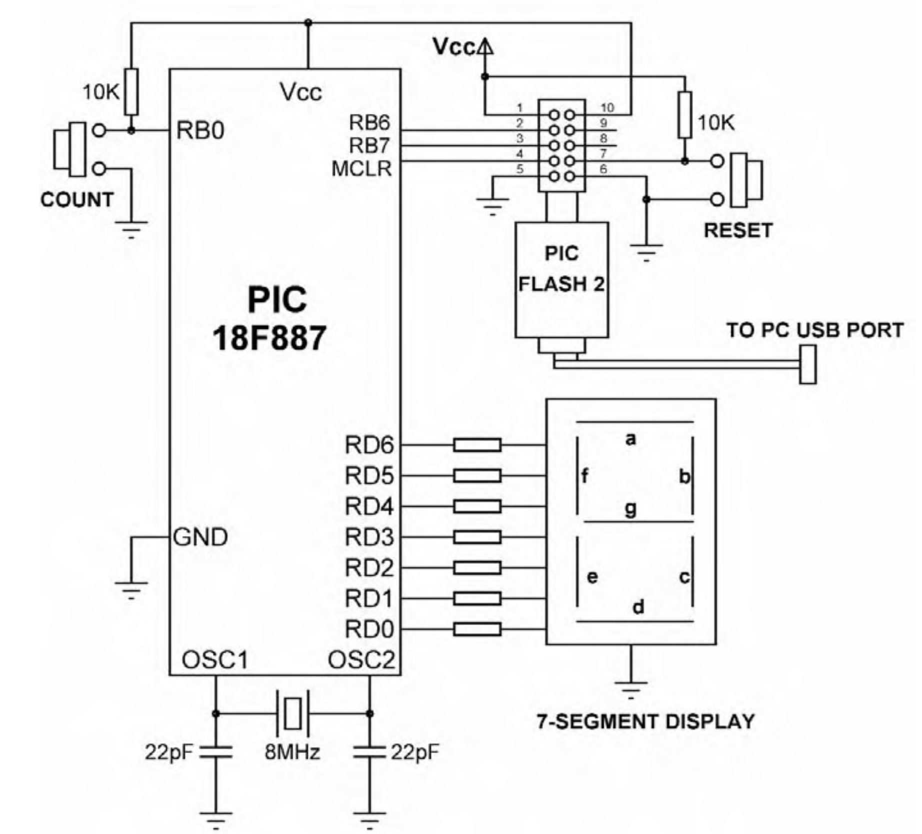


Figure 2: *Circuit diagram of the example*

part of target microcontroller's memory and, with the aid of a monitor program, a user can download a program code, execute the code, set breakpoints in the code and examine and modify memory locations or registers.

The target microcontroller is usually connected to a terminal via an RS232 serial port (or USB) and the monitor commands are implemented directly on the target. One disadvantage of a monitor tool is that the execution of the application program must be stopped before a memory location or a register can be examined or changed. Monitor tools used to be very common in the early days of microprocessors and microcontrollers but they are seldom used nowadays.

In-Circuit Emulators

In-circuit emulators (ICE) offer real-time code execution, full peripheral implementation and breakpoint capability. An in-circuit emulator is plugged into the socket of the microcontroller in the target development system, replacing the target microcontroller. User program is loaded into the RAM memory of the emulator and the code executes in real-time.

In-circuit emulators offer real-time trace buffers, full internal register and memory access, and multi-level conditional breakpoints. Although an in-circuit emulator can be an invaluable debugging tool, its cost is usually much higher than the other debugging tools and different microcontrollers from different manufacturers, or even different models from the same manufacturer require different in-circuit emulator probes.

A popular ICE for PIC microcontrollers is the MPLAB ICE 4000 (**www.microchip.com**), consisting of an Emulator Pod, Processor Module, Device Adapter and a Transition Socket. A common emulator pod is used for all PIC microcontrollers and the pod communicates with the PC via an USB connection. The processor module, together with the device adapter and transition socket, is used for a specific processor, or processor family.

Burn and Learn Method

In many non-complex microcontroller-based system developments the 'burn and learn' method can be used for testing and debugging the system. This is basically a testing method, although it can be used for debugging as well.

Here the microcontroller is programmed with the application code and then inserted into the target development system. Routines are then added to toggle the I/O pins, to dump data through the serial port, to send test data to an LCD and so on. For example, the result of a multiplication can be sent to the I/O ports and the program can be halted to examine the I/O ports, say by connecting LEDs or by measuring the voltage at the port pins to check whether or not the data is as expected. Alternatively, data can be sent to the LCD at various points of the program in order to trace the execution path of the program.

'Burn and learn' does not require any specialised software tools, and testing a system using this method is usually very inefficient, tedious and very slow.

In general, the following hardware can be useful in burn and learn method of testing:

- LED – An LED can be blinked on and off to tell what the code is doing. The disadvantage is that it cannot be used in fast time-critical applications.
- LCD – Characters can be displayed on an LCD to tell what the code is doing. The disadvantage is that it uses an 8-bit port.
- USART – Data can be sent to an LCD to see what the microcontroller is doing. The disadvantage is that the data transfer time is slow and extra hardware is usually needed.
- Logic Analyzer – Can be useful in testing the interface and control of peripheral devices such as USB, I2C, CAN or SPI bus. The disadvantage is that it can be expensive.
- Voltmeter or Oscilloscope – This is the simplest testing method where the state of a pin can be checked and, thus, some idea about the flow of program code can be obtained.

In-Circuit Simulation

An in-circuit simulator is very similar to a software simulator with the added advantage that inputs can be provided from the target hardware and, also, outputs can be sent to the

Parameter	Software Simulation	Burn and Learn	In-Circuit Simulator	In-Circuit Emulator	In-Circuit Debugger
Cost	very low	very low	Very low	high	low
Breakpoints	yes	no	no	yes	yes
Trace	yes	no	yes	yes	no
Single stepping	yes	no	yes	yes	yes
Loss of target pins	No	no	no	no	yes
Program downloading	yes	no	yes	Yes	yes
Real time execution	No	yes	no	yes	yes
Learning curve	medium	low	medium	medium	medium

Table 1: *Features of debugging and testing tools*

target hardware. In-Circuit Simulators are not very common and are only available for specific hardware platforms. Because an in-circuit simulator runs at the speed of the simulator software, it runs much slower than the target microcontroller and, thus, can not be used to simulate time critical applications, such as an USB port or the data transfer from an USART port.

In-Circuit Debuggers

In-circuit debuggers (ICD) are very clever tools used instead of the more expensive in-circuit emulators. An ICD is a small hardware device connected between a PC and the microcontroller development system (some development systems have built-in ICD circuits).

An ICD uses the In-Circuit Serial Programming (ICSP) capability of the target microcontroller where two or three pins of the microcontroller are allocated to the ICSP operation. The ICD downloads a small control program to the target microcontroller's flash program memory and then the user can develop and debug source code by setting breakpoints, watching variables, single-stepping the program, or running the program in full speed, thus enabling the time critical routines to be tested in real-time.

An ICD requires specialized circuitry to be present on a target microcontroller, such as logic to communicate to the ICD device, logic to single step program code and logic to halt and interrogate the target microcontroller. Although an ICD can be an invaluable debugging tool, it has two main disadvantages: it uses some memory of the target microcontroller and it requires the use a few pins of the target microcontroller to communicate and control the target.

MPLAB ICD2 and, lately, the ICD3 are two of the popular in-circuit debuggers developed by Microchip. Some other popular PIC microcontroller in-circuit debuggers are: ICD-U40 (by CCS Inc., **www.ccsinfo.com**), PICFlash 2 (by mikroElektronika) and others.

Table 1 gives a comparison of the various features of the debugging and testing tools.

In this article, an example is given to show how an ICD device can be used in a simple microcontroller-based system development. Although the operation and use of most ICDs are similar, the low-cost PICFlash 2 ICD is used in the example below for illustrative purposes.

PICFlash 2 In-Circuit Debugger

PICFlash 2 ICD is manufactured by mikroElektronika as a general purpose ICD and, also, for use in their development systems. A picture of the PICFlash 2 ICD is shown in **Figure 1**. The ICD is connected to the USB port of a PC and to the following pins of a PIC microcontroller:

- RB6
- RB7
- MCLR

Pins RB6 and RB7 are used for data and clock and pin MCLR provides the chip programming voltage. ICD manufacturers usually provide headers to connect their devices easily to the target microcontroller. Commands can be sent to PICFlash 2 from the mikroElektronika language compilers to watch and modify program variables, to set breakpoints and to single-step the program.

Example Use of PICFlash 2

A simple 7-segment display example is given here to illustrate how useful an ICD can be during the microcontroller-based system development cycle.

As shown in **Figure 2**, a 7-segment display is connected to PORT D of a PIC16F877 type microcontroller and a push-button is connected to bit 0 of PORT B (RB0). In this example, a count is incremented and its value sent to the 7-segment display whenever the push-button is pressed. As such the display shows the count as 0, 1, 2, 3…9, 0, 1… as the button is pressed. Notice that ICD pins RB6 and RB7 and MCLR of the microcontroller are connected to a PICFlash 2 ICD.

The software in this example is based on the mikroC language, a popular C language compiler from mikroElektronika, supporting a built-in software simulator and the PICFlash 2 ICD. The program listing is given in **Figure 3**. Variable count is incremented every time the button (PButton) is pressed. Array LED stores the bit pattern to be sent to the 7-segment display to turn on a digit and this array is indexed by variable count.

In-Circuit Debugging

The debugging steps are given below:

- Write the program given in Figure 3, making sure that the compiler is configured as follows:

Device:	P16F887
Clock:	8MHz
Build Type:	ICD debug
Debugger:	mikroICD Debugger

- Compile the program with no errors
- Connect the ICD to the target microcontroller system
- Send the program to the target microcontroller by pressing F11 or by selecting *Tools -> PicFlash Programmer*
- Select the mikroICD debugger. *Debugger -> Select Debugger -> mikroICD Debugger.*
- Start the debugger. *Click Run -> Start Debugger*
- Select variables and I/O ports count, PORTD and PORTB from the Watch Window.
- The program is now ready for debugging. Press F7 to single step through the program. As shown in **Figure 4**, a blue bar moves down the program lines to indicate the statement being executed. You should see the values of variables changing as the program is executing in single step mode.

```
/***************************************************************************
                    ICD DEBUGGER EXAMPLE
                    ====================

This is an ICD example. In this example a 7-segment display is connected to PORT D and a push-button switch is connected to
RB0. When the switch is pressed a count is incremented and displayed on the 7-segment display. The display counts as 0 1 2 3 ….9
0 1…..
A PIC16F887 type microcontroller is used in the project with an 8MHz crystal.
Date: January 2009
File: ICD.C
***************************************************************************/
#define PButton PORTB.F0

void main()
{
 char count = 0;
 unsigned char LED[] = {0x3F, 0x06, 0x5B, 0x4F, 0x66, 0x6D, 0x7D, 0x07, 0x7F, 0x67};

 ANSELH = 0;
 TRISB = 1;
 TRISD = 0;
//
// Endless loop
//
 for(;;)
 {
 while(PButton);                     // Wait until Button is pressed
 PORTD = LED[count];                 // Send count to display
 count++;                            // Increment count
 if(count == 10)count = 0;           // Count is between 0 and 9
 }
}
```

Figure 3: *Program listing*

- Click on PORTD value to change the display type to hexadecimal. You should see the PORT D output sent to the 7-segment display as the value of count changes. The program stops whenever it is waiting for the push-button to be pressed. Pressing the button on the target system advances the program to the next statement, where the data is sent to PORT D and the next number is displayed on the 7-segment display.
- In addition to the Watch Window, the ICD can also display the EEPROM data *(View -> Debug Windows -> View EEPROM),* code data *(View -> Debug Windows -> View Code) or the RAM data (View -> Debug Windows -> View RAM).*

Most Popular Tool

In this paper the commonly used microcontroller debugging and testing tools are described. It is discussed that although an in-circuit emulator is probably the most useful tool, it is also the most expensive tool to use.

In-circuit debuggers are currently the most popular debugging tools because of their low-cost and the ability to debug in real-time using the target microcontroller development system. ■

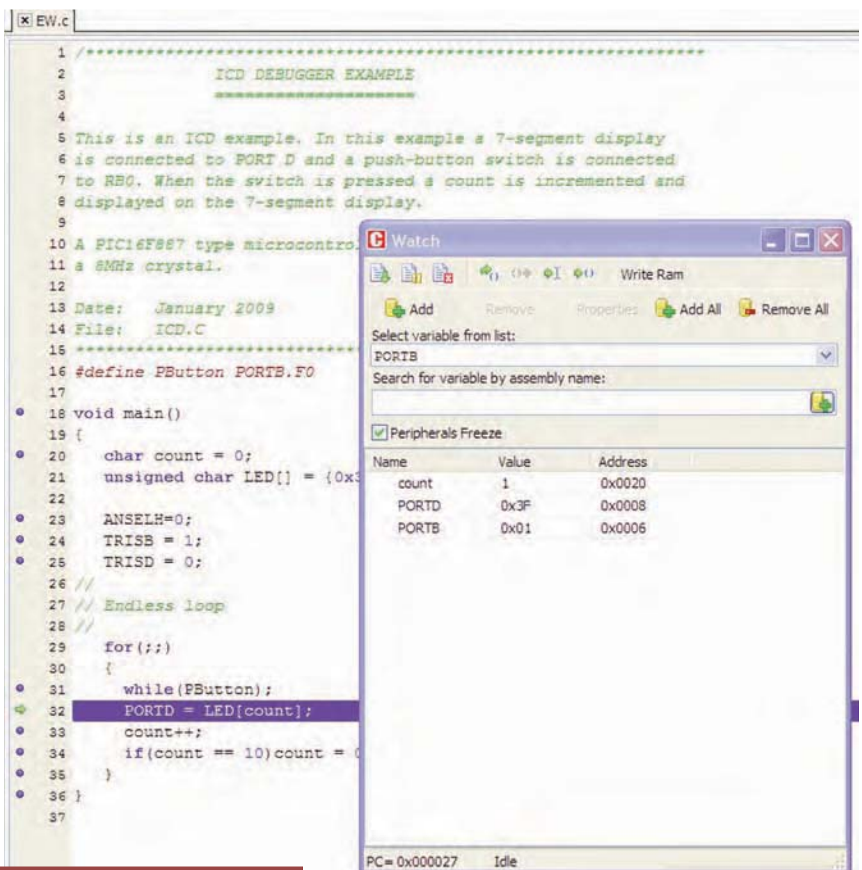


Figure 4: *The Watch Window*

Cortex Microcontroller – THE NEW STANDARD?

Reinhard Keil, Director for MCU Tools at ARM, discusses the benefits brought to embedded designers by the Cortex-Mx processor, especially when used with the Cortex Microcontroller Software Interface Standard (CMSIS)

TODAY, THE GENERAL purpose microcontroller segment is one of the most fragmented markets in the electronics industry. The many microcontroller architectures that are available often have a long history; most 8- and 16-bit architectures were invented more than 20 years ago.

Over the years, these old-fashioned CPU architectures have been re-shaped numerous times to meet the requirements of today's demanding applications. In order to cope with the lack of CPU performance, strange peripherals are sometimes introduced such as an arithmetic accelerator or a hardware CORDIC.

The situation is highly reminiscent of the computer industry before the introduction of the PC. Software programs have to deal with a lack of memory and CPU performance. Since no peripheral and interface standards exist, programmers must invent solutions time and again for the very same basic problems, and adopt existing software algorithms to new hardware.

In such environments, object-oriented programming can rarely be used. Generic software components that are common in the PC world are not available and the lack of programming standards limits software reuse. Instead, silicon vendors must provide free software frameworks for new devices that are tailored towards specific applications. This slows down the introduction of new devices and significantly increases the development costs.

Another shortcoming of today's 8- and 16-bit microcontrollers is the proprietary debug technology that is integrated into these devices. In most cases only run-stop tests with breakpoints are possible. Data trace capabilities required for the dynamic analysis of running applications are not available. Together with the high expectations for modern end-products it is not surprising that software development for deeply embedded applications becomes more and more expensive. All these symptoms prevent real innovation of new technologies and products. Once the PC became a standard, many new software products appeared on the market and new businesses built around such solutions became successful.

It seems that the deeply embedded market needs a new approach and the Cortex-Mx processors, together with the large ARM ecosystem, have the potential to solve most problems that have been described here.

Microcontrollers that are based on the ARM Cortex-M3 processor are rapidly becoming popular in the industry. LuminaryMicro (now part of Texas Instruments) and STMicroelectronics (ST) released Cortex-M3 processor-based microcontrollers sometime ago and are continuously extending their offerings. New on the market are Cortex-M3 processor based devices from Atmel, NXP and Toshiba. In the next few months other

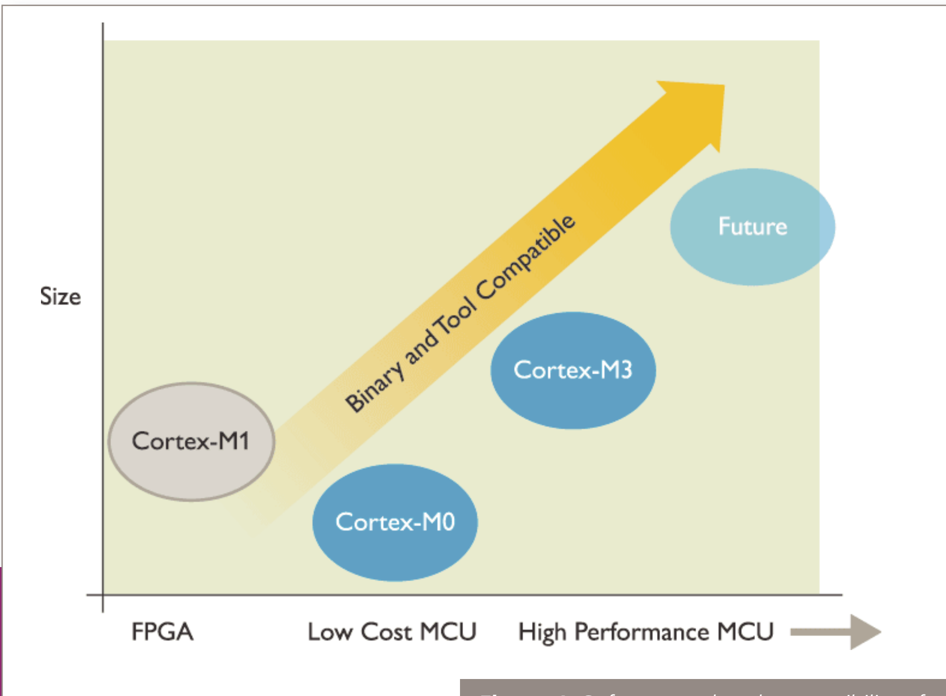
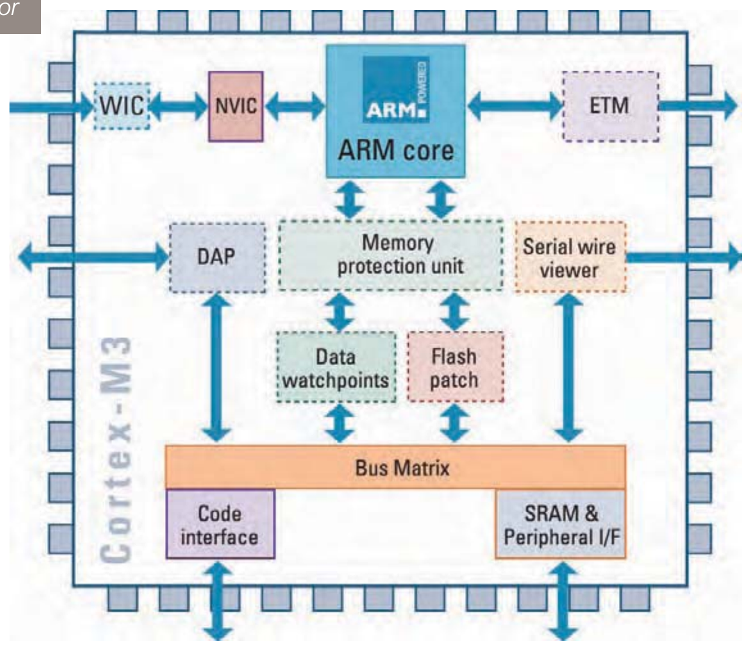


Figure 1: *Software and tool compatibility of current and future Cortex-Mx processors*

Figure 2: *Components of the Cortex-M3 processor*



vendors will follow. At the Embedded Systems Conference 2009, NXP announced its new Cortex-M0 microcontroller family which is fully peripheral and software compatible with their higher performance Cortex-M3 microcontroller family (see **Figure 1**).

So, Why Cortex-M3?

Every CPU implementation requires innovation and last year ARM released the second revision of the Cortex-M3 processor. As shown in **Figure 2**, this release introduced a Wake-up Interrupt Controller (WIC) for extreme low-power designs. The WIC works together with the Nested Vector Interrupt Controller (NVIC), which features very fast interrupt response times with multiple interrupt priorities. A Debug Access Port (DAP), combined with the Serial Wire Viewer (SWV) and the Embedded Trace Macrocell (ETM), provides extensive trace capabilities enabling non-intrusive software verification of a running system. The Memory Protection Unit (MPU) enables highly reliable software implementations and RTOS kernels.

The newest member of the Cortex family is the Cortex-M0 processor, tuned to ultra-low power applications that previously required specialized 8-bit or 16-bit architectures. The Cortex-M0 processor has an exceptionally small silicon area and promises substantial savings in system cost. The low gate count of the Cortex-M0 processor now enables analogue and mixed signal devices, as such expanding the application range for ARM processor-based microcontrollers.

The CMSIS Software

To simplify software development, ARM has introduced the Cortex Microcontroller Software Interface Standard (CMSIS), which addresses and solves the challenges faced when software components are deployed in microcontroller devices based on a Cortex-M0 or Cortex-M3 processor. CMSIS will be expanded to include future Cortex-Mx processor cores. By combining the Cortex-M profile processors with the Cortex Microcontroller Software Interface Standard (CMSIS), porting of software is simplified.

CMSIS has been defined in close co-operation with other silicon and software vendors, including CodeRed, Hitex, IAR, Keil, Micrium, Raisonance, Segger and Tasking. Such collaboration, combined with the experience from previous solutions, has resulted in an easy-to-use and easy-to-learn programming interface for Cortex processor-based microcontrollers. CMSIS provides a common approach for interfacing to peripherals, real-time operating systems and middleware components. CMSIS is compatible with several compiler implementations, including GCC, and provides the following software layers as shown in **Figure 3**:

- Peripheral Access Layer (CMSIS-PAL) contains name definitions, address definitions and helper functions to access processor core registers and device peripherals. It introduces a consistent way to access core peripherals, exception/interrupt vectors and provides a standard system start-up function. CMSIS-PAL also defines a device-independent interface for an RTOS kernel and data trace channels for non-intrusive RTOS kernel-awareness in debuggers, as well as a simple printf-style debugging.
- Middleware Access Layer (CMSIS-MAL) provides common methods to access peripherals for the software industry. The Middleware Access Layer is adapted by the silicon vendor for the device-specific peripherals used by more complex middleware components, such as communication stacks. The middleware access layer is currently in the development phase and we expect that IAR, Keil, Micrium, Segger and other middleware vendors to start shipping CMSIS-MAL compliant components during 2009.

Re-Usable Code

Today, application programmers are already re-using code that has previously been developed in-house. Now, CMSIS introduces a common programming standard that extends code re-use.

CMSIS is not another complex software layer that forces silicon vendors to produce identical features. It does not make peripherals equal, but the CMSIS-PAL defines common methods to program peripherals. The device peripherals such as I/O Port, Timer, PWM, A/D, D/A etc, can have different performance and functions. CMSIS does not prevent direct hardware access since the peripheral registers of a device can still be accessed directly by the application software and, therefore, it has no impact on the program and I/O performance.

CMSIS does not require immense resources either; the CMSIS-PAL requires less than 1KB code and just 4 bytes data space. The CMSIS-MAL is only required to interface to standard middleware (sophisticated communication stacks); a hardware abstraction layer (HAL) is common in such components. As such CMSIS-MAL replaces a proprietary middleware HAL and should not be considered as additional overhead.

Effectively, CMSIS provides a consistent software framework and a proven software layer. This enables easy deployment of template code and program examples across the supported compiler vendors. The Cortex-M3 processor, along with its core peripherals, is consistent across the various silicon vendors and ARM provides a common documentation for these components. Together with the CMSIS, this will allow generic introduction books that are not vendor or device specific. Over time, we expect a reduction in the learning curve for application programmers that have previous experience with Cortex-Mx devices from other vendors and want to start using a new Cortex-Mx device.

CMSIS provides all the files that are required to get started with the software development for a new microcontroller. With the exception of the startup file, the CMSIS files are tool chain independent and compatible with all compilers that support CMSIS:

For the Cortex-Mx processor core itself, ARM provides a header and C source files (core_cm0.h, core_cm0.c, core_cm3.h and core_cm3.c) that define the access to the core peripherals and include C functions to create special CPU instructions. The functionality is available for all Cortex processor based microcontrollers and gives control of the power saving modes, interface to the RTOS kernel and access to the interrupt system.

These processor core specific features are further extended by a device-specific header file (device.h), which is typically provided by the silicon vendor. This file defines all the peripheral registers in a consistent format and may contain additional functions to simplify access to device peripherals.

The silicon vendor also delivers a system file (system_device.c), which typically configures the clock and memory system of the device. It can provide configuration options and is the only CMSIS file that may need user customization.

The device startup file (startup_device.s), which is also provided by the silicon vendor, contains the interrupt vector table and configures the C run-time environment. It is compiler-specific and the only file that must be replaced when migrating projects to another development toolchain.

Figure 4 shows a typical application code which uses the functionality of the CMSIS abstraction layer. A single function, SystemInit, contains the chip-specific initializations and is available for each device that is supported with a CMSIS-compliant software layer. CMSIS also defines naming conventions and, therefore, the functions, registers and definitions that belong to a peripheral block all start with the same prefix. The postfix _IRQHandler indicates an interrupt service routine and the CMSIS start-up code provides a pre-defined handler for each available interrupt that implements an endless loop. Once the user code contains its own handler function, this end-less loop is omitted. This is just one example where CMSIS increases the program security since an application reaches a defined state, even when an interrupt is accidentally enabled.

Since the CMSIS layer is identical across all compiler vendors, no software adaptations are required when changing the toolchain. This provides standard interfaces that can be used by many silicon and middleware partners. Various companies can now work together, even when the software teams are using different compiler vendors. It reduces project risks since a CMSIS interface may be pre-verified and certified. Once the standard is widely adopted, a source code that uses CMSIS interfaces will be easier to understand and, hence, easier to verify.

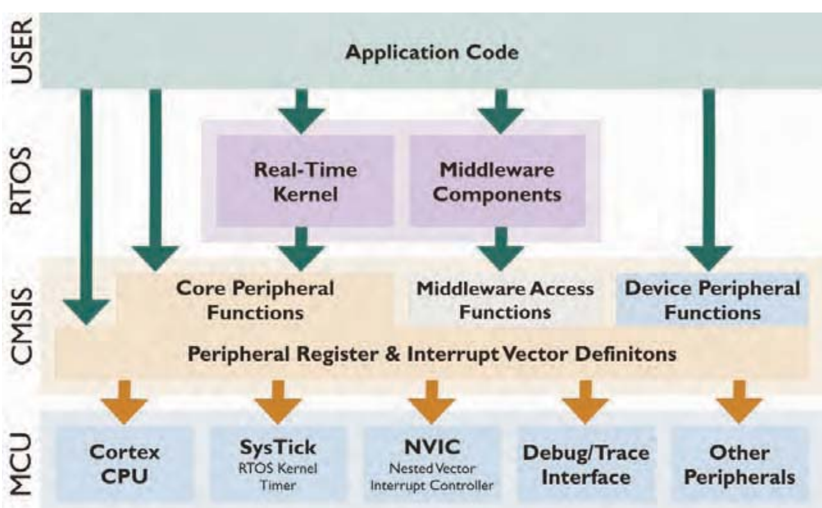


Figure 3: *Structure of the CMSIS abstraction layers*

Figure 4: *Program example using CMSIS*

```
#include <device.h>          // file name depends on device

void SysTick_Handler (void) {      // SysTick Interrupt Handler
 ;
}


void TIM1_UP_IRQHandler (void) {     // Timer Interrupt Handler
 ;
}

void timer1_init(int frequency) {    // set up Timer (device specific)
 NVIC_SetPriority (TIM1_UP_STM_IRQn, 1); // Set Timer priority
 NVIC_EnableIRQ (TIM1_UP_STM_IRQn);   // Enable Timer Interrupt
}

void main (void) {
 SystemInit ();            // global system setup

 if (SysTick_Config (SystemFrequency / 1000)) { // SysTick 1mSec
   : // Handle Error
 }
 timer1_init ();           // setup device specific timer
}
```

Debugging Interfaces and CMSIS

Every Cortex-M3 processor-based device provides data trace capabilities via the standardized 10-pin Cortex debug connector. Some microcontroller devices even have an ETM interface that adds full instruction trace and is accessed via a 20-pin low-cost connector. The data trace capabilities give the software programmer detailed timing and event information about exceptions and interrupts in their application. Periodic PC sampling may be used to derive statistics of program regions and help to determine application hot-spots. Data watchpoints deliver the data value, program location, and timing information for memory accesses of up to four variable locations. Via the Instrumented Trace Macrocell (ITM) the device offers 32 debug channels for code annotations in application-specific format.

CMSIS standardizes ITM code annotations for RTOS kernel debugging and terminal I/O communication for printf-style diagnostic output. **Figure 5** shows the RTX Event Viewer that provides timing information for each task via the CMSIS RTOS debug interface. Each ITM channel can be separately enabled and since the annotations are just memory accesses with minimal code overhead, the application program shipped in the end product can remain unchanged.

Standard Use

Historically, industries use standards to improve product quality and enable component and cost sharing across projects. In practice, such standards achieve wide acceptance since the synergistic effects provide significant benefits to the user community. The electronics industry is full of such standards, but until today the deeply embedded microcontroller market is still using many proprietary and specialized CPU architectures which have prevented the introduction of efficient software standards.

For the first time, the ARM processor offering enables a single architecture for the entire spectrum of embedded applications. The Cortex-M0 and the Cortex-M3 standard processors provide benefits other than just reusing the same development tools for many projects. For instance, together with the CMSIS, it also reduces development costs as software components can be more easily shared across projects and there are additional effects such as the reduction in the time-to-market for new products. Silicon vendors can focus more on device features and peripherals, rather than creating a proprietary software layer and basic interface routines.

Therefore, it is likely that innovative products based on Cortex-Mx processors will be available faster than with other microcontroller architectures. The common programming techniques that are introduced by CMSIS simplify long-term software maintenance since applications that are using CMSIS interfaces can be easily understood even by new team members. ■

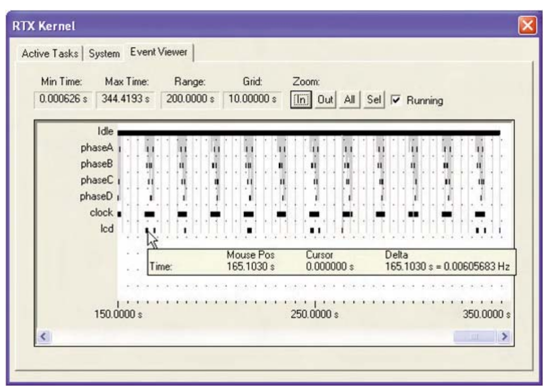


Figure 5: *RTX Event Viewer that uses the CMSIS RTOS debug interface*

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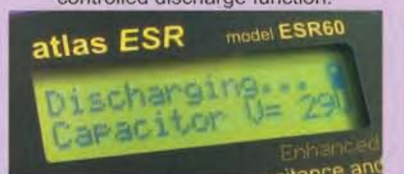

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Associate Professor **Dr Murat Uzam** from Nigde University in Turkey presents a series of articles on a project that focuses on a microcontroller-based PLC. This is the tenth article in the series describing arithmetical macros

PLC with PIC16F648A Microcontroller – Part 10

IN THIS ARTICLE, six arithmetical macros are described. The following operators are applied to the contents of two registers (R1 and R2): ADD, SUB (subtract), INC (increment), DEC (decrement).

Similar arithmetical macros are also described to be used with the contents of an 8-bit register (R) and an 8-bit constant (K).

Arithmetical Macros

Numerical data implies the ability to do arithmetical operations, and almost all PLCs provide some arithmetical operations such as add, subtract, multiply and divide. Arithmetical functions will retrieve one or more values, perform an operation and store the result in memory. As an example, **Figure 1** shows an ADD function that will retrieve and "add" two values from sources labelled source A and source B, and will store the result in destination C. The list of arithmetical functions (macros) described for UZAM_PLC follows. The increment and decrement functions are unary, so there is only one source.

ADD (source value 1, source value 2, destination) – add two source values and put the result in the destination.

SUB (source value1, source value 2, destination) – subtract the second source value from the first one and put the result in the destination.

INC (source value, destination) – increment the source and put the result in the destination.

DEC (source value, destination) – decrement the source and put the result in the destination.

The six arithmetical macros described for UZAM_PLC are shown in **Table 1**. In these macros, EN is a Boolean input variable taken into the macro through W, and ENO is a Boolean output variable sent out from the macro through W. Output ENO follows the input EN. This means that when EN = 0, ENO is forced to be 0 and when EN = 1, ENO is forced to be 1.

This is especially useful if we want to carry out more than one operation based on a single input condition. "IN", "R", "R1" and "R2" refer to 8-bit source variables from where the source values are taken into the related macro, while "OUT" refers to an 8-bit destination variable to which the result of the related macro is stored. "K" represents an 8-bit constant data to be used within the related macro.

When EN = 1, the macro "R1addR2" adds the contents of two 8-bit variables R1 and R2, and stores the result into the 8-bit output variable OUT. Similarly, when EN = 1, the macro "RaddK" adds the content of an 8-bit variable R and 8-bit constant data K, and stores the result into the 8-bit output variable OUT.

When EN = 1, the macro "R1subR2" subtracts the contents of 8-bit variable R2 from the contents of 8-bit variable R1, and stores the result into the 8-bit output variable OUT. Similarly, when EN = 1, the macro "RsubK" subtracts the 8-bit constant data K from the contents of 8-bit variable R, and stores the result into the 8-bit output variable OUT.

When EN = 1, the macro "incR" increments the contents of the 8-bit variables IN, and stores the result into the 8-bit output variable OUT. Finally, when EN = 1, the macro "decR" decrements the contents of the 8-bit variables IN, and stores the result into the 8-bit output variable OUT. The file "arthm_mcr_def.inc" including the 6 arithmetical macros shown in

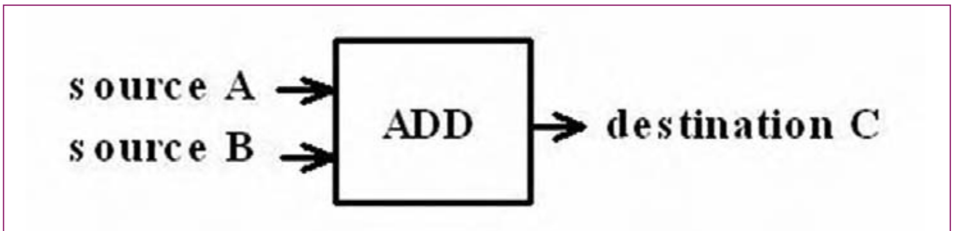


Figure 1: *The ADD function*

Table 1 can be downloaded from **http://host.nigde.edu.tr/muzam/**

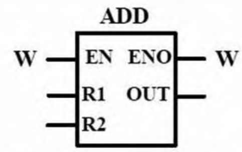
Examples

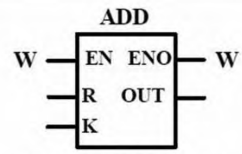
We will now consider three examples, namely UZAM_plc_8i8o_exN.asm, with N = 15, 16, 17, to show the usage of arithmetical macros. In order to test the program, please download the files from http://host.nigde.edu.tr/muzam/ and then open UZAM_plc_8i8o_exN.asm. Make N = 15, 16, 17 and compile it. After that by using the PIC programmer software, take the compiled file "UZAM_PLC_8i8o_exN.hex" and by your PIC programmer hardware send it to the program memory of PIC16F648A microcontroller within the UZAM_PLC. After loading the "UZAM_PLC_8i8o_exN.hex", switch the 4PDT in "RUN" and the power switch in "ON" position. Finally, you are ready to test the program.

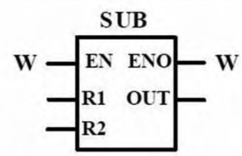
When studying these three examples, note that the output register Q0 is made up of the 8 bits: Q0.7, Q0.6…Q0.0 and that Q0.7 is the most significant bit (MSB), while Q0.0 is the least significant bit (LSB). The three examples considered here make use of the previously described macros "load_R" and "r_edge" and, therefore, the files "mv_ld_mcr_def.inc" and "ff_mcr_def.inc" are included in these examples. Also, bI0.1 (respectively bI0.4) is the bouncing input bit I0.1 (respectively I0.4). For more details on the bouncing and debounced inputs please consider the Part 2 article of this series.

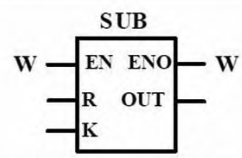
The first example program, "UZAM_plc_8i8o_ex15.asm" is shown in **Figure 2**. It shows the usage of two arithmetical macros – "R1addR2" and "R1subR2". The ladder diagram of the user program of "UZAM_plc_8i8o_ex15.asm" shown in Figure 2 is depicted in **Figure 3**. In the first rung, Q0 is cleared, 8-bit numerical data "02h" is loaded to 8-bit variable M1 and 8-bit numerical data "03h" is loaded to 8-bit variable M2 (for M1 and M2 please consider the article Part 2) by using the macro "load_R". This process is

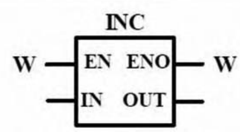
Algorithm	Macro	Symbol

if EN = 1 then
OUT = R1 + R2;
ENO = 1;
else ENO = 0;
end if;
	R1addR2 macro in1,in2,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	movfw in1
	addwf in2,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		R1, R2, OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

if EN = 1 then
OUT = R + K;
ENO = 1;
else ENO = 0;
end if;
	RaddK macro in1,in2,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	movlw in2
	addwf in1,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		R, OUT (8 bit register)
		K (8 bit constant)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

if EN = 1 then
OUT = R1 – R2;
ENO = 1;
else ENO = 0;
end if;
	R1subR2 macro in1,in2,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	movfw in2
	subwf in1,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		R1, R2, OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

if EN = 1 then
OUT = R – K;
ENO = 1;
else ENO = 0;
end if;
	RsubK macro in1,in2,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	movlw in2
	subwf in1,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		R, OUT (8 bit register)
		K (8 bit constant)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

if EN = 1 then
OUT = IN + 1;
ENO = 1;
else ENO = 0;
end if;
	incR macro in,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	incf in,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		IN, OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

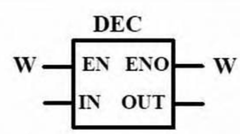
if EN = 1 then
OUT = IN - 1;
ENO = 1;
else ENO = 0;
end if;
	decR macro in,out
	local L1
	movwf Temp_1
	btfss Temp_1,0
	goto L1
	decf in,W
	movwf out
	movfw Temp_1
	L1
	endm
		
		IN, OUT (8 bit register)
		EN (through W) = 0 or 1
		EN0 (through W) = 0 or 1

Table 1: *The arithmetical macros, together with their algorithms and symbols*

```
.
      #include <definitions.inc>    ;basic PLC definitions, macros, etc.
      #include <cntct_mcr_def.inc>  ;Contact & Relay based macros
      #include <mv_ld_mcr_def.inc>  ;move_R, load_R macros
      #include <arthm_mcr_def.inc>  ;Arithmetical macros
      #include <ff_mcr_def.inc>     ;flip-flop macros
.
;--------------- user program starts here ------------------------
      ld          FRSTSCN     ;rung 1
      or          I0.0
      load_R      00h,Q0
      load_R      02h,M1
      load_R      03h,M2

      ld          bI0.1       ;rung 2
      R1addR2     Q0,M1,Q0

      ld          I0.2        ;rung 3
      R1addR2     Q0,M1,Q0

      ld          I0.3        ;rung 4
      r_edge      0
      R1addR2     Q0,M1,Q0

      ld          bI0.4       ;rung 5
      R1subR2     Q0,M2,Q0

      ld          I0.5        ;rung 6
      R1subR2     Q0,M2,Q0

      ld          I0.6        ;rung 7
      r_edge      1
      R1subR2     Q0,M2,Q0
;--------------- user program ends here -------------------------
.
```

Figure 2: *The user program of UZAM_plc_8i8o_ex15.asm*

carried out once at the first program scan by using the "FRSTSCN" NO contact. Another condition to carry out the same process is the NO contact of the input I0.0. This means that when this program is run, during the normal PLC operation if we force the input I0.0 to be true, then the above mentioned process will take place.

In the PLC rungs 2, 3 and 4, we see how the arithmetical macro "R1addR2" could be used. In the rung 2, the addition process Q0 = Q0 + M1 is carried out, when bI0.1 goes true. With this rung if bI0.1 goes and stays true, the Q0 will be added the content of M1, i.e. numerical data "02h", on every PLC scan.

Similar is applicable to the rung 3, where the addition process Q0 = Q0 + M1 is carried out when I0.2 goes true. Again, with this rung if I0.2 goes and stays true, Q0 will be added the content of M1, i.e. numerical data "02h", on every PLC scan.

Rung 4 provides a little bit different usage of the arithmetical macro "R1addR2". Here, we use a "rising edge detector" macro in order to detect the state change of input I0.3 from OFF to ON. So this time, the addition process Q0 = Q0 + M1 is carried out only at the rising edges of I0.3.

In the PLC rungs 5, 6 and 7 we see how the arithmetical macro "R1subR2" could be used. In the rung 5, the subtraction process Q0 = Q0 – M2 is carried out when bI0.4 goes true. With this rung if bI0.4 goes and stays true, the content of M2, i.e. numerical data "03h", will be subtracted from the content of Q0 on every PLC scan. Similar is applicable to rung 6, where the subtraction process Q0 = Q0 – M2 is carried out when I0.5 goes true.

Again, with this rung if I0.5 goes and stays true, the content of M2, i.e. numerical data "03h", will be subtracted from the content of Q0, on every PLC scan. Rung 7 provides a little bit different usage of the arithmetical macro "R1subR2". Here, we use a "rising edge detector" macro in order to detect the state change of input I0.6 from OFF to ON. So this time, the subtraction process Q0 = Q0 – M2 is carried out only at the rising edges of I0.6.

Second Example

The second example program, "UZAM_plc_8i8o_ex16.asm", is shown in **Figure 4**. It shows the usage of two arithmetical macros "RaddK" and "RsubK". The ladder diagram of the user program of "UZAM_plc_8i8o_ex16.asm" shown in Figure 4 is depicted in **Figure 5**.

In the first rung Q0 is cleared, by using the macro "load_R". This process is carried out once at the first program scan by using the "FRSTSCN" NO contact.

Another condition to carry out the same process is the NO contact of the input I0.0. This means that when this program is run, during the normal PLC operation if we force the input I0.0 to be true, then Q0 is cleared.

In the PLC rungs 2, 3 and 4 we see how the arithmetical macro "RaddK" could be used. In rung 2 the addition process Q0 = Q0 + 2 is carried out when bI0.1 goes true. With this rung if bI0.1 goes and stays true, the Q0 will be added the numerical data "02h" on every PLC scan. Similar is applicable to rung 3, where the addition process Q0 = Q0 + 2 is carried out when I0.2 goes true. Again with this rung, if I0.2 goes and stays true, the Q0 will be added the numerical data "02h" on every PLC scan.

Rung 4 provides a little bit different usage of the arithmetical macro "RaddK". Here, we use a "rising edge detector" macro in order to detect the state change of input I0.3 from OFF to ON. So this time the addition process Q0 = Q0 + 2 is carried out only at the rising edges of I0.3.

In the PLC rungs 5, 6 and 7 we see how the arithmetical macro "RsubK" could be used. In rung 5 the subtraction process Q0 = Q0 – 3 is carried out when bI0.4 goes true. With this rung if bI0.4 goes and stays true, the numerical data "03h" will be subtracted from the content of Q0 on every PLC scan. Similar is applicable to rung 6, where the subtraction process Q0 = Q0 – 3 is carried out when I0.5 goes true. Again with this rung if I0.5 goes and stays true, the numerical data "03h" will be subtracted from the content of Q0 on every PLC scan.

Rung 7 provides a little bit different usage

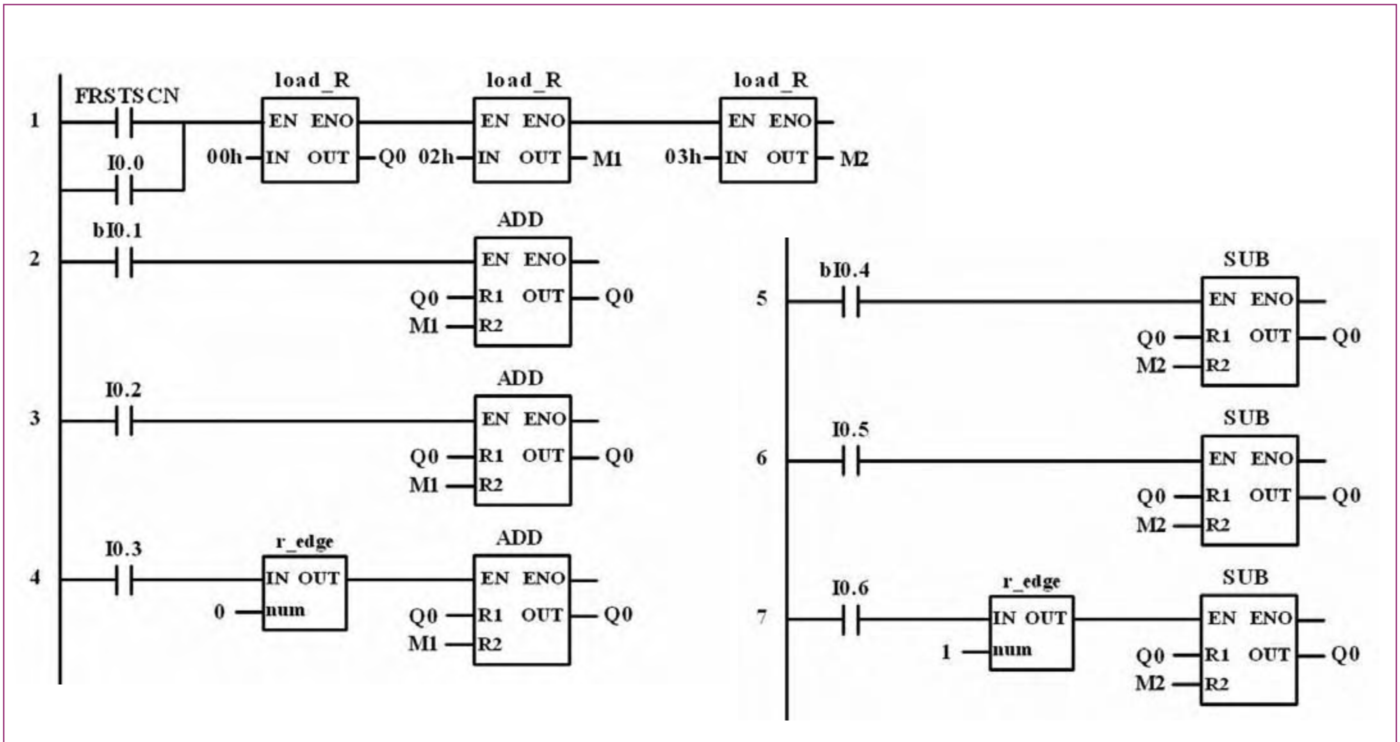


Figure 3: *Ladder diagram for the user program of UZAM_plc_8i8o_ex15.asm*

```
.
      #include <definitions.inc>     ;basic PLC definitions, macros, etc.
      #include <cntct_mcr_def.inc>   ;Contact & Relay based macros
      #include <mv_ld_mcr_def.inc>   ;move_R, load_R, inv_R macros
      #include <arthm_mcr_def.inc>   ;Arithmetic macros
      #include <ff_mcr_def.inc>      ;flip-flop macros
.
;--------------- user program starts here ------------------------
      ld           FRSTSCN      ;rung 1
      or           I0.0
      load_R       00h,Q0

      ld           bI0.1        ;rung 2
      RaddK        Q0,02H,Q0

      ld           I0.2         ;rung 3
      RaddK        Q0,02H,Q0

      ld           I0.3         ;rung 4
      r_edge       0
      RaddK        Q0,02H,Q0

      ld           bI0.4        ;rung 5
      RsubK        Q0,03H,Q0

      ld           I0.5         ;rung 6
      RsubK        Q0,03H,Q0

      ld           I0.6         ;rung 7
      r_edge       1
      RsubK        Q0,03H,Q0
;--------------- user program ends here -------------------------
.
```

Figure 4: *The user program of UZAM_plc_8i8o_ex16.asm*

of the arithmetical macro "RsubK". Here, we use a "rising edge detector" macro in order to detect the state change of input I0.6 from OFF to ON. So this time the subtraction process Q0 = Q0 – 3 is carried out only at the rising edges of I0.6.

Third Example

The third and last example program, "UZAM_plc_8i8o_ex17.asm", is shown in **Figure 6**. It shows the usage of two arithmetical macros "incR" and "decR". The ladder diagram of the user program of "UZAM_plc_8i8o_ex16.asm" shown in Figure 6 is depicted in **Figure 7**.

In the first rung Q0 is cleared by using the macro "load_R". This process is carried out once at the first program scan by using the "FRSTSCN" NO contact.

Another condition to carry out the same process is the NO contact of the input I0.0. This means that when this program is run, during the normal PLC operation if we force the input I0.0 to be true, then Q0 is cleared. In the PLC rungs 2, 3 and 4, we see how the arithmetical macro "incR" could be used. In the rung 2, Q0 is incremented by one, i.e. the process Q0 = Q0 + 1 is carried out, when bI0.1 goes true. With this rung if bI0.1 goes and stays true, then Q0 is incremented by one on every PLC scan. Similar is applicable to rung 3, where Q0 is incremented by one on every PLC scan when I0.2 goes and stays true.

Rung 4 provides a little bit different usage of the arithmetical macro "incR". Here, we use a "rising edge detector" macro in order to detect the state change of input I0.3 from OFF to ON. So this time, Q0 is incremented by one only at the rising edges of I0.3.

In the PLC rungs 5, 6 and 7 we see how the arithmetical macro "decR" could be used. In rung 5, Q0 is decremented by one, i.e. the process Q0 = Q0 – 1 is carried out when bI0.4 goes true. With this rung, if bI0.4 goes and stays true Q0 is decremented by one on every PLC scan. Similar is applicable to rung 6, where Q0 is decremented by one on every PLC scan when I0.5 goes and stays true.

Rung 7 provides a little bit different

```
.
      #include <definitions.inc>    ;basic PLC definitions, macros, etc.
      #include <cntct_mcr_def.inc>  ;Contact & Relay based macros
      #include <mv_ld_mcr_def.inc>  ;move_R, load_R, inv_R macros
      #include <arthm_mcr_def.inc>  ;Arithmetic macros
      #include <ff_mcr_def.inc>     ;flip-flop macros
.
;--------------- user program starts here ------------------------
      ld          FRSTSCN     ;rung 1
      or          I0.0
      load_R      00h,Q0

      ld          bI0.1       ;rung 2
      incR        Q0,Q0

      ld          I0.2        ;rung 3
      incR        Q0,Q0

      ld          I0.3        ;rung 4
      r_edge      0
      incR        Q0,Q0

      ld          bI0.4       ;rung 5
      decR        Q0,Q0

      ld          I0.5        ;rung 6
      decR        Q0,Q0

      ld          I0.6        ;rung 7
      r_edge      1
      decR        Q0,Q0
;--------------- user program ends here -------------------------
.
```

Figure 6: *The user program of UZAM_plc_8i8o_ex17.asm*

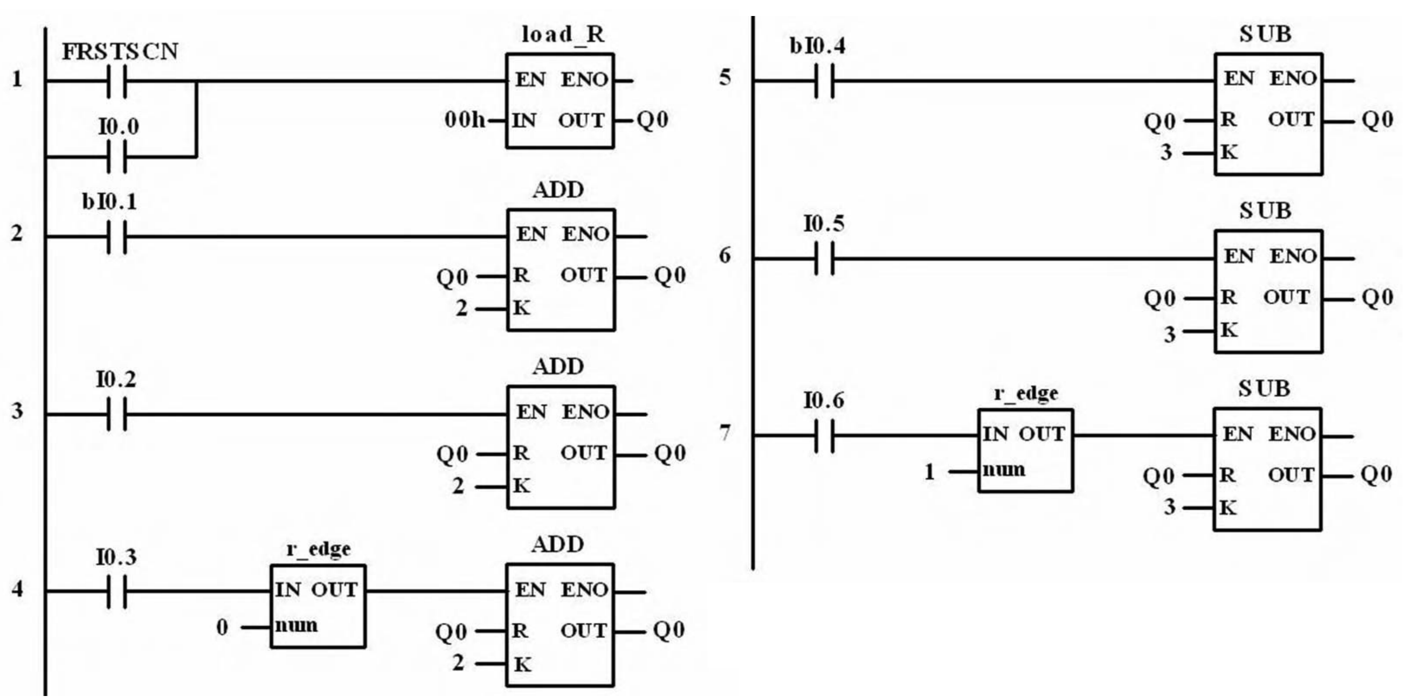
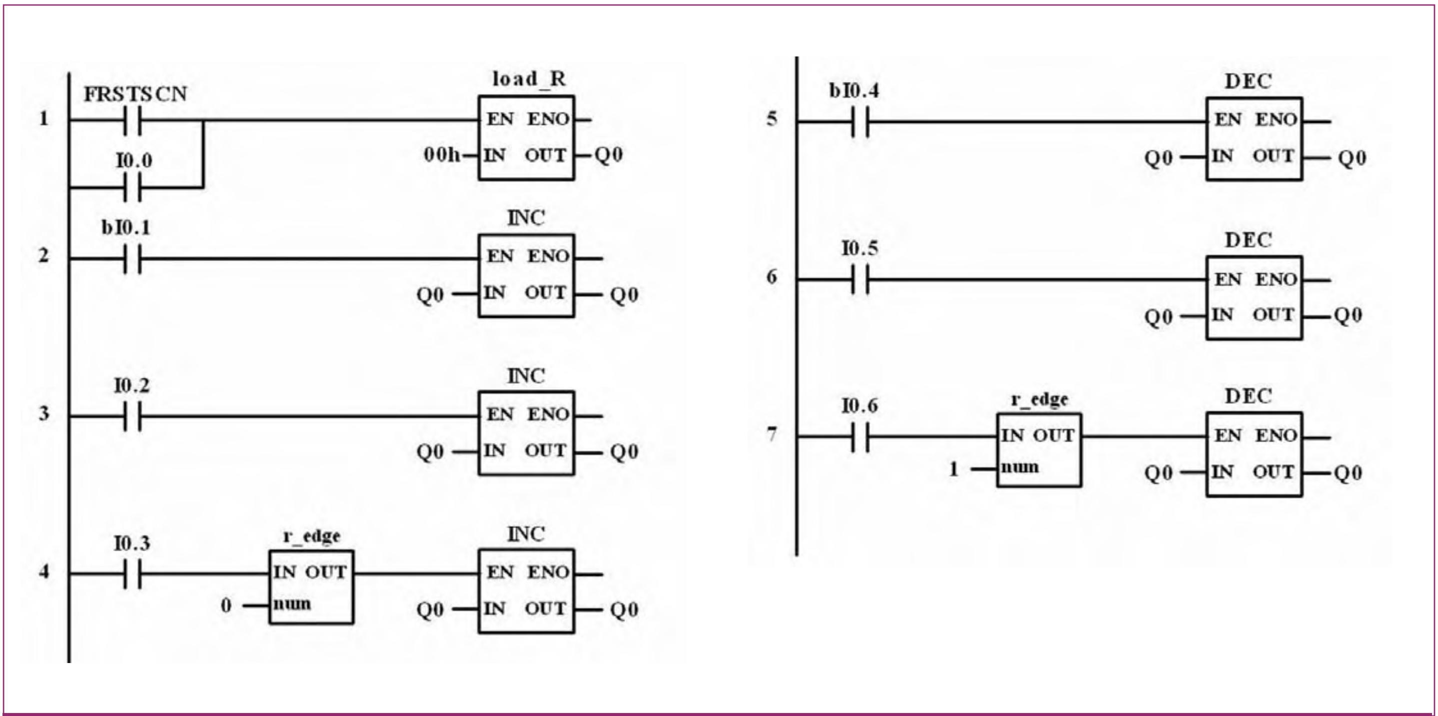


Figure 5: *Ladder diagram for the user program of UZAM_plc_8i8o_ex16.asm*



usage of the arithmetical macro "decR". Here we use a "rising edge detector" macro in order to detect the state change of input I0.6 from OFF to ON. So this time, Q0 is decremented by one only at the rising edges of I0.6. ■

If you've missed any of the previous articles in this series, you can now order it on line at ***www.electronicsworld.co.uk***

Faraz Hasan, Global Industrial and Appliance Marketing Manager at Tyco Electronics Corporation, Raychem Circuit Protection Products, analyses the advantages offered by PPTC devices which will help circuit designers provide safe and dependable products, comply with regulatory agency requirements and reduce warranty repair costs

Resettable CIRCUIT PROTECTION OPTIONS for Electric Motors and Industrial Controllers

THE POPULAR PPTC (polymeric positive temperature coefficient) resettable circuit protection device is now available in line voltage ratings to help protect power supplies, transformers, industrial controllers and electric motors.

The latest generation of PPTC devices includes components that are rated for line voltages of 120VAC and 240VAC and can be used in parallel for increased current capacity. Their low cost, resettable functionality and latching attributes make them a reliable, cost-effective circuit protection solution for power supplies, transformers, controllers and small and medium-sized electric motors.

Protecting an electronic circuit from damage due to excessive current or heat is the primary function of many circuit protection technologies. In the past, this protection took the form of a fuse or fusible link. In today's electric motor applications, resettable devices such as PPTC devices, CPTC (ceramic positive temperature coefficient) devices and bimetal circuit breakers are the preferred solution. These devices help protect against damage resulting from electrical short, overloaded circuit or customer misuse. **Table 1** compares the reset functionality and circuit conditions of the most commonly used devices.

PPTC Principle of Operation

Although often referred to as "resettable fuses", PPTC devices are non-linear thermistors used to limit current. PPTC circuit protection devices are made from a composite of semi-crystalline polymer and conductive particles. At normal temperature, the conductive particles form low-resistance networks in the polymer (**Figure 1**). However, if the temperature rises above the device's switching temperature (T_{SW}), either from high current through the part or from an increase in the ambient temperature, the crystallites in the polymer melt and become amorphous. The increase in volume during melting of the crystalline phase separates the conductive particles resulting in a large non-linear increase in the resistance of the device.

The resistance typically increases by three or more orders of magnitude. This increased resistance helps protect the equipment in the circuit by reducing the amount of current that can flow under the fault condition to a low, steady state level. The device remains in its latched (high resistance) position until the fault is cleared and power to the circuit is cycled – at which time the conductive composite cools and re-crystallizes, restoring the PPTC to a low resistance state in the circuit and the affected equipment to normal operating conditions.

Because PPTC devices transition to their high impedance state based on the influence of temperature, they help provide protection for two fault conditions – overcurrent and overtemperature. Overcurrent protection is provided when the PPTC device is heated internally due to I2R power dissipated within the device. High current levels through the PPTC device heat it internally to its switching temperature causing it to "trip" and go into a high impedance state.

The PPTC device can also be caused to trip by thermally linking it to a component or equipment that needs to be protected against overtemperature conditions, such as a motor. If the equipment temperature reaches the

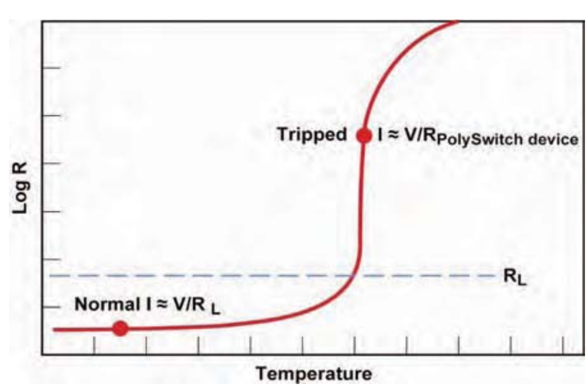


Table 1: *Comparison of reset functionality and circuit conditions in fuses and resettable circuit protection devices*

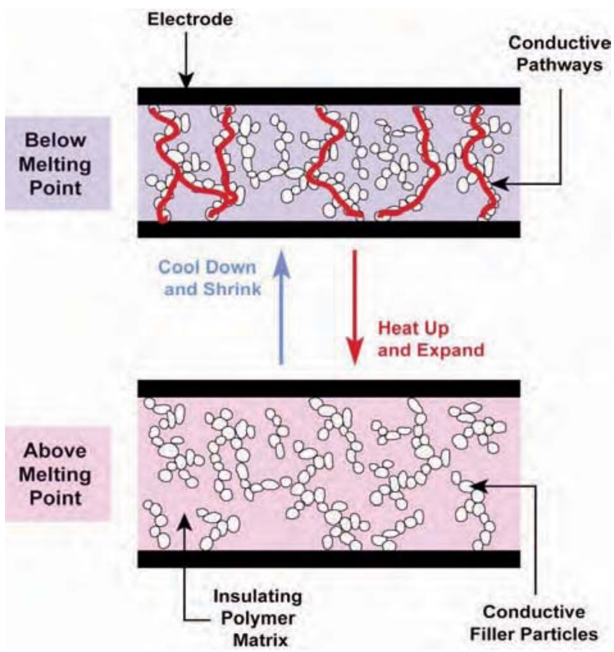


Figure 1: *PPTC devices protect the circuit by going from a low-resistance state to a high-resistance state in response to an overcurrent or overtemperature condition*

PPTC device's switching temperature, the PPTC device will transition to its high impedance state, regardless of the current flowing through it. In this way, the PPTC device can be used either to reduce the current to the equipment to very low levels, or as an indicator to the control system that the equipment is overheating. The control system can then determine what action is appropriate to protect equipment and personnel.

PPTC devices are employed as series elements in a circuit. Their small form-factor helps conserve valuable board space and, in contrast to traditional fuses that require user-accessibility, their resettable functionality allows for placement in inaccessible locations. Because they are solid-state devices, they are also able to withstand mechanical shock and vibration.

Motor Protection Strategy

Although generally reliable, electric motors are subjected to mechanical overloads, overheating, stalls, lost neutral, severe overvoltage conditions, humidity and other damaging factors.

Intermittent operation motors, such as those used in blenders and food processors, are usually designed to operate for a limited time. In general, operating these products for longer than the designed maximum limit usually results in stalling, overheating and, ultimately, failure. Fault conditions arise when the power is held on, either because of contact failure or customer misuse.

To prevent overheating, the circuit protection device used must "trip" quickly, but not sooner than intended, to avoid creating a nuisance condition for the user. The design challenge is to create a protection scheme that effectively protects the motor without nuisance tripping.

Nuisance tripping is often caused by inrush currents associated with certain electrical components found on motorized equipment. The major advantage of the PPTC device is that it can be specified with a trip current substantially below the normal operating current of the motor, but with a time-to-trip that is several times longer than a full system operating cycle, to avoid nuisance tripping.

Figure 2 shows how a PPTC device can be installed in a motor circuit to help protect against damage caused by overcurrent or overtemperature events. When the device is enclosed within the motor housing it reacts to the current flowing in the motor, as well as any temperature rise that may occur during a fault condition.

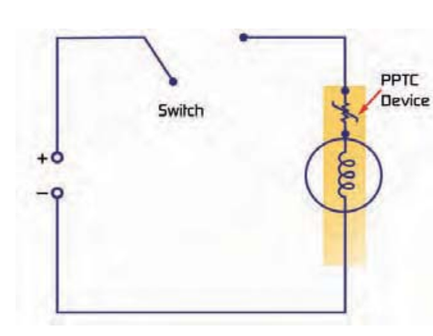
Performance Comparison of a Bimetal Breaker and a PPTC Device

Bimetal circuit breakers, although widely used to help protect electric motors, do not latch and require additional action to interrupt their on-off cycle. The bimetal strip is constructed of two different metals bonded together. When the bimetal's current rating is exceeded, heat generated by the excessive current causes the bimetal strip to bend and open a set of contacts to stop current flow. Once the current stops flowing and the temperature drops, the device returns to its normal shape, closing the contacts so current flow may resume. In the case of a stall, the bimetal circuit breaker continues to cycle until power is removed.

The cycling nature of this device has several disadvantages. Among those are material fatigue and a tendency to burn contacts, spark or weld shut. If the device "fails closed" it can cause overcurrent damage to the motor as well as sensitive follow-on electronics. Potential noise or "chatter" and electro-magnetic interference (EMI) can also make bimetal circuit breakers incompatible with advanced electronic control systems.

Recent testing by Tyco Electronics compared the thermal and electrical characteristics of a popular bimetal thermal

Figure 2: *A practical Li-ion/Li-polymer battery charging profile*



protector and the Raychem Circuit Protection PolySwitch LVR device, each installed on an icemaker motor. The protection devices were coupled to the motor winding and the motor shaft was locked during the test period. The voltage, current, temperatures of winding/core, and the temperature of the PPTC device and the bimetal protector were recorded during the test.

Figures 3 and **4** illustrate the results of the two tests. In the test using a bimetal circuit breaker, the motor winding reached a temperature of approximately 129°C at 60 minutes. This was significantly higher than the test that used a PPTC protection device, where the motor winding reached a temperature of 44°C within the same time frame.

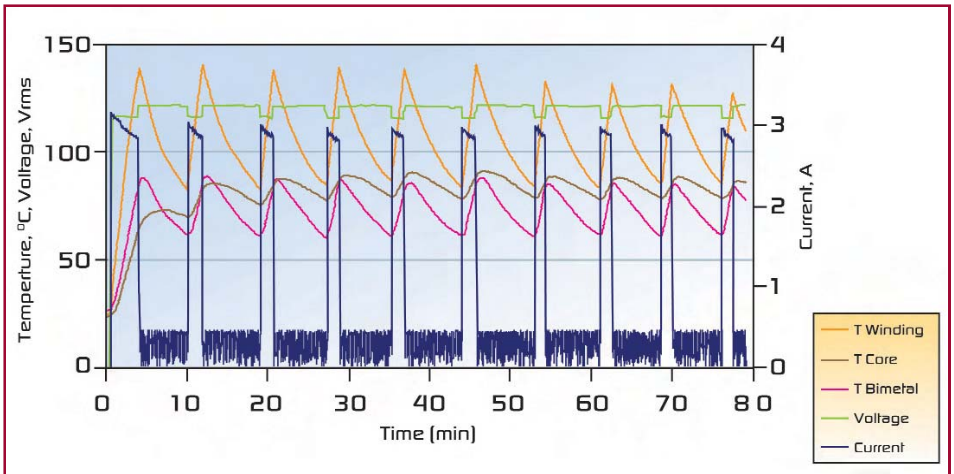


Figure 3: *Icemaker motor (rotor locked) test results with bimetal device protection*

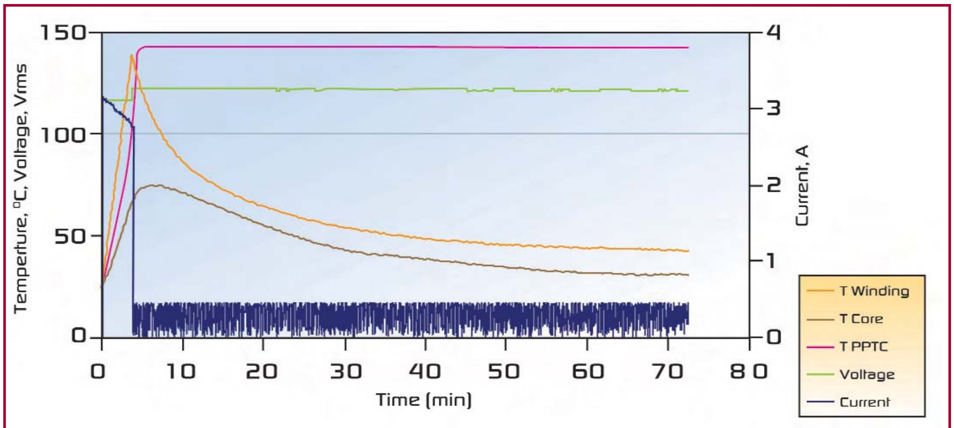


Figure 4: *Icemaker motor (rotor locked) test results with PPTC device protection*

Industrial Controller Protection Strategy

Traditionally, single-use fuses have been used to protect electronic circuits from overcurrent events. With this technology, when a wiring fault or part failure creates a condition in which excessive currents can flow, the fuse blows, breaking the electrical connection and preventing more widespread damage or fire hazards.

The problem with this approach is that a failure in one system component can disable other components downstream and throughout the system. Now, the fuse must be accessed and replaced on all the affected components before the system can be made operational again.

Controllers and remote devices that utilize resettable fault protection technology can help minimize the impact that failure has on the system, reduce the number of system components affected and shorten repair time. PPTC devices offer a practical alternative to fuse technology and help protect valuable electronic systems.

In many industrial controller applications, replacing single-shot fuses with PPTC devices allows designers to maintain the same level of overcurrent protection on the critical interfaces, but no longer necessitates fuse replacement or service when an external fault condition causes high current conditions in the system.

In addition to controllers, any remote sensor, indicator, or actuator that requires a power, analogue or communications bus interface can benefit from the use of PPTC devices. These system components are subject to damage caused by wrong wiring, power cross or loose neutral connections on AC mains inputs (see **Figure 5**).

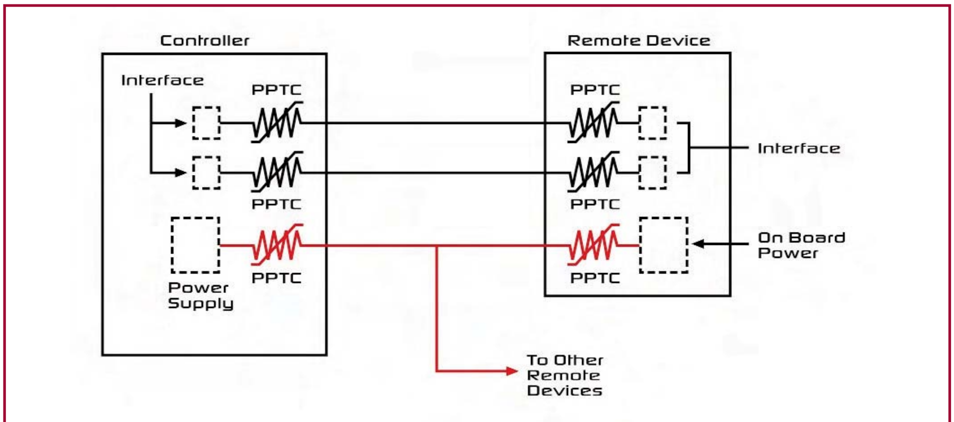


Figure 5: *PPTC devices help protect the interfaces between controllers and remote devices, as well as power inputs*

The New Generation

New generation PPTC devices are qualified for and widely used in appliance designs, compliant with the UL 1434 standard, and are compatible with lead-free solders and high-volume assembly processes. Their low resistance, fast time-to-trip, low profile and resettable functionality help circuit designers provide a safe and dependable product, comply with regulatory agency requirements and reduce warranty repair costs. ■

A NOVEL CIRCUIT FOR PULSE CODE MODULATION TO DIGITAL PULSE POSITION MODULATION CONVERSION

AN OPTICAL FIBRE is increasingly becoming analogous to a free space channel, as a large number of signals are being transmitted simultaneously through the fibre by using various techniques.

Several telephone operators have installed optical fibre links for various inland and under-sea systems. With advanced single-mode fibres like dispersion shifted and dispersion flattened fibres coming in the market, and with the popularity of the optical fibre amplifiers, Intensity Modulated Direct Detection (IMDD) systems are becoming quite popular (Franz et al. 1996). A large bandwidth available with these systems is not exploited by existing PCM systems used for data transmission.

The tremendous growth of portable communication terminals and personal computers has resulted into strong interest in high data-transfer rate wireless links for the interconnection of portable devices and for the establishment of Local Area Networks (LANs) (David et al. 1997). Wireless Infrared (IR) communication systems are often used to implement LANs (Barry 1994) and other interconnections due to various reasons.

DPPM technique is preferred to implement both O.F. as well as IR wireless systems due to a number of reasons, including high average-power efficiency, lower circuit complexity, low cost and the possibility of using time division multiplexing. It has been proved that receiver sensitivity below 100 photons per binary digit can be achieved with direct detection using DPPM, even at high data rates, thereby exploiting the large bandwidth offered by mono-mode fibres. DPPM systems over mono-mode fibres thus offer much improved receiver sensitivity. Hence, there has been a tendency to use DPPM instead of PCM wherever possible.

Since most of the modems for digital communication have been designed for PCM, a PCM-to-DPPM converter is required if DPPM is to be used for data transmission. Similarly, DPPM-to-PCM converter will be needed at the receiver end, as most of the destination units operate on PCM signals. Circuits reported in the literature for this purpose are usually complex (Ian 1983 and Bhat 2006).

In light of the above discussion, a novel and simple technique for PCM-to-DPPM conversion is being discussed here. A 3-bit parallel PCM-message signal is directly converted into the corresponding DPPM signal, using the proposed circuit. Receiver circuit for DPPM-to-PCM conversion is also presented.

Circuit Description of the Proposed PCM-to-DPPM Converter

The circuit diagram for proposed PCM-to-DPPM converter is shown in **Figure 1**. The 3- bit parallel PCM data, to be converted in to DPPM signal, is generated by a 3-bit word generator. The 3-bit PCM data is applied to the comparator circuit as shown in the Figure 1. Each bit of the PCM signal is individually compared with a corresponding bit of a 3-bit words generated by a 3- bit linear counter.

The comparator circuit is implemented using XOR gates and a NOR gate as shown in **Figure 2**, wherein the PCM bits are applied at I1, I2 and I3 and the linear counter is connected arbitrarily at C1, C2 and C3. The comparator output is given by:

$$Y = (I1 \oplus C1) + (I2 \oplus C2) + (I3 \oplus C3) \qquad (1)$$

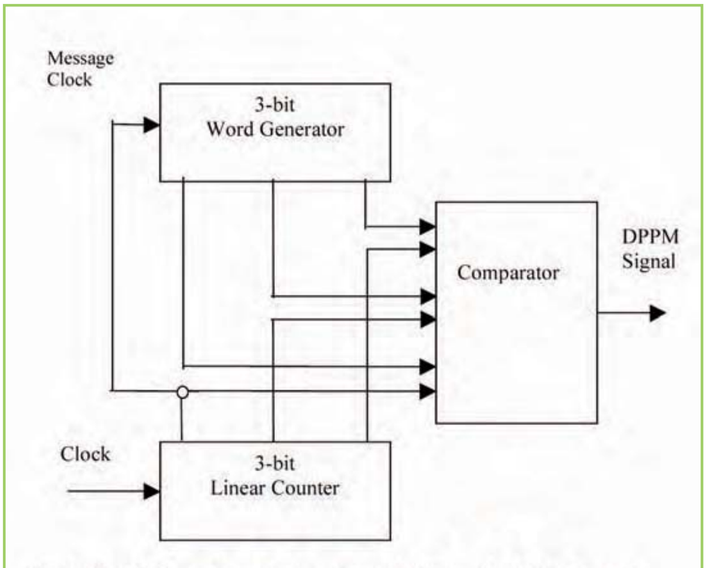


Figure 1: *Circuit diagram for the proposed PCM-to-DPPM converter*

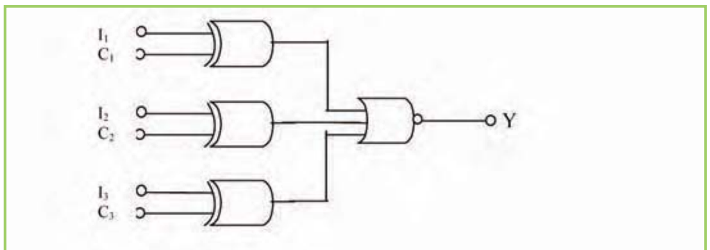


Figure 2: *Circuit diagram of a comparator*

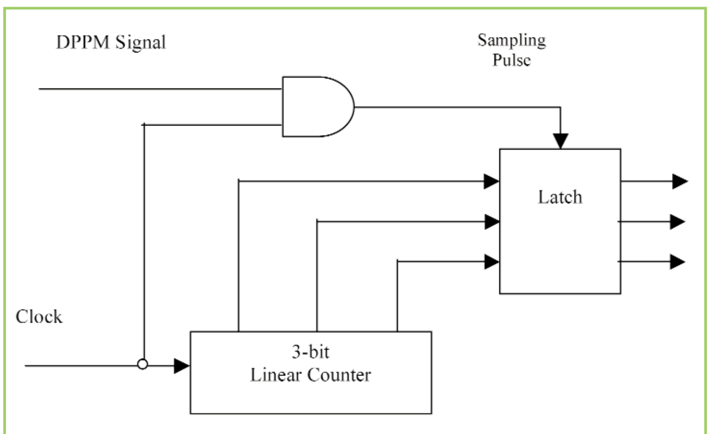


Figure 2: *Circuit layout of DPPM-to-PCM conversion*

The clock signal for the PCM word generator (message) is taken from the most significant bit of the linear counter as shown in Figure 1. Therefore, the clock frequency of the linear counter is eight times the message clock. Thus, during a particular message available at the output of the PCM generator, the linear counter generates all the eight possible

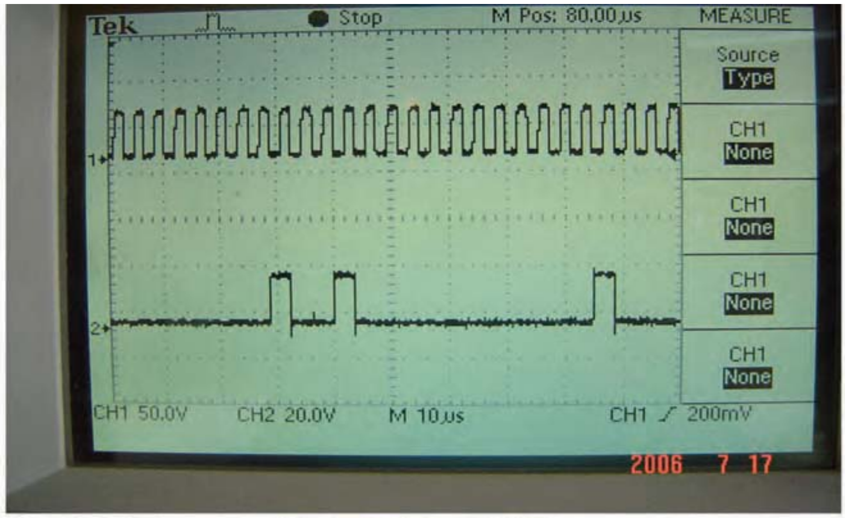
3-bit words. Every time the linear counter reads '000' the PCM word generator receives a high-to-low pulse and generates a new message word.

Now, every time a new word is generated from the PCM word generator, it is continuously compared with all the states of the linear counter by the comparator circuit. When the counter generates the same 3-bit word as the PCM word, the comparator output goes to a high state. However, when the counter generates a different 3-bit word, the comparator output will remain low.

It is evident that the PCM word will be exactly equal to one out of the eight possible 3-bit words generated by the linear counter in one message interval. Since the PCM word being different from the rest of the seven 3-bit words generated by the counter, the output of the comparator thus remains low during this time. This arrangement divides the message bit interval into eight different sub-intervals, and outputs a high pulse on one of the sub-intervals during a message word interval. The position of the pulse depends upon PCM word. This high pulse is then transmitted as a DPPM signal.

To clarify the working of the proposed circuit, let us consider that the PCM word is '101' and the counter has started from '000'. After the counter receives five clock pulses, the counter reads '101'. When it is compared with the PCM data being already '101', the output of the comparator circuit goes high. For rest of the three states viz. 110, 111 and 000, the comparator output remains in '0' state. Thus, a high pulse is transmitted at a particular sub-interval of the message signal. Hence the output signal is a DPPM signal.

Figure 4a: *Waveform generated by the circuit shown in Figure 1 (Upper: Clock signal), (Lower: DPPM signal)*



Receiver Circuit

The circuit diagram for DPPM to PCM converter is shown in **Figure 3**. The received DPPM signal is applied to one input of an AND gate. The other input of the AND gate is excited by the clock signal, synchronized with the clock signal used at the transmitter. The output of the AND gate generates sampling pulses for the latch circuit.

In this circuit 74LS374 has been used for latching purpose. This chip transfers the data to the output on receiving a low to high pulse at its clock input. The inputs of the chip are driven by the 3-bit linear counter. This counter is synchronized with the counter used at the transmitter, i.e. the two counters read the same data at any point in time. When the chip senses a low-to-high signal at its clock input, the data available at the output of the counter is transferred and latched at the output of the IC 74LS374. Since a low-to-high pulse is generated at PCM-to-DPPM converter, when the counter output and the PCM signal generator are the same, therefore, at the receiver the same counter state is latched at the output on arrival of the particular DPPM pulse. Hence, the DPPM signal is converted back into corresponding 3-bit PCM data.

Experimental Results

The proposed circuit has been implemented in hardware for performance evaluation. The clock signal required by the circuit was obtained from a function generator. Further, the clock signals used by the transmitter, as well as the receiver, were assumed synchronous with each other as the same clock was applied to both the systems for experimental purpose. Both linear as well as random data was used for the investigation. The results of experimental investigation conducted over the proposed scheme are shown in **Figure 4**.

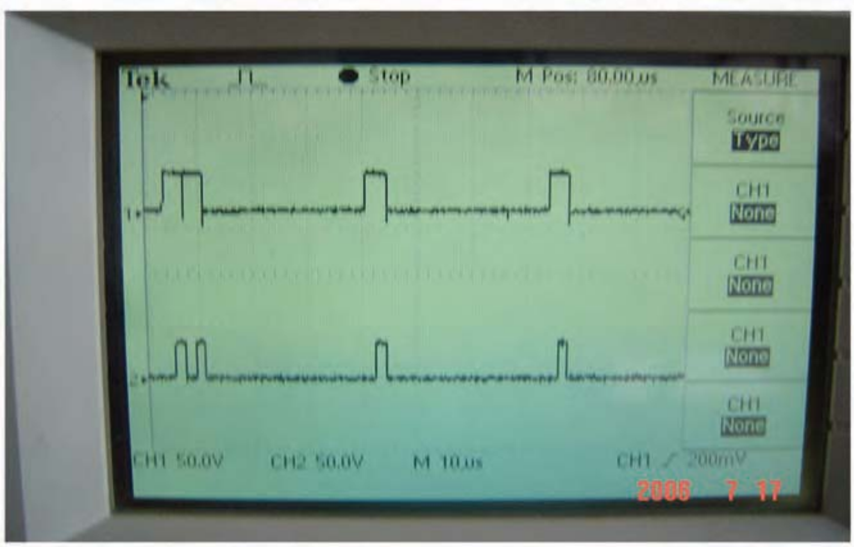
Exploiting the Bandwidth

The tremendous bandwidth available with optical fibres (mono-mode) is not exploited by existing PCM systems. This excess of bandwidth can be exploited by DPPM, because DPPM offers much better performance and increased receiver sensitivity than PCM.

A novel technique for PCM-to-DPPM conversion has been presented here. The proposed circuit was implemented in hardware and the results carried out over experimental investigation were satisfactory.

G. M. Bhat
India

Figure 4b: *Waveforms*
(Upper: Transmitted DPPM signal)
(Lower: Sampling pulses for latch circuit at receiver)



WATCH OUT FOR THAT LOSSY CABLE

I read Ian Darney's letter discussing transmission line transients in the June issue of 'Electronics World' magazine with some interest. The conclusions deserve closer scrutiny.

There seems to be a false assumption that the line in question was a very good one. Not so. The PVC insulation on the cable used is notoriously lossy even at low radio frequencies and increasingly so as the bandwidth increases.

This means that the propagated wavefront rapidly degraded as it moved to the open and again on its reflected passage as energy at the upper frequencies was dissipated. Hence, 'sharp edges' and 'steep wavefronts' were progressively 'rubbed off' and 'flattened' together with a reduction in the peak amplitude. These factors surely account for much of what was observed.

One must also question the integrity of the instrumentation. In particular, the validity of the current transformer system should have been established by tests on a nearly ideal line model.

In passing this "balanced line with one element grounded" configuration is mentioned in Figure 38 on page 17 of Terman's Radio Engineering Hardbook.

S. Hassell UK

Still Unable to Answer a Simple Question

After reading the letters written in criticism of Ivor Catt, I was puzzled as to why there was a controversy that required such negative rebuttals. The letter written by Ivor Catt in Electronics World clearly states the problem. This is that the scientific community of experts is unable to answer a simple problem in electromagnetic theory in a way that presents a coherent answer to an elementary question regarding the motion of electric current in wires.

Since the textbooks maintain that charge causes electric field and that movement of this charge causes magnetic field, the answer to the Catt question poses a crucial test of the textbook assertions regarding the source of electro-magnetic fields. The result that experts in the field can not agree upon the correct answer to the Catt question is an illustration of Catt's assertion that the tradition physical explanation of the problem is incoherent and requires revision.

I think that he is correct in demanding an investigation by the scientific authorities, if only to insure that the textbook answers are all coordinated and give the same answer to this question, rather than giving different and contradictory answers to the question. The reason an investigation or conference to discuss the problem is not wanted by the scientific authorities is that the participants are likely to produce no consensus answer to the question, since they all disagree as to the correct substance of the answer. We see this disagreement in the two different answers given here in Electronics World by Catt's critics.

Those of us who are really interested in the problems of electromagnetic theory would like to have a coherent and rational theory of electromagnetism. Alas, currently there is no such theory at all. The current textbooks teach that the magnetic field vector is the magnetic induction vector B and not the magnetic intensity vector H. This renders the Maxwell equations incoherent. I think this is a much more serious problem than the Catt question. But, if the scientific establishment can't realize that there is a problem in electromagnetic theory regarding the simple Catt question, then it is certainly hopeless that they will straighten out the mess they have created with regard to Maxwell's equations.

I think some action, as requested by Ivor Catt in his letter, needs to be taken by the leadership of the scientific community to resolve the problems in electromagnetic theory that he has raised.

Harry Ricker

PROVOCATIVE QUERIES

I refer to a Letter in the May issue of Electronics World by Ivor Catt, and subsequent Letters by John Ellis and Ian Darney in June.

Besides his technical matter, Catt raises the all important issue of censorship in the publication of scientific papers. There can be no doubt that censorship is rife in matters of scientific publications and anybody who thinks otherwise is either not telling the truth or living in fantasy-land. It is, therefore, to the credit of Electronics World that it has published Catt's letter.

However, the letters by Ellis and Darney do not address the issue of diametrically opposed views expressed by certain experts in the field, as reported by Catt. Such contradictions indicate a definite measure of confusion in established thinking on the subject of electrodynamics and are symptomatic of a deeper malaise in the discipline. No theory is absolute and, so, is always a work in progress. [The field of] Electrodynamics has stagnated for a considerable period of time and is in dire need of improvement. This can only come about by open discussion, free of fear or favour, which, alas, has for a long time been foreign to the circles of science and engineering.

Catt's queries are provocative in that they actually solicit some real thought about the foundations of contemporary theoretical electrodynamics from which other problems with the theory can be revealed and analysed. For instance, the Maxwell-Heaviside equations, as they are always given in textbooks, and almost always in the other literature, pertain to stationary media in that they can be easily generalised to moving media, by which they become Galilean invariant. This stands in stark contrast to the tenets of Einstein's Special Theory of Relativity, which Einstein founded upon his conception of the invariance of Maxwell's usual equations, evidently quite ignorant of the fact that Maxwell's equations are easily made Galilean invariant by means of the very same mathematical apparatus used by fluid dynamicists everyday.

This was first pointed out by Hertz and has been developed in quite some detail by subsequent theoreticians, such as the late British scientist Charles Kenneth Thornhill. But what electrical engineer knows of this work? What 'authoritative' physicist knows of this work? Pitifully few! – because proponents of the established views take deliberate measures to prevent the publication of such works in the journals they control in order to protect their investments (of one sort or another) – convenient for vain glory and self-aggrandizement but anathema to the progress of scientific thought and its applications.

I think it important that Electronics World continue to publish Catt and other authors who are brave enough to voice their objections to what is deemed 'truth', simply by proclamation and authority.

Readers of your magazine are entitled to have before them all the facts so that they can come to a decision on the balance of the evidence, not simply by what so and so might have to say. Authority has no place in science and the democratic vote of scientists and engineers does not determine the nature of the physical world.

Stephen J. Crothers Australia

Contradictory 'Theories'

In the process of an unseemly denunciation of Ivor Catt for his having pointed out "that two eminent scientists provided completely contradictory answers to that question" (a documented fact readily discovered by perusing Catt's many web pages on this topic), two more authors have again provided contradictory responses to The Catt Question, at least in the portions of their responses that can be made sense of.

Both letters in the June, 2009 issue of EW introduce new electricity theories – "Ellis Theory", in which the upper conductor is not charged until the reflected pulse returns, and "Darney Theory", in which the distance between the conductors is a critical variable. Both of these new theories contradict mainstream electromagnetic theory, as well as contradicting each other. Neither one answers The Catt Question – being new theories, whereas The Catt Question is directed at what passes for mainstream theory. Taken together, the two letters form a beautiful illustration of the occulted confusion that reigns at the heart of conventional, mainstream, electromagnetic theory.

We have seen this phenomenon before, in attempting to answer The Catt Question the respondent ends up creating a new electromagnetic theory! Mr Darney even ends with a declaration that "there was certainly no need to invent a completely new theory", after inventing one.

One reason these new theories abound is that conventional electromagnetic theory is an irrational morass of additions, omissions and contradictory statements, leaving the door open for individual interpretation, much like the runes or Tarot cards.

In the new "Ellis Electricity Theory", electric current in the lower wire does not start up until the initial pulse has travelled all the way from the source to the load and begins its return journey. In the new "Darney Electricity Theory" electric current in the lower wire does not start up until some sort of "current" emanating from the upper wire is, somehow, completely intercepted by the lower wire.

Mr Darney claims that "only one explanation is possible: current is departing from the transmission line via capacitive coupling between cable and environment. Moreover, it must be emanating from the signal conductor, since that is the only conductor that is being energized".

Here is, apparently, part of Mr Darney's new theory – that electric current can depart from a wire and move through free space, but only (?) if the current was on a wire at a particular potential relative to another wire. Perhaps the author meant to say "electromagnetic radiation", but he repeats this assertion as "radiated current" and as "each incremental step in the forward direction delivers a transient current pulse into the environment". The reader is left to wonder what the disposition and consequences of these "radiated currents" might be.

The primary hypothesis of Mr Darney's new electricity theory appears to be a partial causality claim, that 'moving electrons on one of the two wires in an electric circuit cause electrons on the other wire to move, but only after a specific time delay due to the distance between the wires'. If this were true, we would find all sorts of applications that could use this principle. We could, for example, design signal delays around it.

A second hypothesis of "Darney Theory" might be that 'energy radiated into free space, as an antenna does, can be completely intercepted by a nearby wire', a hitherto unknown process. If this hypothesis was true, then radio antennae could not work; any nearby metal could completely absorb the radiation.

Ivor Catt, the electrical engineer and scientist, has indeed and long since "set up an experiment, observe how an actual line does respond to a step input, then... analyse and assess the results" as part of his pioneering contributions to high-speed digital logic, electronic systems integration, long-distance communications and fundamental physics.

I urge the experimentalists to repeat these experiments and see for themselves how a transmission line actually "charges" and "discharges".

Kurt Knalty is one such experimenter who has recently obtained the same results that Catt reported back in the 1960s: results which are as different from conventional electromagnetic theory as day is from night.

Forrest Bishop US

CONFLICTING AND VAGUE POSITIONS

I read with interest Ivor Catt's May letter to Electronics World and the June responses by John Ellis and Ian Darney. I would like to congratulate Electronics World for publishing Catt's letter and the responses; albeit I found the responses rather dismissive of the conflicting and vague positions held by major figures in the physics community in relation to the questions that Catt had raised.

It seems to me that this is evidence that many issues must still exist with current theory and one can only ponder as to the reasons why the 'Establishment' seems to have been so reticent for so long to explore the paradoxes of the theory that is being taught to our children at schools and universities.

It seems to me that there's an ever-increasing list of issues raised by Catt and others, from what is apparently a fundamentally flawed theory and one would expect (or indeed hope) that the truth would eventually come out, albeit against the apparent inertia of vested interests.

That being the case, it still could only happen (hopefully) by the efforts of determined and persistent people like Catt, without which the inertia of the status quo would simply retain the current flawed model taught to our children.

Ian Montgomery Australia

WHAT IS LTE?

Helen Karapandžić's article on LTE was very interesting (June issue of Electronics World). If, as she says, LTE "technology can deliver data at a sixth of the cost of UMTS", then I'd say "Go for it!"

Maybe in a future article someone might explain what LTE is and, while they're at it, HSPA, UMTS, HSPA+ and MIMO.

Donncha Butler Ireland

Editor replies: We have had articles in Electronics World magazine on this subject in the past. As a short summary LTE, or Long Term Evolution of Universal Terrestrial Radio Access Network, is a mobile broadband standard, used for mobile, fixed and portable wireless broadband access. It is an update to UMTS; UMTS-TDD, HSDPA/HSUPA and LTE/4G all build upon UMTS-FDD.

LTE is the standard that will allow faster data rates, optimized for IP, packet-based traffic: downlink peak data is expected to offer up to 100Mbps with a 20MHz bandwidth; uplink: 50Mbps, also 20MHz.

PLEASE EMAIL YOUR LETTERS TO: svetlana.josifovska@stjohnpatrick.com

The publisher reserves the right to edit and shorten letters due to space constraints

TIP 1: INPUT NOISE OF POWER AMPLIFIERS – A FAST CALCULATION APPROACH

By Burkhard Vogel of Buvocon-Burkhard Vogel Consult GmbH

IT DOESN'T MATTER if BJTs, JFETs or valves (triodes) are chosen as active input devices for power amplifiers (PA) concerning white noise production mechanisms, as power amplifiers do not differ very much from op-amps. Nearly all of the white noise is produced in the PA's first gain making active device and its associated emitter or source or cathode g_m degenerating resistor.

For a quick calculation and assuming that the source resistance is rather low (< 50R), the noise production of the other bias and gain setting passive components, as well as of the following gain stages, can be ignored. The same applies for the calculation of the 1/f region of the noise spectrum. This should only be taken into account with corner frequencies > 250Hz. **Figure 1** shows the general noise situation of an amplifier PA1. All its noise voltage and noise current is concentrated in the two input noise generators $e_{N.in}$ and $i_{N.in}$.

Equations 1 to **3** calculate noise voltages and currents for a singleton BJT/JFET/triode input device à la **Figure 2** configuration (= ID1), including emitter or source or cathode resistor R2. The set of equations in **Equation 4** calculate parallel operation of n active devices paralleled. To ensure the same DC conditions for each of the devices the single resistors R1, R2 need division by n.

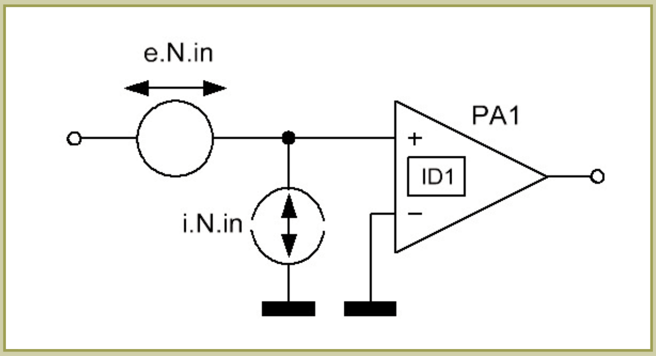


Figure 1: *General noise voltage and noise current situation of an amplifier*

$$\text{BJT}: \quad e_{N.ID1.b} = \sqrt{\frac{2k^2T^2}{qI_C}B + \left(r_{bb'} + R2\right)^2 i_{N.in.b}^{\;2} + 4kT\left(r_{bb'} + R2\right)B} \qquad \textbf{(1)}$$

$$i_{N.ID1.b} = \sqrt{\frac{2qI_C}{h_{FE}}B}$$

$$\text{JFET}: \quad e_{N.ID1.f} = \sqrt{\frac{8kT}{3}\left|\frac{1 + g_{m.f}R2}{g_{m.f}}\right|B} \qquad \textbf{(2)}$$

$$i_{N.ID1.f} \approx 0$$

$$\text{Triode}: \quad e_{N.ID1.t} = \sqrt{4kT\left(\frac{3.06}{\left|g_{m.t}\right|} + R2\left[\frac{r_a + R1}{r_a + R1 + (1+\mu)R2}\right]^2\right)B} \qquad \textbf{(3)}$$

$$i_{N.ID1.t} \approx 0$$

(Abbreviations: b = BJT, f = JFET, t = triode, N = noise, g_m = mutual conductance, k = Boltzmann's constant, q = electron charge, B = bandwidth = 1Hz for equivalent input noise density, I_C = BJT collector current, h_{FE} = BJT current gain at a certain I_C, $r_{bb'}$ = BJT base spreading resistance (calculation or measurement of $r_{bb'}$ see the author's "*The Sound of Silence*", ISBN 978-3-540-76883-8), r_a = triode internal resistance, μ = triode gain factor, R1 = triode plate resistor)

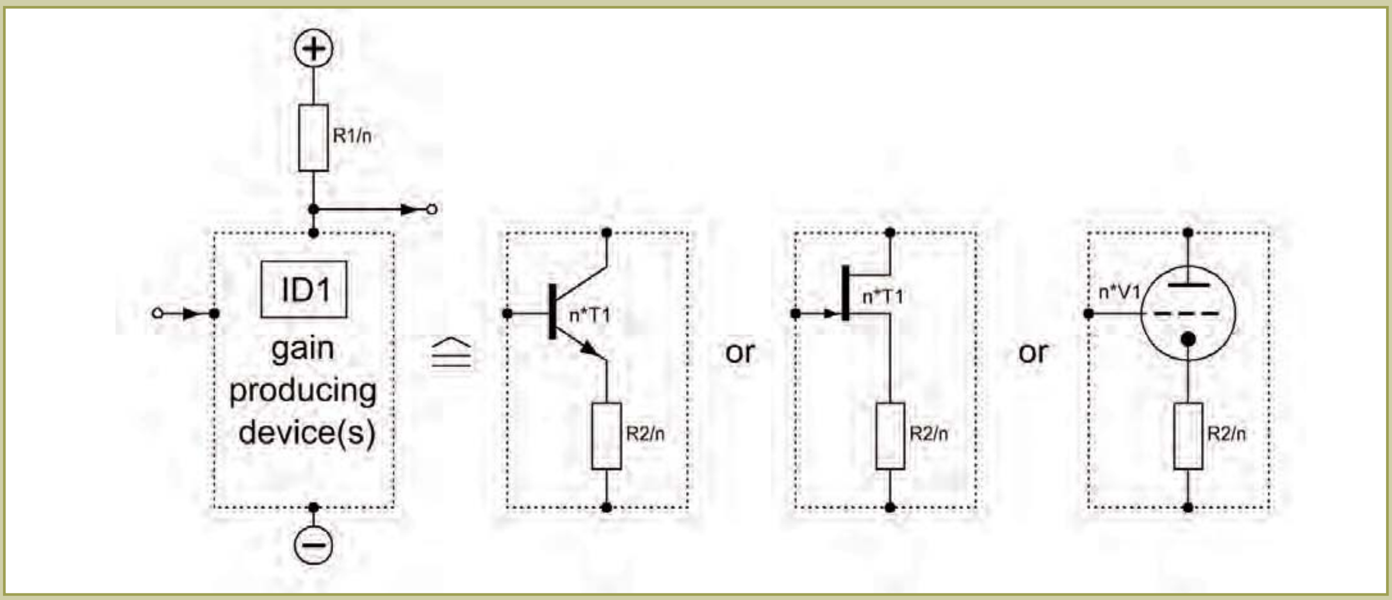


Figure 2: *Singleton input device configuration*

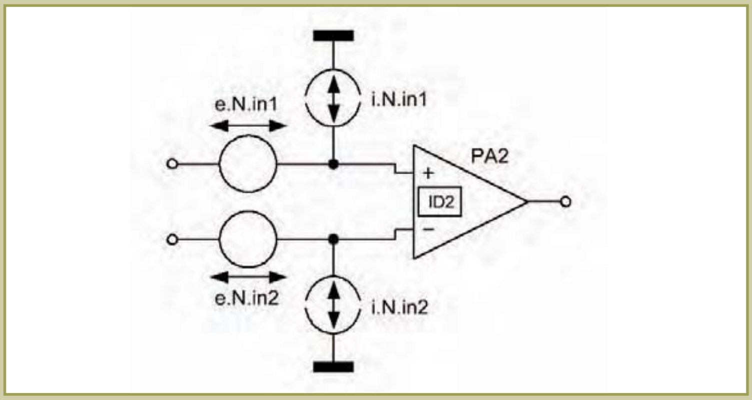


Figure 3: *General noise voltage and current situation of an amplifier with a long-tailed input pair of active devices*

$$\begin{aligned}
&\text{n BJTs}: \quad e_{N.ID1.nb} = \frac{e_{N.ID1.b}}{\sqrt{n}} \\
&\qquad\qquad i_{N.ID1.nb} = i_{N.ID1.b}\sqrt{n} \\
&\text{n JFETs}: \quad e_{N.ID1.nf} = \frac{e_{N.ID1.f}}{\sqrt{n}} \\
&\text{n Triodes}: \quad e_{N.ID1.nt} = \frac{e_{N.ID1.t}}{\sqrt{n}}
\end{aligned} \qquad \textbf{(4)}$$

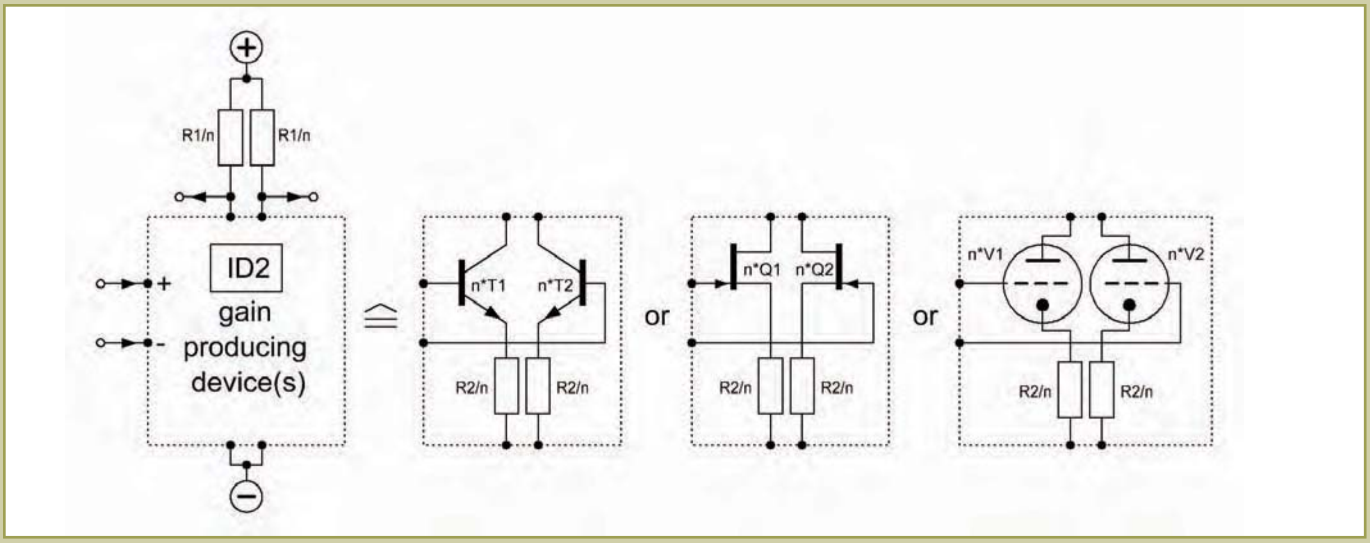


Figure 4: *Long-tailed input device configuration*

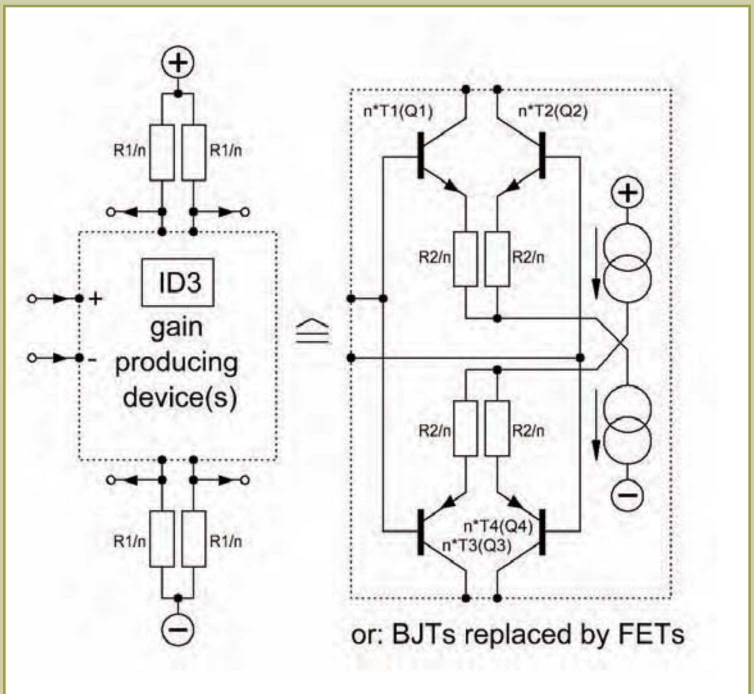


Figure 5: *NPN/PNP paralleled long-tailed input device configuration*

A very different picture comes up with a PA input section formed by a long-tailed pair of input devices (PA2). The general noise voltage and current situation show in **Figure 3**:

ID2 represents PA2's input device configuration. Taking also into account R2, a carefully matched pair of BJTs/JFETs/triodes in a long-tailed input configuration à la **Figure 4** or carefully matched multi (n) BJT/JFET/triode long-tailed input pairs will produce the noise voltages and currents that are given in **Table 1**.

ID3 of **Figure 5** can replace ID2. Table 1 also shows the respective equations, including all R2 noise effects.

Table 1 sums up all the fundamental mathematical relationships for the input referred current noise densities (BJTs only) and voltage noise densities of the different types of input configurations for each input. Based only on one calculation for a single active device (ID1), for these input configurations application of Equations 1 to 3 will lead to the desired results.

By taking only the long-tailed solutions ID2 and

type of i/p noise	current noise density for each i/p	voltage noise density for each i/p		
type of device	BJT	BJT	JFET	Triode
number of devices paralleled	n	n		
n * singleton	$i_{N.ID1.nb}\sqrt{n}$	$\frac{e_{N.ID1.nb,nf,nt}}{\sqrt{n}}$		
n * long-tailed pair	$i_{N.ID1.nb}\sqrt{n}$	$\frac{e_{N.ID1.nb,nf,nt}}{\sqrt{n}}$		
n * complementary long-tailed pair	$i_{N.ID1.nb}\sqrt{2n}$	$\frac{e_{N.ID1nb,nf}}{\sqrt{2n}}$		no solution

Table 1: *Overview of the basic calculation relationships for i/p referred equivalent current noise and voltage noise densities*

type of i/p noise	op-amp equivalent voltage noise density		
type of i/p device	BJT	JFET	Triode
number of devices paralleled	n		
n * long-tailed pair	$\frac{e_{N.ID1.nb,nf,nt}}{\sqrt{n}}\sqrt{2}$		
n * complementary long-tailed pair	$\frac{e_{N.ID1.nb,nf}}{\sqrt{n}}$		no solution

Table 2: *ID2 and ID3 configured as op-amp input: equivalent input voltage noise densities*

ID3 and, for comparison reasons, putting them in an op-amp configuration to get the respective data sheet given op-amp equivalent input voltage noise densities and current noise densities all noise voltages of Table 1 have to be multiplied by the factor "√2", whereas the noise currents will not change. Hence, the respective op-amp circuitry will look like Figure 1 without ID1. With reference to the formulae given in Table 1, the op-amp equivalent noise voltages for each type of n devices (b, f and t) are listed in **Table 2**.

It always makes sense to calculate the total noise voltage of the triode's anode/plate resistor R1 as well. It consists of R1's white noise based noise voltage $e_{N.R1}$ and its excess noise voltage $e_{N.R1.ex}$. Both have to be summed up. As long as their rms sum is more than 10dB smaller than the triode's noise voltage that was calculated with the equations given here and multiplied with the gain factor of that respective triode gain stage, then, to simplify things the total noise voltage of R1 can be ignored. Otherwise, it has to be taken into account too. ■

869MHZ TRANSMITTER CAN ACHIEVE 5KM RANGE

The TX3H-869.5-15 from London-based low power radio specialist Radiometrix is an FM transmitter module achieving a power output of 450mW at 869.5MHz. It is fully pin-compatible with the company's established range of SIL TX modules and is a drop-in UHF replacement for the TX1H VHF product, having near identical dimensions of only 45 x 17 x 6mm.

TX3H is an excellent choice for the designer of a licence exempt wireless data application where the size of antenna is restricted yet a range in kilometres is also specified. The module can support data rates of up to 15kbits/s and has a potential range of 5km or more when paired with Radiometrix receivers such as the new RX3G, depending on the type of antenna used and the environment.

TX3H-869.5-15 operates within the European 869.40-869.65MHz sub-band allocation although custom frequencies may be accommodated on request. It has been designed to comply with EN301 489 (EMC) and EN300 220 (SRD) radio standards.

This module can be employed in a large number of end applications, such as asset tracking systems, meter readers, industrial telemetry/telecommand equipment, data loggers, in-building environmental monitoring/control systems, social alarms, high-end security/fire alarms and vehicle data up/download.

www.radiometrix.com

LPRS UNVEILS LATEST MULTI-CHANEL LOW POWER RADIO MODULES

LPRS has launched the latest narrowband radio modules from Circuit Design. The ultra-compact transmitter CDP-TX-05M-R and receiver CDP-RX-05M-R supersede the very successful CDP-TX-04S-R and CDP-RX-03AS/BS-R modules, maintaining their remarkable size and low power consumption (10mW) while offering multi-channel operation.

Multi-channel operation allows the user to ensure reliable wireless communication by on-site selection to a channel that is not affected by local interference. The new modules operate at 426MHz for Japan, 434MHz or 869MHz for Europe and 915MHz for the USA and each may be switched between four pre-programmed channels. In addition the alternative frequencies can be customized according to the customer's requirements.

The compact CDP-TX-05M-R and CDP-RX-05M-R are supplied in a robust, shielded enclosure and require just a small number of external components to produce a complete wireless system for industrial use. They are both pin-compatible with the existing CDP-TX-04S-R transmitter and CDP-RX-03AS-R receiver modules that have already proved to be very well received in the Japanese and European markets for their quality and reliability.

High frequency stability is ensured by the use of a TCXO as the reference oscillator circuit of the radio module and the operating temperature range has been increased to -20°C to +65°C.

With the output of 10mW (1mW in Japan, 0.5mW in the US) authorised for narrowband FM and double superheterodyne receivers with high receive sensitivity in the European harmonized ISM band, a communication range of 600m (line-of-sight) is possible.

www.lprs.co.uk

INNOVATIVE MACHINED ALUMINIUM SHELL FOR SPACE CONNECTORS

ITT Interconnect Solutions has developed an innovative machined aluminium shell for its K128 and K134 space connectors, which greatly reduces the possibility of misconnects during testing and final assembly, as well as offering substantial weight reductions of up to 15.4% over conventional brass shells.

The connectors have optional polarization keys which ensure that similar pin layouts and genders can be differentiated easily from one another. Customers have a choice of eight different key locations on the plug and socket of each aluminum connector, which are then added to the base part designation for ease of ordering.

Manufactured from a high-stress aluminium alloy with a heavy, non-magnetic nickel under plate and over-plated with gold, these lightweight connectors are stronger than conventional connector shells.

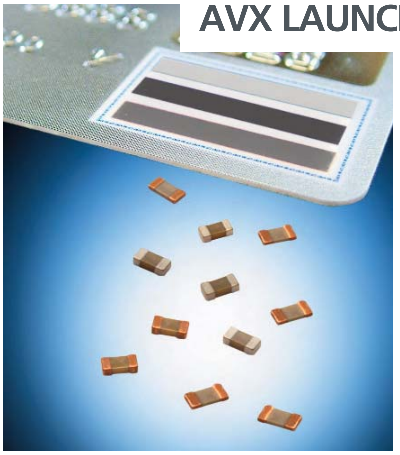
Available in two different series, K128 and K134, all sizes and pin layouts mate with standard ITT space D-subminiature connectors built to NASA/GSFC/ESA dimensions. Weight savings, when compared to standard brass shell connectors, range from 8.1% for size D (50 or 78 pins), right up to 15.4% for shell size E (9 or 15 pins).

The K128 machined aluminium connectors are available in standard and high-density configurations as solder cup, crimp with optional grommet, straight PCB and 90 degree designs.

The second series, K134 aluminium blind hole 90 degree PCB connectors, is available in standard and high density versions, and six different shell sizes with 15, 26, 44, 62, 78 and 104 contacts.

www.itt.com

AVX LAUNCHES ULTRA THIN 0402 SURFACE MOUNT CERAMIC CAPACITORS



AVX Corporation has just released a new series of ultra thin ceramic capacitors targeted at applications where low profile is vital, such as smartcards, high density SIM cards and memory modules.

The new UT parts have the same footprint as 0402 devices but are only as thick as conventional 0201 products. However, they retain the same voltage and capacitance ratings of the standard thicker 0402 capacitors.

Thanks to a novel chemical termination system which allows very precise and highly repeatable termination thickness and dimensions, parts can be produced that measure just 0.3mm high with a capacitance value of 10nF and a voltage rating of up to 25V. Operating temperature is -55 to +85degC. Insulation resistance is 100,000MΩ minimum. ESL is 164pH; ESR is 75.6mΩ.

The new UT ceramic capacitors suit applications anywhere the thickness of components is the major hurdle in the design. AVX also expects to introduce even thinner 0.15mm devices for embedding within PCBs, saving even more space.

www.avx.com

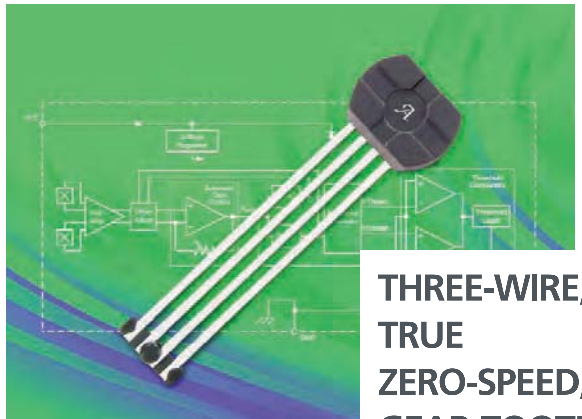
101LOK DATAMATE CONNECTOR SERIES CUTS ON ASSEMBLY TIME

Harwin has just launched 101Lok, a fast-mate version of its secure, 2mm pitch, J-Tek Datamate cable-to-cable, cable-to-board and board-to-board connector family. Historically, secure mating has been achieved with the Datamate J-Tek version using Jack screws. New 101Lok Datamate connectors require only a simple 'quarter turn', or 101 degrees, to ensure complete security of the retention device.

101Lok connectors use specially designed hardware, tensioned by a coil spring to reduce the time required to mate the connector halves. This is ideal for those users that are seeking a faster means of assembly, whilst ensuring complete security of the retention device. This novel locking feature is also ideally suited to Harwin's mixed technology Mix-Tek Datamate connectors and, also, the Trio-Tek range where high production volumes demand minimal assembly costs.

The spring tensioning also helps resist vibration in rugged environment applications such as aerospace. Comments, Product Manager, Paul Gillam: "These new 101Lok connectors are designed to be very simple to use and require no special tooling."

www.harwin.co.uk



THREE-WIRE, TRUE ZERO-SPEED, GEAR-TOOTH SENSOR IC

The new ATS667LSG from Allegro MicroSystems Europe is a 3-wire true-zero-speed gear-tooth sensor IC designed to provide a flexible high-accuracy solution for digital gear-tooth sensing in automotive transmission applications.

The ATS667LSG consists of a single overmoulded module containing a Hall-effect sensor IC and a magnet to provide an optimised magnetic configuration in a compact package that offers a high degree of design flexibility. The small package can be easily incorporated into different designs and used in conjunction with gears of various shapes and sizes.

The device incorporates a dual-element Hall IC that switches in response to differential magnetic signals created by a ferrous target. The IC contains a sophisticated compensating circuit designed to eliminate the detrimental effects of magnet and system offsets.

Features such as small-signal lockout, running-mode gain adjustment and automatic offset adjustment provide a high level of vibration and offset immunity. The device also contains Scan/IDDQ circuitry to enhance the testability and overall quality level of the sensor.

Digital processing of the analogue signal provides zero-speed performance that is independent of the air gap, as well as offering dynamic adaptation of device performance to the typical operating conditions found in automotive applications, in particular reduced sensitivity to vibration effects.

www.allegromicro.com

MICROTCA CONNECTORS FOR INDUSTRIAL APPLICATIONS

The Harting range of MicroTCA backplane connectors now incorporates a number of new features that make them suitable for use in industrial applications.

Originally developed for the telecommunications industry where their high transmission rates and compact dimensions offered significant benefits, MicroTCA systems have largely been limited to low shock and low vibration applications. However, the new features of the Harting devices allow them to be utilized in areas such as industrial control or transport where strong vibrations are encountered.

The Harting MicroTCA connectors meet all the requirements specified in the current version of the PICMG 'Rugged MicroTCA' subcommittee without contact interruptions. The key to the rugged performance of these connectors is a concept known as con:card+, which uses an innovative GuideSpring configuration to stabilise the connection against shock and vibration by offsetting any possible tolerance deviations and provide defined positioning.

As an alternative to the card edge and gold pads on the AdvancedMC card, Harting has also developed a plug connector with manufacturing tolerances much lower than those of the PCB card edge. With this approach, contact interruptions that are based on the tolerance problems of the card edge are prevented from the outset.

www.harting.com

KONTRON EVALUATION KIT FOR THE COMPACT COM EXPRESS CLASS

The Kontron microETXexpress evaluation kit offers developers a fast introduction into the compact class of COM Express. At the heart of Kontron's new Starterkit are the Kontron microETXexpress-SP or –DC Computer-on-Modules (95 x 95 mm) based on the Intel Atom series processors and the Kontron ETXexpress miniBaseboard. Starterkits are also available for evaluation with other microETXexpress modules.

The Kontron microETXexpress Starterkit is an all-round development platform for a wide range of embedded applications that require high-performance and processing density on a compact footprint with low-power consumption. It is ideal for evaluating applications that are to be operated on small mobile devices that are battery-powered or even solar-powered, and small embedded devices that have a compact format while offering a high level of features.

Developers working on applications in areas such as multimedia, test and measurement, medical, automation, energy, telecommunications or POS/POI can start developing on the target platform right away, due to the fact that the Kontron microETXexpress Starterkit comes with the complete embedded hardware including the cables, a very small power supply unit (called picoPSU), combined with a 12V desktop power supply and an active cooler.

At the core of the Kontron microETXexpress Starterkit is the Kontron ETXexpress miniBaseboard (170 x 155mm).

www.kontron.com

CONGATEC INTRODUCES NEW LOW-COST, LOW-POWER ETX/XTX MODULE

congatec AG announces the new conga-XA945 module as the latest addition to the company's successful ETX/XTX product family.

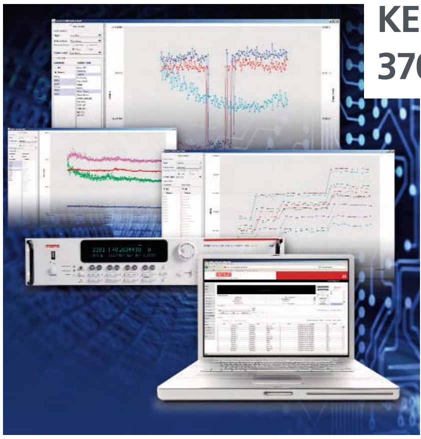
This extremely low-power and attractively priced module features 4 PCI Express links instead of an ISA bus. The module is equipped with the Intel Atom Processor N270 and a fully-featured Mobile Intel 945GME Express chipset including the Intel I/O Controller Hub 7-M.

This compact, 95 x 114mm XTX module is designed to deliver the best performance-per-watt ratio at the most attractive price level. The total thermal design power (TDP) of the processor/chipset combination is only 8W. As a result of enhanced power management functions, modern applications typically require considerably less than 5W. In conjunction with ACPI 3.0 battery management, such low power requirements enable designers to create mobile embedded applications with a full set of interfaces.

The conga-XA945 supports 4 PCI Express links, 6 USB 2.0 Ports, 2 Serial ATA interfaces, an IDE interface as well as Intel High Definition Audio. In addition, it comes with a 32-Bit PCI bus, 10/100 BaseT Ethernet, multi-master I²C bus, LPC bus and fan control. A DDR2 SODIMM socket enables flexible memory configuration up to a size of 2GB.

The conga-XA945 is powered by the 45nm Intel Atom processor N270 that is equipped with 512KB L2 cache.

www.congatec.com



KEITHLEY ADDS FREE GRAPHING TOOLKIT TO SERIES 3700 SYSTEM SWITCH/MULTIMETER FIRMWARE

Keithley Instruments announced the addition of a Web browser based, multi-channel graphing toolkit capability to its Series 3700 System Switch/Multimeter family. This new data visualization capability, which is included at no charge in the firmware for all new Series 3700 mainframes, offers users a quick and easy way to observe measurement data versus time, as channel measurements are made with the optional built-in digital multimeter, without the need for programming or any data file manipulation.

This "early look" capability makes it easy for users to gauge the progress of long-duration tests quickly and then to take quick corrective action if measurement results are not as anticipated. There's no need to write code in Keithley's TSP script language, LabVIEW or Visual Basic programming environments and then to extract data from an instrument's reading buffer into a third-party analysis package or a spreadsheet package such as Microsoft Excel to create graphs. Series 3700 mainframes support high speed, multi-channel measurements.

The addition of the graphing toolkit capability allows users to observe the data acquired either in numerical form or in graphical form on their choice of up to 40 channels simultaneously. The acquired data can be viewed in either real-time mode or in user-defined increments.

www.keithley.com

HERAEUS INFRA-RED EMITTERS WITH NEW QUARTZ REFLECTORS DELIVER HIGH POWER RAPIDLY

Infra-red emitters from Heraeus Noblelight fitted with a newly developed opaque quartz reflective coating provide high-energy, short-wave, infra-red radiation rapidly and responsively. With an operating temperature of around 2000°C, a power density of 300kW/m², stable and homogenous operation and no need for any cooling, emitters fitted with the new coating will find application throughout the industrial spectrum, from the manufacture of solar cells and special pipelines to coil coating and plastics welding.

The new quartz reflective (QRC) coating is extremely resistant to both heat and to the attack of acids, alkalis and other aggressive substances. Its special nano- and micro- structure provide the reflector with very high diffusion characteristics to ensure the stability of process parameters, such as temperature and coating homogeneity to optimise heating processes.

The reflectivity of QRC coatings is similar to that of highly polished aluminium reflectors. However, unlike aluminium reflectors which progressively lose reflectivity as aluminium oxide builds up on the surface, QRC glass suffers no oxide deposition and, hence, no progressive loss in reflectivity. In addition, the use of high purity quartz material minimises product contamination.

Conventional infra-red emitters are already used in the manufacture of solar cells, especially for under-vacuum processes.

www.heraeus.com

YOKOGAWA POWER METERS ARE CERTIFIED FOR TESTING STANDBY POWER TO IEC 62301 STANDARD

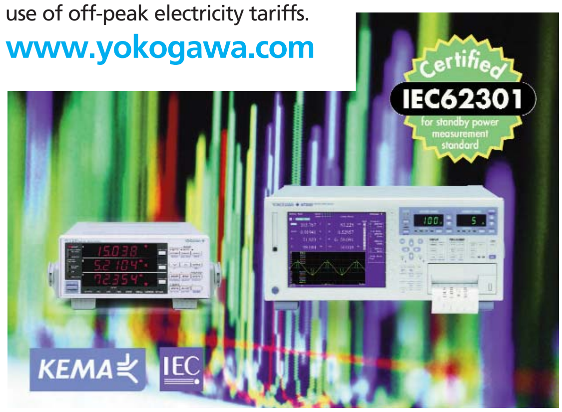
The Yokogawa WT3000-2A and WT210 digital power meters are now certified to carry out the standby power tests specified in the new IEC 62301 standard, which defines the standby mode as the lowest consumption of an appliance not performing its main function, when connected to the mains.

In tests carried out by Kema Quality, a global, independent accredited calibration laboratory and a leading authority in energy consulting, testing and certification, both instruments were shown to comply with all requirements for test equipment specified in the IEC 62301 standard.

IEC 62301 has been introduced in response to the growing awareness of limited energy resources and the resulting urgent need for power savings in household electrical appliances. This need is emphasised by the EU directive 2005/32/EC on standby power losses for both office and household electrical equipment, which comes into effect in all 27 EU member states in January 2010.

Standby power refers to the electrical power consumed by appliances or equipment when they are switched off or in a standby mode. Typical examples might be a DVD recorder set to record in timer mode or a dishwasher timed to make use of off-peak electricity tariffs.

www.yokogawa.com



TESTING TIMES FOR POWER CONSUMPTION

With a greater emphasis on energy conservations than at any time in our past, electrical equipment manufacturers not only have to monitor the power consumed by their products while in operation but also when in standby mode or even switched off.

This requirement for greater energy efficiency has not been driven by the manufacturing sector but by the wider 'Green Lobby', further legal requirements will follow and manufacturers that comply will have a marketing edge by producing 'Greener' products.

The EuP Directive 2005/32/EC covers the eco-design requirements of 'Energy-using Products' (EuP). Regulations controlling the design of electrical products will soon become EU law; manufacturers will then have a short period of time to redesign their products and meet mandatory standards.

Hioki's 'Power HiTESTER' 3332, 3333 & 3334 are ready to meet this monitoring requirement, measuring electrical power consumption under normal running conditions and in standby mode.

For further information contact:

GMC Instrumentation Ltd
Tel: 01543 469511
Web: www.gmciuk.com

PEI-GENESIS CONNECTOR PRODUCTION HITS A NEW MILESTONE

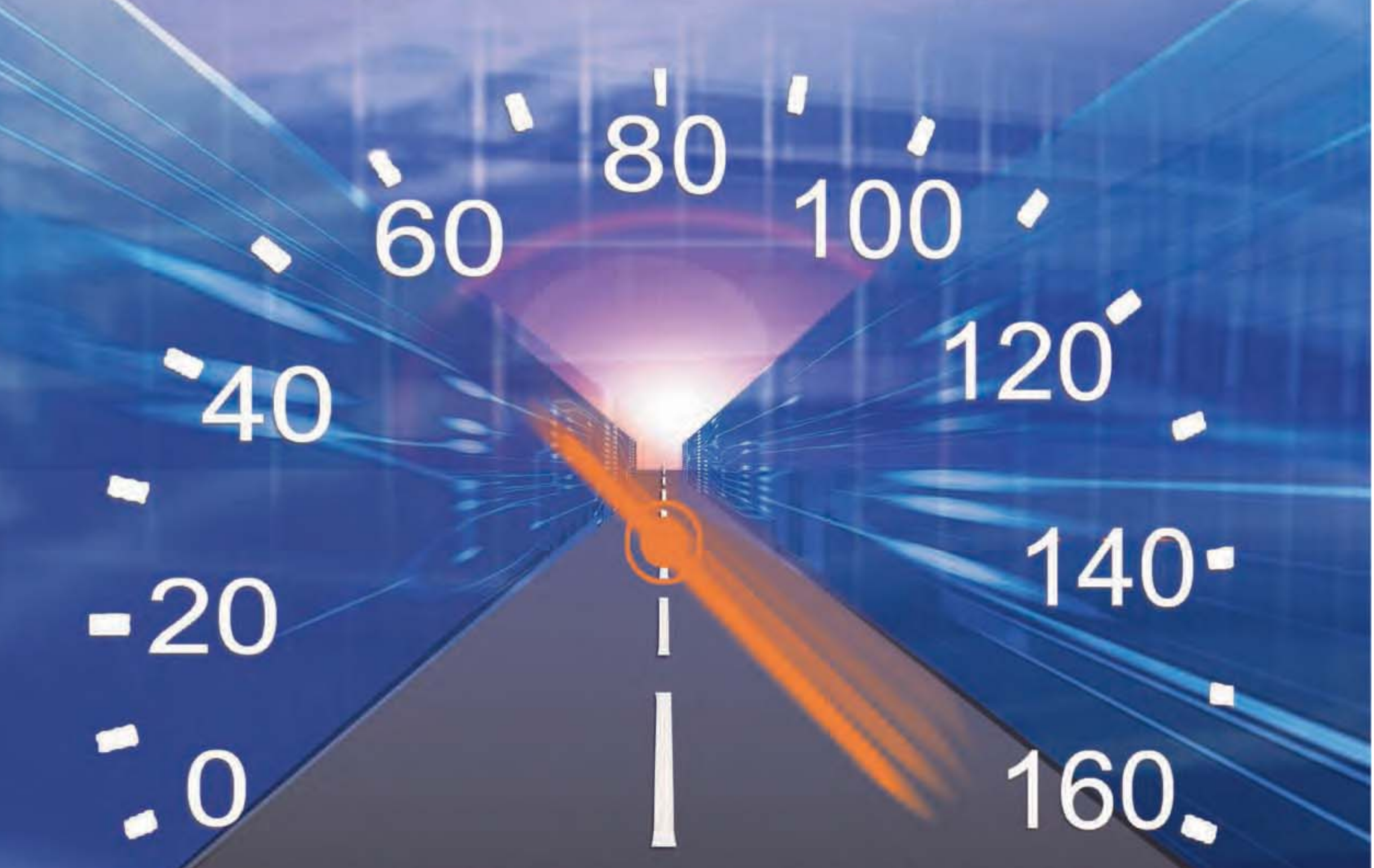
PEI-Genesis, the international franchised distributor specialising in the rapid assembly of multi-pin connectors, has reached a significant milestone in the company's history by achieving a worldwide annual output of over 8 million assembled connectors.

During the last 12 months the company assembled a total of 8,354,671 connectors from 226,068 works orders covering 52,792 different part numbers. Over 50% of the 8 million connectors were built for customer orders of five pieces or less and 65% were for customer orders of 10 pieces or less. All connectors were assembled and shipped in 48 hours.

"These figures underline the fact that our 48-hour connector assembly service is proving to be very attractive to a broad range of customers. Because we have no minimum order quantities, customers know that they can get the exact connector they need, in the shortest possible timescales – and without having to purchase unnecessary extra stock," said Doug Mercer, PEI-Genesis's European Marketing Manager.

"The total volume of connectors is all the more impressive when you realise that the vast majority of the 8 million are not say single-pole RF connectors but complex multi-pin circular connectors in a wide variety of configurations."

Primarily serving the industrial, railway, aerospace and defence sectors, PEI-Genesis works in close partnership with a number of leading connector manufacturers, including Amphenol, ITT Interconnect Solutions (Cannon and VEAM), Polamco, Cinch and Glenair.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