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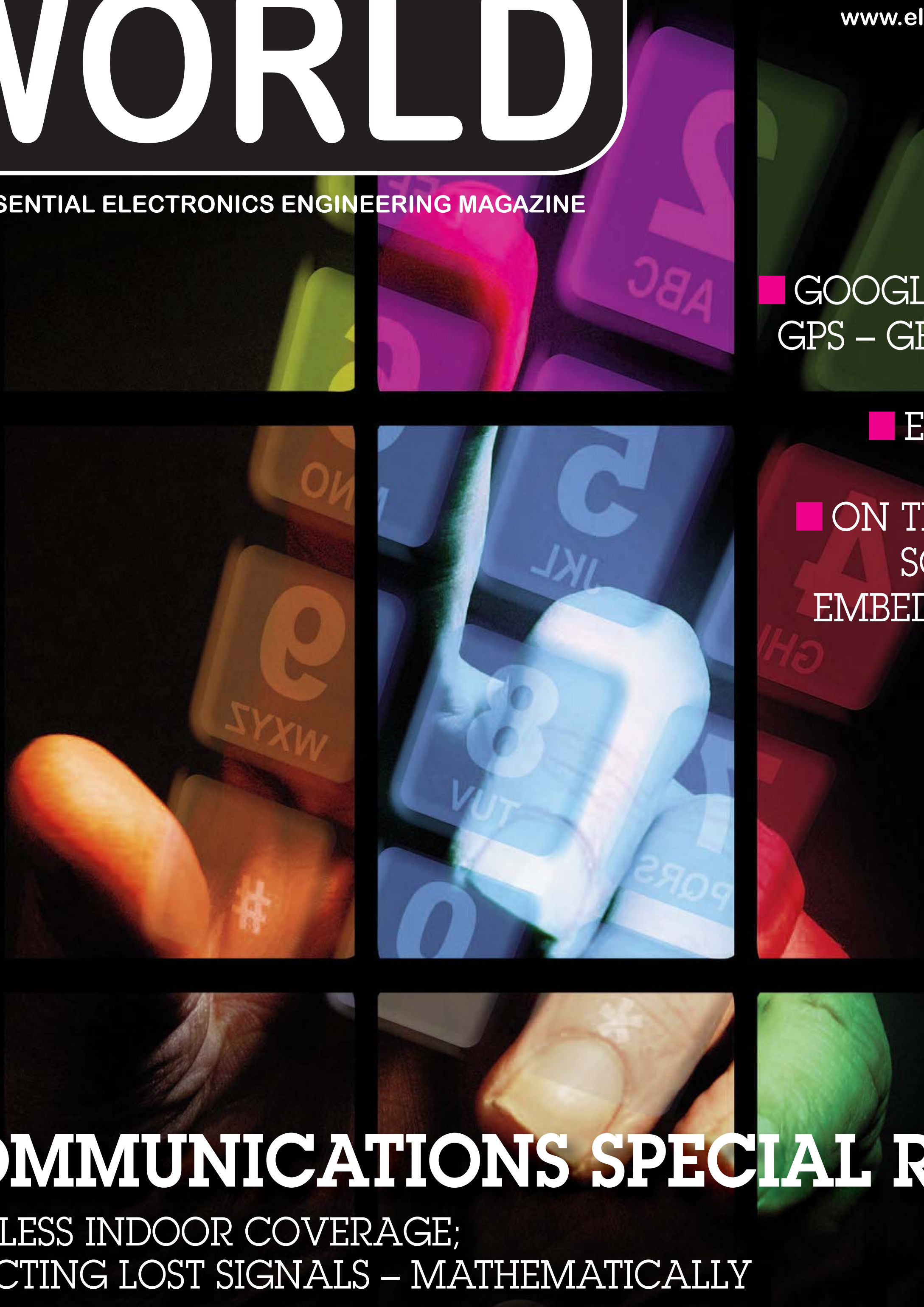
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE



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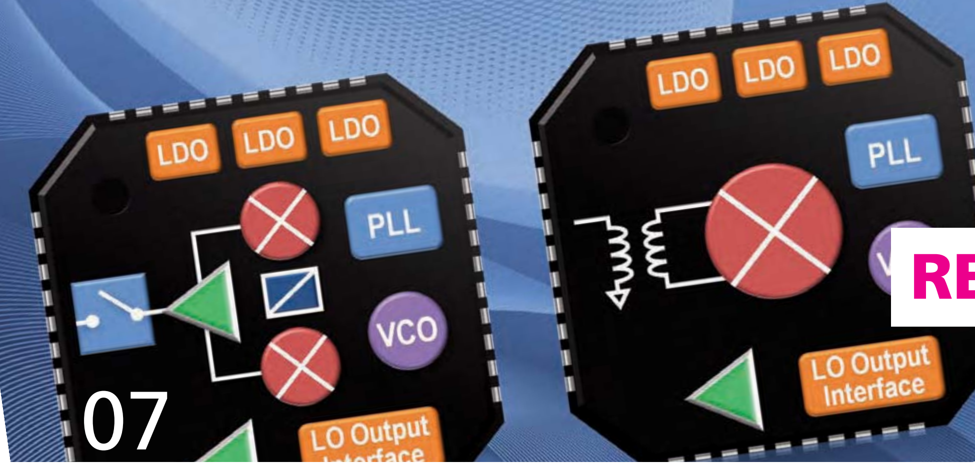
INSIGHT
THE TRANSFORMATION, OPPORTUNITIES AND CHALLENGES IN THE INDUSTRY TODAY

THE RF COLUMN
SHORT RANGE RADIO LINKS – THE REVIVAL

ALSO IN THIS ISSUE: LETTERS • PRODUCTS • DESIGN IDEAS



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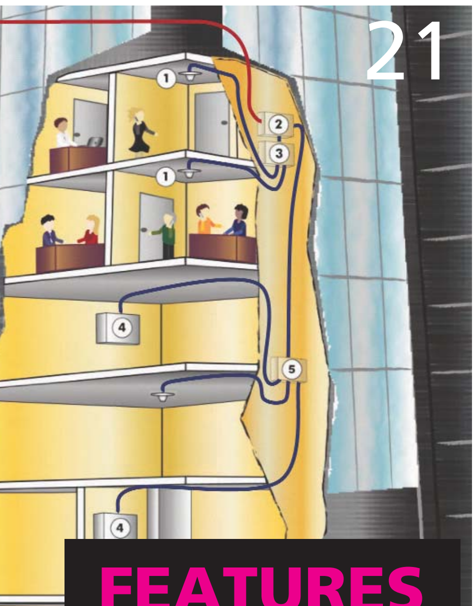

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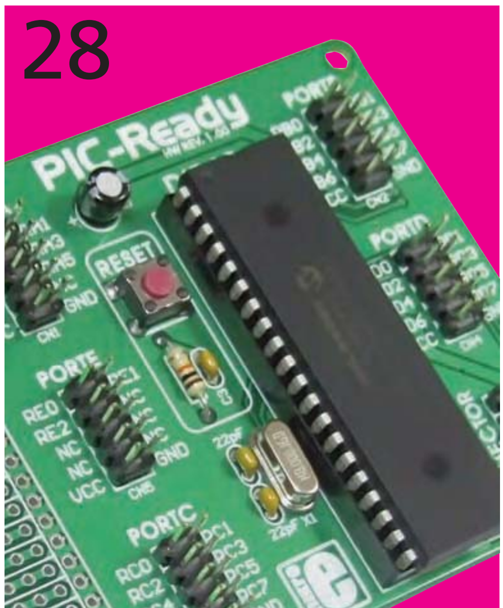

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FEATURES

REGULARS

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Kit Order Code: 3158KT - **£23.95**
Assembled Order Code: AS3158 - **£33.95**

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Engineering Must be a 'Two-Way Street'

A pioneering new qualification aimed at increasing the number of talented, ambitious young people looking to pursue a career in the electronics industry has been launched in classrooms across England.

The Diploma in Manufacturing and Product Design (MPD) is available to pupils and students aged 14 to 19. It has been developed to sit alongside traditional academic qualifications such as GCSEs and A-Levels. The qualification is being delivered by consortia of schools, colleges and employers, allowing students to divide their time between classroom, college and real work environments.

It is claimed that the new Diploma in MPD has been designed to equip young people with the skills and knowledge needed to pursue a career in industry, and will be taught from a curriculum designed by employers for employers. The content is intended to give young people a well-rounded set of skills applicable to manufacturing and, also, ensure they have a good mix of general employment skills prior to entering the workplace.

I don't see anything wrong with this kind of effort – on the contrary, it is good that such initiatives are beginning to surface. Manufacturers have always complained that young people are ill equipped to slot into a 'real life' work scenario straight after leaving school, colleges and universities. This initiative should certainly help.

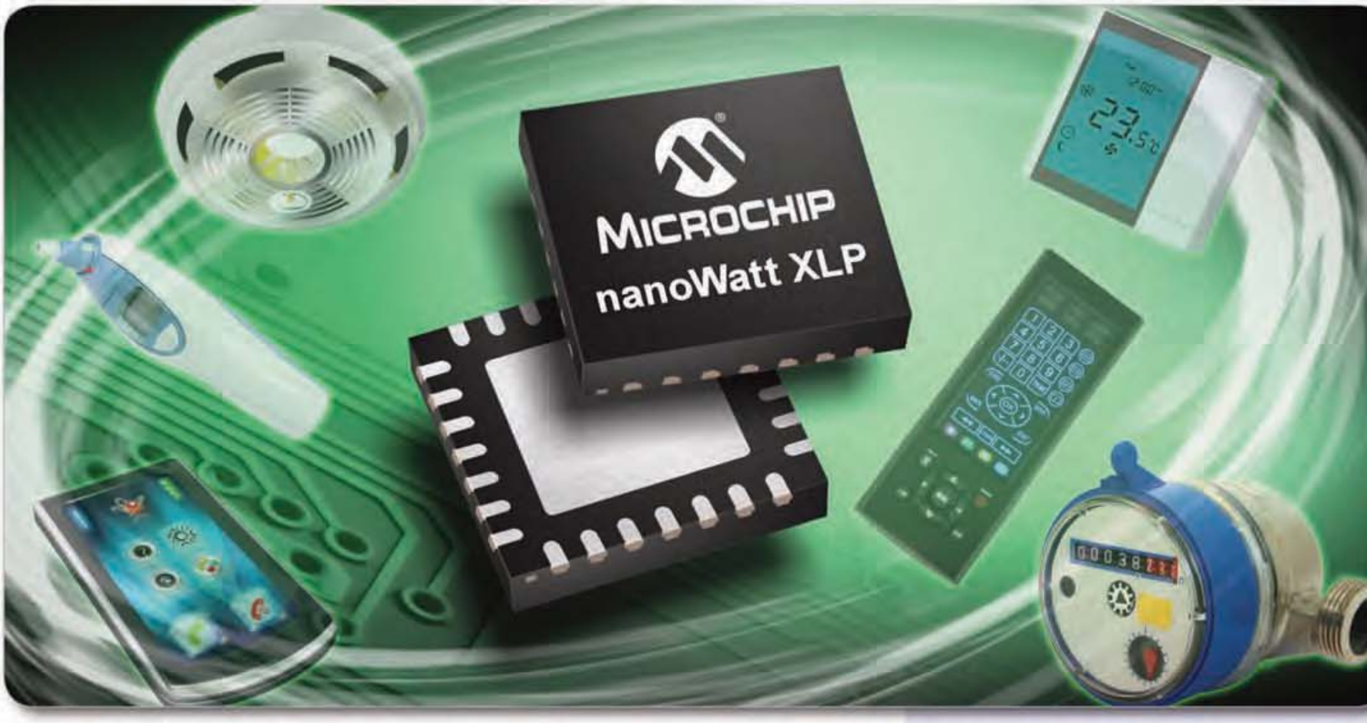
But, this only addresses one side of the problem. What happens to the other side, however, which relates to the lack of interest that currently exists among young people to enter any type of engineering education? Are colleges, employers and governments going to pool their efforts together to find ways of attracting pupils into engineering and, especially, electronics? Nowadays, other disciplines are proving a lot more attractive to pupils: any educational subject that will not pin them down studying/working for hours and a job that may give them maximum rewards seem to be of greater interest.

So, at a time when many technology luminaries are calling for graduates to turn their interest to engineering, we need a completely different approach that will pull them in this direction.

Any ideas?

Editor
Svetlana Josifovska

The World's Lowest Sleep Current MCUs: PIC® MCUs with nanoWatt XLP Technology



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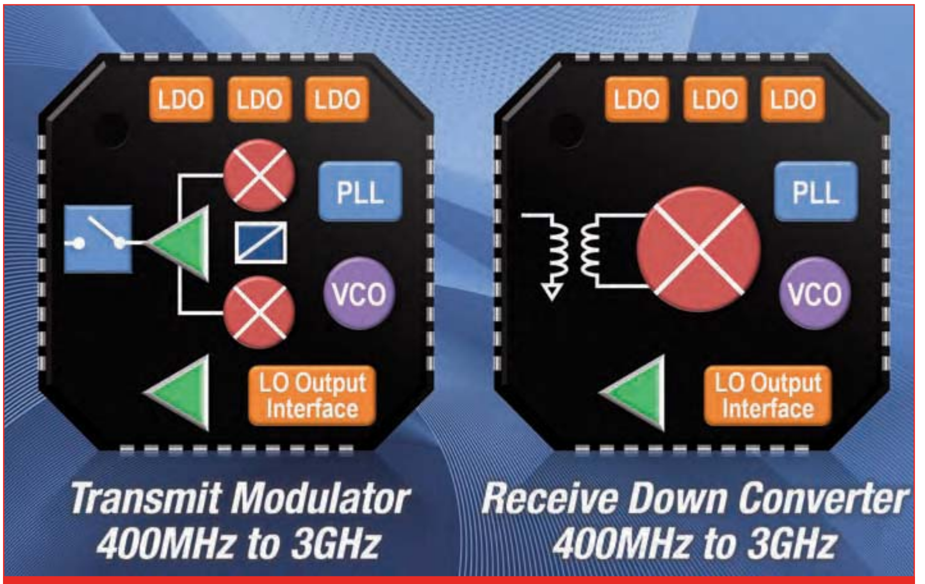
ADI introduces breakthrough RF circuits for 4G basestations

Semiconductor firm Analog Devices (ADI) last month introduced a series of highly integrated radio frequency integrated circuits (RFICs) designed for LTE (long term evolution) and 4th generation (4G) cellular basestations.

ADI's new ADRF660x series of mixers and ADRF670x series of modulators enable high-density radio cards by combining multiple discrete functional blocks into a single device, while meeting the demanding performance required by higher-capacity basestations. The firm claims that with such high level of integration, basestation manufacturers can save up to an "unprecedented" 60% in board space as well as reduce the bill of materials.

"Today's 3G and LTE basestations use many standard discrete RF components to optimize performance across both, the transmit and receive RF signal paths. ADI's new ADRF660x and ADRF670x products combine the radio frequency conversion functional blocks into one integrated circuit, without any sacrifice in performance," said Peter Real, vice president, Linear and RF products, Analog Devices. "These new devices are based on ADI's PLL/VCO synthesizer, mixer and modulator technologies, which offer the industry's leading phase noise performance, power consumption and linearity for smaller form-factor and higher density macro, micro and picocell basestations."



ADI's ADRF670x series of modulators

The four ADRF660x products integrate a high-linearity active RF mixer, RF input balun for single-ended 50Ω input and a PLL synthesizer with integrated VCO. The active mixer provides a voltage conversion gain of 6dB, alleviating the need for additional IF amplification over competing passive mixers. The differential IF output is capable of supporting IF frequencies up to 500MHz. The modulator input bandwidth of 500MHz is capable of supporting either a specified band or complex IF up-conversion transmit signal paths. In addition, the modulator output supports a linear high output power level for wideband multi-carrier LTE applications.

The ADRF660x series can be used for receiver path down-conversion and transmit path observation receiver applications.

RAMBUS AND KINGSTON CO-DEVELOP THREADED MODULE PROTOTYPE FOR MULTI-CORE COMPUTING

Memory architectures IP provider Rambus and Kingston Technology, an independent memory products developer, have announced a joint collaborative development of a threaded module prototype using DDR3 DRAM technology. Initial silicon results show an improvement in data throughput of up to 50%, while reducing power consumption by 20%, compared to conventional modules.

With a growing demand for throughput-intensive computing in notebooks, desktops and servers, the performance requirements on DRAM memory subsystems rises dramatically. As a result, multi-core computing requires more bandwidth and higher rates of random access from DRAM memory.

"As multi-core computing becomes pervasive, DRAM memory subsystems will be severely challenged to deliver the data throughput required," said Craig Hampel, Rambus Fellow. "Our innovative module threading technology employs parallelism to deliver the higher memory bandwidth needed for multi-core systems while reducing overall power consumption."

Threaded memory module technology is implemented utilizing industry-standard DDR3 devices and a conventional module infrastructure. It is capable of providing greater power efficiency for computing systems by partitioning modules into multiple independent channels that share a common command/address port.

Threaded modules can support 64-byte memory transfers at full bus utilization, resulting in efficiency gains of up to 50% when compared to current DDR3 memory modules. In addition, DRAMs in threaded modules are activated half as often as in conventional modules, resulting in a 20% reduction in overall module power.

BACK TO NORMAL ABNORMALITY?

Malcolm Penn is CEO and chairman of market analyst firm Future Horizons, based in the UK

IN JUST ONE quarter, the industry mood has shifted from a debate on the existence or not of the "green shoots of recovery" to a clear sign of relief that "the recession is now over", albeit tempered by a nagging uncertainty as to whether this really is the start of the chip market recovery or a blip on the statistical radar screen. The short answer is both; the industry is not yet completely out of the woods but the chip market can and will recover faster than the global economy.

After a 15.3% first quarter sales decline versus Q4-2008 (30% on an annualized basis), the second quarter grew a staggering 16.9% on Q1-2009. There have been only three previous instances in the history of the semiconductor industry when the second quarter – typically a single digit growth quarter – grew anywhere near this strongly. This dynamic alone was enough to change our 2009 forecast from minus 28% to minus 14%, still negative versus 2008, but nowhere near as bleak as the original outlook seemed.

With hindsight, it is now clear that the immediate effect of the Lehman Brothers bankruptcy was a massive overdose of FUD (Fear, Uncertainty & Doubt) and virtual industry paralysis. The markets did not disappear however, they merely slowed down and, eventually, the panic-induced paralysis gave way to catch up – in short the unknown unknowns yielded ground to the known unknowns, something the industry and business could understand and deal with.

Looking at the revised growth outlook scenarios for 2009, we believe that minus 14% is still the most likely outcome, the worst-case scenario being only minus 16%. The forecast is thus relatively insensitive to the actual Q3/Q4 numbers (within reason).

However, there are still several wild cards in play. Units are now much more aligned with real demand but average selling process (ASPs) are all still over the map, hardening in memories but weak in logic. So too is near-term fab capacity, with 'tight-geometry' 300mm capacity now getting tight, but 'loose-geometry' 200mm capacity still plentiful. This will send mixed signals on pricing over the second-half of the year, which in turn is likely to lull the industry into a false state of complacency.

The second quarter Cap Ex billings run rate is circa $800m per month, supporting a chip sales rate of $16bn per month; that is barely 5% of sales. So, either we have suddenly got 3x mega-efficient at building ICs (we have not!) or we are building ourselves a massive capacity problem down the road (we are!). In short, current Cap Ex spending more to do with line-balancing adjustments than new capacity build. Given the long lead times involved – it takes at least one year from investment decision to an incremental new IC sale – there is nothing now that can be done to alleviate a massive capacity shortage in 2010-11. The foundries will be the big beneficiaries here, the IDMs – the losers (Samsung and Intel excepted).

Fresh data points are now arriving each week indicating that the global electronics industry is rebounding from its 2008-09 financial meltdown. DRAM and PC sales are up with the impetus for renewed growth and recovery coming from Asia.

"IT IS NOW CLEAR THAT THE IMMEDIATE EFFECT OF THE LEHMAN BROTHERS BANKRUPTCY WAS A MASSIVE OVERDOSE OF FEAR, UNCERTAINTY AND DOUBT, AND VIRTUAL INDUSTRY PARALYSIS"

The IMF is currently forecasting a return to world GDP growth in 2010 at +2.5%, up from its +1.9% estimate made earlier this year, but the world could just as easily tip into a second global recession, triggered either by the current sharp rise in oil prices or downstream inflation caused by the current excess liquidity and the longer-term need to increase interest rates everywhere.

Interest rate rises will hit everyone very hard indeed, especially those firms and individuals over-extended in debt, currently saved only by interest rates at near zero levels. We are, thus, nowhere near out of a moribund economy; indeed, it is more likely to get worse before it gets better making a W-shaped economic recovery the most likely scenario, with the economic balance of power now clearly

2009 Forecast Scenarios

F'Cast	Profile A	Profile B	Profile C
Q1-09	44.219	44.219	44.219
Q2	51.707	51.707	51.707
Q3	57.912	56.878	55.844
Q4	59.650	58.585	56.961
2009	213.489	211.390	208.732

Quarterly (3:12) Growth

F'Cast	Profile A	Profile B	Profile C
Q1-09	-15.3%	-15.3%	-15.3%
Q2	16.9%	16.9%	16.9%
Q3	12.0%	10.0%	8.0%
Q4	3.0%	3.0%	2.0%
YoY%	-14.1%	-15.0%	-16.0%

Quarterly (12:12) Growth

F'Cast	Profile A	Profile B	Profile C
Q1-09	-30%	-30%	-30%
Q2	-20%	-20%	-20%
Q3	-16%	-17%	-19%
Q4	14%	12%	9%

2009 Total semiconductor growth rate scenarios
[Source: WSTS/Future Horizons]

shifted to Asia as the new engine of economic growth for the 21st century.

As for the chip market? It's back to normal abnormality. 2010-11 will see strong double digit growth with a sizeable Cap Ex catch-up spending splurge triggering a market slowdown in 2012 and a slow recovery thereafter. The chip cycles are dead … long live the cycles!

Malcolm Penn can be contacted at mail@futurehorizons.com. Future Horizon's website can be found at www.futurehorizons.com

FROM 1970 to 1985, the high-tech and electronics industry was manufacturer-driven and was characterized by vertically integrated companies delivering complete product lines themselves. This model evolved during the late '80s and '90s with the advent of industry standards and the expanding partnerships between the various players in the value chain. The level of partnerships and engagements further accelerated with the advent of today's Internet economies.

During the past 20 years, the industry underwent a transformation from completely vertically-integrated manufacturing to an increasing level of outsourcing to drive cost efficiencies and agility in the high-tech value chain. The power balance in certain businesses also shifted from manufacturers to retailers and now is shifting again to 'consumer communities' powered by the latest Web 2.0 capabilities.

Through our continuing engagement with customers and suppliers worldwide – as well as our own participation in the high-tech market – we at Microsoft have identified six major global trends in the high-tech and electronics industry:

Trend # 1: Power Shift to Consumers – Consumers are becoming more active participants in the high-tech value chain. Active consumer communities leveraging Web 2.0 capabilities have started influencing the success of various new products in the market. These consumers expect to contribute to product and technology innovation as more powerful processors, increasing bandwidth and the ubiquitous Internet are clearing the way for a new generation of technologies that support personal, social and business needs.

To successfully thrive in this new world, high-tech and electronics organizations need to take advantage of digital marketing and Web 2.0 capabilities to proactively engage and listen to the feedback from their consumer communities.

Trend # 2: Digital Convergence – This trend is evident everywhere around us. As the worlds of entertainment, computing and communications go digital, they can be combined to create exciting new products, services and business opportunities for the high-tech and electronics industry where information can be accessed any time, any place and on any device.

The focus on not just the product but on the overall customer experience the product delivers becomes key to future success. Combining products and services that manage the customer experience throughout the lifecycle of the product becomes critical. These new services also drive new and recurring higher-margin revenue opportunities.

Trend # 3: Emerging Economies – The high-tech and electronics industry are feeling the increasing influence of emerging economies and their consumers. As a result, "one size fits all" no longer works to meet unique local consumer needs and demands.

High-tech and electronics companies need global scale to compete, but must be able to execute locally. They must be agile to respond to the changing needs in widely differing markets worldwide. To succeed, they must achieve what we refer to as "profitable proximity" by developing capabilities to observe and serve the unique local needs.

Trend # 4: Sustainability – The rapid growth of global demand is fuelling rapidly rising costs in commodities and transportation across the world economy. It is also having an adverse impact on the environment and quality of life. High-tech and electronics manufacturers must develop and deliver sustainable products and services – now a necessity to compete and survive. The pressure is increasing from both consumers and governments to focus on "green" ecological initiatives. These efforts also present a unique opportunity for high-tech and electronics companies to innovate and bring a new generation of products and services to the market.

"THERE IS A GLOBAL SKILLS SHORTAGE IN THE HIGH-TECH AND ELECTRONICS INDUSTRY TODAY. THIS SHORTAGE IS ONLY GOING TO GET WORSE AS THE WORKFORCE AGES"

Trend # 5: Complex Regulations – Regulations span the gamut from environmental, healthcare and wellness to recycling and privacy

The high-tech and electronics industry have changed radically from the 1970s to the present day. **Sanjay Ravi**, Managing Director, Worldwide High Tech and Electronics Industry at Microsoft, discusses the transformation, opportunities and challenges participants must address to successfully compete and win in the future

THE HIGH-TECH AND ELECTRONICS COMPANY OF THE FUTURE, TODAY

standards including RoHS/WEEE, REACH and Sarbanes-Oxley. The need for transparency is a "license to do business". Manufacturers will increasingly need to rely on flexible frameworks to address multiple regulations and avoid high costs of one-off compliance solutions.

Trend # 6: Changing Demographics – There is a global skills shortage in the high-tech and electronics industry today. This shortage is only going to get worse as the workforce ages. As a result, companies must attract the new Gen-X/Millennial Generation. The fact that this new workforce is also going to be global drives the need for better knowledge management capabilities across the world. Solutions that are familiar and easy-to-use are needed to help the next generation of workers to ramp up at a very fast pace.

To address these trends, high-tech and electronics organizations will increasingly have to work in a high performance business network of partners, customers and consumers, and focus on the following five key business imperatives: grow customer relationships across the customer and consumer network, accelerate innovation, develop dynamic and resilient supply networks, improve operations and drive corporate performance and compliance.

High-tech and electronics manufacturers must grow customer relationships across the customer and consumer network by building customer loyalty and penetrating new global markets. To succeed, they must observe and serve customers globally to drive growth with "profitable proximity".

Business imperatives include the need to create new bundled product and services offerings to manage the overall customer experience, increase sales win rates, increase customer retention, manage marketing costs and reduce service costs. To address these imperatives will require new capabilities to improve campaign execution with digital marketing, and manage customer relationships with better sales and service effectiveness solutions.

Pressed by global competition, high-tech and electronics manufacturers must accelerate innovation across global innovation networks – the conversion of knowledge and ideas into new or improved products, processes and services – to gain a competitive advantage. This innovation no longer happens just within the four walls of an enterprise. To bring new innovative products to market faster, high-tech and electronics companies need to work across an innovation network of business partners, design houses, original design manufacturers, customers and consumers.

To compete on a global scale and execute locally, high-tech and electronics organizations must develop dynamic and resilient supply networks of increasing scope and complexity, including multiple outsourced design and manufacturing partners, and other associated product and content providers. More dynamic and resilient supply chain networks are needed to address the demand and supply uncertainties in today's markets that arise from, on the one hand, changing consumer preferences coupled with increasing product variety and, on the other, strong competitive forces and the potential for external disruptions.

High-tech and electronics manufacturers also must improve operations by flexibly managing manufacturing operations to bring new products to market faster, while reducing costs. By using collaboration, integration and analytics capabilities, they can improve internal operations, as well as identify and quickly and flexibly respond to the key performance indicators and real-time signals from customers and global suppliers.

Finally, to thrive in an increasingly complex global environment, high-tech and electronics manufacturers must improve their organizations by driving corporate performance and compliance across their business network and provide business insights to all employees, leading to better, faster and more relevant decisions. Their focus must be on enhancing collaboration and transparency, and improving corporate performance management across all the key business processes – adding value to every decision. ■

Short Range Radio Links: THE REVIVAL

IN THE LOW POWER wireless industry, there is a technically driven polarization between the long range, low data-rate designs (complex, high specification, narrow-band radio modems) and the short range, high data-rate solutions (Zigbee, Bluetooth and other proprietary UHF wide band radios).

Both these 'camps' are inherently limited by various regulations, which put limits on transmit power and usable frequency bands.

This time, however, I want to examine what happens to the design criteria of a simple ISM band wireless link if a *short range* link is implemented using a very *low* data rate.

Typical uses for short-range radio data links include simple remote control functions, monitoring devices and data download systems. Actual data throughput is typically low (periodic bursts of less than a hundred bytes), but power consumption, physical size and price are often critical.

Such systems are usually implemented using single-chip radio solutions, with data rates of 10-50kbit/s (or more), to keep the duty cycle, and hence effective average current drain, low. Transmitter designs will use the maximum legal power, which is 10mW at 433MHz in Europe, to offer maximum range with the relatively low receiver sensitivity possible with the simple wide band architecture (around -95dBm to -105dBm).

But what happens to the system design if we radically reduce the data rate?

With falling data speeds, receiver sensitivities can be improved, as the effective signal bandwidth is smaller. For the noise levels associated with simple FSK demodulators and low current radio front-ends, a receiver sensitivity of -117dBm for < 1% data errors can be easily achieved with a 1kbit/s biphase coded data burst (a 30mS duration burst containing a preamble/sync/framing sequence and 3 bytes of payload data).

This improvement in link margin (of 20dB or more, compared with high speed units) could be used to increase the range of the link, but for the class of simple, short-range radios under consideration here, the range is (unusually) not the overriding factor.

So we can take the opportunity to reduce the transmitter output power in proportion. A reduction from +10dBm to -20dBm (ten microwatts) has considerable advantages.

The transmitter can be radically simplified. A single transistor VCXO/multiplier design can be easily realized at 433MHz. A bench prototype produces -20dBm, while drawing only 2mA from the 1.8V power supply.

Material costs are low. A discrete design with less than 20 parts is easily produced, with a potential large volume price under three Euros.

The transmitter is small. A 14mm x 14mm module is easily implemented, or the layout 'tile' can be used as part of a larger circuit board.

A usable the range is retained. Calculated range in sub-urban conditions (see Note 1) is 80 meters, while open field line-of sight will be considerable more.

When a practical 'walk around' test was conducted, a prototype of this 10 microwatt link was found to give solid coverage throughout a three-bedroom, brick-built terraced house. Good link performance was retained within 40m of the building, in open ground (see Note 2).

"WHILE THIS APPROACH IS NOT NECESSARILY THE ANSWER TO ALL QUESTIONS, IT DOES ILLUSTRATE HOW A DIFFERENT APPROACH TO AN EXISTING PROBLEM CAN STILL BE FRUITFUL"

Reducing transmitted power to -40dBm would theoretically reduce the range to around 12m. In practice, complete coverage of the building was retained.

In addition to transmitter power consumption and hardware savings, the -20dBm transmit power figure has another significance: it corresponds to the maximum permitted power allowed on 433MHz under the US Part 15 regulations. It will be feasible to obtain FCC approval for such a unit, which should

NOTE 1: REFERRING TO THE EGLI IRREGULAR TERRAIN PATH LOSS MODEL, EXPRESSED IN DB TERMS:

Path gain (dB) = 32.4 - 40 x log(d) - 20 x log(f) + 20 x log (Hr x Ht) + Gt + Gr

F = frequency in MHz
d = distance in meters
Gt, Gr = transmit and receive antenna gain (dBi)
Ht, Hr = height above ground of transmit and receive aerials

Taking the example low data rate radio link: -20dBm tx power
-117dBm rx sensitivity

= link margin of -97dB

Assuming unity gain aerials at 1m elevation, and using the Egli model above:

d = 83m theoretical range

NOTE 2: PRACTICAL RANGE TRIAL. EQUIPMENT USED

Receiver:	Radiometrix WRX2-433-12, on NBEK evaluation unit Operating mode A (CTR44 burst decode, unlatched) 0dBi gain 1/4 wave whip aerial.
Transmitter:	IFR 2023A signal source, modulated by a second NBEK unit Operating mode C (CTR44 mode, periodic transmission) 0dBi gain 1/4 wave whip aerial.
Location:	RG21 4DQ. Urban/residential environment

offer considerable savings in complexity and price over existing US market 915MHz products.

While this approach is not necessarily the answer to all questions (the data burst is still quite long, requiring more receiver on-time, and the overall data throughput is low), it does illustrate how a different approach to an existing problem can still be fruitful and how apparently obsolescent methods (crystal multiplier transmitters, discrete RF circuit designs) are occasionally worth reviving.

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd ***www.radiometrix.com***

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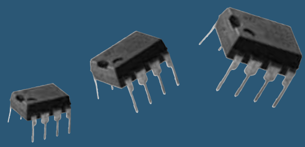


SCHEDULERS IN EMBEDDED SYSTEMS

Vicky Larmour from Cambridge Consultants, explains why solid understanding of the features of the scheduler will help develop robust code

SCHEDULER SERVICES may seem to be of little interest to application programmers; as long as your code runs, why would you need to think about it? In fact, what goes on 'under the hood' is actually of vital importance to the way application programs are written and run; nowhere is this more relevant than in a constrained embedded system.

Note that in various different operating systems, the terms 'task', 'thread' and 'process' may be used to mean specific different things. In this article, which is intended to be generic, I use the term 'task' throughout.

Event Loop

The very simplest form of scheduler involves an event loop that runs continuously, processing external events as they arrive. If further events arrive while one is being processed, they must wait until the processing of the first one is complete; they will then be processed strictly in order of arrival.

This type of scheduler is simple to implement and may be appropriate in a very lightweight operating system, but provides no real-time support and no concurrency.

When developing applications on this type of scheduler you don't have to worry about protecting shared data (no risk of race conditions), but you do need to make sure your event handlers do not hog the processor for too long. If performing a long, slow operation you may need to defer part of the process through the scheduler by manually sending a new event to trigger the next part of the processing (giving other queued events a chance to be handled first).

Round Robin Scheduler

The next level up from this in complexity is known as a Round Robin scheduler. The scheduler maintains a fixed array of tasks; each task element in the array is a structure that contains pointers to the task-specific data, context etc. The scheduler simply chooses the next task in the list and runs it until it completes or blocks, then moves on to the next task in the list. The scheduler relies on each task to yield regularly, referred to as 'co-operative multi-tasking'.

More Complex Schedulers

The basic Round Robin concept can be extended in a wide variety of ways, giving different advantages and depending on the requirements of the application:

- Dynamic creation and destruction of tasks:

If an application needs to dynamically create tasks, the scheduler may keep the tasks in a linked list rather than a fixed array. This involves marginally more overhead in the scheduler, but a much more flexible application development platform.

- Pre-emptive multi-tasking:

The scheduler may time-slice, allowing each task to run only for a fixed length of time, or it may interrupt a lower priority process to allow a higher priority one to run. This means that all accesses to shared data must be appropriately protected.

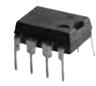
- Task prioritisation:

The scheduler may store a priority level for each task. This allows slow, low-priority activities to take place without blocking user input or other external events, but can cause priority inversion (see below).

- Real time support:

Deadline schedulers provide a way for tasks to indicate a real-time deadline by which execution must be complete. The scheduler then uses a combination of task priority and the deadline information to select which task to schedule next.

These possibilities can be combined as necessary, up to a fully-featured, pre-emptive, real-time operating system with dynamic creation and destruction of variable priority tasks (which would be



overkill for many embedded systems, but may be necessary for some applications).

Issues to Consider

Assigning task priority is not a simple matter of: "this task is clearly important, this one less so"; in a poorly designed scheduler, this can result in priority inversion, where a higher priority task is blocked by a lower priority task and, hence, effectively assumes the lower priority. To resolve this, tasks can temporarily inherit the maximum priority of any higher priority tasks they are blocking.

Consider which actions should take place in interrupt service routines (ISRs) and which in the task context. Switching context entails an overhead (as the stack frame is stored and the new stack frame loaded); a system with a scheduler that invokes frequent context switches will incur a corresponding performance hit.

An application function is 'threadsafe' (runs in a multi-tasking environment) if accesses to global resources are protected. A function is 're-entrant' if multiple instances of the function may be executed concurrently, either by multiple tasks or by recursive calls within a single task. A re-entrant function must not make use of static non-constant data, only data provided by the caller. It must not rely on locks to singleton resources, such as disks or call other non-re-entrant functions.

Whatever the features of the scheduler you are working on, a solid understanding of those features and their implications will provide a sound basis for developing robust code.

Cambridge Consultants is a technology and innovation company, renowned for its ability to solve technical problems and provide creative, practical solutions to business issues.

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WHEN IS 10GBPS NOT 10GBPS?

By Dan Joe Barry, VP of Marketing at Napatech

"WHAT YOU SEE is what you get!" A phrase immortalized by the comedian Flip Wilson and adopted by computer engineers in the famous WYSIWIG abbreviation. Indeed, in engineering we tend to place a great deal of pride in living by this statement; delivering on our promises and not succumbing to the charismatic influences of the irrationally exuberant marketing department.

And yet, there is one fact that has gone quietly unnoticed and tacitly accepted by engineers, almost to the point of being accepted as a natural law. What I am referring to is the uncomfortable truth that 10Gbps ports do not always provide 10Gbps throughput; especially when those ports are based on standard Network Interface Cards (NICs).

"So what?" you may ask. There are plenty of examples where we don't always receive what we expect. Take Internet access rates that are highly contended, for example. This is the case, but it is so by design and policy. This situation can be reversed by policy. The throughput limitations on 10Gbps ports, however, are inherent to the technology being used and cannot be changed without changing the underlying technology.

The Limitations of Standard NICs

There are ways of resolving the throughput issue, but first let's take a look at how big this issue really is. To illustrate this problem in more detail, the graphs in **Figure 1** show typical performance for commercially available standard 10Gbps NICs with respect to throughput and server CPU load (i.e. how much work does the CPU need to do in just handling the traffic being received).

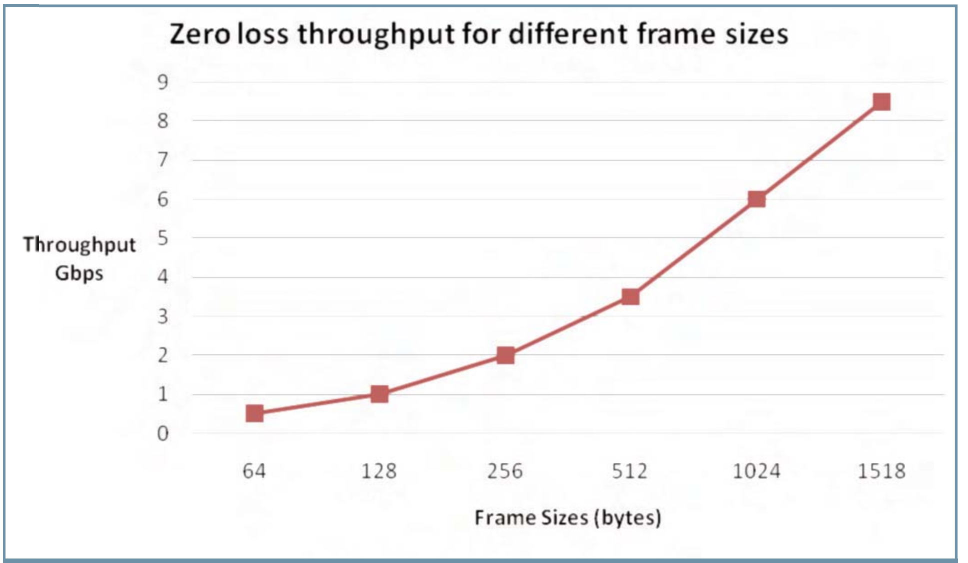


Figure 1a: *Real throughput on a 10Gbps port for standard NICs [Source: CESNET performance tests]*

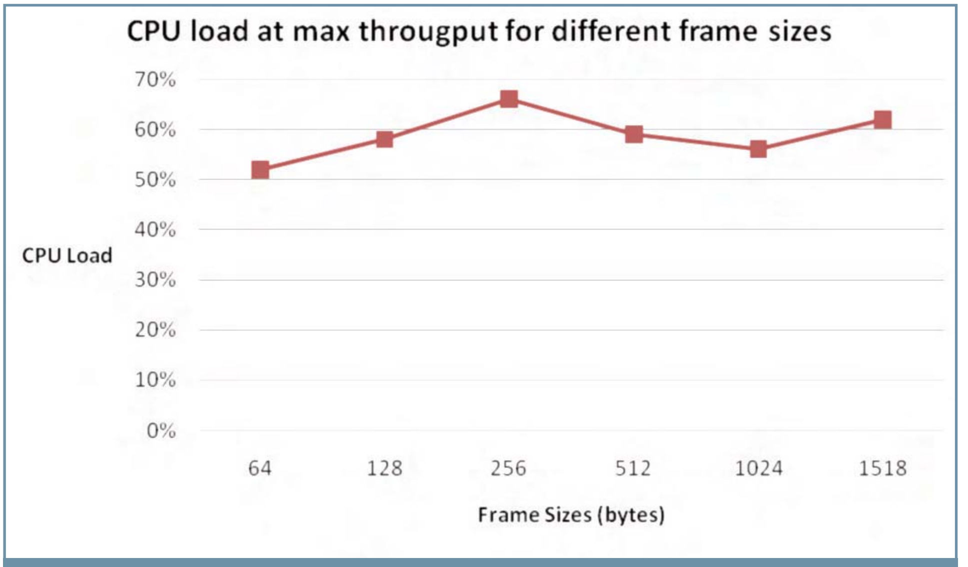


Figure 1b: *CPU load handling 10Gbps data traffic on 10Gbps port [Source: CESNET performance tests]*

The graph shown in Figure 1a is referring to the effective throughput that can be achieved without losing packets at the port. **Table 1** shows the theoretical limit for the throughput one should expect on a 10Gbps port.

As can be seen in Figure 1a, for large Ethernet frame sizes, throughput is close to the theoretical limit. However, as frame sizes decrease, the effective throughput drops off dramatically to less than 1Gbps at small frame sizes.

Typical frame sizes for Internet communication lie in the range from 128 to 1024 bytes, with 300 bytes an often referenced frame size for tests. In this range, it can be seen that throughput is at best 6Gbps and can be as low as 1Gbps.

	Maximum load at zero loss for different frame sizes (in bytes)						
	Measured	64	128	256	512	1024	1518
10G Ethernet (theoretical max throughput)	Gbps	7.3	8.4	9.1	9.6	9.8	9.8

Table 1: *Theoretical maximum throughput for a 10Gbps Ethernet port*

The graphs in Figure 1 are based on 10Gbps port throughput, but the issue is the same for 1Gbps ports. What distinguishes these two cases is the additional load that is placed on the CPU for handling of data traffic. For 1Gbps ports, the CPU load is high, but acceptable, whereas for 10Gbps ports, as Figure 1b shows, almost 2/3 of the CPU resources are used just in handling Ethernet frames. This is not acceptable for many of the compute and data-intensive network applications that are now becoming common in the network.

The explanation for this considerable workload is that standard NICs are designed to interrupt the CPU each time a frame is received and needs to be handled. The CPU must decide what to do with the frame, to re-order and de-duplicate frames received, to discard frames that are invalid etc. This, obviously, is a distraction for CPUs, which should be busy running the network application in question.

The Year of 10Gbps

2009 is expected to be the year that 10Gbps hits prime-time. According to a report by Dell Oro group in March of 2009, 10Gbps is one of the few areas showing growth in the networking segment. Infonetics reported in February that the worldwide revenue for 10Gbps Ethernet switches doubled in 2008 compared to 2007. This is driven by economies of scale now contributing to attractive prices per port, which are making it more economical for enterprises to migrate from 1Gbps to 10Gbps.

One can expect this growth trend and demand for 10Gbps connectivity to continue. With trends such as cloud computing and virtualization, one can expect 10Gbps links to be utilized to their maximum capacity as multiple virtual servers are accessed on a single physical server through a limited number of 10Gbps ports.

Full Line-Rate Network Appliances

For network appliances that monitor, analyze and secure 10Gbps networks, full line-rate 10Gbps throughput and efficient use of CPU resources now become critical requirements.

Network appliances are now more important than ever, as there is increased focus on network security as well as optimizing use of network resources, both from the network providers' and network users' perspective. Throwing bandwidth at the problem is no longer the solution of choice.

The key criterion is that network appliances must be capable of receiving, analyzing and in some cases transmitting data at full 10Gbps line-rate without losing packets, no matter the size of the packets in question.

Network appliance vendors have struggled to achieve maximum throughput performance, as can be evidenced by examining the data sheets of various 10Gbps network appliances currently available. Indeed many have yielded to the issue and tacitly accepted that 5Gbps is what one can expect to transmit through a 10Gbps port without losing packets. Proprietary hardware designs can improve performance, but even here full throughput can be elusive.

Accelerating Throughput

The ideal solution is one based on standard off-the-shelf server platforms, which are relatively inexpensive and flexible and now have the multi-core CPU computational horsepower for even the most demanding tasks.

What is required is an intelligent, real-time network adapter that can be used in standard servers that addresses the issues of throughput and data traffic handling, such that performance can be maximized while CPU load is minimized.

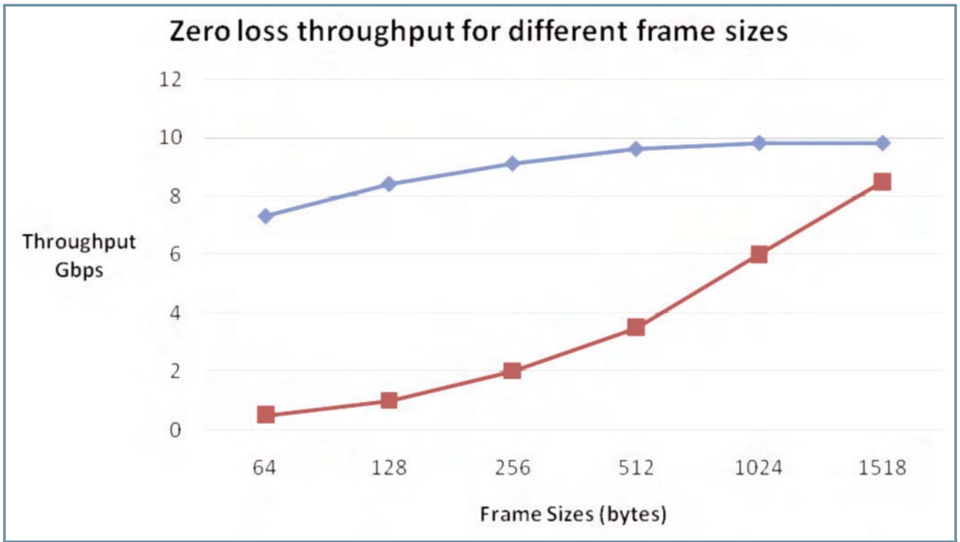


Figure 2a: *Napatech NT20E throughput performance*

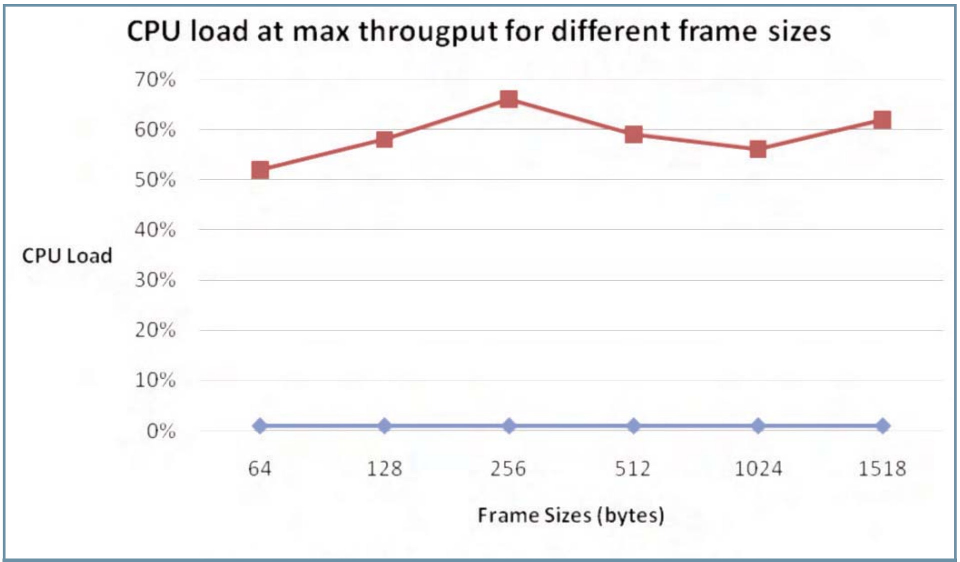


Figure 2b: *Napatech NT20E CPU load performance*

The key ingredients are:

- Handle as much of the data traffic on the adapter as possible;
- Ensure that the packet payloads are delivered to the network appliance applications as quickly and effectively as possible;
- Provide mechanisms to ensure that only the right traffic is presented to the right applications;
- Efficiently distribute the traffic processing load on multiple CPU cores.

By meeting these requirements, it is possible to maximize throughput up to theoretical limits, while at the same time minimizing the load on the server CPU.

As an example, the Napatech NT20E Capture adapter provides the following throughput and CPU load performance (see **Figures 2a** and **2b**):

As can be seen, the throughput can be maximized to theoretical limits while CPU load can be reduced to less than 1%. Intelligent real-time network adapters can bridge the performance gap making standard off-the-shelf servers a viable and powerful platform for network appliances.

From Standard Server to Universal Appliance

What does this mean? Solving the issue of throughput and CPU load is not merely a case of improving performance. It is much more than that. Standard, off-the-shelf servers can be used as platforms for extremely high-performance network appliances, where a standard server is esentially turned into a universal appliance whose application is limited only by the software used.

"FOR NETWORK APPLIANCES THAT MONITOR, ANALYZE AND SECURE 10GBPS NETWORKS, FULL LINE-RATE 10GBPS THROUGHPUT AND EFFICIENT USE OF CPU RESOURCES NOW BECOME CRITICAL REQUIREMENTS"

It is good that it is no longer necessary to build proprietary hardware to ensure optimal performance, instead the focus can be singularly applied to improving the software application. The software can also be ported from one generation of standard server to the next as processing power and other features improve. The application can also be tailored to run on different sizes of standard servers for low-end and high-end customers.

The bottom line is that intelligent real-time network adapters in standard servers can provide a cost-effective and flexible universal appliance for high performance network applications.

Finally, when it comes to 10Gbps throughput, we can all return to the values that we as engineers strive to uphold, namely "What you see is what you get". ■

Have your say – write to or email the Editor at the address on page 3, or at Svetlana.josifovska@stjohnpatrick.com

Growing Demand for In-Building WIRELESS COVERAGE and Capacity

Andrea Casini, Vice President of Europe, Middle East and North Africa Sales and Marketing at Andrew, explains how today's wireless consumers demand a seamless service indoors as well as out

IT IS NOW a universally established fact that approximately three quarters of mobile calls originate or terminate inside building premises – a huge change from ten years ago. In fact, fixed line telephony services are on the decline as an increasing number of consumers and business users are choosing mobile phones as their primary form of communication, even when in close vicinity to a fixed line phone. Not only do mobile phones allow a greater deal of flexibility, but with new technologies and high-functionality handsets becoming more accessible, users are increasingly turning to their mobile devices as a tool for storing and accessing information far beyond the traditional use of voice, including the use of mobile e-mail and Internet browsing, which is becoming increasingly popular.

Mobile operators have been quick to recognise the advantages to be had from offering a wider range of services and are planning network deployment in accordance with the increased use of mobile phones indoors. And with European markets flattening out as far as new network rollouts are concerned, mobile operators are also seeking new ways to boost revenues. Many of these operators are looking towards deployment of in-building and special coverage projects as a means to boost their ARPU (average revenue per user). The recent enthusiasm for in-building solutions is driven by network optimisation activities undertaken by operators trying to address interference, capacity and dead coverage spots, not only within buildings themselves but also in surrounding urban areas, especially in areas where there is a high penetration of business users. Andrew's involvement in the deployment of in-building systems at Canary Wharf in London is a prime example of this.

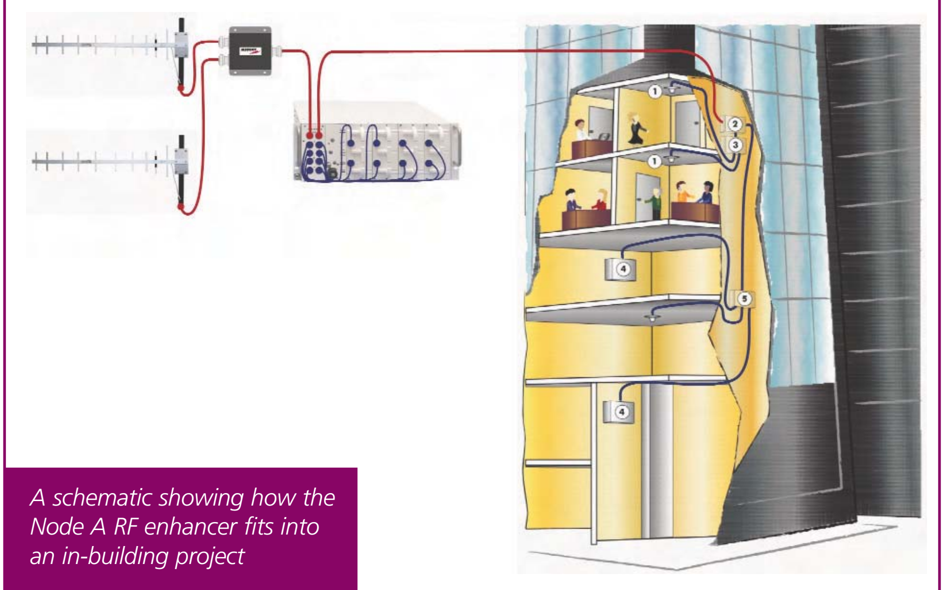
Andrew's Node A product, an RF enhancer used in in-building projects

Meeting Ever-Changing Needs

As the landscape becomes more competitive, mobile operators must get serious about addressing the changing needs of an increasingly mobile society. As wireless technologies evolve, consumers and business users alike are demanding more network coverage and less "down time", where access to a wireless signal is limited or unavailable.

Improvement in high-speed data performance is also becoming an increasingly important factor, with the massive uptake of 3G data services having made a significant contribution to the amount of traffic over wireless networks both in and out of doors. With more and more websites now optimised for the mobile platform, the uptake of mobile data has surged in recent months, with over one quarter of UK users, for example, now using mobile devices to access the Internet.

Enterprises, in particular, are already looking to provide wireless coverage in office buildings as growing numbers of staff demand wireless coverage wherever they happen to be within the business site, and owners of public buildings are now also beginning to realise the benefits of indoor wireless coverage, with airports, shopping malls and stadiums increasingly keen to provide their users with access to a wireless network. Businesses demand instant access to a range of communication methods including e-mail, instant messaging, and voice and video calling. It is no longer acceptable for operators to offer an unreliable service, especially as the market becomes more crowded. In dense urban areas the competition for wireless coverage is amplified significantly, which is why operators need to consider deployment of advanced in-building solutions.



A schematic showing how the Node A RF enhancer fits into an in-building project

In-Building Solutions

So, what are these in-building solutions, which are the most popular with operators, and which are the most effective at providing indoor wireless coverage? Femtocells and picocells are one option. ABI Research predicts the rapid rise of femtocells and picocells as an integrated part of the initial rollouts of Long Term Evolution (LTE) networks. Higher frequencies, which will be used by LTE, penetrate structures less effectively than low frequencies and, so, femtocells and picocells offer an attractive way to compensate for lower indoor signal strength. Although a number of telecom equipment manufacturers are actively supporting the rise of femtocells, the market is limited by the fact that this technology is primarily designed for use only in residential or small business environments.

But whilst many operators are already trialling femtocell technology, others are hesitant due to potential network management difficulties. According to Informa, femtocells will not necessarily make any CapEx or OpEx savings for the operators. If femtocells are sold to customers in sporadic fashion via traditional mobile operators' channels, then this may induce a huge scattering of femtocell deployment over large areas. Femtocells, however, need to be deployed in clusters to ensure they can effectively substitute the capacity of macrocell networks, otherwise they can become a burden to operators. The deployment of femtocells has yet to take off in a big way.

Another option are Distributed Antenna Systems (DAS), which work by taking a donor feed from the macro cell, or from a repeater, and then distributing that over fibre through the building. These systems typically consist of components such as coaxial and radiating cables, power splitters, directional couplers and indoor antennas. A dedicated radio base-station connected to a DAS ensures both dedicated coverage and capacity, confines the signals, prevents signal spillage and interference and, thus, enhances the quality for both speech and data services. In addition to enabling new traffic in previous non-covered areas, the solution also off-loads the macro network in overlapping coverage areas.

Other advantages are that a DAS can serve either one or multiple operators, as well as either one or multiple bands (e.g. GSM 900, GSM 1800 and WCDMA).

It is active DAS in particular that is currently driving the market, according to another report by ABI Research. ABI research states that the provision of coverage in the largest buildings will drive active DAS systems growth at a compound annual growth rate (CAGR) of 28% through to 2013. According to ABI, active DAS systems deliver the greatest cost benefit in very large buildings. Below 500,000 square feet, passive systems such as repeaters and passive DAS systems start to become more cost-effective. But with data services becoming a greater portion of wireless services ARPU, capacity becomes an equally relevant design factor.

Shaping the Future of In-Door Coverage

Capacity is playing an increased role in the design of in-building wireless systems. As buildings get smaller, and with the presence of older passive systems, solutions will use a toolkit of options including repeaters, femtocells, picocells and passive and active DAS systems.

In order to capture revenue share from the enterprise market it is more effective for mobile operators to fund the instalment of DAS and repeater systems in corporate environments. Businesses that rent office space increasingly expect seamless wireless coverage, and although operators may be willing to subsidise the infrastructure costs in order to win large corporate accounts, it is not feasible to expect that any one structure should be limited to one operator. In public buildings, it is even more important to allow access to a multi-operator environment in order to provide sufficient wireless coverage for all users. For this reason, femtocells alone are unlikely ever to be a serious option for large businesses.

The future of in-building is that European building regulations will specify a pre-installed wireless infrastructure model which will be subject to approval by operators, and the implementation of this will inevitably depend on who is financing what. It is still to be confirmed whether the building owner or the operators will ultimately take responsibility for financing the bulk of the wireless infrastructure deployment; what we do know, however, is that the operators are keen to remain in control. One solution would be that the operators share costs; this is already happening at the macro level and is likely to filter down.

Complex buildings such as large office blocks, airports, shopping malls and stadia require dedicated coverage and capacity, not only to satisfy high consumer demand but for reasons of security. The subscriber profile will dictate adequate traffic resources, most normally with micro and pico base-stations complemented by passive and/or active DAS. At times and in certain areas, particularly in suburban areas, backhaul could be a limiting factor.

Another aspect that should be taken into account is that typical network planning is bi-dimensional, hence normally missing out the third dimension of vertical buildings. This factor often skews the visibility of potential high-traffic (and revenue) pockets that are simply neglected or overlooked. As a consequence, networks may face huge traffic crowding and blocking, with lost calls and poor accessibility. A correct assessment of those potential risks is a key factor to accelerate positive customer experience and revenue growth in today's competitive ecosystem.

Seamless Wireless Coverage

Andrew provides appropriate tools to accurately measure network quality and lost traffic. Its wireless coverage solutions are adopted in a number of dense urban areas, such as Canary Wharf and in Glasgow's West End, and in stadia such as those used for the World Cup in Germany and The O2 in London. Solutions are deployed in order to overcome the limiting factors of wireless propagation in confined environments. This could be as simple as typical coverage extension or can extend to optimising the distribution of network capacity by providing an additional street-level wireless layer (usually composed of low-power, low-impact antennas invisibly installed on light poles) that offloads urban traffic from the macro network in areas of high density of subscribers.

These solutions become extremely attractive from both an economical and a technical point of view because of their intrinsic ability to provide a shared infrastructure that can be efficiently used by multiple wireless operators and services. While the cost-sharing factor is obvious, it is also worth noting that the technical advantages of a shared solution with reliably consistent radio performance contribute to reduce interferences and maximise capacity and efficiency, particularly so in WCDMA technology. A robust operations and maintenance system allows independent access to status information by each participant to the system, including third parties in charge of the system itself.

With the Olympics arriving in London in 2012, the question of in-building within stadiums is one that is particularly hot on everyone's lips. Organisers of large events now demand seamless wireless coverage, and with technology having developed to deal with much higher capacity than a few years ago, wireless vendors now need to optimise their services to provide a multi-operator, peak capacity service, with minimal visual impact and at a competitive price, in order to stay ahead of the game. ■

Vladimir Rentyuk, Development Engineer at Modul-98 Ltd in Ukraine, considers the mathematical model of a linear interpolator and its practical applications

The Simple INTERPOLATION System

QUITE OFTEN engineers have a problem of recovering an initial signal, for example, from remote sensors or signals of multichannel communication systems. As a rule, this problem is usually solved either by using an optimum detecting filter or by the most widespread method – using the staircase approximation.

The first method gives good results, as it suppresses the signals of intermodulation frequencies very well; in other words, the sampling frequency and its harmonic components. But this method offers poor signal-to-noise ratio, as the value of a useful signal is equivalent to a quotient of the width of a sampling pulse to a sampling period. High-order Butterworth filters are generally used in this solution. However, the use of such filters is limited, for example in the case when the filter's cutoff frequency needs to be changed. Take notice that these filters require highly precise parts and high-precision adjustments. They are also expensive.

The second method uses well-known interpolation systems based on Sample-and-Hold Devices (SHD). These devices approximate the primary signal with the staircase approximation function. Although the resulting signal-to-noise ratio is not too bad, as the pulse width is equal to the sampling period, it is not a method suitable for many applications. This is due to having to use an additional filter (a second-order or a third-order) to reduce the sampling signal, or for having to use higher sampling frequencies; all this complicates the device's use.

Simplifying Matters

Many troubles could be avoided if a piecewise (linear) approximation could be used instead of the staircase approximation. The classical solution of such interpolator generally represents two in-series filters with a step approximation, clearly with the corresponding control circuit. A possible block diagram of this system is represented in **Figure 1**. In this device we have a sum of two linear-interpolating functions U1(t) and U2(t). The function U2(t) can be shifted (delayed) by a time period equal to the multiplexing time (or the sampling time Tsamp) of the system.

The block diagram can be simplified into the system shown in **Figure 2**.

There are two functions: U1(t) and U2(t). One function, U2(t), is shifted (delayed) by a time equal to the sampling time Tsamp. Let's analyze the system's operation. Let's suppose that an input signal U(t) is a certain constant voltage U, which will not change during a time of at least two periods of the sampling time. The value U will be entered by a control pulse into SHD1, which then forms the first input of the Summing Inverting Integrator. An output voltage Uout(t) of the Summing Inverting Integrator will be:

$Uout(t) = -1/\tau 1\int Udt = -(1/\tau 1)*U*t$ where $\tau 1$ is a constant of integration of the first input (1) of the Summing Inverting Integrator.

A constant of integration is the integration itself, and is characteristic of an integrator. If we use a basic RC integrator, its constant of integration is $\tau 1 = CR$ and $Uout(t) = 1/\tau 1\int U(t)dt$.

If $\tau 1 = T$, where T = Tsamp, then Uout(t) = (–U). At the end of cycle T = Tsamp volume Uout(t) = Uout(T) will be entered by a control pulse into SHD2, which will then follow into the second input of the Summing Inverting Integrator. An output voltage Uout(t) of the Summing Inverting Integrator will be:

$Uout(t) = -U - 1/\tau 1\int Udt - 1/\tau 2\int(-U)dt$ where $\tau 2$ is the constant of integration of the second input (2) of the Summing Inverting Integrator.

If $\tau 1 = \tau 2 = T$, where T = Tsamp, then Uout(t) = (–U). This is the equilibrium condition of this system, because, in this case, we will have a constant output signal as long as the input signal does not

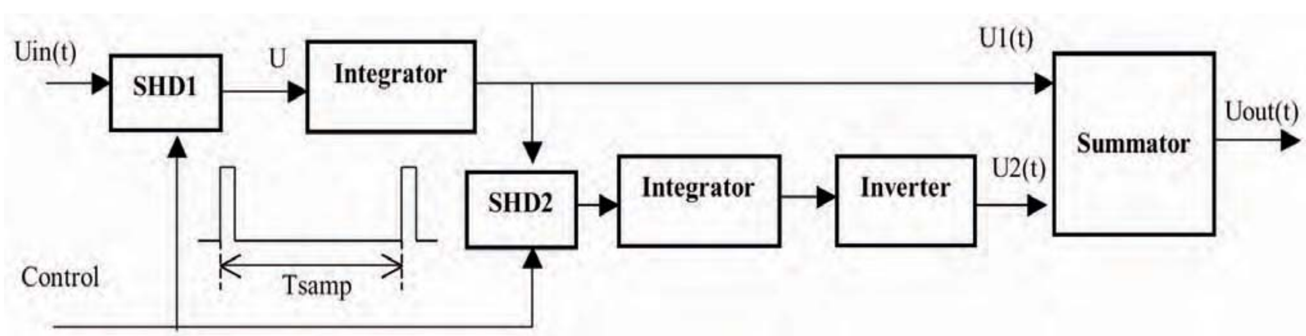


***Figure 1:** Block diagram of the piecewise-linear approximation circuit*

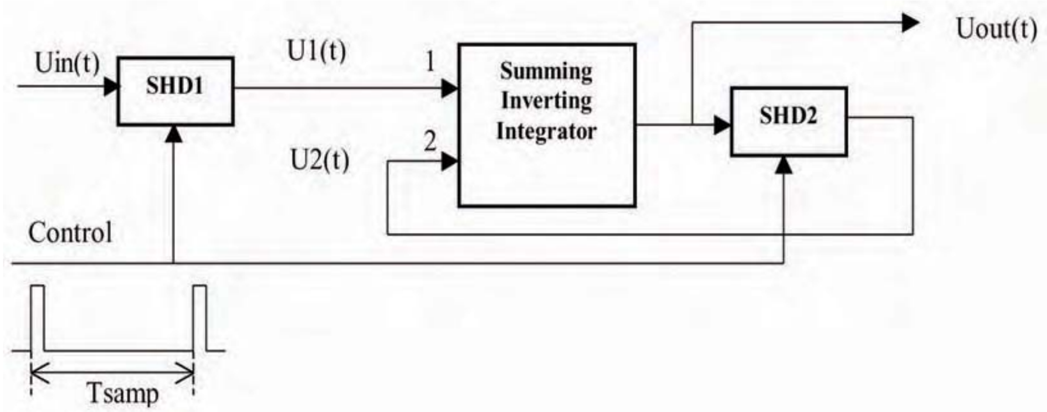


Figure 2: *Block diagram of the simple piecewise-linear approximation circuit*

change, meaning:
$Uout(t) = -U + 1/\tau 1\int Udt - 1/\tau 2\int Udt = -U + U - U = -U$

If we assume that the input signal Uin(t) has had an increase ΔU, then: $Uout(t) = -U - 1/\tau 1\int(U+\Delta U)dt - 1/\tau 2\int(-U)dt$
as such: $Uout(t)= -U - (t/\tau 1)\Delta U$

Thus for a time period of T = Tsamp we have $Uout(t) = -(U + \Delta U)$. In other words, the output signal is increased by ΔU during Tsamp. This increase will be approximated by a function type $A(t)\sim(t/\tau)$ in the interval of Tsamp, thus we have a 'Linear-Interpolation' system. One such simple, applicable, system is shown in **Figure 3**.

An Applicable System

The Sample-and-Hold Devices were replaced by analogue switches (S1, S2) with capacitors (C1, C3). S1, S2 are usual analogue CMOS switches (for example ½ of 74HC4066). DA is a general operational amplifier (OP) with low input current (for example ½ LM358). The R4, C4 combination is an elementary low-pass filter (optional).

The capacitor C1 will be discharged through the resistor R1 after sampling the input signal. The value of the input signal of the Summing Inverting Integrator will then be equal to:
$U(t)=U*e^{-(t/\tau 1)}$ where $\tau 1$ is a discharge time constant $\tau 1$ = C1R1 (C1 are discharging through R1).
NOTE: A discharge time constant of an RC circuit shows the velocity of discharging of the capacitor through the resistor.

This signal will be integrated, thus the output signal of the Summing Inverting Integrator will then be equal to:
$Uout(t)= -(1/\tau)\int(Ue^{-(t/\tau 1)})dt= -(\tau 1/\tau)Ue^{-(t/\tau 1)}$

Let's say that R1 = R2 and C1 = C3, then a constant of integration (τ) of the Summing Inverting Integrator will be τ = C2R1 = C2R2. After a period of T = Tsamp, $Uout(t) = -U(\tau 1/\tau)(1-e^{-(Tsamp/\tau 1)})$, thus $\tau = \tau 1(1-e^{-(Tsamp/\tau 1)})$ then $Uout(t) = (-U)$, which makes it the equilibrium condition of this system.

Let's accept this condition. The next control pulse will restore the value of the signal of the capacitor C1 up to the value U, and it will charge the capacitor C3 up to the value (-U). Both of these values will be integrated, but the output level will not be changed. At this point I'd like to confirm that the discharge time constants of these capacitors are equal, and the absolute values of the signals are also equal, but with opposite polarity.
$Uout(t) = -U - (1/\tau)\int Ue^{-(t/\tau 1)}dt - (1/\tau)\int(-U)e^{-(t/\tau 1)}dt) = -U.$
If the input signal Uin(t) has an increase ΔU, then:
$Uout(t)= -U - 1/\tau\int((U + \Delta U)e^{-(t/\tau 1)}\,dt - 1/\tau\int(-U)e^{-(t/\tau 1)})dt= -(U + \Delta U)(\tau 1/\tau)(1-e^{-(t/\tau 1)})$.

During period Tsamp, the level of this output signal will be changed to: $Uout(t) = -(U + \Delta U)(\tau 1/\tau)(1-e^{-(Tsamp/\tau 1)})$ or $Uout(t) = -(U + \Delta U)$, if the equilibrium condition of this system is used.

This increase will be an approximated by the function type $A(t)\sim(\tau 1/\tau)(1-e^{-(t/\tau 1)})$ of the interval of Tsamp. It is a piece-exponential approximation function, because we have an exponential factor there. Hence, it is not a linear-interpolation system, in the strictest sense. Let's use our equilibrium condition for this function:
$A(t)\sim(\tau 1/\tau)(1-e^{-(t/\tau 1)})= \tau 1(1-e^{-(t/\tau 1)})/\tau 1(1-e^{-(Tsamp/\tau 1)})= (1-e^{-(t/\tau 1)})/(1-e^{-(Tsamp/\tau 1)})$
After differentiation we have the following:
$A(t)\sim(t/T)\,(e^{-(t/\tau 1)})/(e^{-(Tsamp/\tau 1)})$

It can be seen that $(e^{-(t/\tau 1)})/(e^{-(Tsamp/\tau 1)})$ is going to 1, if $\tau 1$ is going to ∞ (infinity). Thus if $\tau 1 \gg$ Tsamp, the approximation function during Tsamp will be $A(t)\sim t/T$ or $A(t)\sim t/\tau$ (remember the equilibrium condition), just as in the case of the idealized linear-interpolating system, which was considered above. See the time graphs (**Figure 4**).
NOTE: The output signal of this Linear-Interpolation System is inverted.

Use of the Idea

This technical idea can be used in systems with time division of channels, as the low-pass filter, etc. The transfer function of such filter is equal to:
$A\,(jF)=(\sin^2\pi F\,Tsamp/(\pi F\,Tsamp)^2) * e^{-j2\pi F Tsamp}$ where F is frequency of the useful low frequency input signal. This would be a function of the type sinx/x for a step interpolator.

The exponential member gives a phase response. It shows that the filter creates a delay equal to Tsamp (for a step interpolator it is Tsamp/2). So this device can be used as lattice cell adjustable (by change Tsamp) delay circuits of an analogue signal. However, you'll need to consider the influence of an additional low-pass filter, if it is used.

It is important that the output resistance of a source of the signal and an on-resistance (R_{ON}) of the switches are suitable for charging the capacitors C1, C3. They should be charged up to the value of the input signal during sampling time.

The values of the resistors R1, R2 should be much higher than the on-resistance of the switches. A constant of integration (τ) of the Summing Inverting Integrator can be calculated by the formula of the equilibrium condition. In this case, the transfer function of such a system will be a combination of two functions: $A (jF) = (\sin^2 pF\ Tsamp/(pF\ Tsamp)^2) * e^{-j2pFtsamp}$ and a transfer function of some low-pass filter with a cutoff frequency according to chosen constant of integration (τ) of the Summing Inverting Integrator. The transfer function of this "additional" low-pass filter should be one, if the constant of integration (τ) of the Summing Inverting Integrator is closely matched to the result of the 'equilibrium condition' formula.

A cutoff frequency of this system can be changed by choosing carefully the constant of integration of the Summing Inverting Integrator; it depends on the interrogation time (Tsamp). The cutoff frequency will be increased if the constant of integration of the Summing Inverting Integrator is decreased, and vice versa.

A cutoff frequency of this system and its proper operation are dependant on the sampling time cycle (Tsamp). Hence, conditions of the Kotelnikov-Shannon theorem (*Nyquist-Shannon sampling theorem or the theorem about the sampling rate*) should be taken into account, when converting from analogue signal to digital (or otherwise sampling a signal at discrete intervals), the sampling frequency must be *greater than twice* the highest frequency of the input signal, in order to be able to reconstruct the original perfectly from the sampled version. A proper layout and a simple low-pass filter (a first- or sometimes second-order), connected to the output of this system will be suitable, too.

Notice that this Linear-Interpolation System does not have any ripples in its bandwidth. We can see a burst of impulse fronts only in the case when the constant of integration (τ) is less than its acceptable minimum value.

This device does not require precision parts or high-accuracy adjustment; it is not expensive either. Equally, the general requirements of using a real operational amplifier should be taken into account. ■

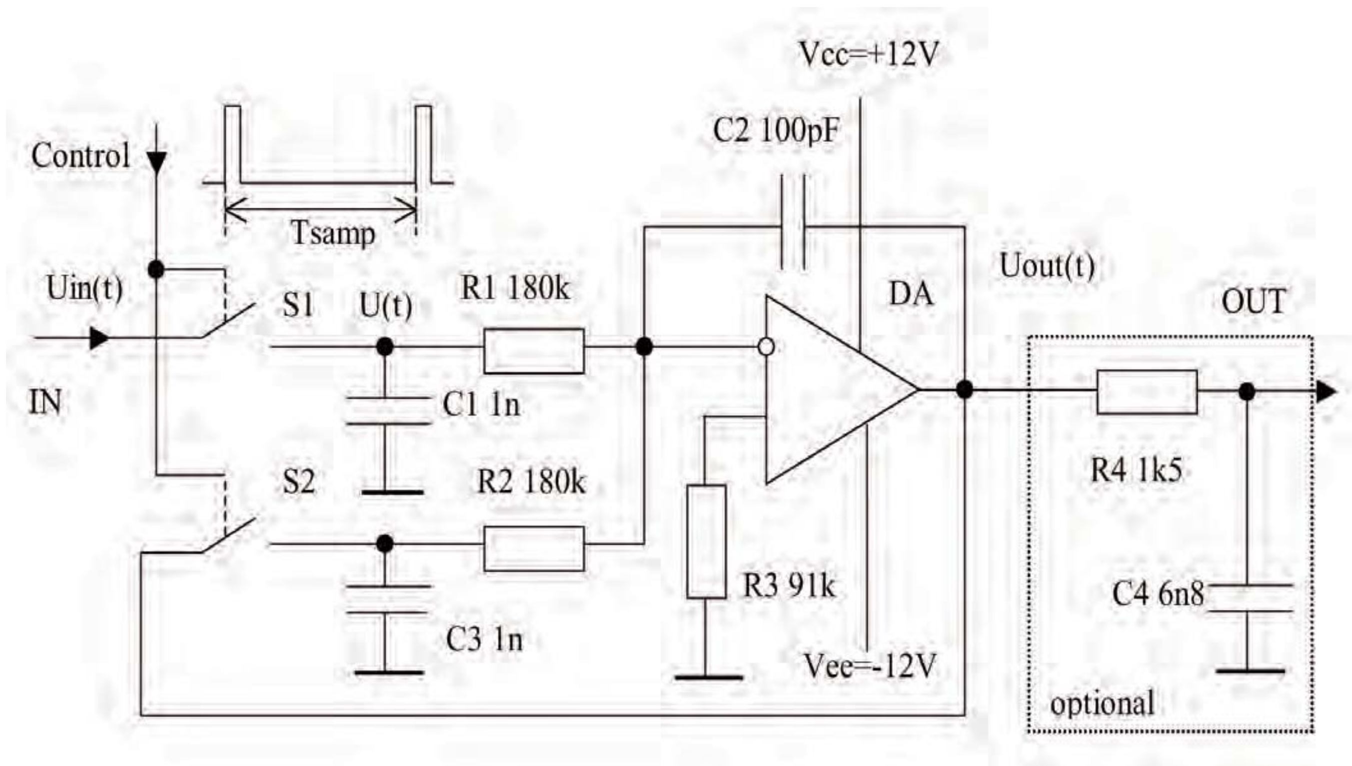
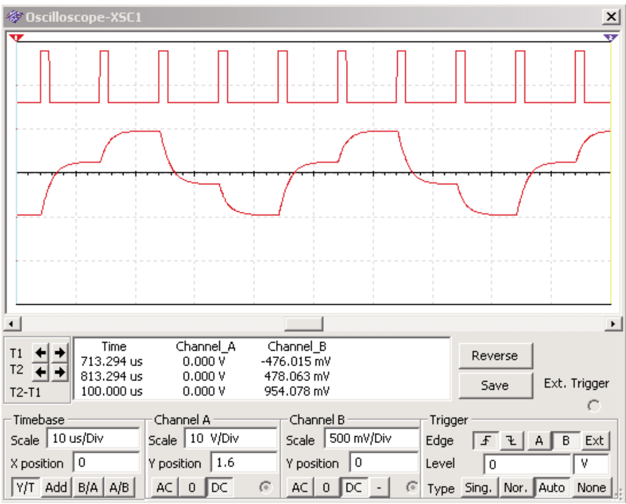
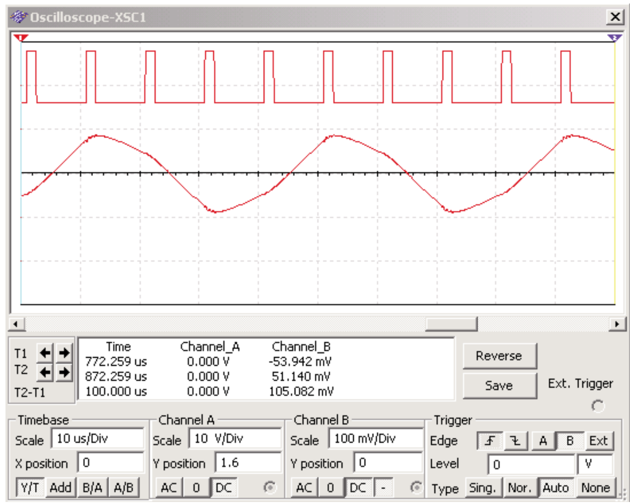


Figure 3: *One simple, applicable, Linear-Interpolation System*

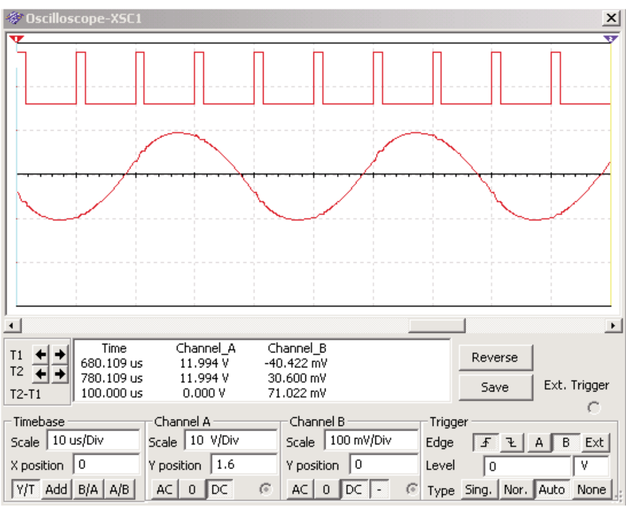


a) *Step interpolator*
(Output low-pass filter R = 1k5, C = 1n)



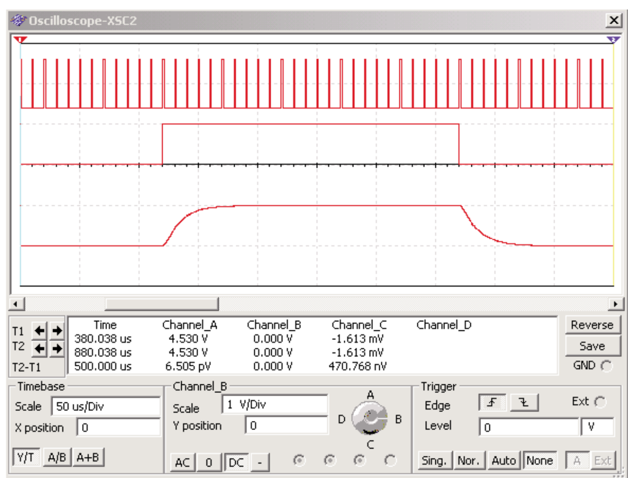
b) *Linear interpolator*
(Output low-pass filter R4 = 1k5, C4 = 1n)

NOTE: *Tsamp = 10usec, Pulse width = 1usec, Input sinusoidal signal 500mVpk, F = 25kHz*



c) *Restored sinusoidal signal*
(500mVpk, F = 25kHz, Output low-pass filter R4 = 1k5, C4 = 6n8)

NOTE: *Tsamp = 10usec, Pulse width = 1usec*



d) *Reaction to the impulse (inverted)*
(1V, Period = 0.5msec, Pulse width = 0.25msec, Output low-pass filter R4 = 1k5, C = 1n)

Figure 4: *Practical results of restoring signals with the Linear Interpolator System*

Professor Dr Dogan Ibrahim from the Department of Computer Engineering at the Near East University in Cyprus describes the design of a GPS data logger device with SD card storage, where the collected data can be displayed in street-level using the Google Earth mapping program

GPS data logger with SD card storage and GOOGLE EARTH map interface

THE GLOBAL Positioning System (GPS) is a satellite-based navigation system developed by the US Department of Defence. The first GPS system was tested in 1960s using a constellation of five satellites. This system was implemented for military purposes and provided navigational fix data approximately every hour; it was not very accurate.

In 1993 the number of satellites increased to 24. The system became fully operational and it was also made available to the civilians with a lesser accuracy. Initially, the accuracy of the civilian GPS system was deliberately disturbed using a method called Selective Availability (SA). With the SA, the position accuracy of a typical civilian GPS receiver was about 100 metres. In the year 2000 the US Department of Defence removed the SA and, as a result, the position accuracy of a basic GPS increased to around 10 metres.

GPS has now become a widely used aid to navigation and it is commonly used in many applications such as land surveying, shipping, piloting, route guidance, map making, study of earthquakes, precise time reference and hobbies and games such as geocaching.

The GPS Satellites

The GPS satellites orbit the Earth twice a day with a speed of 3.9km per second. The four satellites are visible at any point on earth at any time. Normally, three satellites are required to calculate the position of a point accurately on Earth's surface and four satellites are required to calculate the altitude as well. Thus, with the arrangement of the satellites it is possible to calculate both the position and the altitude of any point on Earth's surface accurately. In typical applications it is possible to get signals from at least six or seven satellites in a place with a

ERROR SOURCE	ERROR (METRES)
Selective Availability	30
Ionosphere	5.0
Orbit Errors	2.5
Satellite Clock	1.5
Signal Multipath	0.6
Troposphere	0.5
Receiver Noise	0.4

Table 1: *GPS error sources*

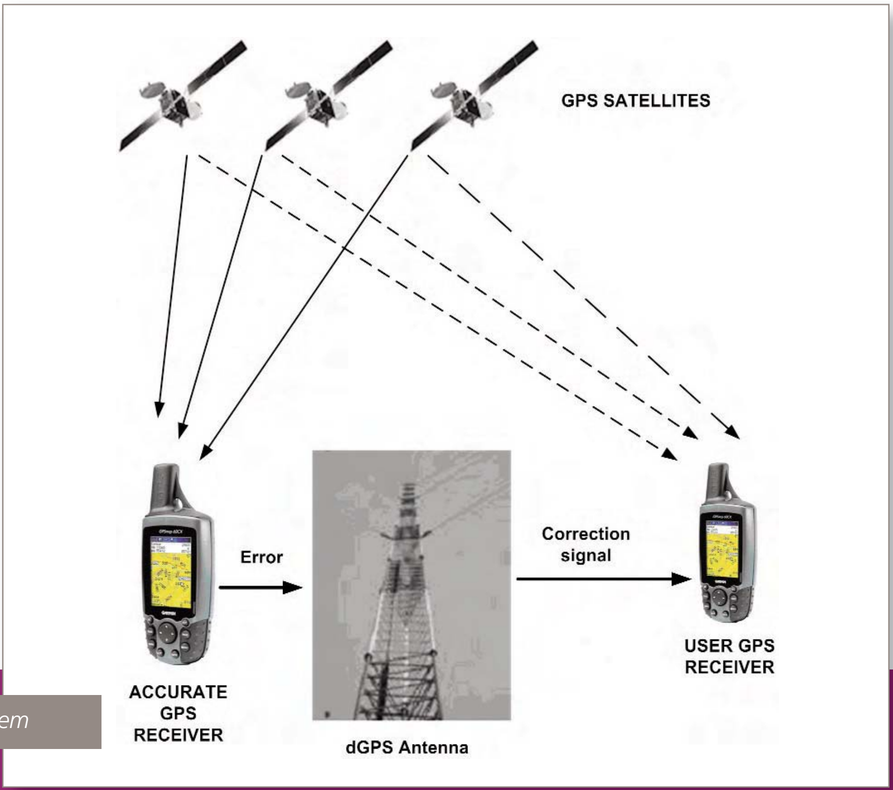


Figure 1: *dGPS correction system*

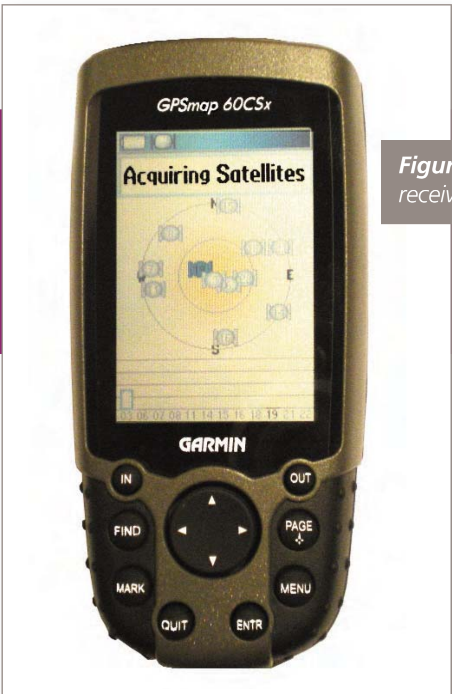


Figure 2: *A typical commercial GPS receiver, such as this one from Garmin*

clear view of the sky. In general, the accuracy is increased as more satellites are used in the position and altitude calculations.

The GPS Accuracy

Table 1 shows the typical GPS error sources (www.kowoma.de/en/gps/errors.htm). The major source of GPS error was the Selective Availability. Selective Availability was first introduced during the Gulf War in 1991 to prevent the Iraqi forces from benefiting from the accurate GPS service. What the US military chiefs did was not to prevent all non-military use of the GPS, but to degrade the accuracy of the GPS to commercial users. By the introduction of a deliberate error, the accuracy of a commercial GPS was reduced to around 100 meters and accurate receivers were only made selectively available to only the US and Allied military and to certain US Government agencies. Fortunately, the Selective Availability has been removed by the US since the 1st May 2000 and, hence, the navigational accuracy of a GPS improved significantly.

The tropospheric and ionospheric effects cause electromagnetic waves to refract. The reasons for the refraction are different concentrations of water vapour in the troposphere, caused by different weather conditions. The ionospheric errors are larger than the tropospheric errors. The errors introduced by these effects can not be eliminated, but their effects can usually be reduced in calculations.

Orbital errors are the other major sources of error, caused by the satellite geometry. If for example a receiver sees four satellites and all are arranged in the north-west, this leads to a bad geometry and the accuracy is reduced. If on the other hand the four satellites are well distributed over the Earth, the position accuracy will be much higher. Most GPS receivers do not only indicate the number of received satellites, but also their relative positions above Earth. This enables the user to judge if a relevant satellite is obscured by an obstacle and if changing the position of the receiver might improve the accuracy.

The multipath effect is caused by reflection of satellite signals from objects on Earth's surface. The multipath error in GPS systems appear when there are large buildings near a GPS receiver and the signal reflects from these buildings. The reflected signal takes more time to reach the receiver than the direct signal and this results in accuracy errors. The multipath errors can be avoided by moving the receiver away from nearby large buildings or trees.

Improving the GPS Accuracy

The position accuracy of a GPS signal can be improved significantly using a technique known as Differential GPS (dGPS). Using the dGPS techniques accuracies in the region of several meters can easily be achieved.

dGPS works by placing a high performance GPS receiver at a precisely known location on Earth (reference station). Since this reference receiver knows its exact location, it can determine the errors in the received GPS satellite signals. This error signal for each tracked satellite is formed into a correction message and is transmitted to ordinary GPS receivers. Users with the correct hardware can receive these correction signals and improve their accuracies. The level of accuracy obtainable with dGPS depends upon many factors, such as the quality of the reference station and user GPS receivers, and the atmospheric conditions. **Figure 1** shows the layout of a typical dGPS implementation.

Although dGPS-based systems provide high accuracies, they add extra complexity and also increase the cost of the basic navigation system.

Another technique used to improve the accuracy of the GPS system is to transmit correction signals from "correction" GPS satellites. The correction satellite is a geostationary satellite above the Equator. This technique was first developed in the US and is known as WAAS (Wide Area Augmentation System). A similar and compatible system is in operation in Europe under the name EGNOS and in the Far East under the name MSAS. Standard compatible GPS receivers can receive the WAAS/EGNOS correction signals and calculate their positions to an accuracy of around 3-5 metres.

The advantage of this technique over the dGPS is that there is no additional cost to the user since the required hardware and software are built into the GPS receiver at a very small extra cost. One disadvantage of this technique is that it may be difficult to receive correction signals at higher latitudes, away from the Equator.

Parts of a GPS System

The GPS system consists of three major parts:

- Space segment
- Control segment
- User segment

Space segment: The space segment consists of the orbiting satellites. The number of satellites is increasing all the time. As of March 2008, there were 31 actively broadcasting satellites in the GPS constellation. With the increased number of satellites, the reliability and availability of the overall system has been improved.

Control segment: The control segment consists of the monitoring stations located on Earth. These stations constantly monitor the operational status of all the GPS satellites and also synchronize the atomic clocks on board the satellites to within a few nanoseconds of each other and adjust

```
$GPGLL,5127.3513,N,00003.2305,E,220702,A,A*40
$GPBOD,,T,,M,,*47
$GPVTG,74.7,T,77.1,M,0.0,N,0.0,K,A*26
$PGRME,14.6,M,18.5,M,23.6,M*16
$PGRMZ,72,f,*1D
$PGRMM,Ord Srvy GB*1B
$HCHDG,245.6,,,2.5,W*39
$GPRTE,1,1,c,*37
$GPRMC,220704,A,5127.3506,N,00003.2307,E,0.0,74.7,051108,2.5,W,A*30
$GPRMB,A,,,,,,,,,,,,V,A*1C
$GPGGA,220704,5127.3506,N,00003.2307,E,1,03,2.2,67.7,M,47.0,M,,*73
$GPGSA,A,2,,,04,,,,,,23,,31,,0.0,2.2,2.2*34
$GPGSV,3,1,12,01,27,049,00,02,09,310,18,04,51,293,39,07,18,317,00*78
$GPGSV,3,2,12,11,22,155,00,13,50,202,00,17,30,237,00,20,49,085,25*7B
$GPGSV,3,3,12,23,76,125,20,25,16,157,15,31,16,034,37,32,26,082,18*79
$GPGLL,5127.3506,N,00003.2307,E,220704,A,A*40
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Figure 3: *Typical NMEA sentences*

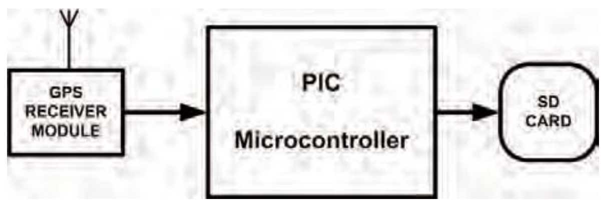


Figure 4: *Block diagram of the project*

the orbital model of each satellite.

User segment: The user segment consists of the user GPS receivers. A GPS receiver is a small battery-operated portable device similar in size to a mobile phone. As shown in **Figure 2**, the device is equipped with a large LCD display, a few buttons and an antenna (usually built-in). The device receives signals from the GPS satellites and then displays user's position, altitude, speed, heading and several other navigational parameters. Some sophisticated receivers also incorporate street level maps where the position of the user is shown dynamically in real time on the map. GPS receivers are also used in car navigation systems and can help the user to navigate to an unknown address or post-code by displaying street level turns or by audio outputs.

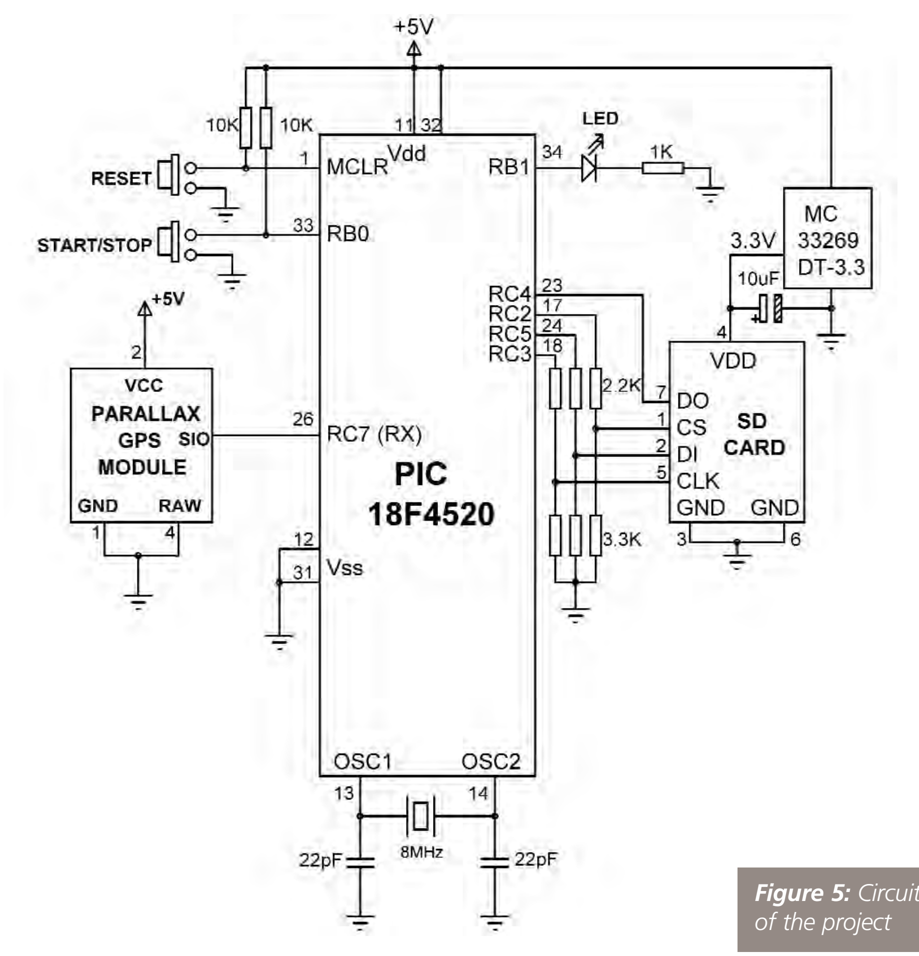


Figure 5: *Circuit diagram of the project*

GPS receivers may include an input for differential dGPS corrections, known as the RTCM interface. As mentioned earlier this interface improves the accuracy of the receiver considerably. In addition to the RTCM interface, some more sophisticated GPS receivers include WAAS/EGNOS correction hardware and software to improve the accuracy of the basic GPS receiver.

GPS receivers also produce RS232-compatible serial output data known as NMEA sentences, which enable them to be connected to a PC (or similar equipment) to relay the navigational data such as the latitude, longitude, altitude, speed, heading and so on. More details are given in the next section about the NMEA interface, as this is used in this project to get the time and geographical co-ordinates of the user.

The NMEA Sentences

Many high-end GPS receivers provide navigational output data so that the device can be connected, for example, to a PC to collect and analyse this data. This output data is usually in serial format and the communication protocol conforms to the RS232 serial standards.

The default serial communication parameters of most GPS receivers are set as follows:

- 4800 Baud
- 8 data bits
- No parity bit
- 1 stop bit

The data output from a GPS receiver is in ASCII text format and is known as the NMEA 0183, or simply the NMEA format. According to this format, navigational information are sent in the form of "sentences", where each NMEA sentence starts with a "$" sign, the navigational parameters are separated by commas and each sentence is terminated with two hexadecimal checksum characters.

The NMEA sentences are usually sent out every second. **Figure 3** shows the NMEA sentences obtained when a Garmin GPSMAP 60CSX type GPS receiver is connected to the serial port of a PC and a serial communication program, such as the HyperTerm (www.hilgraeve.com/), is activated on the PC to display the data received from the serial port.

There are many NMEA sentences for different navigational parameters. In addition to the standard NMEA 0183 protocol, some GPS manufacturers create and define NMEA sentences specific to their own products. The NMEA sentence used in this project is the $GPRMC, having the following parameters: **$GPRMC:** Although there are some variations in its format, this sentence basically defines the basic navigational parameters, speed, course, date of fix and the magnetic variation. An example is:

$GPRMC,220704,A,5127.3506,N,00003.2307,E,0.0,74.7,051108,2.5,W,A*30

Here:

220704	**Fix taken at 22:07:04**
A	**Navigational data is correct**
5127.3506,N	**Latitude 51 deg. 27.3506 min. North**
00003.2307,E	**Longitude 0 deg. 3.2307 min. East**
0.0	**Speed over ground (knots)**
74.7	**Course made good**
051108	**Fix taken on 5 November, 2008**
2.5	**Magnetic variation 2.5 deg West**
30	**Checksum**

The Project Outline

The block diagram of the project described in this article is shown in **Figure 4**. Basically, a microcontroller receives the $GPRMC sentences from a GPS receiver module as the device moves around. The collected data is stored on an SD card continuously with time stamping. This data is then formatted and used as an input to the Google Earth (http://earth.google.co.uk) mapping program to display the track of the movement with or without time stamping.

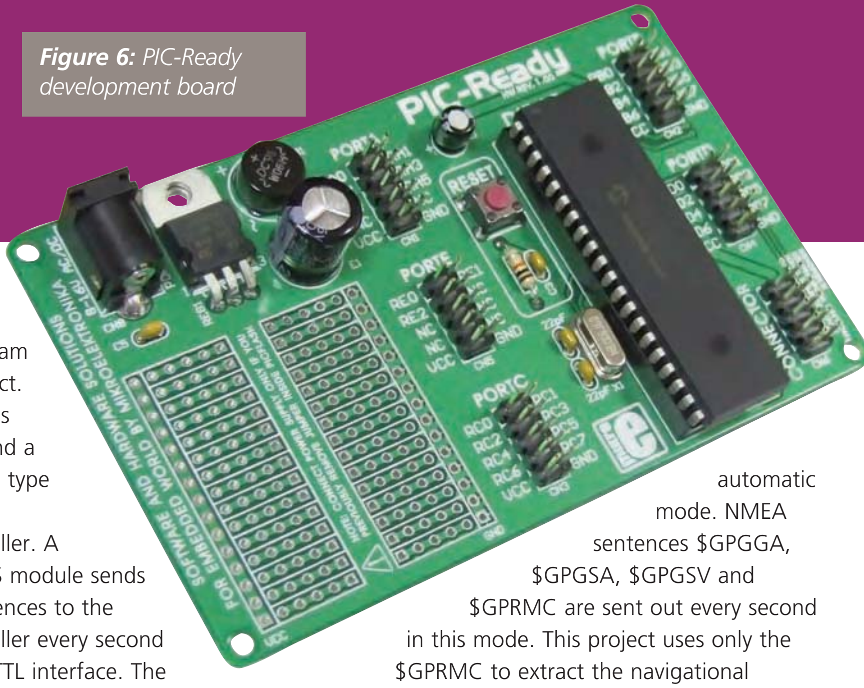


Figure 6: *PIC-Ready development board*

Figure 5 shows the circuit diagram of the project. The design is based around a PIC18F4520 type advanced microcontroller. A Parallax GPS module sends NMEA sentences to the microcontroller every second via a serial TTL interface. The microcontroller receives the NMEA sentences, extracts the $GPRMC sentence and then extracts the time, latitude and longitude of the user co-ordinates and stores this data every two seconds in a file on the SD card. This file is then formatted to be compatible with the Google Earth mapping software, using the GPS Visualizer (www.gps visualizer.com) software package. The Google Earth software can then show the user movements on a street-level map.

The GPS Module

A Parallax GPS module is used in the design. This is a small, low-cost GPS with the following features:

- On-board passive patch antenna;
- Single wire, 4800 baud serial TTL interface;
- Provides either raw NMEA output, or specific data can be requested via a command interface;
- Operates with single +5V supply.

The GPS module has four pins:

- Pins 1 and 2 are the ground and the supply voltage respectively;
- Pin 3 is the TTL compatible, non-inverted serial input-output pin. The data format is 4800 baud, 8 data bits, no parity.
- Pin four is the output format selection bit, called the RAW pin. When RAW is low, the GPS module sends out NMEA sentences automatically every second. When RAW is high (or unconnected), specific GPS data (e.g. the latitude) can be requested from the device by sending commands. In this project the GPS module is operated in the automatic mode. NMEA sentences $GPGGA, $GPGSA, $GPGSV and $GPRMC are sent out every second in this mode. This project uses only the $GPRMC to extract the navigational parameters. Parallax GPS module outputs the $GPRMC sentence in the following format:

$GPRMC,220704,A,5127.3506,N,00003.2307,E,173.8,231.8,130608,,,A*70

Notice that the magnetic variation and its direction are not output by the Parallax GPS module.

The Key Elements of the Project

The SD card is connected to port pins RC2 through RC5 of the microcontroller and is operated in SPI mode. A card holder is used to physically make connections to the card pins. The voltage at output pins of the micro-controller is too high and can damage the input circuitry of the SD card. A pair of potential divider resistors (using 2.2K and 3.3K resistors) is used to lower the microcontroller output voltages to a level acceptable by the SD card inputs. The SD card is powered using a 3.3V regulated supply, obtained using a MC3269DT-3.3 (www.volkin.com/MC3269DT-3.3.html) type regulator. In this project, a ready-made SD card module is used (see **Figure 7**), which is available from mikroElektronika (www.mikroe.com).

A PIC18F4520 type microcontroller (MCU) is used in the design. The microcontroller is operated with an 8MHz crystal. A push-button switch is connected to port RB0 pin and a small LED is connected to port RB1 of the microcontroller. Pressing the switch

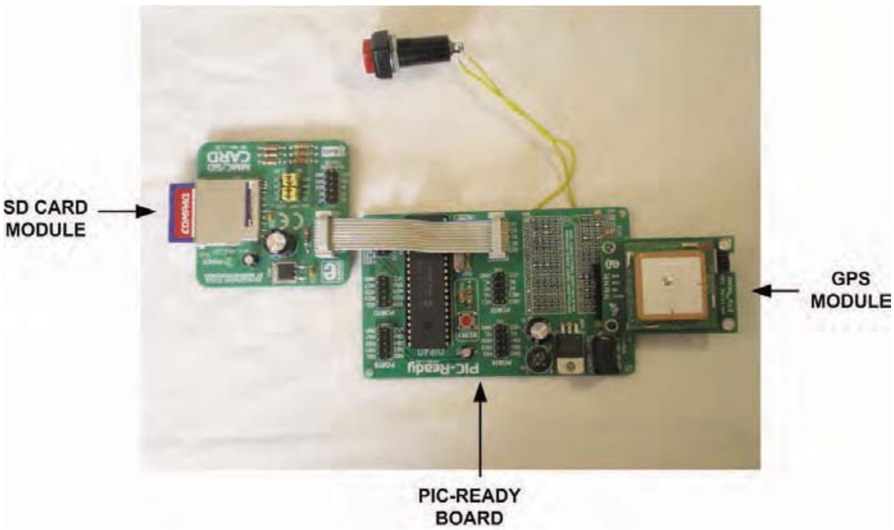


***Figure 7:** The GPS data logger device*

```
BEGIN
      Configure I/O ports
      Wait until START is pressed
      Initialise USART library
      Initialise SD card library
      IF SD card is not present
            Flash LED rapidly
            Wait forever
      ENDIF
      Create a new file on SD card
      DO FOREVER
            Turn on LED
            Wait 500ms
            Get GPS data
            Extract $GPRMC sentence parameters
            Store time, lat, lon on SD card
            IF STOP pressed
                  Turn OFF LED
                  Wait forever
            ENDIF
            Turn OFF LED
            Wait 500ms
      ENDDO
END
```

***Figure 8:** Operation of the software*

starts and stops the data collection. During the data collection the LED flashes at a rate of about once a second. If the SD card is not inserted into its holder, the LED will flash quickly to show an error condition. The switch should be kept pressed for about five seconds to terminate the data logging and wait until the LED turns OFF before removing the SD card from its holder.

The hardware was constructed on a PIC-Ready development board (see **Figure 6**) manufactured by mikroElektronika. This is a low-cost ($24) powerful development board with the following features:

- Socket for 40-pin PIC microcontrollers;
- 8MHz crystal;
- +5V regulator (an external 9-12V power supply is required);
- In-circuit debugger (ICD) and PIC programmer interface;
- Reset button;
- Easy access to microcontroller port pins via 10-way IDC connectors;
- Plug-in compatible with most mikroElektronika development modules;
- Small development solder area.

One of the nice things about the PIC-Ready development board is the built-in ICD and the programmer. This requires the use of a PICFlash2 ICD device, manufactured by mikroElektronika. During program development one can easily insert breakpoints or single step a program with the help of the ICD. The ICD can also program most of the PIC chips on-board, without having to remove the chip from its socket. This feature is extremely useful during program development.

Figure 7 shows the GPS data logger device built on a PIC-Ready development board. The SD card module can be seen on the left, while the GPS module is on the right hand side of the board.

The Software

The software was developed using the mikroC compiler developed by mikroElektronika. This is a very powerful C language compiler and supports both PIC16 and PIC18 series. The compiler provides a very rich library of routines for developing applications for SD cards, Compact Flash cards, RS232/RS485 devices, USB, CAN bus, I2C, 1-Wire bus and much more.

Figure 8 shows operation of the software as a Program Development Language (PDL). The program is modular and consists of a number of functions and procedures for easy modification, update, or maintenance of the code. The following functions and procedures are used:

Format_Data: This procedure reads the received $GPRMC data from array DataLogger and stores in array LogIt in the following comma delimited CSV text format. This data is then written to a file on the SD card continuously every two seconds:

T,22:05:16,5133.3627,00042.1240

The data is stored in a format compatible with the GPS Visualizer conversion program, where:

Character T indicates that this is a track file
22:05:16 is the time the data was received
5133.3627 is the latitude
00042.1240 is the longitude

As explained later, the GPS Visualizer program converts the file into a format compatible with the Google Earth mapping program.

Get_GPS_Data: This procedure reads the NMEA sentence $GPRMC from the serial port where the GPS module is connected. The program first waits to receive the starting character "$". Then the string "GPRMC" is matched and its parameters are read and stored in array DataLogger.

Initialize_SD: This procedure initializes the SD card library routines of the mikroC compiler.

Hex_Byte: This function converts a hexadecimal number into decimal. This function is used in the checksum calculation.

Conv_Hex: This function converts a two digit hexadecimal number into decimal. This function is used in the checksum calculation.

Checksum: This function checks the checksum field of the received NMEA sentence. The checksum field in an NMEA sentence is the last two hexadecimal characters after the "*" character. The checksum is calculated by Exclusive-OR'ing all the characters in a sentence, except the "$ character and the "*" character. This function calculates the checksum and compares with the received checksum. If the two differ, a zero is returned to indicate an error in the received data and the data is discarded and read again. If the checksum is correct the function returns a one. **Figure 9** shows how the checksum can easily be calculated by writing a "C" function. Variable chk is initialised to zero at the beginning of the function. A while loop is then formed to check each character of the received NMEA sentence. A "$" or a "*" character are ignored. Any other received character is saved in variable chk and then 'Exclusive-Or'ed with the older one. This way, the result is the Exclusive-OR (or the checksum) of all the received characters. Variable chk2 is the decimal equivalent of the received checksum which is compared with the calculated checksum chk.

At the beginning of the program PORT B is configured to be a digital port and the program waits until the START/STOP push-button switch is pressed. After the switch is pressed the USART is initialised to 4800 Baud. The program then attempts to initialise the SD card. If there is no card in the card holder the LED flashes rapidly to indicate an error condition. If on the other hand a card is found in the card holder then a new file is created on the card. The created filename is in the following format:

GPSLOGnn.TXT

Where nn is a number stored in the first location of the EEPROM memory. nn is between 01 and 99 and is incremented each time the device is started to collect new data, thus causing a new file to be created every time the data collection is started. The program then enters an endless loop where after receiving valid data from the GPS module, the time, latitude and longitude of the user are determined and stored on the SD card. The loop terminates if the START/STOP button is pressed for more than a few seconds. The data is stored on the SD card in comma delimited CSV format as shown in **Figure 10**, where the first row is a header describing what type of data is stored in each column of the file.

Google Earth Interface

The collected data (see Figure 10) should first be converted into a format suitable to be displayed by the Google Earth mapping program. Google Earth accepts KML (Keyhole Marked Up Language) and KMZ (compressed KML file) formatted files (http://code.google.com/apis/kml/documentation). There are many programs on the Internet that can be used to convert the CSV type file created in Figure 9 into KML or KMZ format. The program used in this project is the GPS Visualizer (www.gpsvisualizer.com). GPS Visualizer is a free, easy-to-use online utility that creates maps and profiles from GPS data, street addresses, or simple co-ordinates. The program can convert between various navigational co-ordinates, calculate the distance between two co-ordinates or two addresses, and many more.

The conversion process is very simple and is given in **Figure 11**.

- Start the GPS Visualizer;
- Select Convert a File from the top menu;
- Click on Google Earth Mapping Form;
- Click Browse under Upload your GPS data files here;
- Select the file to be converted (on the SD card);
- Select Yes, with no names in Draw as Waypoints list-box, under the Track Options;
- Choose a colour for the track (if desired) under Track Options (the default track colour is magenta);
- Click Create KML File to create a converted output file that is compatible with Google Earth.

The file will be converted and a new form will be displayed. Click on the converted filename to invoke the Google Earth program automatically and display the track (Note that the Google Earth software must be installed in order to invoke it and display the track data on the map).

```
unsigned char Checksum(void)
{
        unsigned char chk = 0;
        unsigned char i = 0;
        unsigned char chk2;

        while(DataLogger[i] != '*')
        {
                switch(DataLogger[i])
                {
                        case '$':
                                break;
                        case '*':
                                continue;
                        default:
                        {
                                if(chk == 0)
                                                chk = DataLogger[i];
                                else
                                                chk = chk ^ DataLogger[i];
                        }
                        break;
                }
                i++;
        }
//
// Compare calculated checksum (chk) with the Checksum read from
// the NMEA sentence (chk2). If the Checksum is correct return 1,
// otherwise return 0.
//
        chk2 = Conv_Hex(DataLogger[64], DataLogger[65]);
        if(chk == chk2)
                return(1);
        else
                return(0);
}
```

Figure 9: *Checksum calculation function*

Figure 10: *Example collected data*

```
type,time,lat,lon
T,13:37:12,5127.3687,00003.1291
T,13:37:14,5127.3684,00003.1283
T,13:37:16,5127.3681,00003.1278
T,13:37:18,5127.3679,00003.1276
T,13:37:20,5127.3678,00003.1275
T,13:37:22,5127.3678,00003.1276
T,13:37:24,5127.3677,00003.1275
T,13:37:26,5127.3678,00003.1275
T,13:37:28,5127.3679,00003.1275
T,13:37:30,5127.3680,00003.1274
T,13:37:32,5127.3681,00003.1275
T,13:37:34,5127.3712,00003.1345
T,13:37:36,5127.3727,00003.1423
```

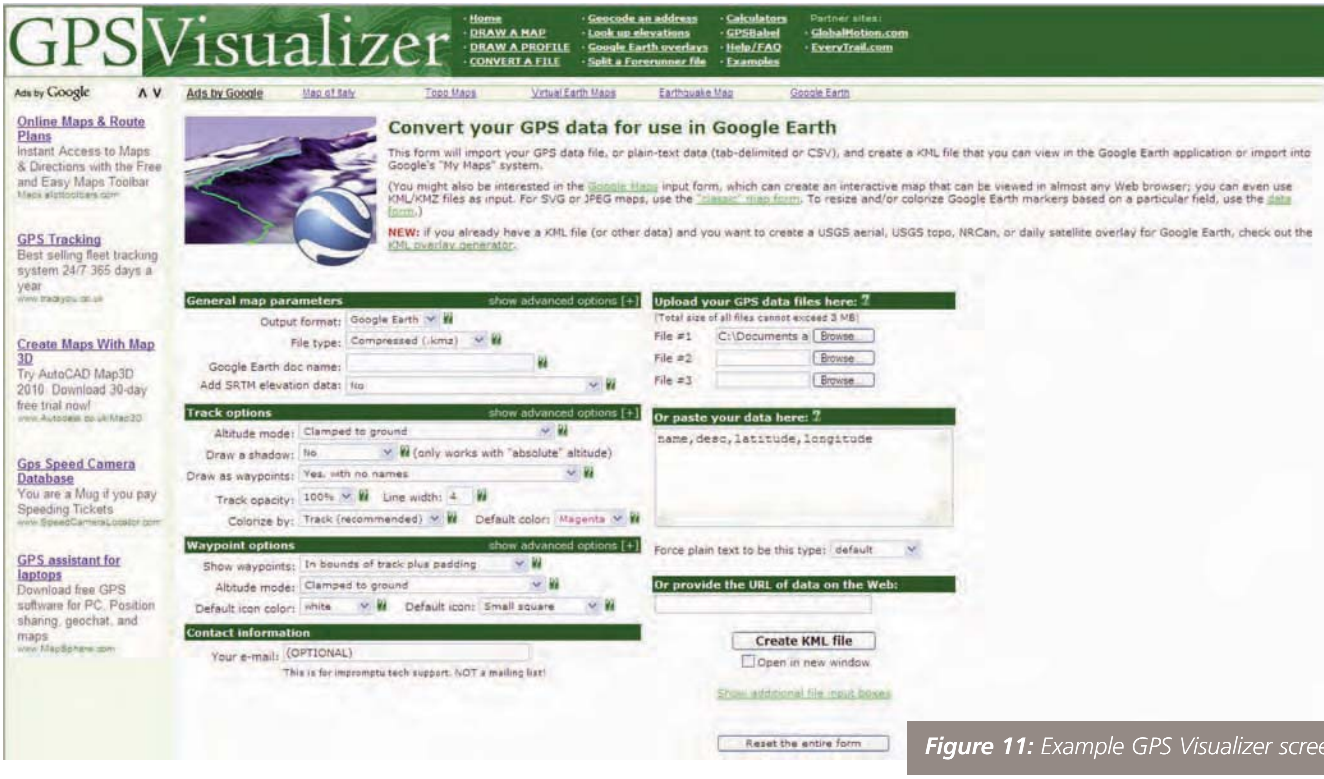


Figure 11: Example GPS Visualizer screen

Figure 12 shows an example output of displaying the track data at street-level using the Google Earth. In this example, the GPS data logger device was placed in a car and a short trip was made is South East London to collect data and test the device. As can be seen from Figure 11, the collected data is very accurate and the data points are placed exactly on street co-ordinates in the Google Earth map display. In **Figure 13**, the same data is displayed with time stamping where the time display is enabled in the GPS Visualizer conversion program before the file is converted (i.e. Select Yes, named with time stamps in Draw as Waypoints list-box, under the Track Options).

Further Improvements

The device described in this article can be improved in several ways:

- Other navigational parameters can be added to the system, such as the speed, bearing and the altitude.
- The power consumption of the device can be lowered using low-power version of the microcontroller, i.e. PIC18LF4520.
- A file conversion utility can be added to the microcontroller software so that the created file is compatible with the Google Map (i.e. in KML or KMZ format) and can be used directly without having to re-format it first.
- An LCD and a keypad can be attached to the device to make it more user friendly, e.g. to display the date, time, speed, or the geographical co-ordinates of the user as the device moves around.
- The data collection interval and the collection algorithm can be modified such that new data is stored only if the device is not stationary. ■

Figure 12: Displaying the data using Google Earth

Figure 13: Displaying the data with time stamping

EMC Analysis

Ian Darney goes into the detail of EMC analysis and the simulation of some critical tests

THE DEVELOPMENT of electronic systems has come a long way since the invention of valves and transistors. Inevitably, the complexity of equipment has also increased, bringing with it the need for systematic control of the development process. Any product can now be designed to meet requirements such as frequency response, power consumption, size, mass and reliability.

One notable exception to the list is Electromagnetic Compatibility (EMC). Although there is a multitude of EMC test requirements, sufficient to keep all the test houses busy for the foreseeable future, there is no systematic way of relating these requirements to the design process.

Many books have been written on the subject. All of them emphasise the complexity of the phenomena, describing in detail many of the myriad ways a signal emanating from one unit of equipment can interfere with the performance of a separate unit, or even a separate system. Many tips and fixes are suggested. Some guidance is ambiguous. One source of advice can contradict another.

In these circumstances, few equipment designers feel competent to handle the problems raised by the EMC requirements. The usual course of action is to implement the advice provided by a trusted expert, explain the details to a design review committee, finalise the design, organise the formal EMC tests and hope for the best.

Simplifying Matters

This state of affairs exists, even though the underlying physics has been well understood for over a century. Electrical design is based on circuit theory that is itself a development and simplification of electromagnetic theory.

One possible reason for this situation is that there is an inexorable increase in complexity in the treatment of every aspect of EMC.

A radical re-think is called for. The search should be for ways of simplifying the problems. The aim should be to provide the engineer at the bench with analytical tools that are useable on a day-to-day basis. After all, personal computers are now in common use. SPICE software allows input data to be entered quickly and easily. Analysing the response of a multi-node circuit is no problem at all.

Since circuit diagrams are familiar to all designers, the need is to invoke the use of circuit models. If it were possible to create a model of any particular signal link, identifying the coupling parameters in terms of current, voltage, inductance, capacitance and resistance, then the performance of that link could be defined in terms of its susceptibility and emission characteristics.

Such an objective is not difficult to achieve. All the clues are available in the old textbooks. Perhaps the most significant of these is the formulation of equations for the inductance and capacitance of the conductors of a three-phase power line. Using this approach to define the properties of the conductors involved in transmitting a signal from one location to another leads to the creation of the general circuit model of **Figure 1**.

In this model, the transmission link consists of two conductors: 'signal' and 'return'. The conductor identified as 'structure' represents the parallel combination of all the other conductors linking the two units. The effect of all the other signals in the system can be represented by the voltage source.

The existence of this voltage source calls into question the widespread belief that the reference voltages of units 1 and 2 are identical. There is no way of reconciling the model of Figure 1 with the notion of a conducting surface on which all points are at zero voltage. The concept of the 'equipotential ground plane' needs to be abandoned. It derives from a misunderstanding of the image solution method used in electromagnetic theory.

A further consequence is that the 'earth' and 'ground' symbols have no place in any circuit diagram used to assess interference coupling.

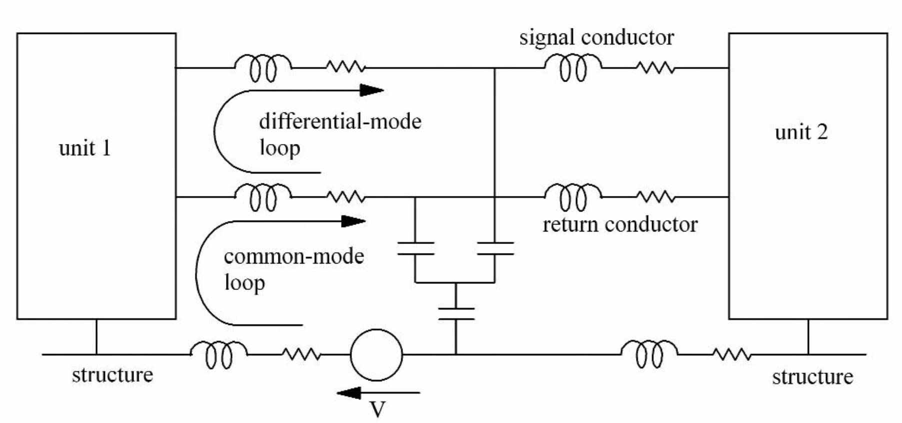


***Figure 1:** General circuit model of coupling parameters*

Critical Tests Simulations

Going back to Figure 1, units 1 and 2 could represent two separate items of equipment connected by a long cable, two printed circuit boards within an equipment unit, two components on a printed circuit board, or even two components within an integrated circuit. The inductors, capacitors and resistors identify the characteristics of the three conductors.

Values for every one of these can be determined from measurements of radius and length, or from electrical measurements. Coupling between the differential-mode loop and the common-mode loop can be analysed by

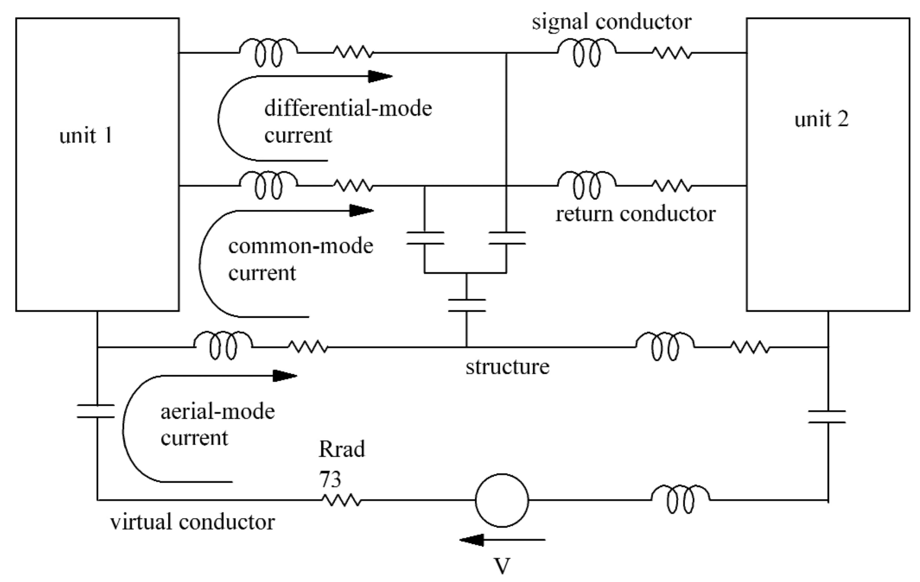


Figure 2: *Analysing the response to external radiation*

SPICE simulation. Such software can handle either transient analysis or frequency analysis.

The configuration of Figure 1 shows how conducted susceptibility tests can be simulated. Here, the voltage source, in the form of an injection transformer, is inserted in series with the common-mode loop. This creates a current flow which induces current in the differential-mode loop via the coupling impedance of the return conductor, resulting in unwanted signals at the terminals of both units.

The SPICE model can be extended to simulate the response of the internal circuitry of both units. If the amplitude of the source voltage is set at the same value as the test requirements, then the results of formal EMC tests can be predicted.

With conducted emission tests, the voltage source is the output signal from one of the units. To simulate this, the voltage source would be in the differential-mode loop and the monitored signal would be the common-mode current. The simulated output can be compared with the test requirements.

This circuit model can also be used to simulate wire-to-wire coupling. In this case, the structure would carry the return current and would form the coupling impedance for both signals.

It is a simple matter to transform the model into one that uses distributed parameters. This will allow simulation well beyond the frequency of quarter-wave resonance. SPICE software is not designed to handle such parameters, but mathematical software such as Mathcad is well-suited to the task.

Simple test equipment can be used to carry out bench checks on the equipment-under-review, to refine the circuit model. A signal generator and an oscilloscope are the most expensive items. Voltage injection transformers and current monitor transformers are quite easy to construct. Test results are easy to interpret and process. Bench testing is an essential part of any development process.

These tests would establish the frequency response of the ratio between unwanted output current in one loop and source voltage in the other; the transfer admittance. A useful feature of the transfer admittance is that it applies to both conducted emission and conducted susceptibility. This means that a wiring configuration which exhibits susceptibility problems at a particular frequency is also likely to have emission problems at that frequency.

By adding a third loop to the configuration, as shown on **Figure 2**, it is possible to simulate the effect of radiated susceptibility tests. Here, it is assumed that worst-case conditions apply. The assembly is assumed to behave as a dipole aerial. Unless the equipment is specifically designed as an aerial, this represents the maximum coupling with the environment which can reasonably be assumed.

Aerial Mode Current Simulation

Aerial-mode current is simulated by including a virtual conductor in the model to represent the effect of the environment. When the aerial is operating at maximum gain, the reactive components linking the conductors to the environment act as a series tuned circuit. So the only limit to the current is provided by the resistive components. These are the resistance of the structure in series with the radiation resistance *Rrad* of the dipole. For a dipole aerial, the radiation resistance is 73 ohm.

The voltage source is a function of the power *Pt* radiated by the transmitting antenna and its separation distance *r* from the cable-under-test. The power density at the surface of the cable is:

$$S = \frac{Gt}{4 \cdot \pi \cdot r^2} \cdot Pt \qquad (1)$$

where *Gt* is the gain of the antenna that will be used during formal susceptibility tests.
The electric field strength is:

$$E = \sqrt{S \cdot Zo} \qquad (2)$$

where *Zo* = 377 ohms.

At all frequencies at or above quarter-wave resonance, the voltage source of Figure 2 can be related to the electric field by:

$$V = \frac{\lambda}{\pi} \cdot E \qquad (3)$$

where λ is the wavelengthis the wavelength. This is effectively an envelope curve through the peaks in the actual response. It is assumed that the *E*-field is aligned with the conductors.

At all frequencies below quarter-wave resonance, the amplitude of the voltage source can be determined using:

$$V = \frac{4 \cdot l}{\pi} \cdot E \qquad (4)$$

where *l* is the length of the conductor assembly between units 1 and 2. This is a flat response at the same level as the highest voltage that can be achieved along the cable at quarter-wave resonance.

This set of equations is about as simple as you can get. Even so, it establishes a clear relationship between power radiated by the test antenna and the voltage source of Figure 2. Applying this source to the model will allow the effect on the functional performance to be assessed. Results of radiated susceptibility tests can be predicted.

To analyse radiated emission, the first step would be to determine the conducted emission characteristic; that is, the variation of common-mode current with frequency.

If the voltage source in Figure 1 were to be located in unit 1, rather than as shown, then the signal current in the differential-mode loop would develop a voltage across the inductors and resistors of the return conductor. This would create a current *I* in the common-mode loop. If it is assumed that the structure provides no shielding, then the cable conductors can be treated as a transmitting aerial. The magnetic field *H* at a distance *r* can be related to the common-mode current:

$$H = \frac{I}{2 \cdot \pi \cdot r} \quad (5)$$

The power density at the receiving antenna is:

$$S = Zo \cdot H^2 \quad (6)$$

Maximum power received by a matched load is:

$$Pr = \frac{Gr \cdot \lambda^2 \cdot S}{4 \cdot \pi} \quad (7)$$

where *Gr* is the gain of the receiving antenna that will be used during formal emission tests.

Equations 5 to 7 establish a clear relationship between the common-mode current *I* and the power received by the monitor antenna when it is positioned for maximum pick-up. By combining the results of a circuit simulation with this set of equations, the outcome of a radiated emission test can be predicted.

Shielding Effect Analysis

The shielding effect of the structure can be analysed by using techniques developed by Lightning Technologies at Culham Laboratories to determine the indirect effects of lightning on aircraft electronics. Another approach would be to use the methodology developed by the Ordnance Board to assess the immunity of electro-explosive devices to electromagnetic radiation. The shielding factor so derived can be included in the analysis of radiated emission or radiated susceptibility.

It may seem that this approach is over-simplistic and does not provide precision analysis. However, the objective is to acquire a reasonable degree of confidence that the equipment-under-review will pass a set of formal EMC tests. Since worst-case conditions are assumed, any errors in the analysis are always on the safe side.

Only a few critical circuits in any given system require the full analytical treatment. These can be selected using knowledge of the physical structure, the coupling mechanisms and the function of the signal-under-review.

The process is more systematic than implementing a set of tips and fixes and hoping for the best.

More details of this approach are available at www.designemc.info. ■

LETTERS

LET'S MAKE SOME PROGRESS

Recent correspondence in Electronics World (May and June) about the Catt Question suggested that it was a "non problem", or that a new theory was not necessary. In fact, the opposite is true; the reasons why are given in a paper at Google search 'Mitchell J Feigenbaum-Galileo's child'. This paper completely overturns everything that has been written in physics since Principia including Maxwell's equations, Lorentz transformations, E = mc^2 and particles.

There is a "dead world" in which particles can move uncontrollably fast (page 22), where the charge on the southern conductor may reside – perhaps?

If contributors address this paper, we will be able to make some progress on a sound and proper basis, explaining some of the other outstanding issues in contemporary physics, such as the cosmological constant, dark matter and dark energy, the fine structure constant or gyromagnetic factor etc. For example, put 1.87Hz in the resonance equation LC=1/4pi^2f^2 to get 1/137, which compares to Somerfeld's spectroscopic value 0.00729 to about 0.2%.

Why? It's the price one pays for understanding Universality a bit better; see page 207 of 'Does God Play Dice?', or page 174 of James Gleich's 'Chaos'.

Real dynamic systems exhibit quasi-periodic oscillations which are nothing like sine waves, and are illustrated in any book on Chaos theory or non-linear dynamics, such as '*Universality in Chaos*' by Predrag Cvitanovic.

Tony Callegari UK

The publisher reserves the right to edit and shorten letters due to space constraints

PLEASE EMAIL YOUR LETTERS TO:
svetlana.josifovska@stjohnpatrick.com

MAKING A PROTEST

I couldn't let the article "Reduce Ear Fatigue In Power Amps" in the March 09 issue go by without making a protest. Since almost every sentence contains a statement that is either incoherent or wrong, I won't waste your time by going through it in detail, but as a sample, this is what I think of Figure 5, which claims to be a "fully simulated and tested circuit that may be fun for designers":

1) The amplifier has a bipolar input but is fed from a source impedance of not less than 4.4K, and as much as 29.4K when VR1 is set in the middle. This error alone will generate avoidable extra distortion of between 4 and 20 times that of the amplifier when it is fed from a low impedance as it should be.

2) There are two bias transistors Q18 Q22, both trying to control the output stage bias. At best, one is redundant.

3) The Zobel network R20 C8 is on the wrong side of the output inductor L4, so cannot fulfill its function. Expect HF instability with inductive loads; loudspeakers, for example.

Douglas Self UK

TRANSMISSION LINE MODEL

The letter by S. Hassell '*Watch out for that Lossy Cable*' suggests that the degradation of the wavefront might be due to current flow in the dielectric material of the cable insulation.

The existence of a circuit model which faithfully reproduces the waveform of the monitored signal cannot be ignored. This is illustrated by **Figure 1**.

In this model, the voltage source *Vgen* applies a step voltage to the transmission line. With transient analysis the current is treated as the sum of two partial currents, the incident current *Ini* and the reflected current *Inr*. The total current 'absorbed' by the termination at the near end is *Ina*, where *Ina* = *Ini* + *Inr*.

Ina is the current delivered to the line and was the current monitored by a current transformer clamped round one of the conductors of the set-up described in the letter '*Transmission Line Transients*'. The output waveform was displayed on channel 2 of the oscilloscope. Simulating the response of the model of Figure 1 to a single step pulse provided a fairly reasonable reproduction of the waveform, and this waveform was illustrated in that earlier letter.

What follows is an attempt to describe the functioning of the circuit model and relate its operation to the behaviour of the system-under-review.

Initially, there is no incident current, so the amplitude of the first step is determined by the current due to *Vgen* applied to the source impedance *R1*, a resistance representing cable losses *Rcable* and the characteristic impedance *Ro* in series. In propagating down the line, some of the current, *Ins*, radiates into the environment via the capacitor *Crad*. This means that the current actually arriving at the far end is *Int*, where *Int* = *Inr* – *Ins*.

Int appears as an incident current *Ifi* at the far end of the line after a transit time of *T* seconds. In this model *T* = *83ns*. Since the far end is open-circuit, the current is reversed in amplitude and reflected back into the line. This means that the time taken for the reflected pulse *Ifr* to appear back at the near end of the line is twice the transit time. This appears as an exponentially rising current *Ini* at the near end.

Since the load *R1* at the near end is very low compared to the characteristic impedance *Ro*, the reflected current is almost doubled in amplitude. The explains the first trailing edge of the waveform illustrated in the note '*Transmission Line Transients*'.

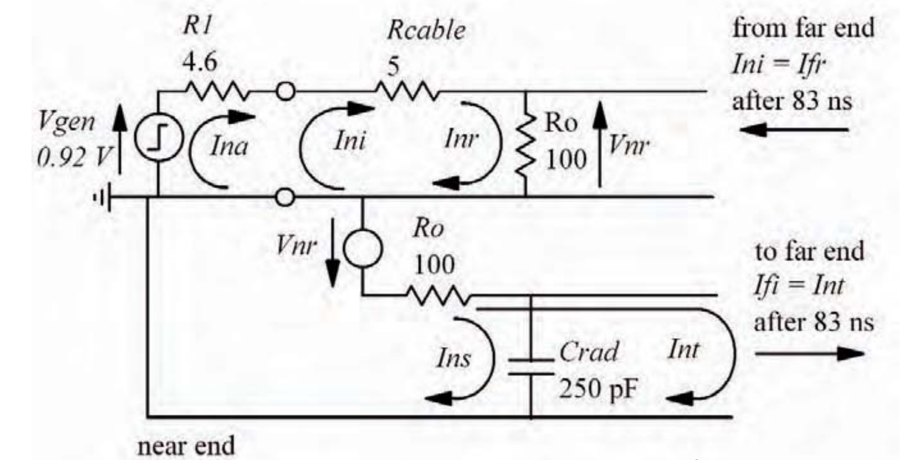


Figure1: *Transmission line model of a 15m, 2-core cable*

The significant characteristic of the model is the fact that the transmission line presents a constant impedance of 100 ohm to the source generator. This is confirmed by the fact the initial step current monitored by the current transformer is a fast rising edge, followed by a relatively constant current. The current in *Crad* is invisible to this monitoring device.

This means that the loss cannot be due to current flow in the dielectric material of the cable insulation. Any such current would be detected by the transformer and would be clearly visible in the waveform.

The fact that the current in Crad was not detected by the transformer was due to the fact that the device was used to monitor differential-mode current. Any common-mode current (in this case aerial-mode current) would not be detected. Hence, the current Ins could only be delivered to *Crad* via the signal and return conductors acting in parallel. The cable was behaving as an unintentional aerial.

The existence of aerial-mode current should not be surprising. Anyone who has investigated the EMC of systems which employ Broadband over Power Lines (BPL) will be well aware of the deleterious effect they have on the radio spectrum.

Mr Hassell questions the integrity of the instrumentation. It can be reported that the bandwidth of the current transformer is 20kHz to 20MHz. The fact that the leading edge of the waveform was clearly visible on the oscilloscope trace indicates that the response of the device was fast enough for the purpose intended.

Details of the construction of the transformer, its calibration, the test set-up, the test procedure, the circuit model, the derivation of the model and the Mathcad program used to simulate the waveform are all available on request. Just visit www.designemc.info and navigate to the Feedback page.

Ian Darney UK

"THE EXISTENCE OF AERIAL-MODE CURRENT SHOULD NOT BE SURPRISING. ANYONE WHO HAS INVESTIGATED THE EMC OF SYSTEMS WHICH EMPLOY BROADBAND OVER POWER LINES (BPL) WILL BE WELL AWARE OF THE DELETERIOUS EFFECT THEY HAVE ON THE RADIO SPECTRUM"

NO NEED FOR CONFUSION

With reference to letters in the August 2009 issue of Electronics World regarding my response to the "Catt Question", it seems that there has been some misinterpretation or misunderstanding of what I wrote.

Let me first provide the answer to Catt's anomaly, for the record. Catt asks a perfectly reasonable question, which I hope is summarised by: "Where do the electrons come from in a wire conveying a pulse". He immediately misstates the problem, however, by saying that the electromagnetic pulse travels down the wire, at the speed of light. This is not the case. The pulse travels down the wire at a rate controlled by the inductance and capacitance of the line. For a typical transmission line, this would be at around two-thirds the speed of light. Only in free space will the pulse travel at the speed of light.

The answer to Mr Catt's question is "both from the wire and the power supply". When the number of electrons in a wire are considered, Mr Catt's concerns appear to pale into insignificance. There may be something like 10^{23} electrons per cubic centimetre of copper wire, but the number of additional electrons needed to charge a moderate diameter wire in a transmission line (pair) up to, say, 240V is less than one trillionth of this number. The additional electrons needed after the pulse has passed requires those present to have "moved up" by a distance corresponding to less than 1 nanometre in one kilometre – and the average thermal velocity of electrons is sufficient to allow enough electrons to move to follow the charge. For example, the velocity they need to accommodate charging a 1km of line is only 1 nanometre per 5 microseconds, or 0.2mm/s. Overall, some additional electrons are needed because the total number has increased in accordance with the charge on the line. These will be supplied by the power supply.

Evidently, electrons are ultimately provided by the supply, or west, in Mr Catt's problem. Those scientists Mr Catt called "westerners" in the past are correct in as far as this is a partial answer. But Catt is right in a sense, because electrons further away from the supply will not have had a chance to have travelled "fast enough" if it is assumed that additional electrons throughout the wire came from the supply.

For the majority of electrons, they arose from within the wire and need only an almost infinitesimal increase in density to readjust to the new charge. Scientists who said that electrons "came from the south" – Mr Catt's "southerners" – are also correct, in part. Neither camp offers a complete explanation: electrons come from both the south and west. Mr Catt has exploited this confusion by suggesting – or at least implying – that only one or the other can be correct.

In his letter, Forrest Bishop is somewhat disingenuous in attributing a "new theory of electricity" to me. I made no such claim and I said that Maxwell's equations seem to be able to account for Catt's question. Mr Bishop's statements appear to be based on a misreading or misunderstanding of what I wrote.

Regarding a pulse travelling down a wire, Mr Bishop says that "the current in the lower wire does not start up until the initial pulse has travelled from the source to the load". In my letter, I referred to electrons in the wire as "only knowing they have to move when the pulse arrives". I suspect Mr Bishop would have realised that my reference meant only these particular electrons at the termination point of the wire.

Another of Mr Bishop's comments – that the wire is only fully charged when the reflected pulse returns – can also be true, but only if there is a reflection. But it was incorrect to ascribe a "new theory" which says that the electrons only move when the pulse returns. This is wrong. It seems necessary to set the record straight by recounting what happens in the transmission line.

Suppose we have a pulse provided by a voltage source which is applied to a transmission line and that this source is matched to the line. The pulse propagates down the transmission line, charging the conductors as it goes. Electrons will flow into the negative wire, and out of the positive wire, as the wire charges.

The wires charge to half the originating pulse voltage because of the load matching. The charging current will flow continuously into (or out of) the wires while the pulse travels along the line. If the line is terminated in a matched load, current will continue to flow after the pulse has reached the far end, because we then have a simple resistive divider, and no reflections occur. If the load is not a matched impedance, we will observe a reflection. Current continues to flow into the line while the reflection heads back to the start. As the reflected pulse returns to the origin, the wires will take on the combined potential of the incident and reflected wave.

In the case of an open circuit, the final voltage of the wire will be equal to the original voltage pulse. In this case, when the reflected pulse returns to the origin the wire will be fully charged at the initiating voltage and current into the wire will stop: the capacitance of the wire is now fully charged. If you were to measure the line potential, you will see the forward and return potentials at half the voltage and full voltage respectively as the pulse travels there and back. If there had been a short circuit at the end, the return potential would have been zero and the current would have doubled when the reflected pulse reached the origin.

Ian Darney, in his letter [August issue], concluded that the "driving signal" induced a current in the "return wire". In fact, the two have to remain in sync or we get an imbalance. The "return" current sees just as much a force pulling electrons into the positive lead of the power supply as the negative supply pushes electrons into the negative lead of the transmission line. The two occur together.

Your other readers who mention the need to maintain open debate are, of course, quite correct. The reason that there has been so much comment about Mr Catt's question seems that some people would like there to be some explanation other than standard physics to account for the apparent anomaly, but it is unfortunate that Mr Catt has made at least one incorrect assumption in stating his problem, and continued to create confusion by exploiting differences of scientific opinion where some thought would have resolved this apparent conflict.

John Ellis UK

The publisher reserves the right to edit and shorten letters due to space constraints

PLEASE EMAIL YOUR LETTERS TO: svetlana.josifovska@stjohnpatrick.com

PLC with PIC16F648A Microcontroller – Part 13

Associate Professor **Dr Murat Uzam** from Nigde University in Turkey presents a series of articles on a project that focuses on a microcontroller-based PLC. This is the thirteenth article in the series describing multiplexer macros

IN THIS ARTICLE, the following multiplexer macros are described: mux_2_1 (2×1 MUX), mux_2_1_E (2×1 MUX with Enable input), mux_4_1 (4×1 MUX), mux_4_1_E (4×1 MUX with Enable input), mux_8_1 (8×1 MUX), mux_8_1_E (8×1 MUX with Enable input). Five examples will be provided in the next article to show the applicability of these multiplexer macros.

As a standard combinational component, the multiplexer, abbreviated as MUX, allows the selection of one input signal among n signals, where n > 1 and is a power of two. Selected lines connected to the multiplexer determine which input signal is chosen and passed to the output of the multiplexer. As can be seen from **Figure 1**, in general, an n-to-1 multiplexer has n data input lines, m select lines where m = log2 n, i.e. 2m = n, and one output line. Although, not shown in Figure 1, in addition to the other inputs, the multiplexer may have an enable line, E, for enabling it. When the multiplexer is disabled with E set to 0 (for active-high enable input E), no input signal is selected and passed to the output.

The macro "mux_2_1" is shown in **Table 1**, together with its symbol and truth table. In this macro, "s0" is a Boolean input variable taken into the macro through "regs0,bits0" and it represents the select input; "d0" and "d1" are Boolean input variables taken into the macro through "regi0,biti0" and "regi1,biti1" respectively, and they represent

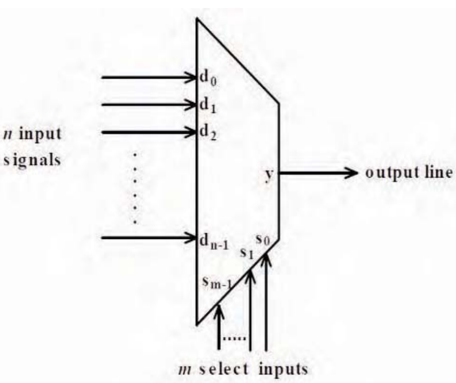
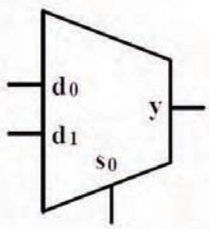


Figure 1: *The general form of an n-to-1 multiplexer, where n = 2^m*

Macro

```
;--------- macro: mux_2_1 -----------
mux_2_1  macro   regs0,bits0,regi1,biti1,regi0,biti0,rego,bito
     local   L1,L2,L3
     btfss   regs0,bits0
     goto    L3
     btfss   regi1,biti1          ;s0 = 1
     goto    L2
     bsf     rego,bito
     goto    L1
L3   btfss   regi0,biti0          ;s0 = 0
     goto    L2
     bsf     rego,bito
     goto    L1
L2   bcf     rego,bito
L1
     endm
;-----------------------------------
```

Symbol



s0 =	regs0,bits0
d0 =	regi0,biti0
d1 =	regi1,biti1
y =	rego,bito

Truth table

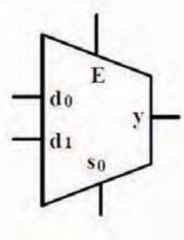
input	output
s0	y
0	d0
1	d1

Table 1: *The macro "mux_2_1" together with its symbol and truth table*

Macro

```
;--------- macro: mux_2_1_E -----------
mux_2_1_E  macro   regs0,bits0,regi1,biti1,regi0,biti0,rego,bito
     local   L1,L2,L3
     movwf   Temp_1
     btfss   Temp_1,0
     goto    L2
     btfss   regs0,bits0
     goto    L3
     btfss   regi1,biti1          ;s0 = 1
     goto    L2
     bsf     rego,bito
     goto    L1
L3   btfss   regi0,biti0          ;s0 = 0
     goto    L2
     bsf     rego,bito
     goto    L1
L2   bcf     rego,bito
L1
     endm
;-----------------------------------
```

Symbol



W	E
s0 =	regs0,bits0
d0 =	regi0,biti0
d1 =	regi1,biti1
y =	rego,bito

Truth table

inputs		output
E	s0	y
0	x	0
1	0	d0
1	1	d1

x: don't care

Table 2: *The macro "mux_2_1_E" together with its symbol and truth table*

two input signals. Finally, "y" is a Boolean output variable produced as an output through "rego,bito" and it represents the output signal.

In this MUX, when s0 = 0, the input signal "d0" is selected and passed to the output "y". When s0 = 1, the input signal "d1" is selected and passed to the output "y".

The macro "mux_2_1_E" is shown in **Table 2**, together with its symbol and truth table. In addition to the "mux_2_1", this multiplexer macro has an active-high enable line, E, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this multiplexer is disabled with E set to 0, no input signal is selected and passed to the output "y". When this multiplexer is enabled with E set to 1, it functions as described for "mux_2_1".

The macro "mux_4_1" is shown in **Table 3**, together with its symbol and truth table. In this macro, "s1" and "s0" are Boolean input variables taken into the macro through "regs1,bits1" and "regs0,bits0" respectively and they represent the chosen inputs. "d_0", "d_1", "d_2" and "d_3" are Boolean input variables taken into the macro through "regi0,biti0", "regi1,biti1", "regi2,biti2" and "regi3,biti3", and they represent four input signals. Finally, "y" is a Boolean output variable produced as an output through "rego,bito" and it represents the output signal. In this MUX, when s1s0 = 00, (respectively, 01, 10, 11) the input signal "d_0" (respectively, d_1, d_2, d_3) is selected and passed to the output "y".

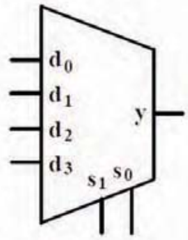
The macro "mux_4_1_E" is shown in **Table 4**, together with its symbol and the truth table. In addition to the "mux_4_1", this multiplexer macro has an active-high enable line, E, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this multiplexer is disabled with E set to 0, no input signal is selected and passed to the output. When this multiplexer is enabled with E set to 1, it functions as described for "mux_4_1".

The macro "mux_8_1" is shown in **Table 5**, together with its symbol and truth table. In

Macro

```
;--------- macro: mux_4_1 -----------
mux_4_1  macro   regs1,bits1,regs0,bits0,regi3,biti3,
regi2,biti2,regi1,biti1,regi0,biti0,rego,bito
        local   L1,L2,L3,L4,L5
        btfss   regs1,bits1
        goto    L4
        btfss   regs0,bits0
        goto    L5
        btfss   regi3,biti3             ;s1s0 = 11
        goto    L2
        bsf     rego,bito
        goto    L1
L5      btfss   regi2,biti2             ;s1s0 = 10
        goto    L2
        bsf     rego,bito
        goto    L1
L4      btfss   regs0,bits0
        goto    L3
        btfss   regi1,biti1             ;s1s0 = 01
        goto    L2
        bsf     rego,bito
        goto    L1
L3      btfss   regi0,biti0             ;s1s0 = 00
        goto    L2
        bsf     rego,bito
        goto    L1
L2      bcf     rego,bito
L1
        endm
;-----------------------------------
```

Symbol



s1 =	regs1,bits1
s0 =	regs0,bits0
d3 =	regi3,biti3
d2 =	regi2,biti2
d1 =	regi1,biti1
d0 =	regi0,biti0
y =	rego,bito

Truth table

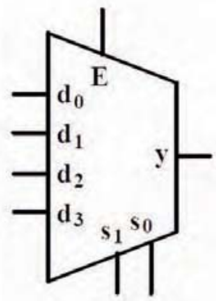
inputs		output
s1	s0	y
0	0	d0
0	1	d1
1	0	d2
1	1	d3

***Table 3:** The macro "mux_4_1" together with its symbol and truth table*

Macro

```
;--------- macro: mux_4_1_E -----------
mux_4_1_E  macro   regs1,bits1,regs0,bits0,regi3,biti3,
regi2,biti2,regi1,biti1,regi0,biti0,rego,bito
        local   L1,L2,L3,L4,L5
        movwf   Temp_1
        btfss   Temp_1,0
        goto    L2
        btfss   regs1,bits1
        goto    L4
        btfss   regs0,bits0
        goto    L5
        btfss   regi3,biti3             ;s1s0 = 11
        goto    L2
        bsf     rego,bito
        goto    L1
L5      btfss   regi2,biti2             ;s1s0 = 10
        goto    L2
        bsf     rego,bito
        goto    L1
L4      btfss   regs0,bits0
        goto    L3
        btfss   regi1,biti1             ;s1s0 = 01
        goto    L2
        bsf     rego,bito
        goto    L1
L3      btfss   regi0,biti0             ;s1s0 = 00
        goto    L2
        bsf     rego,bito
        goto    L1
L2      bcf     rego,bito
L1
        endm
;-----------------------------------
```

Symbol



W	E
s1 =	regs1,bits1
s0 =	regs0,bits0
d3 =	regi3,biti3
d2 =	regi2,biti2
d1 =	regi1,biti1
d0 =	regi0,biti0
y =	rego,bito

Truth table

inputs			output
E	s1	s0	y
0	x	x	0
1	0	0	d0
1	0	1	d1
1	1	0	d2
1	1	1	d3

x: don't care

***Table 4:** The macro "mux_4_1_E" together with its symbol and truth table*

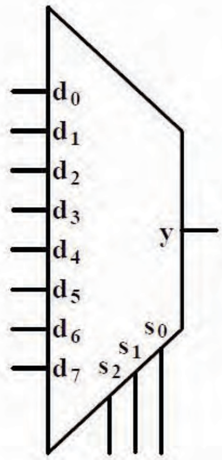
this macro, "s2", "s1" and "s0" are Boolean input variables taken into the macro through "regs2,bits2", "regs1,bits1" and "regs0,bits0" respectively and they represent the select inputs. "d_0", "d_1", "d_2", "d_3", "d_4", "d_5", "d_6" and "d_7"are Boolean input variables taken into the macro through "regi0,biti0", "regi1,biti1", "regi2,biti2", "regi3,biti3", "regi4,biti4", "regi5,biti5", "regi6,biti6" and "regi7,biti7" respectively, and they represent eight input signals. Finally, "y" is a Boolean output variable produced as an output through "rego,bito" and it represents the output signal. In this MUX, when s2s1s0 = 000, (respectively, 001, 010, 011, 100, 101, 110, 111) the input signal "d0" (respectively, d_1, d_2, d_3, d_4, d_5, d_6, d_7) is selected and passed to the output "y".

The macro "mux_8_1_E" is shown in **Table 6**, together with its symbol and the truth table. In addition to the "mux_8_1", this multiplexer macro has an active-high enable line, E, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this multiplexer is disabled with E set to 0, no input signal is selected and passed to the output. When this multiplexer is enabled with E set to 1, it functions as described for "mux_8_1".

The file "mux_mcr_def.inc" including the 6 multiplexer macros shown in Tables 1, 2…6 can be downloaded from **http://host.nigde.edu.tr/muzam/**.

Macro | Symbol | Truth table

```
mux_8_1  macro   regs2,bits2,regs1,bits1,regs0,bits0,regi7,biti7,
regi6,biti6, regi5,biti5,regi4,biti4,regi3,biti3,regi2,biti2,
regi1,biti1, regi0,biti0,rego,bito
      local   L1,L2,L3,L4,L5,L6,L7,L8,L9
      btfss   regs2,bits2
      goto    L6
      btfss   regs1,bits1
      goto    L8
      btfss   regs0,bits0
      goto    L9
      btfss   regi7,biti7           ;s2s1s0 = 111
      goto    L2
      bsf     rego,bito
      goto    L1
L9    btfss   regi6,biti6           ;s2s1s0 = 110
      goto    L2
      bsf     rego,bito
      goto    L1
L8    btfss   regs0,bits0
      goto    L7
      btfss   regi5,biti5           ;s2s1s0 = 101
      goto    L2
      bsf     rego,bito
      goto    L1
L7    btfss   regi4,biti4           ;s2s1s0 = 100
      goto    L2
      bsf     rego,bito
      goto    L1
L6    btfss   regs1,bits1
      goto    L4
      btfss   regs0,bits0
      goto    L5
      btfss   regi3,biti3           ;s2s1s0 = 011
      goto    L2
      bsf     rego,bito
      goto    L1
L5    btfss   regi2,biti2           ;s2s1s0 = 010
      goto    L2
      bsf     rego,bito
      goto    L1
L4    btfss   regs0,bits0
      goto    L3
      btfss   regi1,biti1           ;s2s1s0 = 001
      goto    L2
      bsf     rego,bito
      goto    L1
L3    btfss   regi0,biti0           ;s2s1s0 = 000
      goto    L2
      bsf     rego,bito
      goto    L1
L2    bcf     rego,bito
L1
      endm
;-----------------------------------
```



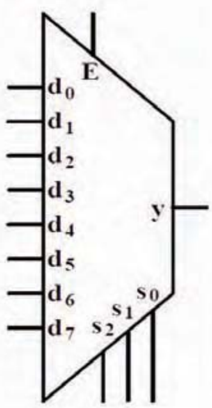
s2 =	regs2,bits2
s1 =	regs1,bits1
s0 =	regs0,bits0
d7 =	regi7,biti7
d6 =	regi6,biti6
d5 =	regi5,biti5
d4 =	regi4,biti4
d3 =	regi3,biti3
d2 =	regi2,biti2
d1 =	regi1,biti1
d0 =	regi0,biti0
y =	rego,bito

inputs			output
s2	s1	s0	y
0	0	0	d0
0	0	1	d1
0	1	0	d2
0	1	1	d3
1	0	0	d4
1	0	1	d5
1	0	0	d6
1	1	1	d7

Table 5: *The macro "mux_8_1" together with its symbol and truth table*

Macro | Symbol | Truth table

```
mux_8_1_E  macro   regs2,bits2,regs1,bits1,regs0,bits0,regi7,biti7,
regi6,biti6,regi5,biti5,regi4,biti4,regi3,biti3,regi2,biti2,regi1,
biti1,regi0,biti0,rego,bito
      local   L1,L2,L3,L4,L5,L6,L7,L8,L9
      movwf   Temp_1
      btfss   Temp_1.0
      goto    L2
      btfss   regs2,bits2
      goto    L6
      btfss   regs1,bits1
      goto    L8
      btfss   regs0,bits0
      goto    L9
      btfss   regi7,biti7           ;s2s1s0 = 111
      goto    L2
      bsf     rego,bito
      goto    L1
L9    btfss   regi6,biti6           ;s2s1s0 = 110
      goto    L2
      bsf     rego,bito
      goto    L1
L8    btfss   regs0,bits0
      goto    L7
      btfss   regi5,biti5           ;s2s1s0 = 101
      goto    L2
      bsf     rego,bito
      goto    L1
L7    btfss   regi4,biti4           ;s2s1s0 = 100
      goto    L2
      bsf     rego,bito
      goto    L1
L6    btfss   regs1,bits1
      goto    L4
      btfss   regs0,bits0
      goto    L5
      btfss   regi3,biti3           ;s2s1s0 = 011
      goto    L2
      bsf     rego,bito
      goto    L1
L5    btfss   regi2,biti2           ;s2s1s0 = 010
      goto    L2
      bsf     rego,bito
      goto    L1
L4    btfss   regs0,bits0
      goto    L3
      btfss   regi1,biti1           ;s2s1s0 = 001
      goto    L2
      bsf     rego,bito
      goto    L1
L3    btfss   regi0,biti0           ;s2s1s0 = 000
      goto    L2
      bsf     rego,bito
      goto    L1
L2    bcf     rego,bito
L1
      endm
;-----------------------------------
```



W	E
s2 =	regs2,bits2
s1 =	regs1,bits1
s0 =	regs0,bits0
d7 =	regi7,biti7
d6 =	regi6,biti6
d5 =	regi5,biti5
d4 =	regi4,biti4
d3 =	regi3,biti3
d2 =	regi2,biti2
d1 =	regi1,biti1
d0 =	regi0,biti0
y =	rego,bito

inputs				output
E	s2	s1	s0	y
0	x	x	x	0
1	0	0	0	d0
1	0	0	1	d1
1	0	1	0	d2
1	0	1	1	d3
1	1	0	0	d4
1	1	0	1	d5
1	1	0	0	d6
1	1	1	1	d7

x : don't care

Table 6: *The macro "mux_8_1_E" together with its symbol and truth table*

If you've missed any of the previous articles in this series, you can now order it on line at ***www.electronicsworld.co.uk***

ONE OA AND ONE NIC-BASED GROUNDED INDUCTANCE SIMULATORS

OPERATIONAL AMPLIFIERS (OAs) are used as active elements in many areas such as inductor simulators, adders, integrators, differentiators, filters, oscillator, amplifiers, analogue-to-digital converters, digital-to-analogue converters and so on. An OA whose symbol is shown in **Figure 1** has two input terminals, two DC power supply terminals and one output terminal. An OA has the following input and output relationship:

$$V_{out} = A_0 \left(V_{inp1} - V_{inp2}\right) \qquad \textbf{(1)}$$

where A_0 is frequency-dependent, open loop, voltage gain. Also, V_{out} as an output voltage is a function of V_{inp1} applied to non-inverting terminal and V_{inp2} applied to inverting terminal of the OA in Figure 1.

There are basically two kinds of negative impedance convertors (NICs), also known as current inversion type NIC and voltage inversion type NIC. Further, using standard notation for an ideal NIC, its symbol depicted in **Figure 2**, can be defined by the following matrix equation:

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \pm 1 & 0 \\ 0 & \pm 1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_1 \end{bmatrix} \qquad \textbf{(2)}$$

In **Equation 2**, the plus and minus signs correspond to the current inversion type and voltage inversion type NICs.

Grounded Inductance Simulators

The circuit shown in **Figure 3** is a well-known active RC network, lossy inductor simulator of A. J. Prescott's. The impedance of this RC network function can be given as

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_1R_2 + R_1 + R_2 \qquad \textbf{(3)}$$

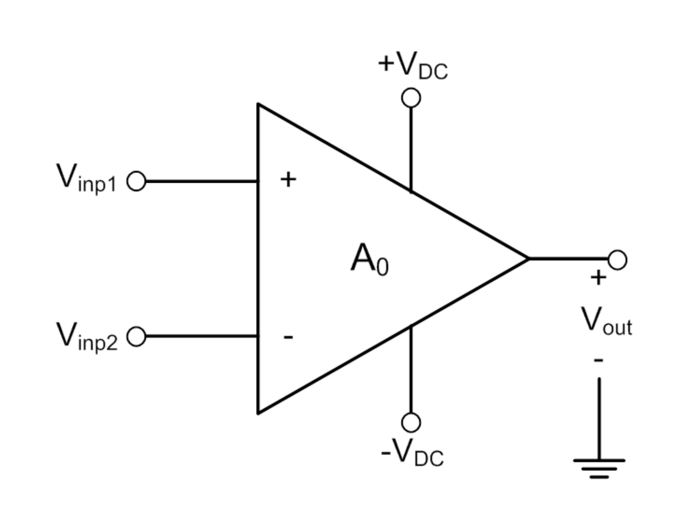


Figure 1: *Op-amp symbol*

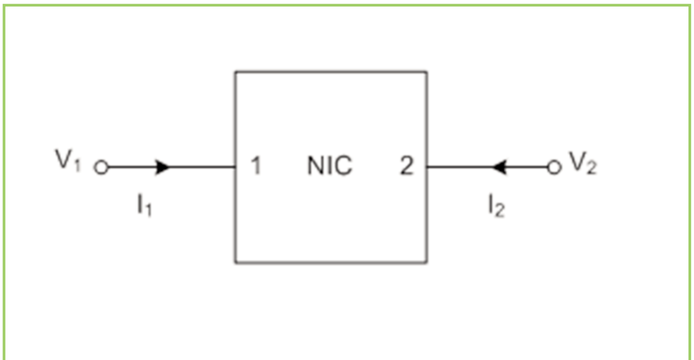


Figure 2: *NIC symbol*

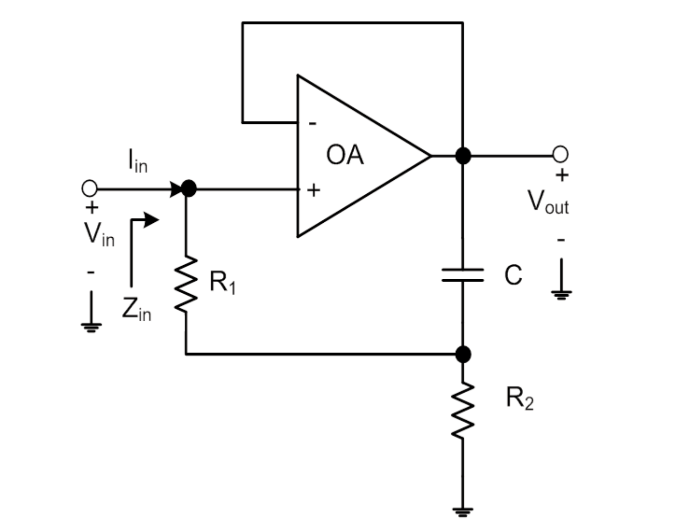


Figure 3: *Inductor simulator of A. J. Prescott's*

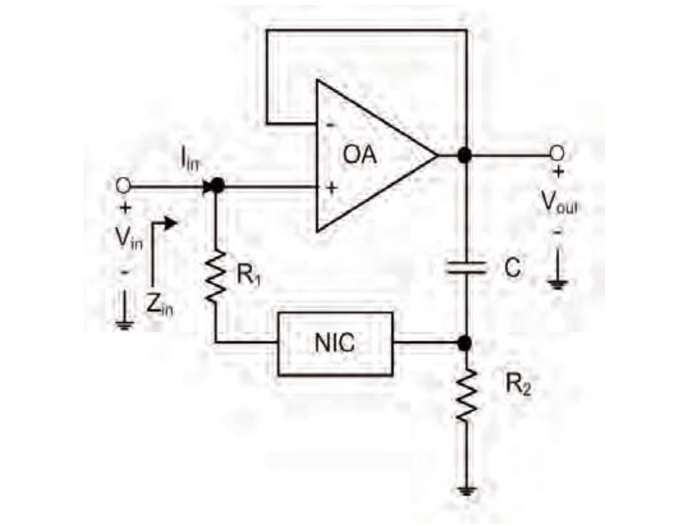


Figure 4: *Proposed circuit derived from the circuit of A. J. Prescott's*

The topology of **Figure 4** derived from one in Figure 3 can be expressed by the following impedance:

$$Z_{in} = \frac{V_{in}}{I_{in}} = R_1 - R_2 + sCR_1R_2 \qquad (4)$$

In **Equation 4**, if $R_1 = R_2 = R$ is chose, the impedance converts to:

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR^2 \qquad (5)$$

As it is seen from **Equation 3**, the circuit of A. J. Prescott is a lossy inductor whereas the proposed circuit, as seen in Figure 4, can be performed as a lossless inductor by adding an extra NIC.

In order to achieve simulations, the values of capacitor and resistors are chosen as follows:

$$C = 50\text{pF}, \qquad R_1 = 1.3\text{k}\Omega,\ R_2 = 1.3\text{k}\Omega$$

The simulation results are shown in **Figure 5**.

Likewise, the circuit in **Figure 6** is one of the well-known RC active circuits, lossy inductor simulator of R. L. Ford and F. E. J. Girling's, which impedance can expressed as:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sCR_1R_2}{1 + sC(R_1 + R_2)} \qquad (6)$$

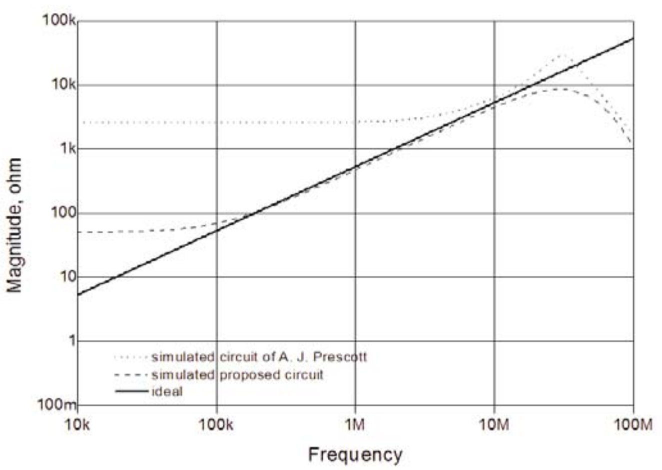


***Figure 5:** Magnitudes of an ideal inductor and the inductances of Figures 3 and 4*

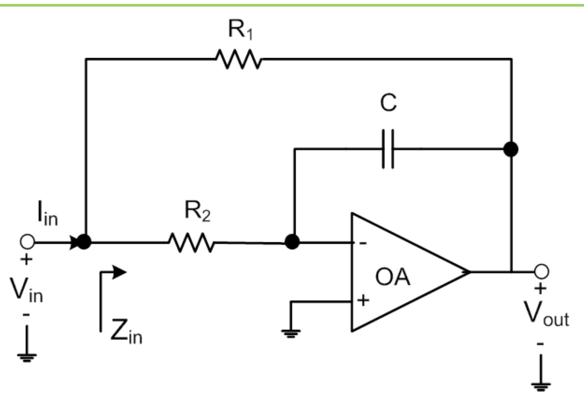


***Figure 6:** Inductor simulator of R. L. Ford and F. E. J. Girling's*

The proposed inductor simulator depicted in **Figure 7**, derived from one in Figure 6, can be defined by the following impedance:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sCR_1R_2}{1 + sC(R_2 - R_1)} \qquad (7)$$

Similarly, if $R_1 = R_2 = R$ is selected, the impedance in **Equation 7** can be expressed by **Equation 5**.

To accomplish simulations, the values of capacitor and resistors are selected as:

$$C = 100\text{pF}, \qquad R_1 = 1\text{k}\Omega,\ R_2 = 1\text{k}\Omega$$

The simulation results are demonstrated in **Figure 8**.

In conclusion, simulation results shown in Figures 5 and 8 verify the theory as expected.

Halil Alpaslan and **Erkan Yuce**
Pamukkale University Electrical and Electronics Engineering, Turkey

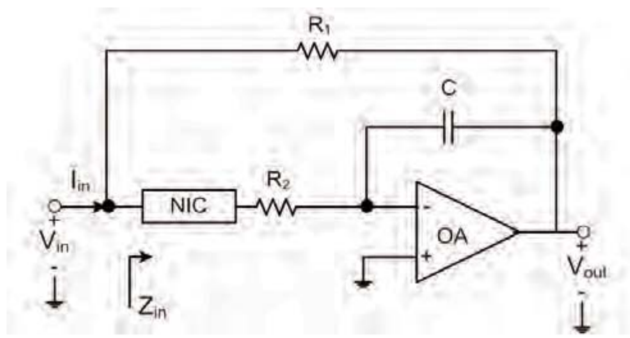


***Figure 7:** Proposed circuit for the one by R. L. Ford and F. E. J. Girlinguc*

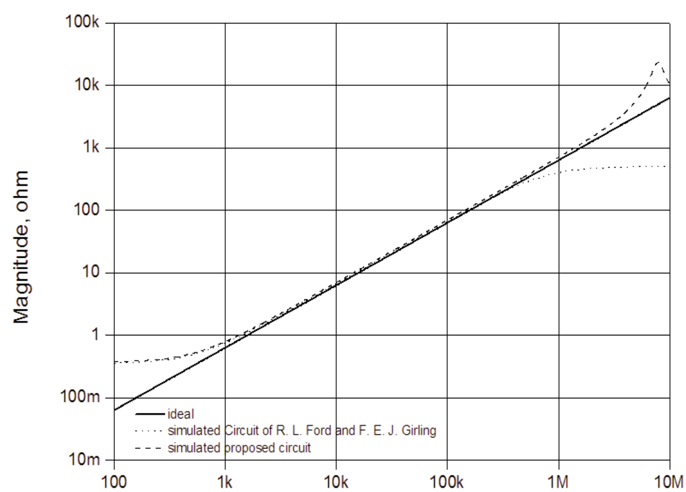


***Figure 8:** The magnitudes of an ideal inductor and the inductances in Figures 6 and 7*

RF VECTOR SIGNAL GENERATOR PROVIDES BEST COMBINATION OF HIGH THROUGHPUT AND LOW PHASE NOISE

Keithley Instruments, a supplier in advanced electrical test instruments and systems, has upgraded its popular RF Vector Signal Generator line for RF engineers with new capabilities that reduce signal generation times and enhance signal quality.

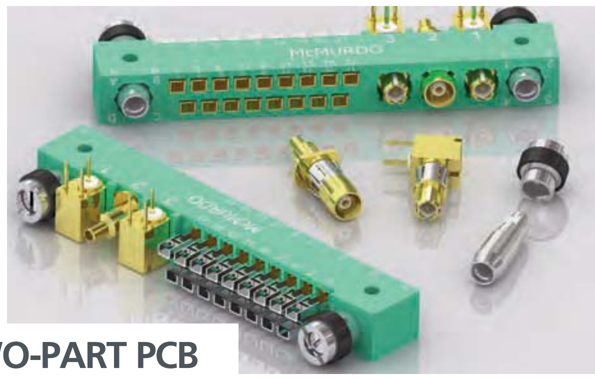
Patent-pending technology allows the Model 2920A RF Vector Signal Generator to support both frequency and amplitude switching rates that are significantly faster than before.

The Model 2920A, which provides signal generation bandwidth options up to 80MHz with a frequency range of either 10MHz-4GHz or 10MHz-6GHz, builds on the capabilities of Keithley's Series 2900 signal generator line. It expands the Series 2900 line's applications for testing wireless devices to today's high throughput, complex modulation and wide bandwidth wireless telecom standards, including LTE, GSM/EDGE, cdmaOne, cdma2000, W-CDMA, HSPA, HSPA+, LTE, WLAN, WiMAX, WiBro, TD-SCDMA, DVB (Digital Video Broadcast) and GPS (Global Positioning System).

The Model 2920A is optimized for calibrating and testing components such as amplifiers, filters and wireless receivers thoroughly over their full range of performance at exceptional speed.

Users have the flexibility to create waveform files offline and download them into the Model 2920A's arbitrary waveform memory using a USB memory stick or the GPIB or LAN interfaces. This transfer flexibility will be useful for those who prefer to employ third-party tools to create signal files, such as The MathWorks's MATLAB interactive programming environment.

www.keithley.com



TWO-PART PCB CONNECTOR SYSTEM MEETS LATEST MILITARY AND AEROSPACE STANDARDS

A two-part PCB connector system from Lane Electronics has been designed to meet the latest UK and international standards for use primarily in mil/aerospace applications. These range from fast jet to gun turret, where high resistance to vibration and extreme reliability are critical. Other applications would be high-end engineering where constant exposure to vibration could be an issue that has caused other two-part connectors to fail.

Produced by ITW McMurdo, for whom Lane Electronics is a franchised assembling distributor, the 801 and 801CX Series utilizes a 1.27mm (0.05in) staggered pitch with 2.54mm (0.1in) between rows and can be supplied on short lead times in a variety of contact configurations.

Key features of the 801 Series include low and high frequency contacts, low and high power contacts and 19 body sizes up to 96 way. Terminations include solder, PC, straight, 90 degrees, crimp and wire wrapping depending on the type of contact used. Polarizing facilities are available and all contacts are removable.

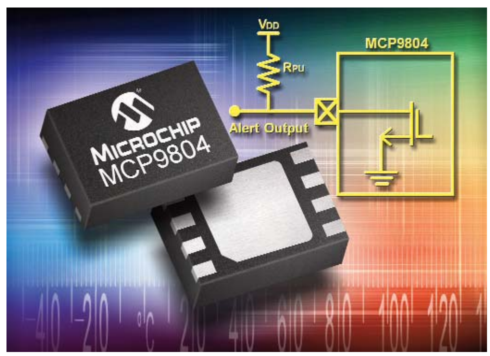
The 801 Series is approved to BS9525 N0001 and was originally designed to meet the requirements of BS9525 F0006, F00012, F0027, F0041 and MIL-C-55302/140-155.

Lane Electronics also supplies other key connector types including circular, filtered, RF, coaxial, sub – miniature, backshells and adaptors, D connectors, aerospace, test and measurement, IDC, PCB connectors, edge connectors and connectors for rack and panel applications.

www.fclane.com

MICROCHIP ANNOUNCES HIGH-ACCURACY, LOW-POWER TEMPERATURE SENSOR

Microchip has announced the MCP9804 Temperature Sensor. The sensor provides high temperature accuracy of +0.25°C (typical) and ±1°C from -40 to +125°C, as well as static current consumption of just 200µA (typ). Available in small 8-pin MSOP and 2mm x 3mm DFN packages, the I2C device reduces board space and enables longer battery life for industrial, automotive and consumer applications.



Many temperature-sensing designs require the use of several external components, making them large, complex and expensive. Silicon-based temperature sensors are becoming more popular because they do not require external components and can be used with little to no design experience. In addition to low power and high accuracy, the MCP9804 sensor features programmable shutdown to extend battery life; an alert feature for over- and under-temperature window monitoring; and a critical temperature-alert feature that provides over-temperature protection, helping to further lengthen system life.

The MCP9804 temperature sensor represents a significant expansion of Microchip's temperature-sensor family, giving designers a tremendous amount of flexibility to design smaller, higher-performing temperature sensing systems at lower costs.

Example applications for the MCP9804 temperature sensor include industrial freezers that require high accuracy at lower temperatures such as -20°C to +45°C; consumer electronic devices that require high accuracy at +85°C, such as personal computers; and automotive applications that demand high accuracy at temperatures up to +125°C, such as engine temperature monitoring.

www.microchip.com

CERTIFIED FOR USE DOWN UNDER

All of Monitran's Group I intrinsically safe accelerometers and velocity transducers have been approved by certification body Simtars to ANZEx for use in mining applications throughout Australia and New Zealand. This certification is in addition to the (EU) ATEX and (International) IECEx approvals Monitran's Group I sensors already possess.

Eight products have been certified to ANZEx. Of these, four are from the MTN/1100 family of general purpose accelerometers with isolated AC outputs, which are ideal for vibration analysis. Included within the family, and certified to ANZEx, are the MTN/M1100I and MTN/M1100IC, which are top-entry devices with integral cables and connectors respectively. Both have a temperature range of -55 to 140ºC and are sealed to IP67. Also included are the side-entry equivalent devices, the MTN/M1100IS and MTN/M1100ISC.

Two ANZEx-certified sensors come from Monitran's MTN/1185 family of general purpose accelerometers with DC outputs, which are ideal for machine protection. These are the MTN/M1185IC and its waterproof variant, the MTN/M1185IWC, which are both top-entry devices with integral cables and which have an operating temperature range of -25 to 90ºC.

The remaining two sensors come from Monitran's MTN/1187 family. Again, the sensors have DC outputs but this time proportional to RMS acceleration. The ANZEx-certified devices are the MTN/M1187IC and its waterproof variant the MTN/M1187IWC.

www.monitran.com

DIN 41612 CONNECTORS OFFER HIGHER CONTACT DENSITY

Harting has expanded its range of DIN 41612 connectors with the addition of two versions which offer increased contact density for use with small printed circuit boards.

The new types 3B and 3C offer 20 or 30 contacts in a compact 2.54mm grid.

Each contact can be loaded with currents of up to 2A, and the connectors are tested to the IEC 60 603-2 standard.

The male and female connectors are available both with and without a flange, enabling further space reductions. The connectors are available in solder, surface-mount compatible (SMC) or press-in technology.

The high-temperature material versions (SMC) are particularly suited for reflow soldering processing. In addition, the new connectors offer the same robust qualities as Harting's larger DIN41612 connectors in the full and half sizes. Harting is offering both the standard versions and customer-specific loadings of the DIN 41612 types 3B and 3C.

The Harting Group develops, manufactures and distributes electrical and electronic connectors, network components, pre-assembled system cables, and backplane assemblies. These products are capable of withstanding the harshest demands in industrial environments and provide high data rates for electronic applications.

www.Harting.com

TYCO ELECTRONICS EXPANDS ESD PROTECTION PORTFOLIO WITH 0201 PACKAGE

Tyco Electronics announced today the addition of three new devices to its line of electrostatic discharge (ESD) protection portfolio. The 0201-sized Silicon ESD (SESD) devices are approximately 70% smaller than prior generation 0402-sized devices, and help provide protection and improve reliability of portable electronics such as mobile phones, MP3 players, PDAs and digital cameras.

The SESD device's miniature footprint, which measures 0.6mm x 0.3mm x 0.3mm, offers flexibility in space-constrained applications. Bi-directional operation allows placement on the PCB without orientation constraint and won't clip signals that swing below ground. Designed to withstand IEC61000-4-2 ESD test pulses, the SESD device helps protect sensitive integrated circuits (ICs).

Tyco Electronics's initial offerings in the 0201 chip scale package (CSP) include the SESD0201C-006-058 and the SESD0201C-120-058. The SESD0201C-006-058 is a bi-directional and ultra-low capacitance 0.6 picofarad (pF) device that is suitable for protecting very-high-speed data lines, such as USB and HDMI, or low-voltage antenna ports. The device's ultra-low capacitance, low insertion loss (< 0.5dB up to 3GHz) and high linearity of voltage vs frequency helps minimise signal degradation.

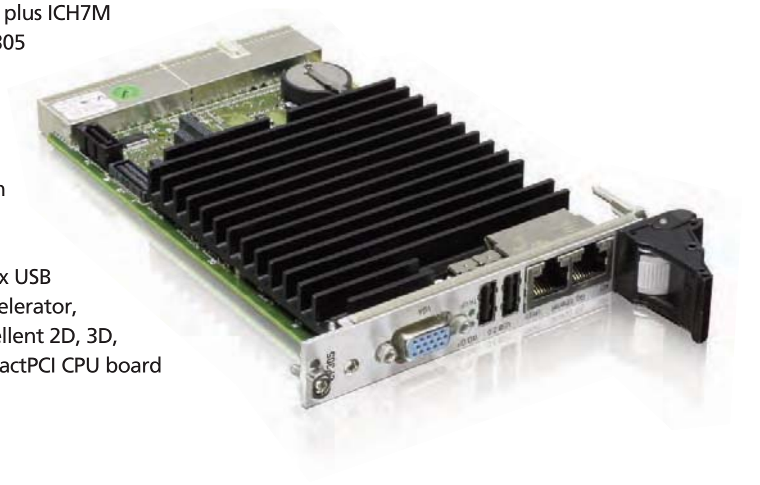
The SESD0201C-120-058 is a higher capacitance (12pF) device that can be used for low-speed generic interfaces such as keypads, power buttons, speakers and microphone ports in portable electronics. Both SESD0201C-006-058 and SESD0201C-012-058 devices offer 8kV contact and 15kV air discharge protection per the IEC61000-4-2 standard.

www.tycoelectronics.com

KONTRON BRINGS INTEL ATOM RECORD-BREAKING PERFORMANCE INTO COMPACTPCI SYSTEMS

Kontron is bringing record-breaking performance per watt to 3U CompactPCI systems with the launch of the longtime available processor board Kontron CP305 with Intel Atom processor. The rugged Kontron CP305 features EN50155 compliant reliability and extremely low TDP (Thermal Design Power), soldered processor, chipset and RAM for harsh environments.

Equipped with the 1.6GHz Intel Atom processor N270, Intel 945GSE plus ICH7M chipset and up to 2GByte of soldered DDR2 memory, the Kontron CP305 has a typical power consumption of only 10 Watt. This is less than half compared to earlier generations with identical performance. Designed for reliable operation in a temperature range from 0 to 60°C for convection cooled environments, the new CompactPCI board powers energy critical and in-vehicle mobile embedded applications in the transportation, automation, energy, military and aerospace markets.



The latest CompactPCI CPU-board offers: 2 x Gbit Ethernet, up to 6 x USB 2.0, two SATA interfaces and a CompactFlash socket. The graphics accelerator, integrated into the Mobile Intel 945GSE Express chipset, provides excellent 2D, 3D, and video features for the VGA connector on the front. The 3U CompactPCI CPU board is available as single slot (4HP) or dual slot (8HP).

www.kontron.com

KEEPING THINGS SIMPLE – ONE FOR ALL

The HMP series offers four programmable high-performance power supplies: two in the 200W class, two in the 400W class. The 200W class instruments are available with two or three channels, the 400W class instruments with three or four channels. The output specifications cover the ranges from 0 to 32V and 0 to 10A. New functionalities, a high set- and read-back resolution, the EasyArb feature and excellent noise/ripple values (150µVrms) characterize the family of power supplies.

Hameg has set great value on the logically combinable electronic fuses (FuseLink), as well as on a convenient tracking function.

The high read-back resolution, down to 1mV/0.1mA, meets even the most stringent requirements. Moreover, applying the EasyArb function, users can form arbitrary voltage/current shapes for each channel.

The HMP series is provided with a LCD display, a dual serial interface (USB/RS-232) (optionally Ethernet/USB or GPIB) and additional terminals for all channels on the rear panel.

The instruments are available immediately at list prices starting from 959 €.

www.hameg.com

FANLESS COMPACTPCI RAID SERVER

The new rugged CompactPCI RAID server, Kontron CP-ASM3-RAID, combines CompactPCI technology with high-speed SATA connections via the backplane, for the first time.

The modular Kontron CP-ASM3-RAID boasts a high-speed RAID array comprising up to 8 SATA-II hard disks (SATA 3.0 Gbit/s) or Solid State Drives, and excels with high availability and high shock and vibration resistance. Thanks to the use of electronic components with protective coating, the fanless system design is securely protected against humidity and dust. Even when using standard hard disks it achieves an impressively long lifecycle in operating temperatures of 0°C to 55°C.

At the heart of the modular Kontron CP-ASM3-RAID is an integrated, high performance, RAID controller. It supports RAID 0/1/5/10/50 or JBOD (Just a Bunch Of Disks) and a wide range of management and recovery mechanisms and guarantees data integrity and security. The hard disks or Solid State Drives are integrated on hot-swappable carrier boards and offer a storage capacity of up to several terabytes, depending on the desired configuration.

The Kontron CP307 CompactPCI processor board serves as a system controller with passively cooled 1.06GHz Intel Celeron M processor and 512MB of soldered RAM, which enable optimal performance with minimal energy consumption of the RAID system.

www.kontron.com

LG ELECTRONICS HAS INTRA EUROPEAN DISTRIBUTION WITH PANTOS

Pantos Benelux Logistics BV has signed an Intra Europe Distribution Service contract with LG Electronics in the Netherlands in August, 2009.

Pantos will provide managed courier and inland trucking services for LG Electronics service parts across Europe. The monthly volume will be in the region of 22,000 transactions. Pantos secured the contract with LG Electronics by working with the firm to identify opportunities to reduce cost and lead times. This will be achieved through improving diversification of shipping methods to encompass a multi-modal solution and providing automation processes through systems interfaces, which will also provide improved visibility.

The E-Speed System which was implemented by Pantos Benelux for this contract provides LG Electronics with a real time cargo tracking service through web based technology, as well as sending pre-alert messages to the cargo recipients.

HQ Park, President of Pantos Logistics Europe said: “This is an excellent development for Pantos as we continue to work with our key customers to identify areas within their supply chain and logistics operations where genuine value can be created. It’s a win/win situation for both parties. We firmly believe that this exciting development will enable us to develop this core service further with a number of other customers over the coming months”.

For further details, contact Mark Talbot on 01753-610-420 or email: mark.talbot@pantosuk.com

ROSENKRANZ-ELEKTRONIK GMBH CONTINUES ITS EXPANSION COURSE

Rosenkranz-Elektronik GmbH, one of the largest suppliers of used Electronic Test and Measurement (T&M) equipment in Europe has expanded its expertise by opening its own auction house, called RKE Auctions, for industrial auctions, as well as purchasing complete insolvent companies and assets in the electronic industry.

Rosenkranz-Elektronik GmbH, founded in 1951 with its head office in Darmstadt, Germany, owns one of the most extensive European inventories with over 10,000 T&M equipment pieces in stock.

The company says that RKE Auctions offers “fair and guaranteed negotiated prices” for pick-and-place machines, climatic and temperature chambers, microscopes and other equipment against immediate payment; it says it offers “a real alternative to the usual industrial auctioneers that generally work as agents for the seller with unknown sales revenues”.

For further information email Axel.Rosenkranz@rosenkranz-elektronik.com