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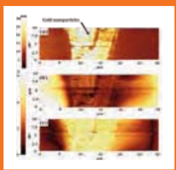
ELECTRONICS WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

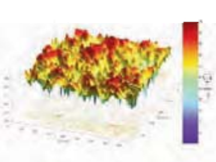
SPECIAL REPORT
T&M:
- 5-MINUTE GUIDE TO CHIP-LEVEL AUDIO TEST
- TESTING RDS-EQUIPPED FM RADIO RECEIVERS

MORAL HIGH GROUND

POWER FACTOR KEY TO AVOIDING HEADACHES



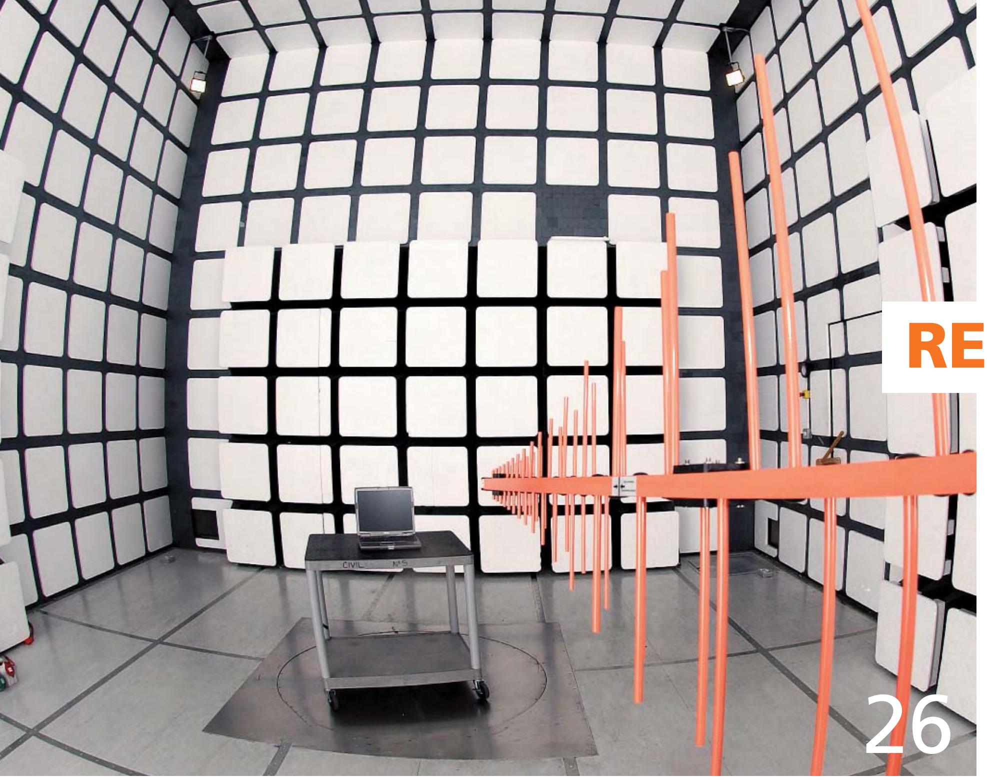
TECHNOLOGY
PAPER WITH MEMORY GIVEN BOOST



GSM
PROPAGATION STUDY OF GSM DIMENSIONS INDOORS – PART 2

PRODUCTS
MEASUREMENT SUITES, DRIVER ICS,CONNECTORS AND MUCH MORE

ALSO IN THIS ISSUE: ANALYST COLUMN • ON THE BUG HUNT • DESIGN



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ALD: FROM STRENGTH TO STRENGTH IN THE UK?

BY DR ALEC READER

What this piece states is that despite the strengths of the UK in the field of Atomic Layer Deposition (ALD),

there are definite areas that need improvement for it to become a clear leader.

ALD processes allow for the creation of easy building structures measuring 100 nanometres and smaller, for use in advanced applications of electronics, catalysis and sensors. And it is the general consensus of many professionals in the industry that the UK could be a leader in the implementation of ALD if the gaps in the basic infrastructure, already present in the UK, be identified and filled.

However, there seems to be lack of communication between all facets of the industry; albeit all working in the same area and on very closely related topics. Furthermore, it is apparent that these industry practitioners are not aware of how the opportunity to collaborate could identify and bridge the gaps they are struggling to fill.

ALD is currently being used in a number of developing markets, including nano-electronics to deposit high-k gate oxides, high-k memory capacitor dielectrics, ferroelectrics and metals and nitrides for electrodes and interconnects. The need to control extremely thin films is essential in high-k gate oxides.

Fuel cells and the highly conformal coatings used in the production of micro-fluidic and Nano Electronic Mechanical Systems (NEMS) also require the flexible and precise thickness control processes offered by ALD, to produce wear resistant, anti-stiction and chemical resistant coatings.

With the introduction of a low-temperature plasma step in the ALD reaction cycle, it is possible to deliver additional reactivity to the surface in the form of plasma-produced species. This allows ALD to be used in an even wider range of applications by improving the film quality, particularly at lower temperatures, and it also increases the number of materials that can be deposited.

Producing efficient devices is a continual challenge to the electronics market and ALD has been recognised as a vital innovation in doing this, as it is a self-limiting service that offers the benefit of giving precise thickness control. As mainstream semiconductor and other nano-electronic applications start to require a reduced dielectric layer thickness, ALD is becoming more frequently used and ever more critical.

Using remote plasma ALD means damages can be kept to a minimum, as well as the end result being higher quality films as a result of improved removal of impurities that lead to lower resistivity and higher density. Plasma ALD processes also offer the widest choice of precursor chemistry available and higher quality films with more process control.

It is apparent that the UK's main strength is its expertise of industry and academia, throughout the supply chain, most of which are available in the UK. The UK is clearly defined in R&D, new product development and process. The UK nanotechnology market has a diversity of interest, with academic expertise in less developed areas such as metrology.

Despite the strengths, there are definite areas that need improvement. There is a clear lack of knowledge about what facilities are available in the UK and the NanoKTN has suggested that if this is going to change, there needs to be a clearer defined and published asset list, available to everyone in this industry. More worryingly there is limited availability of UK suppliers of versatile and experimental facilities that include all techniques and as well as this, there is as yet no equipment supply for high volume production. With gaps between one off and production scale processes not easy to fill in the UK, this could be the downfall of development in this area within the UK.

Once the gaps have been identified and filled, we will start to see the commercial benefits of establishing an end-to-end supply chain, to enable UK technology innovators to get products to market faster and easier.

By ensuring that the whole of Europe continues to invest in ALD technology, and by working in partnership with universities to push the boundaries, we can build on Europe's position as global technology innovators.

Dr Alec Reader is director of NanoKTN

"DESPITE THE STRENGTHS, THERE ARE DEFINITE AREAS THAT NEED IMPROVEMENT; THERE IS A CLEAR LACK OF KNOWLEDGE ABOUT WHAT FACILITIES ARE AVAILABLE IN THE UK"

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Paper with a Memory Given Boost by Nano Breakthrough

Researchers at the Emerging Technologies Research Centre (EMTERC), part of the De Montfort University Leicester (DMU), are exploring the potential of gold nanoparticles and small molecules to create flexible memory chips that can be used in paper and clothing.

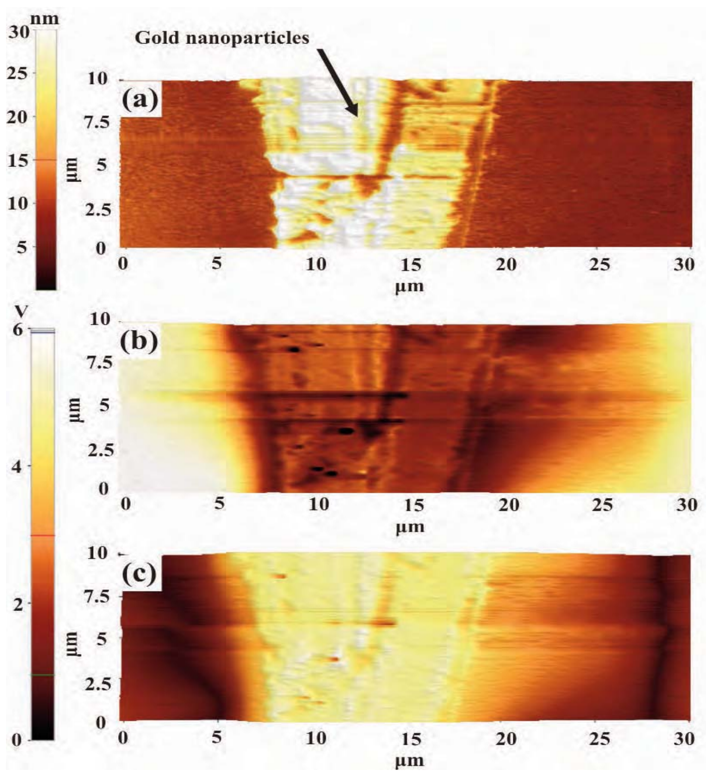
Tests at DMU have shown the nanoparticles can be charged when an electric field is applied, and retain that charge when the field is taken away. This ability is essential for use in memory devices, as it allows information to be stored in the form of charged and uncharged particles.

Silicon-based devices are brittle and can easily be broken if bent. This makes them less robust and harder to put in everyday objects. Organic electronics, on the other hand, can be applied to cheaper materials, such as plastic or paper, and can withstand being bent without breaking, which means they can be used to make foldable or rollable devices, or integrated into things such as clothing.

Equally, organic electronics can be produced at low-cost, are able to be made in room temperature conditions, rather than using very expensive techniques that involve high temperatures, and can be bonded to flexible materials, such as paper and very thin plastic.

"The use of gold nanoparticles could be an essential step towards the mainstream adoption of organic electronics, as they are commercially readily available and do not oxidise or rust, unlike other nanoparticles which have been tested, such as iron," said Dr Shashi Paul, Head of EMTERC, who led the research, which was funded by £207,000 from the Engineering and Physical Sciences Research Council (EPSRC).

"Conventional electronics have manufacturing steps at very high temperatures – sometimes up to 1000°C or greater – and these processes are extremely energy-intensive and therefore expensive," he said. "Organic materials can be processed at room temperature and so require considerably less energy."



(a) Atomic Force Microscopy (AFM) image of gold nanoparticles; (b) Electrostatic Force Microscopy (EFM) image taken after applying positive voltage to nanoparticles; (c) EMF image of gold nanoparticles after applying the negative voltage. EMF images clearly show the electrical charging and discharging of gold nanoparticles

■ A German-Spanish research group, created by the Max Planck Institute for Quantum Optics in Garching and the Institute of Photonic Sciences (ICFO), is using the principle of the Schrödinger's superpositioned cat to test for quantum properties in objects composed of as many as one billion atoms, and possibly including the flu virus.

In order to test for superposition states, the experiment involves finely tuning lasers to capture larger objects such as viruses in an 'optical cavity'; another laser to slow the object down (and put it into what quantum mechanics call a 'ground state'); and then adding a photon in a specific quantum state to the laser to provoke it into a superposition.

■ Baolab Microsystems has announced a new technology to construct nanoscale MEMS within the structure of the actual CMOS wafer itself using standard, high-volume CMOS lines. This allows for much easier and quicker fabrication with fewer process steps; normally MEMS are built on the surface of the wafer. The new process reduces the costs of MEMS by up to two thirds, or more if several different MEMS are created together on the same chip.

The Baolab *NanoEMS* technology uses the existing metal layers in a CMOS wafer to form the MEMS structure using standard mask techniques. The Inter Metal Dielectric (IMD) is then etched away through the pad openings in the passivation layer using vHF (vapour HF). The etching uses equipment that is already available for volume production and takes less than an hour, which is insignificant compared to the overall production time.

■ Touch technology materials maker Peratech Limited has been commissioned by the MIT Media Lab to develop a new type of electronic 'skin' that enables robotic devices to detect not only that they have been touched but also where and how hard the touch was.

The key to the sensing technology are Peratech's patented 'QTC' materials. QTCs, or Quantum Tunnelling Composites, are a unique new material type which provides a measured response to force and/or touch by changing its electrical resistance, which enables a simple electronic circuit within the robot to determine touch.

Uniquely, QTCs provide a 'proportional' response, detecting 'how hard' they have been touched.

INVESTMENT IN ADVANCED MANUFACTURING SKILLS KEY TO ECONOMIC RECOVERY

"There have been some massive shifts in the labour market over the past decade" – Chris Humphries, Chief Executive, the UK Commission for Employment and Skills

High level skills in science, technology, engineering and mathematics will be vital for the UK to take advantage of growth in the multi-billion pound advanced manufacturing industry, says a major new report into the future economy of the UK.

The first National Strategic Skills Audit, commissioned by the government and published by the UK Commission for Employment and Skills, warns that if the economic recovery is to continue, it is vital that future skills development needs are correctly identified and prioritised.

Two specific areas of future skills development have been hailed critical for the growth of advanced manufacturing. One is at the management and leadership level, with the ability to drive new product development and commercialisation as the sectors develop; and the second is at an individual level, for an understanding of multiple scientific disciplines, different target markets and supply chains so the commercial potential of new product innovation can be realised.

"This is an important report for the industry that demands attention. The advanced manufacturing sector depends on people being equipped with the right skills for the jobs of the future," said Chris Humphries, Chief Executive of the UK Commission for Employment and Skills. "Despite having a more skilled workforce than at any time in our history, we still lag behind many of our major economic competitors. In order to catch up, skills investment needs to connect more to the jobs that need doing now and that will need doing in the future."

"We need more and better businesses with more and better jobs, not just to recover from the recession, but be better than we were before it," he said.

Advanced manufacturing is one of six key sectors identified for potential economic expansion and job opportunities in the UK; the others include digital economy, low carbon economy, engineering/construction, life sciences and pharmaceuticals, and professional and financial services. In addition, six manufacturing sub-sectors have been identified as vital to spearhead the advanced manufacturing sector: aerospace, silicon electronics, plastics/printed electronics, industrial biotechnology, composites and nanotechnology.

Sir Mike Rake, Chair of BT plc and the UK Commission for Employment and Skills said: "Our National Strategic Skills Audit doesn't have all the answers, but it does provide a chart by which to sail. Markets – all markets – operate on information and this Audit provides the richest and most comprehensive information ever produced about skills and jobs in England. Tomorrow's jobs are not the same as today's and we would be failing in our collective responsibility if we didn't look to see what's coming down the line and prepare ourselves to meet it."

THE INDUSTRY'S LOST DECADE?

Malcolm Penn is CEO and chairman of market analyst firm Future Horizons, based in the UK

THE 2000S WILL surely go down in history as the worst decade ever for the semiconductor industry. It started off fabulously with a 37% growth only to fall foul of the dot.com bubble implosion and a 32% market decline in 2001. The 2003-04 recovery spurt then proved relatively short-lived paving the way for four years of virtual stagnation.

Year 2009 was then hit by the global economic meltdown and what easily could have been a massive 28% market decline. As it was, the final loss was 'only' 9% but the net result was an IC compound annual growth rate (CAGR) of just 0.8% between 2000 and 2009. At the same time, the technology evolution marched on, down a seemingly inexorable journey to profitless prosperity.

Whilst the 2000s were clearly the industry's worst ever decade, prompting cries of despair that the glory days were over, we believe it is not a sign of impending doom. Clearly, from a mathematically view the 0.8% CAGR number is correct, but the conclusions to be drawn from this need to be interpreted with care. For a start, the data range covered happens to measure a peak (2000) to trough (2009) period; the CAGRs one year either side of this period were 7.8% for 2001-2010 and 5.4% for 1999-2008. Moreover, looking at the corresponding values for IC units, rather than US dollars, shows the underlying annual 10% IC unit growth rate intact.

Herein lies the fundamental danger of statistics. You can derive almost any CAGR value you want, simply by choosing the right start and finish points, and in so doing 'prove' virtually any scenario you like, providing amply fodder for the optimists and pessimists alike.

The fact that IC units showed growth in line with their average points to the fact that the 'problem' with the 2000s was one of declining average selling price (ASP) not growth. The 2000s were thus a decade of depressed ASPs. The real question is thus not the low market value growth – this was the effect – but whether the cause (an above average decline in ASPs) was a bell weather of things to come, as many believe, or a temporary occurrence, the result of a coincidence of events?

ASPs are a very complex issue, driven not just by price increases but also product mix, IC innovation, fab capacity and production techniques. For sure the industry has seen declining ASPs since the 2001 crash, but it is fundamentally flawed logic to extrapolate this into the future; it's a little like saying real-estate prices will forever keep on rising. They do not, neither will IC ASPs keep on falling.

We see the 2000s ASP fall as one side of a cycle; the coincidence of events rather than a sign of more bad news to come. It is vital, therefore, to understand the events that caused the problem. First the industry experienced a major yield bust at the 130nm node, delaying its introduction by a year and destroying the ASP price enhancement it would otherwise have brought.

Second was the transition to 300mm wafers, the sole purpose of which was to reduce IC costs. A 2x plus increase in gross die per wafer for only a 40% wafer cost increase means a 40% die cost decrease. As is typical in our industry, all of this cost reduction was immediately passed on to the customer meaning all 300mm wafer sourced ICs were reduced in selling price by up to 40%. By the end of the decade this was over half of all silicon made.

"THE 2000S WERE MORE A DECADE OF LOST GROWTH, NOT THE END OF THE WORLD; IN NO WAY DO THEY SIGNIFY THE CHIP INDUSTRY DEMISE"

Third, for DRAMs, where fabs must always be kept fully loaded, the increase in die output due to the 300mm transition was more than the market could use meaning rampant oversupply and the mother of all price wars. It is only now that this massive one-off incremental capacity increase has been absorbed that pricing has return to its 'normal' pricing curve. The subsequent Cap Ex restraint has now triggered a fab famine, the like of which no amount of die shrinking can offset. ASPs are already now double what they were just 12 months ago, with a minimum two-year period of positive ASP news now in prospect. Some even say three.

A fourth factor was the brutal Intel-AMD 32-bit MPU price war that saw ASPs fall around 30% from their more normal $100 level to $70. With AMD now bloodied, bruised and losing money, we can expect to see MPU ASPs trending up.

Finally, excess capacity also played its role but is already no longer a factor due to the significant slowdown in new capacity investment over the past two plus years. Wafer fab capacity is now essentially sold out, with allocations, extended lead times and price increases the new industry norm. Some firms are already paying a price premium in order to jump the foundry wafer delivery queue.

Interestingly overall industry revenue per wafer start increased to $7.70 per sq cm in 2009 from $6.96 in 2008, despite 2009 being the worst recession year in the history of the chip industry. Watch for this number to hit its $8 to $9 long-term average in 2010.

We see no near-term end to the underlying industry 10% annual IC unit growth rate but we do see an end to the factors that depressed ASPs in the 2000s. Yield busts come and go, but the 300mm transition is over – we are now on the normal industry learning curve decline.

Wafer fab capacity is now be driven primarily by Cap Ex, not one-off gains such as wafer size transitions, and this will be governed by industry's willingness to invest – they currently are not – which translates into no new capacity for at least the next 12 months. Even a 50-80% increase in 2010 Cap Ex – the current top end of the forecasts – will not significant increase new capacity; the starting point is so low.

With DRAM demand hot – 4Gb is the entry point for 64-bit/Window 7 systems; strong demand for servers; new Intel processors in prospect; and a two to four year backlog in enterprise workstation upgrades – and Flash growing too, driven by exploding demand for Smart phones, the memory market has entered a positive cycle for growth and profits. This will have a positive impact on the industry as a whole.

The 2000s were, thus, more a decade of lost growth, not the end of the world; in no way do they signify the chip industry demise. 10% IC unit growth (the underlying growth trend) coupled with any positive ASP growth means double-digit growth at the IC value level. This is really potentially good news for the industry as a whole but not for all companies.

For a start, the OEMs will need to get used to a capacity (supply) limited market with increasing, rather than decreasing, IC buying prices. Secondly, the fabless and fablite firms will need to adjust to a world of tight foundry wafer supply and increasing prices. It will be a sanguine moment when they suddenly realise that they are no longer in control of the delivery times and prices they quote to their customers; their business is now at the mercy of their foundry partners. ■

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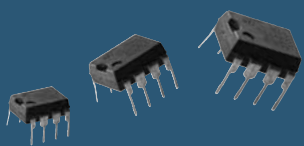
SOURCE CODE REVISION CONTROL

AIMS AND BEST PRACTICES



Vicky Larmour from Cambridge Consultants gives an overview of some of the tools available for source code revision control

THERE ARE A plethora of tools available for source code revision control: proprietary or free open source, centralized or distributed, get-change-merge or lock-change-unlock; explanations of the options and lists of tools of each type are widely available. Here, I aim to cover some best practices in this area, which are applicable regardless of the system or combination of systems you use.

Let's start by looking at the aims of revision control. Software engineers often agree that revision control is theoretically 'A Good Thing', but a lack of clarity as to the main aims of such a system can lead to non-optimal usage and a corresponding failure to reap the full benefits of the system. A poorly implemented revision control system can even become a burden and an obstacle to good practice.

The key aims of a revision control system should be:

- To enable you to identify the source code making up a given release and to re-create that release exactly.
- To allow multiple strands of development to take place simultaneously on the same code base.
- To track changes to a given piece of code over time and revert easily to earlier revisions.

So, to achieve these aims, what belongs under revision control? My opinion is that all manually developed source code belongs under revision control, whereas outputs from the build process (object files, executables, auto-generated code) in general do not. The exception to this is formal releases, which do not change once created.

Storing the required versions of build tools in revision control, alongside the source code, helps with the aim of being able to re-create a given release (watch out for licensing issues, of course). This includes virtual machine images if you use virtual machines as build platforms, which I do recommend as a strategy both for improving the repeatability of builds and also in minimizing the setup time for new engineers joining the project.

How you arrange the contents of the repository is quite dependent on how you will be using it, but I would suggest that at a minimum you should have at the top level:

- A "tools" folder for third-party tools, including any you've developed yourself whose source code lives in a separate system.
- A "releases" folder, ideally configured to be a "write-once" location so releases cannot be changed once committed.
- A folder for your main line of development.

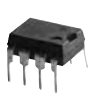
Depending on your specific use case, you may then also want to provide a folder for branches off the main line, and /or a folder containing a "user area" for each developer to work on their own code, without impacting the main line, until they are ready to merge back in.

It may seem obvious, but keep your repository somewhere that is regularly backed up! It is no use at all to be carefully tracking changes to your code base if you then lose the whole lot in a hard disk failure.

Each release should be given a unique release identifier. Ideally this should be built into your binaries automatically by a build system step derived directly from the revision control system. This way you can identify a particular release binary even when the file name has been changed or it has become separated from its software release note; you may well want the binaries to be able to report their own version, either over a debug interface or on a publically-visible user interface.

Once the binary has been built and tested, it can then be stored in your revision control system and labelled with the relevant identifier. The release note must then specify the location of the binary and how to identify the source code and tools it was created from.

Regardless of the particular revision control system you use, does it fulfill the aims listed earlier? Is it a help or a hindrance? Save yourself some long-term pain by taking the necessary steps now to make sure you are getting the most out of it. ■



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Low data rate transmission: Into the NOISE FLOOR

Myk Dormer

WHEN COMPARING similar products in the marketplace, there is a tendency among inexperienced engineers to fasten their attention on a single easily understood parameter and treat it as an approximate 'figure of merit'.

In the low power radio area this parameter is usually data rate. The assumption is made that, if a given module is capable of transmitting a 128kbit/s data stream then it is inherently superior to a unit operating at, for instance, 5kbit/s.

This assumption is, of course, false. Like every characteristic of any component, data rate is just one of a crowd of highly inter-dependant parameters that make up the whole. For radio links, in the simplest sense, data rate, transmit power and operating range constitute three competing factors within which the design must find a compromise.

Basic communication theory shows us that, as bandwidth increases, then (if signal levels are constant) the signal to noise will fall. If communication distance is increased then either transmit power or receiver sensitivity must rise, and if data rate increases the bandwidth must follow it.

In short, you can have a long range, a high data-rate or a low-power transmitter, but you cannot have a long range, very fast, low-power link. Something has to be traded off and it's usually range or power. Short range radio modules offer 64kbit/s or higher data speed, while large, expensive radio modems increase transmitter power to push 5 to 10kbaud data streams 5km or more.

Some applications, however, do not require thousands, or even hundreds of bytes of data. Security, environmental monitoring or control systems might send only a few bytes in an hour, or even in a day, but often use very restricted power supplies (long-life batteries or solar cells are typical). Current methods usually approach such applications with a very short duty cycle method, transmitting a (comparatively) powerful carrier for the shortest period possible, usually with a compromise data rate of a few thousands bits per second, or more.

I'm not sure that this is the only viable method. More sophisticated systems (GPS receivers, long range military communication systems) have successfully used very narrow bandwidth, low data rate techniques for some time and even the Morse Code still used in the HF bands can be considered a form of low speed data link. Perhaps a simple version of these methods could be used in low power radio applications?

Basic communications theory predicts a 3dB improvement in S/N (and hence signalling sensitivity) with each halving of the signal bandwidth. Taking data rate as directly related to bandwidth, a rough 'back of envelope' calculation suggests that an 80 bit per second stream should be detectable at a signal level 18dB lower than a 5kbaud one. This would (for the same range, with the same receiver hardware) correspond to a reduction in power from 500mW to 10mW (although transmit burst duration would need to be sixty times longer, of course).

> "OUR 'USABLE SIGNALLING LEVEL' IS DEFINED AS THE SIGNAL LEVEL AT WHICH EIGHT IN TEN TRANSMISSION BURSTS ARE DECODED WITHOUT ERROR"

Previous tests have suggested that, in practice, a 3dB per halving/doubling is unlikely to be achieved by the simple FM circuitry used in low power wireless module receivers, as the FM discriminator and limiter introduce a non-linear transfer function into the signal path, preventing much improvement beyond the bandwidth of the filters preceding the demodulator.

Some tests do seem worth while, however:

- A basic data communication link, typical of simple ISM band practice, was assembled.
- A -120dBm sensitivity (for 12dB sinad) receiver feeds a biphase/FFSK data decoder device (Radiometrix M48A modem), while the transmitter is simulated using a second modem chip providing modulation for an IFR2023 signal generator.
- A simple program running on the lab PC generates (and displays) a constant sequence of eight byte test transmissions.
- To allow easy variation in data rate, both M48s are clocked from a second signal generator (instead of using local crystal controlled clocks).

Our "usable signalling level" is defined as the signal level at which eight in ten transmission bursts are decoded without error (an 8 byte

M48 packet contains about a hundred decoded bits and a single bit error will result in the burst being voided, so this signalling criteria roughly equates to 0.2% data errors).

TABLE 1:

Data rate:	4800	signalling level -115dBm
	2400	signalling level -118dBm
	1200	signalling level -120dBm
	600	signalling level -123dBm
	300	signalling level -124dBm
	150	signalling level -126dBm
	75	signalling level -128dBm
	37.5	signalling level -129dBm

At data rates below 1200 baud it was found necessary to employ an external data recovery comparator (quantiser) with a much longer averaging time constant.

To maintain improvement in signalling level with reduced baud rate beyond approximately -124dBm an added low-pass filter was required (3 pole Gaussian, matched to the relevant baseband frequency).

Conclusion: Once the baseband signal bandwidth falls below the (approximately) 5kHz audio bandwidth of the receiver, the sensitivity gain for a 50% reduction in data rate falls to around 2dB. As a signal level of -130dBm is approached, the simple methods used in this test cease to yield further significant improvements.

Sensitivity improvement from 4800 baud to 75 baud is 13dB. The transmission time for the 8 byte packet, including preamble times and modem overhead, rises from 50mS to 4 seconds.

This improvement would allow a reduction in transmit power from 200mW to 10mW. Referring to known, practical designs this will reduce transmitter power drain from 150mA at 5V to 10mA at 2.5V. When the different lengths of transmit burst are factored in, this corresponds (in terms of energy used) to 37mJ per burst versus 25mJ.

Interestingly, we see that once the various imperfections and limitations in the actual hardware used have taken their toll, the real power usage of the short/fast burst and the long/slow burst systems are very similar. This allows us to draw some useful conclusions:

- Using these methods, there is little absolute difference in terms of "bits per second per watt per mile". The long burst of the low rate system uses up the power saved, by keeping the transmitter on for longer.
- If band congestion requires duty cycle limitations, or a network architecture requires short, frequent transmission bursts, then a low data rate method is clearly not applicable.
- If there is an external limit on maximum transmit power (a legal limit in band) or a physical limit on peak power/peak current from the power supply, then a low data rate approach can greatly increase maximum signalling range.

Low data rate signalling looks like a useful method, within specific application areas, but when a comparison is made between the primitive test that I've presented here, and the signal levels at which GPS systems operate, or at which cw Morse-Code transmissions can be resolved, one thing is very clear: further experimentation is required!

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

High Power Factor and the MORAL HIGH GROUND

By Chris Richardson, System Applications Engineer, and Kamal Najmi, Power Application Design Engineer, Europe, National Semiconductor

High efficiency lighting is being introduced on a massive scale, but saving watts doesn't necessarily mean saving energy if the new types of lighting have a poor power factor. This article explores the potential problems of replacing large amounts of incandescent and halogen lighting – with a power factor close to 1 – with compact fluorescent or LED lighting which can be quite good, but can also be quite poor. In particular, this article explores the potential headaches for the energy companies and problems that could be generated in each consumer's home if the new "energy efficient" lighting doesn't take power factor into consideration.

To really know if LED light bulbs or light fixtures using LED technology are better than filament lighting, the electric utility must be included as well. In particular, this paper looks at power factor, a measure of how much energy must be generated to do actual work (such as the generation of photons). Filament lamps may not be as efficient at converting electrical power into optical power, but they have very good power factor. LED and CFL bulbs do not provide good power factor unless their electrical drive circuits are designed specifically to do so. The end result is that if millions of households switch to LED or CFL that isn't properly designed, the electric utilities will end up generating energy that they cannot charge their customers for.

SMART METERS AND POWER FACTOR AT HOME

Table 1 shows the test results of two circuits designed for LED light bulbs from National Semiconductor along with two LED light bulbs purchased on the open market. For completeness, the same tests were applied to a typical 17W CFL bulb and a 60W incandescent bulb. All of the bulbs tested were designed to work with standard TRIAC wall dimmers.

To date most utilities still measure and charge homes for real power, in watts, but as shown in Table 1, this could translate into a real losing proposition for the utilities if millions of homes switch to low-quality CFL or LED lighting with a low power factor. With the advent of smart metering, it is reasonable to imagine that residential customers who drag down the power factor could be required to pay more for their electricity.

LM3445 BUCKS WITH OR WITHOUT PFC

The LM3445 is a step-down (buck) controller that uses the "negative buck" or "floating buck" topology shown in Figure 2. Marketed as an offline controller, the LM3445 is still a DC-DC regulator and as such it requires a rectifier and some sort of holdup circuitry to prevent the input voltage from falling below the output voltage on each AC half-cycle. The LM3445 could be operated with just the rectifier but it would create a very low power factor and would need a big bulk capacitor to make it run with a TRIAC dimmer. With the LM3445 National Semiconductor provides a device that avoids visible flickering caused by forward or reverse phase dimmers. The LM3445 overcomes this challenge by translating the TRIAC-chopped waveform to a DIM signal and decoding it to a DC signal. In fact, the LED current is linearly regulated according to the dimming signal.

Figure 2 shows a solution that has a 10W power consumption equivalent to 450 lumens that is comparable to a 40W incandescent bulb providing around 500 lumens. This solution drives 7 high power white LEDs at an average current of 350 mA with the capability to dim them using standard off-the-shelf TRIAC based dimmers.

The valley-fill circuit is used to avoid high peak current during charge of the input bulk capacitor which can be seen in Figure 3. This high input current seen in the 230V line generates high harmonic distortion and therefore is an obstacle to meet the European standard EN-61000-3-2 class C and has a poor power factor. For low power application in lighting, passive PFC is the right approach, giving the current waveform a more sinusoidal shape as seen in Figure 4. But for powers above around 25W this method becomes expensive and bulky, and active power factor correction is a better choice.

The first line of Table 1 shows that the recommended passive PFC gives a power factor of 0.95. The traditional holdup capacitor results in a power factor that drops to 0.66. While it does require more components, a power factor corrected circuit reduces harmonics and energy transmission costs. The question is how long it will be before the utilities take steps to make consumers and homeowners think twice before

Bulb Type	# of LEDs	Real Input Power (W)	RMS Input Current (mA)	Apparent Power (V-A)	Power Factor
LM3445 with passive PFC	7	10.13	45.9	10.65	0.95
LM3445 without passive PFC	7	10.5	68.6	15.7	0.66
Commercial LED Bulb A	4	5.6	47.4	10.8	0.52
Commercial LED Bulb B	4	6.6	41.8	9.7	0.67
17W CFL		16.8	118	27.5	0.61
60W Incandescent		59	259	60	0.99

Table 1: *: Power Factor for Various "High Efficiency" Light Bulbs, V_{IN} = 230VAC*

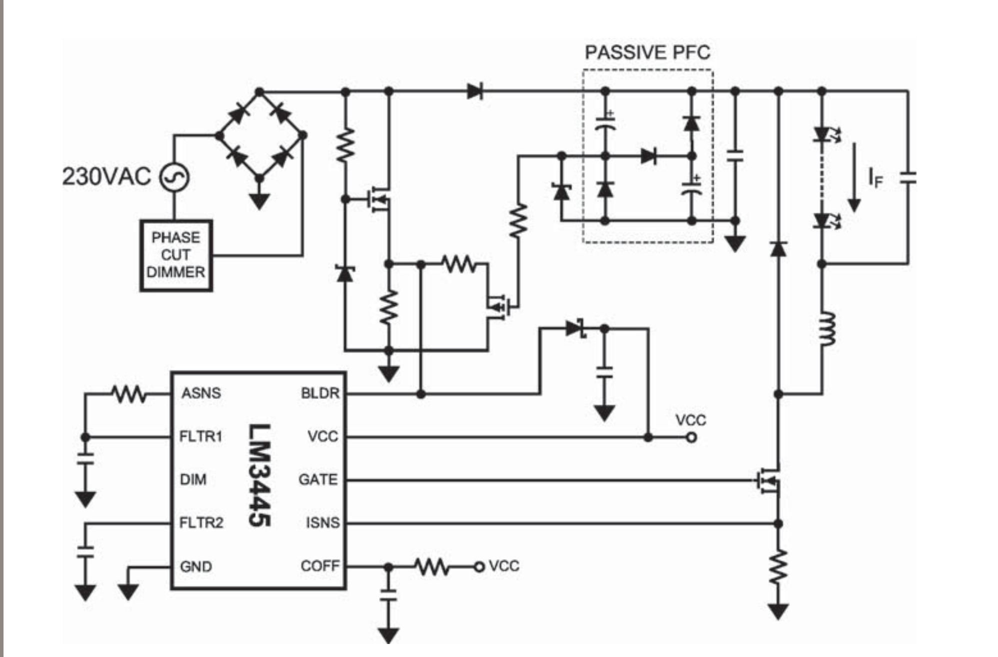

Figure 2: *LM3445 with Passive PFC*

buying a low power light bulb with low power factor.

What happens when one million households switch from filament lighting to low power but also low power factor lighting? The volt-amperes needed to supply those homes decreases, which is good from the standpoint of the consumer and the environment. But the real power delivered drops even further – the lower the power factor, the lower the ratio of real power to apparent power. Roughly speaking, the apparent power that must be generated is equal to the real power divided by power factor, so if one million 60W filament light bulbs were replaced by one million 10.5W LED light bulbs with nothing but a bulk holdup capacitor, then 60 MW for 60 MV-A generated would be replaced by 10.5 MW but would require 15.7 MV-A. The utility company sees an 83% loss in power sold but only a 74% drop in the volt-amperes they must generate.

THE LAW AND THE MORAL HIGH GROUND

The European Union leads the world in dealing with distortion, power factor and pollution of the AC line with harmonics. Eliminating harmonics is essentially synonymous with correction of power factor, and it is the process of both returning the current waveform to the sinusoidal shape of the voltage and ensuring that current and voltage are in-phase.

As it stands, the regulations require harmonic correction for lighting above 25W of input power, including LED lighting. Manufacturers focused on cost will be tempted to omit PFC circuitry to save space, weight and cost. On the other hand, those manufacturers focused on providing a quality product may choose the "high moral ground" and design their LED light bulbs to meet the IEC/EN requirements. The additional cost up front could well lead to savings for both consumers and producers if the regulations change, something that has already happened as the number of rectifiers used in homes and businesses continues to grow.

National Semiconductor will be demonstrating LED lighting solutions at the EuroLED exhibition in Coventry, 9-10 June 2010 (stand LED44).

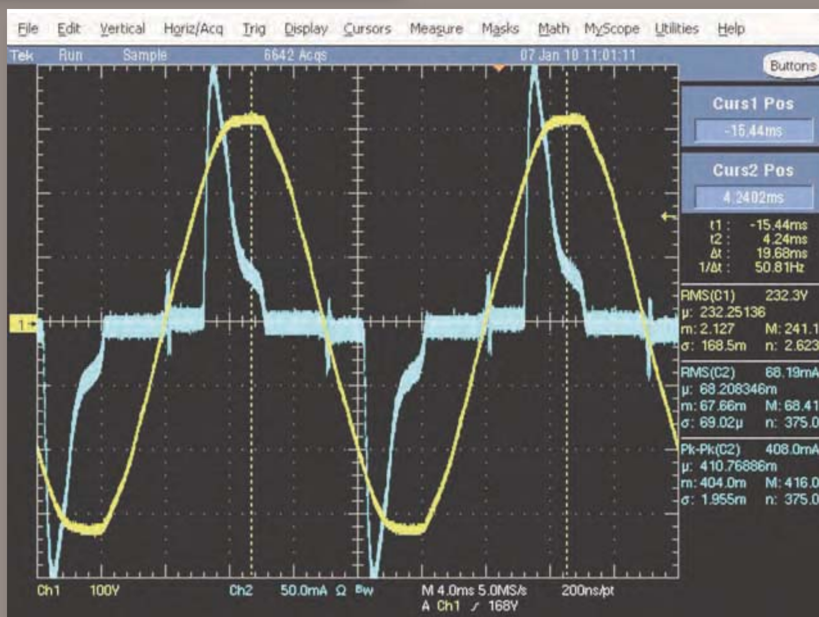

Figure 3: *Input Voltage and Current for the LM3445 without PFC*

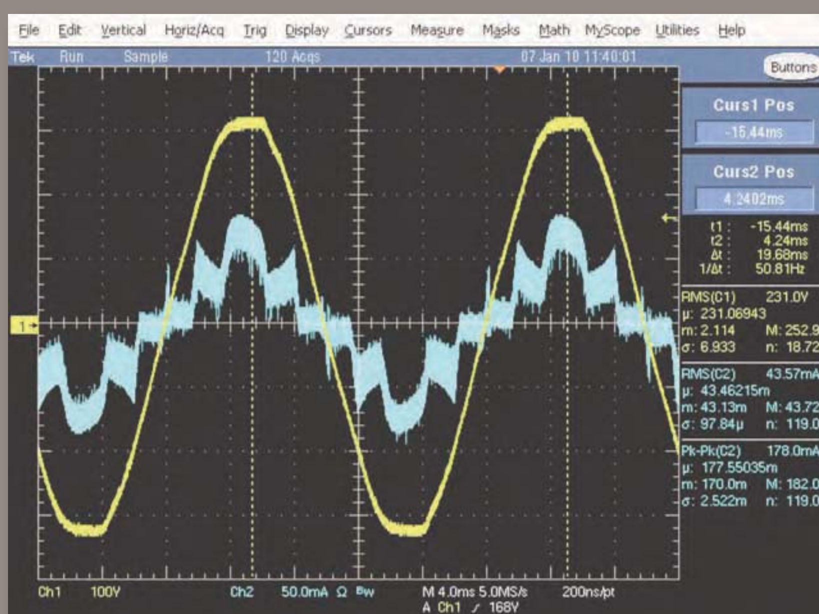

Figure 4: *Input Voltage and Current for the LM3445 with PFC*

THE ZOBEL NETWORK – INSIDE

In response to the letter from Mike Turner in the January issue of Electronics World on the position of the Zobel network, I think there is little doubt that the majority of designers put it inside the output inductor, where it can best do its job of preventing instability caused by inductive loads. Looking at random through my database of circuitry, I find the following models have the Zobel firmly positioned inside:
Accuphase P300 • Cambridge Audio 840A Cambridge Audio 840W • JVC A-S7 • Lecson AP-3 • NAD 3020 • Quad 303 • Sony TA-N7 • TAG-McLaren 250x2R • Yamaha M70.

That is, of course, only a very small sample from hundreds of possible candidates. It covers a wide range of time and country of origin. I am certainly not stating that it is impossible to make a stable amplifier with the Zobel network outside the inductor, but in my experience of designing for mass-production, it is distinctly more difficult.

I must admit that I was not aware that Hi-Fi was "the fag-end of the electronics industry". I thought it was a quite significant multi-billion-pound affair, but we live and learn.

As to why Mr Turner should think that I advocate damping resistors only connected at one end, I feel it best not to even try to make sense of that passage. I am surprised, however, that he advocates taking the negative feedback from outside the inductor. I have the schematic of a Turner A500 amplifier (I assume I am replying to the appropriate Mike Turner?) in front of me and the NFB comes from inside the inductor.

Finally, for the very different business of putting a Zobel network across a loudspeaker to make it look like a purely resistive load: this may be simple when you have a single speaker unit, but it becomes much more difficult when, as in the real world, you are dealing with multiple speaker units and a complex crossover network.

In any case, I have never been sure why some people think this is a good idea. A complicated impedance curve may look daunting to us, but amplifiers are not conscious and providing they are designed with adequate output stage capability, simply carry on delivering the signal; a locally higher impedance is actually a good thing as it reduces the distortion from the typical output stage.

Flattening a loudspeaker's impedance curve by adding shunt elements also means a good deal of power lost in those extra components, which is not so hot for the old carbon footprint.

I am aware that KEF introduced "conjugate load matching" in the 1980s, for example in their C80 model, which had its impedance being described as "4 Ohms resistive" rather than the usual 8 Ohms, and possessed a dauntingly complex crossover network but, as far as I can determine, they abandoned this approach years ago.

Douglas Self UK

Phenomenological , Indeed!

I congratulate you on your courage in printing the article on COBE and WMAP. It should prove both a popular and controversial article. Hopefully, it shall spark comment and interest in other quarters not commonly served by the astrophysics community.

Whereas I note that Robitaille has published various articles in "Progress in Physics", he has been circumspect in his critique and, thus, cannot easily be dismissed. Crothers, however, from a cursory review of his website, appears to have an axe to grind (not unusual given the egos involved) within the theoretical physics community, so I suspect that his comments about Hawking (who, I suspect, qualified his comment cited) shall not go unchallenged.

It is all good sport. Where everyone is ignoring the fundamental relationship between Number Systems, Mathematical Modelling and Physical Reality, so it is also relevant to appreciate that Robitaille's field of Nuclear Magnetic Resonance itself is based on the famous Bloch Equations, which are phenomenological equations that were developed by, the much ignored and derided, Felix Bloch in 1946.

Other phenomenological examples in physics cited from Wikepedia include: "The examples below are in chronological order.

- *Second law of thermodynamics:* Prior to the development of statistical mechanics by Ludwig Boltzmann (1896), this law was phenomenological. For instance, spontaneous net flow of heat from a lower temperature to a higher temperature had never been observed and this fact served as the basis of the second law.
- *Rutherford model* also known as planetary model (1911) describes the structure of an atom based on the experimental results. It has a number of essential modern features, including a relatively high central charge concentrated into a very small volume in comparison to the rest of the atom. It resembles the planetary system, a known physical object larger by several orders of magnitude. It was superseded in 1913 by the Bohr model, which used some of the early quantum mechanical results to give locational structure to the behavior of the orbiting electrons, confining them to certain circular (and later elliptical) orbits.
- *Landau theory* of second order phase transitions (1936).
- *Bloch equations* (1946).
- *Ginzburg-Landau theory of superconductivity* (1950).
- *Modified Newtonian dynamics* (1983).

It might be worth drawing readers' attention that no one really knows what light is and that no one really knows what temperature is also.

With respect to light, it all goes back to Maxwell and the EM model and the deficiencies are generally well known. As for temperature, this is not the case. The Second Law of Thermodynamics (cited above) is also relevant to the published article. Accordingly, you may wish to invite an incendiary comment from Peter W Atkins (professor of Physical Chemistry at Lincoln Oxford) as to why no one knowing what temperature is has a bearing on the arguments advanced, thus getting your defence/retaliation in first and wrong footing the pack.

I trust that you shall agree with me that anyone discovering what light and temperature is would have a definite claim on the scientific discovery of all time.

Barry McKeown UK

The publisher reserves the right to edit and shorten letters due to space constraints

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The 5-MINUTE GUIDE to Chip-Level Audio Test

Dan Knighten, Director of Products at Audio Precision, explains the benefit of testing audio devices at chip level and how R&D engineers can go about it

TESTING DIGITAL audio ICs at the chip level, whether you are the developer of that chip or merely evaluating it for use in a product you are creating, can seem mysterious and difficult. However, it is critically important to be able to measure individual chips. You will never be able to achieve lower residual noise and distortion that what emerges directly from a digital audio converter IC.

Here, we will explain what the basic digital audio connection to ICs is and how to interface directly to it with a standard audio analyzer.

I2S, or Inter-IC Sound, is a relatively simple serial data protocol which originated with early CD players as the connection between the optical transport and the digital to analogue converters inside the device. I2S typically uses three wires: one for multiplexed stereo audio data, one for word select which indicates the start of a new frame of data (sometimes known as the frame clock, word clock or Left/Right clock) and finally a bit clock.

Figure 1: APx digital I/O and digital serial I/O front panel

Today I2S is the most popular chip-level digital audio interface. I2S is not meant to run a great distance, no more than a few inches on a circuit board, but the independent clock and data lines means that I2S has low intrinsic jitter and is not subject to data induced jitter. There are also many other serial data formats with names such as Left Justified, Right Justified, DSP and TDM. These follow the pattern of I2S with a frame clock, bit clock and data line(s). However, the particulars of whether the frame clock goes high or low at the start of a frame, when the data starts in relation to a number of bits after the start of the frame and the alignment of audio data in a frame all vary.

Hooking Up

Assuming you have access to an audio analyzer that provides a direct interface to I2S and other chip-level connection protocols, the primary challenge will be making the physical and logical connection. With external digital

Figure 2: APx DSIO clock and data lines

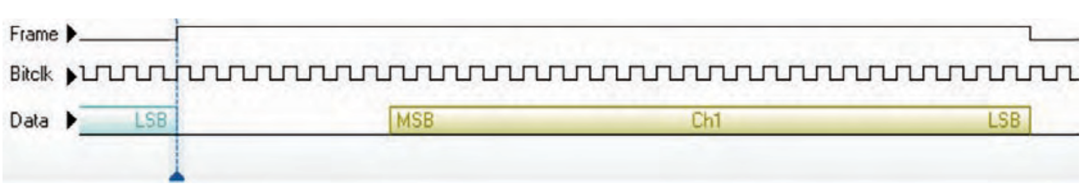


Figure 3: APx DSIO active timing diagram

Audio Precision multichannel audio analyzer

audio interfaces, such as S/PDIF, Toslink or HDMI, you do not typically have to deal with anything more complicated that connecting a single cable and selecting your sample rate. With I2S you will be working directly with a naked circuit board and you will be looking at 2-pin headers that provide master clock (mclock), frame, word, or L/R clock, bit clock and one or more sets of data pins. If the device provides a completely basic I2S interface then there is a reasonable chance that you can simply connect the data, frame and bit clock lines from your analyzer directly to the device. Most analyzers provide configuration presets for I2S and away you'd go. However I2S is not the product of an international standard, it is solely an industry convention. Such that many devices with an I2S interface will not simply work out of the box with the standard settings.

Troubleshooting the Connection

In most situations, the prerequisites for successfully connecting to a digital audio chip, in addition to the audio analyzer, are an oscilloscope and a detailed data sheet for the part in question. The better audio analyzers will provide buffered monitor outputs for the transmitter and receiver clock and data lines. These buffered outputs are provided for connecting an oscilloscope so that you can monitor the actual timing of the different signals.

It is important to monitor the clock and data lines through a buffered output. Remember that I2S is intended to run a few inches across a circuit board. If you attach a one meter cable from the chip to the audio analyzer and then use a BNC T connector to monitor it with an oscilloscope, the electrical loading will exceed what most of these devices can drive and will cause severe degradation of the signal integrity.

Once the device under test is connected to the audio analyzer and an oscilloscope is connected to the monitor outputs of the analyzer, there is a straightforward process to connect them to the device under test:

1. Configure your audio analyzer according to the requirements provided in the part's data sheet.
2. Construct a timing diagram based on the configuration you are using for the device. Many datasheets will come with a timing diagram; the better audio analyzers will also render a timing diagram based on the configuration choices you make.
3. Match the timing diagram for the part to the actual timing displayed by the oscilloscope.

If everything matches, you should then be able to generate and analyze audio through the device under test. If there is a problem, likely a mismatch between the actual data format and the desired format, then troubleshooting begins. For troubleshooting, keep in mind that almost all parts support many different serial data formats and timing arrangements. Make sure you have configured the device for the format and timing arrangement you want to use.

Audio Measurements

Once you have successfully connected to the device your audio analyzer, it should allow you to make all the normal audio measurements. In the world of ICs it is particularly important to test devices across their full operating range; checking for amplitude linearity, alias products and pass-band ripple among other features. Also, many ICs have different performance at different sample rates.

Finally, if you are measuring a multichannel IC and your audio analyzer supports a direct connection to either TDM multichannel data or multiple data lines, you can verify time alignment on all the channels. Using phase offset signals you can also verify the absence

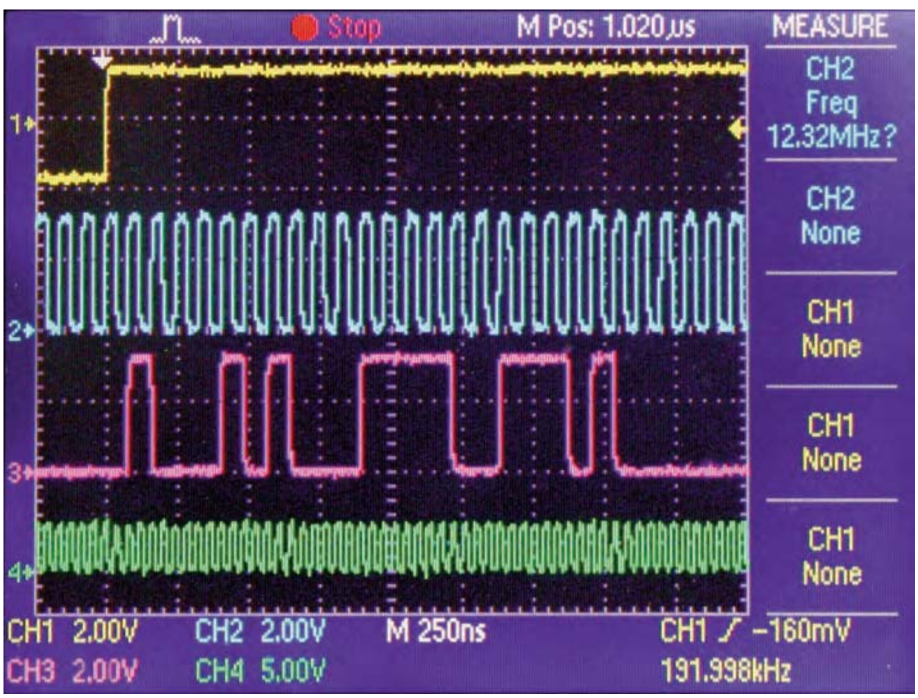


Figure 4: *Monitoring the clock and data lines with an external scope*

of distortion crossover. Finally, if your audio analyzer supports independent transmitter and receiver clocks, you can verify the performance of devices that perform sample rate conversion at the chip level.

Top Tips for Testing Chips

- Keep your cables short and watch out for excessive loading and impedance mismatches. I2S is not meant to drive signals over long distances. Use the cables supplied with your audio analyzer. These are usually the maximum length and are impedance matched to the analyzer.
- Don't forget grounding and don't use digital grounds for analogue audio signals. In complex test setups, stray noise can be easily introduced by ground loops between the device under test and multiple items of test equipment. Pick a common ground point and star ground all devices to that point (typically the audio analyzer chassis).
- Troubleshooting connection issues can be rapidly expedited by monitoring the digital signals with an oscilloscope. Just remember to connect the oscilloscope to buffered monitor ports on the analyzer not in parallel with the device itself.
- The unmarked side of double-row pin headers is often ground, but it's not always safe to assume that.
- Observe static protection measures to prevent failures (yes, you really can fry those chips just like that!).

***Figure 5:** Sample rate converter input and output clock rates*

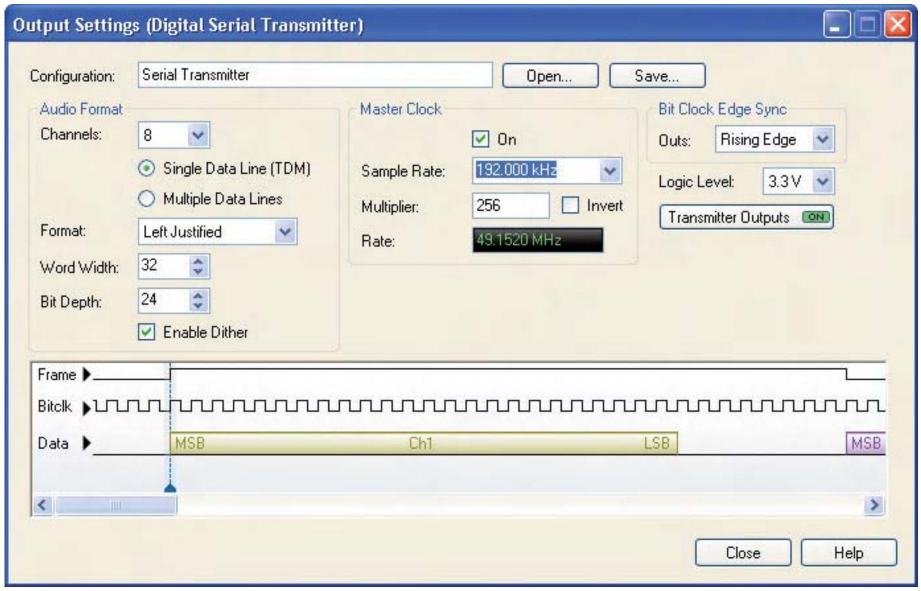


Figure 1: *FM radio test setup, with APx526, transmitter and car stereo*

Testing RDS-equipped FM RADIO RECEIVERS

Joe Begin, Director of Technical Support, and **Adam Liberman**, Technical Writer, both at Audio Precision, explain how best to go about testing FM radio receivers, including a look at how FM broadcast and Radio Data System (RDS) signals work, and how to encode test signals for use with a receiver in a test and measurement workflow

TESTING FM RECEIVERS is not that much different than testing other pieces of audio equipment. Appropriate tests include "the big six": level, frequency response, THD+N, phase, inter-channel crosstalk and signal-to-noise ratio. You make the measurements just like you would when testing other audio gear – by connecting an audio analyzer to the device's output and measuring the signals to see what effect the device has had on them.

However, in practice, there are a couple of significant differences between testing a usual line-level audio device and an FM receiver. This has to do with how you format the test signals and how you get them into the receiver.

Audio recorders and processors are typically connected directly to the inputs and outputs of an audio analyzer. But an FM receiver accepts its audio input over the airwaves as a multiplex encoded FM radio signal. What's more, since most FM receivers are capable of receiving Radio Data System (RDS) signals, the onboard systems for decoding such signals should, ideally, also be part of your test routine. RDS is a communications protocol for sending small amounts of digital information within a conventional analogue FM radio broadcast. Typically, RDS signals are used to transmit program-related information, such as the name of the program, artist or song title currently being transmitted or emergency messages directly to the front-panel display of FM receivers.

In this article, we'll look at how multiplex and RDS encoding for FM broadcast transmission works, and how this is used to send suitably encoded signals to an FM receiver as part of a thorough test routine.

FM Broadcasting

Frequency modulation (FM) was invented

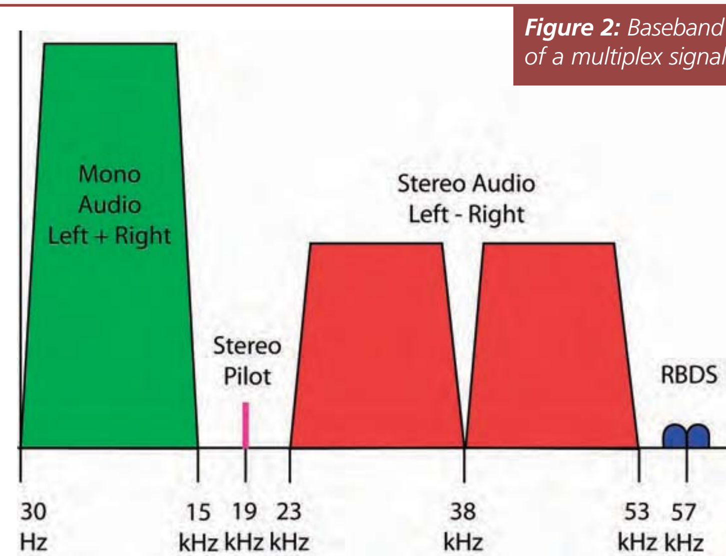
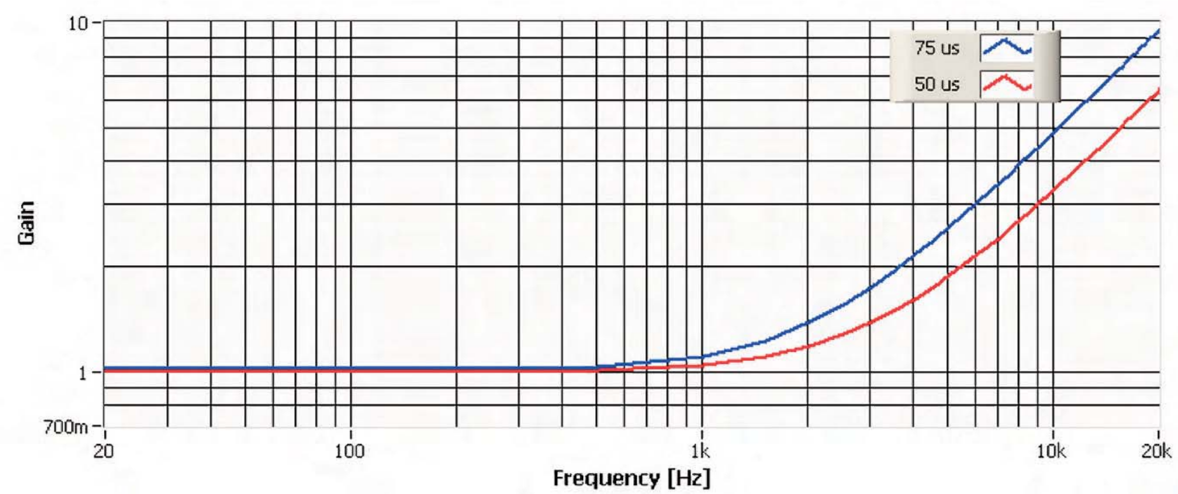


Figure 2: *Baseband spectrum of a multiplex signal*

Figure 3: Pre-emphasis filters (50 and 75µs)



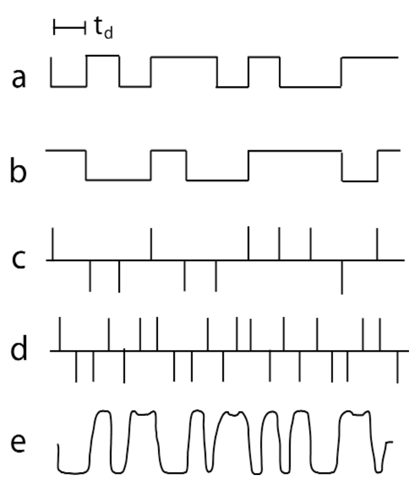
in 1933 by Edwin H. Armstrong, one of the founding fathers of radio technology, and is a technique whereby a baseband message signal m(t) varies or modulates the frequency of a carrier wave. In broadcasting, FM is used to provide high-fidelity sound over broadcast radio. In this case, the 'message' signal is music and speech, and the carrier wave is at a radio frequency within the VHF radio band, usually 87.5 to 108MHz.

FM radio was first used for monaural broadcasting in the 1940s, and FM stereo was introduced in the 1960s. One of the key requirements for stereo FM broadcasting was to maintain backward compatibility with the large existing base of monophonic FM receivers. This goal was achieved by using a clever scheme to multiplex the stereo signal channels as follows.

The left (L) and right (R) audio signals are first low-pass filtered at 15kHz, and then the sum (L+R) and difference (L-R) signals of the two stereo channels are formed. The (L+R) signal is broadcast in the lower portion of the baseband spectrum (0 to 15kHz), such that a monophonic receiver correctly receives the signal as a monaural transmission. The (L-R) difference signal is then amplitude modulated onto a suppressed 38kHz subcarrier in the 23 to 53kHz region of the baseband spectrum. A 19kHz pilot tone is added to the multiplexed signal – one half the frequency of the 38kHz subcarrier and with a precisely defined phase relationship to it. This pilot tone is used by FM receivers to detect a stereo transmission and to reconstruct the stereo signals from the multiplexed signal.

To improve the signal-to-noise ratio, it is a common practice to apply a pre-emphasis filter to the audio signals before breaking them into L+R and L-R components, to boost the higher frequency portion of the signal. The pre-emphasis filter has the high pass characteristic of a simple RC filter circuit (**Figure 3**). The amount of pre-emphasis is defined by the time constant of the RC circuit. In North America, a 75µs time constant is used; in the rest of the world, 50µs is used.

Figure 4: RDS waveforms

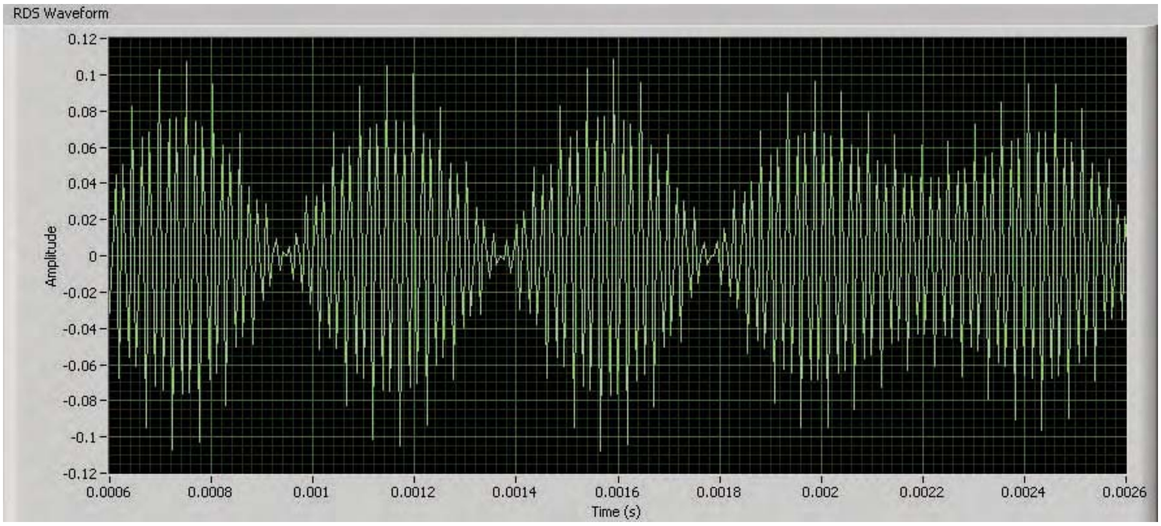


FM receivers incorporate a reciprocal de-emphasis filter, which removes the effect of the pre-emphasis. This restores the message signal's flat frequency response after transmission. The trade-off for using pre-emphasis and de-emphasis is that high frequency headroom is reduced.

Note that the multiplex signal shown in **Figure 2** also contains an RDS signal. To add an RDS message to an FM stereo broadcast signal, an RDS encoder is used, as illustrated in **Figure 4**. The bit rate is 1187.5 bits per second, 1/48th of the 57kHz RDS subcarrier frequency (the second harmonic of the 19kHz broadcast pilot tone). As this bit-rate is quite low, RDS is only suitable for sending small amounts of text, or other data, that get updated with a time frame in the order of seconds.

The RDS message (a) first passes through a differential encoder, which is the equivalent of a logical exclusive OR (b). It is then converted from non-return-to-zero (NRZ) coding to pulses (c), and then to a series of bi-phase symbols, to minimize the power of the data signal near the 57kHz subcarrier (d). The bi-phase symbols are then filtered with a data-channel spectrum shaping filter to achieve the required band-limited spectrum (e). Finally, the filtered data waveform is used to modulate the 57kHz subcarrier frequency and is then summed with the rest of the multiplex stereo signal (the waveform of the modulated signal is seen in **Figure 5**). A decoder in the FM receiver is used to

Figure 5: RDS signal waveform in the Signal Preview Window



decode the RDS message, usually so that the text can be displayed.

Testing, Testing...

Testing an FM receiver requires an FM transmitter or exciter; these are small transmitters that are typically used to drive an RF power amplifier to create a more powerful signal. The transmitter takes the monaural or multiplexed stereo signal (with or without RDS) and modulates an RF frequency within the FM band. Transmitters are available from various vendors, with solutions varying from inexpensive do-it-yourself kits to professional-grade broadcast equipment.

It's important that the audio quality of the transmitter be better than the receiver under test, or else the measurements will reflect the transmitter's limitations and not the receiver's. When comparing transmitter specs: note that some companies may be more conservative in their numbers than others and that testing methodologies can differ. Sometimes the testing conditions are not stated, which makes comparison difficult.

To test RDS, the RDS signal must be added to the audio signal after the FM multiplex stage. Stand-alone hardware encoders are available to do this, but for testing purposes, software solutions can do the job much more affordably – some, such as the Stereo Tool plug-in for the PC audio playback utility Winamp, are freeware.

Test and measurement manufacturer Audio Precision offers an RDS encoder utility for use with its APx Series audio analyzers. The utility creates sine-wave test signals, which it multiplexes and combines with RDS messages. The completed waveforms can be uploaded to the analyzer's generator section and then output directly to an FM transmitter. Audio Precision also has more complex encoded sweeps and test signals that are available for download and on disc.

Figure 6 shows a block diagram illustrating a complete FM receiver test setup. Only one mono channel is needed for the input to the FM transmitter, because the multiplexed waveform already includes both the left and right stereo channels. From the transmitter, the signal is fed to the FM receiver via a direct connection to minimize outside interference and to reduce spurious radiation from the transmitter. The main RF output is often an N connector, in which case an N-to-BNC adaptor will be needed, with a 50Ω inline BNC terminator to provide an appropriate load for the transmitter. A 50Ω BNC cable adapted to the receiver at one end completes the RF connection.

To calibrate the system, the transmitter is briefly driven by the audio test system to

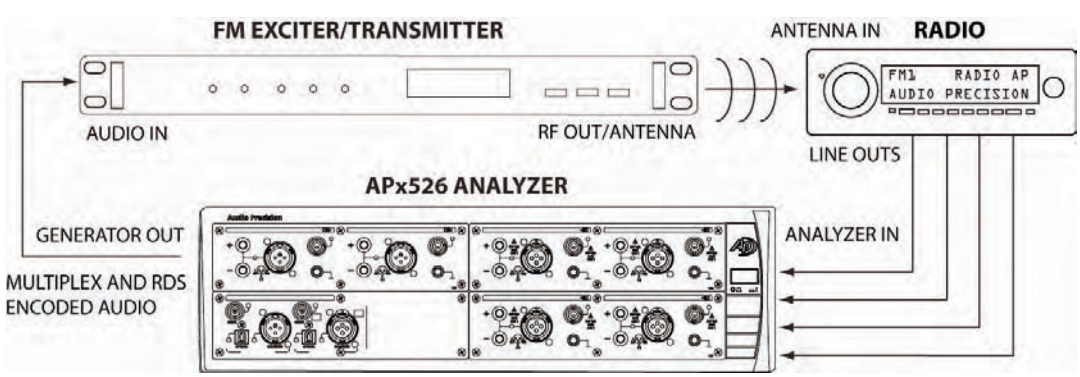


***Figure 6:** Block diagram illustrating an FM receiver test with an audio analyzer*

100% modulation (±75kHz deviation). This establishes the level of the FM stereo pilot and RDS signal. The audio signal should be reduced to the desired test level while leaving the pilot and RDS level unchanged.

The receiver is now tuned to the transmitter frequency and the transmitter's RF output is adjusted to provide sufficient level for full FM quieting, yet not so high as to overload the receiver's front-end. Since the transmitter in this suggested setup is directly connected to the receiver, a minimal RF level is needed.

Many receivers have an FM stereo indicator, an RDS indicator, or a signal strength meter to help determine sufficient signal strength. If an RDS message is being received and decoded by the receiver, it should be visible on the receiver's display (**Figure 7**).

Finally, the audio outputs of the radio receiver should be connected to the inputs on the audio analyzer being used for the tests. Typically, the audio outputs are unbalanced analogue on consumer tuners and receivers, and balanced on professional FM monitors. If a car radio without line-level outputs is being tested, then the speaker outputs should be connected to dummy loads and then to the balanced inputs on the audio analyzer.

Since an FM stereo signal is just two channels, it is only necessary to connect the first two channels of a multi-channel receiver in order to analyze the FM reception quality. A home receiver usually provides many ways to input a signal and its multi-channel functions are best tested independently of the FM reception. However, in the case of a car radio that has multiple outputs and no way besides FM to input test signals, a multi-channel audio analyzer that can simultaneously take measurements on all the outputs can be highly useful for both speeding up measurements, as well as revealing any crosstalk or interactions that may occur between channels.

Figure 7: *Radio receiver displaying RDS text*

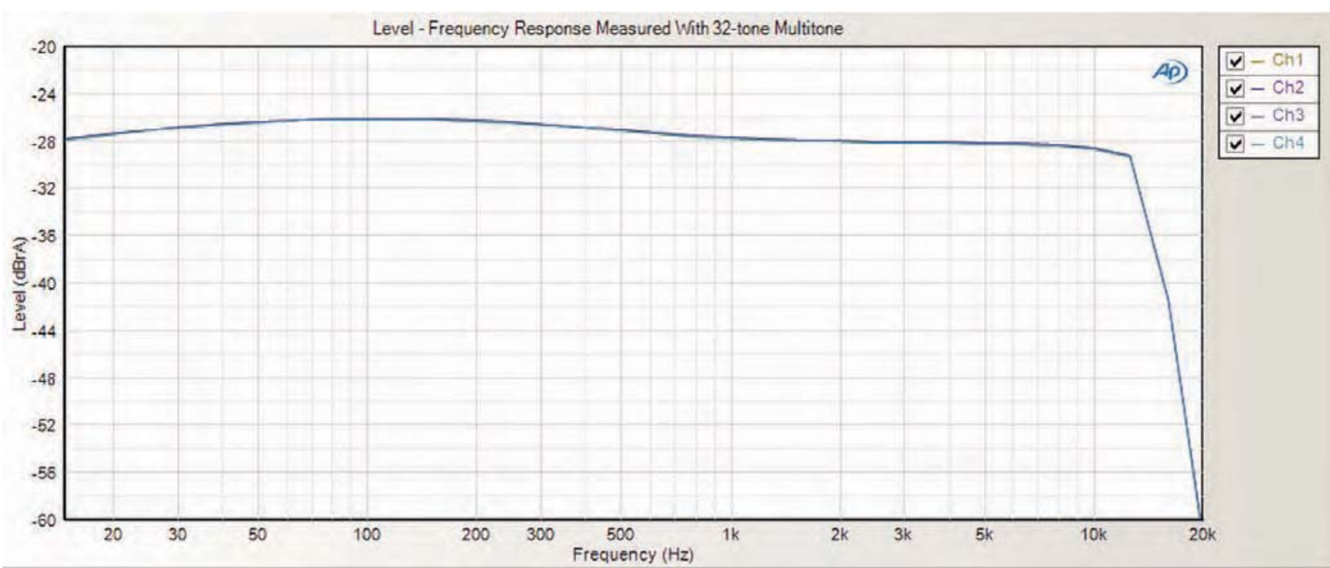
Points To Watch For

With the hookups completed, the generator and transmitter at the right level, and the receiver tuned to the correct frequency, it's now time to make measurements. Common audio test measurements include level, total harmonic distortion plus noise, phase, crosstalk, signal-to-noise ratio and frequency response. All frequency response measurements taken from an FM receiver will show a sharp high-end roll-off just before 19kHz, due to the FM multiplex filter (see **Figure 8**). When making crosstalk/stereo separation measurements, double check the transmitter specifications, as some transmitters have limitations in this area that may skew the test results.

Significant crosstalk in the transmitter or receiver can also affect THD+N measurements. This effect can be seen by selectively driving one or both channels with audio.

The exact measurements you take will depend on the analyzer you use, but we hope that this article will give you enough basic information to construct a test workflow that meets your requirements. Happy testing!

Figure 8: *Frequency response measurement*



Jean-Louis Evans, Managing Director at TÜV Product outlines the key stresses that may fail a product and gives pointers to engineers of how to secure product reliability

The Road to RELIABILITY

ELECTRONIC PRODUCTS and components need to be designed and produced in a way that ensures they will operate reliably when used. This is especially relevant in today's economic climate, as we see an increased focus on a longer product life and total cost of ownership, moving away from delivery price that was often the sales mantra pre-economic bust.

The new dawn brought on by the downturn calls for a more robust method of assuring product reliability prior to delivery. While total cost of ownership now being key to the buyer, how can producers of electronic goods and components ensure that they remain competitively priced, as well as deliver increased reliability? With time-to-market being a vital element of the sales

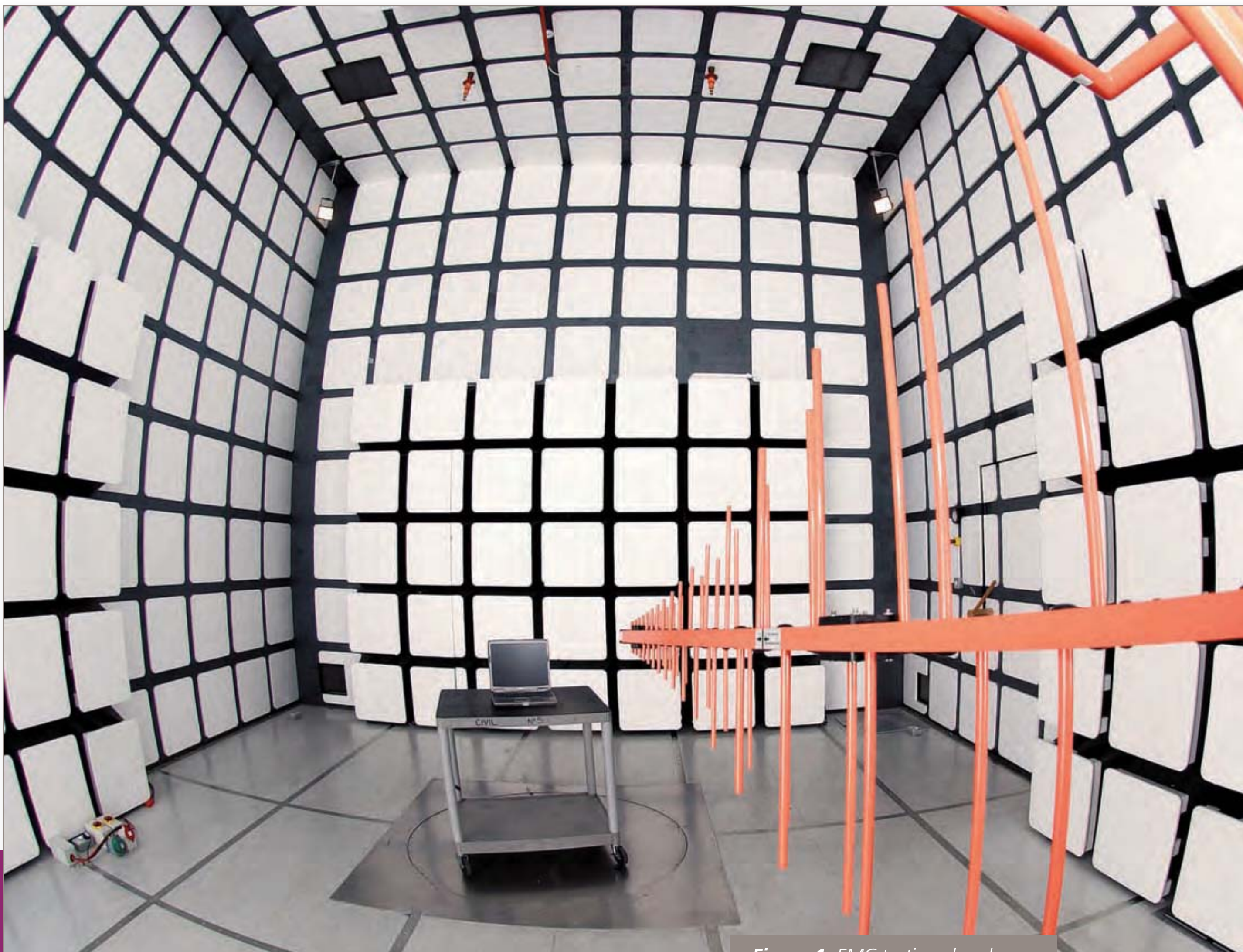


Figure 1: *EMC testing chamber*

Figure 2: *More robust methods of assuring product reliability are vital*

cycle, companies require techniques that are both fast and cost-effective, but that also produce worthwhile results. Clearly, the time required to obtain failure data must be considerably less than the expected life of the product.

Difficulties Facing Designers

A common difficulty facing design engineers working on electronic equipment is establishing exactly what is meant by reliability. A vast amount has been written about the definition and theory of reliability.

The term 'reliability' is internationally defined as "the ability of an item to perform a required function under stated conditions for a stated period of time".

1. The "required function" includes the specification of satisfactory operation, as well as unsatisfactory operation.
2. For a complex system, unsatisfactory operation may not be the same as failure. The "stated conditions" are the total physical environment including mechanical, thermal and electrical conditions.
3. The "stated period" of time is the time during which satisfactory operation is desired and is often called the "service life of a product".

To make matters more complex, depending on the application, different terms are used in the same context as reliability. For example, 'survivability' is the probability that an item will perform a required function under stated conditions for a stated period of time, but without failure.

It sounds confusing, but the difference between these two terms is that 'reliability' may be described qualitatively while survivability may be described quantitatively. Reliability can include the possibility of repair, whereas survivability applies only to applications in which failures are not routinely repaired.

To extend the reliability conundrum further, for items such as telecommunications equipment, where a measure of its reliability must include the possibility of repair as well as failure, then a measure of 'reliability' may well, in fact, be 'availability' instead. This applies in situations in which failures are routinely repaired, where 'availability' is a measure of the degree to which an item is in an operable state when called upon to perform.

A further dimension is that the other general measure of 'reliability' is 'maintainability'. This refers to the maintenance process associated with system reliability and is the degree to which an item can be retained in, or restored to, a specified operating condition.

However, 'maintainability' adds yet another layer of complexity to the issue of reliability with the element of human error which is difficult to fully include in the reliability testing. End users may find that while they maintain a product, as advised in the manufacturer's schedule, a product is still unreliable. In some circumstances, servicing periods are over specified and other parts within a product can be disturbed during the process, or the end user may not have the correct tools and be 'making do'. In such circumstances, maintainability actually introduces unreliability.

Reliability Testing

An early approach to evaluating the reliability of a product was design verification testing (DVT), also known as product assurance testing. This testing methodology was used to ascertain a product's reliability and was widely used by the new computer companies in the 1970s, which had huge laboratories continuously testing their complex systems over weeks and sometimes months.

Very simply, this was a series of tests devised to repeatedly show that the product would survive how it would be used. As a simple tool to demonstrate reliability, machines would be designed to automate the process, such as continuously pressing buttons on a keyboard.

Today, the more traditional approach of life cycle testing has evolved from DVT. This involves carrying out tests combining the product's expected environment with the actual operational conditions. The test process could also include a qualification test based on the predicted life cycle of the product.

The problem with this approach is that it is not time-to-market friendly, as it often has to fully replicate the total estimated usage time in order to precipitate failures. For example, if a five-year life cycle for a product is expected, a traditional reliability evaluation programme could require testing of 43,800 hours of usage. This would not only be costly, but also delay the product's entry into the marketplace. Waiting five years to bring a product to market simply isn't viable today. In reality, the market window for most products is small and, so, the time available for reliability evaluation of the product is typically days, or maybe weeks at best.

Also, if this kind of testing is performed at normal operational conditions, it is not likely to yield a statistically significant number of failures, unless a large number (tens of thousands) of products are tested. Indeed, for most components or sub-assemblies, full life-cycle testing is not practical because of the high costs involved. So, what are the alternatives?

Accelerated Life Testing and Environmental Stress Screening (ESS)

If the competitive marketplace requires that reliability testing needs be performed in only a few weeks, then a different test methodology is required. The answer for many electronics production and test programmes could be accelerated life testing and environmental stress screening. These have become increasingly accepted as methods of assessing product reliability before shipment. Indeed, they are now recognised by major multinationals operating in Europe and around the world as legitimate product reliability test methods. The key reasons are that they give a level of confidence that a product will not develop faults after delivery or in use and provide a process to identify any design defects, component problems or production-related issues.

As our reliance on electronic equipment and, therefore, on their reliability has become increasingly important, so ESS has become an established part of production processes. As it is widely accepted that failures are most likely to occur during the early operation of a product, this process stresses the equipment during the early stages of its life to highlight any problems so they can be quickly resolved. This 'infant mortality' phase helps to indentify defects that are caused during the manufacturing process.

Accelerated life testing is based on using real-life operational data and trying to accelerate fault conditions by applying key operational failure-causing stresses at levels above those that the product would experience in its application environment.

This accelerated ageing approach allows a distribution of failure times to be obtained, albeit at more stressful conditions than ordinary operating conditions. For example, test units are often operated continuously during a test when they do not operate continuously under normal 'real life' conditions. This means that failures are likely to be encountered earlier than if the units were tested at normal usage or, in some cases, by compressing the test time many failures can arise that wouldn't usually be seen during normal usage.

It is therefore important that these accelerated effects are taken into account when the test is formulated. This requires the distribution of failure times to be related to the failure times that would be anticipated under normal operational conditions. This would call for an accelerated life model to be created which is typically characterised by a linear relationship between failure times at different sets of conditions.

Operational Failure-Causing Stresses

The key operational failure-causing stresses that contribute most commonly to the impairment of a product's reliability are thermal cycling, vibration and fatigue, and power cycling.

Temperature cycling induces stresses within a product due to differential expansion of components and materials. Extending the temperatures (both high and low) to which a product is exposed accelerates creep due to coefficient of thermal expansion (CTE) mismatches within the product; the more extreme the temperature cycle, the higher the acceleration factor.

Vibration promotes mechanical failures due to cyclic stressing. The deterioration of material strength due to cyclic stressing is known as fatigue. If a product's operational vibration environment is known, then it may be accelerated too.

Putting a product through thermal and

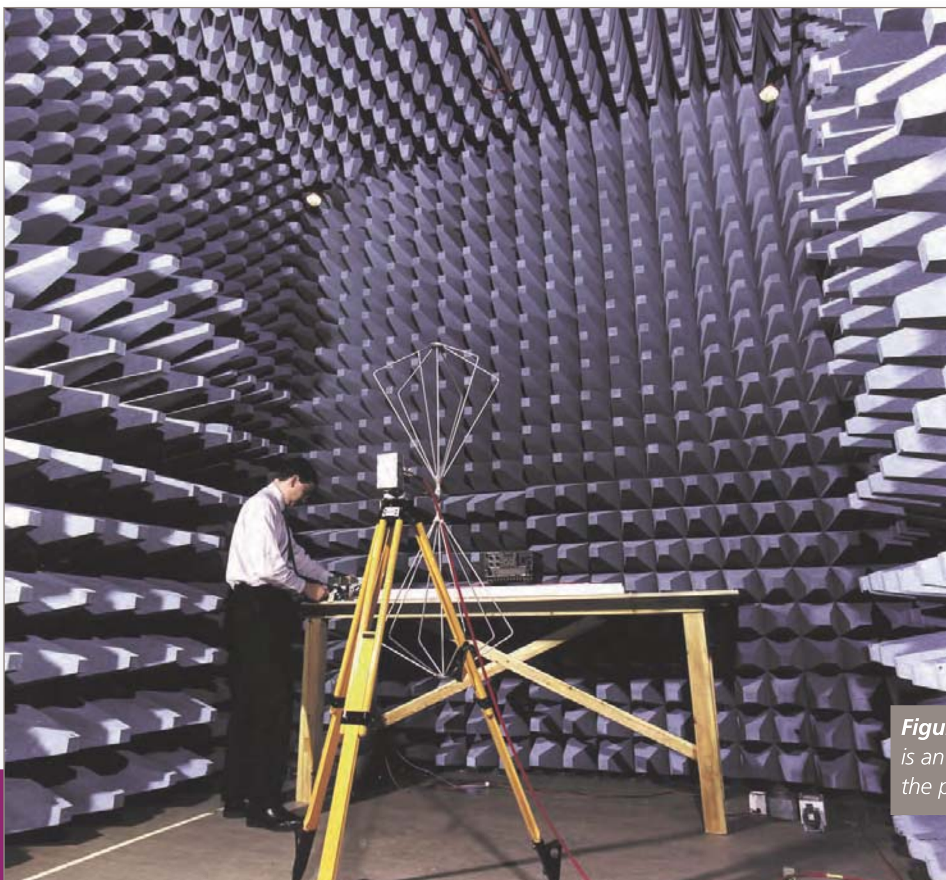
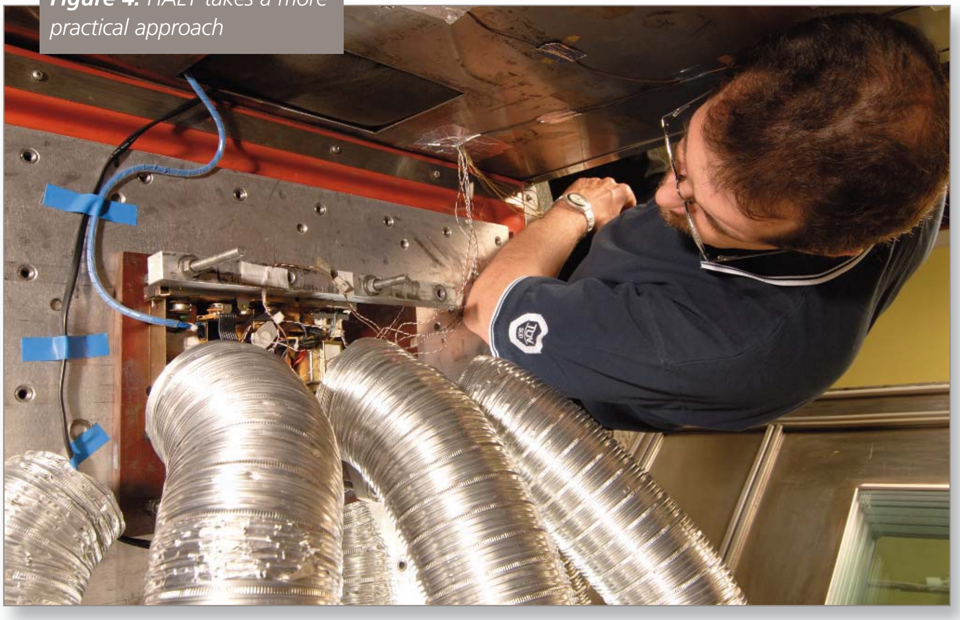


Figure 3: *Effective testing is an established part of the production process*

__Figure 4:__ HALT takes a more practical approach



vibration stresses in combination with power cycling will accelerate the discovery of a product's failure mode. It is vital to keep in mind that the test programme has to be devised and implemented in a way that should not damage the product due to extreme stresses.

The benefit of accelerated life testing is principally that it helps detect the design flaws which are most likely to give rise to a product's 'infant mortalities'. The disadvantage is that this method may precipitate some unrepresentative failures that cannot be predicted in a reliability test model, and Highly Accelerated Life Testing may, therefore, provide the answer here.

Highly Accelerated Life Testing

First developed in the US during the 1980s, highly accelerated life testing (HALT) takes a more practical rather than the predictive approach of accelerated life testing.

This method is actually an extension of accelerated life testing, but the test levels used are not based on operational data. Thermal and mechanical stimuli are applied separately and then together, in order to determine the operating and destruct limits of the item under test.

This testing methodology is particularly suited to products in the development or prototype stage. When, coupled with power cycling and product specific stresses, this test method has been proved to expose design flaws within hours when traditionally this has taken many days or weeks using the more conventional test methods.

A key difference between HALT and traditional accelerated life testing is that stress factors, such as high temperatures, are applied directly to the component or sub-assembly under test and not to the system as a whole. This can make a great difference in accelerating failure rates.

Defect analysis is a key stage in the HALT process and is conducted when the operation and destruct limits are known. The operating limit is defined as the point at which the unit remains operational, but any further increase in stress causes a recoverable failure. The destruct limit is the level at which the product stops functioning and remains inoperable. At this stage, all major flaws in the design should be exposed. Most may require a simple fix, some may require major modification, yet it may be considered that the design is sufficiently rugged and that no further action is required.

There is a common misunderstanding by engineers that HALT has a tendency to lead to 'over engineered' products. This is not the case. In fact, a HALT appraisal allows designers to establish the limitations of their product designs.

Reliability and Product Evolution

A common mistake when developing new versions of an existing product is that product reliability history can be relied on too much when assessing the reliability of the next generation. As a known product, there will be data from previous reliability tests, as well as in-service failure information from warranty returns.

It is, therefore, imperative that some form of gap analysis is performed between the known product currently available on the market and the new version under development. What can be perceived as the slightest alteration, such as the use of different plastics, more up-to-date electronic components, or a change in the manufacturing process, can have a significant impact on the product's reliability. The gap analysis data should then be mapped onto previous reliability information to gain a clearer understanding of the upgraded product's reliability.

Some of Life's Surprises

In reality, as much as can be done in the test laboratory, there is no accounting for end-user behaviour. Reliability testing focuses on performance of the product and not what the people might do to it or with it, which is very difficult to predict. Very often products are used in ways that the design engineers and testing never envisaged.

While all reliability tests can be fully explored in the laboratory, in an ideal world these should be taken a step further to include user tests in the field. Observations can then be made of how the product might be used and, as mentioned earlier, how maintenance will be managed. In the rush to release a product onto the market, this is a key part of reliability testing that is often overlooked. However, it is now widely recognised as a problem and we are increasingly seeing standards that try to compensate for this element of 'abnormal use'.

What's in a Name

Reliability is a difficult beast to tame, as time-to-market constraints require accelerated testing that cannot guarantee 100% reliability, and end-user behaviour cannot be predicted. However, it is a vital element to differentiate a product from the competition's. On an increasingly technologically level-playing field, today's market is all about brand reputation. A significant part of that reputation is created through reliable products that satisfy use and meet expectation. Never more so as a bruised world economy moves from a throw-away culture back to one that demands a long product life to maximise total cost of ownership. This raises the importance of reliability testing, as without it there is no assurance for designers, manufacturers and purchasers alike. ■

Propagation Study of GSM DIMENSIONS in Indoor

This article is in two parts. This is the second part, where **José Carlos Gamazo**, **Juan Blas**, **Rubén Lorenzo** and **Jaime Gómez**, from the Department of Signal Theory, Communications and Telematic Engineering at the University of Valladolid in Spain, present the material, methods, results and conclusion of the propagation study of GSM power in indoor environments. The first part was published in the last issue of *Electronics World*

THIS ARTICLE IS based on the application of an experimental system to measure the power of the electric field indoors. A robotic system is used to automatically position an antenna in a fixed grid within an environment. The collected data is then processed, analyzed and demonstrated graphically, in order to explain the 2D and 3D pattern of the electric power signal.

Finally, a concrete environment is studied and the measured data evaluated in order to characterize the electric field radiated by a GSM base station and to analyze its impact on the human body. The results show that the measured signals have space and temporal variability in a concrete point of their propagation, which produces slow and fast variations with the distance.

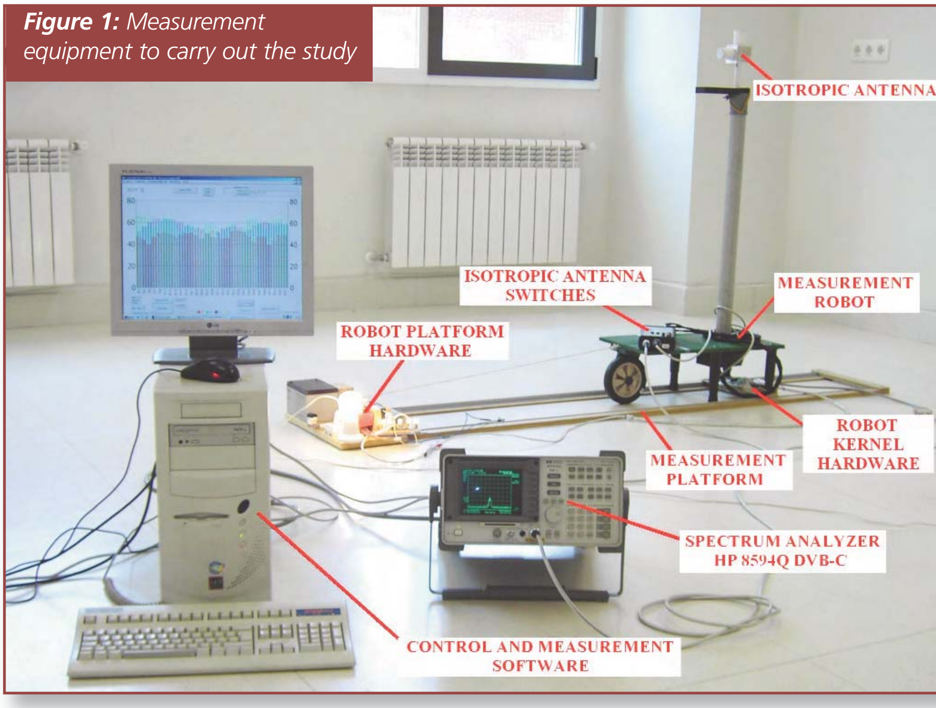


***Figure 1:** Measurement equipment to carry out the study*

The Measurement Equipment Used

The most important measurement equipment, besides an isotropic antenna and control probe switches (both made by Antennessa), is composed of two spectrum analyzers: Hewlett-Packard 8594Q DVB-C (9kHz-2.9GHz) and Rohde&Schwarz FSH3 (100kHz-3GHz) (see **Figure 1**).

The isotropic antenna consists of three probes (or monopole antennas). Probe 1 measures the vertical polarization of the GSM signal (Z direction) and probes 2 and 3 the horizontal polarization (X and Y directions, respectively). The antenna measures a range of frequencies from 100kHz to 3GHz, so that the structure of three orthogonal monopoles optimizes the operation and the isotropy of the three-dimensional probes in a wide range of frequencies (the antenna radiates or receives the same in all the directions, being ideally the radiation pattern a circumference in 2D or a sphere in 3D).

The electric field is measured by each monopole (in X, Y and Z), which can be written as in **Equations 1, 2** and **3**:

$$E_X = AF_X \cdot V_X \tag{1}$$

$$E_Y = AF_Y \cdot V_Y \tag{2}$$

$$E_Z = AF_Z \cdot V_Z \tag{3}$$

where E is the electric field measured in X, Y and Z directions, AF is the antenna factor of each monopole and V is the voltage measured in each space direction by the spectrum analyzer.

Once each one of the components of the electric field has been obtained (X, Y and Z), the total electric field (in volts per meter) can be calculated as it appears in **Equation 4**:

$$E_{TOTAL}\left(\frac{V}{m}\right) = \sqrt{E_X^2\left(\frac{V}{m}\right) + E_Y^2\left(\frac{V}{m}\right) + E_Z^2\left(\frac{V}{m}\right)} \tag{4}$$

The probe switch allows selecting one or another axis of the antenna by hand or by means of a software program. In addition, the switch contains an amplifier to improve sensitivity of the sensors to LF (Low Frequency). Then, the measured electric

Power in TWO Environments – Part 2

field can be written as in **Equation 5**:

$$E_i\left[dB\left(\frac{V}{m}\right)\right] = P_M(dBm) - 13 + |L| + AF(dBm^{-1}) \quad (5)$$

where i is the index X, Y or Z, PM is the measured power (in dBm), L is the losses of the wire and the switch, and AF is the antenna factor.

Figure 2 shows a schematic drawing of the location of the environment with respect to the electromagnetic field source, a base station of GSM-900 mobile phone. The angle whereupon this station is located with respect to the plane of the building facade (where there are two windows) is approximately 25º. In addition, the distance from the windows to the base station has been measured, obtaining 300m. It is important to say that the emission antennas are approximately the same height as the roof of the building (less than 10 meters over this environment).

The area of the environment to characterize has these dimensions: 4.77m in the X dimension and 4m in the Y dimension, presenting an area of approximately 19m^2 (see **Figure 3**).

The Main Criteria

Two objective criteria of evaluation have been applied in the comparative study. One of them is duration, with an assigned score according to the time measured, and the other one quality, with an evaluated score according to the simplicity with which the results of the measurements are interpreted, number of errors and so on.

This study is based on analyzing the 2D graphics obtained, similar to the graphs shown in **Figure 4** and **5**. Taking into account these considerations, the method and resolution which obtains the best balance of the score in both criteria will be chosen. Also, it is necessary to consider the duration of each measurement method, that is the time that the robot needs to move until the next sampling slot and the time necessary to take measurements in all three space directions.

In order to select the measurement method and the most appropriate grid resolution, one the following have been used:

- **Measurements method:** using the duration criteria, the method with the smaller measurement time will have the maximum score.
  - *One standard measurement:* it is the measurement that takes a lower time in realizing. It uses around six seconds for a measurement with the three probes (one measurement per probe).
  - *Arithmetic mean of three standard measurements:* nine measurements are taken (three per probe) in each sampling slot, and later (off-line) the arithmetic mean is computed (using a Matlab program). It uses 18 seconds.
  - *A measurement Video Avg using an acquisition time of 7 seconds:* it takes 26 seconds to realize three measurements (one per probe).
  - *A measurement Video Avg using an acquisition time of 4 seconds:* it takes 19 seconds to realize three measurements.
  - *A measurement Video Avg using an acquisition time of 1 second:* it takes 11 seconds to realize three measurements.
- **Grid resolutions:** 1cm, 3cm, 6cm and 10cm for the X direction; and 1cm, 5cm, 9cm, 13cm and 17cm for the Y direction (where the electromagnetic field pattern will have a bigger wavelength with respect to the X direction). Also, the necessary time for moving the robot between sampling slots has been measured. For example, the robot takes two seconds in moving in a grid of 1cm; five seconds in a grid of 3cm; eight seconds in a grid of 6cm and 12 seconds in a grid of 10cm in the X direction.

Measurements have been realized taking into account that the wavelength for GSM-900 (the central frequency used is 946.988MHz), see **Equation 6**:

$$\lambda = \frac{c}{f} = \frac{3\cdot 10^8}{946.988\cdot 10^6} \cong 0.3168m = 31.68cm \quad (6)$$

In addition, measurements have been taken with a fixed measurement method but varying grid resolutions (and number of samples) and vice versa, with a fixed resolution and varying measurements method. Using these measurements, 2D graphs have been obtained to realize the comparisons and the assessments in order to select the best method and resolution. Two examples of these 2D plots are shown in Figures 4 and 5.

In the graph shown in Figure 4, the arithmetic mean of the three standard measurements method has been used for

Figure 2: *Location of the studied indoor environment with respect to the location of the electromagnetic field source*

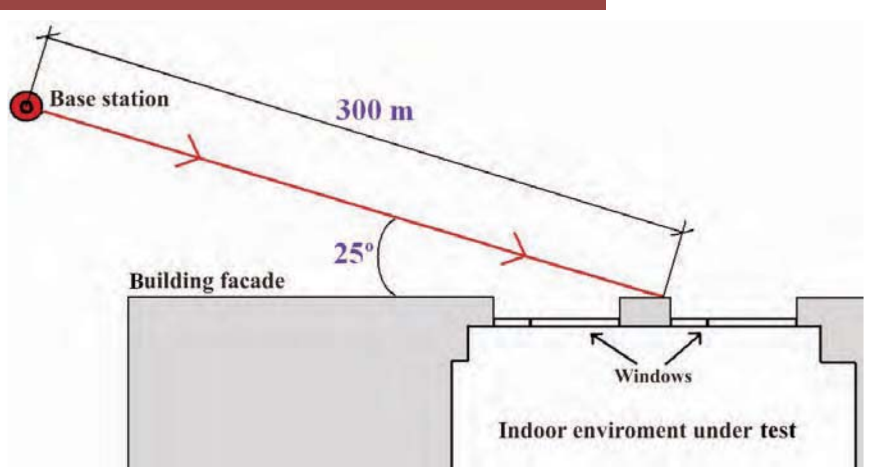


Figure 3: Plan view (in metres) of the selected area for the studied indoor environment

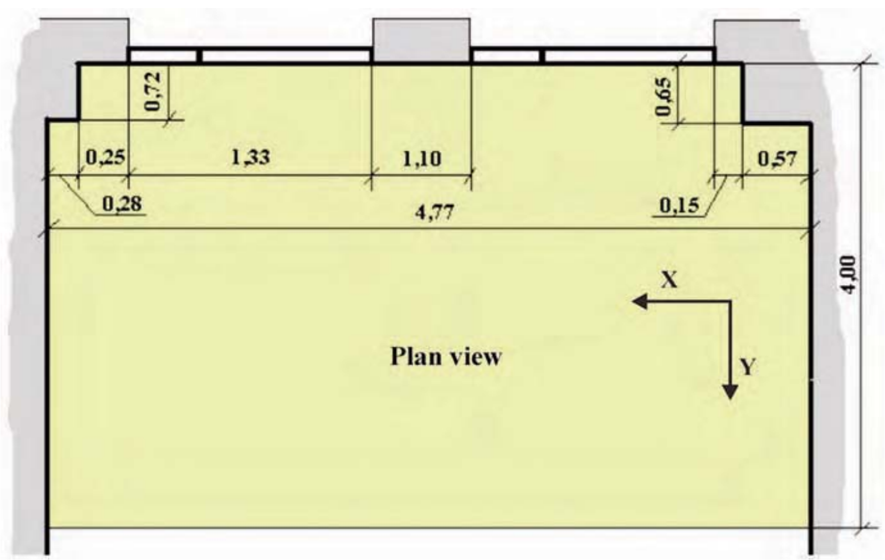
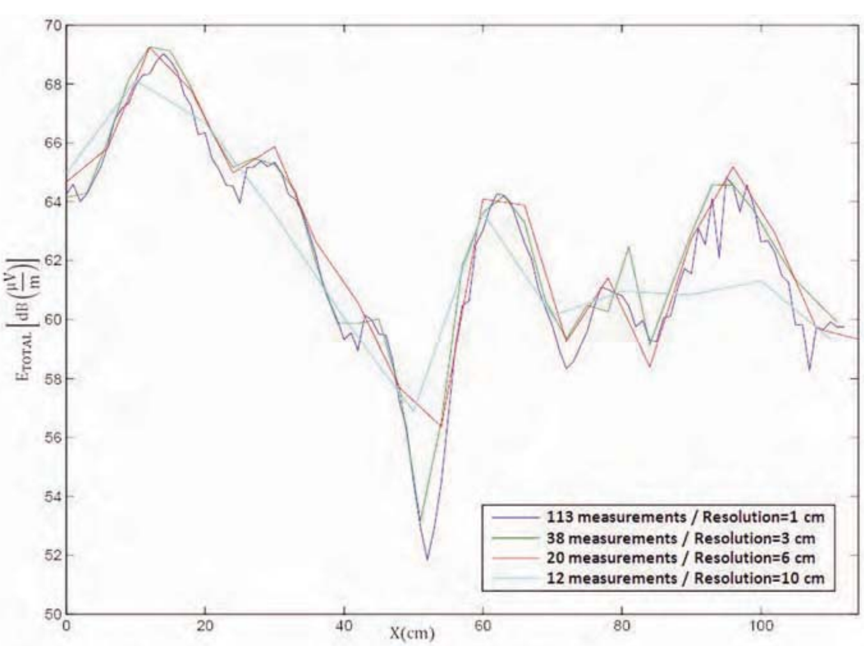


Figure 4: Electric field strength (dB [µV/m]) versus distance (cm) in the X direction. Evaluation of arithmetic mean of the three standard measurements method using four different values as grid resolutions



SLOTS NO. / RESOLUTION	T_M	T_D	T_T	$\%T_M$	$\%T_D$
113 / 1 CM	2,034 s	226 s	2.260 s	91%	9%
38 / 3 CM	684 s	185 s	869 s	79%	21%
20 / 6 CM	360 s	152 s	512 s	70%	30%
12 / 10 CM	216 s	132 s	348 s	62%	38%

Table 1: Measurement time (T_M), displacement time (T_D), total time (T_T) and $\%T_M$ and $\%T_D$ ratios with respect to T_T for the arithmetic mean of the three standard measurements method, using different slot numbers and grid resolutions

computing the total electric field power. The data have been measured with four different values of grid resolution: 1cm, 3cm, 6cm and 10cm.

In Figure 5 we have the total electric field plotted with a resolution of 3cm for different measurements method, for example one standard measurement, arithmetic mean of three standard measurements and Video Avg with several acquisition times (7s, 4s and 1s).

In **Table 1** we analyze the percentage of the measurement time (T_M) and displacement time (T_D) with respect to the total time (T_T) when the arithmetic mean of the three standard measurements method is applied for different grid resolutions. These percentages ($\%T_M$ and $\%T_D$) are obtained dividing T_M and T_D between T_T.

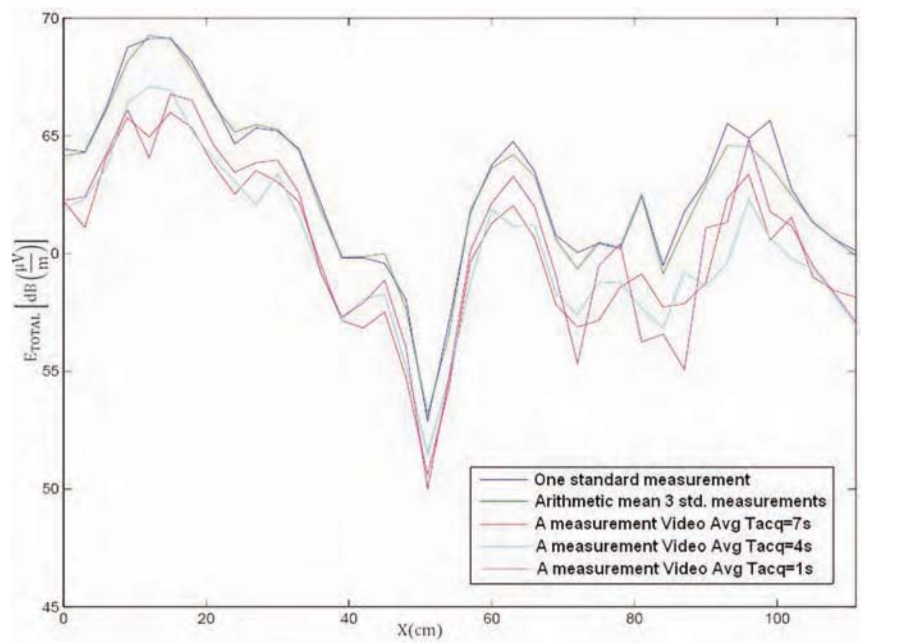
Studying the results in this table, it can be seen that the measurement time increases in inverse proportion to the displacement time, when a greater resolution is applied, so the total time also increases. Thus, in order to score the tests with different grid resolutions, a gradation can be established, considering that approximately all the percentages differ among them by 30% at the most, for example 38%-9% = 29% or 30%-21% = 9%. In addition, it is necessary to consider that whichever grid resolution is better, it takes a shorter time in moving the robot between measurement slots, but a greater number of measurements have to be acquired. Therefore, the best resolutions for $\%T_M$ and $\%T_D$ ratios are between 3cm and 6cm.

Finally, once all the measurements have been realized, the graphs with the electric field power have been obtained and the statistics of the measurement duration have been calculated and tables with the evaluation scores of the measurement results for each method and resolution have been constructed for two dimensions of the horizontal polarization (X and Y).

The tables have been done according to the measurement duration and measurement quality criteria. For example, weightings for each method and resolution evaluated in direction X are shown in **Tables 2** and **3**.

Analyzing Tables 2 and 3, the method and resolution which obtain the best balanced score in both criteria will be selected, that is, it must be good in both criteria (and not very good in one and very bad in another). The assigned scores go from 1 to 10 according to the following intervals: very bad, [1,3); bad, [3,5); medium, [5,7); good, [7,9) and excellent, [9,10].

Figure 5: *Electric field strength (dB [µV/m]) versus distance (cm) in the X direction. Evaluation of five different measurements method using a resolution of 3cm*



Taking into account these weightings, it could be said that the best grid resolution is between 3cm and 6cm (or between 20 and 38 sampling slots), since the total score is good (or medium-good) and these scores are balanced in both criteria. These conclusions agree with the obtained ones when Table 1 is analyzed.

But, on the other hand it is observed clearly that the measurement method which has obtained a better balanced score is the arithmetic mean of the three standard measurements method (good-excellent). This is followed by the Video Avg/4 s method, which has a worse total score (medium) than the one of the arithmetic mean, but it has scores balanced in both criteria, unlike the rest of the methods (that are good according to one criterion and bad according to another).

Similar conclusions for the Y direction can be obtained by means of the analysis of equivalent tables and graphs.

SLOTS NO. / RESOLUTION	DURATION CRITERION	QUALITY CRITERION	TOTAL SCORE
113 / 1 CM	very bad	excellent	medium
38 / 3 CM	medium	excellent	good
20 / 6 CM	good	medium	medium-good
12 / 10 CM	excellent	bad	medium

Table 2: *Scores for different sampling slot numbers (or grid resolutions), taking into account the measurement duration and measurement quality criteria*

MEASUREMENT METHOD	DURATION CRITERION	QUALITY CRITERION	TOTAL SCORE
ONE STANDARD MEASUREMENT	excellent	bad	medium
ARITHMETIC MEAN 3 STANDARD MEASUREMENTS	good	excellent	good-excellent
VIDEO AVG TACQ=7 S	bad	excellent	medium
VIDEO AVG TACQ=4 S	medium	medium	medium
VIDEO AVG TACQ=1 S	good	very bad	bad-medium

Table 3: *Scores for different measurements method having into account two criteria: measurement duration and measurement quality*

Useful Insight

This study provides a useful insight into the spatial and temporal variability of the electric field, which is derived from the use of wireless devices, with special emphasis on the mobile phone.

In a previous study it is verified that the most appropriate method is the arithmetic mean of three standard measurements with resolutions of 4cm and 7cm for the X and Y axis, respectively. Using this method, 198 measurement rows have been obtained (29 measurement points per row) and 50 hours were needed to complete the measurement.

Although the arithmetic mean of the three standard measurements method has been selected, the Video Avg/4s method could have been chosen as a second option, taking into account that the quality of the results is greater in the arithmetic mean method than in the Video Avg method for the same measurement duration (around 18s). In addition, Video Avg methods have the dependence on a functionality of a concrete spectrum analyzer, such as the automatic computing of the average of the samples during an acquisition period.

A Video Avg method is not a good option because it could be necessary for certain applications using an economic or less sophisticated analyzer, which may not feature this utility. This disadvantage does not affect to the arithmetic mean method, since samples are only acquired and their average is calculated off-line later.

In this study, the environment was divided in four sectors in order to acquire the samples. Each sector consists of 54 measurement rows and each row is split into 29 sampling points, which are separated by 4cm (that is 28 segments).

The measurement segment has a maximum length of 112cm (28 × 4cm). All the measurements have been realized within a time slot of 5 hours and 30 minutes (between 13:30 and 19:00), for this reason it can be considered that the GSM base station, whose central frequency is 946.988MHz, transmits with a similar electromagnetic power in that range of time.

Finally, 3D graphs for each probe of the isotropic antenna have been obtained with different values of azimuth (30° and 110°) and the same angle of elevation (50°). In addition, contour graphs, which result from 3D graphs, have been realized in order to identify the maximums and minimums of the signal clearly. In **Figure 6**, the 3D graph showing the total power of the electric field is presented.

Results Analysis

All things considered, the distribution of the electric field power and the standing wave

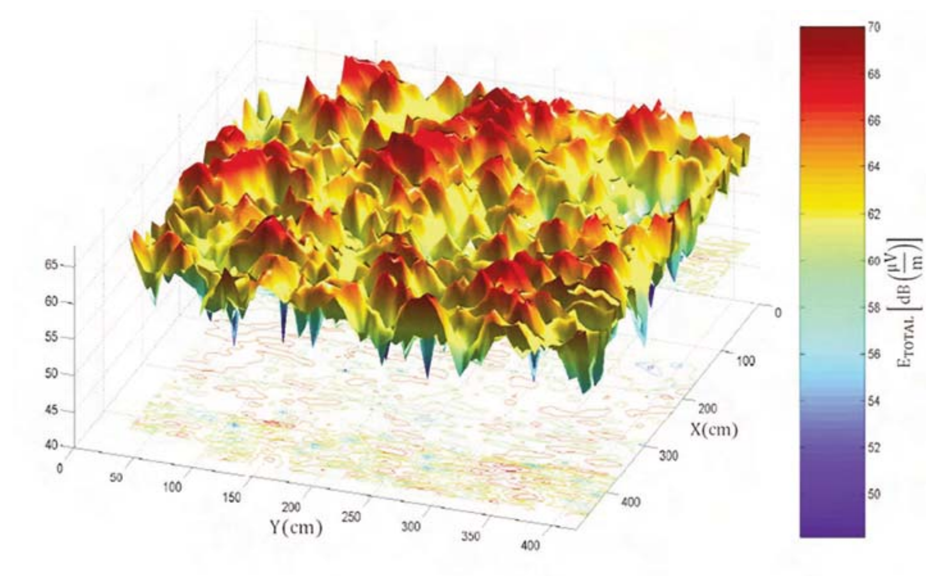


***Figure 6:** Three dimensional graph showing the total electric field (dB [μV/m]) in the indoor environment*

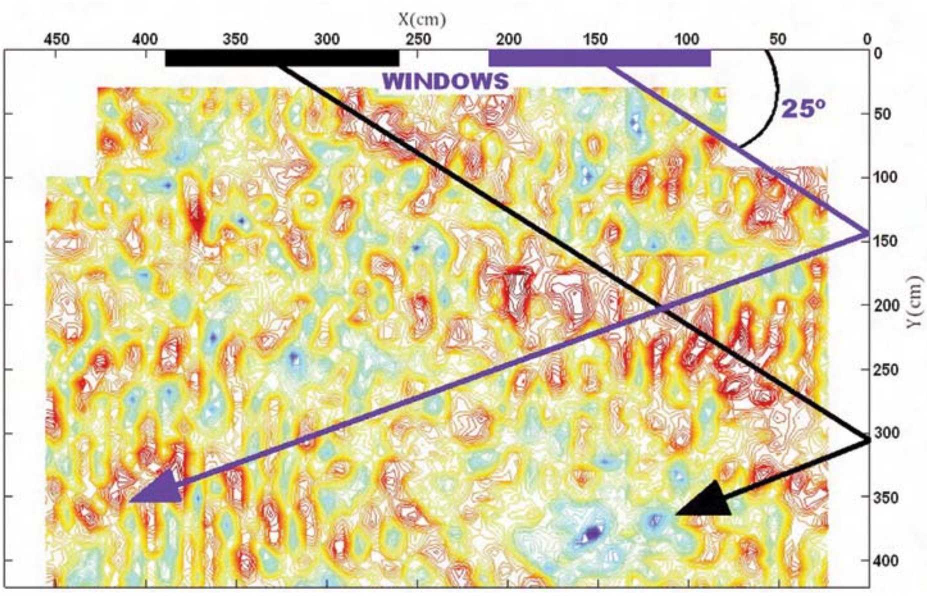


***Figure 7:** Two dimensional graph (contour graph) showing the electric field (dB [μV/m]) in the X and Y directions (cm)*

pattern are shown in Figure 6. Some parameters, such as the signal period or the peak power, can also be obtained from this graph.

Due to the existence of two windows in the environment, they can be considered as aperture antennas and they are the main radiation source inside the environment, thanks to the emitted radiation by the GSM base station. Then, using the Ray Theory, in the point where the main radiation beams of the "virtual antennas" (windows) come together, there are constructive interferences, that are maximums of power, as shown in brown/red in **Figure 7**. But, in the areas where the radio frequency power is smaller (areas near the left wall), there are destructive interferences and, therefore, minimums of power (coloured in yellow).

Likewise, when the possible risks involved in using radio transmitters are evaluated, some considerations must be taken into account. Firstly, the operational frequency could be considered, since the exhibition guides impose limits that vary with the frequency (the operational frequency is 946.988MHz in this article).

A second consideration to keep in mind is the transmitted power and the distance between the human body and the mobile device. The handheld devices (mobile phones, PDAs and so on) operate on low powers, but they are used near the body, whereas the devices mounted in vehicles operate with a greater power and the distance between the antenna and the body is also greater. So, when someone is exposed to the radio frequency energy, this influence can be measured in different ways.

If devices are used near the body, the most useful magnitude is SAR (Specific Absorption Rate). Several organizations have defined limits for the human exposure to the RF fields. Some of the most important are the IEEE's (Institute of Electrical and Electronics Engineers) or ICNIRP's (International for Commission Non-Ionizing Radiation Protection). A SAR value of 4W/kg, temporally and spatially averaged over the whole body mass, was accepted as the working threshold for adverse biological effects in humans. Above this limit value, disruption of work schedules in trained rodents and primates, and other adverse biological effects, have been demonstrated. Some hypothesis state that depositions in this range of power in human bodies would produce similar effects, although they have not been verified experimentally. For higher values of SAR, it could produce a thermal effect in the human body, equivalent to an increase as a result of intense exercising.

Finishing Touches

The developed method for realizing radio electric field analyses in environments works correctly, as predicted and in line with the theoretical models of propagation (Ray Theory, space-temporal models and so on). Thanks to the acquired samples, important conclusions have been obtained, such as the importance of spatial and temporal variability of the signals. This signal variability is known as Short-Term Fading or Multipath Fading. An automatic system (hardware and software) has been developed for studying indoor environments, which allows a fast and reliable characterization and simplifies the off-line analysis.

Both the methodology and the implemented system can be used to characterize the distribution of the radiated electric field by a GSM base station (or other radiating devices, such as repeaters, electric transformers and so on), and to be able to analyze the impact on the human body, comparing the field distribution in presence or absence of people in the environment under test. ■

If you missed the first part of this article in the last issue of Electronics World, you can order it now by going online at ***www.electronicsworld.co.uk***

Professor Stojce Dimov Ilcev from the Durban University of Technology (DUT) explains the factors that engineers and designers need to consider when creating antenna hardware design for global mobile satellite communications systems

This is a two-part article, with the first part now available online at ***www.electronicsworld.co.uk***

Antenna Systems for Mobile SATELLITE Applications – Part 2

THE CONSIDERATION of antenna transmission is inevitable, especially in Global Mobile Satellite Communications (GMSC), where their propagation characteristics are much affected by different and changeable local environments during movement, and differ greatly from those observed in fixed satellite systems.

To create an adequate antenna hardware design for mobile GMSC systems, engineers have to consider all of the related factors in order to realize full mechanical and transmission potentials. This article describes the radiation and transmission characteristics of mobile antenna systems for Maritime Mobile Satellite Communications (MMSC), Aeronautical Mobile Satellite Communications (AMSC) and Land Mobile Satellite Communications (LMSC).

Radiation Pattern, Beamwidth and Sidelobes

In principle, a calculation of the radiation is possible if the electromagnetic (EM) field can be described quantitatively at all points of the antenna surface, whose boundaries are those of the apertures. Here we consider the radiation pattern from a circular aperture as this type antenna has generally been used in MSC, especially in MMSC. This should give an insight into the characteristics of mobile antennas.

For an antenna that generates a single focused beam, the principal parameter affecting the antenna radiation pattern E(θ, ϕ), after the aperture size (a), is the aperture illumination distribution Ea(r, ψ), which is the amplitude of the far field radiation pattern E, at the point (θ, ϕ), this being essentially the Fourier transform of the illumination distribution, given by:

$$E(\theta, \phi) = 1/\pi a^2 \int_0^{2\pi} \int_0^{a} E_a(r, \psi) \exp [-jkr \sin \theta \cos (\phi - \psi)]\, r dr d\psi \qquad (1)$$

An example of **Equation 1** can be to consider antenna solutions employed in MSC for all applications, which utilizes a circular aperture and where for circularly symmetric aperture illumination distribution this relation reduces to:

$$E(\theta) = 2/a^2 \int_0^{a} E_a(r)\, J_0 (kr \sin \theta \cos (\phi - \psi))\, r dr \qquad (2)$$

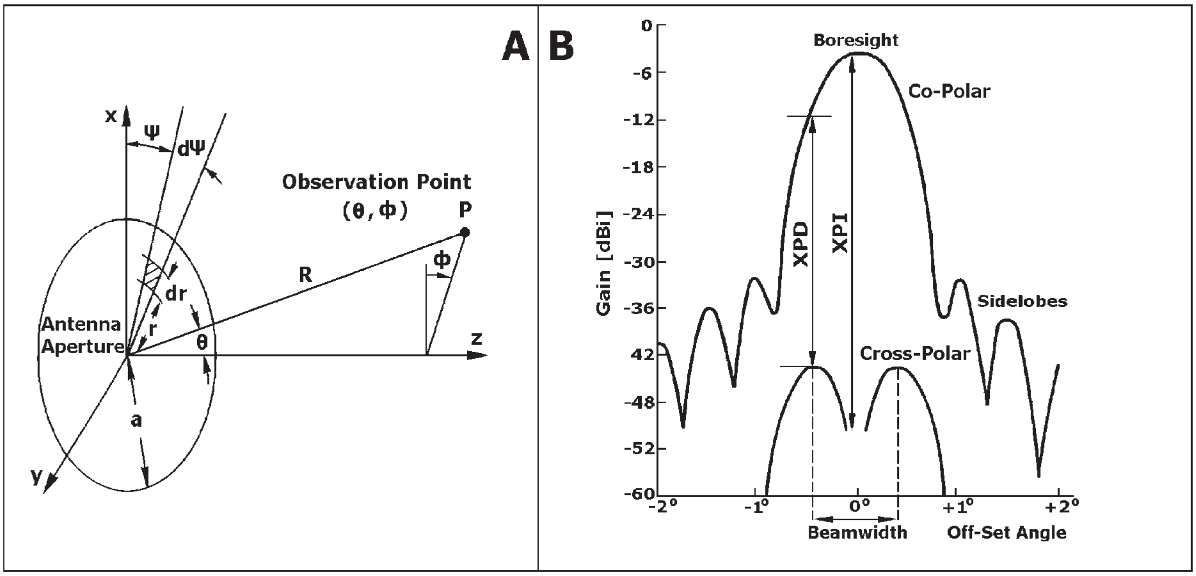
where a = d/2 denotes the radius of antenna aperture; J_0 is the first kind and order zero of the Bassel function and k = 2 π/2 denotes the wave number. The other notations that represent distance and angles in coordinates are defined as in **Figure 1 (left)**. The antenna radiation pattern is three-dimensional in nature, so it usually has to be represented from the point of view of a single-axis plot.

The characteristics of the MES antenna radiation pattern affect interference levels directly. Any improvement in the pattern will, therefore, be fully reflected in the interference level. Such improvement constitutes a very effective means of solving interference problems. To improve the pattern, one can either increase the antenna diameter or, with a constant diameter, use a specific technique for reducing the sidelobes. This method is, therefore, applicable when the MSC network is in the initial stages of development.

The antenna gain is normally calculated with reference to the boresight, i.e. the direction at which the maximum antenna gain occurs, in the case of θ, ϕ = 0º. Gain is usually expressed in dBi, where the component 'i' refers to the fact that it relates to the isotropic gain. In a dual polarization frequency re-use satellite communication system, what's important is the "polarization discrimination" between the co-polar and cross-polar signals, especially in the antenna main beam region, see **Figure 1 (right)**.

An important parameter used in an antenna's specification is the beam width evaluated by Half Power Beam width (HPBW) 2θHP, where θHP is the half-power angle when radiated power becomes

Figure 1: *Geometrical parameters of antenna pattern (left) and gain characteristics (right)*
[Courtesy of Book: "Satellite Communication Systems" by B.G Evans]



half the maximum level -3dB. The HPBW (θ_0) is given by the following equation:

$$\theta_0 = 65\ (\lambda/d) \tag{3}$$

Here, it is possible to realize that the half-power bandwidth is inversely proportional to the operating frequency and the diameter of the antenna. For example, a 1m receiver antenna operating in the C-band (4GHz) has a 3dB bandwidth of roughly 4.9°, while the same antenna operating in the Ku-band (11GHz) has a 3dB bandwidth of approximately 1.8°.

The antenna systems have co-polar and cross-polar gains, where the reception of unwanted, orthogonally polarized cross-polar signals will add to the co-polar signal as interference. The ability of an antenna to discriminate between a wanted polarized waveform and its unwanted orthogonal component is termed as its Cross-Polar Discrimination (XPD). When dual polarization is employed and the antenna's ability to differentiate between the wanted polarized waveform and the unwanted signal of the same polarization, introduced by the orthogonal polarized wave, it is termed Cross-Polar Isolation (XPI). In this context, an antenna would typically have an XPI > 30dB.

The level of the antenna pattern's sidelobes is also important, as this tends to represent gain in an unwanted direction. For a transmitting gain this leads to the transmission of unwanted power, resulting in interference to other systems, or in the case of a receiving antenna, the reception of unwanted signals or noise. The sidelobe characteristic of MES is one of the main factors in determining the minimum spacing between satellites and, as such, the orbit and spectrum utilization efficiency. The ITU-R S.465-5 recommendation gives a reference radiation diagram for use in coordination and interference assessment, which is defined by:

$$G = 32 - 25 \log \phi \text{ [dBi] for } \phi_{min} \le \phi < 48^\circ$$

$$= 10 \text{ dBi for } 48^\circ \le \phi \le 180^\circ \tag{4}$$

where G is the gain relative to an isotropic antenna; ϕ is the off-axis angle referred to the main lobe axis and $\phi_{min} = 1^\circ$ or $100\lambda/d$ degrees, whichever is greater. In this context, most of the effective power radiated by an antenna is contained in the so-called main lobes of the radiation pattern, while some residual power is radiated in the sidelobes.

Sidelobes are an intrinsic property of antenna radiation and diffraction theory shows that they cannot be completely suppressed. However, sidelobes are also due partly to antenna defects which can be minimized by proper design.

Conversely, due to the reciprocity theorem, the receive antenna gains and radiation patterns at the same frequency, are identical to the transmit antenna gains and radiation patterns. Unlikely, unwanted power can also be picked up by the antenna sidelobes during reception.

For large satellite antennas, with a diameter over 100λ (wavelengths), a reference radiation pattern is recommended by the CCIR for interference to and from other satellite and terrestrial communication systems. At this point, the diameters of the vehicle antennas under discussion are usually below five wavelengths in the L-band. Further CCIR action is expected to define a reference radiation pattern for mobile antennas in MSC.

Polarizations and Axial Ratio

The antenna and the EM field received or transmitted have polarization properties. Thus, the polarization of an EM wave describes the shape and orientation of the locus of the extremities of the field vectors as a function of time. A wave may be described as linearly, circularly or elliptically polarized. Linear polarization is such that the electric E-field is oriented at a constant angle as it is propagated that can be either vertical or horizontal.

If a plane wave is propagated along the z axis and electric field (E) is on the x-z or y-z planes, the relations for linear vertical and horizontal polarization can be written as follows:

$$E_x = E_a \cdot e^{j(\omega t\text{-}kz+\phi a)} \text{ and } E_y = E_b \cdot e^{j(\omega t\text{-}kz+\phi b)} \quad (5)$$

where E_a, ω, k and ϕ_a denote the maximum amplitude of electric field, angular frequency (2πf), wave number and initial phase respectively, while Eb and ϕ_b are the maximum amplitude and the initial phase of the wave.

Circular polarization is the superposition of two orthogonal linear polarizations, such as vertical and horizontal, with a 90º (π/2) phase difference. The tip of the resultant E-field vector may be imagined to rotate as it propagates in a helical path. There is a Left-Hand Circularly Polarized (LHCP) wave with anticlockwise rotation and a Right-Hand Circularly Polarized (RHCP) wave with clockwise rotation.

An elliptically polarized wave may be regarded as the result either of two linearly or two circularly polarized waves with opposite directions. This type of polarization is the case when the amplitudes and phase difference between the two waves are not equal (π/2).

As discussed before, the signal fields can contain co- and cross-polar components. In this way, the cross-polarization of a source becomes of increasing interest to the MSC antenna designers.

In the case of Tx or Rx antennas with a linearly polarized field, the cross-polar component is the field at right angles to this co-polar component. Namely, if the co-polar component is vertical, then the cross-polar component is horizontal. Circular cross-polarization is that of the opposite hand to the desired principal or reference polarization. Impure circular polarization is, in fact, elliptical. The level of impurity is measured by the elliptical polarization and known as the Axial Ratio (AR). The AR can be defined as the ratio of the major axis electric component to that of the minor axis by:

$$|AR| = |E_1/E_2| \ (1 \leq |AR| \leq \infty) \quad (6)$$

The signal for AR denotes the rotation's direction, however an absolute value is usually used to evaluate circular polarized radiated waves and can be expressed in decibels by the following equation:

$$|AR| = 20 \cdot \log (|E_1/E_2|) \text{ [dB] for } (0 \leq |AR| \leq \infty) \quad (7)$$

Accordingly, the AR is determined by the performance of the antenna, so the AR is one of the most important parameters of circular polarized antennas. It can easily be understood that the AR depends on the direction with respect to the axis of the antenna. In general, the AR is best (smallest) in the boresight direction and becomes progressively worse further away from the boresight.

Circular polarized waves are used in order to eliminate the need for polarization tracking. RHCP has been used in the Inmarsat transmission system. The aperture antenna, such as the parabolic reflector antenna, is commonly used as a shipborne antenna in the current Inmarsat-B terminal, an axial ratio of below 1.5dB in the boresight direction is so easy to achieve that polarization mismatch loss is almost negligible. In the case of phased array antennas, a degradation of the axis ratio caused by beam scanning must be taken into account.

Figure of Merit (G/T) and EIRP

Although gain is an essential factor in considering antennas, the figure of merit ratio of a gain-to-noise temperature (G/T) is more commonly specified from the standpoint of MSS and satellite systems in general.

The figure of merit for the receiving station is defined as the ratio between the gain of the antenna in the direction of the receiving signal and the receiving system noise temperature; the gain-to-noise temperature ratio (G/T) is generally given for the maximum gain derived from the following formula:

$$G_{max} = P_{max}/P0/4\pi = 10\log G \text{ dB} \quad (8)$$

The G_{max} is often called the antenna gain expressed in dB, where the total radiated power in all directions can be determined by the following integration:

$$P_0 = \int_0^{2\pi}\int_0^{\pi} P(\theta, \phi) \sin\theta \, d\theta \, d\phi \quad (9)$$

The G/T value is expressed in decibels per Kelvin dB(K-1) by the following equation:

$$(G/T) = 10\log G - \log T_{SA} = 10\log G - \log T_S \ \text{dB}(K^{-1}) \quad (10)$$

The Earth station G/T typical values range from 35dB(K^{-1}), for instance an LES receive antenna with a 15 to 18m diameter has some 15.5dB(K^{-1}). The G/T is a very important parameter of an Earth station, so the methods used for its measurement and the contribution to the noise temperature are the subject of the ITU-R S.733 Recommendation.

The noise temperature measured at the terminals of antenna pointed to the sky depends upon the frequency of operation, elevation angle and the antenna sidelobe structure. In more formal terms, the noise temperature will be derived from a complete solid angle integration of the noise power received from all noise sources (terrestrial and galactic) and determined for clear weather conditions by the following integral:

$$T_A = 1/4\pi \int_\Omega P(\theta, \phi)\, T(\theta, \phi)\, d\theta \, d\phi \quad (11)$$

Thus, to produce a low noise antenna, its sidelobes must be minimized, especially in the direction of the Earth's surface, where T = noise temperature.

The total noise temperature of the system (T_{SR}) at an input port of receiver LNA or at the antenna output (T_A), taking account of losses caused by tracking, feed lines and a radome is defined by:

$$T_{SR} = T_R + T_a (1 - 1/a) + T_A/a \text{ or } T_{SA} = T_A + T_a (a - 1) + a\, T_A \quad (12)$$

where T_R is the noise temperature of the receiver (LNA), with a typical value of about 80K to 100K in the L-band; T_a is the temperature of the environment of about 300K; L_f is the total loss of feed lines and components such as diplexer, cables and phase shifters if a phased-array antenna is used; a = attenuation expressed as a power ratio (a ≥ 1 or in decibels a_{dB} = 10log a); T_A is the antenna noise temperature that comes from such effects as the ionosphere and the Earth, which value of about 200K depends on factors such as frequency and bandwidth and T_{SA} = antenna with a noise temperature. In such a manner, the noise of the antenna temperature must be kept as low as possible by a proper solution of special design, in order to obtain a high figure of merit (G/T).

With reference to the previously expressed formula ($P_{id} = P_{in}/4\pi r^2$) of transmitting antenna power density on the spherical surface, if it has a transmitting gain GT and where Pin is equal to the transmitted power PT, the power density PD can be written as:

$$P_D = G_T \cdot P_T/4\pi r^2 \quad W/m^2 \qquad (13)$$

where ($G_T \cdot P_T$) related values are considered to be the radiation power transmitted by an ideal type of omnidirectional antenna. Therefore, this term is considered as an EIRP, which can be expressed in antilogarithm and decibel expressions respectively, as follows:

$$EIRP = G_T \cdot P_T \text{ [W] and } EIRP = [G_T] + [P_T] \text{ dBW} \qquad (14)$$

The EIRP value is an important parameter in evaluating the transmitting performance of an MES terminal including an antenna. However, the EIRP amount (dBW) is defined by the sum of the antenna gain (dB) and the output power of HPA (dBW), taking account feed losses such as feed lines, cable and a diplexer.

Compact and Lightweight Design

The design and configuration of MSA needs to be compact and lightweight, especially for LMSC systems. On the other hand, the physical characteristics for MMSC and AMSC applications may be quite different, but both have to be designed compact for harsh environments and very extreme operating temperatures. These requirements will be difficult to achieve because the compact antenna has two major electrical disadvantages such as low gain and wide beam coverage, and because directional antenna has very heavy components for satellite tracking and getting satellites into focus. However, a new generation of powerful satellites with high EIRP and G/T performances should permit the design of compact and lightweight MSA.

In such a way, new physical shapes and less weight are very important requirements in connection with compactness and lightweight, which will permit easier installation and maintenance. Shipborne antennas still have very big dimensions, especially those integrated in Inmarsat Standard B and Fleet 77. The new Inmarsat antennas for FleetBroadband are getting smaller dimensions and can be employed for communications and multimedia transmissions.

The Swift64 airborne antenna is well suited for large jumbo jets, which installation requirements are not as limited compared to very small aircraft and helicopters. However, new aeronautical SwiftBroadband can be installed even on small jets with reduced space on fuselage. A phased array MSA is considered to be the best prototype for aircraft and helicopters because of its very low profile, convenient mechanical strength and easy installation. ■

PLC with PIC16F648A Microcontroller

Part 19

Professor Dr Murat Uzam from Nigde University in Turkey presents a series of articles on a project that focuses on a microcontroller-based PLC. In this article he describes priority encoder macros

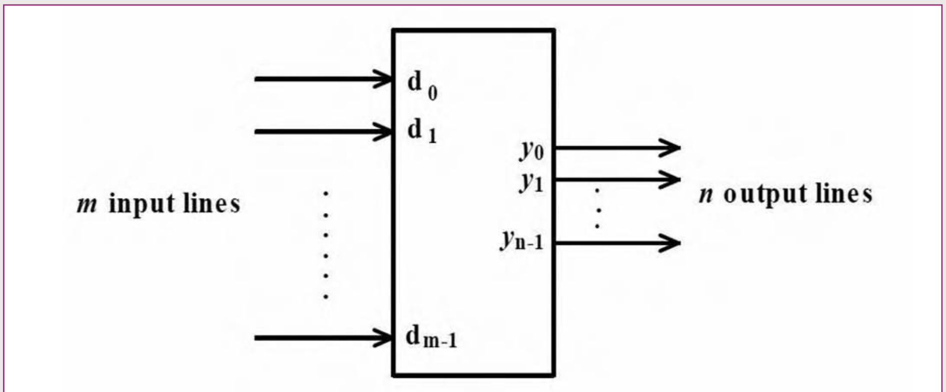


***Figure 1:** The general form of an m-to-n encoder, where $m = 2^n$*

HERE, THE FOLLOWING priority encoder macros are described: encod_4_2_p (4×2 priority encoder), encod_4_2_p_E (4×2 priority encoder with Enable input), encod_8_3_p (8×3 priority encoder), encod_8_3_p_E (8×3 priority encoder with Enable input), encod_dec_bcd_p (decimal to BCD [Binary Coded Decimal] priority encoder), encod_dec_bcd_p_E (decimal to BCD priority encoder with Enable input).

Four examples will be provided in the next article to show the applicability of these priority encoder macros.

Priority Encoder Macros

An encoder is a circuit that changes a set of signals into a code. As a standard combinational component, an encoder is almost like the inverse of a decoder where it encodes a 2^n-bit input data into an n-bit code. The encoder has $m = 2^n$ input lines and n output lines, as shown by the general form of an m-to-n encoder in **Figure 1**.

For active high inputs, the operation of the encoder is such that exactly one of the input lines should have a 1, while the remaining input lines should have 0s. The output is the binary value of the index of the input line that has the 1. It is assumed that only one input line can be a 1.

Encoders are used to reduce the number of bits needed to represent some given data either in data storage or in data transmission. Encoders are also used in a system with 2^n input devices, each of which may need to request for service.

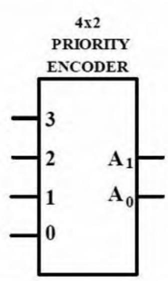
One input line is connected to one input device. The input device requesting for service will assert the input line that is connected to it. The corresponding n-bit output value will indicate to the system which of the 2^n devices is requesting for service. However, this only works correctly if it is guaranteed that only one of the 2^n devices will request for service at any one time. If two or more devices request for service at the same time, then the output will be incorrect.

To resolve this problem, a priority is assigned to each of the input lines so that when multiple requests are made, the encoder outputs the index value of the input

Macro

```
;--------- macro: encod_4_2_p -
encod_4_2_p   macro    reg3,bit3,
reg2,bit2,reg1,bit1,reg0,bit0,
regA1,bitA1,regA0,bitA0
        local    L1,L2,L3,L4
        btfss    reg3,bit3
        goto     L4
        bsf      regA1,bitA1
        bsf      regA0,bitA0
        goto     L1
L4      btfss    reg2,bit2
        goto     L3
        bsf      regA1,bitA1
        bcf      regA0,bitA0
        goto     L1
L3      btfss    reg1,bit1
        goto     L2
        bcf      regA1,bitA1
        bsf      regA0,bitA0
        goto     L1
L2      bcf      regA1,bitA1
        bcf      regA0,bitA0
L1
        endm
;------------------------------
```

Symbol



3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A1 =	regA1,bitA1
A0 =	regA1,bitA0

Truth table

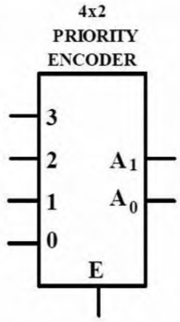
inputs				outputs	
0	1	2	3	A1	A0
x	x	x	1	1	1
x	x	1	0	1	0
x	1	0	0	0	1
1	0	0	0	0	0

x: don't care

***Table 1:** The macro "encod_4_2_p" together with its symbol and truth table*

Macro	Symbol	Truth table

```
;--------- macro: encod_4_2_p_E -
encod_4_2_p_E  macro   reg3,bit3,
reg2,bit2,reg1,bit1,reg0,bit0,
regA1,bitA1,regA0,bitA0
        local   L1,L2,L3,L4
        movwf   Temp_1
        btfss   Temp_1,0
        goto    L2
        btfss   reg3,bit3
        goto    L4
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L4      btfss   reg2,bit2
        goto    L3
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L3      btfss   reg1,bit1
        goto    L2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L2      bcf     regA1,bitA1
        bcf     regA0,bitA0
L1
        endm
;--------------------------------
```



W	E
3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A1 =	regA1,bitA1
A0 =	regA1,bitA0

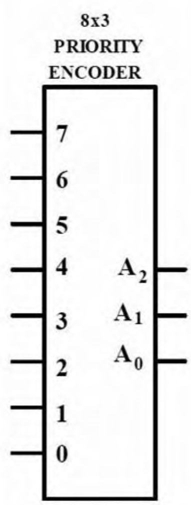
inputs					outputs	
E	0	1	2	3	A1	A0
0	x	x	x	x	0	0
1	x	x	x	1	1	1
1	x	x	1	0	1	0
1	x	1	0	0	0	1
1	1	0	0	0	0	0

x: don't care

***Table 2:** The macro "encod_4_2_p_E" together with its symbol and truth table*

Macro	Symbol	Truth table

```
;--------- macro: encod_8_3_p -------
encod_8_3_p  macro   reg7,bit7,
reg6,bit6,reg5,bit5,reg4,bit4,
reg3,bit3,reg2,bit2,reg1,bit1,
reg0,bit0,regA2,bitA2,regA1,
bitA1,regA0,bitA0
        local   L1,L2,L3,L4,L5,L6,L7,L8
        btfss   reg7,bit7
        goto    L8
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L8      btfss   reg6,bit6
        goto    L7
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L7      btfss   reg5,bit5
        goto    L6
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L6      btfss   reg4,bit4
        goto    L5
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L5      btfss   reg3,bit3
        goto    L4
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L4      btfss   reg2,bit2
        goto    L3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L3      btfss   reg1,bit1
        goto    L2
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L2      bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
L1
        endm
;-----------------------------------
```



7 =	reg7,bit7
6 =	reg6,bit6
5 =	reg5,bit5
4 =	reg4,bit4
3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A2 =	regA2,bitA2
A1 =	regA1,bitA1
A0 =	regA1,bitA0

inputs								outputs		
0	1	2	3	4	5	6	7	A2	A1	A0
x	x	x	x	x	x	x	1	1	1	1
x	x	x	x	x	x	1	0	1	1	0
x	x	x	x	x	1	0	0	1	0	1
x	x	x	x	1	0	0	0	1	0	0
x	x	x	1	0	0	0	0	0	1	1
x	x	1	0	0	0	0	0	0	1	0
x	1	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0

x: don't care

***Table 3:** The macro "encod_8_3_p" together with its symbol and truth table*

line with the highest priority. This modified encoder is known as a priority encoder. In this article, we discuss the priority encoders.

Although, not shown in Figure 1, the priority encoder may have an enable line, *E*, for enabling it. When the priority encoder is disabled with *E* set to 0 (for active-high enable input *E*), all the output lines will have 0s (for active-high outputs). When the priority encoder is enabled, then the output lines issue the binary data representation of the highest priority input signal asserted (set to 1 for active-high).

In this article, there are six priority encoder macros, namely encod_4_2_p (4×2 priority encoder), encod_4_2_p_E (4×2 priority encoder with Enable input), encod_8_3_p (8×3 priority encoder), encod_8_3_p_E (8×3 priority encoder with Enable input), encod_dec_bcd_p (decimal to BCD priority encoder), encod_dec_bcd_p_E (decimal to BCD priority encoder with Enable input), described for UZAM_PLC as shown in **Tables 1, 2…6**, respectively. Let us now consider these macros.

The 4×2 priority encoder macro "encod_4_2_p" is shown in Table 1, together with its symbol and truth table. In this priority encoder, there are four input lines, namely 3, 2, 1 and 0, represented by Boolean variables "reg3,bit3", "reg2,bit2", "reg1,bit1" and "reg0,bit0" respectively.

Input line 3 has the highest priority, while the input line 0 has the lowest. The two output lines are A_1 (Most Significant Bit – MSB) and A_0 (Least Significant Bit – LSB), represented by Boolean variables "regA1,bitA1" and "regA0,bitA0" respectively. How the macro "encod_4_2_p" works is shown in the truth table. It can be seen that the output binary code is generated based on the highest priority input signal present in the four input lines. For example, when the signal present in the input line 3 is 1, the output lines generate the following binary code A_1A_0 = 11 for this input signal, regardless of the signals present in other input lines.

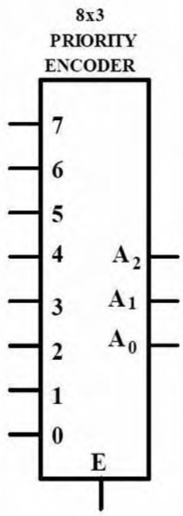
The 4×2 priority encoder with Enable

Macro	Symbol	Truth table

Macro

```
;--------- macro: encod_8_3_p_E -----
encod_8_3_p_E  macro reg7,bit7,
reg6,bit6,reg5,bit5,reg4,bit4,
reg3,bit3,reg2,bit2,reg1,bit1,
reg0,bit0,regA2,bitA2,regA1,
bitA1,regA0,bitA0
        local   L1,L2,L3,L4,L5,L6,L7,L8
        movwf   Temp_1
        btfss   Temp_1,0
        goto    L2
        btfss   reg7,bit7
        goto    L8
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L8      btfss   reg6,bit6
        goto    L7
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L7      btfss   reg5,bit5
        goto    L6
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L6      btfss   reg4,bit4
        goto    L5
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L5      btfss   reg3,bit3
        goto    L4
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L4      btfss   reg2,bit2
        goto    L3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L3      btfss   reg1,bit1
        goto    L2
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L2      bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
L1
        endm
;-----------------------------------
```

Symbol



W	E
7 =	reg7,bit7
6 =	reg6,bit6
5 =	reg5,bit5
4 =	reg4,bit4
3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A2 =	regA2,bitA2
A1 =	regA1,bitA1
A0 =	regA1,bitA0

Truth table

inputs									outputs		
E	0	1	2	3	4	5	6	7	A2	A1	A0
0	x	x	x	x	x	x	x	x	0	0	0
1	x	x	x	x	x	x	x	1	1	1	1
1	x	x	x	x	x	x	1	0	1	1	0
1	x	x	x	x	x	1	0	0	1	0	1
1	x	x	x	x	1	0	0	0	1	0	0
1	x	x	x	1	0	0	0	0	0	1	1
1	x	x	1	0	0	0	0	0	0	1	0
1	x	1	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0

x: don't care

Table 4: *The macro "encod_8_3_p_E" together with its symbol and truth table*

input macro "encod_4_2_p_E" is shown in Table 2, together with its symbol and the truth table. In addition to the "encod_4_2_p", this priority encoder macro has an active-high enable line, *E*, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this priority encoder is disabled with *E* set to 0, all the output lines will have 0s (for active-high outputs). When this priority encoder is enabled with *E* set to 1, it functions as described for "encod_4_2_p".

The 8×3 priority encoder macro "encod_8_3_p" is shown in Table 3, together with its symbol and truth table. In this priority encoder, there are eight input lines, namely 7, 6…0, represented by Boolean variables "reg7,bit7", "reg6,bit6", "reg5,bit5", "reg4,bit4", "reg3,bit3", "reg2,bit2", "reg1,bit1" and "reg0,bit0" respectively.

Input line 7 has the highest priority, while the input line 0 has the lowest priority. The three output lines are A_2 (MSB), A_1 and A_0 (LSB), represented by Boolean variables "regA2,bitA2", "regA1,bitA1" and "regA0,bitA0" respectively. How the macro "encod_8_3_p" works is shown in the truth table. It can be seen that the output binary code is generated based on the highest priority input signal present in the eight input lines. For example, when the signal present in the input line 7 is 1, the output lines generate the following binary code $A_2A_1A_0$ = 111 for this input signal, regardless of the signals present in other input lines.

The 8×3 priority encoder with Enable input macro "encod_8_3_p_E" is shown in Table 4, together with its symbol and truth table. In addition to the "encod_8_3_p", this priority encoder macro has an active-high enable line, *E*, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this priority encoder is disabled with *E* set to 0, all the output lines will have 0s (for active-high outputs). When this priority encoder is enabled with *E* set to 1, it functions as described for "encod_8_3_p".

The decimal to BCD priority encoder macro "encod_dec_bcd_p" is shown in Table 5, together with its symbol and truth table. In this priority encoder, there are ten input lines, namely 9, 8…0, represented by Boolean variables "reg9,bit9", "reg8,bit8", "reg7,bit7", "reg6,bit6", "reg5,bit5", "reg4,bit4", "reg3,bit3", "reg2,bit2", "reg1,bit1" and "reg0,bit0" respectively.

Input line 9 has the highest priority, while the input line 0 has the lowest priority. The four output lines are A_3 (MSB), A_2, A_1 and A_0 (LSB), represented by Boolean variables "regA3,bitA3", "regA2,bitA2", "regA1,bitA1" and "regA0,bitA0" respectively. How the macro "encod_dec_bcd_p" works is shown in the truth table. It can be seen that the output binary code is generated based on the highest priority input signal present in the ten input lines. For example when the signal present in the input line 9 is 1, the output lines generate the following binary code $A_3A_2A_1A_0$ = 1001 for this input signal, regardless of the signals present in other input lines.

The decimal to BCD priority encoder with Enable input macro "encod_dec_bcd_p_E" is shown in Table 6, together with its symbol and truth table. In addition to the "encod_dec_bcd_p", this priority encoder macro has an active-high enable line, *E*, for enabling it. In this macro, E is a Boolean input variable taken into the macro through W. When this priority encoder is disabled with *E* set to 0, all the output lines will have 0s (for active-high outputs). When this priority encoder is enabled with *E* set to 1, it functions as described for "encod_dec_bcd_p".

The file "p_enc_mcr_def.inc", including the 6 priority encoder macros shown in Tables 1, 2…6 can be downloaded from **http://host.nigde.edu.tr/muzam/**. ■

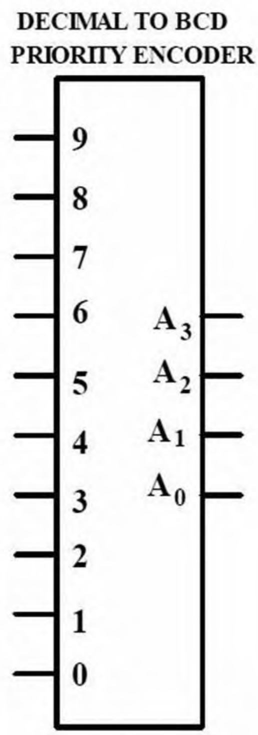
Tables 5 and 6 are shown on the next page

Macro	symbol	Truth Table

Macro

```
;--------- macro: encod_dec_bcd_p -----------
encod_dec_bcd_p  macro   reg9,bit9,
reg8,bit8,reg7,bit7,reg6,bit6,
reg5,bit5,reg4,bit4,reg3,bit3,
reg2,bit2,reg1,bit1,reg0,bit0,
regA3,bitA3,regA2,bitA2,regA1,bitA1,regA0,bitA0
        local   L1,L2,L3,L4,L5,L6,L7,L8,L9,L10
        btfss   reg9,bit9
        goto    L10
        bsf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L10     btfss   reg8,bit8
        goto    L9
        bsf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L9      btfss   reg7,bit7
        goto    L8
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L8      btfss   reg6,bit6
        goto    L7
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L7      btfss   reg5,bit5
        goto    L6
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L6      btfss   reg4,bit4
        goto    L5
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L5      btfss   reg3,bit3
        goto    L4
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L4      btfss   reg2,bit2
        goto    L3
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L3      btfss   reg1,bit1
        goto    L2
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L2      bcf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
L1
        endm
;-----------------------------------
```

symbol



9 =	reg9,bit9
8 =	reg8,bit8
7 =	reg7,bit7
6 =	reg6,bit6
5 =	reg5,bit5
4 =	reg4,bit4
3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A3 =	regA3,bitA3
A2 =	regA2,bitA2
A1 =	regA1,bitA1
A0 =	regA1,bitA0

Truth Table

inputs										outputs			
0	1	2	3	4	5	6	7	8	9	A3	A2	A1	A0
x	x	x	x	x	x	x	x	x	1	1	0	0	1
x	x	x	x	x	x	x	x	1	0	1	0	0	0
x	x	x	x	x	x	x	1	0	0	0	1	1	1
x	x	x	x	x	x	1	0	0	0	0	1	1	0
x	x	x	x	x	1	0	0	0	0	0	1	0	1
x	x	x	x	1	0	0	0	0	0	0	1	0	0
x	x	x	1	0	0	0	0	0	0	0	0	1	1
x	x	1	0	0	0	0	0	0	0	0	0	1	0
x	1	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0

x: don't care

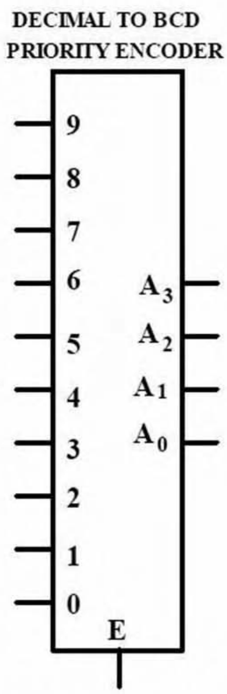
Table 5: *The macro "encod_dec_bcd_p" together with its symbol and truth table*

Macro	Symbol	Truth table

Macro

```
;--------- macro: encod_dec_bcd_p_E -----------
encod_dec_bcd_p_E  macro   reg9,bit9,
reg8,bit8,reg7,bit7,reg6,bit6,
reg5,bit5,reg4,bit4,reg3,bit3,
reg2,bit2,reg1,bit1,reg0,bit0,
regA3,bitA3,regA2,bitA2,regA1,bitA1,regA0,bitA0
        local   L1,L2,L3,L4,L5,L6,L7,L8,L9,L10
        movwf   Temp_1
        btfss   Temp_1,0
        goto    L2
        btfss   reg9,bit9
        goto    L10
        bsf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L10     btfss   reg8,bit8
        goto    L9
        bsf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L9      btfss   reg7,bit7
        goto    L8
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L8      btfss   reg6,bit6
        goto    L7
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L7      btfss   reg5,bit5
        goto    L6
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L6      btfss   reg4,bit4
        goto    L5
        bcf     regA3,bitA3
        bsf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L5      btfss   reg3,bit3
        goto    L4
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L4      btfss   reg2,bit2
        goto    L3
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bsf     regA1,bitA1
        bcf     regA0,bitA0
        goto    L1
L3      btfss   reg1,bit1
        goto    L2
        bcf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bsf     regA0,bitA0
        goto    L1
L2      bcf     regA3,bitA3
        bcf     regA2,bitA2
        bcf     regA1,bitA1
        bcf     regA0,bitA0
L1
        endm
```

Symbol



W	E
9 =	reg9,bit9
8 =	reg8,bit8
7 =	reg7,bit7
6 =	reg6,bit6
5 =	reg5,bit5
4 =	reg4,bit4
3 =	reg3,bit3
2 =	reg2,bit2
1 =	reg1,bit1
0 =	reg0,bit0
A3 =	regA3,bitA3
A2 =	regA2,bitA2
A1 =	regA1,bitA1
A0 =	regA1,bitA0

Truth table

inputs											outputs			
E	0	1	2	3	4	5	6	7	8	9	A3	A2	A1	A0
0	x	x	x	x	x	x	x	x	x	x	0	0	0	0
1	x	x	x	x	x	x	x	x	x	1	1	0	0	1
1	x	x	x	x	x	x	x	x	1	0	1	0	0	0
1	x	x	x	x	x	x	x	1	0	0	0	1	1	1
1	x	x	x	x	x	x	1	0	0	0	0	1	1	0
1	x	x	x	x	x	1	0	0	0	0	0	1	0	1
1	x	x	x	x	1	0	0	0	0	0	0	1	0	0
1	x	x	x	1	0	0	0	0	0	0	0	0	1	1
1	x	x	1	0	0	0	0	0	0	0	0	0	1	0
1	x	1	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

x: don't care

Table 6: *The macro "encod_dec_bcd_p_E" together with its symbol and truth table*

USE OF AN AGC AMPLIFIER AS A SOFT LIMITER OF SIGNALS

PROPOSED AUTOMATIC Gain Control (AGC) amplifier can be used for "soft" limitation of signal value regarding its peak value (it is important to note that it's not about its rms value, but about its absolute value) with low distortions. This is necessary for some voice processing systems, communication systems etc.

Usual simple AGC amplifiers cannot work properly in these applications. The usual simple AGC amplifiers have comparatively high total-harmonic distortions. They work from rms value of signals and have a harmful effect, which can be named "temporary signal fading". This effect shows up in an AGC amplifier as the gain control circuit starts to operate (when the AGC feedback is "turned on"). It is of the 'step' nature. This provides a momentary reduction of the signal level, with a subsequent slow increase.

Secondly, the simple AGC amplifiers have different reactions on the positive and negative half-waves of a signal. Sometimes this is inadmissible, for example when modulation is heavily applied. These negative effects must be removed and speech intelligibility provided, if it's for a voice system application.

The schematic diagram of the "soft" limiter of signals without the imperfections stated above is presented in **Figure 1**.

The device consists of an adjustable attenuator (R4, RDSV4), an amplifier (DA1-1), a precision full-wave rectifier (DA1-2, DA1-3) and a control element (VT2) with a capacitive integrator (R7, C4).

An input signal comes through an adjustable attenuator to an amplifier. The adjustable attenuator in contrast to usual devices is adjusted so that it reduces the output signal (when the AGC feedback still will not "turned on") approximately to -1dB by using the adjustable resistor R6.

In the proposed device we use a P-channel silicon field-effect transistor (VT1) with high gate-source cut-off voltage (VGS off) and a suitable drain-source on-resistance (RDS on). VGS off between 3-7V and RDS on of about 200Ω would be optimal.

However, it is important to note that the value of the gate-source cut-off voltage (VGS off) influences the reducing of "the temporary signal fading" effect, too.

The drain-source on-resistance (RDS on) together with value of resistor R4 determines the dynamic range of the device. This range is K = 20log(1+R4/RDS).

The cause of high total harmonic distortions in simple AGC amplifiers is high non-linear distortions of the adjustable attenuator. Non-linear distortions of the adjustable attenuator of the proposed device can be reduced by using a special RC chain (C3, R13, R14).

A precision circuit of the signal's absolute value is used and thereby the second problem analyzed above is solved.

An important element of the control circuit is the transistor VT2. The voltage reduction on the gate of transistor VT1 reduces its resistance and, accordingly, this reduces the factor of transfer ratio of the attenuator. Thereby the level of the output signal will not exceed the adjusted value, as long as the voltage on the gate of transistor VT1 is not 0V. In this case, the transistor VT1 is fully opened.

The speech intelligibility depends on the response time of the capacitance integrator (R7, C4) and can be selected experimentally. A suitable choice is R7 = 330K and C4 = 10uF. The adjustable

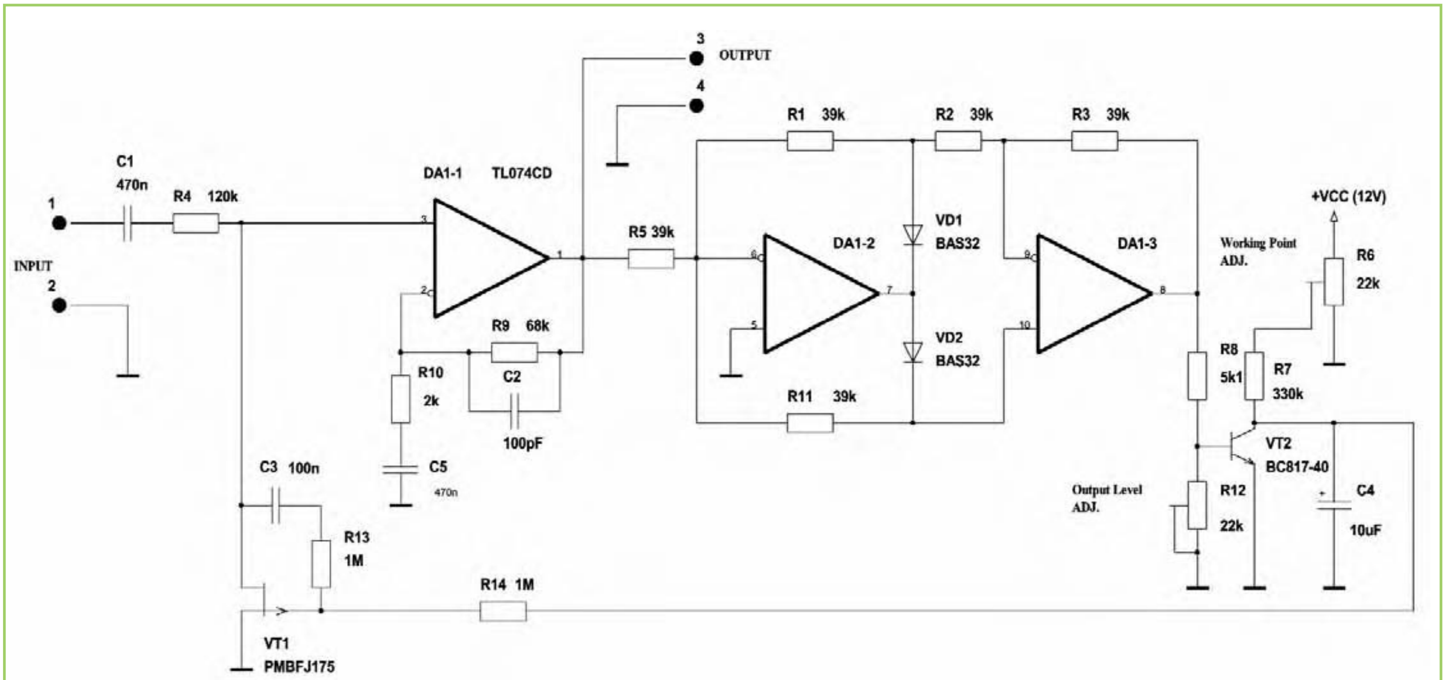


Figure 1: *Soft limiter*

resistor R12 can be adjusted to the needed amplitude value of the output signal. Note that this is not some root-mean-square (effective) value! Naturally, the maximum amplitude of the output signal cannot be less than the operational threshold of the transistor VT2 (which is about 0.68V). The necessary value of the input can be set by a suitable choice for the gain of the amplifier DA1-1. It can be calculated by KU = 1+R9/R10. This is correct within the operational frequency range only.

This device has excellent response speed. It is less than one half-wave of the signal.

Background

My "discovery" is using: 1) precision full-wave rectifier, 2) the control element with a capacitive integrator, 3) P-channel silicon field-effect transistor (VT1) with high gate-source cut-off voltage (VGS off) and 4) tuning control of its working point.

The first time I used this device as limiter of modulation was in one of my private projects. I needed to have an amplitude value of a signal (in any time interval and of any polarity), no more than it was specified, and with a wide dynamic range, low total harmonic distortions and without perceptible distortion of articulation. I could not use usual limiters and I tested many technical ideas; it turned out that this design was the best.

I used this device in a musical system as automatic mixer for a DJ, too. Two signals (music and voice) come as inputs to this limiter and their total level was supported constantly. The music signal was reduced when the DJ began to speak and slowly rose to its former level if the DJ stopped talking.

Any overloads of amplifiers and loudspeaker systems were not presented. I used this idea as a base for a precision Wien-bridge (Wien-Robertson bridge) oscillator of sinusoidal signals. The results were excellent and exceeded all my expectations.

Vladimir Rentyuk
Development engineer of "Modul-98 Ltd"
The Ukraine

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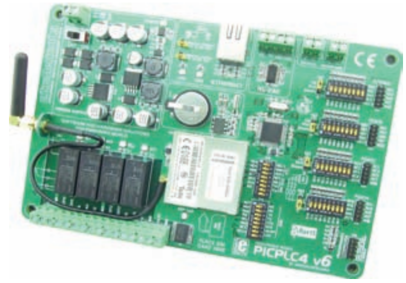
NEW ADDITION TO THE PIC DEVELOPMENT TOOL FROM MIKROELEKTRONIKA



mikroElektronika is proud to announce PICPLC4 v6 PLC System as an addition to its PIC development tool product line. The new PICPLC4 v6 is a PLC system for development of industrial, home or office control devices. The PICPLC4 v6 PLC includes new features such as four relays outputs, GSM/GPRS communication, Ethernet, RTC and much more.

Each feature of the board is supported by example written in mikroC PRO, mikroPascal PRO and mikroBasic PRO compiler for PIC. Also, PICPLC4 v6 comes with the full color printed documentation.

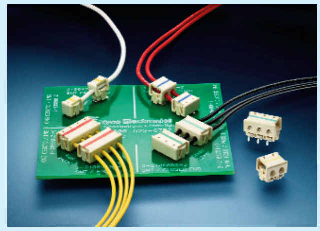
The system price is $99 and it is available for purchase on the mikroElektronika website and through authorized distributors.

www.mikroe.com/en/tools/picplc4-v6/

ROHS-COMPLIANT IDC SOLID STATE LIGHTING CONNECTOR

Tyco Electronics has released the new IDC solid state lighting (SSL) connector for quick, tool-less termination of discrete wires onto LED printed circuit boards (PCBs). The product terminates 18 through 24 AWG solid and stranded wire utilizing insulation displacement technology to eliminate the labour-intensive task of pre-stripping wires and soldering.

The robust design of the IDC SSL connector suits harsh environments in the solid state lighting industry. Specific LED applications include: lighting controls, general illumination fixtures and interconnection of strings in PCB light modules. Additionally, the product supports various non-lighting applications that require the attachment of discrete wire leads to PCBs. The RoHS-compliant connector – available in one, two, three and four positions – meets UL 1177 specifications.



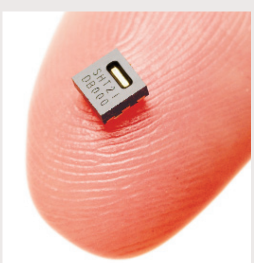
Product offerings include SMT/thru-hole and closed-end/feed-thru configurations. The closed-end version contains a "viewing" window to ensure that the wire is fully seated and secure after termination. The product, built with 94 V0-rated high-temperature resistant thermoplastic, enables reflow processing.

www.tycoelectronics.com

WORLD'S SMALLEST DIGITAL HUMIDITY SENSOR: SHT21

With the new SHT21, Sensirion launches the world's smallest digital humidity and temperature sensor. The SHT21 consists of a newly designed, sophisticated sensor chip, encapsulated in a 3x 3 x 1.1mm DFN 3-0 package. Over-moulding provides excellent protection against ageing and ambient impact, such as condensation and harsh environments and, thus, yields outstanding long-term stability.

The SHT21 is fully calibrated and provides an I2C digital interface. Analogue output modes (such as PWM) are available on request. The digital communication mode enables superb low power consumption: A value in the range of 3µW at normal operation is well achieved. Typical sensor accuracy is ±2% RH over 20-80% RH and ±0.3°C over 25-42°C. Provided on tape & reel, the reflow solderable SHT21 is suitable for high volume applications. Furthermore, the sensor is qualified in accordance with automotive standard AEC-Q100 and an extended quality assurance program guarantees low PPM values.



Free samples of the humidity and temperature sensor can be ordered at

www.sensirion.com/mysht21

NEW SUPER FAST UNIVERSAL PROGRAMMER – DATAMAN 48PRO2

Dataman, a provider of device programmers, has recently released a new 48-pin universal programmer that now supports over 52,000 devices. Since programming times are faster than ever before, this new product will appeal not only to the community of hardware developers, but also to small and medium sized manufacturers.

The 48Pro2 is an enhanced version of the popular 48Pro+ universal programmer. The company's target was to optimize this product for fast programming of high density memories which has been achieved through the use of a much more powerful FPGA based core inside the programmer. The 48Pro2 is able to program NAND and NOR Flash memories up to 70% faster than its predecessor.

The programmer reliably programs a wide range of programmable chips in the ZIF socket (more than 800 models of socket converters are available), as well as through the ISP connector.

www.dataman.com

NEW 12GHZ TDR/TDT SAMPLING OSCILLOSCOPE FROM PICO TECHNOLOGY

The PicoScope 9211A TDR/TDT Sampling Oscilloscope is a new instrument specially designed for time-domain reflectometry (TDR) and time-domain transmission (TDT). It provides a low-cost method of analysing cables, connectors, circuit boards and IC packages.

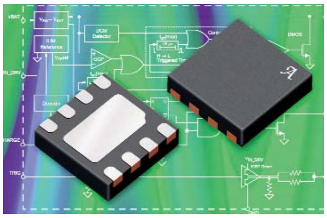
The PicoScope 9211A works by stimulating the device under test using its two independently programmable, 100-ps (typical) rise-time step generators. It then uses its 12GHz sampling inputs to build up a picture from a sequence of reflected or transmitted pulses. The results can be displayed as volts, ohms or reflection coefficient against time or distance.

As well as TDR/TDT analysis, the PicoScope 9211A can also be used for mask limit testing of a wide range of communications standards including SONET/SDH, Fibre Channel, Ethernet, InfiniBand 2.5G and 5.0G, XAUI, ITU G.703, ANSI T1/102, RapidIO 1.25G and 3.125G, G.984.2, PCI Express 2.5G and 5.0G, and Serial ATA 1.5G and 3.0G. Over 150 industry-standard masks are included.

www.picotech.com

ULTRA-SMALL XENON PHOTOFLASH DRIVER ICS

The A8732 and A8735 from Allegro MicroSystems Europe are two ultra-small, new, Xenon photoflash charger ICs, designed to offer a compact and robust low-cost solution to meet the requirements of very low power, small form-factor cameras and camera phones.



Size and cost are minimised through a high level of integration within the confines of a 2 x 2mm DFN package. Battery life is extended by using primary-side voltage sensing to remove the need for a secondary-side voltage divider and associated leakage current, and the devices also feature very low supply current in both shutdown and standby mode.

The A8732 and A8735 are optimised for use in mobile devices using single-cell lithium batteries and achieve more than 75% efficiency using zero-voltage switching for lower losses. Capacitor charging is provided by an IGBT driver, while an integrated 50V DMOS switch offers self-clamping protection.

www.allegromicro.com

MIXED-SIGNAL OSCILLOSCOPE SUPPORTS FLEXRAY BUS ANALYSIS

A FlexRay serial bus analysis function is now available as an option to 4-channel models in the Yokogawa DLM2000 Series of mixed-signal oscilloscopes.

Designed to provide physical-layer waveform observation and protocol analysis for the fast, highly reliable FlexRay in-vehicle local area network, the new facility allows the user to capture FlexRay bus signals with a wide variety of dedicated triggers and carry out analysis and troubleshooting on parameters that can affect the FlexRay signal.

With the new analysis function, the DLM2000 can automatically detect and display packet information directly beneath the time-domain waveform and can search or trigger on specific serial bus conditions. A wide variety of trigger conditions can be set, including ID/data trigger combinations and combinations of serial bus triggers with normal edge triggers.

An important feature of the serial bus analysis function on the DLM2000 Series is that it enables simultaneous analyses of different buses.

http://tmi.yokogawa.com/ea

DIN 41 612 CONNECTOR SERIES WITH TRIPLED VOLTAGE TRANSFER CAPABILITY

Harting's surface-mount compatible series of DIN 41 612 connectors now has triple the voltage transfer capability of earlier versions.

This performance gain has been achieved through the use of special plastics featuring higher values of CTI (comparative tracking index: a measure of insulation capability defined by Underwriters Laboratories). These new plastics comply with the Group II specification, with a CTI of between 400 and 600, while the standard plastics are classified as Group IIIa or IIIb, with a CTI of between 100 and 400.

Given a creepage distance of 1.2mm, the voltage between two adjacent contacts can amount to 160V: considerably higher than the usual 50V.

The new connectors are available in types C, 2C, 3C, B, 2B, 3B, R, 2R and F. Additional construction types and sizes are available on request.

www.harting.com

HIGH RELIABILITY COMPACT CONTACTLESS JOYSTICKS

Specialist Emech distributor Foremost Electronics announces the availability of the 3000 Series of contactless joysticks and accessories. The patented 3000 Series Joystick embodies the latest technologies to offer high-precision, contactless control. With a class leading depth of < 19mm, it is available in one, two of three axis formats and its Hall Effect technology offers long, trouble-free life. A range of analogue output signals are available and custom PWM outputs may be specified.

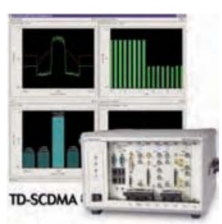
The 3000 Series Joystick offers a radically improved mechanism construction for maximum robustness, strength and long-term performance and requires a significantly reduced number of components, further contributing to reliability. A metal ball mechanism is at the heart of the joystick, tested to withstand greater forces than possible with older generation plastic or gimbal style mechanisms. All 3000 Series Joysticks are sprung to return to the centre position with an operating force of 1.3N with lighter (1.0N) and stronger (1.6N) forces as options.

www.4most.co.uk

PXI MEASUREMENT SUITE FOR FAST TESTING OF MOBILE PHONES AND RFICS

Aeroflex introduced its PXI 3030 TD-SCDMA Measurement Suite to provide fast and cost-effective production testing of mobile handsets and RFICs based on ETSI 3GPP TS 34-122.

The PXI 3000 Series supports all major cellular standards, including 3GPP LTE, CDMA2000, 1xEVDO, GSM, W-CDMA and mobile WiMAX. The wireless connectivity standards WLAN and Bluetooth are expected to be integrated into most TD-SCDMA phones and are also supported in this single box solution.



The PXI Measurement Suite makes parametric measurements of TD-SCDMA transmitters and supports high-speed alignment and performance verification of devices operated in a non-signalling mode. Applications include high-speed/high-throughput mobile handset testing, as well as RFIC characterization.

The platform provides high yield and throughput, achieving dramatic improvements in test time using speed-optimizing techniques such as multi-thread processing, pipelined capture and fast-sequence tuning (FST).

TD-SCDMA test solutions are available to ship within four to six weeks. Software upgrades to existing systems are available immediately as software retrofits.

www.aeroflex.com

PICMG 1.3-COMPLIANT 2U BUTTERFLY BACKPLANE FOR PCI EXPRESS GEN 2 SYSTEM DESIGNS

The new Kontron 2U Butterfly Backplane xPB-6E5PO for PICMG 1.3-based system designs boasts comprehensive PCI Express Gen 2 support in the smallest of spaces. Compared to competing custom solutions, the PICMG 1.3-compliant standard component offers a more cost-effective and fast system design using COTS components, ultimately helping to accelerate OEMs' time-to-market and reducing total cost of ownership.

The Kontron 2U backplane xPB-6E5PO is designed for highest throughput (5.0GT/s) with the latest frame grabbers, graphics and network cards. The space-saving butterfly backplane was developed for image processing, gaming and infotainment, as well as networking applications. Via standard graphics cards, the high-speed backplane can provide, for example, 10 displays with different video signals. With high-end components, control of up to 40 monitors – each with different content – is possible. Equally, very fast image processing systems with multiple frame grabbers and graphics cards or ultra-bandwidth routers with integrated firewall and 2 x 10 Gigabit Ethernet for upstream and downstream can be implemented.

www.kontron.com

APD DIRECT PCB CONNECTOR ELIMINATES BOARD TO BOARD CONNECTORS

A new cost-saving plastic connector, which eliminates the need to use board- to-board connectors, has been developed by ITT Interconnect Solutions. The APD direct PCB connector provides a direct interface into the "box" but is connected to a PCB internally, instead of using the standard crimped cable connection. Additionally, this new connector requires no harnessing which saves board space and results in reduced manufacturing costs.

Robust and lightweight, the APD connector is sealed to IP67/IP69K, providing protection against the effects of dust and temporary immersion. Combined with excellent resistance to oil, this connector suits a wide range of industrial, transportation and military applications. Operating voltage is 48V maximum.

The connector is available in 6, 7, 19, 37 or 51-way versions, plus a 4-way configuration for sensor applications. Machined contacts have a press-in contour and up to four colour and mechanical codings are available. It is compatible with selective wave solder processing.

www.ittcannon.com

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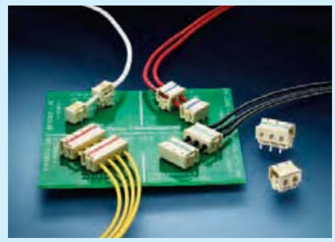

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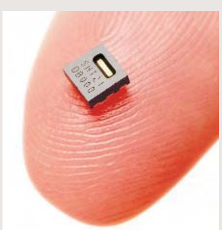

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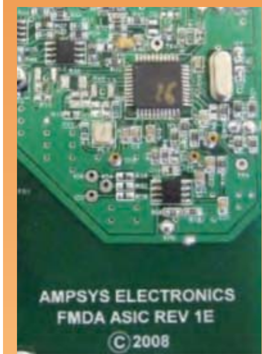
Free samples of the humidity and temperature sensor can be ordered at

www.sensirion.com/mysht21

TRANSFORMER MANUFACTURE

AMPSYS ELECTRONICS READIES THE ANTI-MULTIPATH FM DEMODULATOR AMPD

FM radio specialist Ampsys Electronics has completed successful road tests of the world's first single antenna radio that eliminates multipath distortion (MPD) in car radios. Using the amplitude locked loop (ALL), double demodulation has become possible. The envelope of the carrier is used to correct for the distortion in the FM transmission path and the destructive spikes are reduced to insignificant levels. There is no need for second antennas, tuners, cable harnesses or switching circuitry representing substantial cost reduction. Licences to manufacture including the AMPD-IC are now available.



www.ampsysltd.co.uk

HCD ANNOUNCES PETER FULLER AS BUSINESS DEVELOPMENT MANAGER

HCD, UK-based contract electronics manufacturer and PCB design house, has announced Peter Fuller as its Business Development Manager. Fuller, a veteran of 25 years in the UK PCB and CEM markets, is tasked with helping to continue HCD's sales efforts, which have seen the company, grow despite the current recession.

From PCB design through to final product assembly, HCD has developed by investing in plant and personnel, and now offers a complete in-house solution for electronics prototyping and assembly.

HCD continues to invest in new technology and it now has two surface mount lines, but also retaining its through-hole production capability, making it very flexible in technology and turn-around time.

www.hcduk.com

AWS ELECTRONICS OFFERS QUICK TURN CABLE ASSEMBLY SERVICE

AWS Group, UK based independent Electronic Manufacturing Solutions (EMS) provider, is now offering a quick turn-around service from its AWS Electronics manufacturing site in Newcastle-under-Lyme. Whereas the standard production lead-time offered is 15 working days, AWS offers a 3-5 day turn around for prototype or 'Fast Track' requests.

AWS set up the dedicated cable assembly operation seven years ago and now employs 55 people in that activity alone at the Staffordshire works. The dedicated business unit occupies 15,000 sq ft and includes dedicated technical, purchase and stores support, as well as manufacturing operations. As with many of its activities, AWS backs up its UK facilities with a low cost manufacturing option through its Slovakia plant.

www.awselectronicsgroup.com

NEW CUSTOM FRONT PANEL SERVICE FROM BETA LAYOUT

Having pioneered the facility for engineers to purchase PCBs online (pcb-pool.com), Beta Layout has announced the introduction of a new online Front Panel service.

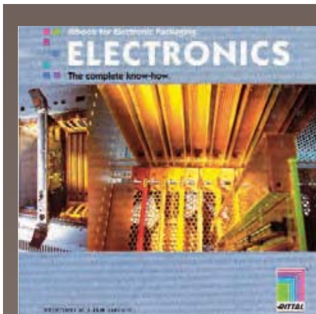
The service enables users to configure their own Front Panel designs and place an order directly online. As well as providing professional free-to-download design software, numerous machining options, material thickness, fonts, colours and finishes are available.

The free, easy-to-use, design software simplifies the configuration and ordering of custom Front Panels. You can choose from many standardised construction units (e.g. ventilators, sub connectors) which are available in the software's library. The software even calculates the price of the finished front panels for you. Once your Front-Panel design is complete, an order can be placed directly through the software itself.

Email: sales@pcb-pool.com or Free phone UK: 0800 389 8560

www.panel-pool.com

RITTAL'S ELECTRONICS CATALOGUE NOW ON CD



Rittal has released a CD of its popular catalogue for electronics enclosures and associated products.

Customers faced with the size of Rittal's Handbook 32 were demanding a more portable look-up system that complemented the information available on the website.

Packed with details on everything from backplanes to power supplies and with some base systems included to give designers a head start, the catalogue includes all of the Ripac branded Subrack ranges, both as kits and individual parts, as well as desktop cases and rack cases.

For your copy, please call 01709 704000 or email information@rittal.co.uk

www.rittal.co.uk

PLESSEY SEMICONDUCTORS OUTLINES **PRODUCT STRATEGY**

Plessey Semiconductors is planning to release a number of innovative semiconductor products including a range of amplifiers, demodulators, synthesisers and high-speed pre-scalers. These products have been designed primarily for the defence and space markets, but are also used in the general communications, automotive and industrial control market segments. The types of end products that will use these components include television systems, fibre optic communications, CCTV and data communication systems. Prototypes for some of these products will be available in autumn 2010. Plessey Semiconductors operates from its semiconductor manufacturing facility in Roborough, Plymouth and a technology and design centre in Swindon, Wiltshire. The bipolar process technologies that were originally developed in Swindon are being transferred to the Plymouth facility.

Our panel of commentators says the following on this development:

BARRY MCKEOWN, RF AND MICROWAVE ENGINEER IN THE DEFENCE INDUSTRY, AND DIRECTOR OF DATOD LTD, UK:

Is it a case of 'back to the future' in the pursuit of technical excellence? The reformation of Plessey Semiconductors, through teaming the Xfab UK foundry and Plus-Semi engineering services, enables the arduous task of design and fabrication of mixed-signal components to be optimised. This is particularly relevant for the case of DDS products, with architecture that scales upwards in frequency with change of fabrication process, where the multi-octave coverage of balanced and unbalanced front-ends requires a fundamental understanding that only in-house expertise can achieve. Success, I suspect, shall also depend on the recovery of the loss of institutional memory.

I hope that they succeed with this venture.

I note that they also have received part funding from the South West Regional Development Agency of nearly £1m under the Grant for Business Investment scheme. Also, there is a potential pitfall, if they adopt the historical Pythagoras Processor Architecture, which served low MHz, low dynamic range applications. This architecture does not scale for high dynamic range, high spectral purity requirement, due to the error involved in the estimation procedure as the following extract from the Zarlink AB04 that evolved from the original Plessey PDSP16330 architecture:

"In a signal processing system it is frequently necessary to calculate the modulus and argument of Complex numbers. This operation is particularly common after Fast Fourier Transforms or in coherent receiver systems. The evaluation of $\sqrt{(x^2 + y^2)}$ and arctan (y/x) are far from easy, so approximations are often used.

A common technique for estimating the magnitude of x + jy is to take the larger value of x or y and add to it half the smaller value. The PDSP16330 Pythagoras Processor is a dedicated DSP engine capable of accurate calculation of both magnitude (modulus) and phase (argument) of Complex data at a rate of 100ns per sample."

PROFESSOR DR DOGAN IBRAHIM FROM THE NEAR EAST UNIVERSITY IN NICOSIA, CYPRUS:

The re-launch of the Plessey Semiconductors's brand is very exciting and very encouraging at this time, as the UK struggles economically. Plessey Semiconductors is well known for its high performance analogue/mixed signal processors and products for the defence, medical and the automotive markets. The combination of bipolar technology and the 0.35-micron CMOS process, both on silicon and silicon-on-insulator substrates, gives the company an advantage to manufacture new, high temperature and radiation tolerant families of high performance devices.

The availability of the first innovative prototypes in Q3 of this year will be a major positive step in the continuation of the microchip technology in the UK. This new initiative from Plessey Semiconductors will create new employment opportunities in the region and will also attract well-paid engineering professionals to the company.

HAFIDH MECHERGUI, ASSOCIATE PROFESSOR IN ELECTRICAL ENGINEERING AT THE UNIVERSITY OF TUNISIA:

The opening of the world of industry encouraged competition in all fields and allowed a spectacular scientific and technological development. Thus, companies are obliged to fix a strategy to be more competitive and increase their production.

As such Plessey Semiconductors is trying to place itself at the head of other semiconductor companies, which could be easily done given it's experience in the field of electronics, the performances of its materials and its reputation.

This company is able to adapt to the rate/rhythm of production and the capacities of competition from the other electronics industrial companies. Plessey Semiconductors has an enormous technological advance; it specialized in the design and the manufacture of sophisticated electronic material. This company has a lot of ambition and this is legitimate considering its seniority and its radiant history.

MAURIZIO DI PAOLO EMILIO, TELECOMMUNICATIONS ENGINEER, INFN – LABORATORI NAZIONALI DEL GRAN SASSO, ITALY:

CMOS technology offers less power dissipation, smaller noise margins and higher packing density. The 0.35-micron CMOS process that Plessey Semiconductor announced is ideal for any electronic product that requires high precision and reliability. In the data acquisition system, which is applied widely in the electronic world, this technology will also bring the development of new processors for optical data acquisition systems (1Gb/s). And it could be a good opportunity to realize the RF application in it, too.