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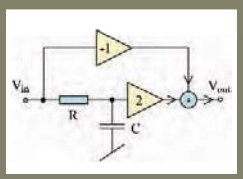

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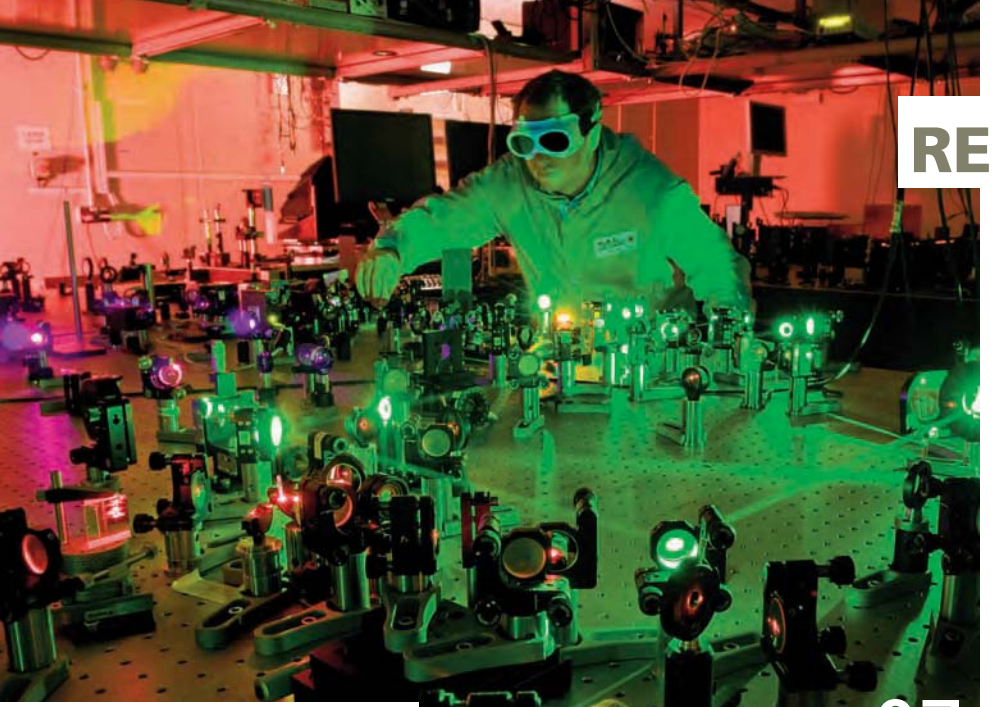

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EFFORTS TO HALT UNSAFE SOFTWARE

There are two critical questions every executive needs to answer:

"Are there safety-critical software defects shipping in my products?"
"Are there safety-critical software defects in my supplier's products?"

BY DAVE PETERSON

These two questions, while critical, are anything but easy to answer. Business risk is the result. Software complexity is the culprit.

Innovation is a key factor in sustaining competitive advantage and upholding customer satisfaction, but the other side of the innovation is software complexity. For example, the magnitude of software complexity in today's modern automobiles, aircraft and safety-critical systems is staggering, with a luxury automobile containing 100 million lines of software code. And it doesn't stop with in-house developed code. Software complexity is creating an entirely new class of business risk across the entire software supply chain. Companies are now accountable for both the software shipping in their products and the software from their third-party providers, elevating the need for visibility to assess whether they are shipping safe software to their customers.

Most companies have existing requirements and processes to identify quality and safety issues, such as manual code review and scenario testing, but traditional testing methods are not sufficient to expose all the possible risk in the software code. Complex modern systems require transformational practices that leverage automation to ensure code quality before testing begins. Two of the primary problems that leave traditional testing methods insufficient to meet today's software complexity challenge are combinatorial path complexity and test coverage complexity. This can be particularly challenging for companies that integrate multiple software components from different companies and suppliers. Each software component has combinatorial path complexity of its own. For example, a code base of one million lines of code can have more than a trillion possible paths to defects. When combined with another software component, the complexity rises dramatically because the interaction between the components can cause new and unexpected behaviours that would not exist before integration. This problem compounds even more when integrating components from different suppliers that use different forms of testing and integrity analysis. Test coverage complexity is also a significant challenge in large code bases. Typical manual code review can cover only small fragments of a code base. Situational testing such as functional testing, unit testing, performance testing and security testing can cover significant portions of the code lines, but almost never a significant portion of the combinatorial paths. Automated software integrity analysis is required to test the entire code base and comprehensively exercise all the possible paths that may contain defects.

> **"SITUATIONAL TESTING SUCH AS FUNCTIONAL TESTING, UNIT TESTING, PERFORMANCE TESTING AND SECURITY TESTING CAN COVER SIGNIFICANT PORTIONS OF THE CODE LINES, BUT ALMOST NEVER A SIGNIFICANT PORTION OF THE COMBINATORIAL PATHS"**

In response to the software complexity challenge, some firms, including Coverity, are providing software integrity audits to qualified Global 2000 companies with safety-critical software concerns. These types of audits can expose software defects that could change the behaviour, freeze the operation or impair the performance of safety-critical devices or products.

Software complexity should fuel innovation, not introduce business risk. Companies need to make software integrity a priority and mandate it across the entire software supply chain.

Dave Peterson is Chief Marketing Officer at Coverity

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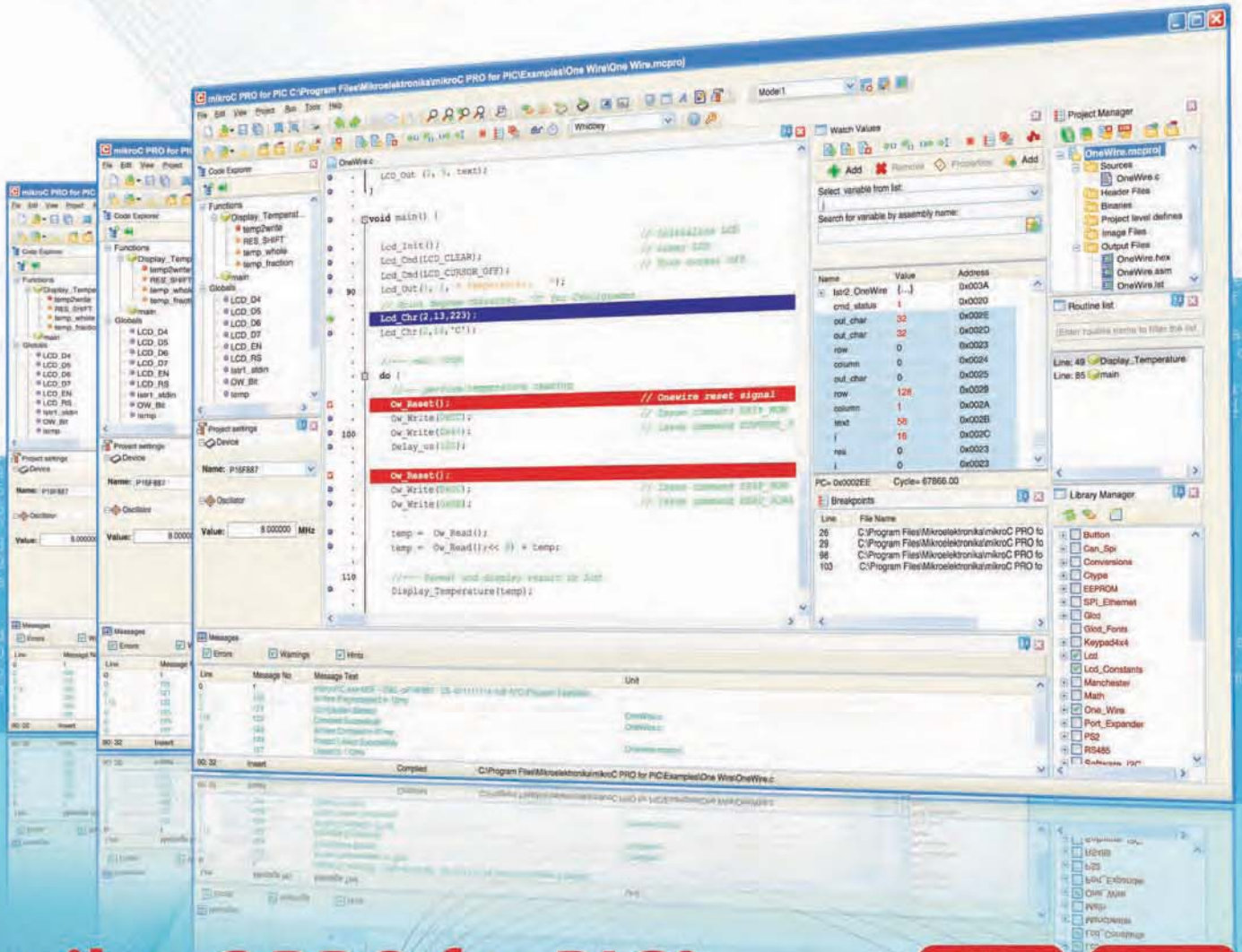

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■ Smart houses that recognize when someone is ill or has forgotten to take medication – or even if the fridge needs replenishing – are likely to become commonplace in the UK. Telemedicine expert at the University of Portsmouth, Dr Jim Briggs, has won £128,000 government money to take some of these ideas to market; he'll be working closely with Newbury-based Smart home technology firm PassivSystems.

Sensors will be able to 'read' the health and well-being of those who live in a house and upload the information to a secure website for a relative or carer living remotely to view.

RADIO SIGNALS RESEARCH SCANS NEW HORIZONS

A study at the University of Leicester aims to understand the reasons why radio signals sometimes act unpredictably, travelling beyond the horizon and interfering with other signals.

This is important because reliable radio signalling is not only economically beneficial, it is important in terms of safety.

Doctoral research by Naveed Mufti at the Radio Systems Research Group in the Department of Engineering at Leicester University focuses on examining transmission of radio signals across the English Channel.

"The research is aimed at analysing the data to produce statistics that will aid network designers in predicting interference between radio signals. This is expected to lead to more reliable radio communication and efficient utilization of available radio resource, generating socio-economic benefits," said Mufti. "Unpredictable behaviour by radio signals can disrupt vital communication.

Radio communication uses the radio frequency spectrum. Use of the spectrum in 2007 contributed almost 3% of the UK's GDP. In early 2008, Ofcom, the telecom regulator auctioned portions of mostly unused portions of this spectrum, raising roughly £1.4m.

"Normally, the power of radio signals decreases with distance. Most public-use radio signals are not intended to travel beyond the horizon. However, certain meteorological conditions cause radio signals to travel beyond the expected range. This enhancement potentially causes interference to other systems. Hence, there is a need to fully understand the propagation of radio signals in different environments," added Mufti.

Laser Celebrates Its 50th Birthday

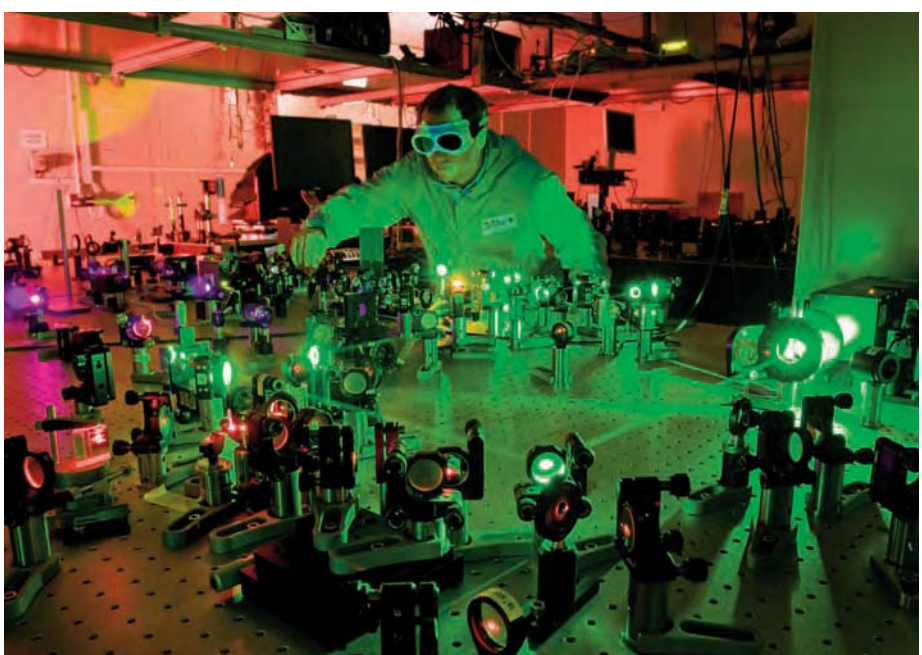
The Institute of Physics (IOP), the Engineering and Physical Science Research Council (EPSRC) and the Science and Technology Facilities Council (STFC) are using the laser's fiftieth birthday as an opportunity to highlight how ubiquitous this fundamental physics discovery has become and its potential for future applications.

The trio says that lasers will help humankind out of its energy quandary – either by directing renewable energies towards greater efficiencies by, for example, detecting changes in the wind to ensure wind turbines are in the most efficient position or, as part of the world's most powerful laser facility, HiPER, to demonstrate the feasibility of laser driven fusion as a future clean and affordable energy source.

Laser sales amount to around £5bn a year globally. The first was the ruby laser, created by Theodore Maiman at Hughes Research Laboratories in California. At the time, experts referred to it as a 'solution looking for a problem'.

One of its first commercial uses was in 1974, when a packet of Wrigley's chewing gum became the first ever product to be bought using a laser barcode reader. In 1982, singer-songwriter Billy Joel's 52nd Street became the first album to be etched onto a compact disc for CD players' lasers to read. Nowadays, lasers are being used as communication channels for all optical fibre-based communications. In medicine, dyes are being used alongside lasers to identify misbehaving molecules personal to any individual's ailment which will give doctors the information required to create individual medicines which meet each individual's needs. And lasers are also being used by the pioneers on the frontiers of human knowledge to try and detect gravitational waves, to create star-like conditions on Earth, and to make desk-size particle accelerators.

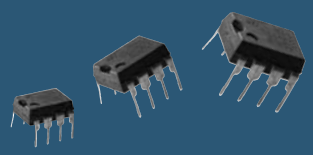
"Since its invention 50 years ago the laser has had a dramatic impact on all our lives and it's hard to imagine life without it. New applications are being researched and developed almost daily in medicine, communications, industry and science – undoubtedly the laser has become a key tool in driving a whole range of socio-economic applications – a far cry from its genesis of looking for problems to solve," said Dr Kate Lancaster, Central Laser Facility, Science and Technology Facilities Council.



The Vulcan laser at STFC's Central Laser Facility at the Rutherford Appleton Laboratory in Oxfordshire, is one of the highest intensity lasers in the world

DESIGNING FIRMWARE FOR MANUFACTURE

Vicky Larmour from Cambridge Consultants states how spending time on every detail in the early stages of design pays off later



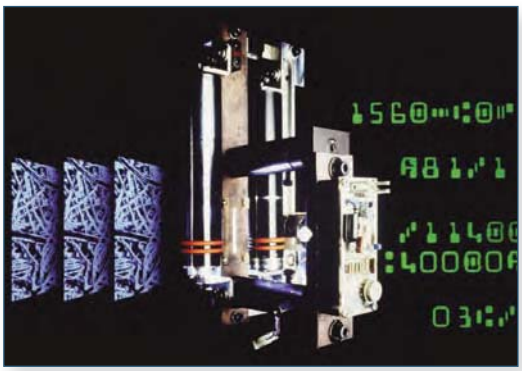
QUITE A LOT is written about designing electronics for manufacture, but often very little attention is paid to the firmware requirements; however, designing firmware for embedded devices with the manufacturing needs firmly in mind from the start can greatly simplify the process of taking a product to manufacture.

Programming considerations

When the device is to be manufactured in volume, either the firmware may be pre-stored (for example in an EEPROM or Flash chip), or the device may be manufactured with a blank part to be programmed after assembly.

If the firmware will be pre-stored then the manufacturer will need some way of identifying the parts based on the firmware version they contain (some manufacturers may allocate a different part number to the same physical part depending on the firmware it is loaded with). In this case, making frequent firmware releases containing updates may be quite disruptive to the manufacturing process; if you expect your firmware to change, it might be simpler to program a boot loader only onto the parts and allow them to be upgraded as required after assembly.

If the device is to be programmed or upgraded after assembly, consider the programming interface to be used and whether it has other implications – for example, will the relevant connectors be brought out to the exterior of the device, or must the boards be programmed before assembly.



These considerations may also affect the format of firmware releases; you may need to supply the firmware in multiple formats, for example an Intel Hex record or a Motorola SREC for the manufacturer to load over a JTAG interface, and a Windows executable for end users to update firmware over USB. Ensure that all formats in which the firmware is released contain their own version number in an accessible way, either in the file name or in a known fixed location in the file. Don't rely on folder names or zip file names to identify firmware releases since firmware files can easily become separated from their original containers.

Firmware/hardware compatibility

You will need to consider firmware and hardware compatibility right from the start; by the time you release spin 3 of your hardware and discover that the earlier firmware is not compatible it is too late to deal with the problem!

Ideally the firmware will have some way of identifying the hardware revision (for example using combinations of pull-up/pull-down

Top: *Designing with the manufacturing needs firmly in mind from the start can greatly simplify the process*

Middle: *If the device is to be programmed after assembly consider the programming interface that will be used*

Bottom: *Once manufactured the device will need to undergo a series of factory tests*

resistors on an analogue IO pin), but think about how the firmware should behave if it can't read the hardware revision or if it encounters a hardware revision it doesn't know about.

If you provide a custom interface for programming new firmware, it's useful to provide version checking in that interface to help prevent old incompatible firmware being loaded onto a newer device and vice versa. In a custom programming interface you will also need to consider firmware integrity checking and how the device should behave if it ends up with invalid firmware – can the boot loader detect this by means of a signature, for example.

Test requirements and interfaces

Once manufactured, the device will need to undergo a series of factory tests. You will need to agree these tests with the input of the hardware designers and the manufacturers, and make interfaces available for this testing that match the resulting requirements.

Aspects to consider here include:

- Will the test firmware be a special mode of the main firmware, or a separate firmware load?
- Does the test plan cover all internal communications interfaces, GPIO pin functionality, signal timings, external connectors?
- Will the testing be fully automated or will parts of it require human intervention?

Product lifetimes/volumes

Some of the considerations may be different depending on the intended lifetime and manufacturing volume of the product. For example, the longer the expected product lifetime, the greater the risk of component obsolescence issues leading to part substitutions and possible firmware compatibility issues. ■

The Common Cathode Gain Stage CCS

Burkhard Vogel presents a series of short features with general remarks on triodes in audio applications

LIKE IN THE well-known bipolar junction transistor world we find active device configurations of the same kind in the valve world: the common emitter stage equals the common cathode stage; the common collector stage (known as emitter follower) equals the common anode/plate stage (known as cathode follower); and the common base stage equals the common grid stage. The FET world offers similar gate, source and drain configurations.

The CCS circuit is given in **Figure 1** and **Figure 2** shows the respective small signal equivalent circuit. They look a bit like **Figures 5** and **6**, but, because of the inclusion of a cathode resistance R_c and load resistance R_L, they will offer a significant different behaviour.

Two basic stage types are shown here. One with R_c bypassed by C_c (subscript "$_b$") and another one without bypassing C_c (un-bypassed and subscript "$_u$").

Because of the interruption of the current feedback by bypassing R_c with a capacitance of a size that does not hurt a flat frequency and phase response in B_{20k} (= 20Hz…20kHz), the gain and the distortion of the stage will increase.

As function of the output load R_L, with r_g = infinite and an un-bypassed resistor R_c , the general gain equation for the CCS becomes:

$$G_u(R_L)=\frac{v_o}{v_i}=-\mu\frac{R_a}{r_a+R_a+(1+\mu)R_c+\frac{R_a}{R_L}\left[r_a+(1+\mu)R_c\right]} \quad (1)$$

To increase the gain we can bypass R_c by C_c, thus, in Figure 2 R_c becomes 0Ω. This leads to the R_L dependent gain $G_b(R_L)$:

$$G_b(R_L)=\frac{v_o}{v_i}=-\mu\frac{R_a}{r_a+R_a+\frac{r_a R_a}{R_L}} \quad (2)$$

Quite often we find CCS gain equations without R_L effect. They really look a bit shorter and nicer than **Equations 1** and **2**. However, this does not reflect the real life of a valve gain stage. Nevertheless, to cut short the formula development of the output resistances $R_{o.u}$ and $R_{o.b}$ of the two CCS versions we need Equations 1 and 2 without the R_L effect, hence, G_u and G_b become:

$$G_u=-\mu\frac{R_a}{r_a+R_a+(1+\mu)R_c} \quad (3)$$

$$G_b=-\mu\frac{R_a}{r_a+R_a} \quad (4)$$

To derive the output resistances $R_{o.u}$ and $R_{o.b}$ for the un-bypassed and bypassed cases we can simply apply the following: "In case of a constant input voltage v_i the gain stage output resistance $R_{o.u}$ equals the load resistance R_L if the R_L-loaded output voltage $v_o(R_L)$ equals half of the unloaded output voltage v_o, hence, $v_o(R_L) = 0.5*v_o$".

The same applies to $G(R_L) = 0.5*G$ (R_L=infinite) = 0.5*G. Hence, $R_{o.u}$ and R_{ob} become:

$$R_{o.u}=R_L=R_a\frac{r_a+(1+\mu)R_c}{r_a+R_a+(1+\mu)R_c} \quad (5)$$

$$R_{o.b}=R_L=\frac{r_a R_a}{r_a+R_a} \quad (6)$$

We've seen in the last issue of *Electronics World* (Part 1) that most of the input

Figure 1: *CCS including R_c bypassing possibility*

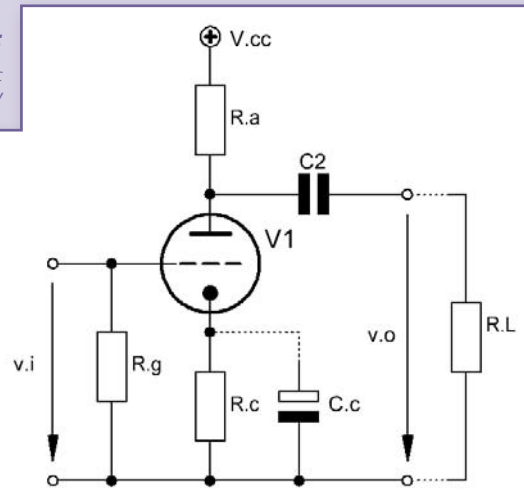
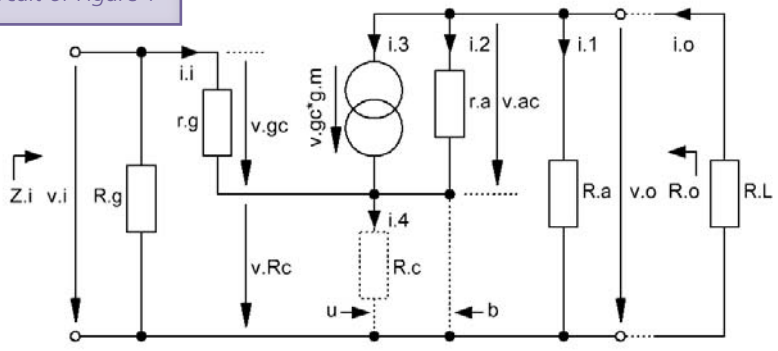


Figure 2: *Equivalent circuit of Figure 1*



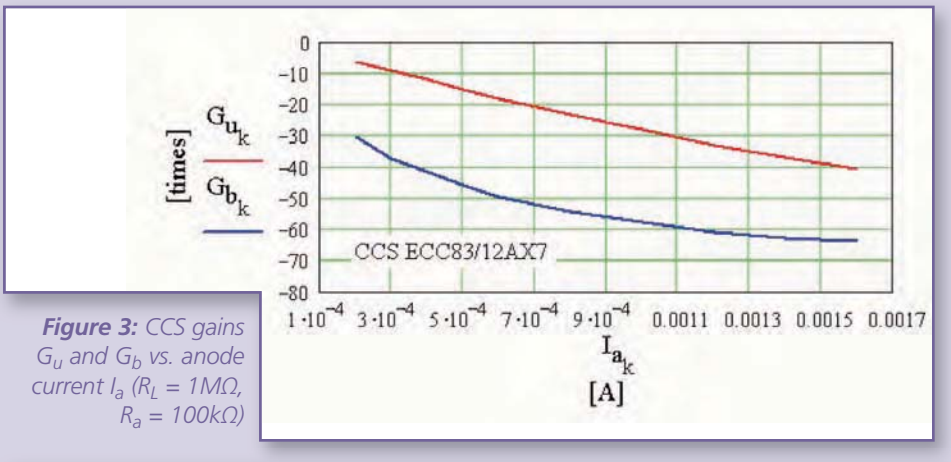


Figure 3: *CCS gains G_u and G_b vs. anode current I_a (R_L = 1MΩ, R_a = 100kΩ)*

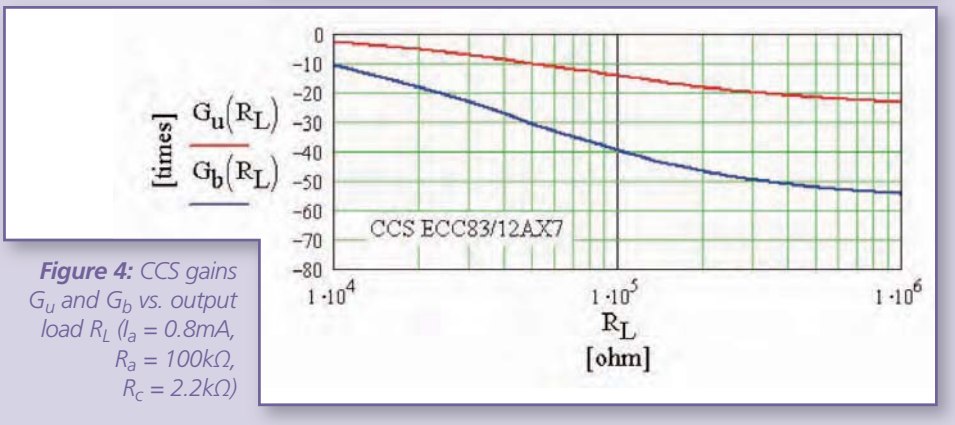


Figure 4: *CCS gains G_u and G_b vs. output load R_L (I_a = 0.8mA, R_a = 100kΩ, R_c = 2.2kΩ)*

capacitance C_i depends on the valve's Miller capacitance. Basically, the CCS offers two different input capacitances. They also depend on the output load R_L and the "u" or "b" state of the gain stage:

$$C_{i.u}(R_L) = (1+|G_u(R_L)|)C_{ga} + C_{gc} + C_{stray}$$
$$C_{i.b}(R_L) = (1+|G_b(R_L)|)C_{ga} + C_{gc} + C_{stray} \quad (7)$$

I ignore the capacitance reducing R_c effect on C_{gc} for $C_{i.u}(R_L)$ in **Equation 7**. It can simply be covered by a reasonable choice of an input stray capacitance C_{stray} (≈ 2pF…10pF). With these findings the input impedances $Z_{i.u}$ and $Z_{i.b}$ become:

$$Z_{i.u}(R_L) = |R_g \| C_{i.u}(R_L)|$$
$$Z_{i.b}(R_L) = |R_g \| C_{i.b}(R_L)| \quad (8)$$

Taking the Miller effect into account and ignoring any R_c effect of the gain stage's "u" state, the output capacitance C_o can be calculated as follows:

$$C_o = C_{ac} + C_{ga} + C_{stray} \quad (9)$$

In most cases the output C_{stray} dominates and all Cs together won't play a significant role. That's why C_o becomes rather small and can be ignored. Therefore, I do not present output impedance equations. In addition, because of a particular correlation, I'll present in the next issue of *Electronics World* the rules to get the value of C_c via the equation that enables calculating the cathode output resistance $R_{o.c}$.

With a constant anode operating voltage V_a = 200V of the Figure 1 circuit, we can plot the following graphs for ½ ECC83/12AX7 double-triode (Note: with a constant V_a a constant R_a means automatically a changing V_{cc} for a changing I_a; "$_k$" indicates the number of the ten I_a values from 0.2mA to 1.6mA): ■

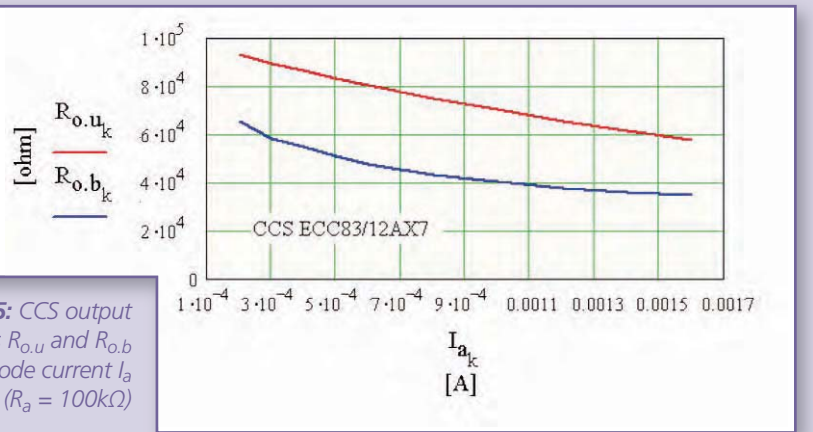


Figure 5: *CCS output resistances $R_{o.u}$ and $R_{o.b}$ vs. anode current I_a (R_a = 100kΩ)*

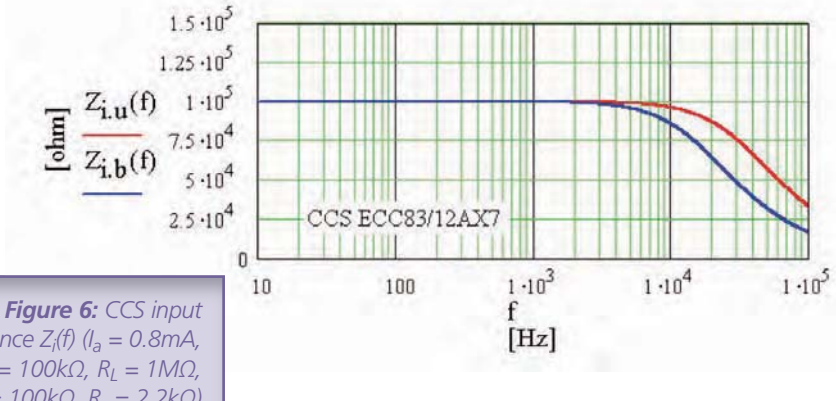


Figure 6: *CCS input impedance $Z_i(f)$ (I_a = 0.8mA, R_g = 100kΩ, R_L = 1MΩ, R_a = 100kΩ, R_c = 2.2kΩ)*

*Coming in the next issue of Electronics World: "**The Common Grid Stage CGS".** If you have missed the first part of this series, please go onto our website and order a copy of it:* ***www.electronicsworld.co.uk***

The 'Flying' GOALPOSTS

Myk Dormer

QUESTION: What are the fastest moving objects ever encountered in engineering?

Answer: Project design specifications.

It is a common complaint of engineers in all sectors of industry – common enough to have become something of a standing joke – that their lives are made considerably more difficult by random, uncontrolled changes to a project's specifications during the design process.

While it is easy to point a finger and jeer at the amorphous mass of management, sales and marketing, who seem to thoughtlessly originate these changes, it will be far more useful to examine the causes and ways of coping or deflecting these problems when they occur.

It is convenient to examine the 'moving goalpost' problem in the context of the familiar low power radio industry, as the projects tend to be relatively simple, teams are small and uncomplicated, and customer-driven custom projects are fairly usual.

So what do we actually mean by a 'moving goalpost'?

Three specific categories can be identified:

Time constraint changes – where the amount of time initially estimated for the completion of the project is suddenly curtailed. This occurs either where the delivery date is moved, or where the design team workload increases, reducing the manpower resources assigned to the specific project.

Core specification changes – where the basic performance requirements, or the approval specification being designed to, are altered. This can be as simple as a need for more transmitter output power, or as complex as a change from one compliance document to another; i.e. from EN300-220 to EN300-113.

Feature creepage – the inclusion of apparently desirable extra functions, outside the original scope of the design, such as the addition of a display, an additional interface, or an extra power source.

The actual reason for a goalpost change is harder to pin down:

Incomplete specifications. At the outset of any design project, it is necessary to establish within a reasonable framework just what is being made. All too often, this process concentrates on a handful of vital characteristics, for example "the link must transmit 4800 baud data over a 10km sea-path", while ignoring apparently mundane details which have considerable influence over the subsequent design choices, such as "nominal operating temperature is -45 degrees", for example.

Attempt at an early stage to capture as much data as possible regarding the final application and insure that the design covers all these eventualities. Any areas where the customer (or application) seems vague or uncritical should also be detailed in some respect.

"EVERY 'IMPROVEMENT' TAKES EXTRA EFFORT, INTRODUCES UNFORESEEN PROBLEMS AND RISKS INDETERMINATE DELAY"

Late customer consultation. The end user must be involved from the beginning of the specification process and their actual requirements must be the foundation of the design. Once the program has started, however, they must not be allowed to 'edit' their specification, unless the entire project is revised.

I once worked on a project where a discussion with the customer produced a draft design based on minor changes to existing product. Work commenced. The customer was then approached again by sales and effectively asked for a 'clean slate' wish list. This resulted in a second specification far removed from the original, requiring far more design work, but which was promised within the same time scales as the first.

In-company enthusiasm. "If the new product can do X, then wouldn't it be so much better if it could do Y as well". People are unavoidably ambitious and enthusiastic. Salesmen and applications engineers will see exciting possibilities for a new product "which only requires this tiny change, or addition".

This way lies disaster. Every 'improvement' takes extra effort, introduces unforeseen problems and risks indeterminate delay. While it is important not to stifle such enthusiasm, it must be curbed.

Offer the existing design "today" with the promise of the better thing "tomorrow" – when it can be properly designed, with sufficient resources.

Malicious actions. In the ideal world, everyone in a company will be working toward the same – profitable – ends. Any engineer with more than a few years of experience will know that the real-world is very different.

Not every decision taken in a company directly aids the whole. Internal power politics and personal feuds can result in changes to specifications or, more commonly, resource allocations which are calculated to disrupt the project, either slowing completion, or forcing a cancelation.

If a work environment is dominated by such issues, then the only professional response is to seek alternative employment. The challenges thrown up by both physics and commerce are too great to tolerate malicious meddling as well.

Insufficient research. It is an unpalatable (to most managers) fact that engineering is not necessarily a completely deterministic process. Not every design idea can be made to work in a given number of days. Some things never work at all.

It is vital to plan for some 'feasibility' work before finalising the project specification, in order to check that all the basic concepts and circuit techniques that are needed will actually function as intended.

In conclusion: How can the goalposts be kept still?

- Talk to the end user. Get the whole story.
- Do some research, some experiments, calculations. Make sure it's possible.
- Write a complete specification and get it agreed to by all parties.
- Plan the project conservatively. Allow enough time and resources.
- Stick to the program. Be professional, but be firm. Avoid distraction.
- Then, if you are really fortunate, you might see the product reach the marketplace in vaguely the shape originally intended, within your lifetime. Good luck!

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

IDT Integrated Device Technology

IDT: The Leader in Serial RapidIO®

Ron Jew - General Manager of Wireless Products, IDT

For years, the leading Serial RapidIO® suppliers have been Integrated Device Technology (IDT) and Tundra Semiconductor. With the IDT acquisition of Tundra in 2009, the strengths of both companies have been combined to further grow the Serial RapidIO ecosystem.

The IDT commitment to grow the Serial RapidIO market has several facets. We have taken our switching devices and combined them with the former Tundra products to provide customers with a complete unified portfolio of switches that span all bandwidths and port configurations. In addition, IDT is continuing to develop innovative switches, intellectual property (IP), clocking products and other Serial RapidIO solutions for their customers in wireless, defense, and other markets requiring a peer-to-peer network of multiple processors that leverage a low latency, low power and highly reliable interconnect.

Most recently, IDT announced a new family of Serial RapidIO Gen2 switches, which build on its industry-leading portfolio of version 1.3 switches. The new switches leverage best-in-class technology from the IDT CPS and TSI product lines and are designed for use in wireless infrastructure, defense and aerospace, imaging, and video markets. The devices support the Serial RapidIO 2.1 standard and double the capacity on a per-port basis when compared to Serial RapidIO 1.3 solutions, as well as competing 10 Gigabit Ethernet options.

The initial products are the full duplex, non-blocking 240 Gbps CPS-1848 switch, which offers 18 ports and 48 lanes for large processor clusters or backplanes, and the full duplex, non-blocking 80 Gbps CPS-1616 switch, which offers 16 ports and 16 lanes optimized for line cards and smaller processor clusters.

The CPS-1848 was designed to meet the Serial RapidIO 1.3 and 2.1 specifications, and provides support for twelve 4-lane ports operating at 20 Gbps data rate per port, eighteen 2-lane ports each supporting 10 Gbps, or eighteen 1-lane ports, each supporting 5 Gbps. Combinations of 4-lane, 2-lane, and 1-lane ports are also supported. This device has already been designed into both wireless infrastructure and military designs.

Figure 1: *The new IDT Serial RapidIO Gen2 Switches*

The CPS-1616 also meets the Serial RapidIO 1.3 and 2.1 specifications and supports four 4-lane, eight 2-lane, or sixteen 1-lane ports. Combinations of various port widths are also supported. This device has already been designed into wireless infrastructure and military designs.

Both switches support all Serial Rapid IO speeds — 1.25, 2.5, 3.125, 5 and 6.25 gigabaud (Gbaud). The new Serial RapidIO Gen2 switches also feature a cut-through latency of 100 nanoseconds (ns) and a 40-percent power reduction per 10 Gbps of bandwidth compared with the previous generation of Serial RapidIO 1.3 switches.

Other CPS-1848 and CPS-1616 features include IDT-developed high-performance SerDes that provides a long-reach distance of 100 cm over 2 connectors with Decision Feedback Equalization (DFE) support. The switches include transmit pre-emphasis, receive equalization, on-die scope and bit error rate (BER) test features. They also include dynamic ingress and egress buffer management to improve throughput and latency under real-time dynamic system-level traffic conditions.

The new IDT Gen2 Serial RapidIO switches support a maximum per-port data rate of 20 Gbps, compared with 10 Gbps for Serial RapidIO 1.3 devices. In addition, the Gen2 switches complement the Gen1 switch portfolio, raising the maximum number of 4-lane ports from 8 to 12. This allows 3.5G and 4G wireless networks to be deployed with smaller base stations containing fewer switches but with more processing capacity per base station, improving the economics of network rollout and coverage.

WHY DEVELOP SERIAL RAPIDIO GEN2 SWITCHES?

As the industry leader in Serial RapidIO devices, developers in the wireless, video and imaging, and defense and industrial markets look to IDT for devices that help to solve their current and next-generation design challenges. In the wireless market, designers need to support more subscribers with more services per baseband card. In addition, more data must be passed between endpoints and backplanes in their next-generation designs, which include much denser systems. Management of this ever increasing traffic requires increased switch performance and traffic management features.

Video and imaging developers are creating systems that must process more frames per second, including larger frame sizes at a higher resolution.

In the defense and industrial market, payload processing cards must support sensor input data at higher rates to keep up with real-time performance. Many signal-processing applications already include Serial RapidIO 1.3 on their backplanes, making the transition to Serial RapidIO Gen2 an obvious choice. In addition, the Open VPX standard, which is prevalent in this market segment, already includes Serial RapidIO in its backplane.

In all of these applications, systems designers have a need to cluster multiple high performance processors in a peer-to-peer network. In their Serial RapidIO 1.3 systems, they leveraged the Serial RapidIO Messaging construct that allow them to pass large amounts of data with a "push architecture" where the receiving processor manages its own memory

space, which makes scalable applications much easier to develop. Because of this, Serial RapidIO has become the standard interconnect in the aforementioned applications.

IDT SERIAL RAPIDIO GEN2 PORTFOLIO

Customers continue to choose IDT for their Serial RapidIO needs because we offer more than just switches. Along with multiple switch variants currently in development, IDT has developed Serial RapidIO Gen2 endpoint IP, which is available for ASIC development.

The IDT Gen2 endpoint IP builds upon the Tsi and CPS Gen1 experience to develop a fifth- generation innovative switch fabric in its Gen2 switches. Making this advanced fabric a reality required the invention and filing of several patent applications, such as those for per-port route tables, which increases the flexibility and number of unique traffic routes supported. Also, multiple modes of traffic scheduling allow the user to control and ensure quality of service through various fairness algorithms. Other filed patent applications include innovative mechanisms to minimize cut-thru latency and memory utilization, and improve switching performance and cost-efficiency leveraging mechanisms, such as dynamic memory buffer allocation and the unification of available memory resources.

IDT SERIAL RAPIDIO TOOL SUPPORT

In support of its Serial RapidIO switches, IDT has helped develop an ecosystem of hardware and software tools. This includes the Serial RapidIO Gen2 hardware development platform, which features IDT switching between Advanced Mezzanine Cards, Infiniband, SMA and SFP connections. This hardware is ideal for prototyping systems when used in conjunction with other vendor's endpoint, evaluation boards and related tools. Fabric Embedded Tool Corporation's RapidFET JTAG tool provides switch configuration, bring-up and diagnostics with simple connectivity direct to the switches from a PC.

IDT offers a Gen2 System Modeling Tool for assistance in determining an overall system architecture that optimizes performance and power. Use of this powerful modeling tool allows designers and architects to create a virtual Serial RapidIO Gen1- or Gen2-based system. The tool allows optimization of traffic flows within the design, and evaluation of different system architectures. Systems can now be perfected virtually before creating a physical prototype, improving IDT customers' design efficiency and speeding their time to market. Designers and system architects can now rapidly and confidently design their entire RapidIO based system.

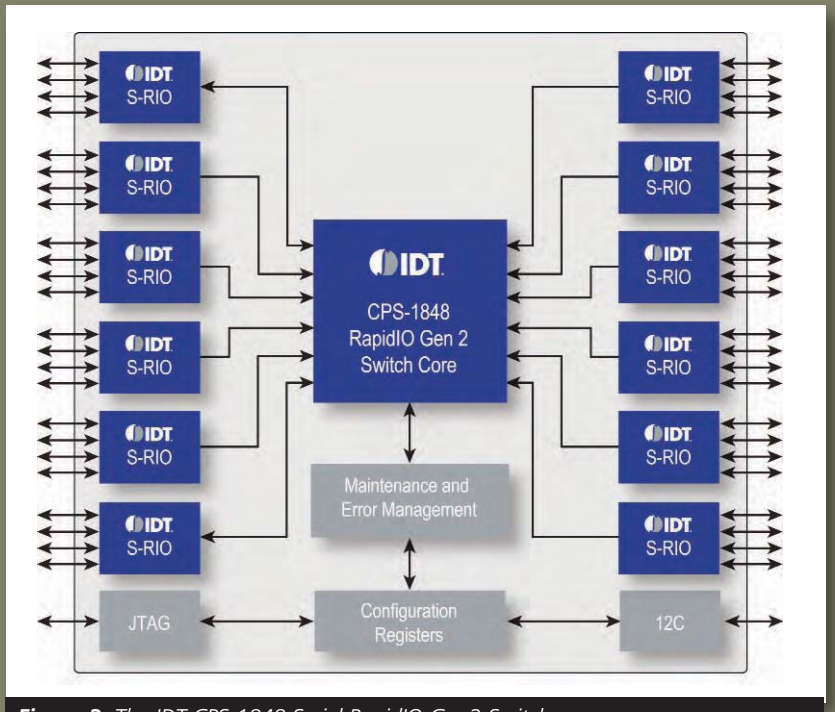


Figure 2: *The IDT CPS-1848 Serial RapidIO Gen2 Switch*

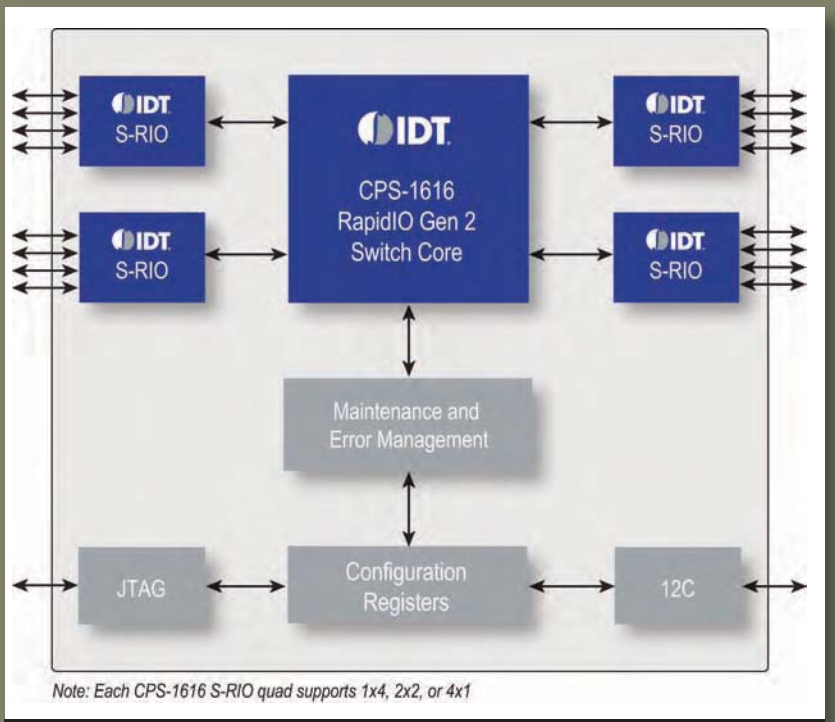


Figure 3: *The IDT CPS-1616 Serial RapidIO Gen2 Switch*

SUMMARY

IDT is the leader in Serial RapidIO, and continues to invest heavily in and develop innovative products in support of the Serial RapidIO ecosystem. The newest IDT Serial RapidIO Gen2 switching, IP, prototyping and diagnostics support solutions enable designers to rapidly develop system leveraging Serial RapidIO's high performance and reliability.

Contact IDT Europe ltd • Tel: (44) (0)1372-363339 • Fax: (44) (0)1372-378851 • Email: idteurope@idt.com • Website: www.idt.com

Seyi Verma, Product Marketing Manager for High-End FPGAs at Altera explains what makes FPGAs a true technical alternative to ASICs and ASSPs without compromising power, cost and development requirements in a broad range of applications

FPGAs Beyond MOORE'S Law

IT IS MORE and more likely these days to see someone using a mobile phone to download and listen to music, open an e-mail attachment or even watch video or a TV program, whilst for the home many people are purchasing HD television sets boasting Internet connectivity.

Elsewhere, the broadcast industry is evolving, both movies and television programs are now being filmed and broadcast in 3D and this will soon become the next must-have technology. Both applications push bandwidth requirements at an increasing data rates in the communication infrastructure.

However, it is not just in broadcast and communications that we are seeing such a dramatic demand for greater bandwidth; applications for industrial surveillance, military radar and a variety of compute and storage usages are also emerging.

Driving Requirements

The requirement for greater bandwidth infrastructure continues to grow significantly and is having an effect on the technology that drives it. FPGA vendors have progressed from previous silicon processing technologies to 28nm to provide the benefits of Moore's Law, doubling the FPGA capacity and performance every 18 months.

For years, progressing to smaller geometries has enabled FPGA vendors to provide solutions with increased functionality, customizable capabilities, re-programmability and higher processing performance while reducing cost. But, smaller silicon geometries result in increased leakage currents resulting in higher static power, which in turn raises the total power of FPGAs.

Riding the Moore's Law train will not mitigate the problem of increased power because processing techniques only go so far. FPGA vendors must find innovative ways to go beyond Moore's Law and meet the ever-increasing demand of bandwidth requirements while reducing cost and power. So the million dollar question is how can all this be achieved?

Achieving Power Efficiency

While the 28nm process delivers clear performance benefits, to realize the full potential of the 28nm process, the proper "process option" must be selected. Altera chose the 28HP (high performance) high-K metal gate (HKMG) process from TSMC and optimized the process for low power. This process allows FPGAs to provide 28Gbps power-efficient transceivers for ultra-high bandwidth applications.

The exceptional performance at 28nm is driven not only by the introduction of HKMG, but also by the second generation of advanced strain technology, including embedded silicon germanium (SiGe) in source-drain regions of transistors for faster circuit designs.

Altera produces tensile strain in NMOS transistors through a cap layer and compressive strain for PMOS transistors through embedded SiGe in the source and drain. These strained silicon techniques increase electron and hole mobility by up to 30%, while the resulting transistor performance is increased by up to 40%. Since better performance at the same level of leakage is achieved with strained silicon, part of this performance gain is traded off for reduced leakage, leading to a process that has faster performance and lower leakage compared to processes without strained silicon.

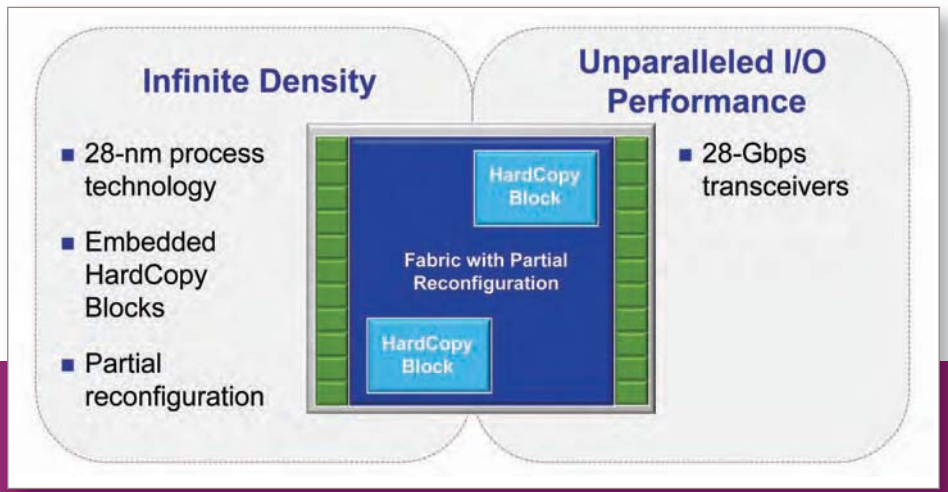


Figure 1: *Technology innovations in the Stratix V FPGAs*

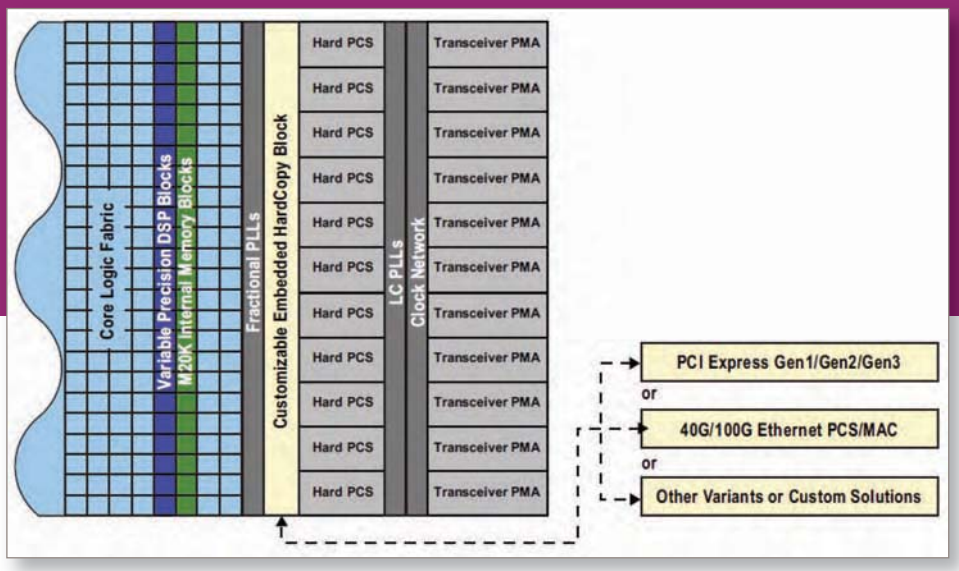


Figure 2: *Floorplan view of the Stratix V embedded HardCopy block*

Increasing Bandwidth

The next step is to increase transceiver bandwidth per channel while minimizing the power. At 28nm, each 28Gbps channel consumes 200mW of physical medium attachment (PMA) power, which is about 7mW per gigabit. Moving from 10 x 10Gbps transceivers to 4 x 25Gbps transceivers allows designers to achieve the same bandwidth at half the power. Secondly, the board layout generally becomes easier, thereby reducing design costs.

For example, a 100Gbps interface could be supported by 4 channels rather than 10. At mainstream data rates such as 12.5Gbps, transceivers are 10GBASE-KR-compliant to drive 40" of backplane and are designed to support optical modules directly by including optical electrical dispersion compensation (EDC) features. This further reduces cost by eliminating the need for an external EDC chip when interoperating with all types of optical modules, including SFP+.

Another solution is to integrate more hard

Figure 3: *Next-generation FPGA design without embedded HardCopy blocks*

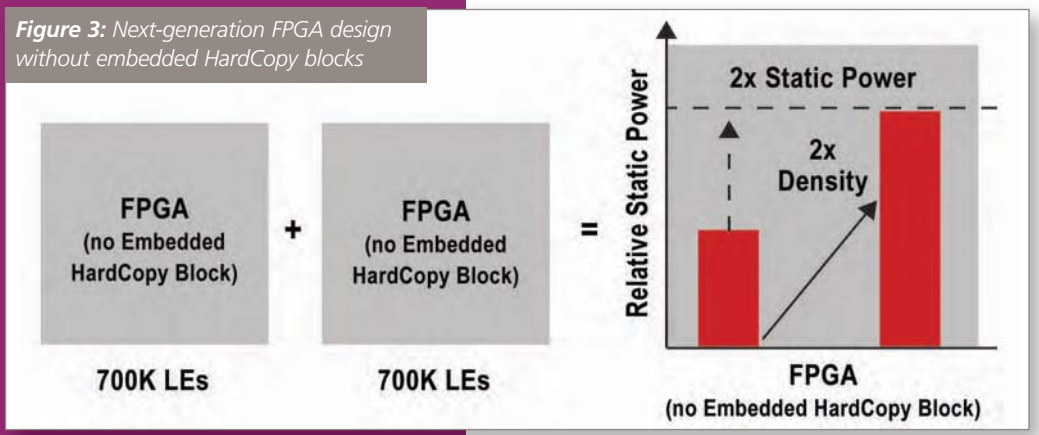
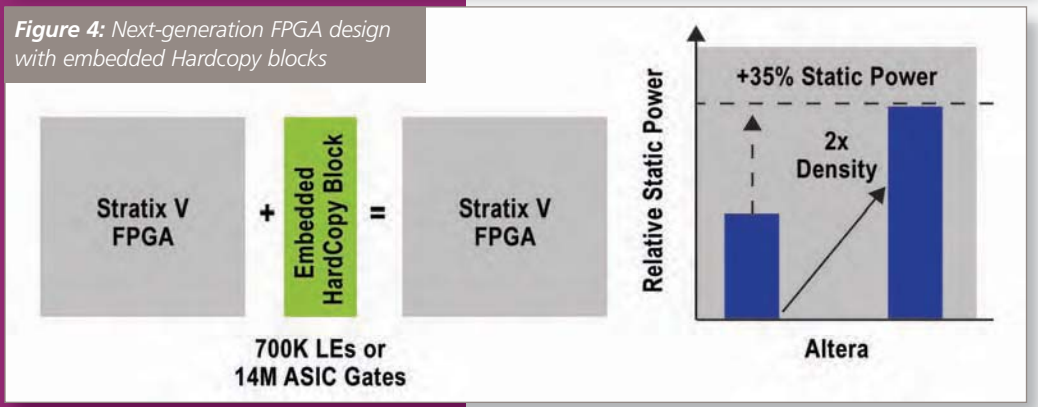


Figure 4: *Next-generation FPGA design with embedded Hardcopy blocks*



intellectual property (IP) into the FPGA. This enables the users to increase the functionality per unit area without the penalty of increased power and cost. Today, many FPGAs include DSP, memory bocks, embedded PLLs and even PCI Express MAC layers as hard IP. For Stratix V FPGAs, Altera takes this one stage further by using embedded HardCopy blocks.

Embedding ASIC Gates

The embedded HardCopy blocks offer up to 14 million equivalent ASIC gates or up to 700K logic elements (LEs) and are used to harden standard or logic-intensive functions, such as interface protocols, application-specific functions and proprietary custom IP. To fully understand the benefits of the embedded HardCopy blocks, let's consider a simple example.

If the density of the design is doubled on an FPGA with no embedded HardCopy block(s), then a designer must use a larger FPGA that not only increases costs, but also consumes twice the static power.

By using an FPGA with embedded HardCopy blocks, designers can easily double the size of their FPGA design, by hardening some of the key components of the design and only have a minimal impact on power.

The embedded HardCopy blocks provide benefits that enable the hardening of IP, thus reducing power by up to 65% when compared to soft logic. These blocks also guarantee timing requirements for high performance applications, while increasing the FPGA capabilities. This dramatic increase in density per area enables customers to create a new class of application-targeted devices for their own market-specific programmable solutions.

Partial Reconfiguration

High-bandwidth applications that support multi-standard client interfaces can require updates or changes to FPGA functionality on-the-fly, while other portions of the FPGA are still operating. For this, Stratix V FPGAs incorporate an easy-to-use, fine-grain partial reconfiguration to change the functionality of the core and dynamic reconfiguration to change the transceiver configuration.

Partial reconfiguration in an FPGA also improves effective logic density by removing the necessity to place functions that do not operate simultaneously in the FPGA. Instead, these functions are stored in external memory and loaded as needed. This reduces the size of the FPGA by allowing multiple applications on a single FPGA, thus saving board space and cost while reducing power.

Partial reconfiguration is by customer demand, rather than process. A number of applications are now emerging that makes it a viable option for use in FPGAs. These include:

- OTN Muxponder applications, where it is sometimes necessary to change the functions of a line card client channel, while others continue to operate.
- High performance computing applications, where data is passed from the main processor to an FPGA co-processor enabling the ability to modify a process that would dramatically improve efficiency.
- Software Defined Radio applications, where the waveforms may need to change depending on the required standard.

Tools – The Integral Part Development

Tool flows are an essential part of any FPGA project. The largest Stratix V device will have in excess of one million LEs or 12 million equivalent ASIC gates, if you exclude the embedded HardCopy blocks. It is important for the tool to minimize the development times, so the customer can deliver their products to the market ahead of the competition, freeing up their design resource and increasing the revenue time of the product.

Altera's Quartus II Development software includes an incremental compilation flow, to help reduce development time. Incremental compilation only compiles changes within a design and leaves the remainder of the design intact thus dramatically reducing compile times. In a large, highly-populated FPGA this could allow two or three re-compiles per day, taking man-weeks of effort out of a development schedule.

The flow works on partitions within a design and enables a team-based design flow, where the project can be partitioned into smaller designs and divided between several engineers. Once the engineers have completed their individual designs, the overall design can be easily reassembled with minimal compilation effort. Incremental compilation will play a significant role in Stratix V-based designs by reducing compile times and providing a simplistic flow for partial reconfiguration, which has always proved challenging to EDA tools in the past. ■

FPGA Solutions for TOUCH-SCREEN Display Technologies

Niladri Roy from Lattice Semiconductor Corporation summerises the types of touch-screen technologies being used in designs and how FPGAs can add flexibility to those designs

TOUCH-SCREEN displays are now ubiquitous in handheld consumer and medical applications, vending/ticketing/ATM machines, point of sale (POS) terminals and industrial and process control equipment. Other applications where touch-screen displays are making inroads are office automation, automotive and marine instrument clusters, home appliances and gaming.

Factors Influencing the Choice of Touch-Screen Technologies

Touch-screens can be implemented in a variety of ways. The choice of technology depends, apart from cost, on several factors:

- **Performance:** Performance includes parameters such as speed, sensitivity, accuracy, resolution, drag, Z-axis, double/multi touch, parallax and stability of calibration.
- **Input Flexibility:** Input flexibility parameters address human interaction elements such as gloves, glove material, fingernails, styli, handwriting recognition and signature capture.
- **Environmental:** Environmental considerations are temperature, humidity, chemical resistance, scratch resistance, splash/droplet tolerance, altitude, in-vehicle mounting, shock, vibration, breakage resistance and safe break pattern.
- **Electrical and Mechanical:** Electrical and mechanical requirements encompass power, floating ground, electrostatic discharge (ESD), electromagnetic interference (EMI), size, curvature, etc.
- **Optical:** Optical characteristics influencing the choice of technology include transmissivity, clarity, colour purity and reflectivity.

Types of Touch-Screen Technologies

Depending on the combination of the above factors, the major touch-screen technologies can be subdivided into the categories below:

Resistive: Resistive touch-screen is the dominant touch technology in deployment today. It consists of a glass panel with a resistive coating of iridium tin oxide (ITO) and a coversheet with a conductive coating, with silver bus-bars along the edges. The two layers are separated by tiny insulating dots. When the screen is touched, the coversheet flexes to make contact with the coating on the glass (**Figure 1**).

The controller alternatively drives the glass layer and coversheet with +5V and reads the resulting voltage from the coversheet and glass layer, determining the X and Y coordinates respectively, based on the voltage drop in the measured layer. This technology requires four wires – the aforementioned bus-bars – and is referred to as 4-wire resistive touch-screen technology.

Four-wire resistive touch-screen technology suffers from degradation of linearity and accuracy, caused by constant flexing of the

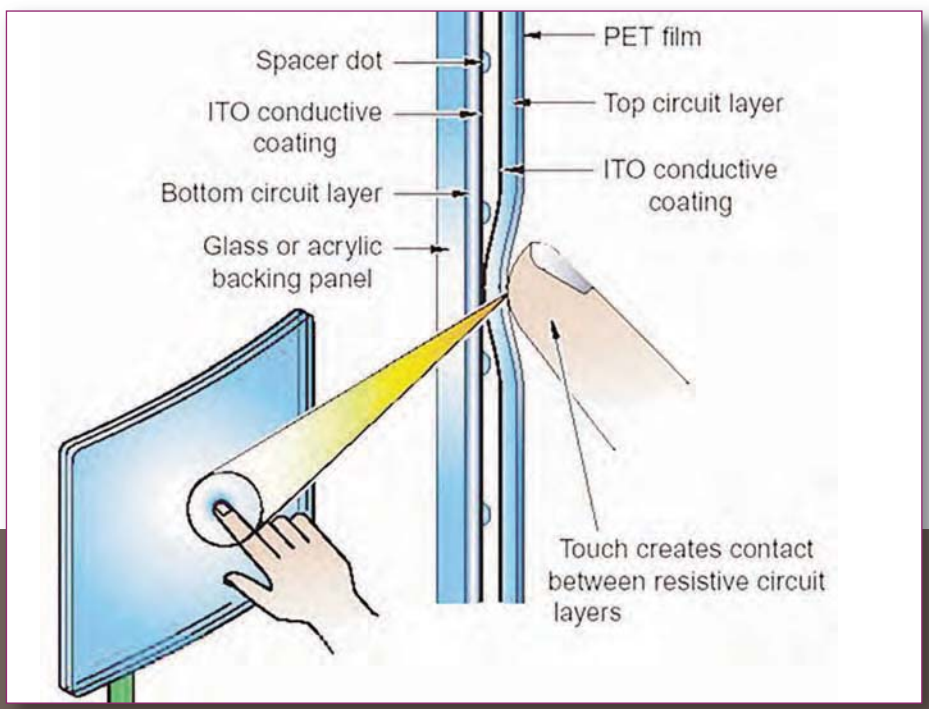


Figure 1: *Resistive touch technology*

Table 1: Benefits and applications of different touch technologies

TOUCH TECHNOLOGY	BENEFITS	APPLICATIONS
Resistive	4-wire: Stable operation, Quick touch response, Input flexibility, Narrow border width, Low weight, and Low power consumption. More-wire: Adds stable, drift-free operation	4-wire: Light industrial, Portable medical devices, Access control terminals, Portable field automation, Wearable computers and Home appliances. More-wire: POS and Retail where very large numbers of transactions occur
Acoustic Pulse Recognition	Optics and durability of pure glass, works with finger, glove, pen; is resistant to water, dust, grease; has virtually no wear, works even with scratches; has excellent drag performance.	Restaurant and Hospitality automation, Retail, POS terminals, Pharmacy automation, Industrial automation and Office automation.
Surface Acoustic Wave	Superior image clarity, resolution, and light transmission through pure glass. Durable, scratch-resistant and continue to work if scratched. Finger, gloved hand, and soft stylus activation, with fast, sensitive touch response, recognizing location and amount of pressure applied.	Point-of-information kiosks, Vending and ticket sales, Electronic catalogs, Gaming, Lottery, and amusement, Public pay phones, Multimedia marketing, Banking/financial transactions, Industrial control rooms and computer-based training.
Surface Capacitive	Fast, sensitive touch response with excellent drag performance.	POS terminals, Kiosks and Gaming.
Projected Capacitive	Works with gloves for true input flexibility and works even if glass is scratched or broken.	Outdoor kiosks, Ticketing machines, ATM, Phones, Pay-at-the pump gas machines and through-glass under-counter, and bar-top applications.
Infrared	Low profile, high resolution; no parallax; highest clarity; high durability; operates in extreme environments; multi-touch capable.	Food processing, Industrial Automation, Medical Equipment, In-vehicle, POS terminals.

coversheet that cause microscopic cracks in the ITO coating. It also suffers from accuracy drift caused by environmental changes.

Variations, such as 5, 6, 7 and 8-wire resistive touch-screens have evolved to counteract these effects.

Acoustic Pulse Recognition (APR): APR consists of a glass display overlay or other rigid substrate, with four piezoelectric transducers mounted on the back surface. The transducers are mounted on two diagonally opposite corners out of the visible area and connected via a flex cable to a controller card. The impact when the screen is touched, or the friction caused while dragging between a user's finger or stylus and the glass, creates an acoustic wave. The wave radiates away from the touch point, making its way to the transducers, which produce electrical signals proportional to the acoustic waves. These signals are amplified in the controller card and then converted into a digital data stream. The touch location is determined by comparing the data to a profile. APR is designed to reject ambient and extraneous sounds, as these do not match a stored sound profile.

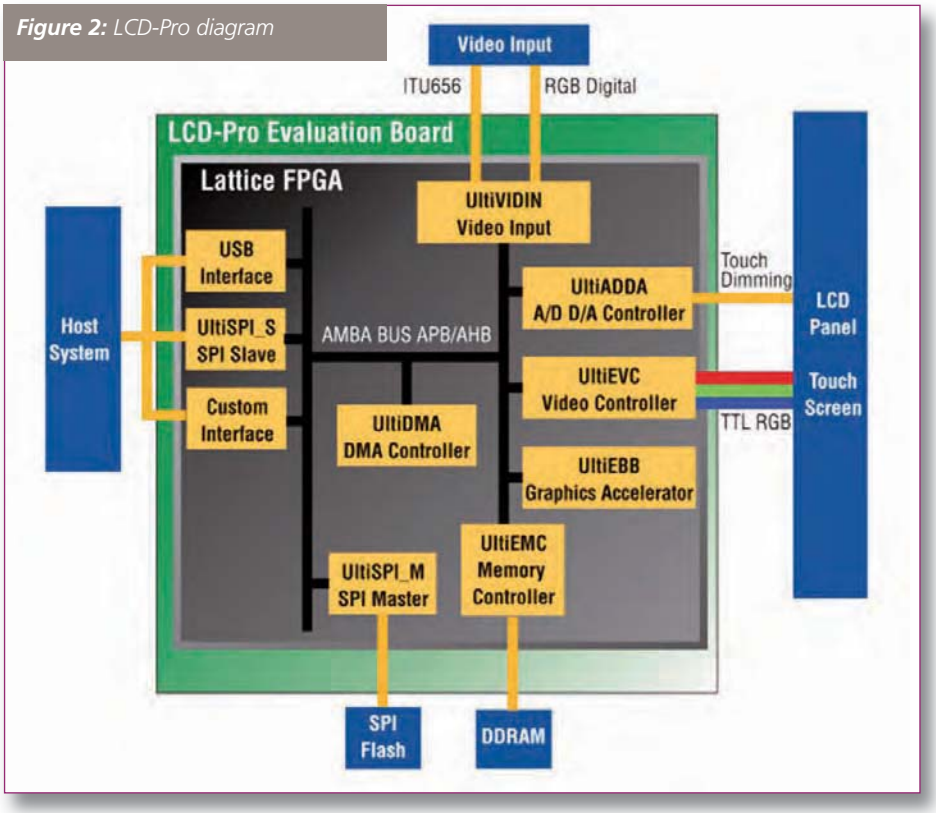
Surface Acoustic Wave (SAW): SAW touch-screens consists of a glass overlay with transmitting and receiving piezoelectric transducers for the X and Y axes. The controller sends an electrical signal to the transmitting transducer, which converts the signal into ultrasonic waves within the surface of the glass. These waves are directed across the touch-screen by an array of reflectors. Reflectors on the opposite side gather and direct the waves to the receiving transducer, which reconverts them into an electrical signal. The process is repeated for each axis. A touch absorbs a portion of the waves traveling across it. The received signals for X and Y are compared to the stored digital maps, the change recognized and a coordinate calculated.

Capacitive: Capacitive touch-screen technology can be further subdivided into Surface Capacitive and Projected Capacitive. Surface Capacitive technology consists of a uniform conductive coating on a glass panel. Electrodes around the panel's edge evenly distribute a low voltage across the conductive layer, creating a uniform electric field. A touch draws current from each corner. The controller measures the ratio of the current flow from the corners and calculates the touch location.

Projected capacitive touch-screens consist of a sensor grid of micro-fine wires laminated between two layers of protective glass. The assembly can be placed behind customer-installed materials, including vandal-resistant glass up to 18mm thick. During a touch, capacitance forms between the finger and the sensor grid. The touch location is calculated from the changing electrical characteristics of the sensor grid.

Infrared/Optical: High-resolution infrared (IR) technology uses a small frame around the display with surface-mounted LEDs and

Figure 2: *LCD-Pro diagram*



photoreceptors on opposite sides, hidden behind an IR-transparent bezel. The controller sequentially pulses the LEDs to create a scanning grid of IR light beams. A touch obstructs one or more of the beams in each axis, which identifies the X, Y coordinate.

The salient benefits and typical applications of the above major touch-screen technologies are summarized in **Table 1**.

Applications for Touch-Screens

Touch-screens are now commonplace in many applications from smart phones, vending machines, industrial applications, marine systems, to name just a few. The types, sizes and resolution of these displays are constantly increasing as new applications are developed. This wide variation means that LCD interfaces between panels often differ based on the type of touch technology, type of display and display manufacturer.

This makes it difficult for OEM equipment designers to select one display controller chip to take care of all the different displays in their product lines. Increasingly, designers of Human Machine Interface (HMI) Systems incorporating touch-screen LCD panels are turning to programmable logic to achieve the flexibility they need.

Programmable Logic in LCD Touch Panel Control

The use of Field Programmable Gate Array (FPGA) technology enables system architects to define their HMI controller architecture only once, while being able to scale it to entire product families, employing different microcontrollers, CPUs and LCD panels suitable for each application. Programmable logic, for example, provides the flexibility for a single design to accommodate multiple applications. FPGA technology also makes it easy to implement high-performance vector graphics and real-world interfaces on a single chip. To help designers take advantage of programmable logic, Lattice Semiconductor has introduced an evaluation kit called the LCD-Pro that enables design engineers to evaluate a number of solutions to their design problems. This kit includes a complete LCD-Pro library, a set of flexible, configurable IP cores that can be used to implement versatile and powerful display control, graphics and video applications. A block diagram is shown in **Figure 2**.

The Library is based on the industry standard AMBA bus architecture, allowing interconnection of the evaluation board and embedded soft IP with a wide range of system components. The evaluation board uses the low-cost LatticeECP2M family of FPGAs. This implementation of IP and hardware enables design engineers to quickly and easily configure, integrate and test FPGA-based graphics systems with powerful features, including video for those display applications where promotional video features may be needed. **Figure 3** gives some examples of the IP modules available.

The application of programmable logic to touch-screen technology facilitates and simplifies design, enabling faster time to market and quick response to changing market requirements. ■

Figure 3: *LCD-Pro examples*

IP Core	Base Enhanced Video Controler Module	Base Plus Graphic Accelerator Module IP Library	Base Plus 2D & Video Module
UltiEVC Video Controller	√	√	√
UltiEMC Memory Controller	√	√	√
UltiADDA A/D, D/A Controller	√	√	√
UltiEBB 2D Graphics Accelerator		√	√
UltiVIDIN Video Input		√	√
AMBA APB AHB System Bus IP Modules	√	√	√
UltiSPI_M SPI Master	√	√	√
UltiSPI_M SPI Slave	√	√	√

Analysis of the Design of a 60W-72W High-Density POWER SUPPLY for FPGAs

Alan Chern, Associate Design Engineer, and **Afshin Odabaee**, µModule Product Marketing Manager, both at Linear Technology Corporation, go in depth of the electrical, thermal performance and layout design of a 60W-72W high-density power supply for FPGAs

ALTHOUGH THE VERSATILE and configurable nature of FPGAs is attractive to system designers, the complex nature of design rules that govern the inner working of these devices and their outer interface protocols require extensive training, reference design evaluation, design simulation and verification. As a result, FPGA suppliers provide detailed hardware and firmware support to assist system architects with new challenges in the digital domain.

However, obscure intricacies in the analogue domain, specifically in the realm of delivering power and regulation voltages with DC/DC regulators for core, I/O, memory, clocks and other rails, demand new solutions. For instance, today's FPGAs and supporting components require multiple voltage rails. To power each rail efficiently and in a smallest possible space requires a DC/DC regulator circuit that contains on average 10 components – inductor, MOSFETs, capacitors, DC/DC regulator and so on.

A 6-rail FPGA may require as many as 60 components to power it. Aside from the long list of components needed to power the FPGA, there are hidden costs of component insertion, reliability, circuit board complexity and more. Now is time for DC/DC manufacturers to raise the performance bar for their products.

Managing Multiple Voltage Rails

Prior generations of FPGAs required two or three power rails; some of the high-end multiple-core devices require as many as seven rails: a mixture of 3.3V legacy power rails and recent lower voltages, ranging from 2.8V to 1.0V and below. Moreover, a mix of other voltage rails that are needed for devices other than FPGAs, such as memory, network processors, graphics processors, digital-to-analogue or analogue-to-digital converters, as well as op-amps and RF ICs.

To ensure a "clean" start-up of a system with multiple voltage rails such that none of the rails conflict with each other requires a DC/DC regulator equipped with sequencing and tracking functions. Simply stated, each regulator must be able to track the output voltage of other regulators. The good news is that FPGAs no longer require any sequencing on their rails. However, sequential ramp-up or ramp-down of several voltages across different sections within a system are still required to prevent possible latchoffs that may occur when a voltage rail comes up too fast or too slow.

In the past, tracking and sequencing of power rails was handled by a separate power management IC. Today, designers require that both the sequencing and tracking functions are embedded into the regulators, particularly when they must be located at different corners of the system.

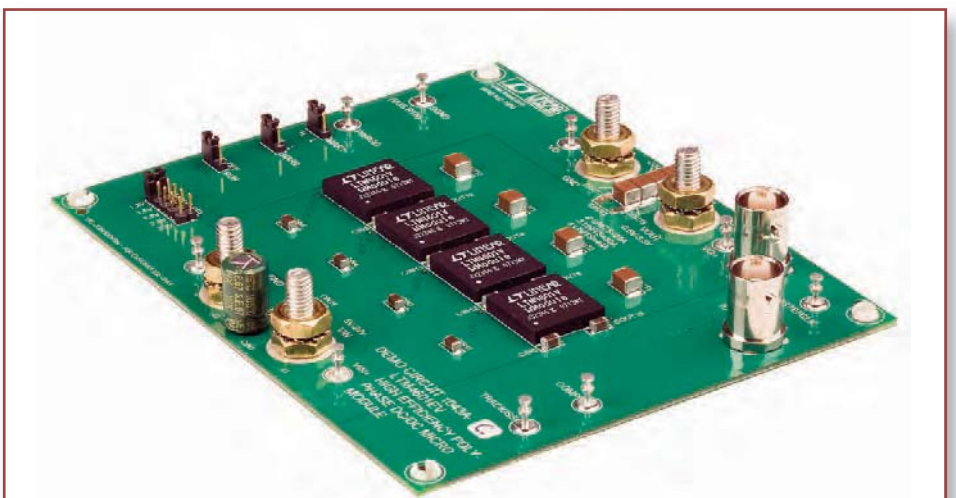


Figure 1: *Four DC/DC µModule regulator systems current share to regulate 1.5V at 48A with only 2.8mm profile and 15mm x 15mm of board area. Each µModule weighs only 1.8g and has an IC form-factor that can easily be used with any pick-and-place machine during board assembly*

Regulating Low Vt and Blazing Fast, High-Current I/O Voltages

Fast I/O nodes often demand the most power in FPGA-based applications. It's usual to see 1.8V and 2.5V I/O voltages that create loads in tens of Amperes. The very high-end systems have requirements for 40A up to 80A I/O designs.

Due to the logistics of a board design, the DC/DC regulator must be placed at a distance from its load and requires a long printed circuit board (PCB) trace from its output to the point

Figure 2: *Simply parallel multiple DC/DC µModule regulators systems to achieve higher output current. Board layout is as easy as copying and pasting each µModule regulator's layout with very few external components required*

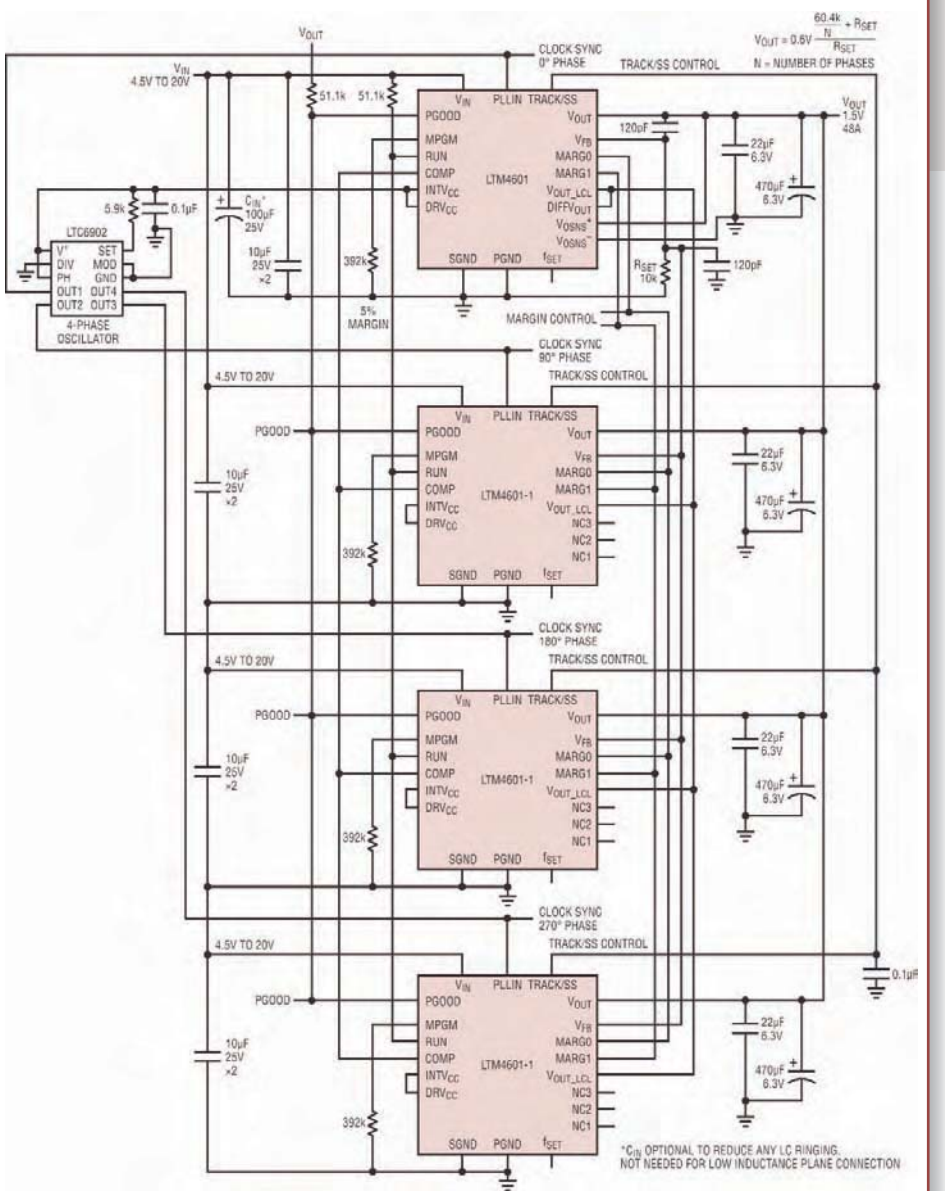
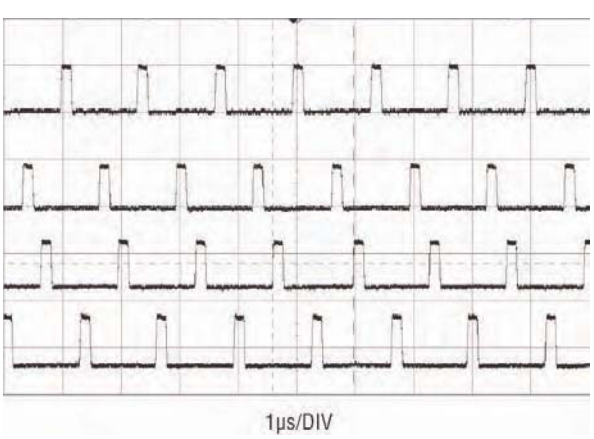


Figure 3: *By operating each DC/DC µModule regulator 90° out-of-phase, the input and output ripples are reduced, which also reduces the requirement for input and output capacitors. The image shows individual µModule switching waveforms for Figure 2*



of regulation. At large load current levels, PCB traces introduce a voltage error equal to the value of the load current (I) multiplied by the impedance (R) of the trace. This IxR voltage error has become more problematic since the load voltages have been decreasing and load currents increasing. For example, a 200mV IxR drop for a 3.3V rail produces 6% error, whereas for a 1.2V rail it introduces a 17% error. Therefore, although the DC/DC regulator can be set to regulate a 1.2V output, the load will only see 1.0V due to IxR voltage drop.

With today's 90- and 65-nanometer processes, where Vt and performance of the FPGA are dependent on the precision of supply rails, an error of 17% can easily degrade performance. For example, a 100mV difference in Vt can scale the leakage current by factor of ten or more.

Standard DC/DC regulators provide precise regulation but only if the load is very close to its output. It cannot compensate for the IxR voltage drop. The error correction must be handled with the help of a remote sense amplifier. The tightest regulation is possible with differential remote sensing of the load, which requires a precision op-amp and precision resistors. An ideal regulator should provide better than ±1.5% regulation accuracy right-at-the-load, even over the -40ºC to 85ºC temperature range. This accuracy may be insignificant for a 3.3V rail, where the digital ICs can tolerate ±0.5V variation, but a 90nm or 65nm device with 1.8V, 1.0V or 0.9V rails will require higher accuracy.

Once the output voltage of the regulator is set by the user, the differential remote sensing automatically adjusts the regulated voltage at the point of the load by compensating for any IxR voltage drop across the PCB trace for a wide range of load currents. As a result, the regulation is very precise when the system is in standby mode, or at full speed when load current and IxR voltage drop are their peak.

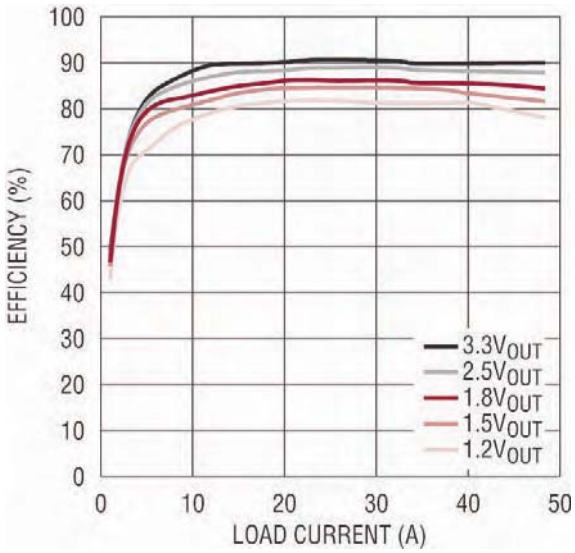


Figure 4: *Efficiency of the four DC/DC µModule regulators in parallel remains high over a wide range of output voltages*

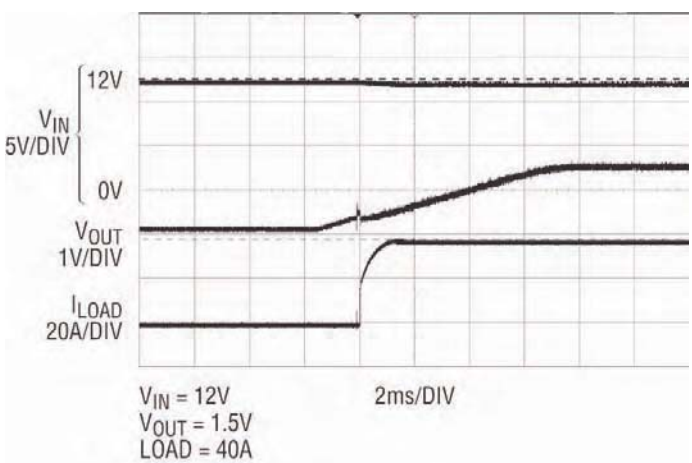


Figure 5: *Controlled soft start is important in proper start-up of the FPGA or the system as a whole. Soft-start current and voltage ramp for four DC/DC µModules in parallel*

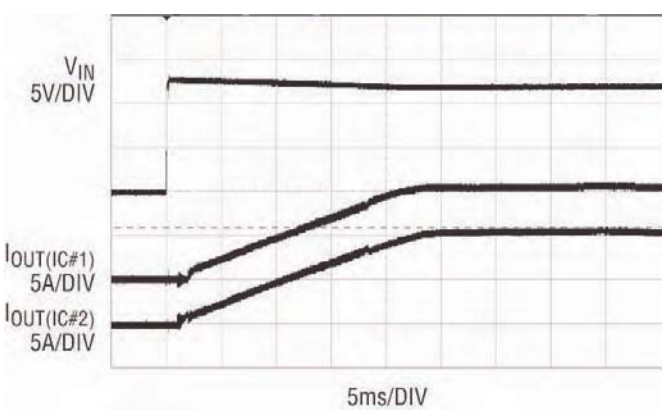


Figure 6: *Each DC/DC µModule regulator starts and ends by sharing the load current evenly and balanced, a crucial feature to prevent one regulator from overheating. Two parallel LTM4601s, as each rises to a nominal 10A each, 20A total*

Lowering the Voltage Ripple Noise

In non-portable applications, as the requirements for voltages drop and currents rise, heat dissipation and operating efficiency become more important factors in the selection of a DC/DC regulator. In portable applications, although load current per rail is less, the operating and standby efficiencies still play an important role in preserving a battery's energy and simplifying thermal management of the portable product.

A switchmode DC/DC regulator offers a higher performance solution than a linear regulator in either portable or non-portable applications, especially for high power requirements. For example, a switchmode regulator providing 1.2V at 5A from a 3.3V input supply at 90% efficiency compares to a linear regulator's 36% efficiency; furthermore, whereas the switchmode regulator dissipates 0.7W, the linear regulator dissipates 10.5W.

On the other hand, a switchmode regulator introduces switching noise and higher output ripple noise (output voltage peak-to-peak ripple) because of its inherent switching operation. Unfortunately, the lower voltage rails of new FPGAs and tighter eye-diagrams of faster I/O signals are less tolerant of power supply "noise". To alleviate the ripple noise, more input and output capacitors can be added to the circuit to dampen peak-to-peak ripple voltage. However, dampening the switching noise is more challenging. One possible approach is to synchronize the DC/DC regulator's operating frequency to an external clock, which forces the regulator to operate within a set frequency chosen to have minimum interference with other noise-sensitive parts of the system. This method is especially effective when several switchmode regulators are all synchronized to a clock frequency that is safe for the rest of the system.

These methods help with design of a less noisy switchmode point-of-load regulator, however the problem of noise can be greatly reduced if the DC/DC regulator is designed from the ground up with the proper architecture, functions and layout. Such a regulator minimizes its dependency on capacitors, filtering and EMI (electromagnetic interference) shielding.

Fine Tuning Voltages

The performance of an FPGA or its supporting ICs can differ when they are assembled into a complete system versus when they are individually tested on a lab bench. Elements such as the type of solder, temperature, PCB layout, trace impedances and

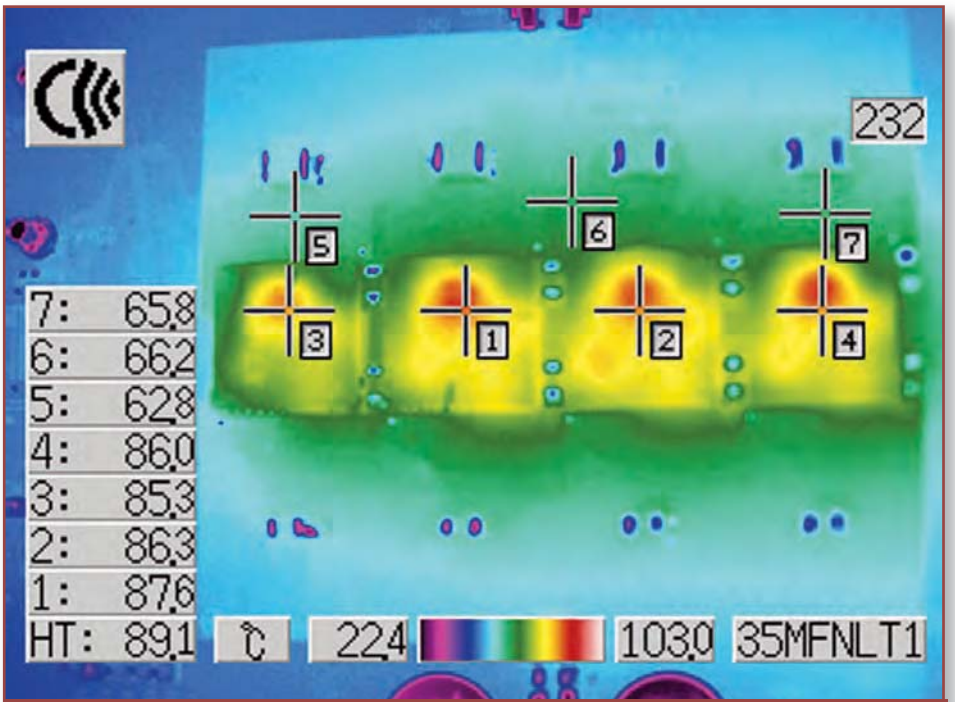


Figure 7: *Thermograph of 48A, 1.5V circuit of Figure 1 shows balanced power sharing among each DC/DC µModule regulator and low temperature rise even without airflow (V_{IN}=20V to 1.5V_{OUT} at 40A)*

assembly process influence the performance of a component. For example, if the core of the FPGA is regulated at a voltage other than expected and this leads into a slower speed, the system's computational capability will be degraded. In some instances, the quality control personnel must reject a system that deviates from its expected performance.

For this reason, as engineers evaluate the performance during qualification or assembly, they need the ability to raise or lower the output voltage in small increments. This function is called margining. In the previous example, the core voltage could be increased so that the operating frequency of the FPGA reaches its desired level. The margining function can also help the system manufacturer increase the overall yield during production.

In a recent discussion with a system designer, the requirement for his power supply was to regulate 1.5V and deliver up to 40A of current to a load that consisted of four FPGAs. This means that up to 60W of power must be delivered in a small area with lowest profile (height) possible to allow smooth flow of air for cooling. The power supply had to be surface-mountable and operate at high enough efficiency to minimize heat dissipation. He also demanded the simplest possible solution so his time could be dedicated to the more complex tasks. Aside from precise electrical performance, this solution had to remove the heat generated during DC to DC conversion quickly so that the circuit and the ICs in its vicinity did not over heat. Such solution requires an innovative design to meet these criteria:

1. Very low profile to allow efficient air flow and to prevent thermal shadow on surrounding ICs.
2. High efficiency to minimize heat dissipation.
3. Current sharing capability to spread the heat evenly to eliminate hot spots and minimize or eliminate the need for heat sinks.
4. Complete DC/DC circuit in a surface mount package that includes the DC/DC controller, MOSFETs, inductor, capacitors and compensation circuitry for a quick and easy solution.

Innovation in DC/DC Design

The innovation is a modular but surface mount approach that uses efficient DC/DC conversion, precise current sharing and low thermal impedance packaging to deliver the output power while requiring minimal cooling. Because of the low profile and power sharing among four devices, a system using this solution depends on fewer fans or slower fan speed as well as minimal or no heat sinks. These contribute to a lower cost system that consumes less power to remove heat.

Figure 1 shows a test board for such circuit. The design regulates 1.5V output while delivering 40A (up to 48A) of load current. Each "black square" is a complete DC/DC circuit and is housed in a 15mm x 15mm x 2.8mm surface mount package. With a few input and output capacitors and resistors, the design using these DC/DC µModule systems is as simple as shown in the photo.

DC/DC µModule Regulator

The LTM4601 µModule DC/DC regulator is a high performance power module shrunk down to an IC form-factor. It is a completely

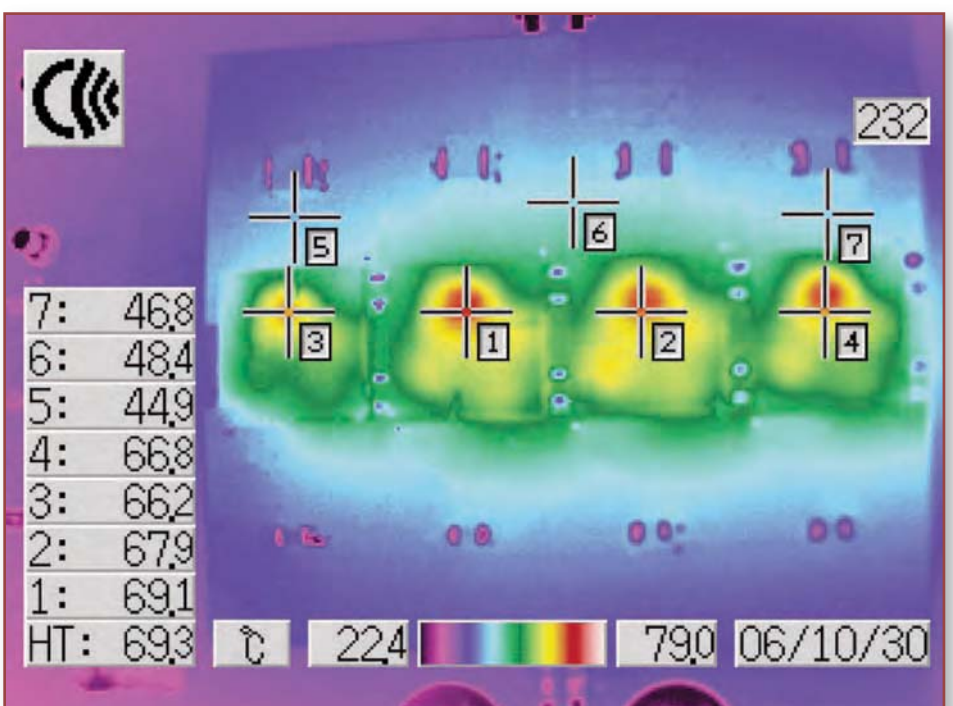


Figure 8: *Thermograph of four parallel LTM4601s with 200LFM bottom-to-top airflow (20VIN to 1.5VOUT at 40A)*

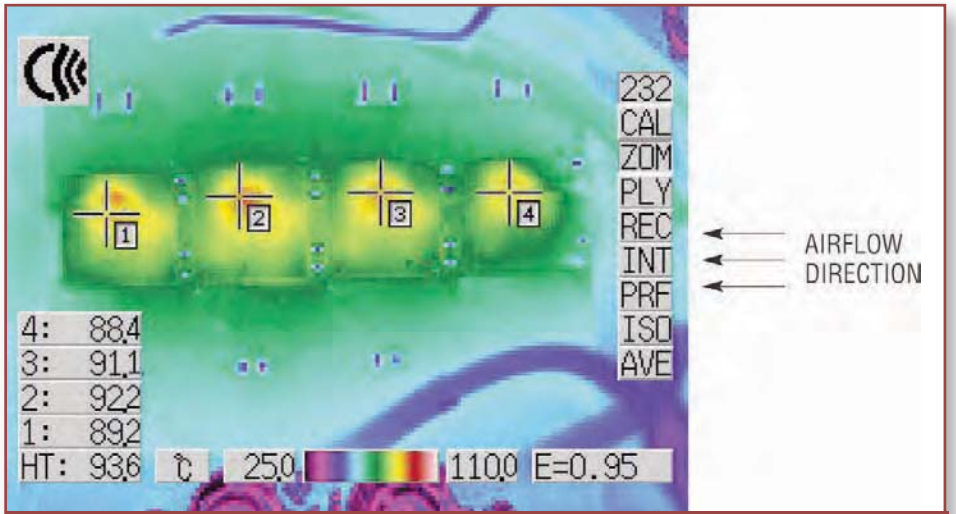


Figure 9: *Thermograph of four parallel LTM4601s with 400LFM right-to-left airflow in 50°C ambient chamber (12VIN to 1.0VOUT at 40A)*

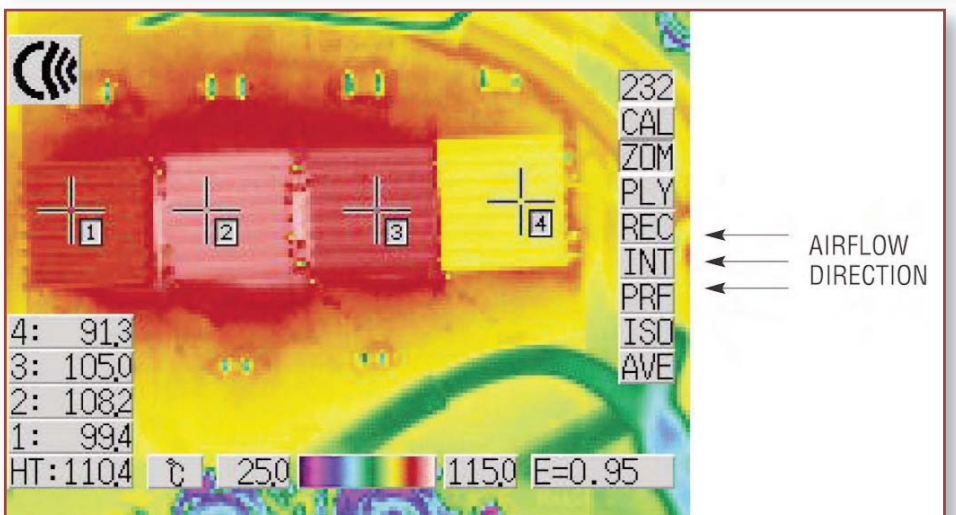


Figure 10: *Thermograph of four parallel LTM4601s with BGA heat sinks and 400LFM right-to-left airflow in a 75°C ambient chamber (12VIN to 1.0VOUT at 40A)*

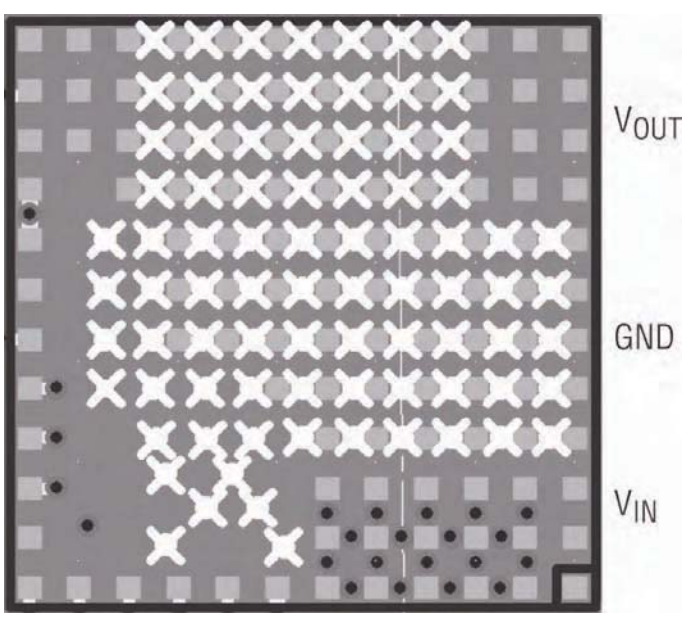


Figure 11: *By adding vias underneath the LGA package, more heat can be dissipated. Vias provide a path to the power planes and into the PCB to draw heat away*

integrated solution, including the PWM controller, inductor, input and output capacitors, ultralow RDS(ON) FETs, Schottky diodes and compensation circuitry. Only external bulk input and output capacitors and one resistor are needed to set the output from 0.6V to 5V. The supply can produce 12A (more if paralleled) from a wide input range of 4.5V to 20V, making it extremely versatile. The pin-compatible LTM4601HV extends the input range to 28V.

A significant advantage of the LTM4601 over power-module or IC-based systems is its ability to easily scale up as loads increase. If load requirements are greater than one µModule regulator can produce, simply add more modules in parallel. The design of a parallel system involves little more than copying and pasting the layout of each 15mm × 15mm µModule regulator. Electrical layout issues are taken care of within the µModule package; there are no external inductors, switches or other components to worry about.

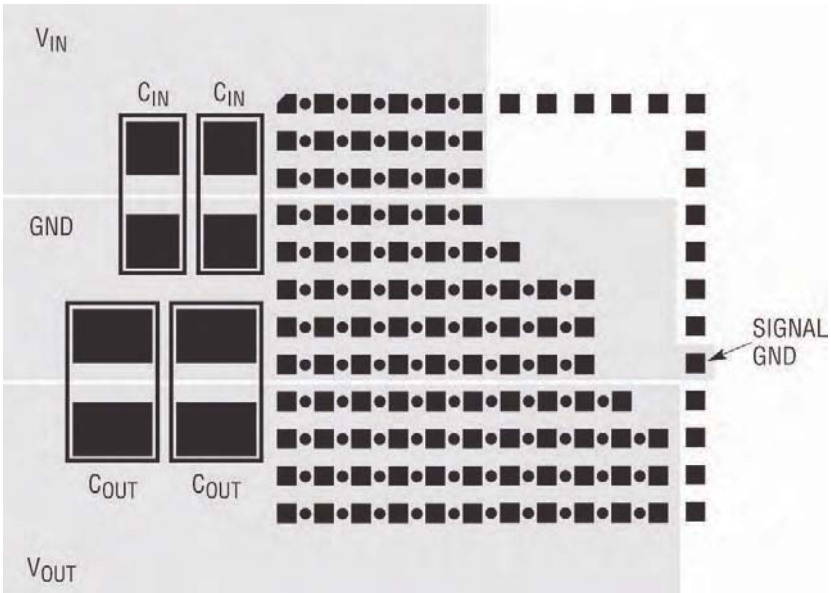
Output features include output voltage tracking and margining. The high switching frequency, typically 850kHz at full load, constant on time, zero latency controller delivers fast transient response to line and load changes while maintaining stability. Should frequency harmonics be a concern, an external clock can control synchronization via an on-chip phase lock loop.

48A from Four Parallel DC/DC µModule Regulators

Figure 2 shows a regulator comprising four parallel LTM4601s, which can produce a 48A (4 ×12A) output. The regulators are synchronized but operate 90° out of phase with respect to each other, thereby reducing the amplitude of input and output ripple currents through cancellation (**Figure 3**). The attenuated ripple in turn decreases the external capacitor RMS current rating and size requirements, further reducing solution cost and board space.

Synchronization and phase shifting is implemented via the LTC6902 oscillator, which provides four clock outputs, each 90° phase shifted (for 2 or 3-phase relationships, the LTC6902 can be adjusted via a resistor). By operating the µModule regulators out-of-phase, peak input and output current is reduced by approximately 20% depending on the duty cycle (see the LTM4601 data sheet). This reduction in turn, reduces the requirement for

Figure 12: *The LTM4601's pin layout provides simple power plane placement and easy paralleling capability (copy and paste approach)*



input and output capacitors. The clock signals serve as input to the PLLIN (phase-lock loop in) pins of the four LTM4601s.

The phase-lock loop of the LTM4601 comprises a phase detector and a voltage-controlled oscillator, which combine to lock onto the rising edge of an external clock with a frequency range of 850kHz. The phase lock loop is turned on when a pulse of at least 400ns and 2V amplitude at the PLLIN pin is detected, though it is disabled during start-up. Figure 3 shows the switching waveforms of four LTM4601 µModule regulators in parallel.

Only one resistor is required to set the output voltage. In a parallel setup, the value of the resistor depends on the number of LTM4601 used. This is because the effective value of the top (internal) feedback resistor changes as you parallel LTM4601s. The LTM4601's reference voltage is 0.6V and its internal top feedback resistor value is 60.4kOhm, so the relationship between VOUT, the output voltage setting resistor (RFB) and the number of modules (n) placed in parallel is:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{n} + R_{FB}}{R_{FB}}$$

Start-Up, Soft-Start and Current Sharing

The soft-start feature of the LTM4601 prevents large inrush currents at start-up by slowly ramping the output voltage to its nominal value. The relation of start-up time to VOUT and the soft-start capacitor (CSS) is:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

$$t_{SOFTSTART} = 0.8 \bullet \left(0.6V - V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A}$$

For example, a 0.1µF soft-start capacitor yields a nominal 8ms ramp (see **Figure 5**) with no margining.

Current sharing among parallel regulators is well balanced through start-up to full load. **Figure 6** shows an evenly distributed output current curve for a 2-parallel LTM4601 system, as each rises to a nominal 10A each, 20A total.

In summary, the DC/DC µModule regulators are self-contained and complete systems in an IC form-factor. The low profile, high efficiency and current sharing capability allow practical high power solutions for the new generation of digital systems. Thermal performance is impressive at 48A of output current with balanced current sharing and smooth uniform start-up. The ease and simplicity of this design minimizes development time while saving board space.

Thermal Performance and Layout

In the first portion of this article, we discussed the circuit and electrical performance of a compact and low profile 48A, 1.5V DC/DC regulator solution for a four-FPGA design. The new approach uses four DC/DC µModule regulators in parallel (Figure 1) to increase output current while sharing the current equally among each device. This solution relies on the accurate current sharing of these µModule regulators to prevent hot-spots by dissipating the heat evenly over a compact surface area. Each DC/DC µModule device is a complete power supply with onboard inductor, DC/DC controller, MOSFETs, compensation circuitry and input/output bypass capacitors. The µModule regulator occupies only 15mm x 15mm of board area and has a low profile (height) of only 2.8mm. This low profile allows air to flow smoothly over the entire circuit while removing heat from the circuit (**Figures 7-10**). Moreover, because of its low profile, this solution casts no thermal shadow on surrounding components, further assisting in optimum thermal performance of the entire system.

Thermal Performance

The move to shrink the size of FPGA-based systems while increasing functionality, memory storage and computational power, have prompted designers to refine the techniques used to cool the components. One simple method is to provide an efficient air flow over the components. Tall components obscure the flow over the thinner packages such FPGAs or a memory ICs. In the case of pre-fabricated DC/DC point-of-load regulators, the blockage is severe as these devices reach a height that is between 6 to 10 times the height of the FPGA and other ICs.

The thin ball grid array (BGA) packaging of the FPGAs is extremely helpful in efficient dissipation of internally generated heat from the top of the package. This benefit is diminished when a taller device such as a pre-fabricated DC/DC regulator inhibits air flow and casts a "shadow" on the device next to it.

Figure 7 is a thermal image of the board shown in Figure 1 with readings of the temperatures at specific locations. Cursors 1 to 4 show an estimation of the surface temperature on each module. Cursors 5 to 7 indicate the surface temperature of the PCB.

Note the difference in temperature between the inner two regulators, cursors 1 and 2, and the outside ones, cursors 3 and 4. The LTM4601 µModule regulators placed on the outside have large planes to the left and right promoting heat sinking to cool the part down a few degrees. The inner two only have small top and

Figure 13: *Top layer planes for Figure 1 circuit*

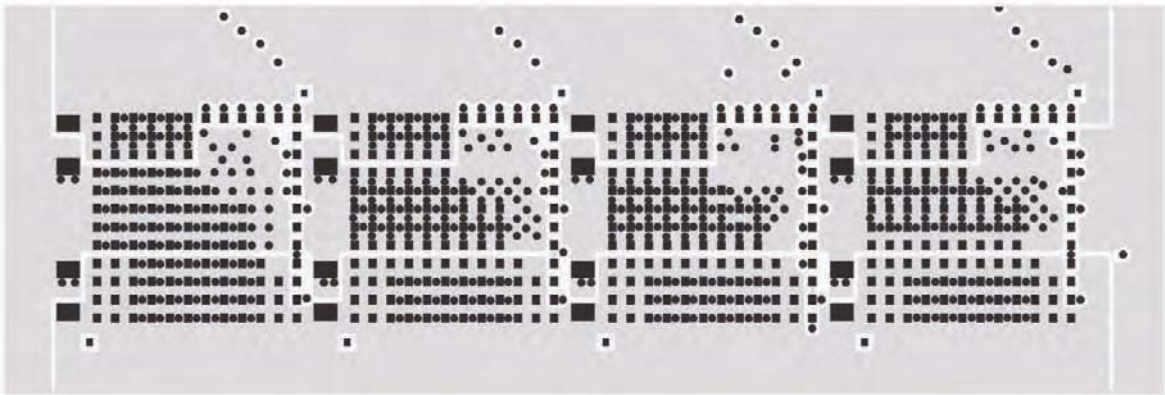
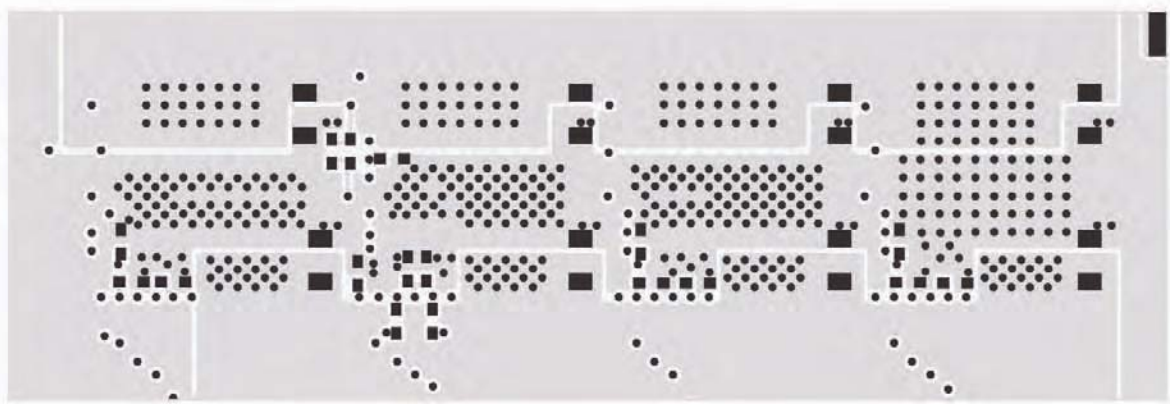


Figure 14: *Bottom layer planes for Figure 1 circuit*



bottom planes to draw heat away, thus becoming slightly warmer than the outside two.

Airflow also has a substantial effect on the thermal balance of the system. Note the difference in temperature between Figures 2 and 3. In Figure 7, a 200LFM airflow travels evenly from the bottom to the top of the demo board, causing a 20°C drop across the board compared to the no air flow case in Figure 7.

The direction of airflow is also important. In Figure 4 the airflow travels from right to left, pushing the heat from one µModule regulator to the next, creating a stacking effect. The µModule device on the right, the closest to the airflow source, is the coolest. The leftmost µModule regulator has a slightly higher temperature because of spillover heat from the other LTM4601 µModule regulators.

Heat transfer to the PCB also changes with airflow. In Figure 7, heat transfers evenly to both the left and right sides of the PCB. In Figure 9, most of the heat moves to the left side. Figure 10 shows an extreme case of heat stacking from one µModule device to the next. Each of the four µModule regulators is fitted with a BGA heat sink and the entire board is operated in a chamber with an ambient temperature of 75°C.

Simple 'Copy and Paste' Layout

Further heat dissipation is possible by adding vias underneath the part. Vias provide a path to the power planes and into the PCB, which helps draw heat away. Vias should not be placed directly under the pads. Figure 6 shows the layout of the vias on the DC1043A demonstration circuit. The cross marks indicate the vias in between the LGA pads.

Layout of the parallel µModule regulators is relatively simple, in that there are few electrical design considerations. Nevertheless, if the intent of a design is to minimize the required PCB area, thermal considerations become paramount, so the important parameters are spacing, vias, airflow and planes.

The LTM4601 µModule regulator has a unique LGA package footprint, which allows solid attachment to the PCB while enhancing thermal heat sinking. The footprint itself simplifies layout of the power and ground planes, as shown in Figure 7. Laying out four parallel µModule regulators is just as easy, as shown in **Figures 11, 12, 13** and **14**.

If laid out properly, the LGA packaging and the power planes alone can provide enough heat sinking to keep the LTM4601 cool.

Managing Heat and Cooling

Delivering 60W of power in a compact space without efficient means to remove the heat from the power supply exacerbates the already challenging task of system heat management and cooling. The DC/DC µModule family is designed with careful attention to the layout of its internal components, package type and electrical operation, which ease thermal management of a very dense power supply circuit. The LGA package and simple layout allow 100% surface mountable and low profile design for maximum efficiency in air flow. This new approach in power supply design takes advantage of paralleling multiple DC/DC µModule regulators and following a 'copy and paste' approach in layout design, to provide a 60W power supply with minimum components while operating efficiently in a compact, low profile space. ■

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MICROCHIP

Rajiv Nema, Senior Product Marketing Manager at Actel Corporation, explains how the SmartFusion mixed signal devices team up many elements including high-density, flash-memory-based FPGA, an ARM Cortex-M3 MCU core with peripherals and high-performance programmable analogue functions on a single device to create single-chip SoC solutions

The DREAM Comes True

SYSTEM-ON-CHIP (SoC) means many different things to embedded system designers, depending on the type of systems they are working with. At one extreme, say for mass-market consumer products in the entertainment or communications markets, SoC can imply a very large, multi-million-gate IC comprising many large blocks of custom logic, together with mixed-signal functionality that interfaces the chip's digital processing capabilities to the outside world. In reality, the number of projects that can support SoC designs on that scale is limited. Many designers of embedded systems that might be classed as "mid-range" would be very pleased to achieve a SoC solution, but in practice and for a variety of reasons it has proved elusive.

The attractions of a design outcome in which all major functions reside in a single device are obvious; minimising bill-of-materials cost, parts inventory and printed-circuit-board (PCB) area are just a few of the benefits, to which can be added a likely reduction in power over a multi-chip solution and more subtle gains such as increased protection of Intellectual Property (IP). If the essence of a design's functionality can be deeply buried within a single piece of silicon, it becomes much more difficult for a third party to access it.

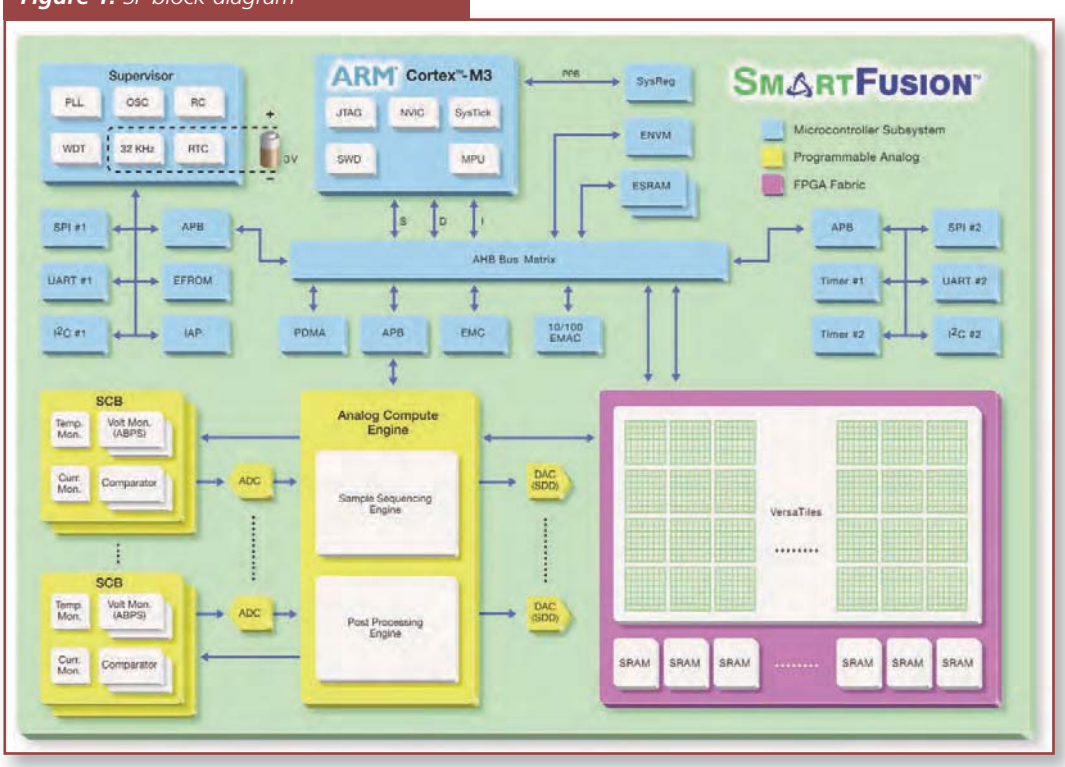
The SoC dream

For most design teams, that SoC outcome has remained a dream. Few products will be made in the volumes that justify a full-custom mixed-signal chip design; for the majority, either an ASSP (application-specific standard product) or a microcontroller will be at the heart of the solution.

In both of those cases, finding a part whose capabilities exactly match the task at hand is often a challenge. Almost by definition, any ASSP will offer a solution to a typical design problem in a given application space, and that typical solution is unlikely to be an exact match for most real-world projects. The result is either that an over-specified part is used, or that extra circuitry has to be created to fill the gaps where the "typical" specification falls short of what is actually needed. In addition, the ASSP is a relatively inflexible solution; once an IC has been chosen, its feature set constrains how the product design will progress from that point onwards.

The most common solution is invariably based around a microcontroller. While software programmability offers great flexibility, it is very rare for an MCU to provide an exact match of features to the needs of a typical embedded design. A large number of such designs will place some form of programmable logic – FPGA or CPLD – alongside the MCU to add logic functions in hardware; and despite the varied peripheral mix on the broad range of MCUs available today, it is a rare embedded-system PCB that does not also carry an assortment of analogue components for signal conditioning and I/O connections.

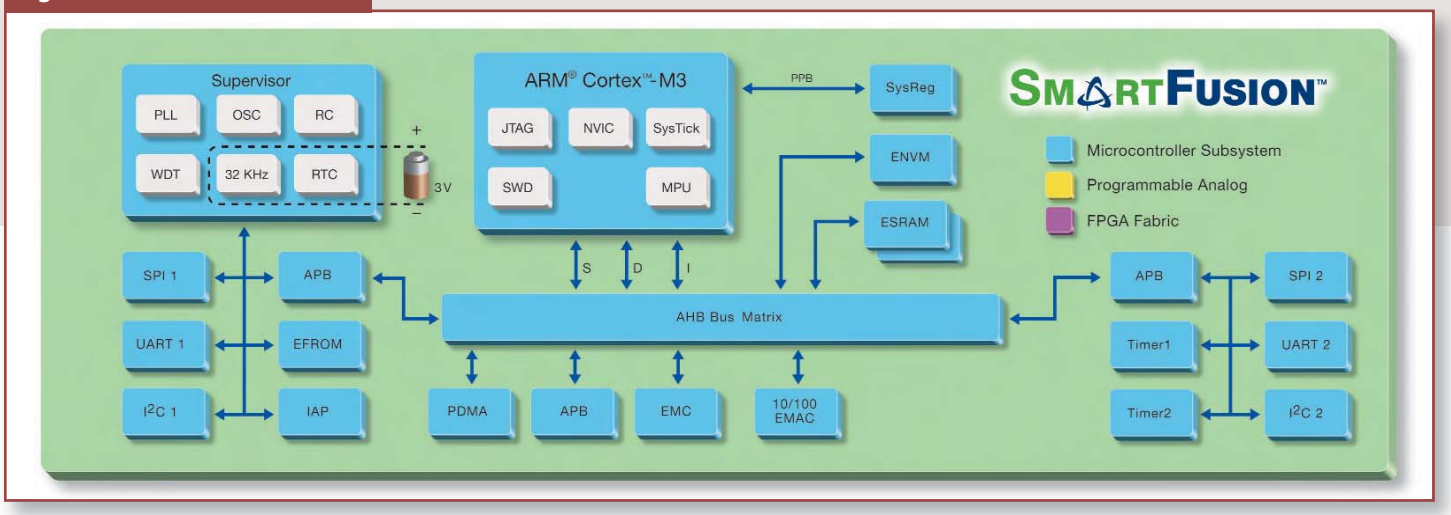
Figure 1: *SF block diagram*



Mixed-Signal FPGAs

For some time, Actel has provided a solution for such designs in the form of its Fusion Mixed-Signal FPGAs. They offer a single-chip combination of high-density programmable logic and configurable analogue circuit functions, together with large flash

Figure 2: *ARM microcontroller*



memory blocks, comprehensive clock generation and management circuitry, and the option of embedding a "soft" microcontroller core in the chip's FPGA logic.

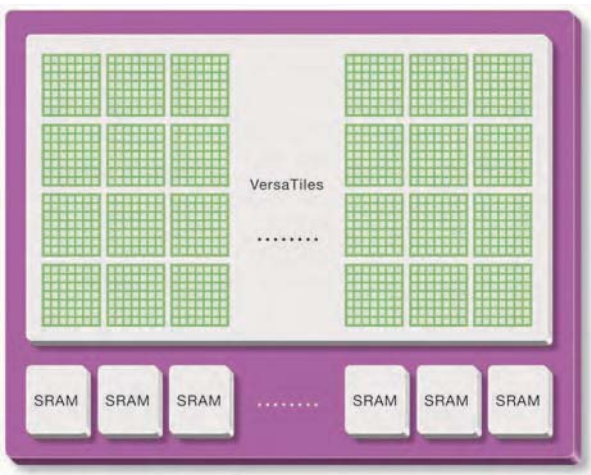
Now, that principle is advanced and greatly extended in the new SmartFusion devices, which offer embedded design teams everything they need to create genuine single-chip SoC solutions; SmartFusion combines high-density, flash-memory-based FPGA, an ARM Cortex-M3 microcontroller core with a full peripheral set and high-performance programmable analogue functions, all on a single device.

The ARM Cortex-M3 core needs little introduction: it has proved to be a powerful and economical implementation of the ARM architecture in a wide variety of settings and has been the platform on which many designers have advanced from 8-bit to 32-bit architectures. In the SmartFusion chips, it is a 100MHz (125DMIPS) device with up to 512kB of flash memory and 128kB of SRAM. In this new series of devices, the processor is a "hard" core. This means that it is in the silicon in the most area-efficient implementation. This has several consequences: it is powerful enough to run complex algorithms, readily running precision motor control, or even multi-axial control of several motors. Alternatively, in an application such as systems management, it could supervise all of the voltage monitoring, sequencing, fan control and associated "system housekeeping" tasks, while having ample capacity to also run a higher, user-application-level, task.

Peripherals and Interfaces

In the same way that the processor core is build in a "hard", area-efficient form on the SmartFusion ICs, a comprehensive set of commonly-used peripherals is also provided as standard. There is a 10/100 Ethernet MAC (media access controller) and other interfaces include SPI, I2C and UARTs. A large number of digital (FPGA) I/Os operate at up to 350MHz, support I/O levels for interface standards such as LVDS PCI and LVPECL. Other capabilities that the engineer who is more used to working with microcontrollers will recognize include real-time clock, DMA controller and external memory controller, timers and watchdog function.

Figure 3: *FPGA*



On the die, together with the ARM Cortex-M3 core, there is a large resource of Actel's flash-based ProASIC 3 FPGA logic. Just as the processor core is a full-specification implementation, the programmable logic offers 350MHz system performance and the chips in the SmartFusion family range offer up to 500K gates of programmable logic and 108kB of SRAM embedded in the fabric. As with Actel's all flash-based FPGAs, the structure offers complete immunity to high energy radiation-induced "firm" errors that can, on occasions, affect SRAM-based devices and that are a concern for many embedded system designers.

As the configuration of the FPGA is set in flash cells (and the ARM core can execute from on-chip flash memory), the entire chip is "live" – fully operational – at power-up, with no requirement to wait while a configuration file loads from ROM or EPROM. The flash memory also permits in-field upgrades, unless that option is explicitly de-selected, which is one of the security options; once programmed, further access to the configuration memory can be permanent disabled.

Within the microcontroller subsystem itself, a five-layer ARM AHB-bus matrix structure has a total theoretical on-chip bandwidth of 16Gbit/s; there are five functions that can act as bus masters, two from the Cortex-M3 core plus the 10/100 Ethernet MAC, DMA controller and FPGA fabric master, with the various other interfaces and memory blocks acting as slaves.

Programmable Analogue

The third major element of the SmartFusion design is the provision of high-voltage bipolar analogue functions. To accurately capture signals from the application, SmartFusion

Figure 4: *Analogue Compute Engine (ACE)*

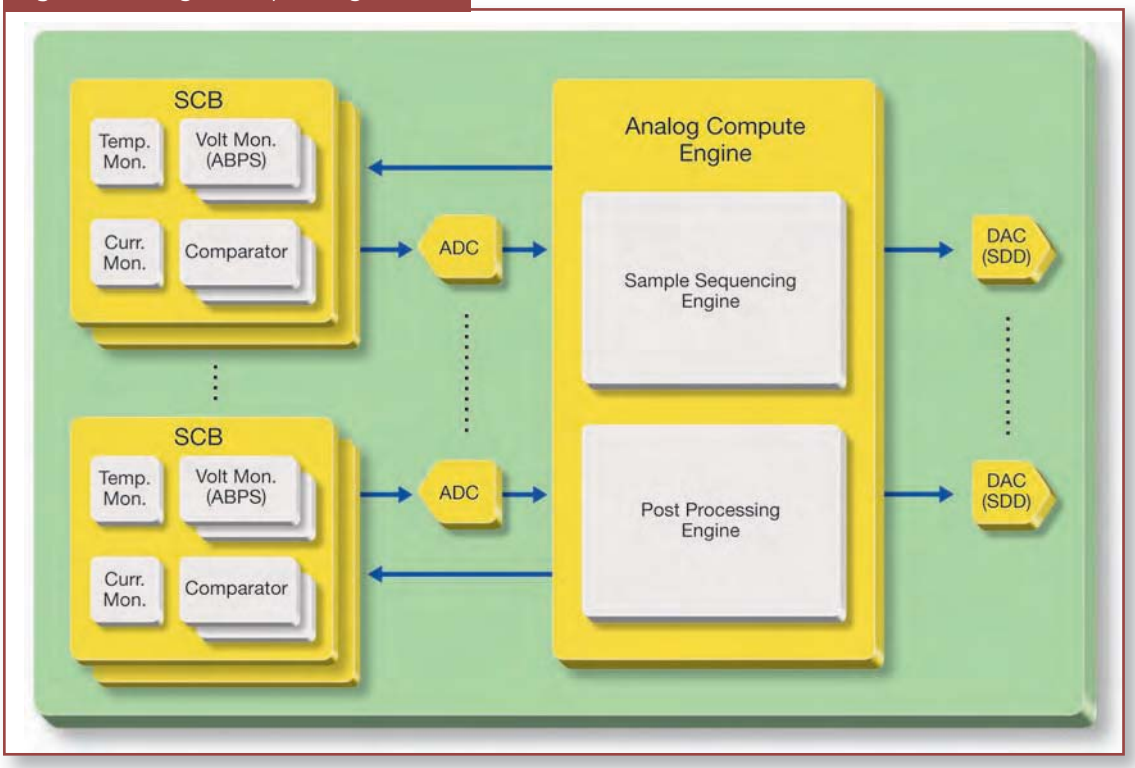
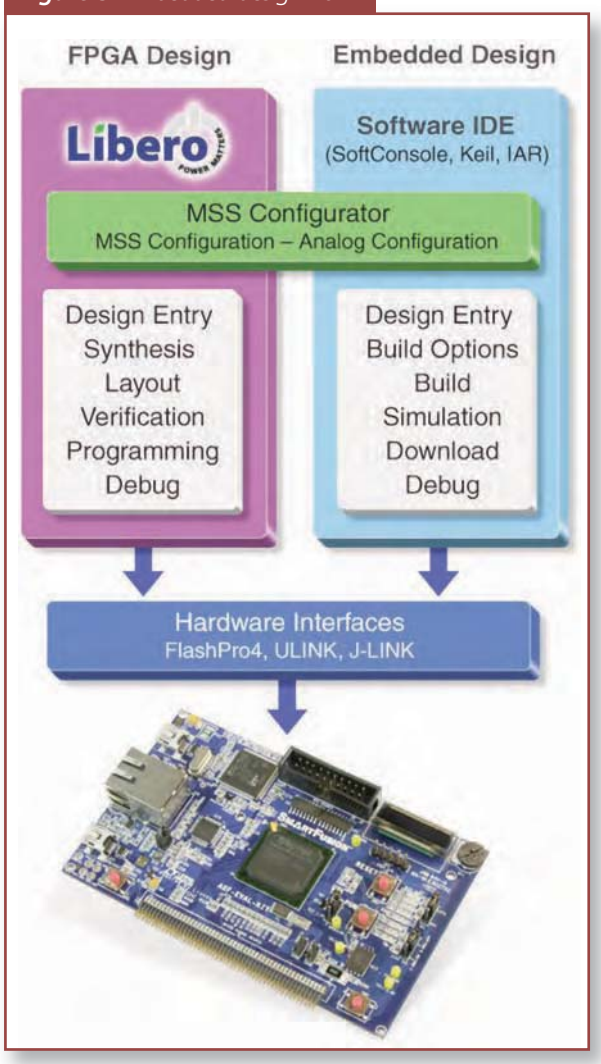


Figure 5: *Embedded design flow*



temperature reading. The on-chip comparators are plentiful (up to 10 in 500K gate device) and super fast with propagation time of just 50ns.

Autonomous Analogue Signal Processing

That, however, is only part of the analogue processing capability within the intelligent mixed-signal FPGA. A completely new concept is the Analogue Compute Engine or ACE, a semi-autonomous block that carries out extensive analogue pre- and post-processing, including sampling and sequencing of signal acquisition, without the intervention of the ARM Cortex-M3processor.

At first sight it might appear superfluous to include that capability within the ACE block when there is an adjacent ARM Cortex-M3core; however, the ACE can offload the processor core from routine tasks, to the point where many actions involving signal acquisition, processing, storage and output may be carried out completely without the involvement of the Cortex-M3. Designers might configure the device in this way to leave the Cortex-M3 free to carry out (for example) real-time processing tasks.

In a system/power management design exercise, the entire function of monitoring every voltage rail for deviation from its nominal value, and generation of alarms should any of them do so, would be a suitable function to assign to the ACE: but its capabilities extend beyond that level of complexity to include filtering and linear transformation.

The programmable analogue block that it handles is comprised of ADCs, DACs and SCBs; an important fact is the analogue block has a rich set of connections to both the microcontroller subsystem and to the FPGA fabric. Each of these elements, separately and as a grouped functional block, is completely programmable in terms of both its interconnections and its operating parameters.

chips will host up to three 12-bit successive-approximation register (SAR) analogue to-digital converters (ADCs) that will run at up to 600 ksamples/s. Each ADC has a corresponding first-order, 1-bit sigma-delta DAC, with 500ksps update and effective 12-bit resolution. Multiple analogue functions are collected within Signal Conditioning Blocks (SCBs) comprising, for example, accurate high-voltage and current monitors, temperature monitors and high-speed comparators. The high voltage monitors, termed ABPS (active bipolar pre-scalers), offer voltage monitoring capability from -1.5V to +14V.

Also likely to be of great utility to designers working in the system-management or power regulation domains, the current monitors amplify the voltage drop measured across an external sense resistor placed in the application's current path with differential gain of 50; and the temperature monitors convert the voltage drop across a simple PN-junction (for example a diode) into a

New Level of Design Flexibility

This unprecedented blend of capabilities on a single chip does, however, mean that the SmartFusion part will represent a departure for some design teams. It has a powerful processor core; embedded designers who have a mainly software orientation will be completely at home with the ARM architecture and will immediately be able to apply the vast amount of experience that has been built up in coding for the ARM 32-bit ISA. Conversely, they may be less comfortable with the FPGA design paradigm of implementing functions directly in hardware, via coding in RTL. They may consider designing in the analogue domain to be completely out with their expertise.

In a mirror-image, the hardware designer who comes to a project with a background of RTL design may be less comfortable with processor-based, C-coding, and may likewise pass analogue-function design to a colleague experienced in that area.

SmartFusion and its associated design tools have been structured so that engineers from either of those backgrounds can confidently execute a complete design. The engineer with ARM experience can view the task as a processor-centric exercise and the tools will provide the confidence to implement additional logic and custom functions in the programmable logic array. The converse also holds true: an FPGA-centric design can hand off procedures to the processor core, or use it for background scheduling and supervisory tasks, see **Figure 5**.

When designing with SmartFusion, a GUI-based, drag-and-drop-style approach will provide immediate access to extensive libraries of pre-defined IP functions. For either the C programmer or the RTL coder, the tool suite will extend his or her area of competence to fully use the resources of the chip; or, the design tools will provide a collaborative environment where a conventional team can work together on the different aspects of the SmartFusion IC.

Designers and design teams may benefit from taking time to explore the new freedoms that this architecture offers. Take, once again, the example of a generic system management function that would be required to sequence, ramp and monitor multiple power rails, generating voltage trim signals (analogue and/or digital), monitoring temperature probes, passing alarm and status signals to a higher-level supervisor, driving fan outputs and indicators, and probably executing numerous other minor but essential tasks. Almost by definition, the exact specification of such a sub-system can be fluid right up until development of its host system is finalized, so the option of a totally programmable solution is immediately attractive.

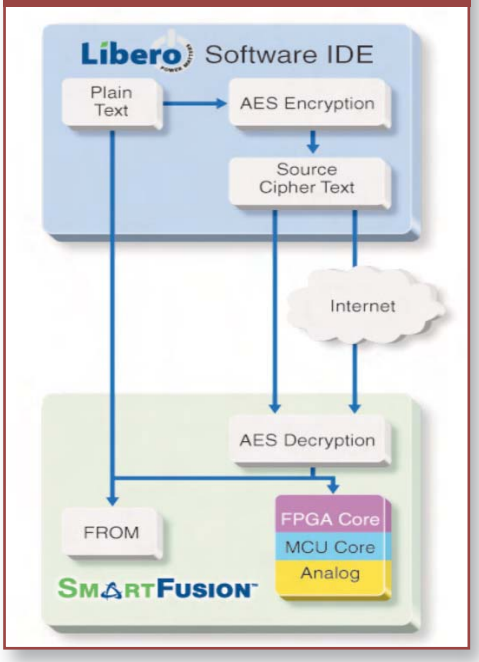
Waiting to be explored is the fact that SmartFusion offers more than one way to perform almost every function in the above list. Voltage thresholds can be monitored directly by an analogue comparator, or by an ADC; the decisions can be taken and actions initiated by the ACE block, or by code running on the Cortex-M3 core. Fan control may be implemented by a simple set of stepped values, sequenced by the ACE; or it could use a full PID control algorithm running in the Cortex-M3. To drive the fan, the system would generate a PWM output waveform. A PWM generator could be configured from one of the ARM core's timers: or it could be instantiated in the FPGA fabric by a small piece of pre-defined IP, imported with a few clicks into the FPGA design flow.

The engineer coming to such a task from a microcontroller background might previously have employed two or more 8-bit MCUs to control a complex power-management scenario such as this. Stepping up to the 32-bit ARM core, his or her first instinct might be to exploit that power, write the C code and configure the entire scheme under processor control. But equally, the FPGA-fabric design-tool flow that accompanies SmartFusion could rapidly generate one, or a series, of complex state machines that would reside in (and use a relatively modest amount of) the programmable logic array, to execute the same feature set.

Design Security

In its existing series of Flash FPGAs, Actel previously established an enhanced level of design security over prior programmable logic offerings. A measure of confidence in that solution was expressed by ARM's licensing of a soft version of its processor core for deployment in FPGA. Once programmed into the array it would be unfeasibly difficult for an attacker to retrieve the IP of that core from the silicon. Now, with a microcontroller core on the same die as the FPGA fabric, that protection is extended to the system software as well as the FPGA configuration code. The ARM Cortex-M3 core, as a "hard" block, now no longer needs that form of protection.

Figure 6: *A built-in 128-bit AES decryption engine permits secure in-system programming during final product manufacture*



Inherent IP security is provided by the single-chip environment; as a flash device, SmartFusion has no need to read a configuration file from an external memory, and once in operation, internal interfaces such as the FPGA-to-ARM-core buses are not visible and traffic on them cannot be monitored.

A number of additional options are available to designers seeking to protect their IP. The simplest is to program the flash that holds FPGA configuration and the area for Cortex-M3 code in "clear", and set a condition – in effect, blowing a fuse – that prevents that area of flash from being read or re-programmed. This capability is known as "FlashLock".

The data output from Actel's Libero design tool suite, comprising again configuration and run-time code, may also be encrypted using 128-bit AES standard for distribution outside the safety of a secure manufacturing environment. A built-in 128-bit AES decryption engine, permits secure in-system programming during final product manufacture if programmed with a matching programming file.

Taking into account the ability to design exactly the system a designer might need, unparalleled IP security plus the ease of design now available to FPGA, embedded and analogue designers, SmartFusion devices offer innovative, intelligent integration at its best. ■

Design Function Before HARDWARE

Rob Evans, Technical Editor at Altium Limited, analyses what's needed from today's electronics design tools to provide high-level systems that unlock the functionality from the constraints of a predefined hardware platform

IN TODAY'S electronics designs, the true competitive value tends to lie in the software-defined elements that characterize the product's function and user experience. This change towards software-focused design has continued at a rapid pace to the point where a product's physical hardware now takes a supportive back-seat role. It acts as a host and external interface for the software that defines a product, rather than determining the unique aspects of that product in its own right.

However, in conventional design flows the initial part of the design cycle is directed toward creating the physical hardware platform to support those all-important software elements. In this hardware-focused approach to electronics design, meaningful software development can't proceed until a hardware prototype is available. In practice, key device hardware decisions must be made first and then a suitable platform designed and created.

Perhaps the main barrier to a soft-centric approach to product design then, in a nutshell, is that current tools and design flows lock the development of software and physical hardware together. What's needed is a way to isolate the defining IP of the design – the device intelligence that determines its functionality and competitive value – from the hardware platform and devices that support it.

This requires the use of a design system that raises the abstraction of the design processes to a point where the design IP is not tied to particular physical hardware devices, microprocessors or even proprietary IP cores. Such a system would allow designers to focus first and foremost on creating a product's core design intelligence.

Separating IP from Hardware

The starting point for a design system that frees designers to create a product's key functionality is one that is independent of FPGA vendor or device. Unlike conventional IDE toolsets from device vendors, a 'neutral' embedded development system allows designers to both choose and change the programmable device to suit the software under development, rather than the other way around.

Such a system can achieve this capability by providing matching driver files and hardware libraries for each supported programmable device. The drivers can automatically supply the design system with full knowledge of the target architecture such as programming information, pin-out capabilities and boundary scan data, while the library files provide the physical and graphical models for the device. The system can also be supported by a hardware development board featuring plug-in device boards, allowing the entire design system to simply align itself to the current choice of programmable device.

In a conventional design flow however, changing to a different FPGA means that the design requires significant re-engineering to suit the new programmable device. This is because the design-to-device targeting information that needs to change – timing requirements, place and route data and port to pin mapping – is generally contained within the source design files. However, if that linking information is stored in separate design 'constraint' files, the design is configured to the target FPGA in a more flexible way. A new constraint file will target the design to a

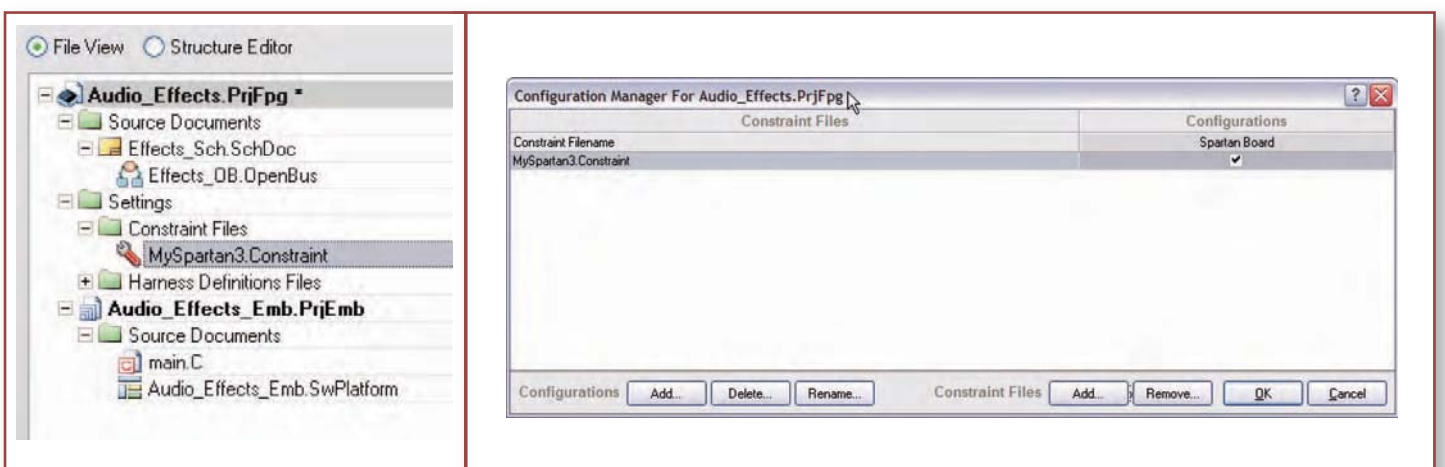


Figure 1: *Constraint file added to project (left) and configured to target the Xilinx Spartan hardware board (right)*

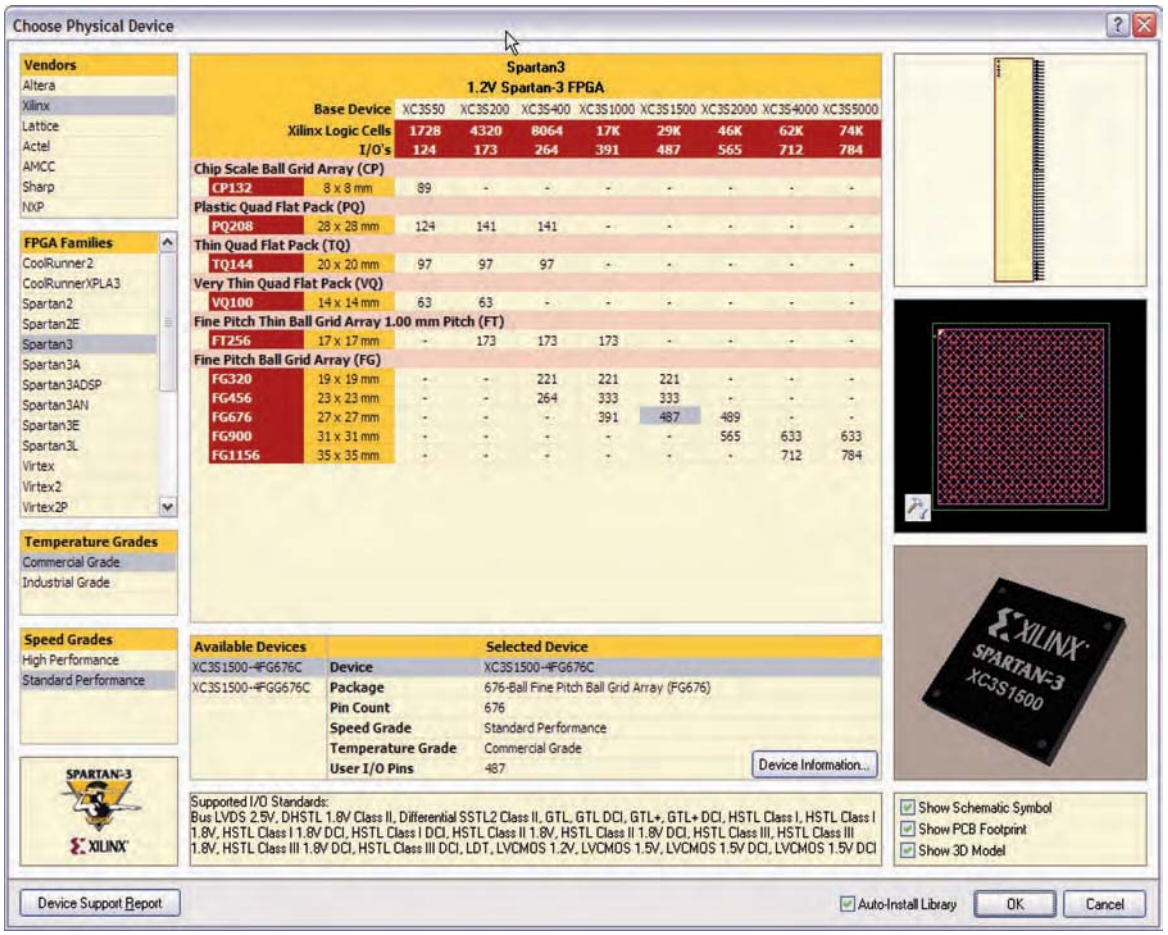


Figure 2: *Selecting the Xilinx device*

different FPGA, allowing the design source to remain largely unchanged and independent of the device it is implemented on.

Consider, for example, a design where we've selected to use a Xilinx Spartan 3 device. The design system is aware of this FPGA, plus a large range of other devices, and it's just a matter of instigating a constraint file then selecting that device as the 'target' for our design. The constraint configurations are a separate element within the design structure and can, therefore, be changed or added to without affecting the core design files.

Multi-device compatibility can also extend to library collections of embedded IP. If the function blocks and components in the IP libraries are pre-synthesized and verified to suit the architecture of all supported devices, the embedded design can be easily developed from ready-to-go blocks of circuitry without having to worry about the underlying device architecture. Along with core blocks of functional logic, this soft IP would include easily-connected Wishbone bus standard microprocessors, peripherals and memory, so everything you need is ready to go, regardless of the hardware platform.

With high-level 'abstracted' interface systems in place, and the underlying hardware complexity hidden, the opportunity then exists to raise the abstraction level of the embedded design capture system itself. At a practical level, the arcane nature of HDL entry can give way to simpler embedded design capture systems that raise the level of design abstraction. These might take a graphical flow diagram approach, or even use a schematic capture system where functional blocks of IP can be moved around and interconnected in a familiar way.

Our FPGA design, in this case a DMX lighting controller, is assembled as an OpenBus system based on the TSK3000 32-bit processor coupled with a UART serial controller. This system, shown here, uses the development board's SRAM for program and data memory, along with a LED controller core and a Custom 'desk' Digital IO. The FPGA-independent components are simply selected from a library palette then hooked up to provide the functionality we want.

With this approach changing to a different processor IP block causes minimal impact to the surrounding hardware and, when backed by compiler toolchains for all supported processors, the embedded software can also remain intact. The OpenBus design connects and drives the external peripheral devices, in this case on the advanced development board, as configured by a top level schematic sheet.

Simplifying the embedded hardware structure and design processes in this way means that complex processor-based embedded systems can be created and changed easily. The division between hardware and software is more flexible, allowing the partition to be moved throughout the design cycle rather than be locked at the beginning of the embedded development process.

Flexible Configurations

The separation of design functionality from physical hardware also offers a high-level of design portability, where multiple hardware configurations are easy to explore. Because the

Figure 3: *The high level OpenBus design document can be 'wired up' very quickly*

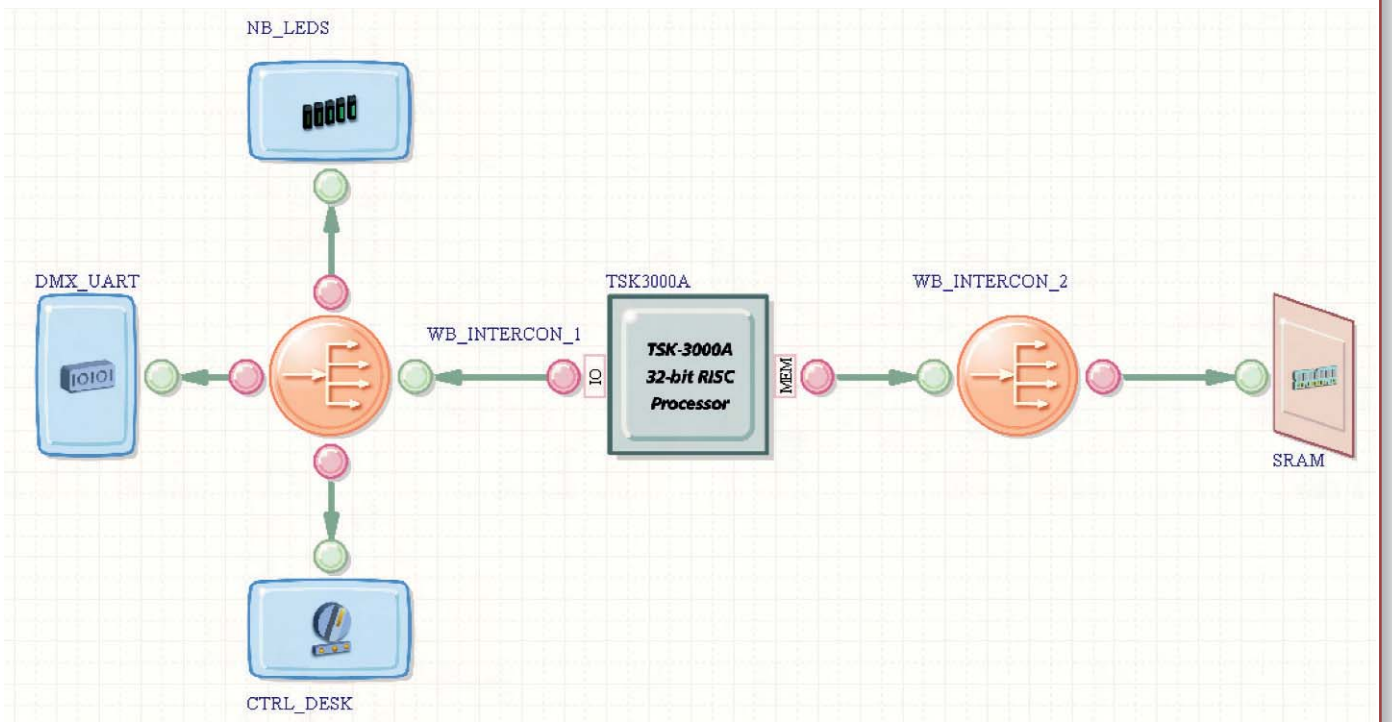
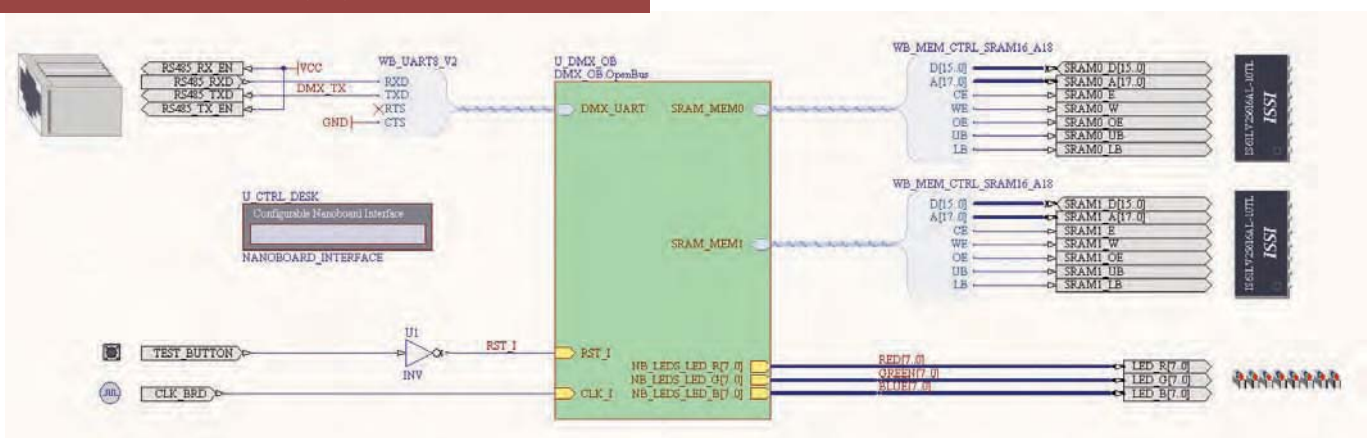


Figure 4: *The overall schematic shows the OpenBus document (green) connected to the board peripherals*



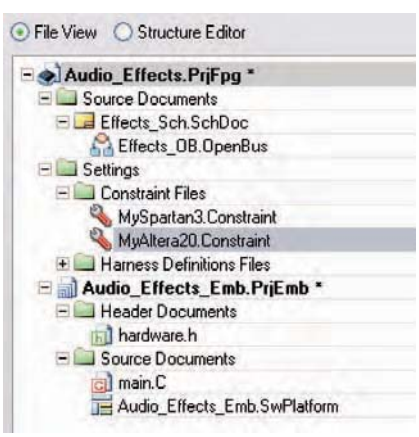


Figure 5: *A new constraint file added to the project (left) and configured to target the Altera hardware board (right)*

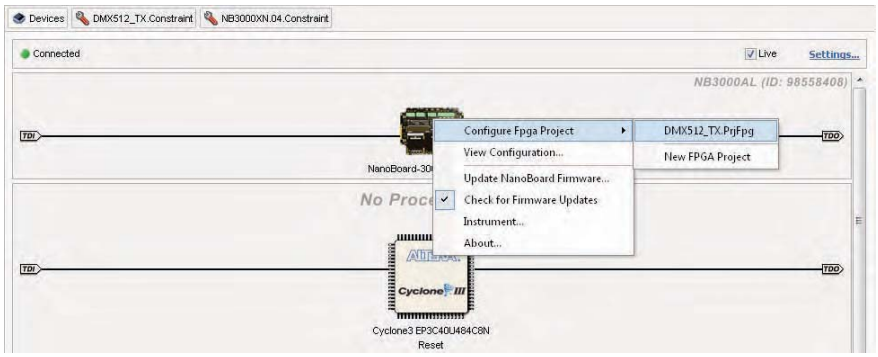


Figure 6: *The Altera device is automatically detected, then the design project re-configured*

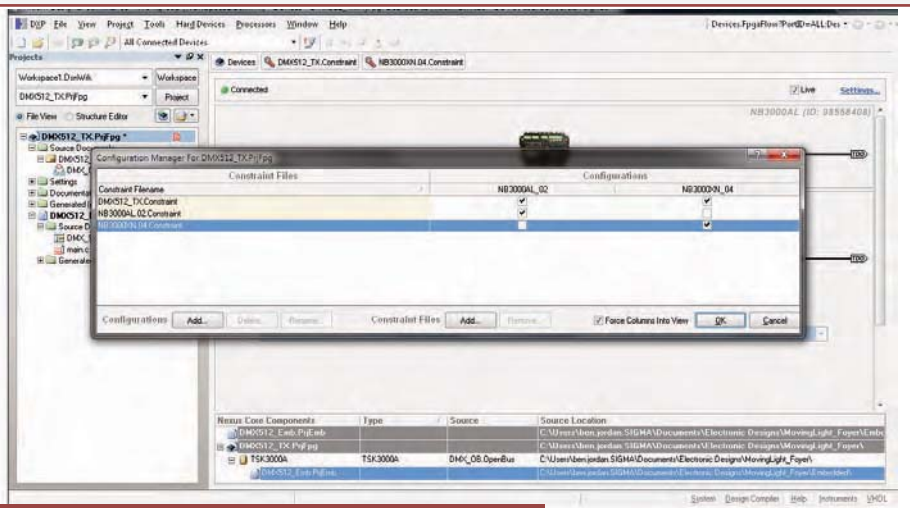


Figure 7: *Matching the new automatically-loaded constraint files to the Altera development board*

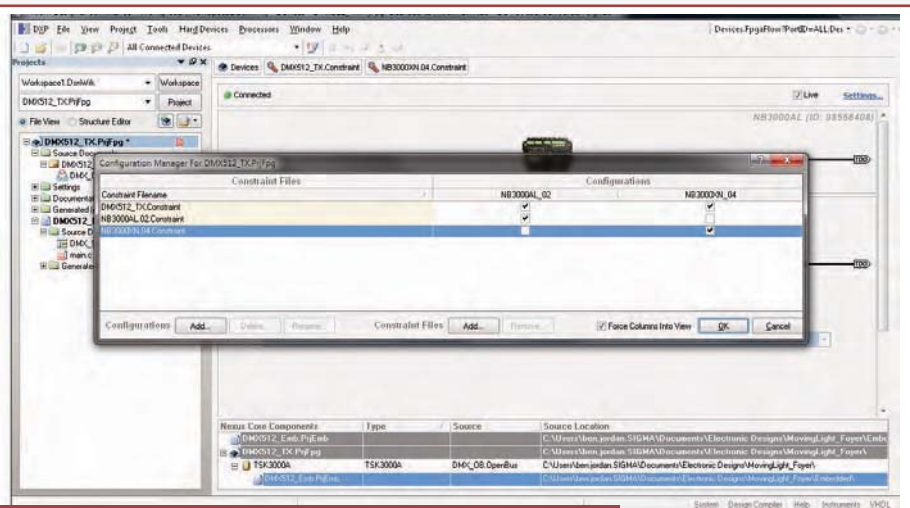


Figure 8: *Building the reconfigured project design for the detected development board, ready for testing*

core IP of the design – where its true value lies – is largely independent of the hardware that supports it, it can be implemented on different hardware platforms that might deliver benefits such as improved performance, a simpler implementation or even lower costs.

Let's say we'd like to compare the design's performance and efficiency when changing from the Xilinx FPGA to an Altera device. When this would traditionally constitute a significant redesign, the process is quite straightforward when the FPGA configuration data is held separate from the design itself. We simply create a new constraint file for the Altera device, add it to the design project, then change to that configuration when targeting the Altera FPGA.

Even better, when the design system is coupled with a smart hardware development board featuring plug-in device boards (as mentioned earlier), the complete design system can automatically align itself to the current choice of programmable device. Thanks to plug-in FPGA daughter boards and peripheral modules that identify themselves to the system, the matching design configurations load when a sub-board is changed.

Swapping from a Xilinx to an Altera daughterboard, or changing to the Altera equivalent board, means the device is immediately recognized and the FPGA project can re-configured with a few mouse clicks.

The appropriate constraint files load and can be selected as the new configuration. With the project targeted to the new FPGA, the design can be synthesized, rebuilt and programmed into the Altera device, ready for assessment, see **Figures 6** and **7**. Note that the system outlined here harnesses the FPGA vendor ISE tools, which are installed on the PC but do not need to be accessed directly.

One important point here is that the embedded development system coexists and communicates with the physical hardware design tools in a unified product development system. A single design model is used for the entire design, so components and connectivity are reflected through all domains. For example, the high-level system that responds to a change in FPGA device can implement the reconfiguration at a physical hardware level, as well as at the embedded hardware level.

The end result is a design system that streamlines and simplifies the product development process from conception though to the finished product. A high level of design abstraction, when implemented through the entire design system, removes the need to define and create the physical hardware prior to developing a product's software-defined functional intelligence.

It is the unique 'soft' functionality implemented in a design that delivers sustainable product differentiation and not the nature of the physical hardware that it resides on. Today's electronics design tools need to provide high-level systems that unlock that functionality from the constraints of a predefined hardware platform, allowing designers to focus on creating the intelligent, connected products of tomorrow. ■

PLC with PIC16F648A Microcontroller

Part 21

Professor Dr Murat Uzam from Nigde University in Turkey presents a series of articles on a project that focuses on a microcontroller-based PLC. This article describes an example of remotely-controlled model gate system and declares seven different control scenarios to be carried out

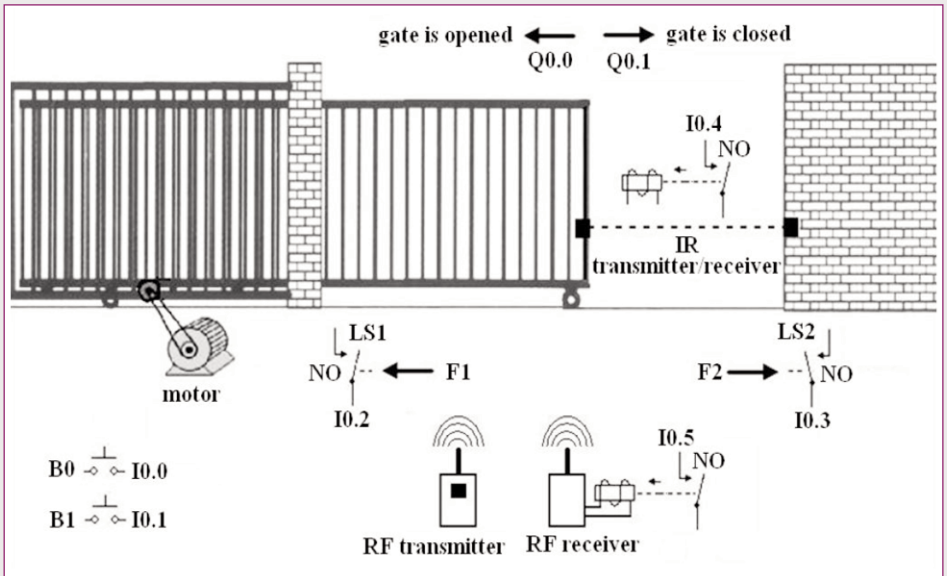


Figure 1: *The remotely controlled model gate system*

Figure 1 shows the remotely controlled model gate system, used in this article as an example to show how UZAM_PLC can be utilized in the control of real systems. In this system, when the DC motor turns backwards (or forwards) the gate is opened (or closed). To control the DC motor in backwards and forwards directions, the UZAM_PLC outputs Q0.0 and Q0.1 are used respectively.

In the system there are two buttons, B0 and B1, and they both have only one normally open (NO) contact. When pressed, button B0 (or B1) is used to give the control system the following order: "open the gate" (or "close the gate"). UZAM_PLC inputs I0.0 and I0.1 are used for identifying the "on" or "off" states of the buttons B0 and B1. When the gate is completely open, it applies the F1 force, shown in Figure 1, to the limit switch 1 (LS1). In this case, the NO contact of LS1 is closed.

To detect whether or not the gate is completely open, the UZAM_PLC input I0.2 is utilized. When the gate is completely closed, it applies the F2 force, shown in Figure 1, on to the limit switch 2 (LS2). In this case, the NO contact of LS2 is closed. To detect whether or not the gate is completely closed, the UZAM_PLC input I0.3 is utilized. An infrared (IR) transmitter/receiver sensor is used to detect if there is any obstacle in the gate's path. This is very important because when the gate is closing there shouldn't be any obstacle in its path in order not to cause any damage to anybody or anything. When the light emitted from the IR transmitter is received from the IR receiver, the NO contact of the sensor in closed. In this case, we conclude that there is no obstacle in the path.

When the light emitted from the IR transmitter is not received from the IR receiver, the NO contact of the sensor is open, i.e. in its normal condition. This means that there is an obstacle in the path. To detect whether or not there is an obstacle in the path, the UZAM_PLC input I0.4 is utilized. In addition, there is also an RF (Radio Frequency) transmitter/receiver used as a remote control mechanism within the system. In the RF transmitter there is a button. When this button is pressed, the RF waves are emitted from the transmitter and they are received from the RF receiver. In this case, NO contact at the RF receiver is closed, signalling the button press from the RF transmitter counterpart. To detect

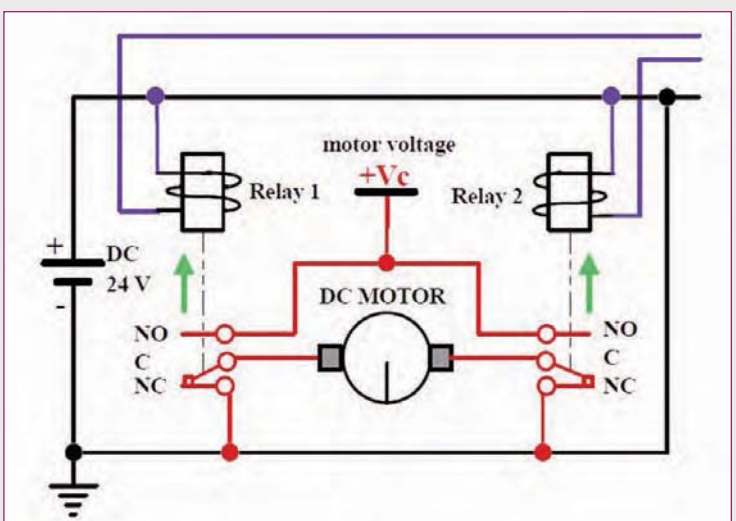


Figure 2: *The DC motor control circuit embedded within the model gate system*

whether or not the RF transmitter button is pressed, the UZAM_PLC input I0.5 is utilized.

The DC motor control circuit embedded within the model gate system is depicted in **Figure 2**, where there are two relays, Relay 1 and Relay 2, operating at 24V DC. Both of them have an SPDT (Single Pole, Double Throw) contact, with the terminals named NO (Normally Open), C (Common) and NC (Normally Closed). Terminal C is shared between the other two contacts.

The normal states of the contacts are shown in Figure 2. In this case, the C and NC terminals of both relays are "closed", while C and NO terminals are "open". If any of these relays' coils is energized, the contacts are actuated and, as such, the C and NC terminals of the relay are "open", while the C and NO terminals are "closed".

With this set-up, by means of the two relays, we can have the DC motor turning forwards or backwards as shown in **Table 1**. It is important to note that if both relays are ON, then the DC motor will not be working. One terminal of each relay coil is connected to 24V DC, while the other one is left unconnected.

To operate any relay it is necessary to connect its open terminal to the ground of the 24V DC. The control of the DC motor is achieved by means of the Q0.0 and Q0.1 outputs of the UZAM_PLC. As can be seen from **Figure 3**, when Q0.0 is ON (and Q0.1 is OFF), the NO contact of Q0.0 will switch on Relay 2, in which case the motor turns backwards and the gate is opened. Similarly, when Q0.1 is ON (and Q0.0 is OFF), the NO contact of Q0.1 will switch on Relay 1, in which case the motor turns forwards and the gate is closed.

Figure 3 shows the wiring of the UZAM_PLC with the remotely controlled model gate system. In this set-up, when any of the NO contacts of the model gate system are closed or a button is pressed, 5V DC is applied to related UZAM_PLC input.

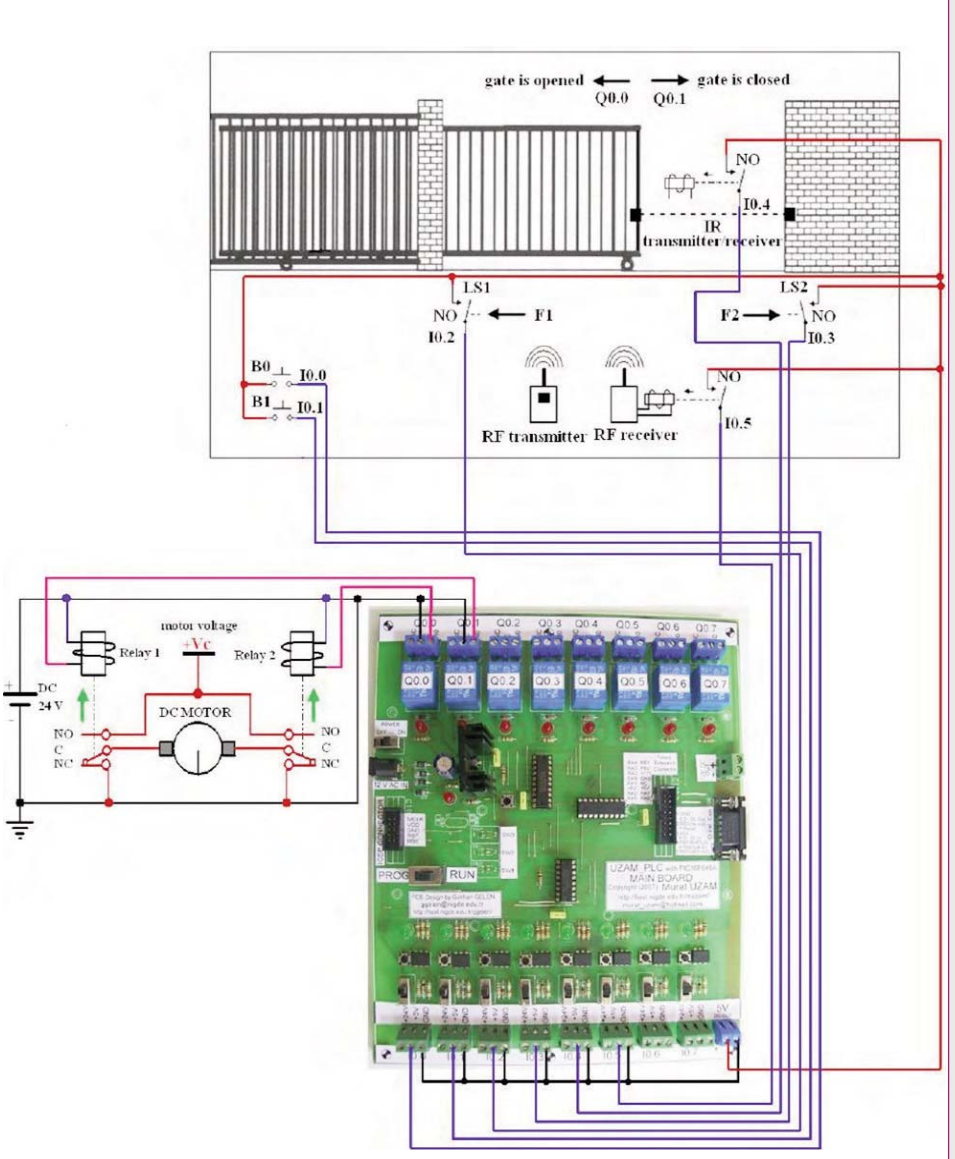


Figure 3: *Wiring of UZAM_PLC with the model gate system*

Relay 1	Relay 2	DC motor
OFF(Q0.1=0)	OFF(Q0.0=0)	OFF (not working)
OFF(Q0.1=0)	ON (Q0.0=1)	Turns backwards (the gate is opened)
ON (Q0.1=1)	OFF(Q0.0=0)	Turns forwards (the gate is closed)
ON (Q0.1=1)	ON (Q0.0=1)	OFF (not working)

Table 1: *The state of the DC motor based on two relays*

Control Scenarios for the Model Gate System

In this section we will declare seven different control scenarios for the remotely controlled model gate system as follows:

1. When B0 is being pressed, the gate will open.
2. Once B0 is pressed, the gate will open.
3. Once B0 is pressed, the gate will open. The motor will stop when the gate is completely open.
4. Once B0 is pressed, the gate will open. The motor will stop when the gate is completely open. Once B1 is pressed, the gate will close. The motor will stop when the gate is completely closed.
5. If the gate is not closing, then once B0 is pressed, the gate will open. The motor will stop when the gate is completely open. If the gate is not opening, then once B1 is pressed, the gate will close. The motor will stop when the gate is completely closed.
6. If the gate is not closing, then once B0 or RF transmitter button is pressed, the gate will open. The motor will stop when the gate is completely open. When the gate is completely open, it will wait five seconds before automatically closing. The motor will stop when the gate is completely closed.
7. If the gate is not closing, then once B0 or the RF transmitter button is pressed, the gate will open. The motor will stop when the gate is completely open. When the gate is completely open, it will wait five seconds before automatically closing. The motor will stop when the gate is closing, if there is an obstacle in the gate's path, the gate will open. In this case it will wait five seconds before automatically closing as defined above. ■

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TIP 1: DISCRETE LED DISCONNECT PROVIDES FAST LED TURN ON AFTER LONG LED OFF TIME

By Keith Szolusha, Senior Applications Engineer, Linear Technology Corporation

LEDS USED IN

machine automation and flash photography sometimes require fast turn on time and long off time. It is not always possible by conventional methods to achieve 100us regulated LED current turn on after being shut off for more than a few seconds.

Conventionally, for energy savings, the shutdown function is used to turn the LED driver off for longer periods of time. In shutdown, the output voltage falls and the restart after shutdown invokes soft-start to prevent high inrush currents. This causes relatively long and controlled turn on. PWM turns the LEDs on and off, but is usually designed for repetitive and short on and off times at 100Hz and higher.

During the short off time, the output capacitor is expected to hold its value

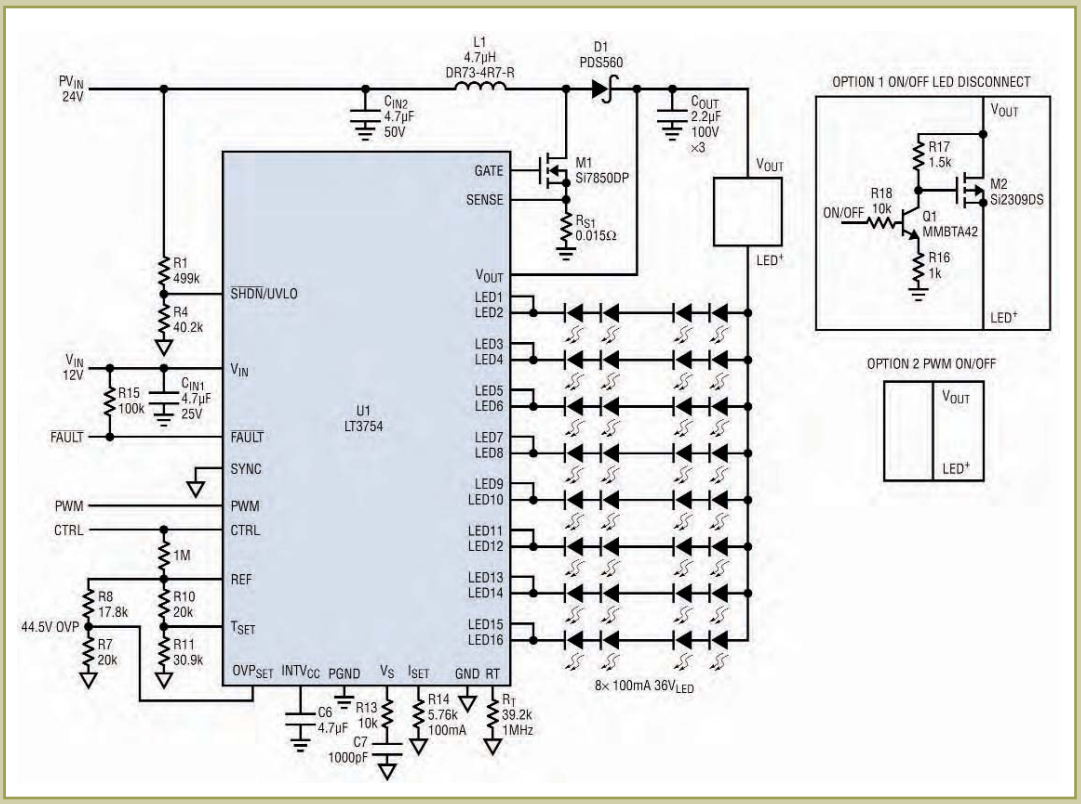

Figure 1: *LT3754 16-channel 50mA LED driver has discrete LED disconnect (option 1) with less than 100us turn on after long LED disconnect time. Option 2 is the conventional LED string connection to the output for typical PWM dimming and shutdown – but not fast enough for machine automation*

Figure 2a: *Fast LED turn on using LED disconnect option 1 after 5s LED off*

despite some minimized leakage. The ability for the output capacitor to hold its voltage during PWM OFF is crucial for LTC's LED drivers' extremely high PWM dimming ratios. With PWM held low for a long time, the output voltage can still collapse. Subsequent turn on can be ten times or more too slow for machine automation. A different method for turning off the LEDs and keeping the output voltage from collapsing (other than using gigantic and unacceptable output caps) is needed.

Using a discrete LED disconnect without turning PWM OFF or shutting the converter down is an alternative method that provides as low as 100us turn on after more than several seconds of disconnect with the LT3754 16-channel LED driver in **Figure 1**. When the LEDs are disconnected from the circuit but the IC remains running, the LED current drops to zero and the output voltage regulates up to the OVP level (higher than the LEDs). The output never collapses, in fact, it rises and regulates high.

When the LEDs are reconnected after any amount of time, the LED current quickly settles at its programmed 100mA level (50mA per channel with two channels in parallel for eight LED strings). The high output voltage allows the internal eight string ballaster to operate immediately. The ballast LED pin voltages quickly rise up to the level needed for 100mA through each LED string tied to the high output voltage. Then the output voltage and ballast voltage drop down to their expected operating points with the LEDs turned on.

Figure 2a shows the LED current with 100us turn on using the discrete LED disconnect shown in Figure 1. **Figure 2b** shows the 1.35ms LED current turn on in comparison with 2a when the conventional LED connection is made and PWM is used to turn the LEDs on and off. In both cases, the LEDs were held off for five seconds before being turned on. ■

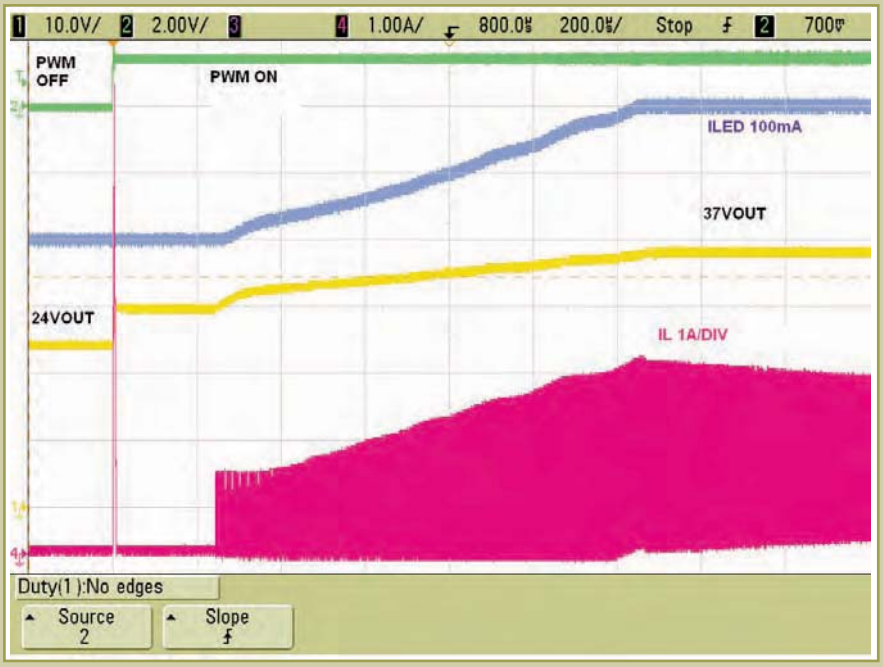

Figure 2b: *LED turn on using conventional option 2 PWM dimming after 5s PWM off*

ALL-PASS FILTERS EMPLOYING DIFFERENTIAL OP-AMPS

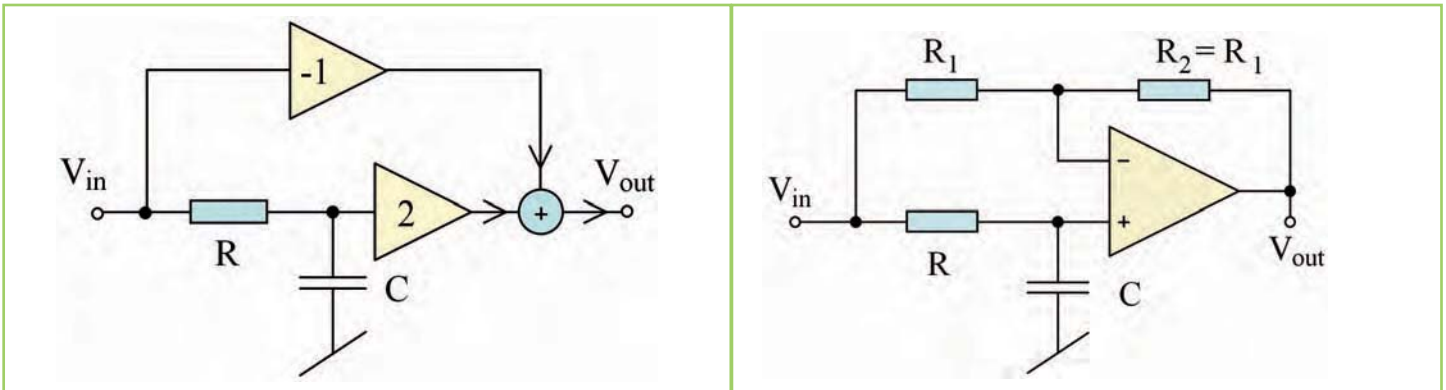

Figure 1: *All-pass cell, version 1:* ***(a)*** *notional principle;* ***(b)*** *op-amp implementation*

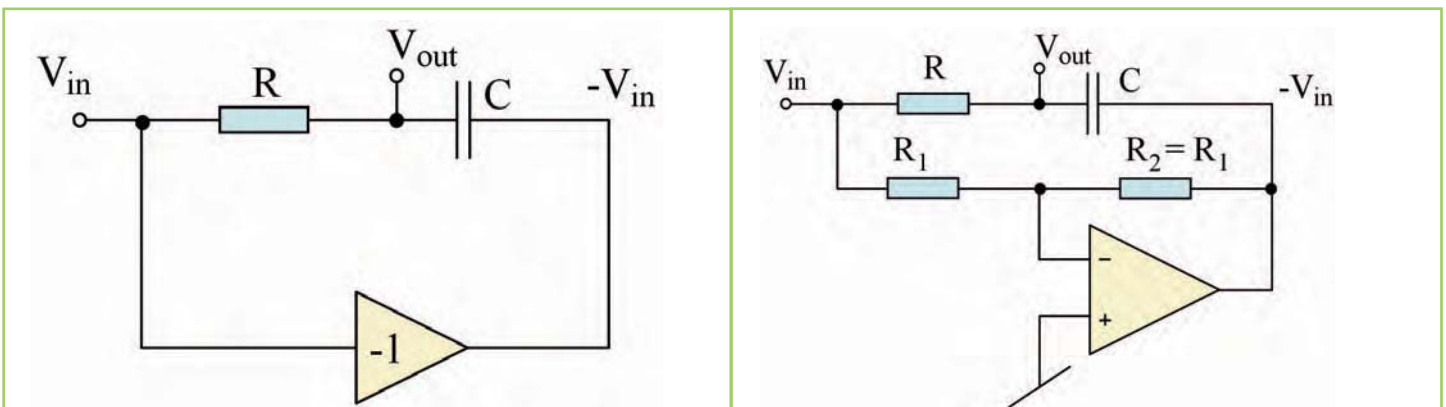

Figure 2: *All-pass cell, version 2:* ***(a)*** *notional principle;* ***(b)*** *op-amp implementation*

ALL-PASS FILTERS belong to basic circuits with their wide utilization in communication systems, measurements and instrumentation electronics. The purpose of 1st-order all-pass filters is to provide the phase shift of the processed signal within an interval of 0-180 degrees depending on its frequency while preserving constant amplitude. As a circuit, the all-pass cell can be designed in two versions with the following transfer functions:

$$\frac{V_{out}}{V_{in}} = \pm \frac{\omega_0 - s}{\omega_0 + s}, s = j\omega \quad (1)$$

Here the sign ± is for the non-inverting/inverting version. If the signal frequency is equal to the characteristic frequency ω_0, the phase shift between Vout and Vin is 90 degrees less than the low-frequency phase shift. The follow-up increase of the frequency causes a continuous increase of this phase shift towards 180 degrees. The characteristic frequency is determined by the all-pass cell structure.

The most popular operational amplifier (op-amp) based designs of all-pass cells are shown in **Figures 1** and **2**, together with their ideal operation diagrams. In Figure 1a, the output voltage of the RC cell is twice amplified and the input voltage is subtracted from the result. Both operations can be smartly accomplished by a single op-amp according to Figure 1b.

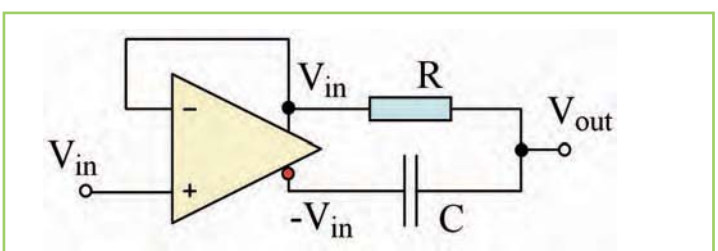

Figure 3: *All-pass filter employing a differential op-amp, version 1*

Figure 2 shows another principle: the RC cell is connected as a floating two-terminal device between the +Vin and -Vin nodes, and the output voltage is taken across the common R and C node and ground. The voltage -Vin is generated from +Vin by the inverting amplifier as in Figure 2b. Either circuit can implement a non-inverting version of the transfer function shown in Equation 1.

The inverting version can be obtained by interchanging R and C. The characteristic frequency is given by the following, simple, equation:

$$\omega_0 = 1/RC \quad (2)$$

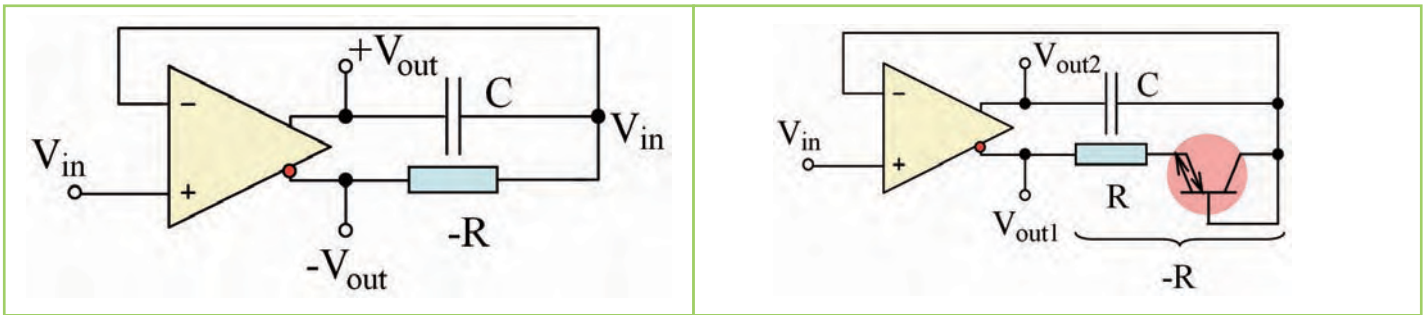

Figure 4: *All-pass filter employing a differential op-amp, version 2:* ***(a)*** *principle, utilizing negative resistance;* ***(b)*** *implementation by a diamond transistor*

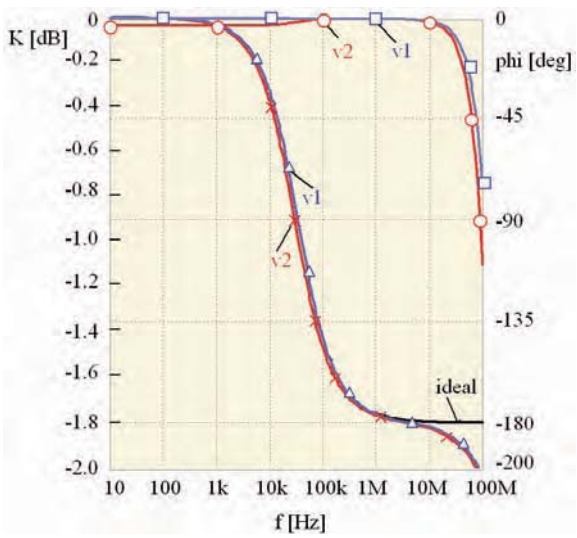

Figure 5: *Experimental frequency responses of all-pass cells with differential op-amps: version 1 (v1), version 2 (v2)*

These circuits have been known for many years. The circuit in Figure 1b was published by Genin in 1968 and Aronhime, Budak and Bhattacharyya proposed the circuit in Figure 2b a year later. The advantage of the circuit in Figure 1b lies in the low output impedance, whereas the output of the circuit in Figure 2b should be buffered.

A common drawback of both filters lies in their frequency-dependent input impedance and also in the necessity of observing the condition R1 = R2 as accurately as possible.

In addition to common op-amps, commercial op-amps with differential outputs are currently available, with output voltages of both polarities. This fact can be utilized for designing new topologies of all-pass cells in which there is no necessity to set matching conditions such as R1 = R2.

A description of two new circuits follows. The first is a simplification of the circuit in Figure 2b, the other is based on a new principle.

Novel All-Pass Cells Based on Differential Op-Amps

The all-pass filter in **Figure 3** is an economical version of the circuit in Figure 2b. Negative feedback from the non-inverting output to the inverting input makes the op-amp operate as unity-gain follower with respect to the non-inverting output, and as unity-gain inverter with respect to the inverting output.

The RC cell is thus connected between the +Vin and -Vin nodes just like in the original circuit in Figure 2b, but without the need to use an additional inverter with two resistors. The high-impedance input is another advantage of this circuit. A drawback, inherited from the original circuit principle, is the need to additionally buffer the output terminal.

The root of the all-pass cell in **Figure 4a** is again formed by the RC cell. In contrast to the circuit of Figure 2a, it is now connected between the +Vout and -Vout nodes, and the cell is driven by voltage Vin across the common node of R and C and ground. In other words, the input and output signals are mutually interchanged, compared to the principle of the circuit in Figure 2a, and the transfer function of this cell is an inversion of those in Equation 1.

However, the numerator/denominator replacement in Equation 1 will result in a transfer function of an unstable circuit. A formal solution to this problem consists of considering a negative resistance as in Figure 4a. Then the corresponding transfer function is again in the form of Equation 1.

Positive resistance can be easily transformed into negative resistance with the help of a diamond transistor (OPA860), connected in series with the resistor R, as in **Figure 4b**. The transistor operates as a current 'conveyor' of second order (CCII) such that the current, flowing from the resistor to the emitter, moves toward the collector and thus its direction is reversed.

The voltage drop at the transistor, i.e. between the base and emitter, is ideally zero. In reality, the transistor adds a small resistance RT = 1/gm (of about 10Ω) in series with R, where gm is the transconductance of the diamond transistor (of about 0.1 A/V). The gm can be set by a bias current. When designing the all-pass cell, the resistance R should be selected minus this value.

This circuit provides several advantages: high input and also low output impedance, simultaneous utilization of both outputs which provide non-inverting and inverting versions, and the possibility to electronically cut off the characteristic frequency by means of gm tuning of diamond transistor.

Experimental Verification

To verify the functionality of the filters from Figures 3 and 4b, the LMH6550 differential operational amplifier with symmetrical supply voltages ±5V was used. The OPA860 diamond transistor, used in the circuit of Figure 4b, was supplied in the same way. Its transconductance was set to 100mA/V via an auxiliary resistor RADJ = 330Ω, according to the datasheet of the LMH6550 from National Semiconductor.

The R and C values of 100Ω and 47nF were used, and the corresponding theoretical values of the characteristic frequency according to Equation 2 are 33.9kHz for the circuit in Figure 3 and 30.8kHz for the filter in Figure 4b. The frequency responses of both filters (**Figure 5**) are in good agreement with the theoretical curves. The f0 frequency measured is 33.8kHz for the circuit in Figure 3 and 29.6kHz for the circuit in Figure 4b. ■

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LED BACKLIGHT DRIVER IC FOR LARGE DISPLAYS

The new A8512 from Allegro MicroSystems Europe is a multi-output white LED RGB driver IC for the LED backlighting of large-area LCD monitors and television screens.

The new device integrates a scalable-output boost controller operating in constant-frequency current mode control – adjustable between 300kHz and 1MHz, driving an external MOSFET. It integrates six internal current sinks each capable of sinking up to 80mA, which can be combined together to achieve even higher currents. PWM dimming allows LED currents to be precisely controlled over a 500:1 ratio as a percentage of the maximum set point determined by the user.

Multiple A8512 devices can be connected in parallel, with one master controller controlling the boost stage and up to five slave controllers acting as LED sinks. This configuration allows up to 36 LED strings to be powered by a single boost converter, significantly reducing the number of external components required.

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These cost-effective sensors are perfectly suited for use in energy-recovery systems, air handling units, underfloor heating and other HVAC applications.

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EAGLE CAD TOOL NOW INCORPORATES DESIGNLINK

Premier Farnell has announced the launch of EAGLE software version 5.10.0, the latest version of CadSoft's award winning EAGLE software that now incorporates "DesignLink", giving electronic design engineers (EDEs) complete flexibility to manipulate component data. With this tool, designers can 'cut and slice' information in any which way they need to.

The latest version of EAGLE provides EDEs with an array of new functions that allow them to write user language programs (ULPs) to do things such as pricing of the current schematic under development, as well as the ability to update previously existing designs with pricing and availability. Not only that, EAGLE users can write a ULP to select and add component attributes.

The software is now available from element14, the company's innovative technology eCommunity for EDEs, bringing Web 2.0 to engineers along with over 10,000 technical documents and software tools. Customers can find the DesignLink credentials required directly from the element14 website.

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THR CONNECTOR SOLUTIONS FROM WIELAND ELECTRIC

In response to increased use of surface mount devices (SMD), Wieland Electric has introduced a range of Through Hole Reflow (THR) connector solutions for use with two-piece connectors and single-piece terminal blocks. Savings of up to 30% in manufacturing costs can be achieved using Wieland's THR printed circuit board connectors, which are available in 3.5mm, 3.81mm, 5mm and 5.08mm. The temperature resistance required for the reflow process is achieved through the use of a new insulating material.

With this technology, THR and SMD can be processed simultaneously using the same equipment. On the solder templates, the holes for the THR compatible connectors can be placed next to the SMD components. During the board printing process, the lead-free solder paste is pressed into the holes and during the mounting of components onto the board, the solder pins are placed through the paste and into the holes.

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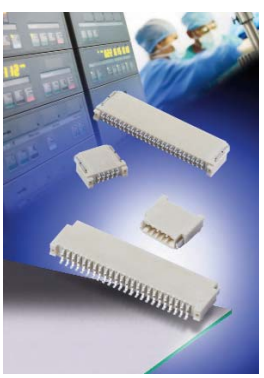
AVX LAUNCHES COST-EFFECTIVE 0.5MM PITCH LIF CONNECTOR SERIES

AVX Corporation has developed a new range of 0.5mm pitch low insertion force (LIF) FFC/FPC connectors for price-sensitive applications, such as white and brown goods including audio/video/recording devices, set-top boxes and satellite receivers. Series 6284 connectors feature a staggered dual contact arrangement which results in a low insertion force and makes positioning and insertion of the FFC/FPC cable easier. However the design does not compromise mating security; although 6284 connectors require a lower insertion force – nearly 25% less than other LIF connectors – their separation force is around double that of other designs.



With a low profile of 1.5mm, 6284 connectors are available in 8, 10, 12, 15, 16, 20, 24, 26, 30, 40, 50, 55 and 60 ways, which can be increased for new projects. Operating temperature range is -40 to +85degC which can be extended to 105degC on request to meet automotive standards.

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NEW VEAM CIR-M12 DATABUS CIRCULAR BAYONET CONNECTOR

ITT Interconnect Solutions new VEAM CIR-M12 Databus connector has been designed to meet the challenge of enabling a variety of different data types to be transmitted between coaches in modern mass transit systems. In particular, customers in this sector requested a solution which bundled multiple Ethernet and MVB lines into a singular connector.

ITT ICS mounted its new Quadrax QXM12 contacts into FRCIR connector circular bayonet series hardware. With this pioneering design, four conductor wires and the associated braid from shielded cables are integrated into the QXM12 contact. A special plastic insert groups multiple QXM12 contacts and their cables into a singular connector. With this connector, designers can incorporate data transfer from Ethernet, MVB, WTB and video lines, according to VG95234 (where applicable), within the same connector, handling diverse data feeds such as engine diagnostics, brake controls, environmental conditioning, passenger display systems, networking and lighting control.

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The modular 19-inch 6U MicroTCA platforms are redundant and compliant with the MTCA.1 specification for applications with the highest demands for robustness, availability and performance. Applications include infrastructure nodes for mobile telephony, public safety engineering, medical and military.

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Housings for the Vario-Module are now supplied as either basic or EMC frames for standard and double Euroboards, to which a choice of plain or ventilated top and bottom covers can be added in a "pick and mix" fashion according to the application. A mounting plate is also now available to avoid perforating the bottom cover when mounting heavy or awkward components.

Vario-Module cases may be completed as desktop, rack-mount or tower units with the dimensions conforming to IEC 60 297-3-101, the subrack standard. Internal fittings are standard parts from the Ripac subrack range and may be configured to hold VME, CompactPCI or other backplane systems.

www.rittal.co.uk

NEW PCB RETAINER DESIGN ELIMINATES THE NEED FOR A TORQUE WRENCH

New from Schroff are the Calmark Series 223 and 224 Card-Lok PCB retainers, which incorporate a patent-pending torque-limiting feature that enables a PCB assembly to be fixed into a chassis at a prescribed clamping force without the need for a torque wrench.

Primarily aimed at cold-plate heat-transfer applications within the defence and aerospace sector, these new five-wedge devices are designed to prevent damage to the PCB or to the Card-Lok itself due to over-tightening.

By turning the centre screw clockwise, the outer wedges are drawn together, forcing the centre wedge sections to expand outwards. When the turning force exerted on the screw reaches the preset torque, the built-in ratchet clutch disengages with an audible click to prevent further tightening.

The Series 223 and 224 retainers generate a minimum clamping force of 1200N when torqued. As well as providing maximum resistance to shock and vibration, the Card-Loks also play a major role in dissipating heat from the PCB.

www.calmark.com

SINGLE-BOX MULTI-RAT TESTER FOR MULTI-MODE EHRPD/LTE HANDSETS

Aeroflex launched a new option for the 7100 LTE Digital Radio Test Set that supports CDMA-based data standards such as Evolution-Data Optimized (EV-DO) and evolved High Rate Packet Data (eHRPD) as well as LTE-eHRPD handover.

As CDMA network operators migrate towards LTE, the devices used by their subscribers will need to operate with both the legacy EV-DO sectors of the network and those that have been upgraded to LTE, as well as being able to hand over seamlessly between them. Option 104 for the Aeroflex 7100 tester has been developed to allow testing of these multi-mode devices across all the standards they are required to support, and also to test hand-over between LTE and eHRPD.

The Aeroflex 7100 with Option 104 provides test capabilities for EV-DO Release 0, EV-DO Revision A and eHRPD, an important stepping stone in a CDMA and LTE network rollout.

www.aeroflex.com

COST-EFFECTIVE WLAN ACCESS POINT FOR UNINTERRUPTED CONNECTIONS

Belden has extended its range of Hirschmann products to include the new WLAN Access Point BAT54-Rail Single. This device is designed for mounting on a top-hat rail and can be used both as Access Point and Access Client. Unlike the BAT54-Rail, this new Access Point has only one WLAN interface, making it a cost-effective alternative for applications that do not require a second interface. In common with its 'elder brother', however, the BAT54-Rail Single offers the full range of functions supported by the powerful HiLCOS operating system.

This Access Point offers transmission rates of up to 108Mbit/s in either the 5GHz or 2.4GHz waveband. Fast roaming facilitates uninterrupted connections, even while changing from one radio cell to another. Network management can be carried out using browser-based, Telnet or Windows software that supports rogue AP detection, and all standard encryption methods as well as authentication compliant with IEEE 802.1x are also available.

www.belden.com

VECTOR INTEGRATES ADDITIONAL PROCESS AREAS IN THE EASEE AUTOMOTIVE E/E SOLUTION

In release V1.3 of the eASEE Automotive Solution, Vector is integrating the process areas Requirements Management, System Data Management and Test Data Management in one solution. The common data backbone circumvents tool limits and enables quick access to all engineering data. This leads to quickly realized efficiency gains. The eASEE Automotive Solution is customized to the requirements, artifacts and processes of automotive E/E development.

The core of the solution is the integrated System Data Management. It provides a universally consistent systems engineering environment. This environment seamlessly interconnects all applications: from the description of the vehicle electronics to the functional level, logical and technical architecture levels and, finally, the software architecture of ECUs. This will benefit all E/E development departments striving for data consistency and role-specific engineering support.

Plans call for integrating the process areas Change Management, Project Planning and Release Planning and an interface to Simulink.

www.vector.com

TTI ADDS TOSHIBA ELECTRONICS TO ITS PORTFOLIO

TTI Inc has announced that is has signed a pan-European franchise deal with Toshiba Electronics Europe to stock and support the semiconductor company's power, discrete, optoelectronic, logic and motor control driver products. In North America, TTI Inc has already become Toshiba's premier authorized distributor of these technologies and TTI expects to have similar success in Europe.

Products covered by the new agreement include high and low voltage MOSFETs, optocouplers, LEDs including high-power white LEDs, diodes and a wide variety of discrete components, ranging from low noise amplifiers to bus switches and Single Gate Logic. Motor control solutions include optimized MOSFETs and highly integrated single-chip inverters.

Geoff Breed, Vice President Marketing for Europe at TTI Inc said: "Toshiba has been ranked number one supplier of discrete components worldwide since 1986. We added discrete components to our European portfolio in 2008 and Toshiba fits naturally with our line card."

www.ttieurope.com

www.toshiba-components.com

EEMBC ANNOUNCES NEW WORKGROUP DEVELOPING COMPREHENSIVE **FLOATING-POINT BENCHMARK SUITE**

The Embedded Microprocessor Benchmark Consortium (EEMBC) announced it is developing new benchmarks that will track the performance of embedded processors with floating-point hardware units, an increasingly popular chip feature for graphics, audio, motor control and other high-end processing tasks.

Floating point (FP) refers to the ability of an embedded processor to crunch numbers that are too large or small to be represented as integers. Today, many embedded processors include hardware FP units (FPUs) to enable higher levels of precision. The new EEMBC benchmarks will allow users to evaluate FPU performance on the basis of consistent and controlled data, thus serving the needs of processor vendors, compiler vendors and system developers alike.

"The new benchmarks will enable system developers to make their own unbiased evaluations and compare their own workloads to the specific benchmarks," said Ron Olson of IBM, one of the Leaders of the EEMBC workgroup.

Examples of the real-world applications that the forthcoming FP suite will likely address include DSP filtering, audio encoding, video encoding and PID motor control, but also a series of generic kernels such as bi-cubic filtering and FFT, which are particularly revealing of FPU performance. The benchmarks will likewise measure the performance data between single (32-bit) and double (64-bit) precision.

Our panel of commentators says the following on this development:

BURKHARD VOGEL, MANAGING DIRECTOR, GERMANY:

I'm surprised how long it took in finding a common basis on this issue. It would be very interesting to find out the obstacles that hindered the respective evolution in the past. Pressure from competition, maybe?

BARRY MCKEOWN, RF AND MICROWAVE ENGINEER IN THE DEFENCE INDUSTRY, AND DIRECTOR OF DATOD LTD, UK:

I once had a colleague who began to investigate the effects of the Matlab FFT that were occurring at the order of 350dB down, before the question of where the noise floor would be in the real application if the input data was obtained from a real instrument as opposed to a Matlab model arose. The answer on determining this fact is not printable. It was a valuable lesson.

The most basic of benchmarks is the thermal noise floor model associated with kTB: in engineered systems this equates too -174dBm in a 1Hz bandwidth of 50ohm impedance. Deciding between a fixed point or floating point processor fundamentally relates to the software overhead involving the AtoD and DtoA conversion dynamic ranges and signal processing bandwidth requirements for the application sought. As there are no floating converters available, attention should always be exercised to ensure that the massive dynamic ranges required for scientific FP computing are properly benchmarked to the thermal noise floor in the analogue and digital signal processing chain.

PROFESSOR DR DOGAN IBRAHIM FROM THE NEAR EAST UNIVERSITY IN NICOSIA, CYPRUS:

Floating point operations are highly important in most real-time embedded applications. Fast and efficient floating point number-crunching is required in time-critical applications, such as in image processing, audio encoding, video encoding and in many other digital signal processing applications. Some low-end embedded processors are equipped with hardware multiplier modules in order to simplify and speed-up the floating point operations. Most high-end embedded processors incorporate floating point hardware modules to enable them to be used in non-integer and high-precision mathematical operations demanded by graphics, image, video, audio, motor control and many other high-end complex tasks.

It is good news that the EEMBC is developing new benchmark standards to track the performance of embedded processors with floating point hardware modules. With the new benchmark standards, the designers will be able to make their own unbiased evaluations and comparisons of various FPUs, before the most suitable one for a given task is chosen. In addition, the chip manufacturers will be able to optimize the performance of their FPU hardware by developing chips and comparing their performances using the EEMBC benchmarks.

MAURIZIO DI PAOLO EMILIO, TELECOMMUNICATIONS ENGINEER, INFN – LABORATORI NAZIONALI DEL GRAN SASSO, ITALY:

The advantage of floating-point representation over fixed-point (and integer) representation is that it can support a much wider range of values. The floating-point format needs slightly more storage, so when stored in the same space, floating-point numbers achieve their greater range at the expense of precision.

Without a doubt, floating point implementations of many algorithms take fewer cycles to execute than fixed point code. Floating-point processors are also often much easier to program in assembly code.

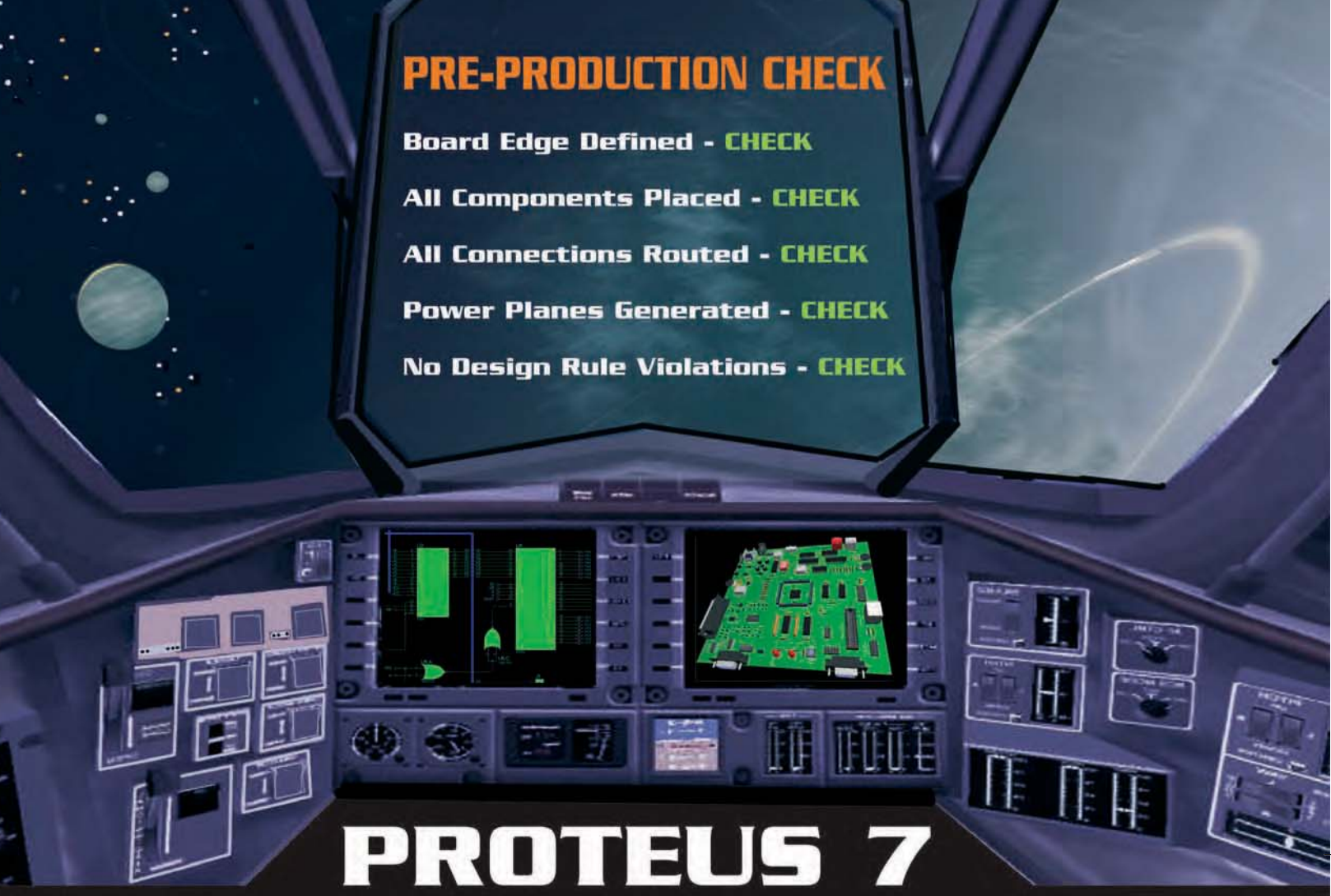
With the quality of compilers getting better and better each day, hardly anyone codes in assembly anymore, and writing code in C is nearly equally simple, be it fixed or floating point.

HAFIDH MECHERGUI, ASSOCIATE PROFESSOR IN ELECTRICAL ENGINEERING AT THE UNIVERSITY OF TUNISIA:

The spectacular evolution of digital electronics and integration with large scales of the components made it possible to develop increasingly fast PC and carrying out an infinitely large number of calculations at the same time.

Indeed, the units of floating-point calculation are processors or part of a processor particularly designed to carry out operations on comma floating numbers.

One can carry out even exponential or trigonometric calculations.



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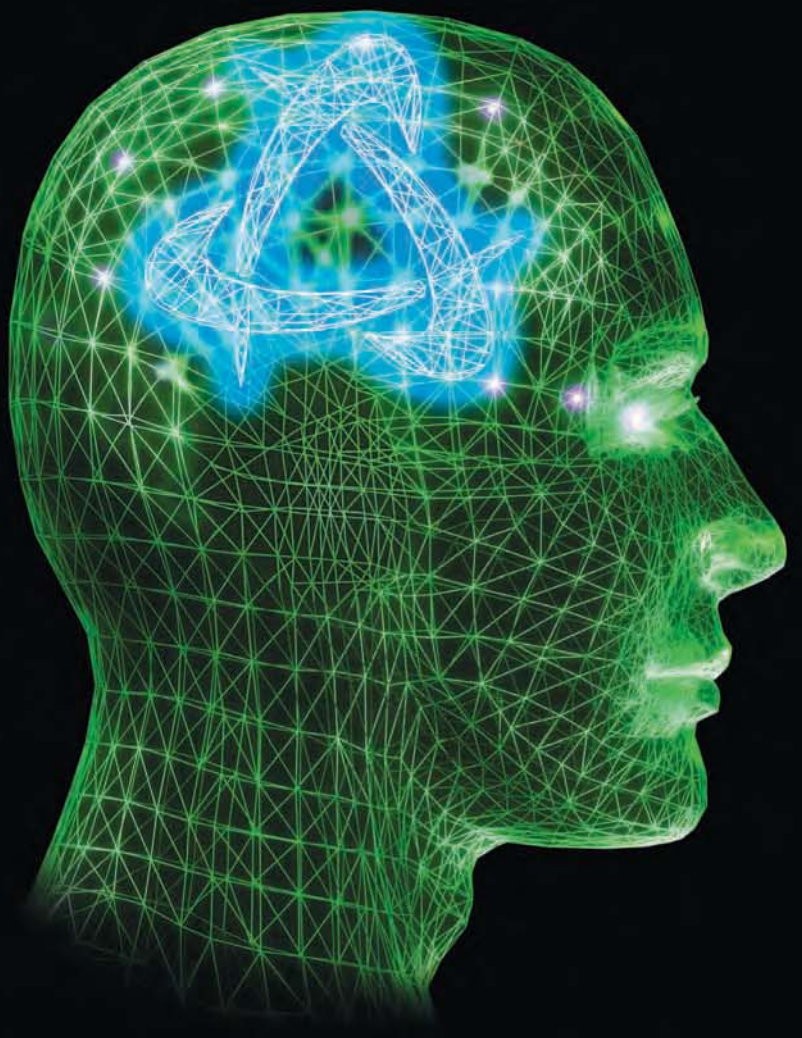

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