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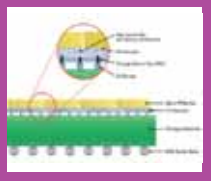

TECHNOLOGY
'MORE THAN MOORE' FPGAS

FOCUS
MEETING MOBILE BROADBAND DEMAND

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ALSO IN THIS ISSUE: ENERGY EFFICIENCY IS COVERED IN TREND, INSIGHT, LAST NOTE

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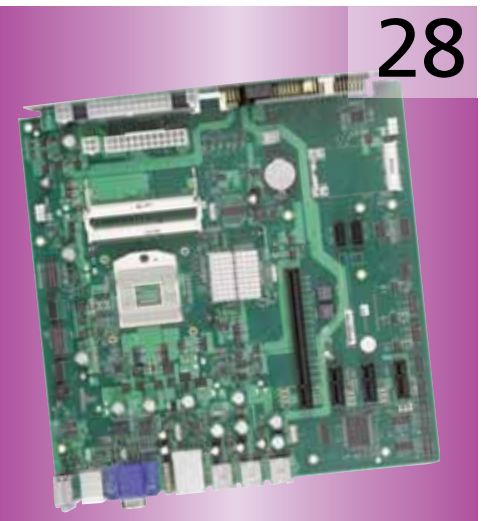

FEATURES

Cover supplied by PEI GENESIS More about its 48-hour assembly on pages 12 - 13

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INTELLIGENT ENERGY METER MAKES SMARTER CONSUMERS

In the future, Intelligent Energy Metering will be all that is required to manage all domestic utilities. Sophisticated metering solutions will accurately measure electricity consumption of each home appliance, providing consumers with unprecedented level of control over home energy usage.

They'll be capable of monitoring gas and water usage and also home-generated electricity for sale back to the grid. Home energy hubs will offer distribution companies a single point to monitor multiple utilities and develop more creative billing options.

Energy billing is set to become more complex. As homeowners begin to sell back to the grid energy they generate from solar panels and wind turbines, so new approaches are needed to tackle this complexity and provide intelligent switches.

Nick Wellington of Navetas, the company who in conjunction with Cambridge Design Partnership and Oxford University has already developed one such intelligent energy hub, explains that the intelligent meter, together with its separate display unit, has been developed to be easy to install by utility companies and intuitive to use by consumers.

"Home energy monitor products have recently become popular, but these have limited functionality as they only provide an estimate of usage," he said. "The problem for the householder is that the final bill can vary widely from this estimate. Our solution provides an accurate measure of the actual energy usage and can be broken down by appliance. It is possible then to compare the efficiency of appliances and see at a glance where energy is being used."

The trend is to have smart hubs easily retro-fitted by the utility company at the point where the service enters the house. The information can then be sent wirelessly and made available to the householder through a touch-screen display located in the house.

The ability to drill down to the consumption of individual appliances comes from a new technology that identifies the 'signatures' of individual electrical appliances by interpreting both mains voltage and current electricity waveforms.

The benefit to the customer is that usage is displayed in real time and it can quickly be identified where savings can be made. It also paves the way for novel billing models, which could reward greener energy use and assist in 'load levelling' of the national grid.

"If people are aware of the true cost of their consumption of services they are in a stronger position to introduce strategies that will save them money and cut down on waste," said Richard Hunt of Cambridge Design Partnership. "Our work has been directed at making this information easy to collect and display in a format that the householder can understand and act upon."

Intelligent energy metering is seen as a fast-growing trend and various players are entering the market already. "This is a huge and growing international market," confirmed Navetas's Wellington.

"AS HOMEOWNERS BEGIN TO SELL BACK TO THE GRID ENERGY THEY GENERATE FROM SOLAR PANELS AND WIND TURBINES, SO NEW APPROACHES ARE NEEDED TO TACKLE THIS COMPLEXITY AND PROVIDE INTELLIGENT SWITCHES"

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RESEARCHERS USING THE DIAMOND LIGHT SOURCE DISCOVER THE POTENTIAL OF LEAD-FREE PIEZOELECTRIC CERAMICS

Diamond Light Source, the UK's national synchrotron facility

Scientists from the Institute for Materials Research at the University of Leeds's Faculty of Engineering used the Diamond Light Source, the UK's national synchrotron facility, to investigate the structure and properties of piezoelectric ceramics in order to develop more environmentally-friendly alternatives to the widely-used but toxic ceramic crystal lead zirconium titanate (PZT).

The team used the I15 Extreme Conditions beamline at Diamond to probe the interior crystal structure of the ceramics with a high-energy pinpoint X-ray beam and saw changes in the crystal structure as an electric field was applied. Their results demonstrate that this new material, potassium sodium bismuth titanate (KNBT), shows the potential to perform the same job as its lead counterpart. As such, future electronic gadgets can be less "toxic".

"Although harmless when in use, at the end of their lifetime these PZT gadgets have to be carefully disposed of due to their lead content and, as a consequence, there is significant interest in developing lead-free ceramics," said Dr Tim Comyn, lead investigator on the project.

Piezoelectric materials generate an electrical field when pressure is applied. In an electrical field, the material undergoes a phase transition, changing its crystal structure.

The team will continue to work at Diamond to study the electric field induced transformation at high speed (1000 times per second) and under various conditions using state of the art detectors.

"Not only could a lead-free solution mean safer disposal of electronic equipment, by virtue of the absence of lead, these new materials are far lighter than PZT. The piezoelectric market has applications in many fields, where a lighter lead-free alternative could make quite a difference," added Adam Royles, who is also part of the project.

Lead-based electronic ceramics are one of only a few exemptions to the European directive on the restriction of the use of certain hazardous substances in electrical and electronic components (2002/95/EC). This exemption will be reviewed again in 2012.

The LAST POWER Project Aims to Put Europe First in New Power Semiconductor Technologies

The partners in a new publicly-funded European research project announced details of the multinational/multidisciplinary program called LAST POWER – 'Large Area silicon carbide Substrates and heTeroepitaxial GaN for POWER' device applications.

The aim of this important 42-month ENIAC (European Nanoelectronics Initiative Advisory Council) project is to provide Europe with strategic independence in the field of wide band-gap (WBG) semiconductors. This field is of major strategic importance as it involves the development of highly energy-efficient systems for all applications that need power, from telecommunications to automotive, from consumer electronics to electrical household appliances, and from industrial applications to home automation.

The consortium will develop European technology for the complete production chain for semiconductor devices built with SiC (Silicon Carbide) and heteroepitaxial GaN (Gallium Nitride on silicon wafers). These two semiconductor materials offer higher speed, current capability, breakdown voltage and thermal capability compared to conventional silicon technologies.

"The power semiconductor market, which represents approximately 30% of the overall semiconductor market, is set to change significantly in response to the ever-increasing demand for more energy-efficient devices," said project coordinator Salvatore Coffa, Group Vice President and R&D General Manager, Industrial and Multisegment Sector at STMicroelectronics, a partner in the project. "This key project, which targets secure strategic independence in the emerging field of SiC and GaN technologies, will place Europe at the forefront of energy-efficient devices."

The overall objective of the project is to develop a cost-effective and reliable integration of advanced SiC and GaN semiconductors in the European power microelectronics industry. This will be achieved via five specific objectives, including growth of large area (150mm) SiC and high quality heteroepitaxial GaN on 150mm Si wafers; the development of new dedicated equipment for material growth, characterization and processing; processing of reliable and efficient SiC and GaN devices on 150mm wafers; demonstrating high-performance devices with properties that cannot be obtained on Si, including a 1200V/100A SiC MOSFET, SiC JFET capable of operating up to 250°C, and GaN HEMT devices for power switching; and to develop advanced packages for high-temperatures devices and improve device reliability.

Xilinx Extends FPGA Technology to Deliver "More than Moore" Density, Bandwidth and Power Efficiency

Programmable logic maker Xilinx is using stacked silicon interconnect technology to deliver breakthrough capacity, bandwidth and power savings. It is using multiple FPGA die in a single package for applications that require high transistor and logic density, as well as tremendous levels of computational and bandwidth performance.

The company has used 3D packaging technologies and through-silicon vias (TSV) for its 28nm 7 series FPGAs, to address resource requirements that are more than double the reach of the largest single-die FPGAs. This innovative platform approach enables Xilinx to overcome the boundaries of Moore's Law and offer electronics manufacturers unparalleled power, bandwidth and density optimization for the large-scale-integration of their systems.

"Five years of Xilinx research and development, coupled with industry leading technology from TSMC and our assembly suppliers, has made possible our efforts to provide an innovative solution for enabling electronic systems developers to take the benefits of FPGAs further into their manufacturing flow," said Vincent Tong, Xilinx Senior Vice President.

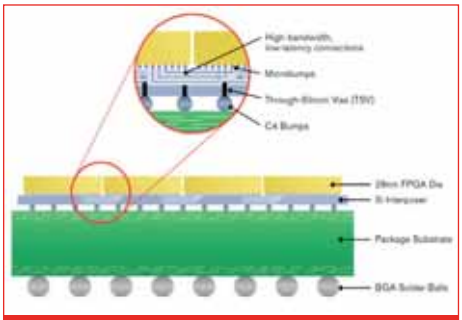


Diagram of the stacked silicon interconnect developed by Xilinx

The 28nm Virtex-7 LX2000T device will be the world's first multi-die FPGA and will provide more than 3.5X the logic capacity of the largest current-generation Xilinx 40nm FPGA with serial transceivers.

"Compared with traditional monolithic FPGAs, multi-chip packaging approach is an innovative way to deliver large-scale programmability with favourable yield, reliability, thermal gradient and stress tolerance characteristics," said Shang-yi Chiang, Senior Vice President of R&D at TSMC. "By using through-silicon via technology and silicon interposer to implement stacked silicon interconnect approach, Xilinx expects to reduce risks and is on the way to volume production with well-designed test vehicle runs that meet the company's criteria for design enablement, manufacturability validation and reliability assessment."

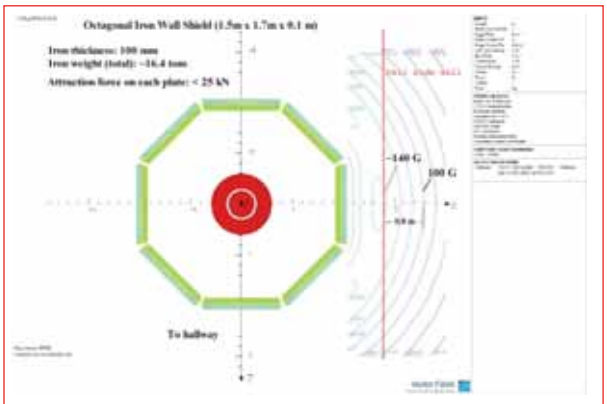
Within the Xilinx stacked silicon interconnect structure, data flows between a set of adjacent FPGA die across more than 10,000 routing connections. Compared with having to use standard I/O connections to integrate two FPGAs together on a circuit board, stacked silicon interconnect technology provides over 100X the die-to-die connectivity bandwidth per watt, at one-fifth the latency, without consuming any high-speed serial or parallel I/O resources. By having die sit adjacent to each other and interfaced to the ball-grid-array, Xilinx can avoid the thermal flux and design tool flow issues that would be introduced had a purely vertical die-stacking approach been taken. Xilinx's choice of 28nm HPL (high-performance, low-power) process technology for the base FPGA device provides a comfortable power budget in the package for integrating FPGA die.

ELECTROMAGNETIC FIELD SIMULATOR HELPS SPEED CHARACTERISATION OF INNOVATIVE HYBRID MAGNET

Cobham Technical Services's Opera 3D electromagnetic field simulator is playing a vital role in the design of an innovative hybrid magnet being developed by the US's National High Magnetic Field Laboratory (NHMFL) in Tallahassee, Florida. The simulator was used to aid the design of the SCH magnet and its shielding.

Electromagnetic shielding of the Series-Connected Hybrid (SCH) magnet, designed for unprecedented power efficiency and field homogeneity, is provided by a set of eight magnetically soft, 100mm thick iron plates which form an octagonal wall around the entire magnet system. The magnetic properties of these shields were characterised by a B-H curve, obtained by using Opera 3D.

"We chose to use Opera v12.0 to evaluate the 3D magnetic field uniformity and fringe fields of the SCH because the simulator is accurate and fast. The inner coils of the SCH are of Florida-Bitter type with essentially non-uniform current densities. To emulate this, we subdivided each coil into a large number of radially thin coils with uniform current densities, and the whole coil system was generated by use of an external program called by Opera from command line," said Iain Dixon, Research Associate at the Magnet Science & Technology division.



Field measurements on SCH electromagnetic shields

The SCH uses a water-cooled Florida-Bitter resistive magnet – a highly innovative technology developed by the MS&T group, capable of generating high magnetic field strengths more efficiently than alternative means. It is nested within a superconducting magnet that is cooled by liquid helium. The two magnets are connected in series and together create a very high intensity central magnetic field of 36T. The SCH is connected to a 650V supply and has an operating current of 20,000A; this 13MW power consumption is 66% less than what would be required for an all-resistive magnet providing the same field and bore.

Opera 3D has also been used for a variety of other performance-related studies on the SCH, including evaluating the magnetic fields around the magnet's HTS (high temperature superconductor) vapour-cooled leads and calculating eddy currents in the thermal radiation shields surrounding the superconducting coil.

Not a module?

Myk Dormer

"WHEN IS A WIRELESS module not a module?" This sounds like the beginning of a very engineer-specific joke, but my intent here is entirely serious. A change, or rather a new development, has begun to appear in the low-power radio module market and it deserves examination.

Traditionally – if such a word can be used for a market sector barely 30 years old – the familiar 'module' is a pretty much self-contained radio circuit, capable of operation with little external support beyond the baseband (data) signals, a power supply and an aerial.

Additional functionality then varies hugely from module to module, from very basic (small, cheap) 'audio path' or 'raw data' devices, up to multi-function, multi-channel 'radio modems' that integrate a great deal of processing power into a powerful, but large and expensive, device. What they all share in common, however, is a defined level of standalone 'works out of the box' autonomy, which in turn gives them one of their main benefits: they are supplied pre-tested and compliant, unless some serious misapplications are perpetrated, with relevant radio regulations, such as EN300-220.

Within the last ten years the simpler end of the module market has been progressively eroded and replaced by the ever improving legion of 'single chip radio' devices, offered by a number of silicon vendors. These devices offer the non-RF specialist engineer a good but far from 100% certain chance, of implementing a workable, cost-efficient, wireless link without recourse to a module.

In most cases these parts provide inferior performance to a properly implemented 'discrete' design, especially in the receiver rejection parameters, as the on chip filters and oscillators cannot match the stop-band or phase noise performance of conventional circuits, but their performance does fall within the legal regulatory limits and, provided the link range is short and the RF environment is sufficiently kind, they do work, at least as well as the low end (super-regenerative or SAW resonator based) modules which they have supplanted.

Unfortunately, the happy status-quo I describe above is no longer quite so stable. Module designers have become lazy and chip suppliers have got greedy, and now there is a third kind of low power radio device creeping into the market: The 'chip pretending to be a module'.

These devices are presented in the familiar radio module formats, but consist internally of one of the major-vendor radio chips, and precious little else; usually just a frequency reference part and some decoupling. Sometimes these devices include their own CPU to control the radio chip, which results in a standalone module, with all the performance deficiencies of the parent silicon, but all too often they rely on the user to provide the, overly complex, data streams needed to set-up, configure and control the chip.

Such a device offers the worst of all possible worlds: poor 'radio on silicon' specifications; complicated, error prone interface requirements; and none of the price advantage or design flexibility of a single chip. In a few cases the offense is taken even further and an over-ambitious manufacturer attempts to produce a module for one of the higher power (500mW) sub-bands by cascading a 10mW output radio chip with an external power amplifier, invariably with insufficient additional filtering and, often, with a big dose of extra front-end gain, to upset the receiver's already inadequate large signal performance. This results in a design where the output spuri from the chip, barely regulation-compliant when used alone, are amplified by 20dB or more. Such 'designs' are rarely completely successful and in a few cases the regulatory authorities have forced the products to be withdrawn.

"MODULE DESIGNERS HAVE BECOME LAZY AND CHIP SUPPLIERS HAVE GOT GREEDY, AND NOW THERE IS A THIRD KIND OF LOW POWER RADIO DEVICE CREEPING INTO THE MARKET – THE 'CHIP PRETENDING TO BE A MODULE'"

The tone of my discourse has probably already revealed my feelings about this newer class of mongrel devices, but just in case, allow me to conclude:

- A properly designed module offers reliability, ease of use, rapid time to market, and superior RF performance.
- A single chip gives cost and size benefits, and keeps control of the radio design and production in-house.

A 'chip pretending to be a module' gives none of these benefits. Either source a good module, or do a good RF design (single chip or conventional circuitry, depending on the application).

But don't be tricked into paying module prices for 'on silicon' radio performance. ■

Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd
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A SMARTER GRID FOR A SMART FUTURE

Michael Anderson, Echelon's Senior Vice President for smart grids states that the UK electricity grid needs to get smarter

THE FACT THAT electricity suppliers in the UK rely on their customers to let them know when there is a power shortage, despite huge advancements in automation and communication technology, seems absurdly inefficient. This reactive approach illustrates how "not-so-smart" power grid that is in the UK. Based, as it is, on technology that was developed 100 years ago, the electricity grid is struggling to meet new stresses it was never designed to handle.

Increased energy demand, unpredictable generation from renewable sources, volatile energy costs, distributed generation, electric vehicles and environmental concerns are coming together to change the nature of the grid. Many utilities are looking to smart metering and smart grid solutions to help address these challenges.

It is important to note that simply installing smart meters in homes does not create a smart grid. A true smart grid is significantly broader than smart metering, which represents a single application within the smart grid. A true smart grid goes beyond billing and metering applications, and provides utilities with essential information about the health and status of the grid necessary to implement diverse and innovative services.

Last month Echelon unveiled the Echelon Control System (ECoS) – an open and secure application framework which enables intelligent distributed control at the edge of the smart grid network. The 'edge' describes the "last mile" of the grid where the distribution network connects to customers. Many of the devices (transformers for example) that are critically important in getting electricity from the source to the destination can be found here. Using ECoS, utilities can monitor and control the health and status of these devices, giving utilities unprecedented visibility at the edge of the grid. Anomalies such as voltage fluctuations, power quality and line signal strength can be quickly identified, presenting utilities with the potential to see where their next outage may strike and proactively take corrective action.

By way of analogy, ECoS is to the smart grid what Google's Android operating system is to smart phones. Android provides an open and secure software framework for smartphone apps. Likewise, ECoS provides an open and secure software framework for the development of smart grid applications.

ECoS will move the grid beyond the smart meter-only model of the centralised automated reading of meters to a truly open, intelligent and distributed system that can monitor and react to an increasingly dynamic and demanding environment.

However, technology alone will not solve all of the challenges faced by utilities. Consumers need to be better educated on energy consumption. Today's consumers are accustomed to having constant access to electricity. Imagine the outcry if people came home from work and could not turn on the heating, cook their dinner or watch television. Unfortunately, energy supplies are not endless and if supply and demand is not better managed, this could be the end result.

Using smart grid technology, consumers can actively monitor how much energy they use and make informed decisions regarding their energy usage – for example, you might choose to dim your lights or reduce the heating by a few degrees. Similarly, utilities can use this energy consumption data to control the flow of electricity and better manage peak energy loads.

If all the people living in a town, for example, came home at the same time and plugged in their electric cars, the chances are the grid would go down. Using smart grid technology, utility companies could stagger when each car receives electricity by a couple of seconds, thus avoiding an outage. This would be completely invisible to the end user and it would not affect the consumer's ability to use energy when they want to but it ensures the strength and reliability of the grid.

> "IF ALL THE PEOPLE LIVING IN A TOWN CAME HOME AT THE SAME TIME AND PLUGGED IN THEIR ELECTRIC CARS, THE CHANCES ARE THE GRID WOULD GO DOWN"

We only need to look at examples, such as Duke Energy in the US, that are already using smart grid technology to better control energy supply and demand. The electricity grid in the UK was designed over a hundred years ago and the architecture of the grid needs to be updated to account for the expected surge in demand. There needs to be a process and cultural change on behalf of end-users and utilities. This will not be an overnight change and it is going to take time, but it will lead to a better and brighter future for everyone. ■

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PEI-Genesis offers 48-hour assembly on ITT Micro-D connectors

Doug Mercer
Global Marketing Communications Manager
PEI GENESIS UK LTD

Connector-assembly specialist PEI-Genesis has expanded its portfolio of ITT Interconnect Solutions products to include the MDM series of microminiature D-type connectors and is now carrying large stocks ready for assembly within 48 hours.

Featuring a 1.27mm pitch between contacts, the MDM connectors offer a higher contact density than traditional rectangular connectors. They are ideal for harsh-environment applications where space is restricted, particularly in military, aviation and industrial systems.

ITT's D-subminiature connectors are available from PEI-Genesis in standard configurations from nine to 104 ways.

The gold-plated copper-alloy contacts have a high current rating of 3A, while the use of twist-pin contact technology ensures high reliability even when the connectors are subjected to extreme levels of vibration or rapid changes of temperature. Shells are made from aluminium and plated in either RoHS-compliant electroless nickel or yellow chromate over cadmium.

PEI-Genesis also stocks ITT's huge range of RoHS-compliant D-subminiature connectors, which are available with the same 48-hour assembly service in a vast array of different types to suit almost any requirement. They can be specified in standard configurations ranging from nine to 104 ways or with a combination of power and signal contacts to meet customers' specific requirements.

Manufactured to the highest quality standards to ensure optimum performance and reliability, the connectors are available with turned or stamped-and-formed contacts in a wide variety of termination styles, such as crimped, solder bucket, insulation displacement, wire-wrap and press-fit.

In addition to general-purpose commercial products, the ITT D-subminiature range includes filtered versions for applications requiring EMI/RFI protection, corrosion-resistant stainless-steel versions designed to withstand harsh environments, and high-spec hermetically sealed MIL-DTL-24308 connectors for use in military and aerospace systems.

PEI-Genesis is the world's fastest assembler of precision connectors. From the world's largest inventory of connector components, the company develops engineered solutions that support the military, industrial, medical, aerospace, transportation and energy sectors worldwide.

PEI-Genesis can build over 12 million unique connectors from stock at a rate of over 5000 per hour. Using proprietary automation for speed, consistency and quality, PEI-Genesis can build one piece or 10,000 pieces with equal ease; built to a standard or customised specification.

ITT's Micro-D connectors are ideal for harsh-environment applications where space is restricted.

As the world's largest distributor for ITT Interconnect Solutions, PEI-Genesis is the only partner that guarantees to build and ship connectors in 48 hours. No matter what the customer's requirement is, there is a good chance that PEI-Genesis will have the necessary parts in stock. There are no minimum order quantities, and the same 48-hour service applies to every order, whether it is for one connector or hundreds.

The company has recently carried out a major upgrade of its website and introduced a personalisation facility called MyPEI, which not only enables customers to shop online but also gives them access to a host of additional features.

Using the 'Part # Search' field at the top of every page, customers can view detailed technical information and product availability for a particular connector part number. Connector comparison charts are available to help customers select the right product for their application, and PEI-Genesis also has a specialist engineering team on hand to provide further advice if needed.

When logged into MyPEI, individuals can buy connectors online using either a credit card or their company's trade account. In addition, MyPEI enables customers to view orders, track shipments, see over ten years of purchase history, print or e-mail invoice copies, check contract pricing, request special quotations and even ask technical questions.

Headquartered in Philadelphia, PEI-Genesis has assembly facilities in Southampton, UK, and South Bend, Indiana, as well as 23 sales offices in eight countries.

More information can be found at www.peigenesis.co.uk.

PEI-Genesis – the partner that understands what you want, when you want it, and how you want it.

- PEI-Genesis can build over 12 million unique connectors from stock at a rate of over 5,000 per hour, assembled from our $60 million component inventory.
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- On average, we can assemble connectors in a little over a day. So whether you need it in 48 hours or 4 weeks, we'll have product there when you want it.
- As the world's largest Amphenol and ITT Cannon distributor, we can leverage our strong supplier relationships on your behalf.
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The CHALLENGE and opportunities of meeting future mobile broadband demand

Geoff Varrall, Executive Director at RTT, sheds some light on some of the challenges that are facing the mobile phone and electronics industries

The Samsung Tab – latest arrival in the tablet/slate market – is a revenue opportunity and network challenge for the mobile broadband operator community

IT IS PROVING hard to keep up with the present growth in demand for mobile data. Opinions vary as to the scale of the increase. According to Ericsson, data volumes as at the end of the second quarter of 2010 are running at 225,000 terabytes per month, which is equivalent to 2.7 exabytes per year. An exabyte is equivalent to one million terabytes.

Vendor estimates earlier this year suggested a dongle in a laptop or a laptop with embedded connectivity was generating about 2GB a month of data traffic, an iPhone about 165MB, a smart phone about 115MB per month and a standard phone about 30MB per month including voice.

By August a new set of numbers suggested things are changing very fast with smart phones and iPhones generating between 300 and 500MB per month. It is too early to tell what tablets and slates are likely to generate but probably somewhere between a laptop and a smart phone.

Applying these numbers to present device sales and sales trends produces a demand of at least 90 exabytes in 2015. This is a thirty-fold increase from the present level of data demand. Over the same period the income from this traffic will have increased by at most a factor of three. This is clearly a demand side opportunity with an associated cost and income problem that needs to be solved. This implies some interesting challenges and opportunities for the electronics industry.

Different Solutons

The issue is partly solved by improving radio access efficiency. Vendors are encouraging operators to invest in '4G' network hardware and software known as LTE (for Long Term Evolution). This delivers spectral efficiency benefits over and above present mobile broadband network technology of the order of three, which is impressive, but still short of the increase needed to redress the income/cost disparity.

An alternative is to reduce the cost of network hardware. Some network hardware costs scale with Moore's Law but some do not, RF hardware in the radio access network being one example. Although hardware cost reduction yields a reduction in capital cost investment, there are associated increases in through life software cost, an operational expense.

Operators and carriers can scale up their present spectral assets to accommodate the additional data volume. However, this amount of spectrum is unlikely to be made available, any spectrum made available will be expensive and, probably most important, present and planned user equipment lacks the band flexibility to access the spectrum effectively or efficiently. Unless an operator is bidding for spectrum for speculative gain, which is rightly discouraged by regulators, there is no point in buying bandwidth if it cannot be economically used.

> "PRESENT AND PLANNED USER EQUIPMENT LACKS THE BAND FLEXIBILITY TO ACCESS THE SPECTRUM EFFECTIVELY OR EFFICIENTLY"

Another approach is to increase network density. This has the effect of improving the link budget which increases capacity, improves data rates and reduces user power budgets up to the point at which the radio network becomes interference limited.

The problem with this from an operator EBITDA (Earnings Before Interest Tax and Depreciation of Assets) perspective is that capital and

operational costs increase, a composite of site acquisition, site rental, site energy cost, hardware and software investment and backhaul costs.

The industry has a number of other options. One is to use a much greater number of femtocells. These are the mini base stations that you can now buy from some operators. Using subscriber ADSL lines as backhaul via femtocells partly provide a solution to the back haul cost issue and can increase local area network density in a cost-effective way at the subscriber's expense. However femtocells address local area access economics not wide area or high mobility user access economics. Femtocells do not deliver wide area or high mobility user value.

Another alternative is to add extra antennas into user equipment to increase peak data rates. This is known as MIMO (Multiple Input Multiple Output). But, the problem with this is that there is not much space available in small form-factor user equipment. Additionally there is a requirement to support additional frequency bands, for example the new 700MHz bands in the US and 800MHz band in Europe made available from the switch from analogue to digital TV and a new band at 2.6GHz, which will soon be auctioned on a world wide basis.

These new bands not only complicate antenna design but introduce additional insertion loss and isolation loss in the multiple switch paths between the antennas and back end 'base band' processing functions. The loss of sensitivity and selectivity results in lower peak and average data rates but also increases DC power drain. The user's battery goes flat faster.

existing networks that typically use a mix of IP and traditional circuit switching. This applies to all forms of data including voice.

Fourth generation radio systems deliver high physical layer peak data rates by using higher order modulation (typically OFDM, nPSK or nQAM) and wider channel bandwidths. These improve bandwidth efficiency but require more linearity so are not inherently energy-efficient.

For these reasons, RF transmission efficiency will have a greater impact on user duty cycles (voice minutes and data megabytes per watt hour of battery capacity) and peak and average data throughput. This in turn affects the user experience and by implication operator profitability – the energy cost of connectivity.

Similarly, receiver front-end sensitivity, selectivity and stability determine downlink data rates. Poor sensitivity will increase baseband coding and error correction overheads, trigger high retry rates and compromise scheduling efficiency. This will further reduce the user duty cycle and absorb useful network bandwidth.

In recent years sensitivity has been considered as less important as connections are often made at medium power in interference limited conditions. However, applications such a rural broadband at 700 and 800MHz will increase the likelihood of a noise-limited channel.

User devices have to discriminate an OFDMA waveform across multiple frequency sub-carriers modulated with higher order modulation. As with the transmit path, these mechanisms achieve high peak data rates but are noise and distortion sensitive and not inherently power efficient.

"BATTERY ENERGY AND CAPACITY BY VOLUME AND WEIGHT ARE GENERALLY INCREASING AT AN ANNUAL RATE OF 10% TO 15%"

The Technical Side of It

The RF power budget in user equipment has been considered in recent years as less important than the power drain from baseband and application processor functions and touch-screen displays. The display on its own can be responsible for 40% of the energy consumed in the user's device. In dense networks built for capacity, phones transmitting voice or text are often transmitting at a fraction of their potential peak power output.

However, this is less true with data duty cycles and particularly not the case in LTE 700 or 800MHz deployments in larger cells in rural areas. Additionally in LTE, if voice is supported, the energy budget is an issue that also needs to be addressed. LTE voice avoids most of the packet overheads of pure IP voice by using Packet Header compression techniques. However, compression and decompression use fast memory, absorb processor bandwidth and introduce processing delay. Additionally the process of extracting a narrowband information stream, for example a 12kbps voice codec, from a broadband channel, for example 20MHz, is computationally complex and results in an energy drain that is higher than present GSM handsets. This is, or at least should be, in the 'things to be addressed' in box of most LTE design teams.

For many data exchanges, packets received on the downlink will be acknowledged on the uplink creating an additional load on the transmit chain. Always-on applications like push email, location-based services and social networking create signalling load which absorbs power, particularly in mobile smart phone devices.

IP networks were designed to be resilient rather than power efficient. As a wireless IP network, LTE has to deliver a user experience that is equal to or preferably better than that available from existing user equipment on

Alternatives such as higher capacity batteries offer only a partial answer. Battery energy and capacity by volume and weight are generally increasing at an annual rate of 10% to 15%. According to the Semiconductor Association, mobile system power requirements are increasing at an annual rate of 35 to 40%. The user data duty cycle therefore decreases over time, a disincentive to product replacement.

Innovations

It would be absurd to have engineered a new generation of mobile broadband device that needed to be tethered to a mains or 12V socket to meet user expectations. Even if batteries suddenly improved, RF device and system efficiency gains would be needed to avoid heat dissipation issues. Heat dissipation will, of course, also be a problem for portable devices connected to an external power supply.

The answer to all these problems is to deliver a step function improvement is user equipment efficiency.

Examples of new materials or mechanical structures being introduced into or considered for RF front-ends include gallium nitride for RF power amplifiers, silicon on sapphire for switch paths, digital capacitors and tuneable filter banks, barium strontium titanate for adaptive matching, ceramic substrates for antennas and RF MEMS for adaptive matching, filtering and tuning or as oscillators to replace the TCXO, the frequency reference at the heart of all RF devices.

These new materials when combined with new packaging techniques provide the basis for new families of RF components that potentially introduce band flexibility without cost or performance compromise. These components can be coupled to innovative antenna solutions that minimise additional space requirements.

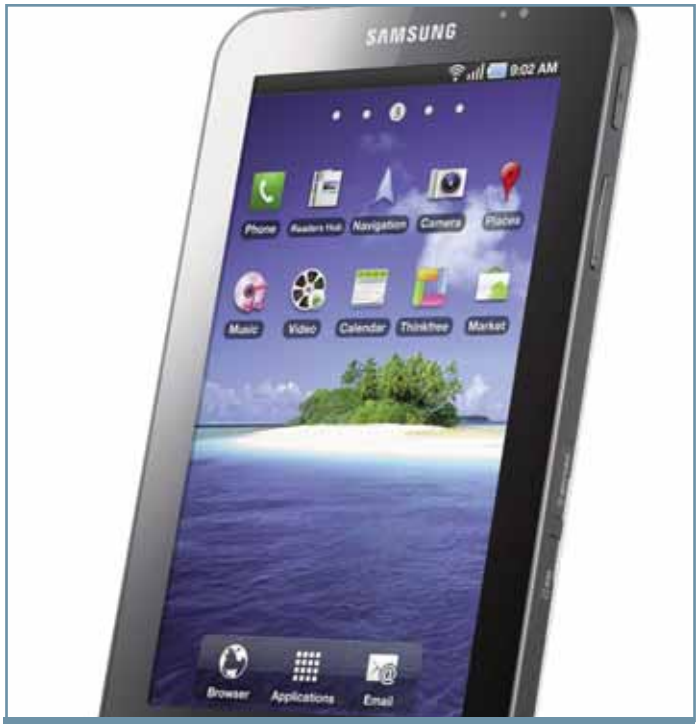
Any or all of these innovations are capable of delivering a performance gain. They can be made to be technically efficient. However, to be successful these devices also have to make commercial sense for RF component and baseband component and algorithmic vendors, user equipment manufacturers, infrastructure vendors, network operators and users. In other words, the devices have to be commercially efficient.

Avoiding Regulatory Pitfalls

Inherent technical and commercial inefficiencies have been introduced as a consequence of well intentioned but misguided regulatory policies that have resulted in a multiplicity of band plans that are hard to support in the front end of a user's device. The 'front end' is an industry term to describe the signal paths in and out of a user's device including the antenna, filters, oscillators, mixers and amplifiers, a complex mix of active and passive components that are not always easily integrated. The physicality of these devices often means they do not scale as efficiently as baseband devices. It should be remembered that any radio wave is analogue as are many of the front end functions.

These inefficiencies need to be resolved to ensure the long term economic success of the mobile broadband transition. The band allocations cannot easily be changed or harmonized so technology solutions are needed.

A technical challenge should translate into a commercial opportunity. A commercial challenge should translate into a technical opportunity. Mobile broadband appears to meet both criteria. ■



The Samsung Tab – latest arrival in the tablet/slate market – is a revenue opportunity and network challenge for the mobile broadband operator community

TEST AND MEASUREMENT SYSTEM GROUNDING

DAVE MATHEW FROM AUDIO PRECISION (AP) TAKES A QUICK LOOK AT THE ISSUE OF EARTHING IN TEST AND MEASUREMENT SET-UPS, INCLUDING BOTH ANALYSERS AND DEVICES UNDER TEST, AND SUGGESTS SOME OPTIMAL CONFIGURATIONS AND MEANS OF PROVIDING ADDITIONAL GROUNDING WHERE REQUIRED

WHEN INTEGRATING instruments, accessories and DUTs (devices under test) into a test and measurement system, observing good grounding practice is always important in achieving optimal measurement results. Small ground potential differences between devices in the test system (such as switchers, accessories, the DUT and the test instrument) can couple into the signal path and cause undesirable interference or noise due to the inherent stray capacitance between signal conductors and the chassis (see the '*What Is A Ground Loop*' box).

To prevent this problem, best practice suggests that the chassis ground of each device should be directly connected to the ground of the test instrument via wires having as low an impedance as possible. This technique is often referred to as 'ground bonding' or 'chassis bonding'.

Star & Bus Grounding – or a Combination?

The most effective grounding arrangement for multiple devices is 'star grounding', where each device in the system is connected to the measurement instrument ground via a separate grounding wire (see **Figure 1**). However, this can make for a series of complicated grounding connections, depending on the complexity of the test and measurement rig.

Bus grounding, where several devices are serially connected to a low-impedance conductor called a ground bus (see **Figure 2**) is not recommended, as it's not as effective as star grounding; the resistance in each leg of the chain puts the devices at different ground potentials.

By keeping serial links very short, a combination star/bus grounding configuration (see **Figure 3**) can simplify connections, while still providing good grounding performance – a decent compromise. Some companies, including audio analyser manufacturer Audio Precision, provide the parts required to create star or combination star/bus connections to several devices, including grounding cables designed to connect test switchers to an analyser.

Alternatively, you can make your own ground cables. These must be very low-impedance, heavy gauge copper wire, as short as possible for the application and terminated with large surface area low-impedance spade lugs. If the lugs are a crimp type, a proper crimping tool should be used to ensure a secure, gas-tight connection. One end of the lug should be fastened to the test switcher with a large, truss head screw and the other should be attached to one of the ground posts on the front of the test and measurement analyser.

Other Grounding Techniques

Some older switchers do not have a place for a grounding screw on the chassis; however, such units are commonly grounded through the power line, which is usually sufficient. If the switchers are rack-mounted, additional grounding may be provided through the rack. The entire ground path should be made continuous by removing paint under the rack screws and rack ears as needed – the larger the contact surface, the better.

If a good rack ground is not available and additional grounding is needed, a hole may be added on the side of the switcher to add a grounding screw. Before doing this however, the loose end of a ground cable should be held against the chassis and the noise measured. Sometimes having multiple grounds can cause ground loops that make noise worse instead of better! ■

Dave Mathew is Senior Technical Writer at Audio Precision

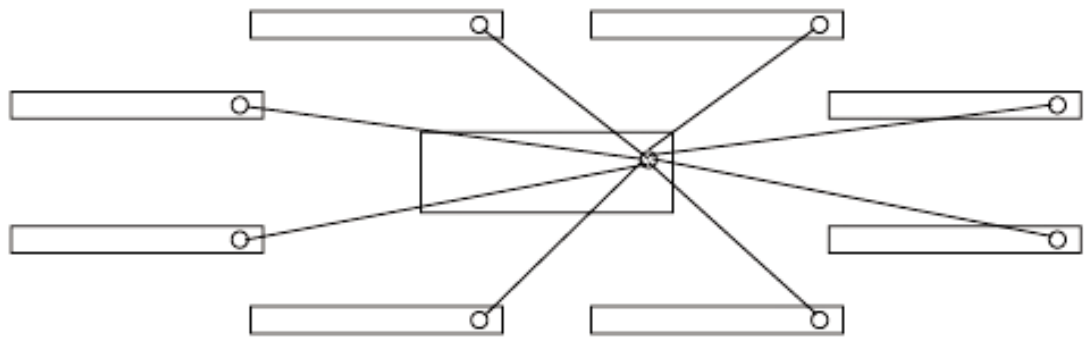


Figure 1: *'Star grounding' type arrangement*

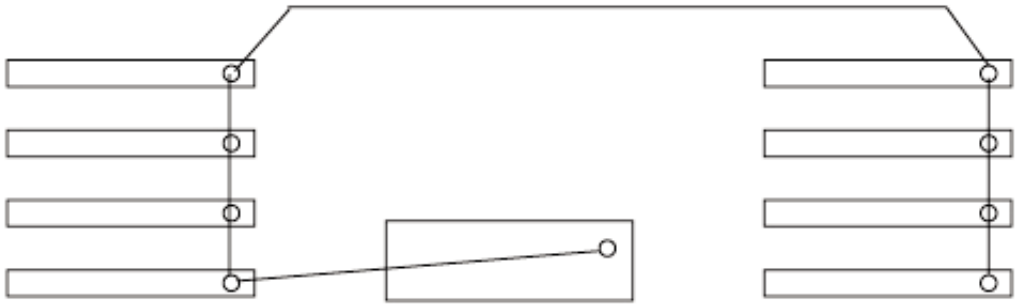


Figure 2: *Serial type grounding*

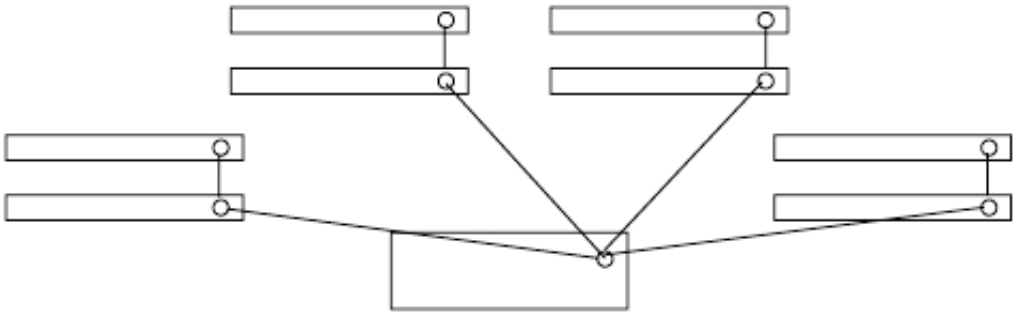


Figure 3: *Combination star/bus grounding configuration*

WHAT IS A GROUND LOOP?

A ground loop is an inadvertent electrical circuit formed whenever there is more than one path from the signal ground of a device to the local ground reference.

Here's what happens. Noise, hum and crosstalk currents, either electrostatically or magnetically induced, will flow in this accidental circuit, the ground loop. The loop current flows through the resistance of the ground connections of the device, appearing as a noise voltage at the device's signal ground.

Since the signal is defined as the voltage in the signal line in reference to the signal ground, the noise becomes a component of the signal. Hum, buzz, or radio stations are now part of your signal. Unfortunately, ground loops are very easily formed. In most systems, the signal ground is carried from device to device by interconnection cables. Additional ground paths are commonly created by a common rack connection, or by electrical safety grounds. It's hard to avoid.

The solution is to break the loop, without compromising safety (never cut a safety ground or use a 'ground lift' adapter on a mains cord!). Can the equipment be rack-mounted while keeping the chassis electrically isolated from the rack? Can isolating transformers or optical connections be used with your signal? Do the devices support balanced signal connections, where the signal ground can be maintained independent of safety and cable shield ground?

In a permanent installation, ground loops are best dealt with by careful design before installation. Only star grounding, as described in this article, provides a grounding system that entirely eliminates ground loops, but it may be difficult to implement later in the process. Many recording studios, for example, avoid ground loop problems by using variances in the jurisdictional electrical code that allow the safety ground to be configured in a star ground network and connected to a central high-quality technical ground.

The White Cathode Follower CF

Burkhard Vogel presents a series of short features with general remarks on triodes in audio applications

MR WHITE'S INVENTION shows a cathode follower with a gain < 1 and a very low output resistance. Typical values are 2Ω < R_o < 200Ω. The price to pay is a double-triode or two different triodes driven by the same anode current and careful handling of the maximum V1 input level. The maximum peak signal level at the anode of V1 (= level at the grid of V2) should not exceed the DC bias level of the V2 grid. Otherwise, a V2 cut off would happen. The typical circuit and its equivalent are shown in **Figure 1** and **2**.

The equivalent circuit does not mirror Figure 1 exactly. Three adaptations have to be taken into account: R_{a1} = R3||R4, R_{g1} = R1||R2 and R_{c2} = R5. In conjunction with a high anode current the inclusion of the cathode capacitor C2 pushes R_o to the low side of the above given range. C1 and C2 must be of a size that does not hurt a flat frequency and phase response in B_{20k}.

Although it's a nightmare deriving the gain equations for the WCF case with two different triodes V1 and V2, I will present the un-bypassed version's extensive gain equation as function of R_L. It will be the main derivation basis for all other important small signal equations.

$$G_u(R_L)=\frac{v_o}{v_i}=\frac{\mu_1\left[r_{a1}r_{a2}^3+r_{a2}^3R_{a1}+(\mu_2-1)r_{a1}r_{a2}^2R_{a1}+K\right]}{M+N+O+P+\frac{r_{a1}r_{a2}^2(r_{a1}+R_{a1})\left[r_{a2}+(1+\mu_2)R_{c2}\right]}{R_L}} \quad (1)$$

$$K=R_{c2}r_{a2}(1+\mu_2)(r_{a1}r_{a2}+R_{a1}(r_{a2}-r_{a1}))$$
$$M=(1+\mu_1)r_{a2}\left[r_{a2}^2(r_{a1}+R_{a1})-R_{c2}(R_{a1}(r_{a1}-r_{a2})-r_{a1}r_{a2})\right]+r_{a1}r_{a2}^2(r_{a1}+\mu_1R_{a1})$$
$$N=\mu_2\left[r_{a2}R_{a1}(r_{a1}^2+R_{a1}(r_{a1}-r_{a2})+R_{c2}\left[r_{a1}r_{a2}^2+R_{a1}(r_{a1}-r_{a2})(r_{a1}-r_{a2}+R_{a1})\right])\right]$$
$$O=\mu_1\mu_2r_{a2}\left[r_{a1}r_{a2}R_{a1}+R_{c2}(r_{a1}r_{a2}+R_{a1}(r_{a2}-r_{a1}))\right] \quad (1)$$
$$P=R_{c2}\mu_2^2R_{a1}(r_{a1}+R_{a1})(r_{a1}-r_{a2})$$

The respective equation for the un-bypassed output resistance $R_{o.u}$ becomes thus:

$$R_{o.u}=\frac{r_{a1}r_{a2}^2(r_{a1}+R_{a1})(r_{a2}+(1+\mu_2)R_{c2})}{M+N+O+P} \quad (2)$$

Setting R_{c2} = 0Ω leads to the bypassed version's gain $G_b(R_L)$ with output resistance $R_{o.b}$. However, with a double-triode the gain and output resistance equations become less complex. We set $r_a = r_{a1} = r_{a2}$ and $\mu = \mu_1 = \mu_2$ in the above given equations. This will lead to the un-bypassed and bypassed G and R_o equations:

Figure 1: *WCF circuit*

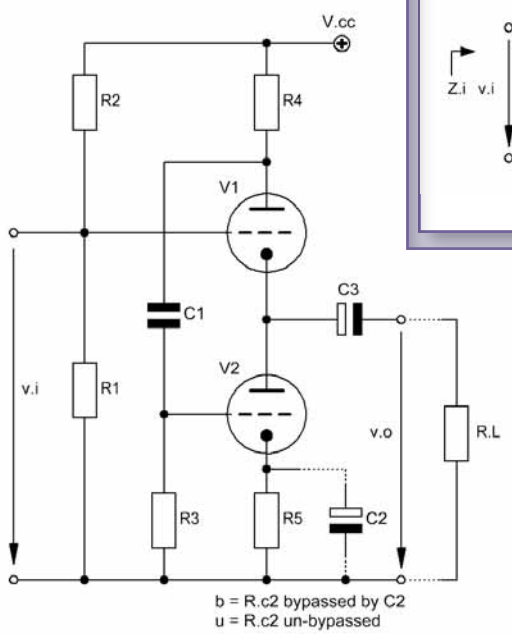


Figure 2: *Equivalent circuit of Figure 1*

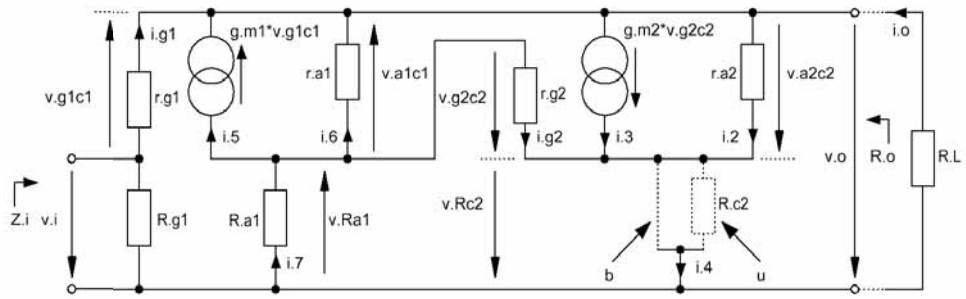
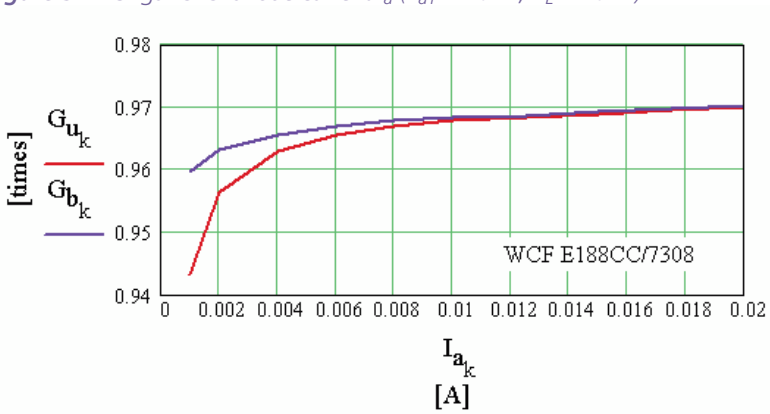


Figure 3: *WCF gains vs. anode current I_a (R_{a1} = 10kΩ, R_L = 10kΩ)*



$$G_u(R_L)=\frac{\mu\left[r_a+\mu R_{a1}+(1+\mu)R_{c2}\right]}{(2+\mu)r_a+(1+\mu+\mu^2)R_{a1}+(1+2\mu+\mu^2)R_{c2}+\frac{(r_a+R_{a1})\left[r_a+(1+\mu)R_{c2}\right]}{R_L}} \quad (3)$$

$$G_b(R_L)=\frac{\mu(r_a+\mu R_{a1})}{(2+\mu)r_a+(1+\mu+\mu^2)R_{a1}+\frac{r_a(r_a+R_{a1})}{R_L}} \quad (4)$$

$$R_{o.u}=\frac{(r_a+R_{a1})\left[r_a+(1+\mu)R_{c2}\right]}{(2+\mu)r_a+(1+\mu+\mu^2)R_{a1}+(1+2\mu+\mu^2)R_{c2}} \quad (5)$$

$$R_{o.b}=\frac{r_a(r_a+R_{a1})}{(2+\mu)r_a+(1+\mu+\mu^2)R_{a1}} \quad (6)$$

A rule of thumb for C_i allows calculating the input impedance Z_i:

$$Z_i(f)=\left|R_{g1}\|C_i\right| \quad (7)$$

$$C_i\cong C_{ga1}+C_{stray1}$$

The graphs show the most relevant traces of the example double-triode E188CC/7308 at a constant $V_{a1} = V_{a2} = 90V$ and R1, R2 adequately chosen ("$_k$" indicates the number of the ten I_a values from 1mA to 20mA).

Because of the very low V1 gain (<< 1), there is practically no i/p capacitance increasing Miller effect. In addition, we can ignore the tiny fraction (<< 1) of the V1 grid-cathode capacitance C_{gc1}. Thus, the input impedance Z_i becomes R_{g1} = R1||R2 in B_{20k}.

Coming in the next issue is *Part 8: 'The Common Cathode Stage with Active Load CCA'*

If you missed any of the previous parts, you can order them online by going to Electronics World's website at www.electronicsworld.co.uk

Figure 6: *WCF output resistances vs. anode current I_a (R_{a1} = 10kΩ)*

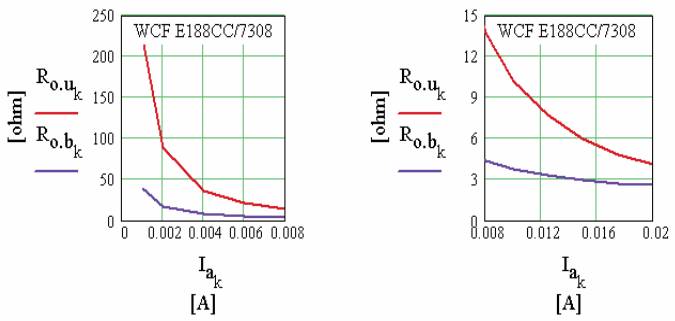


Figure 4: *WCF gains vs. output load R_L (I_a = 10mA, R_{a1} = 10kΩ)*

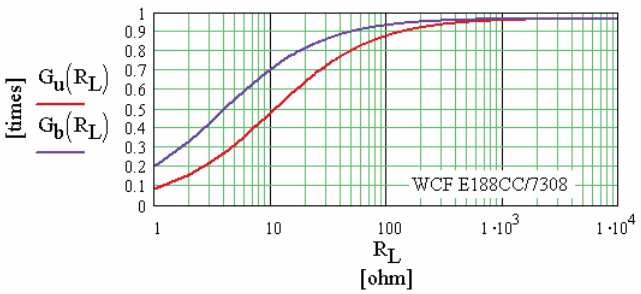


Figure 7: *WCF output resistances vs. V1 anode load R_{a1} (I_a = 10mA)*

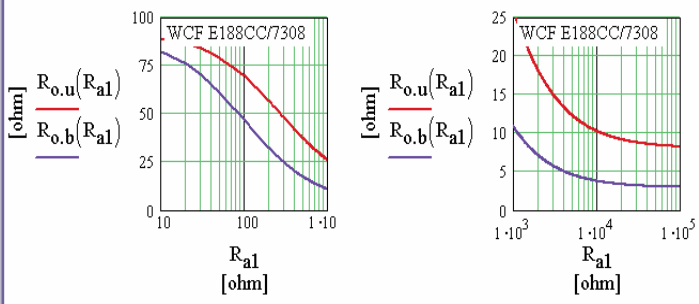


Figure 5: *WCF gains vs. V1 anode load R_{a1} (I_a = 10mA, R_L = 1kΩ)*

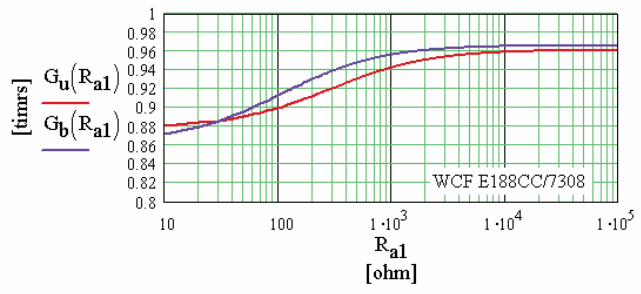
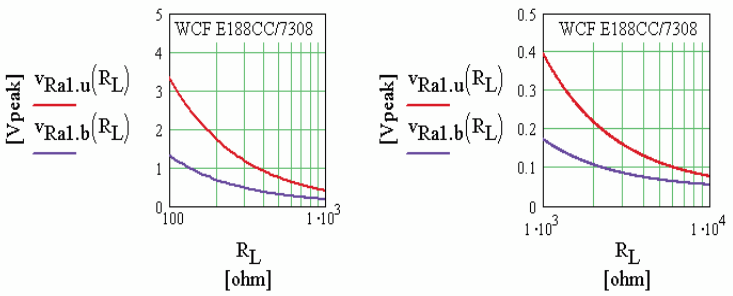


Figure 8: *WCF V1 signal level v_{Ra1} at anode load R_{a1} and at the grid of V2 vs. output load R_L (R_{a1} = 10kΩ, i/p level = 1V_{rms})*



Accelerating the design cycle and reducing unknowns in new PRODUCT DEVELOPMENT

Jas Gohlar, Electronics Development Manager at Farnell looks at how and why reference designs, development boards and evaluation kits have grown in importance and relevance to a fast moving and consumer demand driven marketplace

THE NUMBER AND variety of development boards, evaluation kits and reference designs offered by electronic component manufacturers has expanded considerably in recent years. With electronics technology advancing so quickly and the demand to get new products to market more rapidly, they are a welcome addition to the pressured electronic product designer's resources.

This article looks at exactly how and why reference designs, development boards and evaluation kits have grown in importance and relevance to a fast moving and consumer-demand driven marketplace.

In broad terms, reference designs, development boards and evaluation kits help shorten time-to-market and allow an approach to design that uses proven 'building blocks' to simplify the task of circuit design and reduce the risk of the need for time-consuming and expensive multiple prototype stages during the design process.

The Evolution of Reference Designs

The first form of reference design saw device manufacturers making suggestions for circuit layouts on either 'breadboard' (a solderless plugboard) or veroboard (also known as stripboard). Both of these approaches allowed experimentation with circuit design and the creation of functional, if often cumbersome, prototypes. They certainly provided the electronics design engineer with more help than just a tube of ICs and a datasheet.

Recognising the benefits to both their customers and to themselves has resulted in a remarkable evolution and proliferation in reference designs, evaluation kits and development boards offered by device manufacturers. Circuit designers can now source chipsets and even complete, fully integrated 'plug and play' modules to drop into their circuits to perform a given function.

The huge growth in the importance and prominence of the Internet has also supported the adoption of reference designs, development boards and evaluation kits as a standard approach in new product design. The online availability of a host of resources, such as application notes and development software downloads, and more recently the emergence of audio and video training modules, can all help speed and ease new product development. Third party forums and 'e-communities' that provide independent user experiences, endorsements and advice are also of great value.

Impact on the Equipment OEM

In an increasingly competitive and fast moving market, particularly in the consumer electronics sector, the ability to get a product from initial concept to a revenue generating, saleable product in the shortest possible time is key. Using the tools and kits described can support this objective by allowing the engineer to source proven blocks of core functionality. This may overcome the need for time and cost-consuming prototype stages, and avoid design cycle bottlenecks. The product designer can then spend more time developing and optimising parts of the circuit design that are not encompassed by reference designs, development boards and evaluation kits. These may be aspects of circuitry or electronics that are peculiar to their particular market; for example, sensing and measurement circuitry.

In most situations the degree of electronic engineering skill required to develop a product when utilising various development tools can be less than if a circuit were developed in-house starting from a blank canvas. Reference designs usually deal with tasks such as the selection of passive components to support the correct operation of the integrated circuit.

ST Microelectronics's STM32 Discovery Kit is a good example of the hardware development platforms available today

The Amicus18 board consists of an 8-bit Microchip PIC microcontroller with complementary components to facilitate programming and incorporation into other circuits

Micorchip's grid connected solar micro inverter reference design helps engineers challenged with developing reliable and efficient soar designs

They can also address especially challenging problems including parasitic and grounding in high frequency circuits or thermal management and ESD/EMC protection.

The need for either fewer or less technically qualified engineers on a project can give important cost savings for the equipment OEM that may ultimately lead to a more competitively priced end product.

The only possible negative aspect of development tools is that they may, in some instances, impact the 'uniqueness' of new products. As many companies use the same plug-and-play modules or an identical approach rather than starting from a blank PCB, there can be a reduced opportunity to differentiate one product from another. However, this is not to be seen as a major concern as there are normally so many aspects to a design such that there are still many opportunities to create unique selling points.

The Component Manufacturer's Perspective

As well as helping to simplify, speed and reduce the cost of the development process for its customers, offering development kits evaluation boards or reference designs also has important benefits for the manufacturer of the device or component in question. By making it simpler to incorporate in an end product, potential customers are much more likely to use a particular device.

Component manufacturers often offer development tools and software either free-of-charge or at heavily subsidised rates; this is because they recognise that 'locking' customers in at the earliest possible stage of a product development can have important benefits to long-term business.

Much of the work required to produce development and evaluation tools will have already been done during the original development of a device. Offering such tools can therefore be viewed as a way of sharing existing knowledge and know-how. With strong competition and often more than one device available on the market to perform a given task, component manufacturers need to offer tools that make theirs the easiest to implement in a design.

Utilising Distribution Channels

Ease of access to evaluation and development tools is also important. This means that component OEMs must not only offer access to tools on their own website, but also via nominated distribution channels. This is especially important as distributors are very often the source of supply for prototype and small pre-production batch quantities of parts. Offering reference designs, development boards and evaluation kits in the same place is therefore logical.

Distributors like Farnell have recognised the importance and connection between offering small quantities of parts and development tools that help product designers achieve a shorter design cycle with fewer unknowns and prototype stages. A current range of over 2,000 evaluation boards plus software tools, demo boards, debuggers and emulators backed by data sheets, user manuals/guides and other collateral underlines this and can give the designer a one-stop location during product development before switching to the component manufacturer when significant volume manufacturing begins.

Technical discussion forums and e-communities complement the benefits of development tools by linking designers with similar challenges in order to share challenges encountered, experiences and solutions with one another. The online discussions between engineers on sites such as element14 add another dimension to working with reference designs, development boards and evaluation kits and can support even more efficient working practices with a resultant shortened, lower cost design cycle.

Accelerating Design

Tools, kits and software to accelerate and ease device inclusion into end products give undoubted benefits and lower the risk of a need for expensive, unexpected additional prototype stages. Device manufacturers recognise this and are constantly working to enhance their offering in this area with the aim of securing design wins at an early stage.

Distribution channels provide an important source for not only low volume parts for R&D but also development products and an arena for discussion between engineers faced with similar challenges. The equipment designer at the end of the supply chain is the real winner as all of these efforts culminate in providing tools and information to make their job easier. ■

APIX industrial – the easy way to connect remote DISPLAYS

Martin Danzer, Product Manager at congatec AG discusses the Automotive Pixel Link (APIX) technology has the right solution for long distance communication between a processing unit and display interface

WHEREVER LONG distances between the processing unit and display interface are necessary, the Automotive Pixel Link (APIX) technology is the right solution. The APIX transfer process enables the use of standard Ethernet cables and makes it possible to simultaneously transmit video data and bi-directional control data as well as the power supply for the control or display units used.

A robust technology which yields good value for money, APIX was originally developed by Inova Semiconductors to meet the specific requirements of the automotive industry. However, the technology is also ideally suited for use in a wide range of other applications such as industrial automation solutions, medical technology, gaming machines, weighing scales or in the fast growing digital signage market.

APIX combines high-speed digital video transfer with full duplex and two-wire data communication, and can support the supply of remote displays over the same cable. When applied to industrial applications, APIX technology offers the benefit of a standardized connection for remote displays over single twisted-pair cables, without sacrificing the flexibility necessary to meet the application-specific requirements for the communication between graphics unit and display.

Human-machine interfaces such as buttons or control sticks, combined with small information panels, are replaced or supplemented by small displays capable of presenting high resolution images and acting as user interfaces. Especially in embedded applications, where PC functionality is available in form of small-sized and low-power modules based on Intel Atom processors, control units can easily take care of the content delivered by the digital user interface.

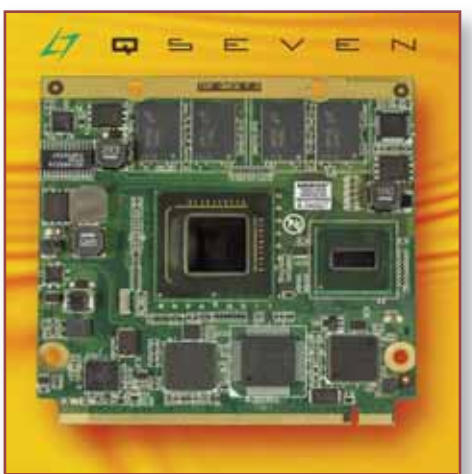


Figure 1: *The conga-QA is a compact PC module, which is based on the Intel Atom processor and allows for easy integration*

Industrial Remote Displays

In industrial automation applications it is common for the user interface and the control PC to be some distance apart. Industrial long distance applications, therefore, often require expensive special cabling or use multiple PCs, connected via Ethernet, for each panel. There is an obvious need for a low-cost, robust, high-speed, full duplex link which meets the requirements of the industrial environment for electromagnetic interference (EMI) and distance.

With the introduction of Apple's iPhone and the increasing availability of smaller displays with ever higher resolutions, the demand for intuitive user interfaces using touch screen displays has been gaining great interest in the markets.

The specific requirements of remote displays in industrial applications are defined by a combination of functional, mechanical and economical aspects. Typical LCD displays offer a digital RGB interface, which is linked to the graphics controller via a flexible flat cable, carrying 18 or 24-bit video signals, synchronous to a specific pixel clock. For EMI reasons, the distance of these parallel data interfaces needs to be kept as short as possible and they can only be used inside closed and shielded devices.

In order to extend the installation of remote displays to several meters, the display link needs to be able to carry the video signal over a long distance, ideally without reducing the quality of the video information. For economic reasons – and to keep the complexity of the display low without losing picture quality – the link needs to be fast enough to transport the information without compression. In industrial environments, the link also needs to be able to meet the requirements of electromagnetic immunity and emissions. In summary, the display link needs to address the following requirements:

- High speed, uncompressed video link for high resolution displays.
- Full-duplex, robust data communication to the main unit.
- Possibility of "extended" user interfaces.
- Minimized cabling effort.
- Flexible, thin cables.
- Possibility of power supply over the same cable.
- Standard cables and connectors.

APIX Automotive

As mentioned earlier, APIX technology was originally conceived to meet the requirements of display and camera links in the automotive environment. Optimized for low EMI, the APIX

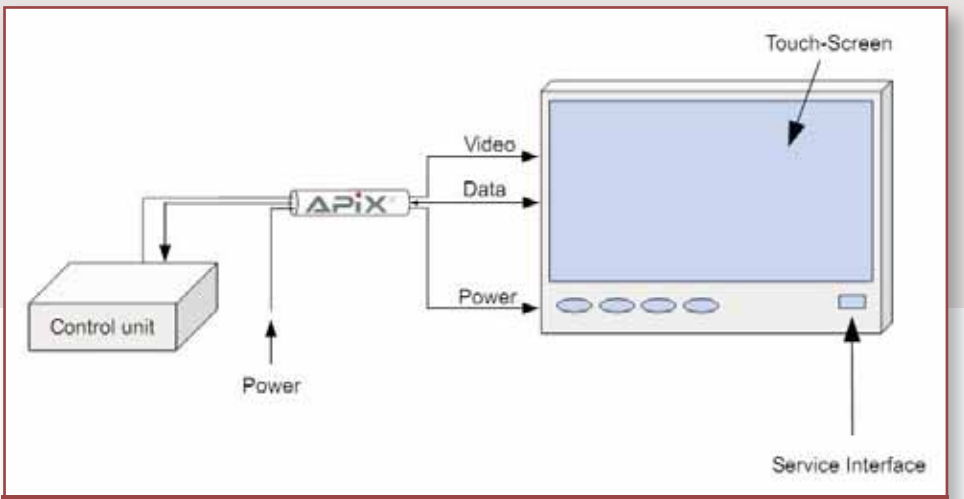


Figure 2: *Remote display connected via a single cable using APIX technology*

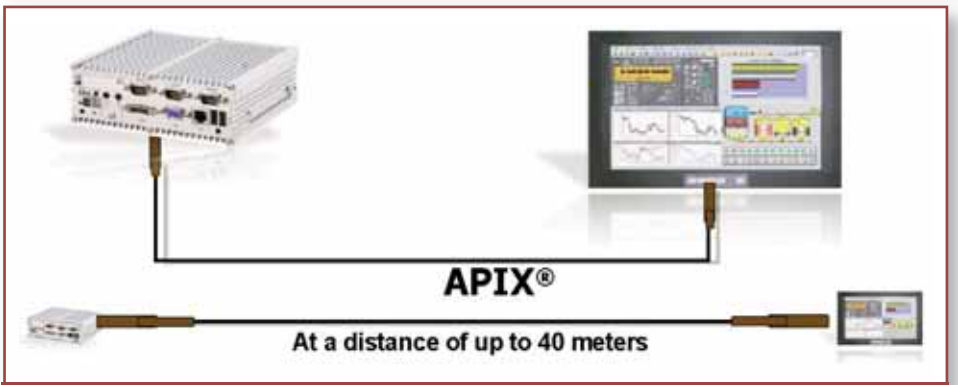


Figure 3: *APIX in automation*

link is ideal for point-to-point display and camera applications using differential Current Mode Logic (CML) technology.

The APIX transmitters and receivers meet the specifications of the stress test qualification AEC-Q100 of the Automotive Electronics Council (AEC), ensuring high product reliability and conforming to the high requirements for electromagnetic emissions and immunity for automotive products. A key requirement which must be met is electromagnetic interference (EMI), as it can have a severe impact on the overall system. EMI includes immunity as well as emissions, which both need to be optimized if an acceptable performance is to be achieved.

APIX CML signalling together with the optimized line code ensures a stable transmission, providing high immunity against external influences at lowest emissions, meeting the high requirements of the automotive market.

With a bandwidth of 1GBit/s, the APIX link supports video resolutions of 800 x 600 and 18-bit colour depth (262,144 colours). The high-speed downstream channel acts as a transparent gateway for the parallel video interface. The data sampled at the graphics processor interface is provided at the same clock at the display. Video data are transmitted in real-time and without compression, minimizing the latency for time critical applications and eliminating the need of decompression at the display. The video interface supports any parallel data format like RGB or YUV, with four different bit widths of 10, 12, 18 or 24 bit. In addition to the pixel data interfaces, three pixel control signals are implemented on the video interface.

The APIX architecture also offers so-called sideband data channels which provide full-duplex downstream and upstream capabilities. For the discrete devices INAP125T and INAP125R, the sideband data are sampled at dedicated pins at either transmitter or receiver and are transparently provided at the respective remote side pin. Since the devices do not require any special formatting, this transparent sampling allows flexible 'extension' of interfaces like UART or SPI over a long distance.

Due to the fact that transmitter and receiver are driven by local reference crystals from which the high speed differential link is derived, the differential link is independent from the video pixel clock. This makes it possible to transmit sideband data even when no pixel clock is available. The ability to carry full-duplex information without pixel interface constitutes a significant advantage for point-to-point applications. Since the sideband data channel is available as soon as the link is powered up, it can be used as the main configuration interface of the camera or display implementation. Even when no video data is available, it is possible to configure and synchronize a remote display or camera.

Since the downstream and upstream data communication is transmitted over the high-speed differential serial lines, it offers the same distance and EMI performance as the video link.

In summary, the digital automotive pixel link is a proven technology for video data transmission which has been developed for in-vehicle applications. Key advantages include:

- Reliability
- EMI Protection
- Low Cost
- Single Low Cost Cable
- Data (Display + AUX)
- Power
- Suitability for other industry applications (e.g. automation, digital signage, gaming).

Cable Considerations

An APIX link requires a maximum of two pairs of shielded twisted wires, transporting the "downstream" video and data stream at one pair, the "upstream" at the other pair.

Due to AC-coupling of the APIX physical layer, the data lines can also be used for

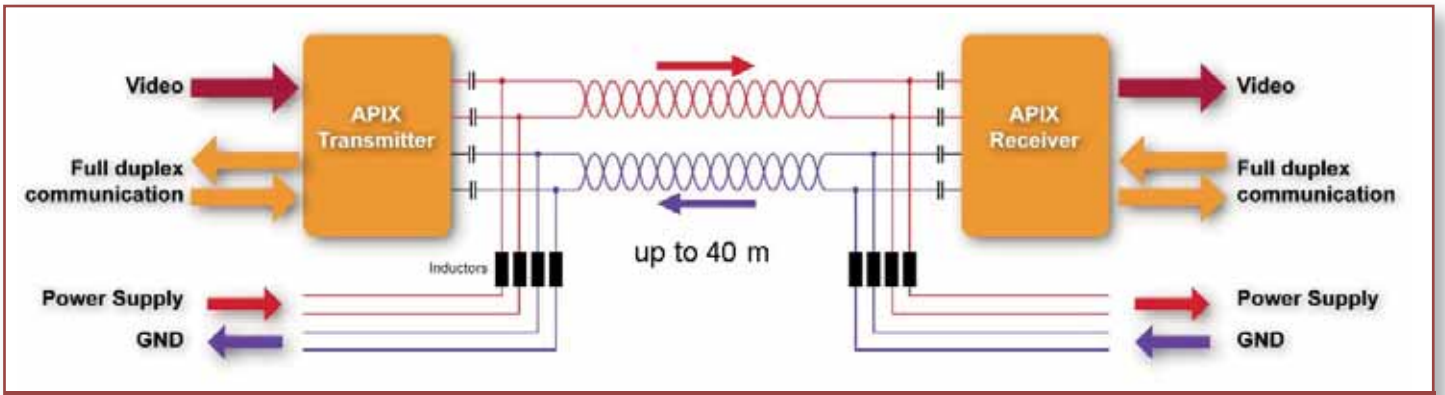


Figure 4: *Power over APIX*

supplying a remote system. The power supply is realized by using either one or both existing wire pairs, with inductors acting as low pass filters to the signal lines. Since typically two pairs of wires are used, it is recommended to use the high speed downstream line for power and the other one for ground.

This way, a display can be supplied with video, data communication and power in a single cable over two pairs of wires.

The APIX link, as any other differential technology, requires a twisted pair cable to ensure that "positive" and "negative" current of the differential signal negate as optimally as possible. The better the continuous cable impedance of 100 Ohm and the more even the twisting the greater the maximum possible cable distance.

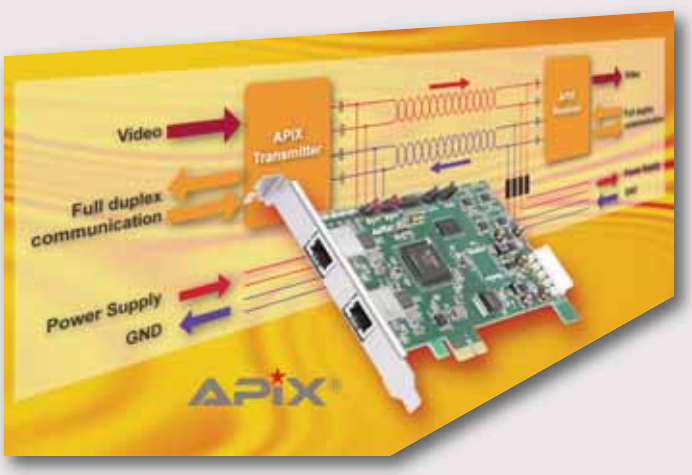
In order to fulfill the EMI requirements, it is recommended to use shielded twisted pair cables, which are slightly thicker and somewhat less flexible than unshielded cables. The standard Ethernet cable CAT5, which is available as shielded or unshielded version, offers four differential pairs of wires, enabling the transmission of APIX downstream and upstream. The remaining two pairs are available for any signalling, such as power supply, or another data bus, which offers high flexibility for different scenarios.

CAT5 cables are available from many vendors at relatively low cost and with small cable diameters. However, the quality of CAT5 cables from different vendors may vary, which can cause unreliable results for the maximum transmission length. If distances above 15 meters need to be spanned, it is therefore recommended to test the desired cables and vendors.

APIX INDUSTRIAL STARTER KIT

In order to enable quick and easy evaluation of the APIX Display Interface congatec created the complete APIX Design Kit.

The kit gives users the opportunity to quickly and easily evaluate the APIX display link interface. As well as all the necessary hardware, the kit contains comprehensive documentation, including all the required circuit diagrams, to allow the implementation of customer specific solutions to be designed as easily as possible. congatec has developed this turnkey APIX Design Kit together with Inova Semiconductors and Fujitsu Microelectronics Europe (FME) in order to make access to this innovative technology easier for users.



The APIX Design Kit consists of a PCI Express add-on card, including the appropriate operating system drivers and a remote display unit with integrated touch screen. The image data, the coordinates from the touch screen and the power supply are all transmitted using a standard Ethernet cable with RJ45 connectors. If high quality cables are used, distances of up to 40 metres or more can be covered.

The PCI Express x1 add-on card has two APIX ports. This expansion card reads directly from the video memory and sends the data to the APIX channels at a current maximum resolution of 800 x 600 pixels. Up to four of these cards can be used per system, creating a maximum of eight APIX channels. The sideband signal data, i.e. the return channel in an APIX solution, is also received by the PCI Express card and made available to the computer. PoA (Power over APIX) is used to supply power to the remote control units and allows a maximum current of 2A with a 12V supply voltage.

PCI Express add-on card features:

- PCI Express X1 slot
- Flexible FPGA design
- DMA readout of video memory
- Two channels for independent video channels
- Up to four cards per system
- Configurable PoA
- Option for Rosenberger HSD connector

congatec Starter Kit features:

- PCI Express APIX transmitter card
- APIX receiver based on Fujitsu "Indigo" chip
- TFT panel with touch screen
- Complete documentation including schematics
- Platform for rapid prototypes
- Kick start for engineering

For extended distances, it is possible to use cables that are specially optimized for differential signalling of two pairs. Good examples are star-quad topology cables, offering high crosstalk attenuation at a very compact cable diameter. Due to the high quality requirements, the cost of those cables may be higher than standard CAT5 cables.

Connector Selection

The selection of connectors and plugs is as important as the choice of cable in terms of EMI and impedance. One of the most common connectors for Ethernet applications is the RJ45 connector, which is used with CAT5 cables and is available as plastic version or surrounded by a metal case for better EMI shielding. RJ45 connectors are specified with high contact durability, which allows many different and flexible installations.

Alternatively, a more rugged but more expensive connector can be used. The Rosenberger HSD connector (High Speed Data Systems) is widely used for automotive applications. The HSD concept is optimized for high robustness in terms of connector/plug stability. The connectors are delivered already assembled with the cable to guarantee maximum signal quality. The HSD connectors are used with star-quad cables, carrying the downstream and upstream of the APIX link while still allowing to transmit power supply over the same cable.

APIX Configuration

The APIX link offers several configuration options to support different application scenarios in terms of bit width, bandwidth requirements and upstream capabilities.

PARAMETER	CONFIGURATION
Downstream Clock	1000MHz
Pixel Data Width	18 bit
Sampling Edge	Rising
Pixel Control Transmission	Even pixels
Upstream Channel	Dedicated
Upstream Clock	62.5MHz

Table 1: *APIX configuration options*

The standard configuration provides support for 18-bit displays and a maximum resolution of 800 x 600.

Outlook

The rapid trend towards smaller display sizes and ever higher resolutions also calls for faster digital display links. Resolutions of 1280 x 1024 or higher require link speeds of 3GBit/s and beyond. In order to fulfill the requirements of these high resolution displays, the APIX technology is currently being "enhanced" to be able to transmit up to 3GBit/s of video data at a single pair of differential wires.

The first implementations will be fully backwards compatible to allow connection to existing INAP125 or third party devices. Thanks to these improvements, APIX technology offers a single cable solution for existing as well as future display products. ■

Solving Software Configuration Challenges in Embedded **MULTI-CORE** Designs

MATXM-CORE-411-B MicroATX motherboard from Emerson Network Power

MOORE'S LAW for software has never been officially defined; however, there is a stunning similarity with the original law pertaining to chips. Replace the number of transistors with the number of lines of code and you get Moore's Law for software.

The number of lines of code (like transistors) doubles about every two years. For now Moore's Law has proven to be correct but in the next decade or so, microprocessor technology will shrink nearly to the atomic level and would not be able to scale. But the same may not be true for software. To stay within reasonable thermal design power, we'll see multi-core chips and designs continue to grow. While this opens up new possibilities for software designs, it can also become a platform developer or a firmware developer's worst nightmare. Embedded virtualization technologies now allow options to run disparate operating systems on different cores over common shared memory, bus and heterogeneous cores.

However, even though multi-core made its debut in the desktop and server environment, one must wonder why it hasn't caused major problems for application developers in that domain. It is very interesting to compare the scenario of the desktop and server realm with the difficulties faced by embedded developers.

Challenges of Designing Software for Embedded Devices

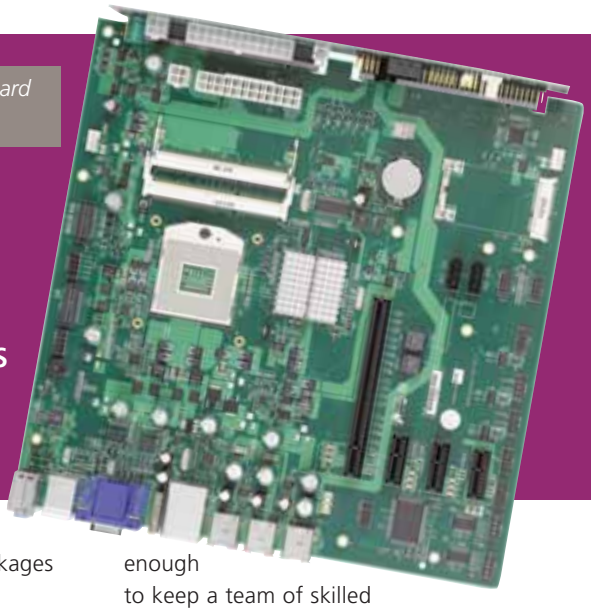
Engineers developing embedded software must face additional complexities that are most often foreign to the desktop or server world. In the desktop or server world, a developer has the advantage of being abstracted from the hardware and for the most part, even from the complexities of the base software platform. There are really just a few permutations to work with and that allows developers to concentrate on their applications rather than having to constantly worry about the complete platform – from hardware to operating system to middleware.

In the embedded world, almost every design has customizations in hardware design, board support package, drivers and operating systems. A large amount of effort goes into creating, configuring and maintaining a base platform before the application developers can start developing their value-add on to the device. This leads to several issues for various engineering departments:

- Platform developers spend the bulk of their time bringing the platform up to a stable state. This leaves them with little spare time to fine tune elements of the platform and optimize it for size, speed and their specific application needs.
- Application developers have to depend on the availability of a stable platform and this creates a significant lead time demand before application code can go live. This leads to longer development times.
- Ability to take early trials and create proof of concepts is severely limited. Designers, of course, always want to make the optimal selection for their hardware and platform configuration. However, since they have to spend time and resources to create a platform before even the first line of their application code is written, their choices are limited to making good guesses. While this historically hasn't been a big issue, it is becoming increasingly critical in the world of multi-core processors and virtualization.

Wind River's Embedded Development Kits

This past September, Wind River introduced Embedded Development Kits to address platform-related challenges for the embedded developer and offer resources that programmers in the desktop world have traditionally taken for granted. Packaged on



MATXM-CORE-411-B MicroATX motherboard from Emerson Network Power

Dinyar Dastoor, Senior Director of Field Engineering at Wind River, discusses the simple yet powerful solutions that will allow developers to unlock the power of very complex systems in this era of multi-core processors

a USB flash drive, these Embedded Development Kits include a processor board with optimized trial versions of Wind River's operating systems, development tools and embedded hypervisor and graphics software, enabling embedded developers to begin application development in less than one hour versus what traditionally can take days or weeks. The Embedded Development Kits are offered as an integral part of COTS and reference boards from all major board vendors.

Simplicity is at the core of these Embedded Development Kits. If you are an application or firmware developer, here is how it works: After setting up the board and connecting power supply, you insert the USB flash drive in any available laptop or desktop and power on the PC.

It does not matter whether you have Windows or Linux as your existing OS. The USB stick comes prepackaged with its own desktop Linux OS and does not even access your connected hard drive. The BIOS is configured to look for a USB flash drive first which allows the desktop to boot off the drive. Once the desktop is powered on, you are ready to start writing code and evaluating your applications within minutes.

The flash drive is a self-contained unit with preconfigured embedded operating systems, embedded tool suite and various media (documents, video) to start development. The board also comes pre-flashed with platform software that has been pre-configured. As a result, the tools work the first time you connect to it. All the sample application code is a part of the application package available in the tools.

The beauty of the Embedded Development Kits is that Wind River and the board partner has already provided all the complex configuration and customization work. This includes not only board support packages but also embedded virtualization (or "hypervisor" technology in embedded world) technologies with their relevant operating systems. For more complex boards, the kit offers several choices of configurations to start evaluation.

Why is Software Configuration So Relevant Now?

In an ever-changing world of technology, what seemed to be a perfect solution even a few years ago can feel very cumbersome today? Most often, these old solutions just simply cannot scale to the needs of evolving technologies. It was only a few years back that a 32-bit embedded single core machine with a good network stack was enough for most tasks. Today, we are constantly dealing with processors with multiple cores (2, 4, 16, 32 and growing), rigid requirements to isolate functionalities as well as faults, and the need to execute multiple incongruent operating systems in the same memory space.

The software content and work needed for configuration and optimization for performance and size has grown tremendously, and engineering departments find it very time-consuming to get it right the first time. In traditional models of embedded software delivery, vendors distribute modules like Lego blocks which engineers are required to put together depending upon their hardware and device design needs.

A typical multi-core embedded project requires up to ~ 10-15 DVDs and a platform engineer has to parse through large amounts of firmware, kernel and middleware components to retain only the bare minimum required for their design. After this exercise, each individual package then needs to be configured with multiple parameters. This is enough to keep a team of skilled engineers busy for couple of weeks just to get the first command prompt on the board!

This method of software distribution worked well over the past 20 years when embedded engineers had to deal with software on a couple of CDs. Given the complexities of multi-core, this approach does not scale. Wind River's Embedded Development Kit provides an alternative method of software development and removes the burden of configuration away from the engineer.

What's in Store for the Future?

Multi-core chips are becoming ever more ubiquitous and each chip vendor hopes to distinguish their value by offering some unique combination of core configuration, interconnect technologies and microcode libraries, providing hardware acceleration for specific applications. Additionally, the demand for complex software functionality for each core is increasing.

While all these elements point to the possibility of having a highly optimized system for a given application, it also typically means that the pressure of configuring these systems falls on the firmware or platform developer. Without assistance from solutions such as Embedded Development Kits, it will become increasingly difficult to create extensive trials, make smart and appropriate decisions or take full advantage of multi-core optimization.

Given the growing adoption of multi-core processors and its accompanying challenges, the embedded industry will have to continue to evolve and produce elegantly simple yet powerful solutions that will allow developers to unlock the power of very complex systems. ■

Colin Dente, CEO of Akya, explains how to avoid modern challenges when designing with DSPs through a new approach to the DSP technology

DRL – The 'Fourth Way' in Digital Signal PROCESSING

DIGITAL SIGNAL processing is one of the most commonly utilised functions in modern electronics. From radars to communications backbones, media players to mobile phones – DSPs are central to a huge variety of computing tasks.

The DSP is, therefore, an area of key interest to companies looking to maximise computing 'grunt' while minimising power usage and physical footprint, as well as producing devices that can be altered according to changing requirements.

DSP Horses for Courses

Traditionally there has been a choice of three ways to do digital signal processing: in software on a conventional "DSP" core, in hardware using fixed-function dedicated circuitry, or using general-purpose programmable devices such as FPGAs. Each of these three methods has distinct advantages and disadvantages.

Software running on a DSP core is extremely flexible. But that flexibility comes with a cost in terms of size and power. DSP cores tend to be large and relatively inefficient in terms of number of gates in total vs. the number of gates actually performing data manipulation functions. They also require large, power-hungry cache memories and sometimes multi-level caches. These complicate the operation of the device and can lead to lots of "wasted" cycles where the device is moving data around instead of processing it.

Hardware implementations of signal processing functions are at the opposite end of the spectrum to DSP cores. They are generally small, low-power and ultimately efficient, but also difficult to design and test, and completely inflexible. If requirements change, or a bug is found, changing their function requires a chip re-spin. Gone are the days when chip designers could say to their boss "We've found a bug in the control FSM, we need to re-spin the chip" and expect to keep their jobs.

FPGAs have been seen as the "third way". FPGAs are like a DSP core in terms of being flexible and easy to change, and they are hardware-like in terms not having the constraints of a fixed architecture in terms of functional units and memory.

Of course, a critic might turn that on its head and say that FPGAs are like DSP cores in terms of being general-purpose and, therefore, come with lots of power and size overhead. He might also say that FPGAs are 'hardware-like' in terms of being difficult to design and debug. Only an FPGA vendor will tell you that FPGAs are suitable for use in battery-powered consumer devices. And if FPGAs were truly easy to build processing solutions with then it'd be 'Xilinx vs Altera' rather than 'Intel vs AMD', and Microsoft would be developing the next version of Excel in Verilog.

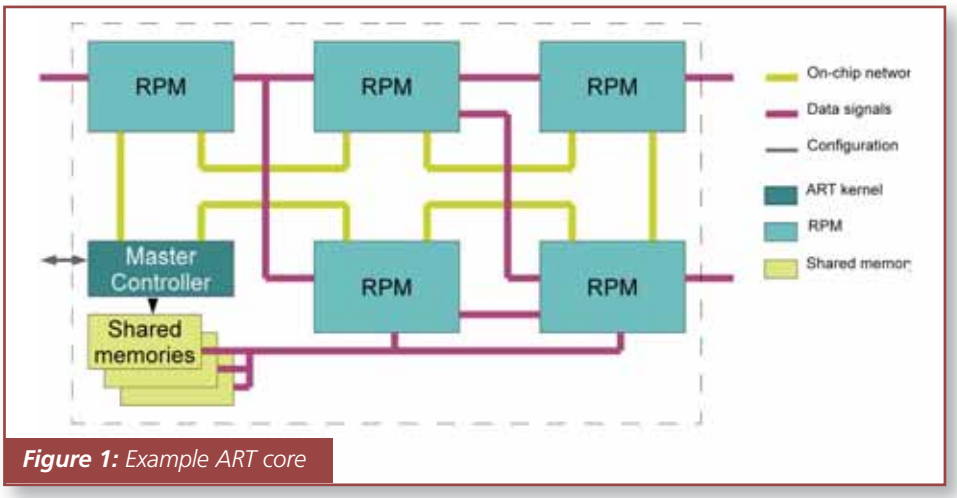


Figure 1: *Example ART core*

The Fourth Way

Having pointed out the shortcomings of the existing three ways of doing digital signal processing, you won't be surprised to learn that there's a 'fourth way'. Akya has developed a technology that combines dynamically-reconfigurable logic building blocks with EDA tools to create a reconfigurable fabric that can be programmed like a processor; the technology is called "ART".

ART achieves enormous gains in terms of size when compared to general-purpose programmable or reconfigurable technologies such as conventional DSPs or FPGAs by the simple expedient of not being general-purpose. More precisely, ART itself is completely general-purpose, but a given instance of ART in a chip is tailored to the specific requirements of that chip.

The phrase we like to use is that ART allows you to make a device that is just reconfigurable enough. How many times do people

build a video codec chip and then, after tape-out, say "Damn! If only we could reconfigure this to control a nuclear reactor?" Maybe in a Hollywood film, but not in the real world!

ART also has significant advantages when compared to a hardware implementation in that it is both flexible and easier to design. An ART-based design separates the datapath and control elements of a design, allowing the designer to consider the two parts separately. This "divide and conquer" approach not only speeds up the design process but also reduces the number of errors in the design, as the designer only needs to think of one thing at a time.

So let's have a closer look at how it works.

ART

ART is delivered as IP, allowing anything from an entire ASIC to a part of an SoC or ASSP to benefit from the flexibility and reconfigurability enabled by ART.

An ART-based device, called an "ART Core", consists of one or more Reconfigurable Processing Matrices (RPMs) connected together with a combination of direct interconnections (DI), a high speed network-on-chip called the ART Token Ring, (ATR NoC) and shared memories plus a Master Controller (MC) which controls the configuration of the device, the operation of the ATR NoC and the debug interface.

The structure of an example ART Core is shown in **Figure 1**.

An RPM consists of several core components plus a number of Processing Elements (PEs).

The core components in an RPM are an Interconnect sequencer (ISEQ), RPM Instruction Memory (RIM), the Reconfigurable Interconnect (RI) and the RPM Interface Controller (RIC).

The ISEQ is a small but powerful address sequencer that is capable of branching, looping and procedure calls, as well as handling interrupts. The ISEQ reads instructions from the RIM and generates the next RIM address based on the current instruction, its internal counters and a

Figure 2: *ART RPM*

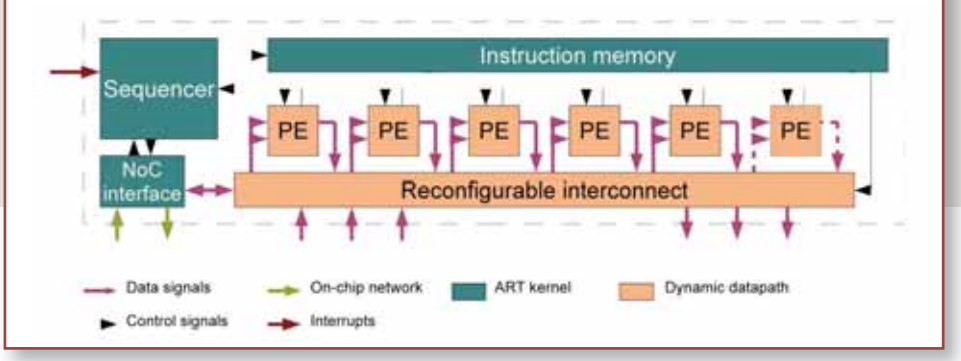


Figure 3: *Simple RPM connectivity*

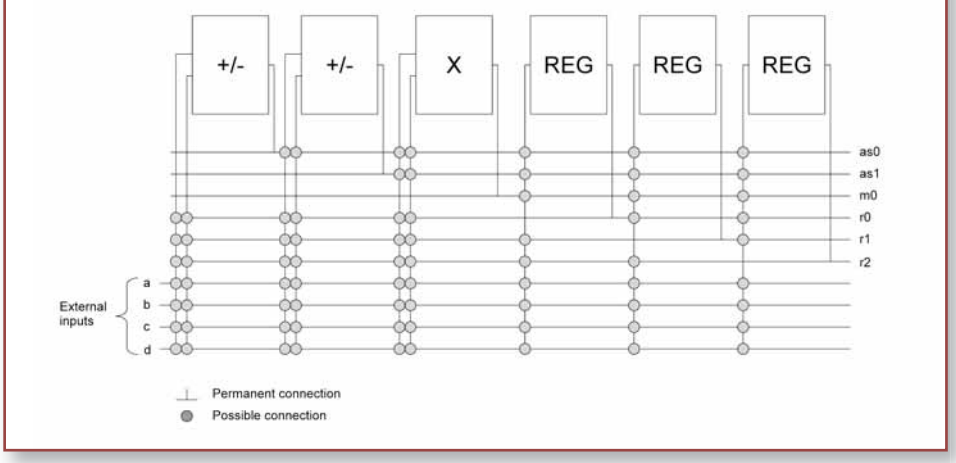


Figure 4: *Example datapath*

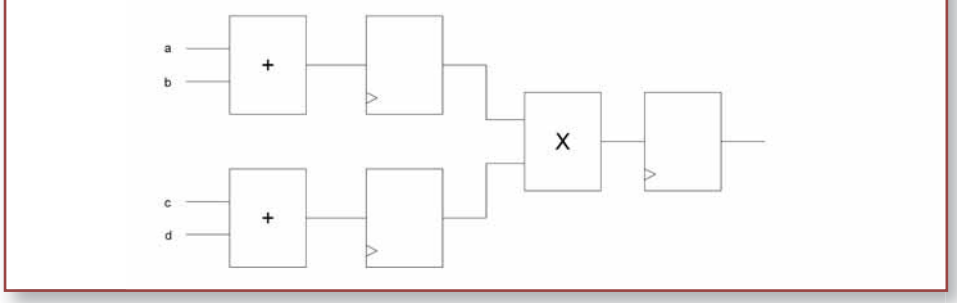
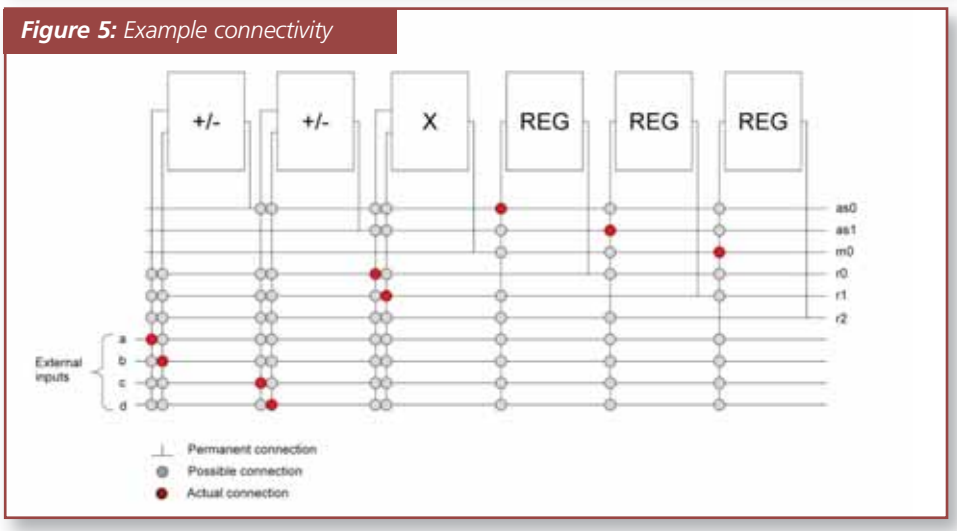


Figure 5: *Example connectivity*



sophisticated Boolean expression evaluator; the Branch Decision Multiplexer, or BDM, which combines the status outputs of processing elements and external control signals to generate a branch decision.

The output of the RIM is split into several fields, including the ISEQ instruction, the BDM control and a data field. In addition to these fields, the majority of the RIM output word consists of control signals that control the reconfigurable interconnect between PEs, and the operation of the PEs themselves.

The RI connects between PE inputs and outputs and external inputs and outputs of the RPM. At design time the engineer selects which outputs may be potentially connected to which inputs (the selection of which output is actually connected to a given input at any moment is determined by firmware).

The RIC controls communication between the RPM and the ATR NoC, providing configuration data for the RPM at power-on and during operation, allowing the RPM to communicate with other RPMs over the ATR NoC, and controlling clocks, interrupts and resets of the RPM.

The structure of a typical RPM is shown in **Figure 2**.

Figure 6: *EVPL mode circuit*

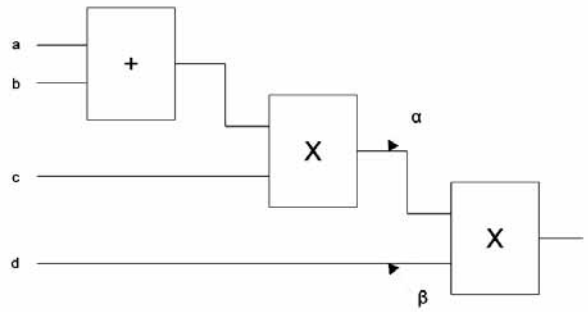


Figure 7: *EVPL mode connectivity – clock phase 0*

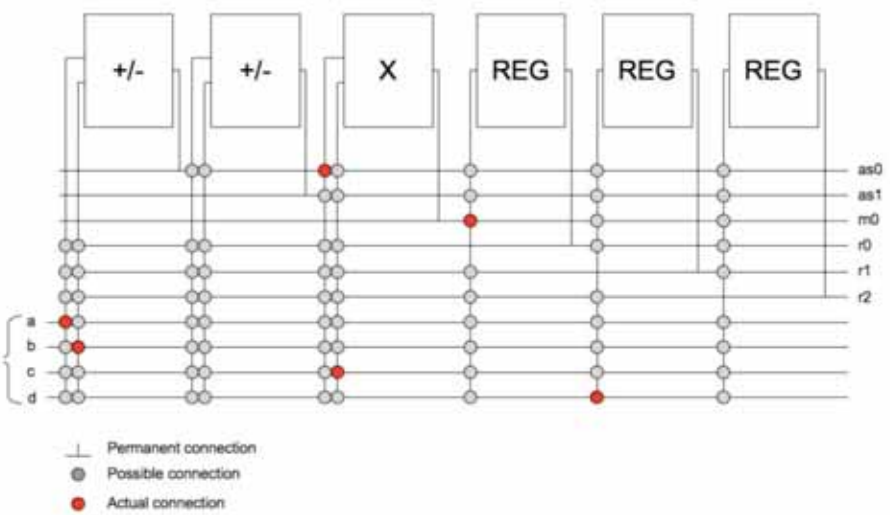
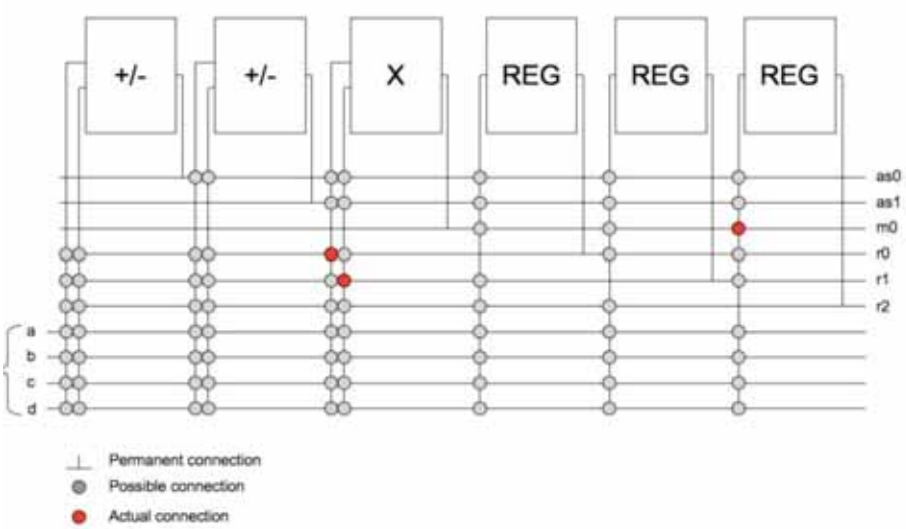


Figure 8: *EVPL mode connectivity – clock phase 1*



Using ART

ART based designs are created by determining the computational resources required to implement an algorithm or a set of algorithms, and describing the required resources using Akya's ART Architecture Description language (AAD), which is a simple Verilog-like HDL. This process is simpler than the corresponding design partitioning and implementation tasks in conventional RTL-based design as the resources described are more abstract ("adder", "multiplier", "register", etc.). Little thought needs to be given to the control aspects of the design at this stage, i.e. no worrying about FSM implementations, etc.

Once the hardware resources are defined, the operation and interconnectivity of the resources is defined by writing ART Firmware in ART Assembly Language (AAL). Depending on the nature of the task (and the background of the designer), the hardware can be viewed in different ways: As a dynamically configurable datapath, or as something like an enhanced VLIW processor where the microarchitecture changes with every instruction.

ART as a Dynamically Configurable Datapath

The hardware resources in an ART-based design are defined by instantiating Processing Elements (PEs) from the ART PE library, and defining the possible connectivity between them. For example, a very simple design might instantiate two adders, a multiplier and three registers, with the outputs of each PE able to be connected to the inputs of other PEs as shown in **Figure 3**.

Figure 3 shows the six PEs (two adder/subtractors, one multiplier and three registers). The output of each of these PEs is connected to its own bus (as0, as1, m0, r0, r1 and r2) and there are four external busses (a to d), which can provide inputs to the design.

The set of busses shown in Figure 3 as0, as1, m0, r1, r1, r2, a, b, c and d and the configurable connections between them and the inputs of the PEs form what we refer to as the "Reconfigurable Interconnect", or "RI".

If the designer wished to implement a datapath as shown in **Figure 4**, this could be achieved by creating connectivity as shown in **Figure 5**. In this case bus "r2" provides the output.

It's important to note that the designer doesn't really need to worry about putting red dots on grids of wires to use ART – the connectivity is expressed in a much more natural way which I'll describe later.

ART as an Enhanced VLIW Processor-Like Device

Very Long Instruction Word processors are characterised by having multiple functional units, each of which is explicitly controlled by the instruction word. An ART RPM consists of a set of registers and functional units together with a control processor (the "ISEQ" or Interconnect Sequencer), which controls the operation of these units and, so, looks superficially like a VLIW processor. However, an ART RPM can do much more than a VLIW processor because the flexibility of the dynamically-reconfigurable interconnect frees it from the constraints of the fixed microarchitecture of the VLIW processor.

An example of this added flexibility is shown by the Register → Function → Register restriction on operations in a conventional VLIW processor. An ART RPM does not have this restriction, function units (PEs) may be "chained together" to form a datapath. This chaining of PEs can replace multiple Register → Function → Register cycles with a single Register → Complex Function → Register cycle, giving substantial power savings and allowing the use of a lower system clock speed.

When using ART as an "enhanced VLIW processor-like device" (let's call it "EVPL mode"), the datapath created by the configuration of the Reconfigurable Interconnect (RI) changes with every clock cycle.

As a simple example of the use of EVPL mode consider the circuit of **Figure 6** (don't worry about the points labelled α and β for now).

Listing 1: *AAL code*

```
phase0:                                 // First clock cycle
        SEQ(NOP),                       // Advance to next instruction
                as0_inst(               // Control of add/sub 0
                        x <- a,  // Input x connects to bus a
                        y <- b,  // Input y connects to bus b
                        op = add        // Operation is "add"
                        ),
                m0_inst(                // Control of multiplier
                        x <- c,  // Input x connects to bus c
                        y <- as0        // Input y connects to output of add/sub 0
                        ),
                r0_inst(                // Control of register 0
                        din <- m0,      // Input connects to multiplier
                        load = yes      // Load register this clock cycle
                        ),
                r1_inst(                // Control of register 1
                        din <- d,       // Input connects to bus d
                        load = yes      // Load register
        );

phase1:                                 // Second clock cycle
        SEQ(BS0, cond = always,         // Unconditional branch
         phase0),                       // to label "phase0"

                m0_inst(                // Control of multiplier
                        x <- r0,// Input x connects to register 0
                        y <- r1 // Input y connects to register 1
                        ),
                r2_inst(                // Control of register 2
                        din <- m0,      // Input connects to multiplier
                        load = yes      // Load register this clock cycle
        );
```

To implement this circuit using the RPM shown in Figure 3 is possible by splitting the computation over two clock cycles. To do this, we partition the problem into two datapaths. The first produces the results labelled α and β; the second takes those two intermediate results and produces the final result. The connectivity required for this is shown in **Figure 7** and **Figure 8**.

In the first clock cycle (phase 0), the add and the first multiply are performed with the result stored in register 0. At the same time the fourth operand is stored in register 1. At the end of this cycle, r0 corresponds to α, and r1 corresponds to β.

In the second clock cycle (phase 1), the intermediate results are read from the registers and the multiplication is performed. By storing the result of the second multiplication in register 2, the result is available the following clock cycle on r2 and remains stable. If the result were read from m0 it would alternate between the true result and the intermediate result (α).

Depending on your view of the world, this example can be seen either as a dynamic reconfiguration of a datapath, or as VLIW-like behaviour, with two instructions – the first performing the instruction "r0 = a + b * c, r1 = d", and the second performing the instruction "r3 = r0 * r1". Which way you think of it doesn't really matter – just don't think of it as "just a VLIW processor" – it's much more than that.

The ART Assembly Language (AAL) code to implement this function would look something like that shown in Listing 1.

So, to summarise, ART IP allows the design of reconfigurable devices that have power and area similar to that of hard-wired RTL-based devices. Designs are easily changed after tape-out, simplifying bug fixes and adaptation to changing markets, reducing risk. Designing using ART is faster than RTL design, and firmware changes to existing designs can be made in a fraction of the time taken to recode RTL. It also carries low area and power cost, combining the flexibility of a programmable solution with area and power close to that of fixed-function hardware. ART provides a new approach to logic design that offers radical performance improvements over existing methods. ■

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Reducing the Burden on the BATTERY

Øyvind Janbu, CTO at Energy Micro, explains how MCUs need to evolve to boost energy efficiency

WHATEVER THE END product, all designers have specific tasks to solve and solutions will be influenced by the resources that are available and the constraints of cost, time, physical size and technology choice.

At the heart of many a good product, the ubiquitous microcontroller (MCU) often has a crucial influence on system power design and particularly in a brave new world that's rightly concerned with energy efficiency; users are entitled to demand a greater service from them. The ways in which MCUs are built and operate need to evolve dramatically, if best possible performance is to be achieved from limited battery resources.

Bearing in mind that the cost of even a typical coin cell battery can be relatively high compared to that of an MCU, there are obvious advantages in designing a system that offers best possible energy efficiency. Firstly, it can enable designers to reduce the cost and size of a battery. Secondly, it can enable designers to significantly extend the lifetime of a battery, consequently reducing the frequency of battery replacement and for certain products the frequency, cost and 'carbon footprint' associated with product maintenance call-outs.

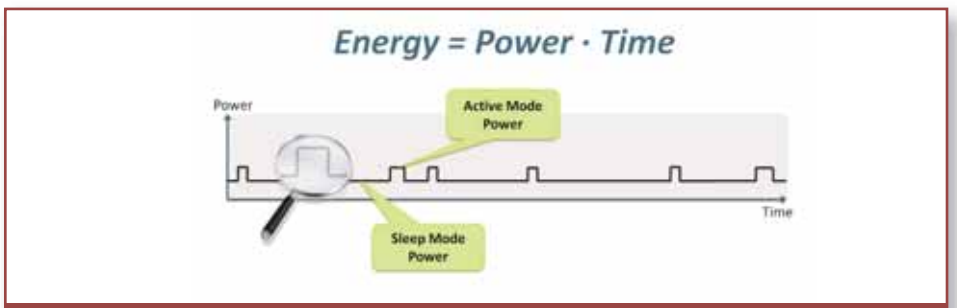

Figure 1: *How an MCU uses energy is what's important, whether active or in stand-by*

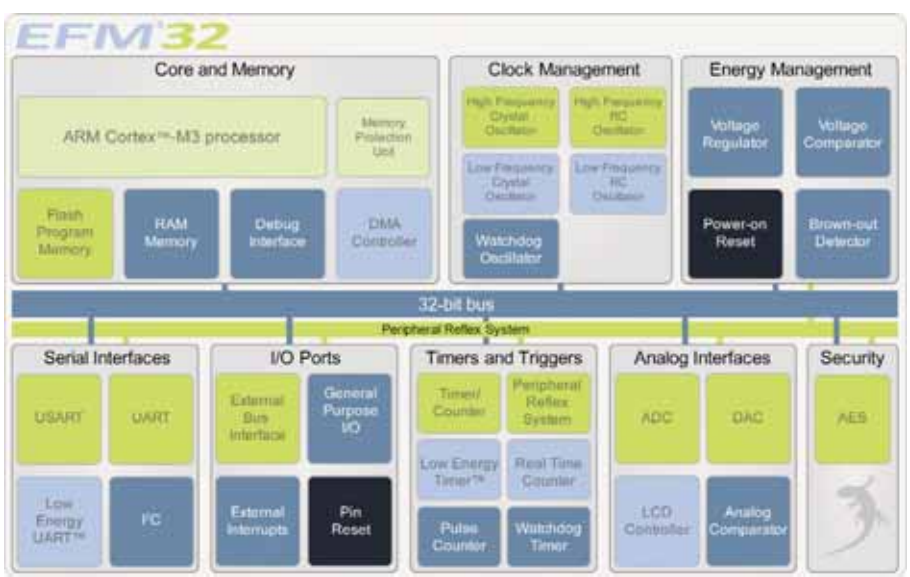

Figure 2: *Chip architecture for Energy Micro's ARM Cortex-M3 based EFM32 Gecko microcontroller*

It's Energy that Matters

MCUs like many other breeds of electronic component are these days very keen to stress their 'ultra low power' credentials, which is perfectly fine and appropriate where a device's dynamic performance merits. However, with a finite amount of charge available from a battery cell, it is how an MCU uses energy – i.e. power over the full extent of time – that needs to be more closely borne in mind, see **Figure 1**.

Product designers need to minimise the product of current and time over all phases of MCU operation, throughout both active and sleep periods – not only does every microamp count, but so does every microsecond that every function takes. With this thought in mind then why then continue to use an 8-bit or a 16-bit MCU?

8-bit vs 16-bit vs 32-bit

Considering alone their current consumption characteristics in a deep-sleep mode, then it's easy to understand why 8-bit or 16-bit MCUs have traditionally seen to be an attractive

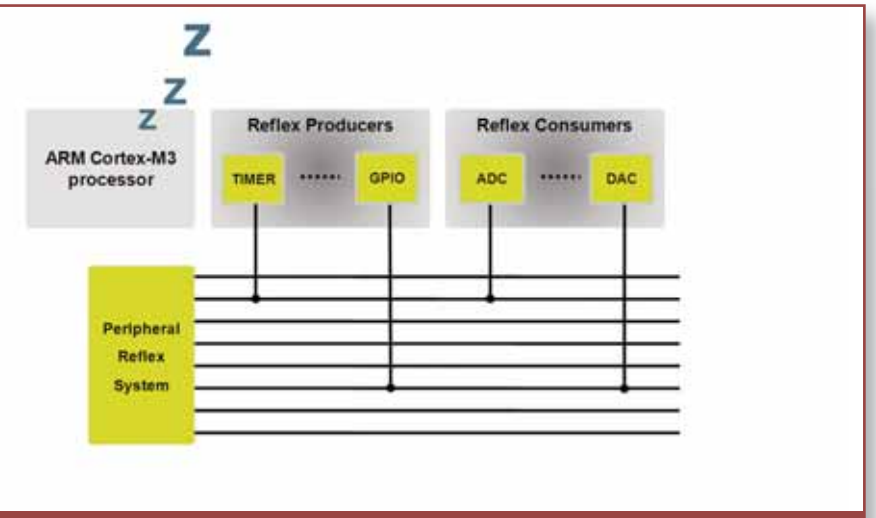

Figure 3: *With an MCU interconnect structure simple tasks can be carried out without waking the processor core*

proposition in energy sensitive applications, where MCU duty cycles can be very low. An MCU may, after all, stay in a deep sleep state for perhaps 99% of the time.

However, if product designers are rightly concerned with every microamp and microsecond every function takes, then using a 32-bit MCU should be considered more often even in the 'simplest' of product designs. The higher performance of 32-bit processors enables the MCU to finish tasks quicker and so spend more time in the low-power sleep modes, which lowers overall energy consumption. 32-bit MCUs are, therefore, not necessarily 'application overkill'.

More than that though, even simple operations on 8-bit or 16-bit variables can need the services of a 32-bit processor if system energy usage goals are to be achieved. And MCU designers really have no excuses either. By harnessing the full array of low-power design techniques available today, 32-bit ARM cores for example can be implemented, offering a variety of low-power modes, as good as or better than those of 8-bit alternatives, and achieving very rapid wake-up times at the same time.

There's also a common misconception that switching from an 8-bit MCU to a 32-bit MCU will result in bigger code size, which directly affects the cost and power consumption of end products. This is borne of the fact that many have the impression that 8-bit MCUs use 8-bit instructions and 32-bit MCUs use 32-bit instructions. In reality, many instructions in 8-bit MCUs are 16-bit or 24-bit in length.

The popular ARM Cortex-M3 and Cortex-M0 processors are based on the Thumb-2 technology, which provides excellent code density. Thumb-2 MCUs have 16-bit as well as 32-bit instructions, with the 32-bit instruction functionality a superset of the 16-bit version. Typical output from a C compiler gives 90% 16-bit instructions. The 32-bit version would only be used when the operation cannot be performed with a 16-bit instruction. As a result, most of the instructions in an ARM Cortex MCU program are 16-bits. That's smaller than many of the instructions in 8-bit MCUs, typically providing less compiled code from a 32-bit processor than 8 or 16 bit MCUs.

Staying Asleep

While using a 32-bit processor can enable an MCU to stay in a deep-sleep mode for longer, there is nevertheless some baseline power consumption which can significantly influence the overall energy budget. However, historically 32-bit processors have admittedly not been available with useful sub-µA standby modes. With the introduction of power efficient 32-bit architectures, the standby options are now complementing the reduced processing and active time.

With the relatively low power consumption many MCUs exhibit in deep sleep, the functionality they provide in these modes is often very limited. Since applications often require features such as real-time counters, power-on reset/brown-out detection or UART reception to be enabled at all times, many MCU systems

Figure 4: *Development kit for the energy friendly EFM32 Gecko microcontroller complete with Advanced Energy Monitoring*

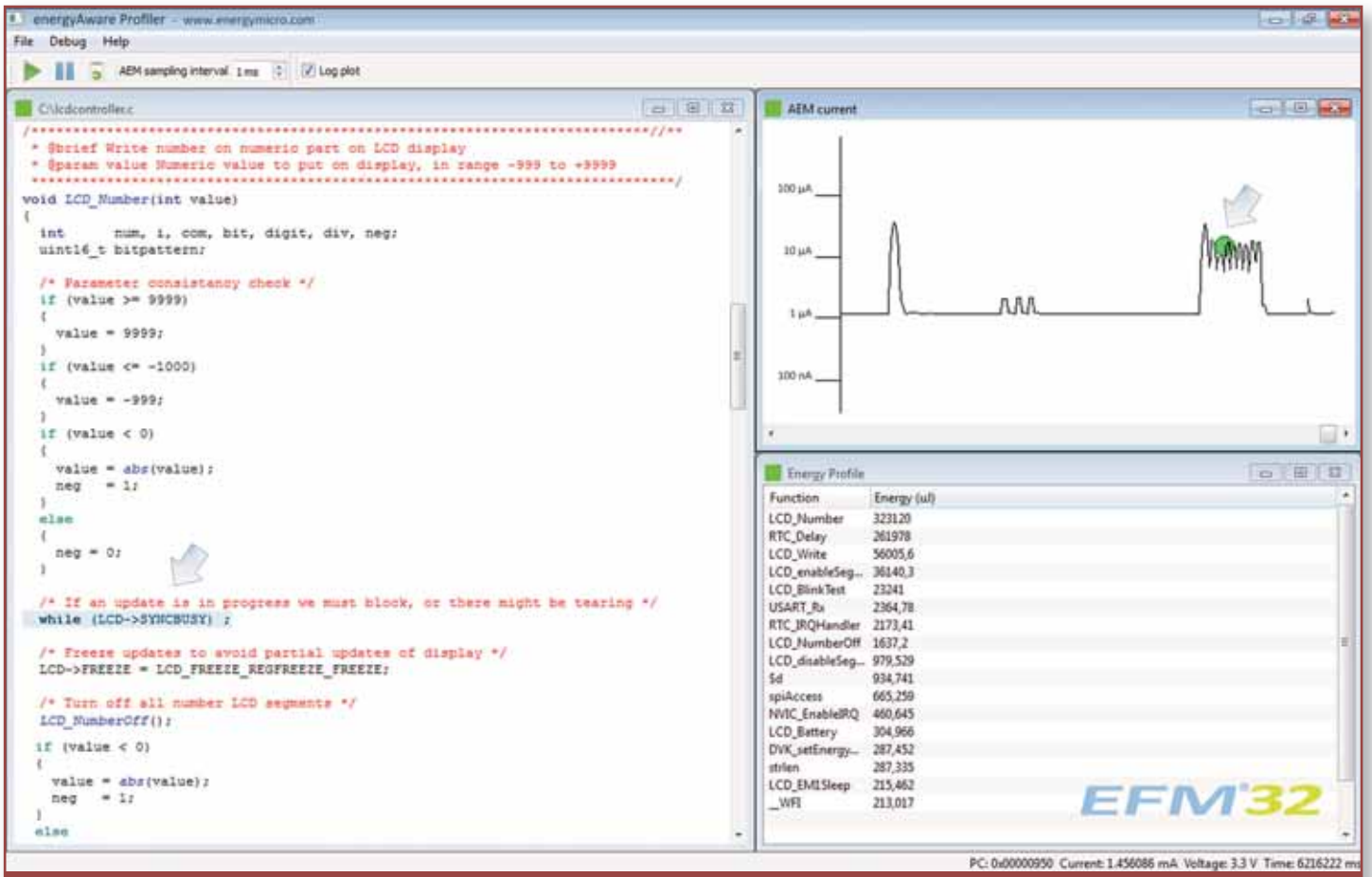

Figure 5: *energyAware Profiler provides three simultaneous views; real-time application current consumption, object code listing and energy profile of individual application functions*

are prevented from ever entering deep sleep since such basic features are only available in an active run mode. Many MCU solutions also have limited SRAM and CPU state retention in sub-µA standby modes, if at all. Other solutions need to turn-off or duty-cycle brown-out and power-on reset detectors in order to save power.

In the pursuit of energy efficiency then MCUs need to provide product designers with a choice a sleep modes offering the flexibility to scale basic resources, and thereby the power consumption, in several defined levels or energy modes. While energy modes constitute a coarse division of basic resources, additional fine-grained tuning of resources within each energy mode should also be able to be implemented by enabling/disabling individual peripheral functions.

A Wake Up Call

There's little point though in offering an MCU with tremendous sleep mode energy consumption if its energy efficiency gains are lost due to the time it takes for the MCU to wake up and enter run mode.

When an MCU goes from a deep sleep state, where the oscillators are disabled, to an active state, there is always a wake-up period, where the processor must wait for the oscillators to stabilise before starting code execution. Since no processing can be done in this period, the energy spent while waking up is wasted energy, and so reducing the wake-up time is important to reduce overall energy consumption.

Furthermore, MCU applications impose real time demands which often mean that the wake-up time must be kept to a minimum to enable the MCU to respond to an event within a set period of time. Since the latency demanded by many applications is lower than the wake-up time of many existing MCUs, the device is often inhibited from going into deep sleep at all – not a very good solution for energy sensitive applications.

A beneficial solution would be to use a very fast RC oscillator that instantly wakes up the CPU and then optionally transfers the clock source to a crystal oscillator if needed. This meets both the real time demands as well as encourages run and sleep mode duty cycling. Albeit the RC oscillator is not as accurate as a crystal oscillator, the RC oscillator is sufficient as the CPUs clock source during crystal start-up.

The Time on the Clock

We know that getting back to sleep mode is key to saving energy. Therefore, the CPU should preferably use a high clock-frequency to solve its tasks more quickly and efficiently. Even if the higher frequency at first appears to require more power, the advantage is a system that is able to return to low power modes in a fraction of the time.

Peripherals however might not need to run at the CPU's clock frequency. One solution to this conundrum is to pre-scale the clock to core and peripherals, thereby ensuring the dynamic power consumption of the different parts is kept to a minimum. If the peripherals can further operate without the supervision of the CPU, we realise that a flexible clocking system is a vital requirement for energy efficient MCUs.

ENERGY EFFICIENT MICROCONTROLLERS

Taking into account the sort of considerations described in this article, Energy Micro has developed a 32-bit energy friendly MCU capable of consuming a quarter of the energy required by 8-bit, 16-bit and 32-bit MCU alternatives.

With the EFM32 Gecko energy-friendly MCU, designers of energy sensitive products have the processing capacity with which to develop fully-featured next generation products, which are at the same time capable of extending the lifetime of a typical 3V battery cell by at least 300%.

Using the latest low power IC design techniques, Energy Micro has built the EFM32 Gecko MCU around the 32-bit ARM Cortex-M3 processor core. The device's chip architecture has been designed from the ground up with energy efficiency in mind, see Figure 2.

EFM32 provides designers with five distinct and graded energy modes serving to help minimise energy consumption. The Gecko MCUs form the basis of systems with a minimum of external components, thanks to a comprehensive set of autonomous low power on-chip peripheral functions. These include an 8-channel, 12-bit ADC using 200µA at full resolution and 1MS/s conversion rate; a 4x40 segment LCD controller using just 550nA and providing boost, contrast, animation and blink functions; and a special low energy UART, a full UART with 32kHz clock, consuming only 100nA at a data transmission speed of 9600 baud.

In addition, for data encryption/decryption tasks the inclusion of a dedicated AES accelerator function block allows the CPU to hand off the AES encryption algorithm work to dedicated hardware, get on with other processing and get the encrypted or decrypted data back in quicker time, so saving more battery energy.

EFM32 integrates an interconnect structure called the Peripheral Reflex System enabling peripheral to talk to peripheral without any intervention from the ARM core, thereby enabling it to stay asleep and so consume less energy, see Figure 3.

The EFM32's development kits also come with an Advanced Energy Monitoring (AEM) system, a facility which continuously measures current consumed. This measurement is integrated to depict accurately the power used over time, allowing real life use-cases to be optimised for low power operation. An energy graph can be displayed on the development kits' on-board LCD display, see Figure 4.

When used with the energyAware Profiler 'energy debugging' software tool, the AEM system enables the user to identify the actual source code being executed at a given moment in time as shown by an energy graph. This instantly gives the engineer a pointer to any part of the program that causes high energy consumption, allowing the code to be optimised to lower overall energy usage, see Figure 5.

Peripheral Autonomy

The obvious way for MCUs to use less energy is to allow the CPU to stay asleep and so the development of peripherals that can operate with minimum or no intervention from the CPU is another worthy consideration for MCU designers. When peripherals look after themselves, the CPU can either solve other high level tasks or simply fall asleep, saving energy either way.

With advanced sequence programming, routines for operating peripherals previously controlled by the CPU can be handled by peripherals themselves. The use of a DMA controller provides a pragmatic approach to autonomous peripheral operation. Helping to offload CPU workload to peripherals, a flexible DMA controller can very effectively handle data transfers between memory and communication or data processing interfaces.

Of course there's little point in using autonomous peripherals to relieve the burden of the CPU if they're energy hungry. MCU makers also need to closely consider the energy consumption of peripherals such as serial communication interfaces, data encryption/decryption engines, display drivers and radio communication peripherals. All peripherals must be efficiently implemented and optimized for energy consumption in order to fulfil the applications' need for low system level energy consumption.

Taking the autonomy ideal a step further, the introduction of additional programmable interconnect structures into an MCU enable peripherals to talk to peripherals without the intervention of the CPU, thereby reducing energy consumption even further.

A typical example of peripheral talking to peripheral would be an ADC conversion periodically triggered by a timer. A flexible peripheral interconnect allows direct hardware interaction between such peripherals, solving the task while the CPU is in its deepest sleep state.

A Final Thought: 'Energy Debugging'

Having an energy friendly microcontroller, however, will not by itself means users are guaranteed of the lowest possible energy usage. Many system implementation choices need to be made and all can impact on energy consumption. While the MCU may play a starring role, choosing the right external components and integrating them in a sensible way is also of great importance. Being able to identify and remove energy drains at an early stage of prototype development can significantly reduce the overall energy consumption of the end product.

We would all be wise then to consider the debug process of low power embedded systems development as becoming a 3-stage cycle from now on: hardware debugging, software functionality debugging and software energy debugging. MCU development tools also need to evolve to enable designers to identify wasteful 'energy bugs' in software during the development cycle. Discovering energy inefficient behaviour, endangering battery lifetime during a product field trial is after all really too late! ■

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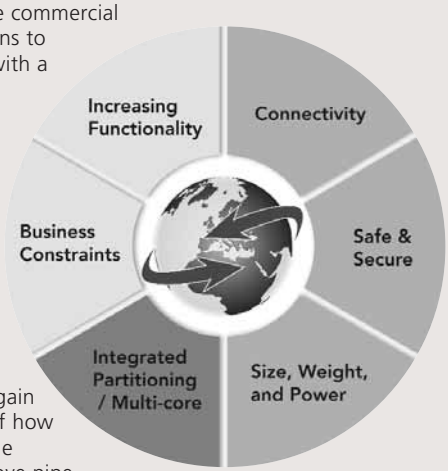

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Next year, the Avionics and Defence Electronics Europe 2011 will be held in March 16-17 in Munich, Germany at the M.O.C. Centre.

Among the session topics will be Single European Sky (SES) and future avionics systems; current ATM/avionics realities; a panel discussion titled 'Integrating new avionics into airplanes in a down economy' with panelists from KLM Royal Dutch Airlines, Airbus, Rockwell Collins and Honeywell Aerospace; avionics market and traffic forecasts; helicopter avionics modernization; and EFBs (electronic flight bags) and avionics systems certification challenges. Content is driven by an advisory board that includes representatives from Airbus, Boeing, SESAR JU, FAA, Avtech and others.

Two other content levels are offered in addition to the main avionics agenda: 50-minute workshops and 2-hour master classes, which cover the technical challenges avionics engineers face every day in the areas of software development, software and hardware safety certification and test and measurement technology among others.

The Defence Electronics part of the event will be in its second year and has content driven by its inaugural advisory board led by Meggitt Defence Systems, Elettronica and General Electric Intelligent Platforms. Session topics will include commercial-off-the-shelf (COTS) integration challenges in defence electronics systems; managing obsolescence and through-life costs in defence electronics; defence electronics market analysis; thermal management challenges in military systems; creating a trusted supply chain and more.

For more information on the event, visit **www.avionics-event.com**. For exhibiting opportunities contact Jo-Ann Pellegrini in North America by phone at 650-946-3169 and by email at JoAnnP@pennwell.com; and internationally James McAuley at +34 651 675 516 and by email at jmcauley@pennwell.com. ■

CURRENT MODE LOG DOMAIN NOTCH FILTER DESIGN BASED ON ADDING FILTERING BLOCKS

LOG DOMAIN FILTERS are a new member of current mode, active, continuous time filters family. Log domain filters, more generally ELIN filters, are suitable for low voltage and power applications, have large dynamic range and work at high frequencies. Additionally, these filters are highly linear, produce low distortion and can be electronically tuneable. The design of log domain filters requires only transistors, capacitors and current sources.

Log domain filters use the natural nonlinear feature of elements directly. While the signal is processed in the circuit nonlinearly, the overall transfer function from input to output remains linear. In the circuit, the input and output variables, dominant variables and control variables are all currents; therefore, the filter is considered to be current mode circuit.

Log domain filters also use the idea of the companding signal processing. The input current is first compressed using a logarithmic function while it is forced to drive a BJT transistor since the emitter-base voltage of the device is a logarithm of the current. The output circuitry has an expanding block, which means that the output voltage is applied to a BJT's base-emitter to obtain a current of exponential of the voltage. Since the output function is reverse function of the input, the overall transfer function remains linear without using any element to linearize it. A general log domain block diagram is shown in **Figure 1**.

Class AB Design

Class AB circuits are combination of Class A and Class B. This circuit has low noise, low distortion and high linearity. It also reduces power consumption comparing to Class A. Although Class AB is used for amplifications, it was not used for filters until the late 90s.

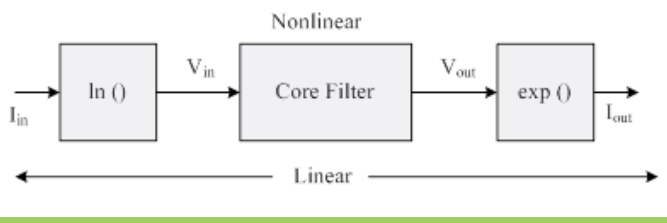

Figure 1: *Log domain filter set-up*

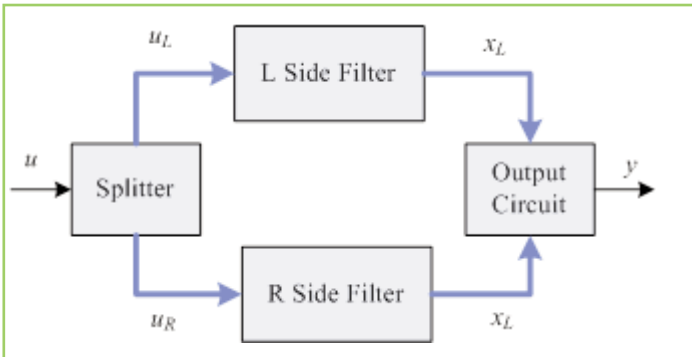

Figure 2: *Block diagram of a differential filter*

The general theory of Class AB filters in the log domain was developed by Frey and Tola. Then, using this theory, various Class AB filters have been designed. According to Class AB circuit procedure we process signals in two parts which are named as "L" side and "R" side. Both sides have the same architecture blocks.

The relationship of L, R and original signals is shown in **Equation 1**. The input signal is split into two pieces by using a current splitter. In this equation u is the input signal, x is the state variable and y is the output signal. A general differential type Class AB block diagram is shown in **Figure 2**.

$$\begin{aligned} u &= u_L - u_R \\ x &= x_L - x_R \\ y &= y_L - y_R \end{aligned} \tag{1}$$

Second Order Low-Pass Filter

General second order low-pass filter transfer function can be written as **Equation 2**. In this equation, ω_0 is equal to pole frequency; Q is equal to quality factor and k_1 is equal to gain.

$$H_1(s) = \frac{k_1 * \omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2}$$

Second Order High-Pass Filter

General second order high pass filter transfer function is given as **Equation 3**. In this equation, ω_0 is equal to pole frequency and Q is equal to quality factor of the filter.

$$H_2(s) = \frac{s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{3}$$

Second order Class AB log domain filter circuit is shown in **Figure 3**. This filter can be designed either low-pass or high-pass filter.

Notch Filter

In signal processing, a band stop filter or band rejection filter is a filter that passes most frequencies unaltered, but attenuates those in a specific range to very low levels. A notch filter is band stop filter with a narrow stop band. A second-order notch filter transfer function can be written as shown in **Equation 4**.

$$H_2(s) = \frac{s^2 + \omega_n^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{4}$$

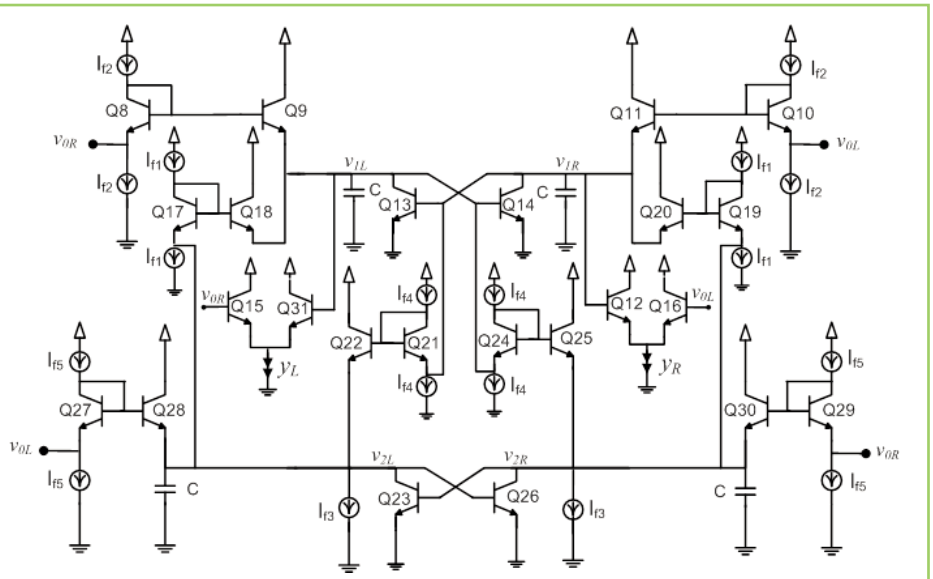

Figure 3: *Second order Log-domain filter circuit*

function turns into a second order low-pass notch filter. The frequency and time domain responses of the second order low pass notch filter are obtained as given in **Figures 8** and **9** respectively. (Figures 7, 8 and 9 are shown on the next page).

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Pamukkale University
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Turkey

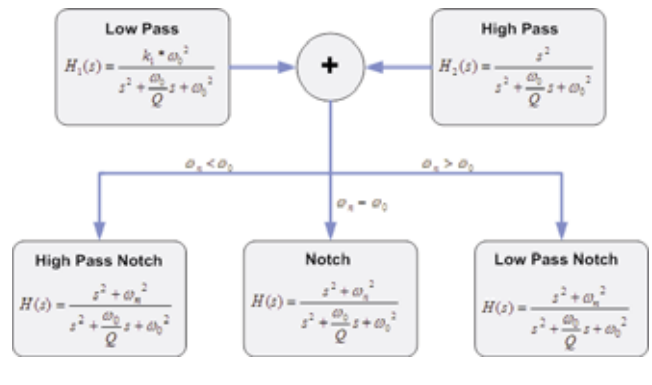

Figure 4: *Block diagram of the proposed notch filters*

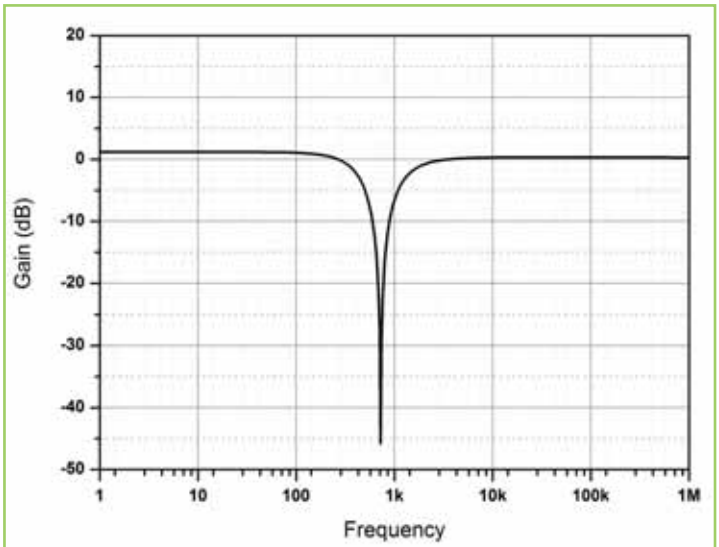

Figure 5: *Notch filter frequency gain response*

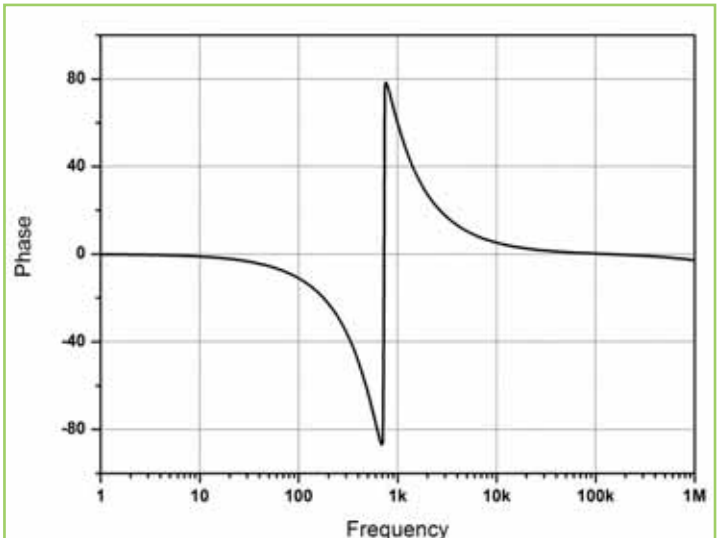

Figure 6: *Notch filter frequency phase response*

Three cases of the second order notch filter are possible: The regular notch, obtained when $\omega_n = \omega_o$; the low pass notch, obtained when $\omega_n > \omega_o$; and the high pass notch, obtained when $\omega_n < \omega_o$.

A notch filter in log domain can be synthesized directly by using Equation 4. An alternative approach is considered in this work. Let us consider the transfer function of low pass and high pass filters of Equations 2 and 3 respectively. Assuming $\omega_n^2 = k1 * \omega_o^2$ and adding these filters properly, a second order notch filter in log domain can be designed. This approach is shown in **Figure 4**.

First of all, if ω_n of Equation 4 is selected to be equal to ω_o, the transfer function turns into that of a second order regular notch filter.

The proposed second order log domain regular notch filter circuit is designed and simulated in PSpice by using the CBIC-R transistor model. The circuit supply voltage is selected to be 3V. Frequency domain analysis is performed. The obtained results are given in **Figure 5** and **6**.

Secondly, if ω_n is selected to be less than ω_o, the transfer function turns into a second order high-pass notch filter. The frequency response of the high pass notch filter is shown in **Figure 7**.

Finally, if ω_n is selected to be more than ω_o, the transfer

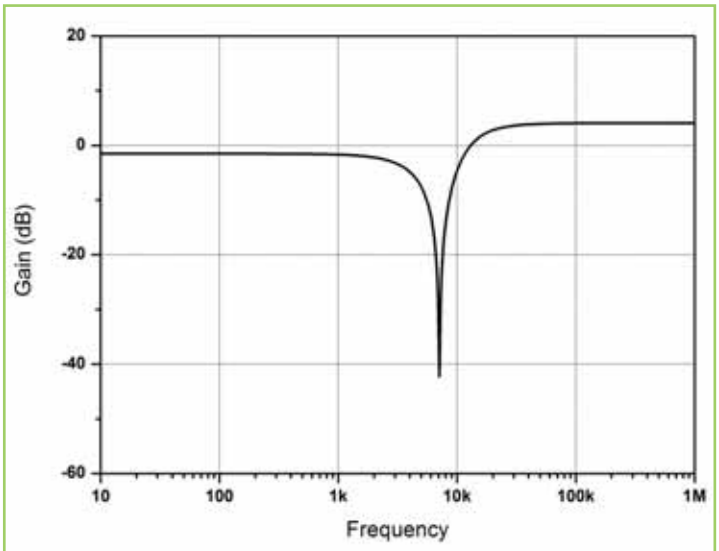

Figure 7: *High pass notch filter frequency gain response*

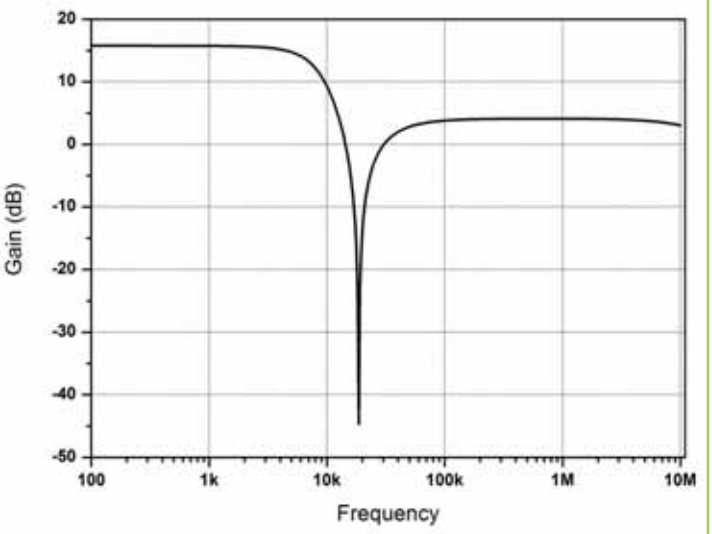

Figure 8: *Low pass notch filter frequency-gain response*

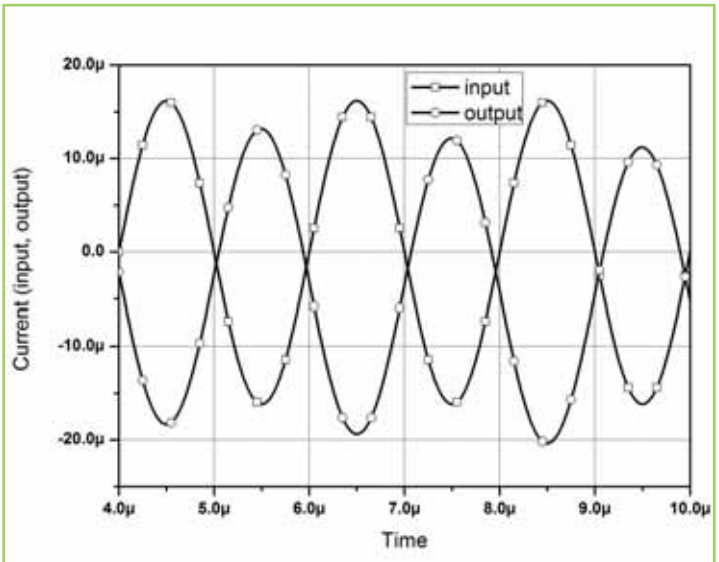

Figure 9: *Low pass notch filter time-domain response*

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NEW IEC 61850 TOOL SVSCOUT SOFTWARE FOR ANALYZING IEC 61850 SAMPLED VALUES

Omicron now offers a new measurement and testing tool for engineers and IED developers. The new SVScout software subscribes to the Sampled Values streams from merging units and displays the waveforms of the primary voltages and currents in an oscilloscope view. Cursor functions allow the user to compare individual values on the traces. RMS values and phase angles calculated from the Sampled Values are displayed in a phasor diagram and a table. Expert functions provide additional information about the received data, such as the detailed decoding of the quality codes.

The broad functionality of SVScout offers the possibility to perform many different tasks, ranging from the simple display of Sampled Values to a detailed investigation of a merging unit's performance. This makes the software ideal for commissioning or research and development. A free trial version of SVScout is available on the Omicron website

www.omicronusa.com

LECROY INTRODUCES SPARQ SIGNAL INTEGRITY NETWORK ANALYZERS

LeCroy Corporation announced the launch of a new class of instrument, the SPARQ series of Signal Integrity Network Analyzers. The SPARQ measures 40GHz S-parameters on up to 4-ports with single button press operation at a small fraction of the cost of traditional methods such as Vector Network Analyzers. With the low price and ease of use of the SPARQ, multi-port S-parameter measurements are now accessible to a much wider audience.

The SPARQ is a time domain instrument, using TDR/T technology along with patented LeCroy innovations to rapidly acquire waveforms and measure the S-parameters of a device under test. The SPARQ measures both frequency and time domain results, and outputs standard Touchstone S-parameter files that are ready to be loaded into the user's simulation software. The unit is small, rugged, PC-based and portable, and includes all of the hardware and software tools required by the signal integrity engineer for characterizing passive devices.

www.lecroy.com

IDT INTRODUCES INDUSTRY'S MOST ACCURATE ALL-SILICON CMOS OSCILLATOR

Integrated Device Technology (IDT) announced the industry's most accurate all-silicon CMOS oscillator, which achieves an industry-leading 100ppm total frequency error across temperature, voltage and other factors.

Using the patented IDT CMOS oscillator technology, the IDT3C02 oscillator replaces quartz crystal-based oscillators with a monolithic CMOS IC at frequency accuracy of 100ppm and below, and at very thin form-factors without the use of any mechanical frequency source or PLL. The product is specifically designed to work with next-generation storage, datacom and connectivity interfaces, such as 1Gb Ethernet, SAS, SuperSpeed USB (USB 3.0) and PCI Express. The product is a low-power, low-jitter replacement to general-purpose quartz crystal oscillators, making it ideal for server and enterprise designs as well as datacom devices with Ethernet ports.

The IDT3C02 oscillator generates highly accurate frequencies on chip without relying on a piezo-electric or mechanical resonator. Built on a standard, readily available CMOS process, the device utilizes a programmable architecture and supports various configuration options.

www.idt.com

SMALLER, LEANER, MEANER

VTI has announced its smallest 3-axis gyro sensor with lowest power consumption to date – the CMR3000.

The sensor utilises a shared sensing mass and coupled resonator structure in orthogonal multi-mode operation. This eliminates cross talk between axes and requires only one drive loop. Patented simplified low current consuming phase-shift readout electronics and wafer level quadrature signal design enable excellent stability in real life environments.

The CMR3000 boasts the market's lowest current consumption of 5mA and is enhanced with a power-save feature. In duty cycled operation, further current consumption reductions of tens of percent can be achieved, which can almost double the battery life in a portable device.

The CMR3000 is optimised for user interface and gaming applications. Due to gaming requirements, the measurement range is ±2000dps with selectable measurement bandwidths. For cell phones the wafer level package enabled smallest size of 3.1 x 4.2 x 0.8mm3 with digital SPI and I2C interfaces.

www.vtitechnologies.com

NEW OPTIONS FOR HARTING'S HAR-MIK MINIATURE D CONNECTORS

Three new bellows-type surface-mount (SMC) female right-angled connectors have been added to the Harting har-mik family of miniature D 1.27mm pitch connectors.

Designed for cable-to-board applications where space saving and high data transfer rates are demanded, the new variants complete the har-mik bellows SMC portfolio by offering 20, 50 and 68 poles, respectively.

Availability of these new connectors will ease automated assembly, since they can be terminated in the same solder reflow process as all other board-mounted SMC components. The connectors are available in suitable tray or reel packaging, which are fully compatible with the various handling equipments of an automated assembly line.

The bellows mating technology used in these har-mik connectors makes them an ideal choice for applications requiring repetitive plugging and blind mating.

The Harting Group develops, manufactures and distributes electrical and electronic connectors, network components, pre-assembled system cables and backplane assemblies. These products are capable of withstanding the harshest demands in industrial environments and provide high data rates for electronic applications.

www.harting.com

NEW FEATURES FOR THE OMICRON CT ANALYZER

The CT Analyzer provides fast and comprehensive testing of current transformers for protection and metering applications. Released in September, the improved CT Analyzer now features additional software functions and new hardware accessories.

As a new measurement function for the CT Analyzer, the RemAlyzer allows current transformers to be tested for residual magnetism. Residual magnetism may occur in current transformers due to very high currents or DC offsets during fault conditions. Core saturation effects caused by residual magnetism, may lead to the incorrect operation of protection relays.

The new CT SB2 switch box for the automated testing of multi-ratio CTs is available as a stand-alone unit. This can be attached to the CT Analyzer thus eliminating the need for re-wiring. This provides simple, colour-coded, six-channel connection possibilities guaranteeing convenient wiring and avoiding time-consuming and error-prone reconnection.

www.omicron.at

OPTICAL SPECTRUM ANALYSER OFFERS 'BEST IN CLASS' OPTICAL PERFORMANCE

The new Yokogawa AQ6370C is an optical spectrum analyser offering the world's 'best in class' optical performance combined with excellent functionality and operability for applications including R&D and production testing of optical devices and transmission systems.

Covering the wavelength range from 600 to 1700nm and applicable to both single-mode and multimode fibres, the AQ6370C provides unprecedented optical performance, including high wavelength accuracy of ±0.01nm, high wavelength resolution of 0.02nm, ultra-high dynamic range of 78dB (typical), wide level range of -90dBm and fast sweep speed of 0.2s/100nm.

Enhanced functionality and operability are provided by a large, bright LCD screen, easy operation via panel keys and a mouse, four USB ports including memory, mouse and keyboard interfaces, and high-speed GPIB and Ethernet remote interfaces. The instrument also has a built-in wavelength reference source and a range of integral analysis functions.

The ultra-high dynamic range (typically 80dB) results from an enhanced stray-light suppression ratio in the monochromator.

www.yokogawa.com

MICROTCA CONNECTORS FOR EXTREME ENVIRONMENTS

The Harting MicroTCA backplane connector has now passed the ruggedised environmental tests laid down in the draft MTCA.3 specification. The PICMG, a leading standards organisation for the communications, industrial and embedded computer industries, recently announced the successful completion of the "MicroTCA conduction cooled" test programme for these devices.

The MTCA.3 subsidiary specification of the MicroTCA standard targets defence and aerospace applications with extreme requirements for vibration, shock and temperature range based on MIL-STD-801. The goal of the recent tests was to show that the card edge connector system meets the stringent environmental requirements for the target markets.

The tests were performed by the independent testing and research company Contech Research. In the test setup, a backplane equipped with Harting MicroTCA connectors featuring the company's con:card+ technology was used.

After completion, the HARTING connector is now the first and currently the only MicroTCA connector recommended for a conduction-cooled MicroTCA system.

www.harting.com

THREE-PHASE SENSORLESS MOTOR DRIVE IC FOR FAN AND BLOWER APPLICATIONS

The new A4941 from Allegro MicroSystems Europe is a three-phase, sensorless, brushless DC motor driver IC, designed for fan and blower applications in the white goods and office automation sectors.

Key features of the new device, which is housed in a small eTSSOP package, include sensorless commutation, a wide (5-16V) supply voltage range, 1.25A peak output current, -40° to +105°C operating temperature range, lock detection with auto restart and soft switching for reduced audible noise.

The motor drive system in the A4941 consists of three half-bridge NMOS outputs, back EMF sensing circuitry, adaptive commutation control and a state sequencer. The sequencer determines which output devices are active, while the back EMF sensing circuits and adaptive commutation circuits determine when the state sequencer advances to the next state.

The three half-bridge outputs are controlled by a state machine with six possible states. Motor back EMF is sensed at the tri-stated output for each state.

www.allegromicro.com

ITT INTERCONNECT SOLUTIONS'S UK FACILITY ACHIEVES SC21 SILVER ACCREDITATION

Global connector manufacturer and supplier, ITT Interconnect Solutions, has announced that its UK facility has been awarded Silver Accreditation in the Supply Chains for the Twenty First Century (SC21) national aerospace and defence supply chain improvement programme. Against a background of increasingly intense international competition, achieving supply chain improvement is crucial to the continued success of the UK aerospace and defence industry. SC21 was set up four years ago with the aim of delivering real results and modernising the UK supply chain through the participation of companies of all sizes.

Of over seven hundred companies in the SC21 programme, ICS Basingstoke becomes one of only six to reach silver status since the programme's inception and achieved the additional accolade of immediate elevation to silver level following an intensive year-long audit process. ICS Basingstoke is a preferred supplier to Thales, who formally nominated it to join SC21 in early 2009.

www.ittcannon.com

HMO352X SERIES – NEW FUNCTIONS ADDED AS STANDARDS

Shortly after the market introduction of the HMO2524 oscilloscopes, the built-in bus signal source turned out to be a most popular feature. This signal source with 4 terminals is the first and unique possibility – worldwide – to take up to 4 bits wide parallel data (stochastic bit pattern or counter output), SPI, I2C or UART/RS-232 signals with user data as a reference directly from the oscilloscope. This helps to perform the usually complex settings with a known signal so the user can turn more quickly to his measuring problem.

Responding to the great demand, Hameg now implemented this feature also in the 350MHz oscilloscopes HMO3522 and HMO3524. Further, a firmware update extends the application areas of the whole HMO series enormously; the most important new features include selectable interpolation (linear, pulse, sin x/x); selectable number of data for FFT analysis (2 to 64k); new screen print-out format; new parameters for automatic measurements and others.

www.hameg.com

MICROLEASE INVESTS £1.5M IN NEW TELECOMMUNICATIONS TEST EQUIPMENT

Test equipment rental, contract hire and asset management organisation, Microlease, is investing £1.5m in new test equipment from JDSU. This will strengthen its inventory with the latest test platforms for the telecommunications and optical communications markets.

The JDSU MTS-6000A and MTS-8000 offer field technicians the highest levels of performance and scalability, and by adding them to its inventory Microlease ensures engineers have access to these powerful tools whenever they need them.

As communications networks become increasingly complex, it is essential that network operators and service providers prove their networks are operating at maximum bandwidth and throughput to ensure the best connectivity and efficiency. Ensuring installation and maintenance engineers have access to the most appropriate test equipment, through the rapid response Microlease service, gives network operators and their contractors an important commercial edge.

The two new instruments Microlease is adding to its inventory provide powerful test capabilities in the field.

www.microlease.com

0.7MM2 UHF/VHF LNAS BRINGS DIGITAL TV TO MOBILE DEVICES

Maxim Integrated Products introduces the MAX2664/MAX2665 low-noise amplifiers (LNAs) designed specifically for UHF and VHF mobile TV applications. These devices offer a fully integrated LNA solution in a 0.86mm x 0.86mm, and 0.4mm-pitch wafer-level package (WLP) with only four pins. Only requiring one external component (an input-match inductor) to complete the board-level design, the MAX2664/MAX2665 minimize solution footprint for today's continually shrinking handheld designs.

Maxim's advanced SiGe BiCMOS process enables these compact broadband LNAs to surpass the performance of today's larger competitive options. They deliver 15dB of gain, support the 75MHz to 230MHz (MAX2665) and 470MHz to 860MHz (MAX2664) frequency ranges, and offer a low 1.1dB noise figure for improved receive sensitivity over discrete and CMOS solutions. In addition, customers can expect longer battery life in their end equipment due to a low operating supply current of 3.5mA (typ). An integrated bypass switch places the LNAs in bypass mode (5µA, typ) during high-signal-level conditions to extend power savings and protect the LNAs.

www.maxim-ic.com

HARWIN ANNOUNCES NEW SERIES OF COMMERCIAL MIL-DTL STYLE CONNECTORS

High-reliability interconnect company Harwin has announced that its MIL-C-5015-style commercial connector series has been improved for increased ease-of-use. Compatible with other MIL-DTL-5015-style devices, the new C90 connectors feature re-styled rear flanges and end-bells to deliver a more streamlined profile.

Available from stock in 10SL, 12S and 14S sizes and with end caps and rubber bushing attachments to suit the entire product family, the newly-available connectors increase design flexibility. Termination options include cable, straight plug or panel mount style. Applications include mass transit, robotics, machine tools, welding equipment, extension leads, power cords and industrial and agricultural vehicles, plus COTS applications where Mil qualification is not mandatory.

End caps are available with inner or exterior thread, so it is possible either to screw the cap into or onto the connector. Rubber bushings deliver IP 67 sealing, protecting the connector from water dust and chemical ingress. End caps are manufactured from an aluminium alloy and are fully ROHS-compliant and competitively priced.

www.harwin.com

LABSPHERE'S TOCS LED MEASUREMENT SYSTEM CONFORMS TO LM-79 AND LM-80 WITH SINGLE INSTRUMENT

To more easily meet new reporting specifications, Labsphere's new Thermal/Optical/Electrical LED Measurement Systems (TOCS) enables measurement of optical properties as a function of temperature and operating current using a single instrument. The TOCS complies with IESNA LM-79 and LM-80 standards, delivering accurate and reproducible LED measurements.

Available in a range of integrating sphere sizes from 20 to 76 inches, the TOCS systems are designed for both 2pi and 4pi measurement geometries. A lamp measurement integrating sphere, high resolution CCD array spectrometer, thermal plate with temperature controller, auxiliary lamp, calibration source, power supply and Labsphere's powerful TOCS-SS software comprise the basic system. Owners of current Labsphere and SphereOptics spectral lamp measurement systems may purchase an upgrade retrofit to the TOCS system to achieve LM-79 and LM-80 compliance.

Labsphere's TOCS-SS is a powerful, accurate software which automates procedures for measuring spectral characteristics, and controlling current and temperature. Users control LED temperature and operating current at specified ranges.

www.labsphere.com

SCHNEIDER ELECTRIC UNVEILS LATEST ENERGY EFFICIENCY INITIATIVES

Solving the energy challenge requires both behavioural change and the utilisation of new technologies. Schneider Electric's commitment to solving the worldwide energy dilemma plans to dedicate the latest resources and solutions to optimize energy efficiency across the entire enterprise. So the company has introduced an industry-first customer Collaborative Project Portal, a private, online community that provides easy access to the people, information and technology to guide technical end-users through energy management projects. Free to all Schneider Electric customers, the site is the first project management tool in the industry to provide real-time access to system engineers, web meeting capabilities and social networking features to decrease costs, expedite time-to-market and boost productivity on energy management projects. Specific focus is made on the challenges of a smarter grid, EcoStruxure solutions for green buildings and the **'Save Energy, Share Energy'** initiative. "By saving energy, one can cut costs and help the environment," commented the firm's representatives.

Our panel of commentators says the following on this development:

PROFESSOR DR DOGAN IBRAHIM, THE NEAR EAST UNIVERSITY IN NICOSIA, CYPRUS:

Energy is a worldwide problem and many countries are already taking steps to improve the energy usage. Reducing energy use reduces costs and results in financial cost-savings.

Schneider Electric's initiative to optimize energy efficiency is a first in the industry and should provide savings to all electric customers. The online site should be extremely useful to system engineers and especially to technical end-users as they will have the opportunity to quickly analyze and to optimize their energy usage. The company's new online EcoStruxure solution has been developed to provide solutions to its customers at all levels of energy utilization, help reduce energy costs and, in addition, with EcoStruxure it is hoped that customers will improve their overall energy usage, reduce inefficiencies, lower their operation costs and consequently help the environment.

BURKHARD VOGEL, MANAGING DIRECTOR, GERMANY:

How nice! If I were a shareholder I would like to know the result of the respective project cost-benefit analysis. This is nothing else but marketing blah-blah and another way to catch people's attention by preventing them from work. After half a year Schneider will forget the whole stuff by starting the next and (more intelligent?) marketing attack.

There are only three things that create a long-lasting and stable customer relationship: quality of the products, quality of the service and appropriateness of the price. This is getting about and leads automatically to new customers. This would be best-in-class marketing for the capital goods industry.

MAURIZIO DI PAOLO EMILIO, TELECOMMUNICATIONS ENGINEER, INFN – LABORATORI NAZIONALI DEL GRAN SASSO, ITALY:

Energy efficiency is the most immediate and cost-effective opportunity to reduce global greenhouse gas emissions. Energy efficiency is attractive in all nations and especially in developing countries as it allows existing energy sources to serve a larger population and facilitates universal access to modern energy services – a key requirement for poverty reduction and sustainable development.

Improvements in energy efficiency can reduce the need for investment in energy infrastructure, cut fuel costs, increase competitiveness and improve consumer welfare. The global community is poised to make huge investments in very costly new electricity generation due to an exploding demand. However, energy efficiency can supply most or all of future electricity demand growth through 2030 and it is two to three times less expensive than conventional supply options.

Investments in efficiency can be profitable and create jobs. Independent system operators that allow efficiency resources to bid into capacity auctions have seen significant interest from utility and merchant providers.

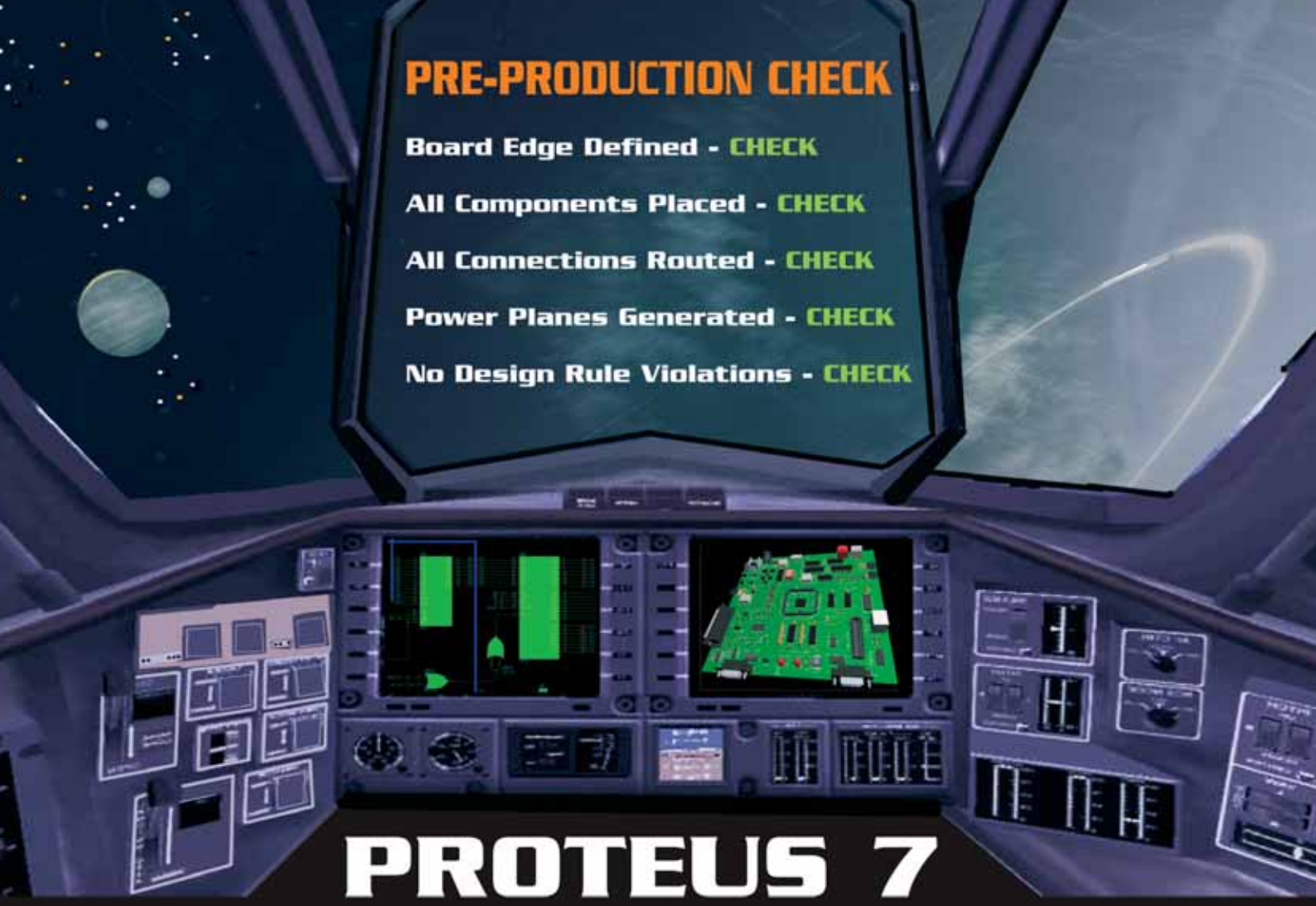
HASNAOUI OTHMAN, ASSOCIATE PROFESSOR IN POWER ELECTRONIC AT THE UNIVERSITY OF TUNIS, TUNISIA:

The decentralized production of electricity, primarily related to renewable energies, knew these last years a ceaseless evolution because they are integrated perfectly in the public network. Moreover, the evolution of new technologies of information and of communication allowed the birth of the intelligent electrical supply networks which offer an optimized management of the electric power thanks to the exchanges of information in real time with the network managers and with the intelligent meters installed by companies, administrations even private individuals.

With this technology one can avoid peak demand of energy, dangerous in several cases, and this, thanks to the systems of storage, where the electric car can play a significant role.

Any contribution in these new tendencies can be only beneficial because, in addition to the energy saving, one preserves nature and we think that a large company like Schneider or Areva is able to master these new intelligent installations.

If you'd like to comment on this subject or want to become a member of our panel, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com



PROTEUS 7

Design with Confidence:

The latest version of the Proteus PCB Design Software provides a multi-stage Pre-Production Check which will detect and prevent a variety of common mistakes prior to your boards being sent for manufacture.

PROTEUS DESIGN SUITE Features:

- Hardware Accelerated Performance.
- Unique Thru-View™ Board Transparency.
- Over 35k Schematic & PCB library parts.
- Integrated Shape Based Auto-router.
- Flexible Design Rule Management.
- Polygonal and Split Power Plane Support.
- Board Autoplacement & Gateswap Optimiser.
- Direct CADCAM, ODB++, IDF & PDF Output.
- Integrated 3D Viewer with 3DS and DXF export.
- Mixed Mode SPICE Simulation Engine.
- Co-Simulation of PIC, AVR, 8051 and ARM7.
- Direct Technical Support at no additional cost.

All levels of the Proteus Design Suite include a world class, fully integrated shape-based autorouter at no additional cost - prices start from just £150 exc. VAT & delivery

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