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ELECTRONICS WORLD

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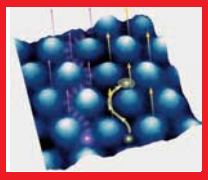

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ELECTRON ORBITS IN MULTILAYER GRAPHENE DISCOVERED

AUDIO TUTORIAL
AUDIO TESTING WITH STANDARDS IN MIND

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***Svetlana Josifovska,** Editor, Electronics World*

FEATURES

REGULARS

Cover supplied by RS COMPONENTS More about DesignSpark on pages 8-9

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Drive any 5-50Vdc, 5 Amp bi-polar stepper motor using externally supplied 5V levels for STEP and DIRECTION control. Opto-isolated inputs make it ideal for CNC applications using a PC running suitable software. Board supply: 8-30Vdc. PCB: 75x85mm.
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See website for full range of PIC & ATMEL Programmers and development tools.

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JDSU PREDICTS OPTICAL COMMUNICATIONS TRENDS FOR 2011

Components and systems that evolve the transport layer of networks will be developed in 2011.

BY SINCLAIR VASS

The end goal of these new optics will be to create self aware networks that have a flexible photonic layer and can knowingly adapt to changing traffic patterns, new applications and unexpected bandwidth fluctuations in a very seamless way.

The big three industry buzz words – colourless, directionless and contentionless – are an important part of self aware networks, providing functionality that allows any type of wavelength to travel across the network in any direction and to any desired end destination.

New sophisticated optical switching components are being developed to construct network and node architectures which provide automated end-to-end wavelength, transponder and route flexibility. These new components and architectures will continue to build upon and complement the wavelength selective switch (WSS), which will continue to be the central building block for flexible optical networks.

The interest and attractiveness of functionally-integrated optical circuit packs that integrate more optical functionality and hardware into a smaller size product will continue to accelerate adoption with network equipment manufacturers (NEM) development processes. Such line cards have already proven to provide significant cost and density advantages through integration at a sub-module level.

Expect to see a transition to self aware networks that contain these optical elements in the 2013 and 2014 timeframe.

2011 is the year that 40G networks go mainstream, as price points go down and bandwidth skyrockets. 40G coherent modulation schemes will increase the length of network links and act as a precursor for volume deployment of 100G coherent modulation schemes.

The 100G market will follow close behind 40G as major NEMs demonstrate in house solutions and start to deploy first networks, while also looking to outsource second generation designs to optical component vendors. In fact, many in the industry believe that 100G will take off very strongly in 2011, capturing a large fraction of the high speed market and curtailing growth of 40G significantly.

When it comes to 100G client side formats, two camps are forming. Brocade, Google, JDSU and Santur announced in December 2010 the formation of a 10X10 Multi Source Agreement, a format where 10 channels at 10G function in parallel to support 100G transmission speeds. Other players are supporting a 4X25G architecture, though there are questions being raised about the overall cost effectiveness of this solution.

In the line side 100G space, a widely supported coherent transmission solution is being adopted for new bandwidth deployments with first networks currently going live. This is driving demand for a new range of high-speed optical components including modulators, narrow line width lasers and passive multiplexing solutions.

Sinclair Vass is Senior Director of Marketing and Business Operations at JDSU

> **"GESTURE RECOGNITION IS ONE EXAMPLE OF A NEW MARKET THAT MADE A BIG DEBUT AT THE END OF 2010 IN GAMING"**

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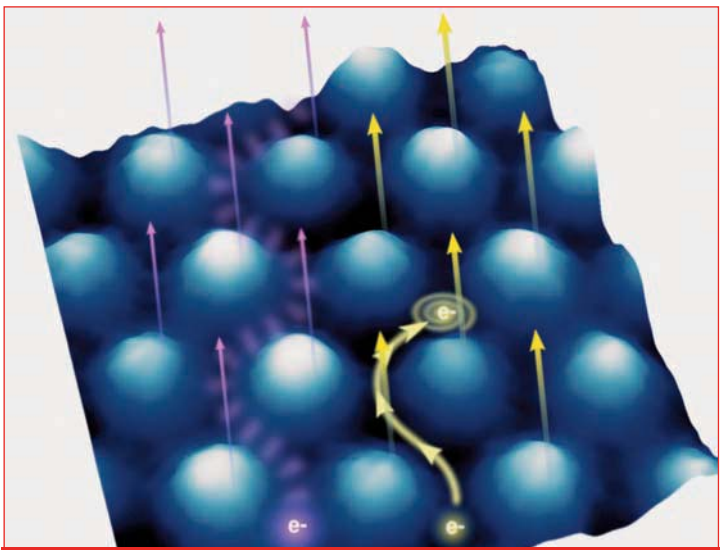
Study of Electron Orbits in Multilayer Graphene Finds Unexpected Energy Gaps



Graphene orbits as observed by a team of researchers at the Georgia Institute of Technology

Researchers at the Georgia Institute of Technology, US, have taken one more step toward understanding the unique and often unexpected properties of graphene, a two-dimensional carbon material that has attracted interest because of its potential applications in future generations of electronic devices.

The research team has seen for the first time how the orbits of electrons are distributed spatially by magnetic fields applied to layers of epitaxial graphene. They also found that these electron orbits can interact with the substrate on which the graphene is grown, creating energy gaps that affect how electron waves move through the multilayer material. These energy gaps could have implications for the designers of certain graphene-based electronic devices.

"The regular pattern of energy gaps in the graphene surface creates regions where electron transport is not allowed," said Phillip First, professor at the Georgia Tech School of Physics and a member of the research team. "Electron waves would have to go around these regions, requiring new patterns of electron wave interference. Understanding such interference will be important for bi-layer graphene devices that have been proposed and may be important for other lattice-matched substrates used to support graphene and graphene devices."

In a magnetic field, an electron moves in a circular trajectory – known as a cyclotron orbit – whose radius depends on the size of the magnetic field and the energy of electron. For a constant magnetic field, that's a little like rolling a marble around in a large bowl, said First.

"At high energy, the marble orbits high in the bowl, while for lower energies, the orbit size is smaller and lower in the bowl. The cyclotron orbits in graphene also depend on the electron energy and the local electron potential – corresponding to the bowl – but until now, the orbits hadn't been imaged directly."

Placed in a magnetic field, these orbits normally drift along lines of nearly constant electric potential. But when a graphene sample has small fluctuations in the potential, these "drift states" can become trapped at a hill or valley in the material that has closed constant potential contours. Such trapping of charge carriers is important for the quantum Hall effect, in which precisely quantized resistance results from charge conduction solely through the orbits that skip along the edges of the material.

FREESCALE CHARGING TECHNOLOGY HELPS PUT AN END TO "VAMPIRE" ENERGY LOSS

Freescale Semiconductor is finding innovative ways to stop "vampire" energy loss, the loss of power that occurs when an AC adapter is plugged into an electrical outlet but isn't charging a device. Its new Watt Saver technology automatically eliminates no-load power consumption for AC adaptors, potentially providing substantial energy savings over existing manual versions.

Freescale's Watt Saver technology consists of patent-pending hardware and software implementations enabling the main power source to be disconnected when no power is required by the connected device. This technology can apply to numerous battery-powered consumer devices.

"With approximately four billion users of rechargeable cell phones, the annual amount of vampire energy lost by AC adaptor chargers totals more than $1bn of wasted electricity or 1,200MW of power, which is about the size of a modern nuclear plant," said Jeff Bock, director of product marketing for Freescale's Industrial and Multi-market segment. "Most people have no idea how much energy they are wasting through the use of older charging devices. By monitoring the power needed by the charging device and stopping that power once it's no longer needed, we are able to make a considerable impact on the amount of energy wasted and ultimately provide real savings for our customers."

According to a report by the International Energy Agency and the European Union, it is estimated that vampire power accounts for more than 10% of the electricity used in homes and offices and it will continue to rise to 49TW hours by 2014, burning as much electricity as the combined electricity consumption for Austria, the Czech Republic and Portugal. It is expected that the energy consumed by information, communications and consumer electronics will double by 2022 and triple by 2030.

Watt Saver charging can be applied to a variety of charging products including mobile device chargers, extra power back-up chargers, wireless charging stations and AC powered equipment. With Freescale Watt Saver technology, a universal power adapter conforming to the ITU-T L.1000 recommended standard can be designed with a zero Watt, no-load power consumption. The eco-friendly charger uses no more energy than needed to charge its device and it has a longer useable life because it can potentially be used with any new device.

Novel Nanomaterial System Will Help Create Materials of the Future

Surrey NanoSystems has announced the first sales of its innovative new nanomaterial growth system, the NanoGrowth-Catalyst, to the École Polytechnique of Montreal and the University of Surrey's Advanced Technology Institute.

These leading research organisations have chosen the NanoGrowth-Catalyst as a platform for their work on materials including carbon nanotubes, silicon nanowires, graphene and nanoparticles for semiconductor, optical device and other applications. The growth system's multi-chamber design ensures the purest nanomaterial processing conditions by continuously maintaining the substrate under vacuum, from the deposition of catalysts to growth of materials.

Surrey NanoSystems has announced several orders for its versatile growth platform for nanomaterials, NanoGrowth Catalyst

One NanoGrowth-Catalyst system will be installed in Montreal, where it will support a wide range of research groups from the École Polytechnique and The University of Montreal studying topics including microelectronics, optoelectronics and thin film physics.

This system will be populated with every major processing facility available, including three processing chambers served by an automated handling system, and growth techniques, including CVD, PECVD, nanoparticle deposition, sputtering, thermal annealing and rapid thermal processing. It will also incorporate a unique form of rapid thermal growth for nanomaterials developed to prevent the agglomeration of catalyst particles.

One research group using the system will be the University of Montreal's chemistry department, led by Professor Richard Martel. The group's interests are very broad ranging and include device-oriented programs looking at electronics, optoelectronics, sensing technologies and energy conversion, and fundamental research into the phenomena occurring at the interfaces of electroactive nanostructure materials – through projects including the deposition of controlled-size nanoparticles and passivation layers.

■ According to Sector Skills Council Semta, the UK's 143,300 electronics employees produce an average of £59,300 Gross Value Added (GVA), compared to a UK average of just £35,500. The data reiterates the important contribution the sector is making in rebalancing the UK economy. However, the electronics industry has a greater than average number of skills gaps within its organisations – 21% of companies compared to 19% across all sectors. Semta's research predicts that 1,500 extra people will be needed between now and 2016 to cover employment growth and retirements within the sector. The sector's priorities as outlined by Semta need to be technical skills training including apprenticeships, leadership and management, productivity and competitiveness and strategic workforce planning.

■ Ann Watson, Managing Director of specialist engineering and manufacturing awarding organisation EAL, has called on the UK government to put vocational training on a par with its academic counterpart.
"The last two years have seen a dramatic shift in the way Government has viewed apprenticeships. For too long now, this country channelled our brightest and best down the degree route, suggesting it was the only option. As a country, we need to ensure that both university and vocational training are promoted equally to young people."

Breakthrough in Low Temperature Growth of Carbon Nanotubes

Researchers at the University of Surrey have discovered a way to grow high-quality carbon nanotubes over large areas at substrate temperatures below 350°C. This means that lowering the substrate temperature below 400°C would make this technology compatible with CMOS – which is currently used to make integrated circuits – and suitable for large area substrates. As a result, potential applications of carbon nanotubes would become feasible and affordable if the growth temperature of the substrates were to be reduced from its current 700°C.

The breakthrough reported by Professor Ravi Silva's group at the University of Surrey allows researchers to couple plasma energy more efficiently to the catalyst particles used to grow carbon nanotubes. The researchers have demonstrated that high-quality carbon nanotubes can be grown controllably, reliably and over large areas while maintaining the device substrates at low temperatures.

Dr Vlad Stolojan, part of the research team, explained the technology used: "Currently the metallic interconnects based on the metal copper used in integrated circuits suffer from poor electrical conduction and the smaller they get in diameter the more resistive they become. In addition to the electromigration issues, they dissipate so much heat energy that they can damage the surrounding devices. With our innovative technology, using a top-down heating methodology, we can precisely grow carbon nanotubes within interconnect vias at CMOS compatible temperatures."

University of Surrey team makes a carbon nanotubes growth breakthrough

Carbon nanotubes are rolled up sheets of honeycomb-structured carbon atoms that are typically ten thousandth the width of a human hair or hundred thousandth of a millimetre in diameter. The single or multi-walled carbon nanotube structures have amazing electronic properties with conductivity better than any other known single element material, including copper, thermal conductivity better than diamond, and extraordinary mechanical strength surpassing that of high tensile steel.

High-tech design goes VIRTUAL

RS embraces the online design paradigm at Embedded World

INCREASINGLY, advanced products are taking shape on the web, transforming into a physical object late in the process as the completed streams of information converge. RS Components is addressing this new paradigm by delivering a new range of free design resources, and by partnering with market-leading technology businesses in the embedded field. Our mission is to help engineers and buyers find, design and buy the right products to achieve their end-product realisation. At Embedded World in Nuremberg, all of the elements that contribute to this mission have been brought together on the RS stand.

DESIGNSPARK PCB V2.0

DesignSpark PCB has attracted tens of thousands of downloads since its launch nearly a year ago. In that time, thousands have contributed suggestions to how to enhance their user experience, pack in more functionality and further reduce design times. The result is DesignSpark PCB v2.0; the first significant upgrade for DesignSpark PCB since its launch last summer. Based on the most popular enhancements recommended by users, DesignSpark PCB has been strengthened in three key areas. It offers new library features and output options for text and graphics. Functionality has also been enhanced through the Project menu items, while visualisation features such as a new 3D view of the PCB and its components help extend the tool's usability.

DesignSpark PCB remains unique in the industry by offering a fully featured, unrestricted PCB development environment that is free to download and use. With no restrictions on the size of the PCB or the number of layers used, DesignSpark PCB has rapidly become the engineer's choice and with the release of v2.0, RS reinforces its commitment to maintaining that position.

PARTNERSHIP APPROACH

A key part of RS success over the past year has been its ability to partner with market leading technology companies like ARM, Arduino and TI to add value to its customers design journey. For example, RS Components is sponsoring internships with the ARM® mbed team to develop mbed hardware and software reference designs that are featured on DesignSpark. The latest design, a breakout audio board, is being shown at Embedded World in Nuremberg, together with its complete design journey. The journey is also being posted on the DesignSpark online community for electronics engineers. RS was also the first global catalogue distributor to support the cult Arduino electronics prototyping platform for creating interactive objects or environments.

Visitors to RS at Embedded World in Nuremberg can follow a virtual design journey every step of the way: from finding the right components to put on the Bill of Materials, through to design of the circuit diagram online on DesignSpark PCB to buying components for the breadboard stage to programming, testing and finished product.

In partnership with Texas Instruments and ARM, technical engineers from RS realised a breakout audio board based on Texas Instruments TLV320AIC32 audio code: the latest module in the mbed program online using DesignSpark PCB. Embedded code development using the online mbed flow and testing using a Tektronix MSO2024 200MHz Mixed Signal scope were also part of the demonstration. The schematics and PCB layout for the design will be posted to the DesignSpark site.

ONLINE: THE NEW DESIGN PARADIGM

Internet-based technical resources can simplify traditionally difficult and time-consuming processes such as collecting information, comparing data presented in different formats by competing manufacturers, and making buying decisions. 2010 saw RS deliver its biggest ever upgrade to its online presence. DesignSpark is the hub of this effort. DesignSpark PCB, SparkStore, 3D models, Component Chooser and eTech itself are all part of that program. Partnerships with ARM, TI, Arduino and many more are further manifestations. 2011 will see us travel further down that road. Watch this space.

Find out more at www.rs-components.com, and download DesignSpark PCB for free at www.designspark.com/pcb

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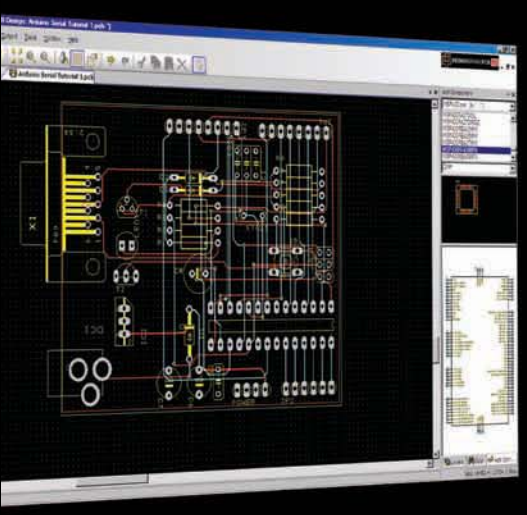

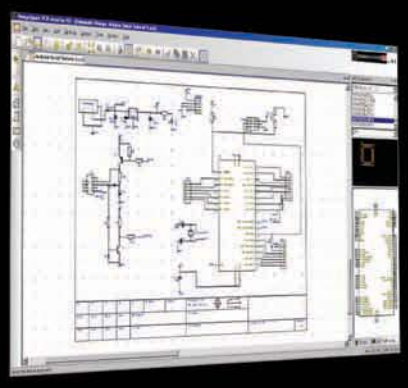

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LTE Indoors – Consolidating Network Services Under the SAME ROOF

Håkan Samuelsson, the Chief Technology Officer at Axell Wireless, explains how SDR and digital filtering in repeaters will enable operators to simultaneously deliver LTE and existing network standards

IT HAS BECOME fashionable over the last few years for mobile network operators to engage in shared infrastructure projects. The most recent high-profile network sharing project is the merger between 3 UK and T-Mobile to consolidate their 3G networks, which has seen the configuration of all 3G base stations, transmitters and core network elements on an enormous scale, spanning a network of 12,000 sites. Bringing the two networks together was an impressive feat of microwave engineering.

Orange, SFR and Bouygues Telecom recently announced that it would jointly roll out an HSPA+ network in rural France. Meanwhile, German mobile operators are having discussions about the possibility of rolling out of a joint LTE network in the country.

This model of network deployment became popular with operators throughout Europe following the emergence of third generation (3G) networks that support mobile broadband access. Network sharing provides operators with economies of scale and helps to reduce costs when major upgrades are required. If this model can be adopted by operators to consolidate the wider macro network, then it makes sense to apply it to other network environments such as in-building.

The high costs associated with migrating to fourth generation technology, such as LTE that has the capability to deliver a 100+ Mbit/s in downlink, will also force mobile operators to find savings by sharing their infrastructure. However, according to research conducted by Analysys Mason, over 80% of global wireless data traffic will be generated indoors by 2016.

The demand for high-speed mobile broadband and data services will be concentrated to public spaces, such as coffee shops, shopping malls or offices, where people have the opportunity to stop and browse the internet, check emails and stream video. The challenge now faced by RF and microwave engineers is how to deploy robust systems that are capable of dealing with multiple users in a small area all wanting to access and transmit large amounts of data. In addition, there are a number of topographical challenges to consider. LTE will be subject to the same problems that impact on 2G and 3G networks, most notably the signal degradation and deflection caused by solid objects such as walls and roofs.

So, how should engineers approach this issue to ensure wireless connectivity for LTE in-building, and squeeze more capacity, and benefit, out of existing spectrum allocations?

One approach would be to deploy dedicated LTE base stations, but installing new equipment can be a costly and time consuming process, even for small scale indoor deployments when backhaul costs are added. Picocells are adequate for providing coverage for wireless hotspots, but they are also capacity limited and prone to overload if too many users want access at the same time. Wi-Fi and femtocell offload have proved to be effective for residential application, but neither of those solutions scale for major in-building implementations, either in terms of the number of concurrent users that can be supported or in the desired quality of service parameters.

In order to deliver reliable and consistent indoor coverage operators are adopting sophisticated digital repeaters connected to a Distributed Antenna System (DAS) that propagates signal throughout the building. A single repeater linked to a roof mounted donor antenna, or to a dedicated base station, can 'drive' a DAS providing coverage for 100,000 square feet. The result is a cost-effective solution that provides universal coverage for mobile users and data transfer capabilities that are the equal of uninterrupted outdoor connections. The system ensures that subscribers remain on the cellular network without having to reconfigure connections for data offload onto a fixed line network and dramatically reduces the risk of network overload.

By adopting a software-defined-radio (SDR) approach RF engineers will be able to accommodate future developments and enhancements in network functionality without having to replace older equipment. RF engineers can remotely change the radio standard that network components operate on simply by installing new software. The migration to LTE won't be taking place overnight and so the repeater needs to be multiband, able to simultaneously handle 2G and 3G network connections and potentially, those frequencies set aside for dedicated emergency services use. Remote monitoring and configuration is important as is the unit's ability to take account of standards variations, spectrum availability and the individual requirements of operators. In that potentially complex mix of requirements software-defined-radio is becoming a vital component in the deployment of next-generation wireless networks.

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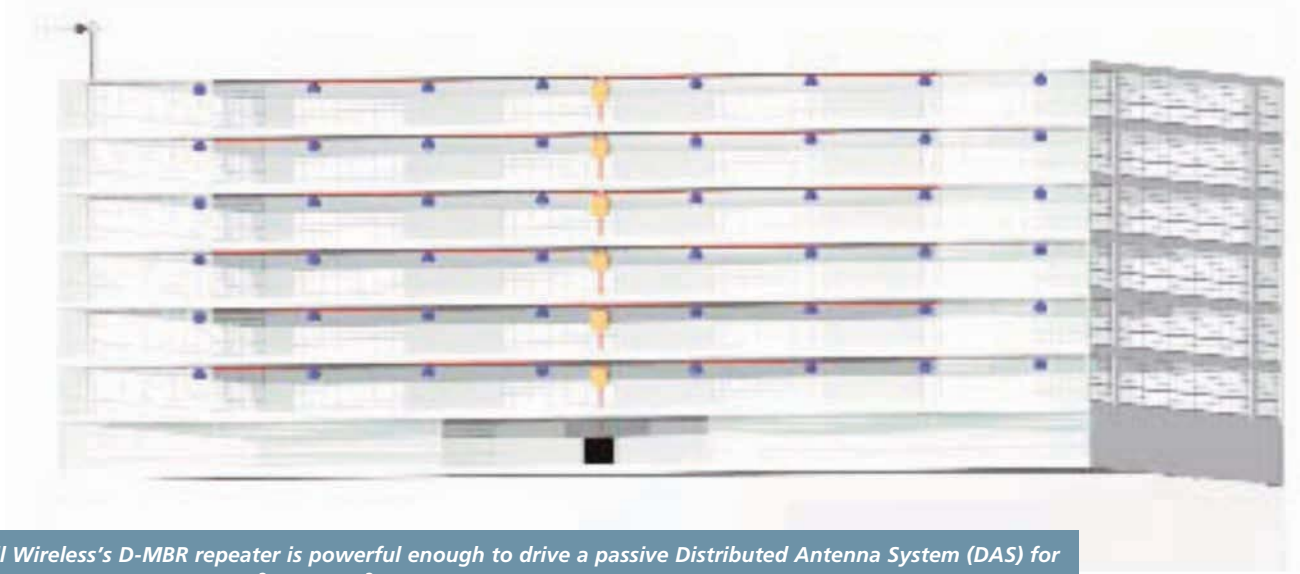


Axell Wireless's D-MBR repeater is powerful enough to drive a passive Distributed Antenna System (DAS) for coverage areas over 100,000ft² (10,000m²) in buildings, parking lots, malls, warehouses and offices

the repeater is serving the subscribers of a single carrier, the system needs to ensure that the repeater only amplifies signals from that operator's basestations and rejects those from other networks. Traditionally that was achieved through the use of surface acoustic wave (SAW) filters but SAW filters have temperature dependent filter characteristics. The pass band drifts in frequency with temperature which becomes a problem in repeater applications where the filter skirts should be able to reject frequencies very close to the pass band.

The ideal filter for repeater applications should have a flat low-loss pass-band over all frequencies belonging to the operator, but should reject all other frequencies. At the same time, the propagation delay through the filter should be minimal with very low ripple within the pass band. If more than one pass-band needs to be amplified (several operators share one repeater or one operator has more than one allocation of spectrum), the repeater must be equipped with several SAW filters working in parallel which amplifies the potential issues. SDR technology meets all the requirements to make it possible to design frequency-stable filters with performance far exceeding analogue SAW filters and which are also programmable in centre frequency and bandwidth.

SDR also makes it is possible to download new field-programmable gate array (FPGA) code to the repeater if a new set of filters are to be implemented. In fact, if the repeater is equipped with an FPGA with sufficient capacity, several sets of filter parameters can be stored and called up at will. This makes the repeater very flexible, as new requirements (more bandwidth, support of a new radio technology etc.) can be immediately implemented to upgrade repeater functionality.

Digital multi-band repeaters, employing SDR, are changing the way operators address in-door coverage for commercial environments. The multi-megabit connection requirements for LTE are demanding, but they can be effectively and efficiently addressed by an established mobile network technology that has now been significantly enhanced. Although individual operators can deploy the equipment for their own dedicated use the system lends itself to innovative micro-network sharing arrangements.

You can understand the appeal of network sharing projects. They enable operators to reduce capital expenditure by sharing network infrastructure such as cell sites, radio masts and the sharing of radio access networks (RANs). By sharing a single network, operators are able to compete on price, services and mobile content, rather than geographic coverage.

For in-building purposes mobile operators are now in a position to consolidate their networks by deploying multi-band repeaters that can be configured remotely to support a wide range of frequency bands to meet the increasing consumer demand for mobile broadband, while still providing reliable coverage for voice and data services. Sharing infrastructure also reduces installation costs and the disruption to commercial buildings or public spaces caused by engineers and maintenance teams.

Apart from the benefits of adopting a collective approach to deploying network equipment indoors to support multiple users and frequency bands, another key benefit for operators is that this system also compensates for the significant increase in backhaul demands placed on a network by LTE. The increased data rates associated with LTE require a dedicated fibre connection or a very high data rate microwave link. Laying a direct fibre connection to support wireless connectivity in an office block, or a shopping mall, can be expensive. Operators can successfully distribute coverage and capacity throughout a building using an over-the-air repeater, which uses the licensed wireless spectrum as network backhaul, removing the need for a direct fibre connection.

The deployment of repeaters has always been perceived as a temporary solution. The shortfalls commonly associated with repeater technology such as interference, noise and sensitivity reduction have been addressed and developments in digital signal processing have solved performance related issues. SDR adds an entirely new dimension that makes repeaters a long-term solution – not just a temporary fix. So much so that for the next release of the LTE standard the industry is considering the integration of repeaters, relay nodes, as a standard network element. ■

Embedded World Exhibition and Conference Products – March 2011

FIRST MEMS-BASED PROGRAMMABLE CLOCK GENERATOR WITH LVCMOS AND DIFFERENTIAL OUTPUTS

MSC expands its existing clock generators product offering with the SiT9105 from SiTime. The SiT9105 is the first MEMS-based programmable clock generator that combines LVCMOS and differential outputs in a single package, thus reducing board area by up to 66%.

The SiT9105 can generate up to three unrelated frequencies. This includes two frequencies on single-ended outputs (up to two copies of each frequency) and one on the differential output. The device support LVDS, LVPECL or HCSL signalling levels. The SiT9105 can be programmed to generate any frequency outputs from 1MHz to 220MHz with 5 decimal places of accuracy. The frequency stability is as low as ±25PPM.

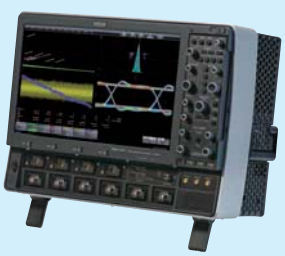
The SiT9105 operates from 1.8V, 2.5V or 3.3V. Each output can operate off a different voltage, eliminating the need for external level translators.

By combining resonator, multiple timing components as well as single-ended and differential outputs on a single chip, the SiT9105 ensures the highest levels of reliability and economic efficiency.

HALL 9, STAND 643 **www.mscge.com**

WAVEPRO 7 ZI-A SERIES 1.5GHZ–6GHZ OSCILLOSCOPES

LeCroy's new line of WavePro 7 Zi-A oscilloscopes with bandwidth ranging from 1.5GHz to 6GHz integrates performance, speed and a user interface optimized for analysis to enhance the design, debug and validation process beyond any other instrument in its class. Powerful feature finder, rare event capture technologies and the deepest toolbox combine for powerful debug capability. Exceptional responsiveness and extremely fast processing throughput lead to more efficient validation. The largest display available in any oscilloscope makes finding the root cause easier.



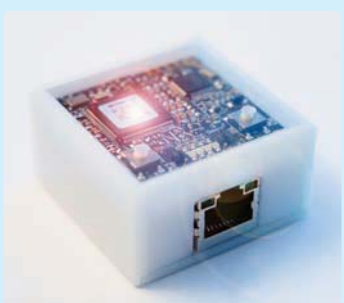
The WP7 Zi-A provides a high sample rate of 20GS/s on all 4 channels and 40GS/s interleaved; long record length (20Mpts/ch standard – 32Mpts/ch for SDA – up to 256Mpts optional); both 1MΩ and 50Ω inputs in all models; and a wide variety of probes and options, the 7 Zi-A Series allows engineers to solve any design challenge.

WavePro 7 Zi makes long acquisition memory a pleasure to use with X-Stream II fast throughput streaming architecture, available exclusively from LeCroy.

HALL 10, STAND 208 **www.lecroy.com**

ARROW SHOWCASES EMBEDDED PLATFORM CONCEPT MODULES AT EMBEDDED WORLD

Arrow Electronics will be showcasing development modules based on the Arrow Embedded Platform Concept (EPC) at Embedded World, Nuremberg. EPC continues to expand with new hardware, software and engineering services designed to deliver system solutions for a wide range of potential industries and enable the rapid market launch of new applications.



The modules on display will include the Arrow 'CUBE' embedded networking reference design, EPC XKIT02 and XKIT03 starter solutions, an Add-On module that adds display capabilities to EPC processor boards, and a DC/DC board.

Based on an ARM Cortex-M3 processor, the Arrow CUBE is a power-over-Ethernet demonstrator that enables Ethernet networking connection without complex configuration tasks. The stand-alone processor board is supplied with energy via either Ethernet or USB and is equipped with light and temperature sensors. An integrated web server allows for control via an Internet browser, eliminating the need to install any PC-based applications.

HALL 12, STAND 366 **www.arrowerurope.com**

ADLINK TECHNOLOGY INTRODUCES 12-COM-PORT FANLESS EMBEDDED COMPUTERS

Adlink Technology announced the release of the MXE-1200, an industrial and rich I/O fanless embedded computer with enhanced RF functions and LVDS and VGA dual display geared specifically for versatile applications such as intelligent transportation, factory automation, home security, environmental monitoring and research. The MXE-1200 retains all the optimal advantages of the Adlink Matrix series, including a rugged fanless operation from -20°C to 70°C, 5 Grms vibration resistance, an Ethernet port and 6-36 VDC wide range power input.

The MXE-1200 series is a compact-size 210mm (W) x 170mm (D) x 54mm (H) I/O platform and suitable for operating in a relatively limited storage space. The cable-free architecture and wide temperature range of the MXE-1200 greatly benefits customers who require compact and reliable computing solutions and a lower maintenance cost of systems.

Featuring Rich I/O and RF support, two of the 12 COM ports can be configured to RS-232, RS-422 or RS-485 via a BIOS setting.

HALL 9, STAND 245 **www.adlinktech.com**

HIGH-PERFORMANCE PICMG 1.0 SLOT CPU WITH INTEL GM45 MOBILE CHIPSET

DSM Computer's current industrial Slot CPU 96M4296o conforms to the proven and still very popular PICMG 1.0 Standard. The compact CPU card is equipped with an Intel Core2 Duo (Penryn) processor with the 667/800/1066MHz front-side bus or a Celeron processor and the Intel GM45/ICH9M chipset with the Intel Graphics Media Accelerator 4500MHD. The module can be equipped with two DDR3 SO-DIMM memory modules that have a maximum capacity of 8GB. This makes the Slot CPU 96M4296o, DSM Computer's most powerful mobile platform in this form-factor.

The PICMG 1.0 plug-in card offers a number of standard interfaces, in particular the two fast GigaBit LAN interfaces that permit a wide range of applications in the various markets. In addition there are eight USB 2.0 ports, GPIO, IrDA, HD audio and IDE as well as three SATA II with 300MB/s data transfer rate among others.

HALL 12, STAND 208 **www.dsm-computer.com**

HALOGEN-FREE DDR3 MEMORY MODULES OF APACER

Apacer Technology adopted halogen-free materials in its products and developed halogen-free DDR3 memory modules. All parts, materials and processes of these products do not contain halogen atoms. By doing so, Apacer commits to play a part in supporting global ecology and environmental protection, as well as in preventing the possible generation of hazardous substances.

The halogen-free DDR3 memory modules newly launched by Apacer include UDIMM and SO-DIMM. Available in capacities from 1GB to 4GB, both products boast a bandwidth of up to 1333MHz/second and are strictly controlled to meet the IEC 61249-2-21 requirements.

Apacer provides not only the modules specialized for various application markets but also technologies for different specifications. All its products have been tested in harsh environments (long-term experiment under high and low temperature and pressure), and undergone an actual motherboard testing procedure. Approved by OEM leaders, Apacer products are the first choice for enterprises that look for professional storage solutions.

HALL 9, STAND 580 **www.apacer.com**

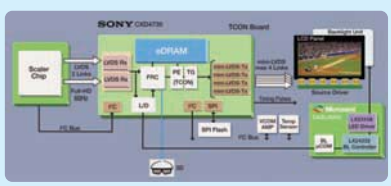
MICROCHIP ADDS NEW COST-EFFECTIVE MEMORY OPTIONS TO 32-BIT PIC MCUs

Microchip announces a new, six-member family of 32-bit PIC32MX5/6/7 microcontrollers that provides the same integrated Ethernet, CAN, USB and serial connectivity peripherals with new, more cost-effective memory options. Additionally, design enhancements also provide lower power consumption of 0.5mA/MHz active current, higher Flash memory endurance of 20k read/write cycles and better EEPROM emulation capability. By maintaining common pin-outs, the PIC32 portfolio also provides designers with the optimum balance of memory and cost for their high-performance applications as well as a seamless migration path for scalability and flexibility.

The latest 80MHz PIC32 microcontroller family helps embedded designers to lower their costs without sacrificing performance or functionality. The raw performance of the MIPS32 M4K core has been maximised to achieve best-in-class performance of 1.56DMIPS/MHz, with integrated Ethernet, CAN, USB and multiple serial communication channels, in addition to more cost-effective memory options. The family provides 32kBytes of RAM and up to 140kBytes of Flash.

HALL 9, STAND 451 **www.microchip.com**

TIMING CONTROLLER PLUS LED BACKLIGHT SOLUTION FOR NEXT-GENERATION 3D LCD TVS



Microsemi Corporation announced collaboration with Sony Corporation Semiconductor Business Group for the first open market 3D-capable timing controller plus local dimming LED backlighting solution for the manufacturing of lower cost, high volume next-generation LCD TVs. The combined solution includes a Sony timing and lighting controller, part number CXD4730GB and the Microsemi LED driver solution consisting of two chips, the DAZL!2000 series 32-port logic chip (LX24232) and 8-port LED driver power chip (LX23108L).

The complete turn-key reference design draws on Sony's powerful video and light processing technology and Microsemi's DAZL! LED drive technology, enabling the production of superior, high quality 3D and 2D images using LCD panels from a wide variety of manufacturers. The combined technologies allow lower cost 60Hz refresh LCD panels to produce the image quality of more expensive 120Hz panels and enable 120Hz panels to match the image quality of costly state of the art 240Hz panels.

HALL 12, STAND 329 **www.microsemi.com**

COM EXPRESS MODULE BOASTS QUAD-CORE PROCESSOR, USB 3.0 AND DIGITAL DISPLAY INTERFACES

Parallel to the launch of the second generation Intel Core processor family, Kontron introduced the COM Express basic form-factor ETXexpress-SC Computer-on-Module. They are the first Computer-on-Modules with an Intel Core i7 2715QE quad-core processor, Intel Mobile QM67 I/O Hub and USB 3.0. Additionally, they feature the fastest Intel graphics on the market.

The new Computer-on-Modules are available with the Type 2 or Type 6 Pin-out of the PICMG COM Express rev. 2.0 specification, increasing the speed of new designs and upgrades. With new features such as enhanced Intel Turbo Boost Technology, Intel Advanced Vector Extensions and Kontron Embedded Application Programming Interface (EAPI) middleware, OEMs will benefit from improved performance and simplified application development.

The Kontron ETXexpress-SC Computer-on-Modules integrate the new monolithic Intel microarchitecture with a CPU, graphics and ECC memory controller as well as a PCI Express controller all on an energy-efficient 32nm die. There's a performance gain of 205% for the CPU and a 170% graphics performance improvement.

HALL 12, STAND 404 **www.kontron.com**

Speech Generation using Pulse Width Modulation (PWM) with AVR MICROCONTROLLER

In this article, **Muhammad Yasir** discusses a basic mechanism behind speech generation using Pulse Width Modulation (PWM) with 8-bit AVR microcontroller

WITH ADVANCEMENT in micro-controller technology it has now become possible to generate speech using Pulse Width Modulation (PWM) feature of AVR microcontroller instead of using some specialized audio chip or DSP processor. This article discusses basic mechanism behind speech generation using Pulse Width Modulation (PWM) with 8-bit AVR microcontroller.

The heart and soul of this digital voice recording playback system is an Atmel ATmega8535 microcontroller. ATmega8535 is a powerful RISC 8-bit microcontroller, with 8kB In-System Programmable FLASH memory, 512 bytes EEPROM and 512 bytes of internal SRAM. Its RISC CPU core can execute almost one instruction per cycle. The core is complemented with a rich set of peripherals, including I/O ports, timers, PWM, A/D converters, etc.

MicroSD card has been interfaced with AVR microcontroller through SPI port using the SPI protocol. The MicroSD card is commonly used in mobile phones for storing audio, video and image files. It is commonly available in market in a wide range of memory capacities ranging from tens of megabytes of storage capacity to about 8GB and even more.

Four LEDs and four push button switches have been added to the system. One push button switch is for recording the speech data on MicroSD card while the other push button switch is for playback of the recorded sound through PWM. One LED blinks while speech data is being recorded over the MicroSD card, while other LED blinks when recorded data is being played back by MCU through PWM. The other two push buttons and other two LEDs are for potential use so that features like fast forward and rewind may be added to this system.

Speech data for almost 20 seconds is recorded on the MicroSD card which is subsequently played back by pressing the play button. The audio is picked up by a condenser microphone and amplified by an LM386 based amplifier from National Semiconductor. The amplified signal is then filtered and passed to the built-in analogue-to-digital (A/D) converter of ATmega8535.The analogue speech input signal is sampled by analogue-to-digital converter at a frequency of 8kHz. Each of the speech samples generated by the A/D converter of MCU comprises 10-bits. The 10-bit speech samples are scaled down to-8 bit samples before storage.

During playback, the samples stored in the multimedia card are sent to the MCU's PWM module, which produces approximately a 16kHz (here which is actually 15.686kHz) PWM signal whose pulse width is proportional to the amplitude of the speech sample. This PWM signal is filtered, amplified and then passed to a loudspeaker for playback. The loudspeaker is driven by the amplifier circuit based on LM386.The loudspeaker used for this system is an 8Ω and 0.5W loudspeaker.

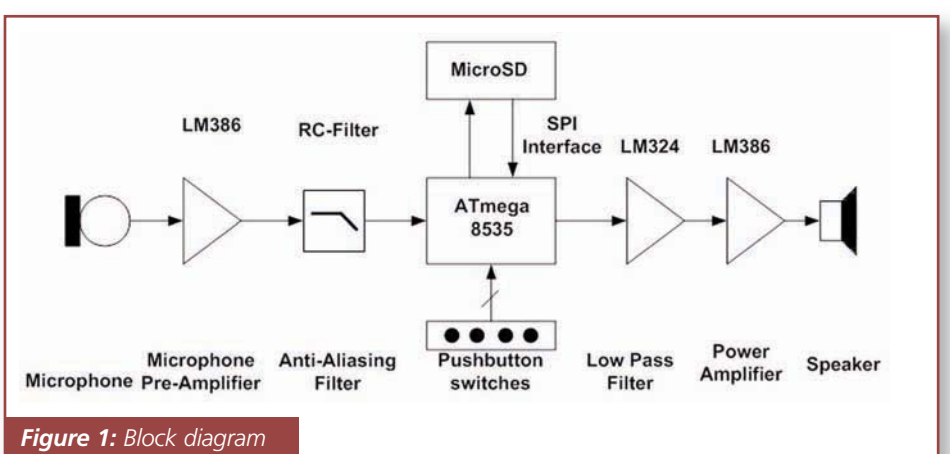


***Figure 1:** Block diagram*

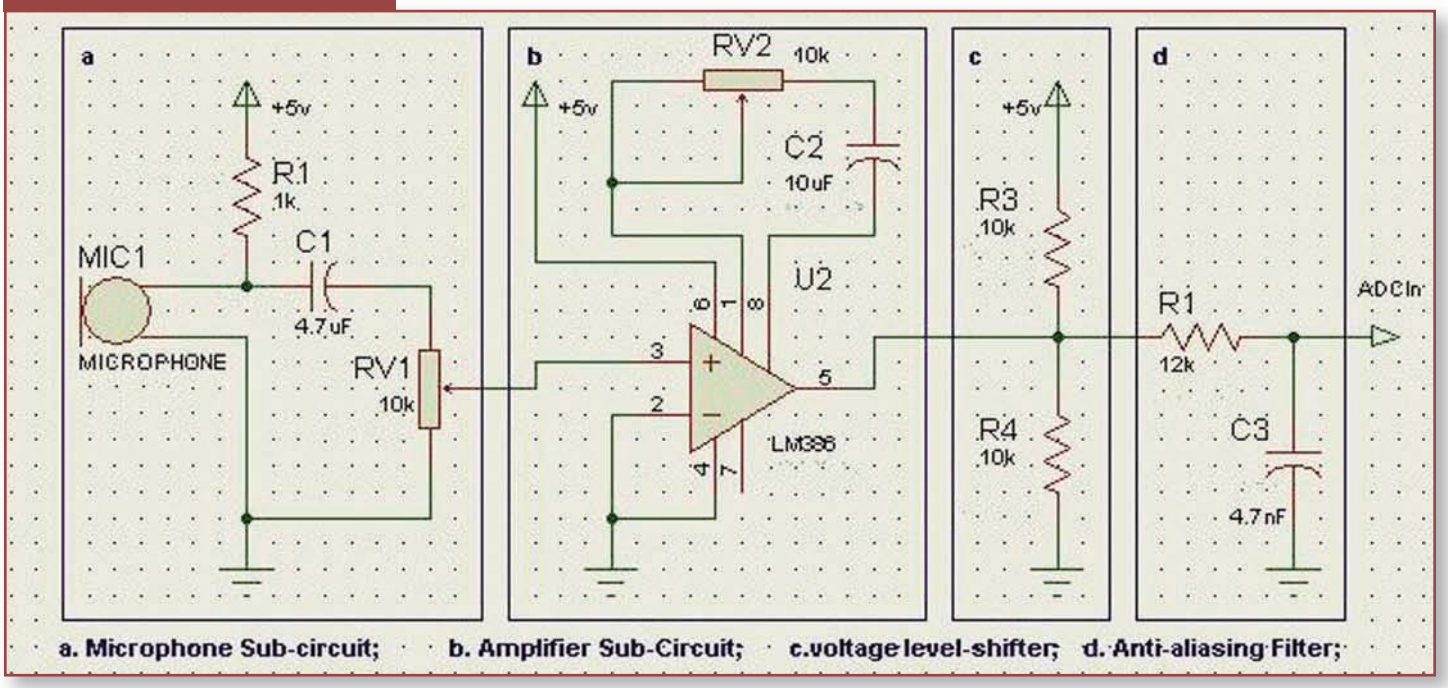
Input Amplifier and Filter

The LM386 has been used as an input amplifier. The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low. Pins 1 and 8 serve for gain control. With pins 1 and 8 open, the 1.35kW internal resistor sets the gain at 20 (26dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35kW resistor, the gain will go up to 200 (46dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24mW when operating from a 6V supply, making the LM386 ideal for battery operation.

When using the LM386 with higher gains (bypassing the 1.35kW resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1µF capacitor or a short to ground depending on the DC source resistance on the driven input.

The condenser microphone is biased using a resistor (R1) and the DC component blocked by a capacitor (C1). The variable resistor RV1 serves for volume control. While variable resistor placed in series with capacitor C2 serves for gain control of the amplifier. Maximum amplifier gain of 200 may be obtained by setting the variable resistor RV2 value to 0. The amplifier section is followed by a voltage level-shifter and an anti-aliasing filter. The anti-aliasing filter is a simple single-stage RC filter comprising R4 and C3.R4 protects the amplifier from any damage if the output is short-circuited. Different sub-circuits of the input amplifier and filter section are marked in the **Figure 1**.

Figure 2: *Input amplifier and filter*



Speech Generation Through PWM

Pulse Width Modulation (PWM) modules, which produces basically digital waveforms, can be used as cheap digital-to-analogue (D/A) converters with only a few external components. A wide variety of microcontroller applications exist that need analogue output but do not require high resolution D/A converters. Some speech applications (talk back units, speech synthesis systems in toys, etc.) also do not require high resolution D/A converters. For these applications, Pulse Width Modulated outputs may be converted to analogue outputs. Conversion of PWM signals to analogue waveforms involves the use of low-pass filters.

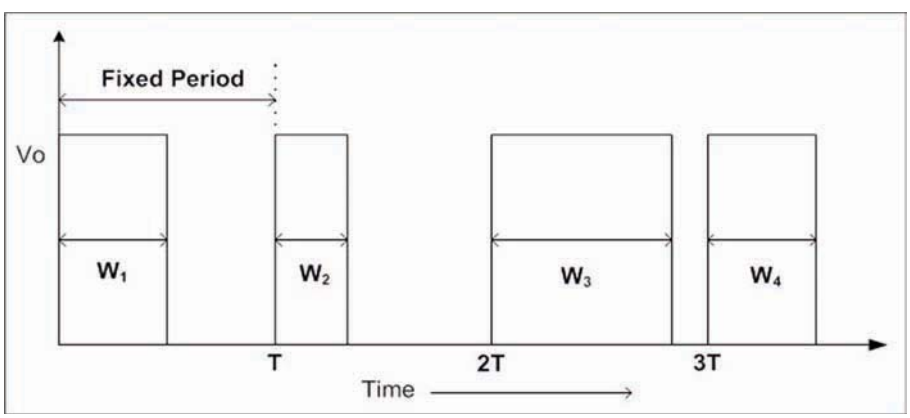
Speech signal is generated from the recorded speech samples by Pulse Width Modulation. The width of the PWM output signal is proportional to the amplitude of the speech sample. The PWM output signal proportional to the amplitude of the speech sample is generated by operating the Timer1/Counter1 of the ATmega835 in Phase Correct PWM mode. In a typical PWM signal, the base frequency is fixed, but the pulse width is a variable. The pulse width is directly proportional to the amplitude of the original unmodulated signal. In other words, in a PWM signal, the frequency of the waveform is a constant while the duty cycle varies (from 0% to 100%) according to the amplitude of the original signal. A typical PWM signal is shown in **Figure 2**.

A Fourier analysis of a typical PWM signal (such as the one depicted in Figure 2) shows that there is a strong peak at frequency Fn = 1/T. Other strong harmonics also exist at F = K/T, where K is an integer. These peaks are unwanted noise and should be eliminated. This requires that the PWM signal be low-pass filtered.

To generate PWM signal from speech samples, for playback of recorded speech, PWM module of ATmega8535 has been utilized in Phase Correct 8-bit mode (or mode1). The phase correct PWM mode is based on a dual-slope operation. This mode provides a high resolution phase correct PWM waveform generation option. For the PWM, 16-bit Timer/Counter1 is used with PWM output on OC1B pin. To compare value with Timer/Counter1 TCNT1 count value, compare register OCR1B has been used, which is loaded with the speech sample to be compared with TCNT1 either in down counting or up counting of TCNT1.

Initially the output compare register OCR1B is loaded with 0 as soon as the Timer/Counter1 overflows the output compare register OCR1B is loaded with the speech sample. Depending on the mode of operation used, the counter is cleared, incremented, or decremented at each timer clock (clkT1). The clkT1 has been generated from an internal clock source without pre-scaling by configuring the Timer/Counter Control Register B (TCCR1B). The timing sequence of the Timer/Counter1 is determined by setting the Waveform Generation Mode bits (WGM13:0) located in the Timer/Counter Control Registers A and B (TCCR1A and TCCR1B). For running PWM at the highest possible frequency, the PWM clock divider is set to 1. In this article Waveform Generation Mode1 has been chosen at the highest possible frequency.

The counter counts repeatedly from BOTTOM (0x0000) to TOP (0x00FF) and then from TOP to BOTTOM. In non-inverting Compare Output mode, the Output Compare (OC1A/ OC1B) is cleared on the Compare Match between TCNT1 and OCR1A/OCR1B while up-counting and set on



Figures 3: *A typical PWM waveform*

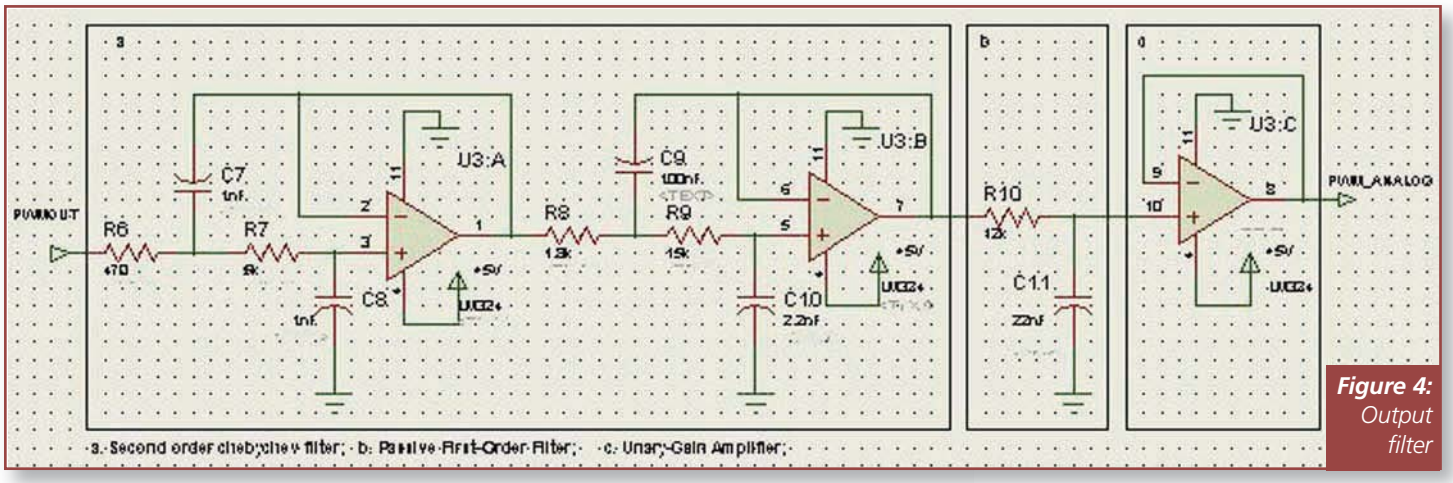


Figure 4: *Output filter*

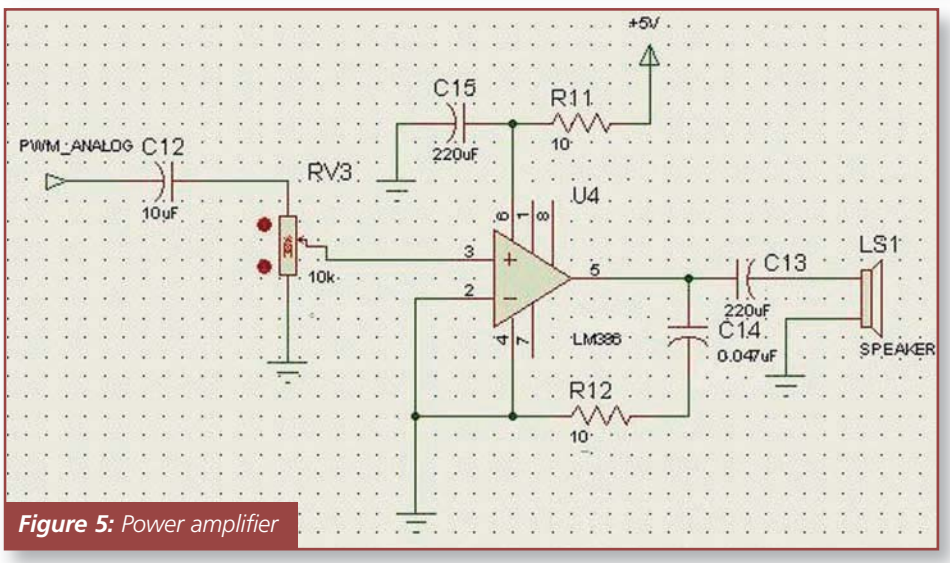


Figure 5: *Power amplifier*

the Compare Match while down-counting. In inverting Output Compare mode, the operation is inverted. The PWM resolution for the phase correct PWM mode has been fixed to 8-bit. The PWM resolution can be calculated in bits by using the following equation:

RPCPW = (log (TOP+1))/log(2) **(1)**

In phase correct PWM mode implemented in this article, the counter is incremented until the counter value matches the fixed value 0x00FF, which is actually the TOP value. When the counter has reached the TOP it changes the count direction. The TCNT1 value will be equal to TOP for one timer clock cycle. The Timer/Counter Overflow Flag (TOV1) is set each time the counter reaches BOTTOM. The interrupt flags can be used to generate an interrupt each time the counter reaches the TOP or BOTTOM value. The OCR1B register, used for comparing value with TCNT1 value, is updated every time with speech sample amplitude value, whenever the timer/counter1 overflow interrupt occurs.

Here, the compare units, while operating in phase correct PWM mode, allow generation of PWM waveform on OC1B pin. Also non-inverted PWM has been generated by setting the corresponding configuration registers. The PWM waveform is generated by clearing the OC1B Register at the Compare Match between OCR1B and TCNT1 when the counter increments, and setting the OC1B Register at Compare Match between OCR1B and TCNT1 when the counter decrements. The PWM frequency for the output when using phase-correct PWM can be calculated by the following equation:

fOCnxPCPWM = (fClk_I/O)/(2.N.TOP) **(2)**

The "N" variable represents the pre-scalar divider (which has been chosen to be 1).

The Output Filter

The output filter section consists of a 5th order, low pass Chebyshev filter and a unary-gain amplifier. The filter is made up by two stagger-tuned, second-order Chebyshev filters (R6, R7, R8, C2, C7 and R7, R10, R11, C9, C5) and a passive first-order filter (R11, C4). The cut-off frequencies of these three filters are slightly shifted against each other ("staggered") to limit pass-band ripple of the whole filter circuit. The overall cut-off frequency is set to 4000Hz, which is roughly one-quarter of the PWM frequency (15,686Hz). This ensures that almost the entire audio spectrum is passed through, but the PWM carrier (at 15,686Hz) is cut off. This filter has been designed using Circuit Wizard of NI Multisim 11.0 Software by National Instruments. The unary-gain prevents the circuit from getting feedback from the output. The capacitor C3 blocks any DC component to the speaker.

The filter and amplifier circuits are based on Operational Amplifier (OpAmp) LM324, which is being operated by single power supply of +5V; instead of utilizing dual power supply. This saves from the trouble of provision for dual power supply to operate OpAmps like 741.

Power Amplifier

The power amplifier is a low-power design. This design is based on the LM386 monolithic power amplifier IC from National Semiconductor. This chip is capable of delivering 1W of output power.

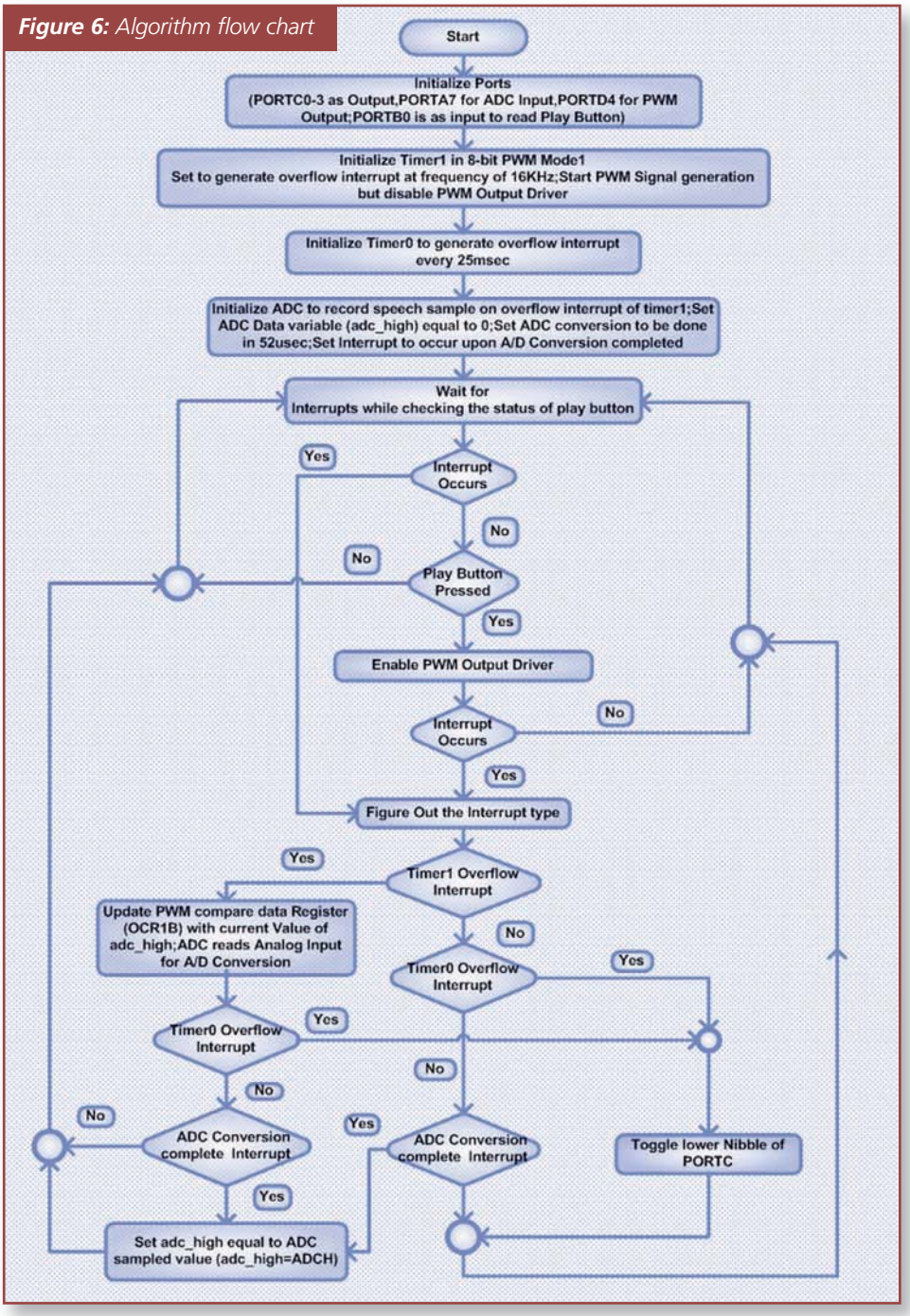
It is a high-efficiency power amplifier, which is ideal for battery-operated applications. The variable resistor RV3 shown in **Figure 5** serves for volume control. The effects of speaker impedance are canalled by the Zobel network connected on the output side of LM386 power amplifier.

The speaker connected with this system is 0.5W and 8 Ohm speaker. This amplifier can easily operate this speaker to play the sound generated by microcontroller using PWM.

Analysis of Code and Algorithm

The primary focus of this article is speech generation using PWM, analogue filters and amplifiers. Speech may be played back in real-time simultaneously while the A/D converted samples are being taken from the analogue input signal. Therefore, to keep the discussion simple and to the point, the analysis of code and algorithm is based only on analogue-to-digital conversion of input analogue speech signal and

Figure 6: *Algorithm flow chart*



simultaneous playback of the digital samples, without storing them in flash memory through Pulse Width Modulation (PWM).

So, in this analysis, the segment of the code that deals with recording of A/D converted speech samples on MMC would not be discussed, although this segment of the code has also been implemented. Therefore, to perform the above mentioned operations, analogue-to-digital converted speech samples are taken by the built-in ADC of ATmega8535 and simultaneously played back through PWM when a pushbutton (Play button) switch is pressed. The delay in playback of the digital speech samples taken from input analogue speech signal is too small to be detected by human ear. The flow chart of this algorithm is shown in the **Figure 6**.

The software that runs on the 8535 MCU is written in C. It is designed for the ImageCraft C compiler for the AVR. It is interrupt driven and makes use of the MCU's inbuilt timers to provide the sampling rate clock. Thus, a stable sampling frequency is produced. All operations of the software are based on these interrupts.

The following steps are performed in this program code represented by Figure 6:

1. Initialization of ports.

a. Lower nibble of PortC is initialized as output for interfacing with LEDs.

b. Pin 7 of PortA is configured for ADC input data.

c. Pin 4 of PortD is configured for PWM output data.

d. PortB pin0 is initialized as input to read the play button connected to it.

2. Timer1 is initialized in 8-bit phase correct PWM mode and set to overflow approximately at a frequency of approximately 16kHz (Actual value is 15,686Hz).
3. Timer0 is initialized to generate an overflow approximately at a frequency of approximately 8kHz, after every approximately 25ms.
4. ADC is in initialized and configured to scan ADC sample from input, i.e. analogue speech signal, upon overflow interrupt of timer1. The ADC data storage variable adc_high is initially set to 0.ADC generates 10-bit sample but only 8-bit sample is saved. The lower byte of ADC data register (ADCL), containing only two bits, is assigned to the unsigned variable adc_low i.e. adc_low = ADCL, which is discarded. The higher byte of ADC data register (ADCH) is assigned to the unsigned variable adc_high i.e. adc_high=ADCH, which is used for speech recording and speech generation.
5. In the main function the status of play button is continuously monitored if the play button is pressed then PWM output driver is enabled otherwise PWM output driver is disabled. The interrupts are awaited while monitoring the status of the input button.
6. Interrupts are serviced on the basis of interrupt priority levels as below:

a. Timer1 Overflow Interrupt has the highest priority. This interrupt may interrupt any other interrupt of lower priority in this code being serviced. Whenever this interrupt occurs the PWM data compare register (OCR1B) is updated with the current value of variable adc_high defined to hold the current value of analogue-to-digital converted sample.

b. Timer0 Overflow Interrupt has the second highest priority. Whenever this interrupt occur the lower nibble of the PortC connected with LEDs toggles state.

c. Analogue-to-digital conversion complete interrupt has the lowest priority. Whenever this interrupt occur the value of adc_high variable is updated with value of the currently obtained analogue-to-digital converted sample.

7. The program control goes to step 5. The steps from 5 to 6 are repeated again and again until the microcontroller is powered off.

The speech generated by PWM module of this system is reasonably good in quality though not of very fine quality. Much finer quality of speech may be generated through PWM if better quality output filters are designed for converting PWM signal to speech signal played back through speaker. ■

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Using Ethernet In Embedded APPLICATIONS

Professor Dr Dogan Ibrahim of the Near East University Cyprus describes the use of Ethernet in embedded microcontroller applications and gives the design of an example Ethernet-based home automation system

ETHERNET IS, BY FAR, the leading wired standard for networking as it enables to connect a very large number of computers, microcontrollers and other computer-based equipment to each other. Ethernet allows devices and equipment to be accessed remotely and provides a cost-effective and reliable means of monitoring or controlling such equipment.

Ethernet has traditionally been implemented on PCs and laptops and has been used widely at home, office and industry to access the worldwide Internet and company-wide intranet networks. Internet can nowadays also be accessed using low-cost portable electronic gadgets such as smart mobile phones, PDAs and others.

With recent advances in technology and especially in chip manufacturing, Ethernet can now be fully realized through single-chip devices. Several manufacturers offer either single-chip Ethernet controllers, or general purpose microcontrollers with on-board Ethernet controllers. Such controllers can very easily be configured, programmed and used in Ethernet-based embedded applications. Typical applications of embedded Ethernet include:

- Home automation
- Access control
- Environmental monitoring
- Industrial control
- Safety and security
- POS terminals
- Remote control
- Lighting control.

PIC18F97J60 is an advanced microcontroller chip manufactured by Microchip Inc (www.microchip.com) with built-in 10Base-T Ethernet capability. The device offers 128K flash program memory, 3908 bytes of RAM memory, 70 I/O pins, 16 10-bit A/D channels, timers, counters and many more features. Microchip's ENC28J60 is a popular 28-pin serial Ethernet chip that can easily be used in microcontroller-based applications to provide Ethernet capability to the application.

Several manufacturers offer Ethernet development kits, enabling users to learn and incorporate Ethernet functionalities in their designs. Examples of some development kits are:

- ETHERNETDK (www.silabs.com) is an Ethernet development kit that provides all the necessary hardware and software to create real-time embedded Ethernet-based applications. The kit contains an 8051 microcontroller-based C8051F120 microcontroller and a CP2200 Ethernet chip with an RJ45 connector. A Silicon Laboratories evaluation kit and application examples are provided on a CDROM distributed with the kit.
- PIC-MINI-WEB (www.olimex.com) is an embedded Ethernet development board using a PIC18F25J10 chip as the microcontroller and an ENC28J60 Ethernet chip. 1Mbit on board serial flash memory is provided to store web pages. In addition, a mini ICSP/ICD is available on the board for programming and debugging.
- The Embedded Ethernet Development kit manufactured by CCS (www.ccsinfo.com) is a complete kit based on the PIC18F4620 microcontroller and the ENC28J60 Ethernet chip. The kit provides 30 I/O pins, one potentiometer, LEDs, serial EEPROM, an MMC card reader and RJ45 socket. The development kit is supported by company's IDE, including a compiler and in-circuit real-time debugging tool.
- The Serial Ethernet Board manufactured by mikroElektronika (www.mikroe.com) is based on the ENC28J60 Ethernet chip and it can easily be connected to company's development boards (EasyPIC5 or EasyPIC6). The board is fully supported by mikroElektronika C, Pascal and Basic compilers.

This article describes the details of the ENC28J60 Ethernet chip and shows how the chip can be used in a simple microcontroller-based networked home automation system to turn lights ON and OFF.

DESTINATION ADDRESS	SOURCE ADDRESS	TYPE	DATA	CRC

Figure 1: *Ethernet packet format*

UDP SOURCE PORT	UDP DESTINATION PORT
MESSAGE LENGTH	CHECKSUM
DATA	

Figure 2: *UDP packet format*

VERSION	IHL	TYPE	LENGTH	
IDENIFICATION			FLAGS	OFFSET
Time To Live	PROTOCOL	CHECKSUM		
SOURCE ADDRESS				
DESTINATION ADDRESS				
OPTIONS			PADDING	
DATA				

Figure 3: *IP packet format*

Ethernet Communications

Ethernet is a frame-based computer networking technology for Local Area Networks (LAN), standardized using the IEEE 802.3.

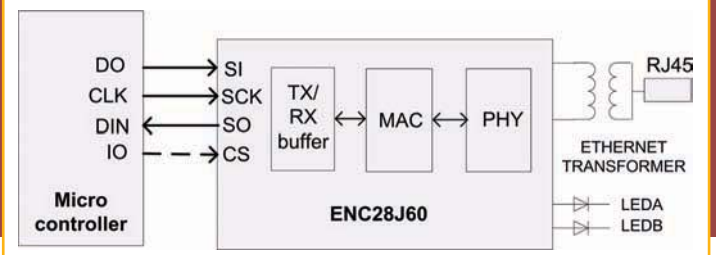


Figure 4: *Connecting the ENC28J60 Ethernet chip to a microcontroller*

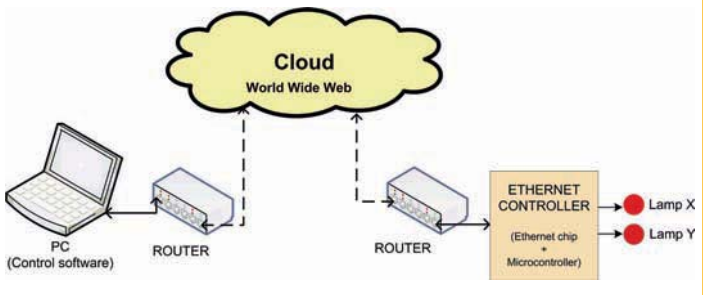


Figure 5: *Block diagram of the project*

Ethernet was originally invented by Xerox in 1972 and then developed by Xerox, DEC and Intel.

An Ethernet LAN typically uses coaxial cable, twisted pair wires, fibre optic, or can be in the form of wireless LANs. The most common form of Ethernet is called 10Base-T and it provides a transmission speed up to 10Mbps. Fast Ethernet or 100Base-T provides transmission speeds up to 100Mbps. Gigabit Ethernet provides even higher level of support at 1000Mbps.

Devices on the Ethernet are all connected together and compete for access using a Carrier Sense Multiple Access with Collision Detection (CSMA/CD) protocol. The advantage of CSMA/CD is that, unlike Token Ring and Token Bus, all nodes can see each other with only one transmitting at a time to avoid any collisions. In case of a collision the transmitting nodes wait for a random time and attempt to re-transmit, hoping to avoid the collision. The maximum length of an Ethernet cable depends upon the speed of transmission and the type of cable used. For standard twisted pair type cables operating at 10Mbps, the maximum cable length is specified as 100m. Using fibre-optic cables this length can be extended to 2000m or over.

Ethernet is used to communicate using various protocols, e.g. DECnet, IP, ARP, etc. **Figure 1** shows the Ethernet packet format (en.wikipedia.org/wiki/Ethernet). A packet consists of 6 byte destination MAC address, 6 byte source MAC address, 2 byte data type, 45 to 1500 bytes data and a 4 byte CRC. Additionally, when transmitted on the Ethernet medium, a 7-byte preample field and Start-of-Frame delimiter byte are appended to the beginning of the Ethernet packet. As we shall see later, the data type for IP packets is 0x0800.

In this article we will use the Ethernet with IP packets for data communication over the network. Two protocols are supported under this scheme: TCP and UDP. TCP is an advanced data protocol requiring connection and providing guaranteed packet delivery with re-transmission if an error occurs. TCP acknowledges transmitted packets to confirm their correct delivery. In most remote data control applications the simpler UDP data protocol is used. Since this is the protocol used in the example in this paper, further details about the UDP is given in the next section.

The UDP

The User Datagram Protocol (UDP) is commonly used in remote automation applications. This protocol offers:

- UDP does not establish connection before sending data, it just packages it.
- UDP has only basic error checking using checksums.
- There is no sequencing of data in UDP and thus UDP does not ensure that data is received in the same order that they were sent.
- UDP is efficient for broadcasting/multicast transmission.
- UDP is faster, simpler and more efficient than TCP, however it is less robust than TCP.
- The delivery of data cannot be guaranteed in UDP.
- There is no re-transmission of lost packets in UDP.

UDP is widely used and recommended for data transfer over a network where performance and speed are more important than reliable delivery and where acknowledgement of delivery is not needed. Another important application area of UDP is in multicast or broadcast transmissions, since these are not supported by TCP.

Some common examples where UDP is used are:

- In multicast systems
- Domain Name System (DNS)
- Simple Network Management Protocol (SNMP)
- Dynamic Host Configuration Protocol (DHCP)
- Routing Information Protocol (RIP)
- Streaming video and VOIP.

A UDP packet consists of a Header and Data (see **Figure 2**). The header is always 4 bytes long and consists of the source and destination port numbers, message length and the checksum. This is followed by the actual data bytes.

The checksum is calculated by forming a UDP Pseudo-Header consisting of the source and destination addresses, protocol number and the data length. The UDP packet is encapsulated within an IP packet (see **Figure 3**) consisting of 20 bytes, followed by the UDP packet. The UDP packet protocol number is 17 (0x11). The IP packet is then encapsulated within an Ethernet packet and is transmitted to its destination node over the network.

There are several programs available in the market that can be used to analyze packets on an Ethernet network. Some programs are open source, provide no user support and can be downloaded free of charge from the Internet (e.g. Ethereal, Wireshark, Tcpdump, Dsniff), while some others come with full user support and can be purchased (e.g. EtherDetect, Colasoft Capsa).

The ENC28J60 Ethernet Chip

The ENC28J60 is a standalone 28-pin Ethernet controller chip with SPI interface and meets all of the IEEE 802.3 specifications. The chip has the following basic features:

- Compatible with 10/100/1000Base-T networks.
- Supports automatic polarity detection and correction.
- Supports half-duplex and full duplex operation.

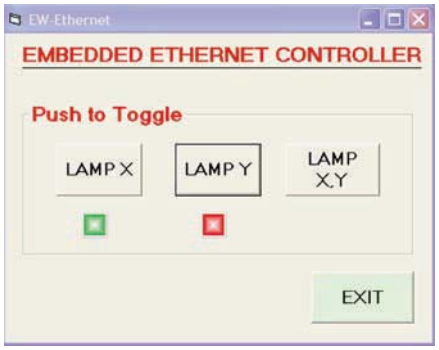


Figure 6: *The PC form*

- Automatic retransmit on collision.
- Automatic rejection of erroneous packets.
- SPI interface with up to 20MHz speed.
- 8K byte transmit/receive buffer.
- Support for unicast, multicast and broadcast addresses.
- Link and Activity LED interface.
- Differential signal input-output for interface to RJ45 connector.

The chip incorporates transmit and receive buffers, MAC (Medium Access Control) module, PHY (Physical Layer) module and associated control and interface logic. **Figure 4** shows how the chip can be used in microcontroller-based applications. Basically, the interface requires the SPI signals SI, SO and SCK to be connected to the microcontroller. In addition, the CS signal can also be driven from the microcontroller. The chip is connected to a network through a RJ45 type socket and a suitable Ethernet transformer.

Example Ethernet-Based Project

This section describes the design of a simple microcontroller-based home automation system using the Ethernet as the communication medium. **Figure 5** shows the block diagram of this example project. The project hardware is in two parts, connected using a network hub or a switch: the Ethernet controller and the PC.

The Ethernet controller consists of a microcontroller and an ENC28J60 Ethernet chip. Two LEDs connected to the microcontroller simulate two lamps X and Y. A GUI-based program on the PC is under the control of the user and sends data packets to the Ethernet controller to turn the lamps ON or OFF.

The PC Program

The PC program is developed using the Visual Basic 6.0 programming language (www.microcoft.com). Microsoft Winsock ActiveX control is used to develop the UDP program on the PC. **Figure 6** shows the GUI form of the PC program. Clicking command buttons Lamp X or Lamp Y toggles the states of lamps X or Y respectively. Similarly, clicking command button Lamp X, Lamp Y toggles the state of both lamps X and Y. Two lights under the command buttons are updated regularly to indicate the status of the lamps, where green indicates ON and red indicates OFF.

The following data is sent to the Ethernet controller when a command button is clicked. Characters "S" and "#" denote the beginning and ending of the command data respectively:

Command	Lamp	Description
SX#	Lamp X	Toggle Lamp X
SY#	Lamp Y	Toggle Lamp Y
SA#	LampX and LampY	Toggle Lamp X and Lamp Y

Similarly, the following data is sent regularly from the Ethernet controller to the PC to indicate the status of the two lamps. Here again "S" and "#" denote the beginning and ending of the data respectively. "x" and "y" can be "0" (OFF), or "1" (ON) and they indicate the status of the two lamps X and Y respectively:

SX=n,Y=m#

Figure 7 shows the program listing of the PC program. When the form is loaded, UDP protocol is selected and remote host IP address is set to "192.168.1.11". Procedures CmdLampX_Click, CmdLampY_Click and CmdLampXY_Click are activated when command buttons Lamp X, Lamp Y and Lamp XY are clicked respectively. Procedure WinSock_DataArrival is activated whenever a UDP packet is received by the program. Here, the status of the two LEDs are updated accordingly on the GUI form.

```
Private Sub CmdExit_Click()
End
End Sub
Private Sub CmdLampX_Click()
WinSock.SendData "SX#"
End Sub
Private Sub CmdLampY_Click()
WinSock.SendData "SY#"
End Sub
Private Sub CmdLampXY_Click()
WinSock.SendData "SA#"
End Sub
Private Sub Form_Load()
LampXLED.Value = False
LampYLED.Value = False
WinSock.Protocol = sckUDPProtocol
WinSock.RemoteHost = "192.168.1.11"
WinSock.RemotePort = 10001
End Sub
Private Sub WinSock_DataArrival(ByVal bytesTotal As Long)
WinSock.GetData stat, vbString

If Left$(stat, 1) = "S" And Mid$(stat, 9, 1) = "#" Then
If Mid$(stat, 2, 2) = "X=" Then
If Mid$(stat, 4, 1) = "1" Then
LampXLED.Value = True
ElseIf Mid$(stat, 4, 1) = "0" Then
LampXLED.Value = False
End If
End If
If Mid$(stat, 6, 2) = "Y=" Then
If Mid$(stat, 8, 1) = "1" Then
LampYLED.Value = True
ElseIf Mid$(stat, 8, 1) = "0" Then
LampYLED.Value = False
End If
End If
End If
End Sub
```

Figure 7: PC program listing

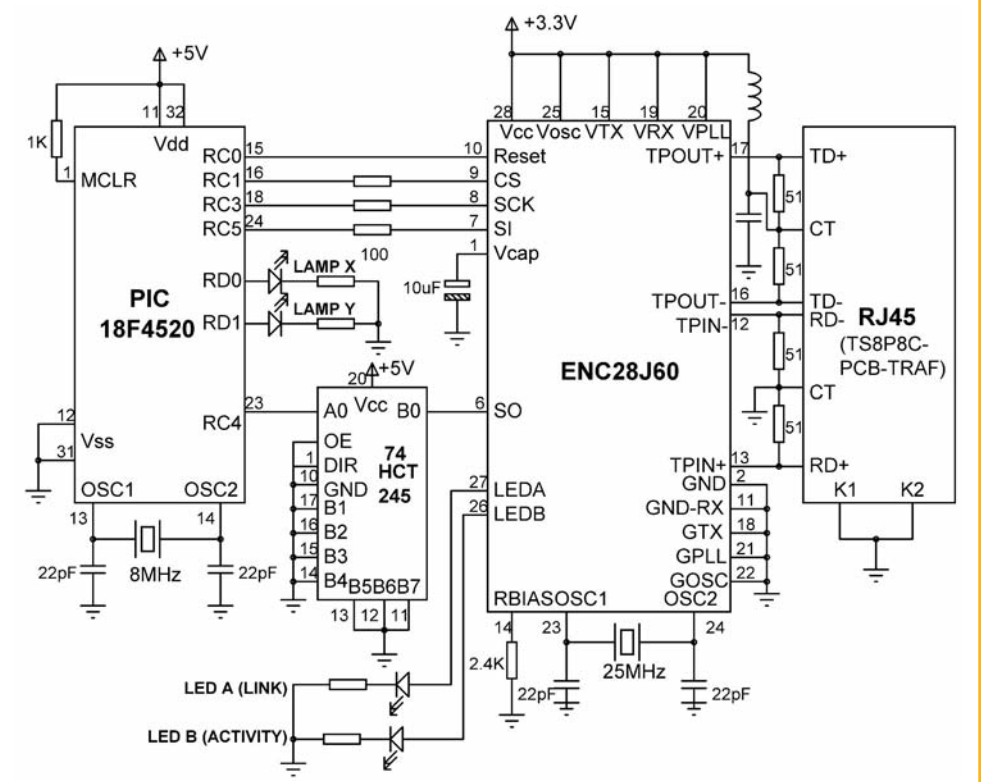


Figure 8: *Circuit diagram of the Ethernet controller*

Figure 8 shows the circuit diagram of the Ethernet controller. The controller is designed around the PIC18F4520 microcontroller, operating at 8MHz and the ENC28J60 Ethernet chip, operating at 25MHz. The interface between the microcontroller and the Ethernet chip is based on the SPI bus protocol (www.zone.ni.com/devzone/cda/tut/p/id/9119) where the SI, SO and SCK pins of the Ethernet chip are connected to SPI pins (PORT C) of the microcontroller. The Ethernet chip operates with 3.3V and its output pins (SO) cannot drive the microcontroller inputs without a unidirectional voltage translator. In Figure 8, a 74HCT245 type buffer is used to boost the output signal level of pin SO. Other low-cost chips such as 74HCT08 (AND gate), 74ACT125 (quad 3-state buffer) or other chips could also have been used instead.

The internal analogue circuitry of the ENC28J60 chip requires that an external resistor is connected from RBIAS to ground. Some of the device's digital logic operates at 2.5V and an external filter capacitor should be connected from Vcap to ground. Lamp X and Lamp Y are connected to RD0 and RD1 pins of the microcontroller respectively. Transmit output pins of the Ethernet chip (TPOUT+ and TPOUT-) and the receive inputs (TPIN+ and TPIN-) are connected to a RJ45 socket with integrated Ethernet transformer (T58P8C-PCB-TRAF). LED A and LED B of the Ethernet chip provide visual indication of the Link and Activity on the line respectively (the RJ45 socket has a pair of built in internal LEDs, but are not used in this project). A 5V to 3.3V power supply regulator chip (e.g. MC33269DT-3.3) is used to provide power to the Ethernet chip. If the PC and the Ethernet controller are on the same network then the two can be connected together using a twisted network cable, otherwise, a hub or a switch may be required. If the PC and the Ethernet controller are located on different networks then routers may be required to establish communication between the two.

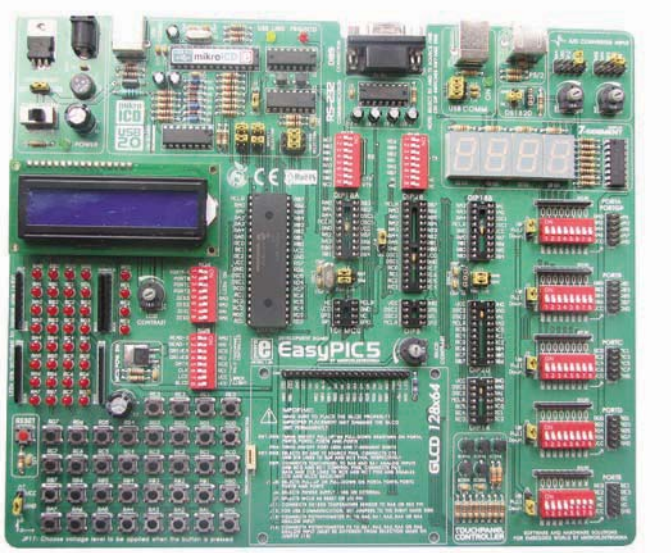


Figure 9: *EasyPIC 5 development board*

The Construction

The project was constructed using the EasyPIC 5 Development Board (see **Figure 9**) and the Serial Ethernet Board (www.mikroe.com). EasyPIC 5 is a fully integrated development board where a program can be developed and compiled on a PC and then downloaded to a PIC microcontroller via the on-board USB programmer. The board also incorporates in-circuit debugger hardware, making it easy to debug software during the development cycle.

The Serial Ethernet Board (see **Figure 10**) simplifies the design of Ethernet-based applications. The board is equipped with an ENC28J60 Ethernet chip, 74HCT245 for voltage level translation, three LEDs, RJ45 socket with integrated transformer and LEDs and a 5V to 3.3V voltage regulator. A 10-way IDC socket is provided at the edge of the serial Ethernet board and this can be directly connected to the 10-way PORT C plug provided at the edge of EasyPIC 5 development board (see **Figure 11**).

The Software

The software of the Ethernet controller is developed using the highly popular mikroC language. It provides built-in libraries for peripheral devices such as RS232, RS485, SD card, Compact Flash card, USB, CAN, Serial Ethernet, LCD, GLCD, touch screen and so on. Development of the controller software using the built in Serial Ethernet Library routines was extremely simple. **Figure 12** shows operation of the controller software as a PDL. The software is based on the UDP protocol. After the basic initialization, the software looks for command data on the line, decodes this data and turns the lamps ON and OFF as requested.

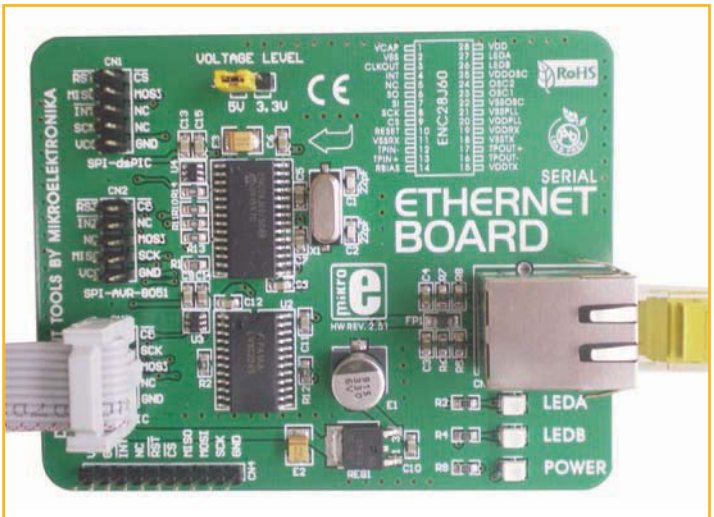


Figure 10: *Serial Ethernet board*

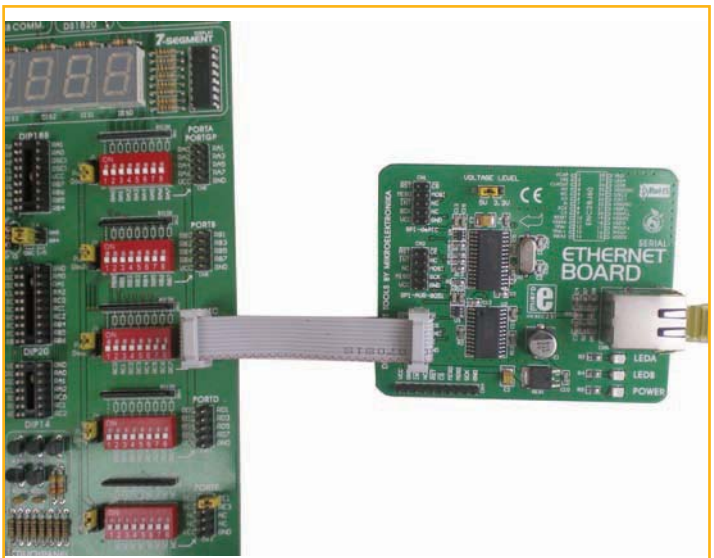


Figure 11: *Serial Ethernet board connection to EasyPIC 5*

MAIN Program
BEGIN
Configure I/O ports
Initialize SPI bus
Initialize serial Ethernet library
DO FOREVER
Check for packets
ENDDO
END

User UDP Code
BEGIN
IF a correct packet received
Decode the packet
Turn appropriate LEDs ON or OFF
ENDIF
Get status of LEDs
Send status of LEDs
END

Figure 12: *Operation of the controller software*

The operation of the Ethernet controller software is very simple and its complete listing is given in **Figure 13**. At the beginning of the main program the I/O ports are configured and the SPI bus is initialized by calling to built-in library function SPI_Init. Then, the serial Ethernet library is initialized by calling to function SPI_Ethernet_Init and specifying the MAC address, the IP address and the mode of operation (Full-Duplex).

The main program then enters an infinite loop where function SPI_Ethernet_doPacket is called to check for the arrival of packets and also to send any outstanding packets. UDP packet arrival and sending outstanding packets are handled in procedure SPI_Ethernet_UserUDP. Here, UDP data is received by calling to function SPI_Ethernet_getByte and the received command data is decoded and the appropriate LEDs are turned ON or OFF. In addition, the state of the two LEDs are read and sent to the PC using function SPI_Ethernet_putBytes.

```
sbit LampX at RD0_bit;
sbit LampY at RD1_bit;
sfr sbit SPI_Ethernet_Rst at RC0_bit;
sfr sbit SPI_Ethernet_CS at RC1_bit;
sfr sbit SPI_Ethernet_Rst_Direction at TRISC0_bit;
sfr sbit SPI_Ethernet_CS_Direction at TRISC1_bit;

unsigned char MACAddr[6] = {0x00,0x14,0xA5,0x76,0x19,0x3F};
unsigned char IPAddr[4]= {192,168,1,11};
unsigned char buffer[3];

typedef struct {
 unsigned canCloseTCP: 1;
 unsigned isBroadcast: 1;
} TEthPktFlags;

unsigned int SPI_Ethernet_UserTCP(unsigned char *remoteHost,
unsigned int remotePort, unsigned int localPort, unsigned int
reqLength, TEthPktFlags *flags)
 {
 return (0);
 }

unsigned int SPI_Ethernet_UserUDP(unsigned char *remoteHost,
unsigned int remotePort, unsigned int destPort, unsigned int
reqLength, TEthPktFlags *flags)
{
 unsigned char i,x,y;
 unsigned char tx[] = "SX=1,Y=0#";
 for(i=0; i<3; i++)
 {
 buffer[i] = SPI_Ethernet_getByte();
 }
 if(buffer[0] == 'S' && buffer[2] == '#')
 {
 switch (buffer[1])
 {
 case 'X': LampX = ~ LampX;
 break;
 case 'Y': LampY = ~LampY;
 break;
 case 'A': LampX = ~LampX; LampY = ~LampY;
 }
 }
```

```
 x = LampX; y = LampY;
 x = x+'0'; y = y+'0';
 tx[3] = x; tx[7] = y;
 SPI_Ethernet_putBytes(tx, 9);
 return(9);
}

void main()
{
 TRISD = 0;
 CMCON |= 0X07;
 PORTD = 0x00;
 SPI_Init();
 SPI_Ethernet_Init(MACAddr,IPAddr,0x01);

 while(1)
 {
 SPI_Ethernet_doPacket();
 }
}
```

Figure 13: Controller software

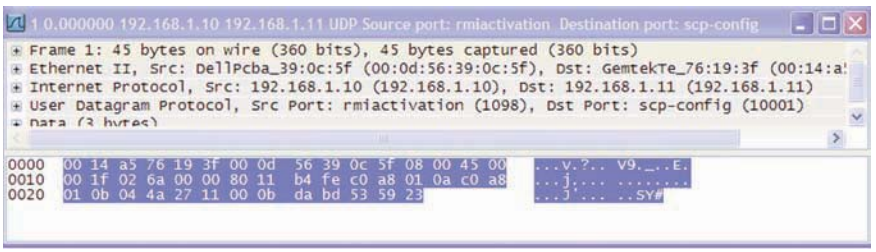


Figure 14: *Packet when command "SY#" is sent from the PC*

Figure 14 shows contents of a packet captured using the Wireshark (www.wireshark.com) data capturing software when command "SY#" was sent from the PC to toggle Lamp Y. The total packet consists of 45 bytes. The first 12 bytes are the destination and source addresses respectively. Two bytes 08 00 denote that this is an IP packet. The UDP data occupies the last 11 bytes of the packet where:

04 4a	**UDP source port**
27 11	**UDP destination port**
00 0b	**Message length (11)**
da bd	**Checksum**
53 59 23	**Data (SY#)**

Clamp SIZING

Paul Lacey, Applications Engineer at Power Integrations Inc in the US, discusses the designing of effective protection circuits to ensure MOSFET reliability in flyback power supplies

AC-DC POWER SUPPLIES up to approximately 100W commonly utilize the flyback topology. Its low cost and ability to provide multiple tracking outputs with a single controller have made it a favourite among designers and a de facto standard for low component count AC-DC converters.

One disadvantage of a flyback converter is the high stress placed on the primary switching element.

Storing Energy

Flyback topologies operate by storing energy in the transformer during the on-time of the power switch and transferring this energy to the output during the off-time. A flyback transformer is comprised of two or more coupled windings on a core containing a series air gap across which (magnetizing) energy is stored until it can be transferred to the secondary.

In practice, the coupling between the windings is never perfectly matched and not all of the energy is transmitted across this gap. A small amount of energy is stored within and between the windings in what is referred to as the leakage inductance of the transformer. When the switch opens, the energy in the leakage inductance is not transferred to the secondary, but instead generates a high voltage spike across the transformer primary winding and the switch. It also results in high frequency ringing between the effective capacitance of both the open switch and primary winding and the leakage inductance of the transformer (**Figure 1**).

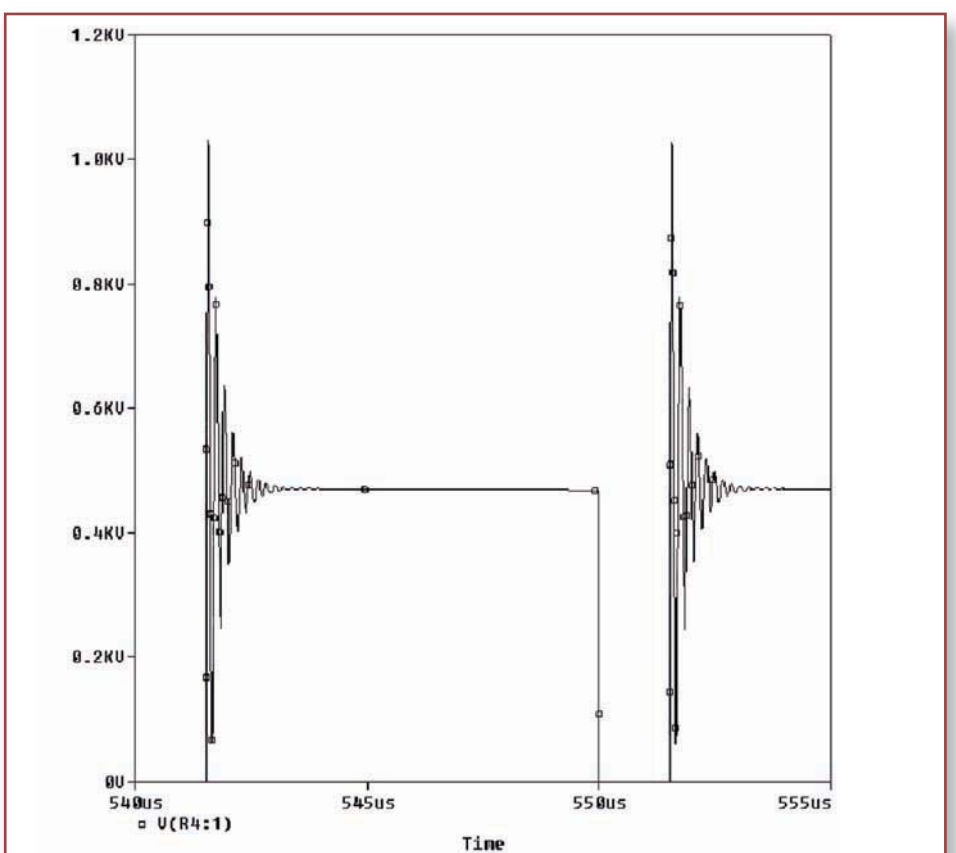


Figure 1: *Drain node switching transients generated by leakage inductance*

If the peak voltage of this spike exceeds the breakdown voltage of the switching element, which is normally a power MOSFET, it can result in a destructive failure. Moreover, the high amplitude ringing on the drain node causes a significant amount of EMI. For power supplies above approximately 2W, a clamp circuit is used to limit the voltage spikes across the MOSFET by safely dissipating leakage inductance energy.

How the Clamp Works

A clamp circuit is used to limit the maximum voltage across the MOSFET to a specified value. Once the voltage across the MOSFET reaches the threshold, all additional leakage energy is diverted into the clamp circuit where it is either stored and slowly dissipated or recycled back into the circuit.

One disadvantage of a clamp is that it dissipates power and can reduce efficiency. For this reason, there are many different types of clamp circuits (**Figure 2**). Several use Zener diodes to minimize power consumption, but also increase EMI generation from the sharp turn-on of the Zener. The RCD clamp provides a good balance of efficiency, EMI generation and cost and, as a result, is the most common.

The RCD clamp operates as follows: Immediately after the MOSFET turns off, the secondary diode remains reverse biased and magnetizing current charges the drain capacitance (**Figure 3a**). When the voltage across the primary winding reaches the output reflected voltage (VOR) defined by the turns ratio of the transformer, the secondary diode turns on and magnetizing energy is transferred to the secondary. Leakage energy continues charging the transformer and drain capacitance until the voltage across the primary winding equals the voltage across the clamp capacitor (**Figure 3b**).

At this point, the blocking diode turns on and leakage energy is diverted into the clamp capacitor (**Figure 4a**). The charging current drawn through the capacitor clamps the peak voltage seen on the drain node to VIN(MAX) + VC(MAX). After the leakage energy is fully

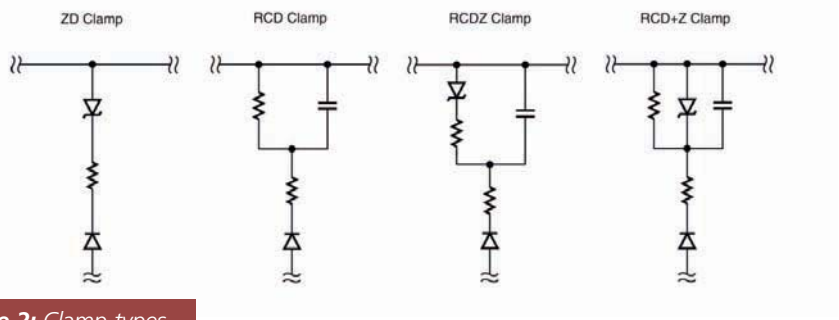


Figure 2: *Clamp types*

transferred, the blocking diode turns off and the clamp capacitor discharges into the clamp resistor until the next cycle (**Figure 4b**).

A small resistor is often added in series with the blocking diode to dampen any ringing between the transformer inductance and clamp capacitor at the end of the charging cycle. This complete cycle causes the voltage ripple seen across the clamp circuit referred to as VDELTA, with the amplitude controlled by the sizing of the parallel capacitor and resistor (**Figure 5**).

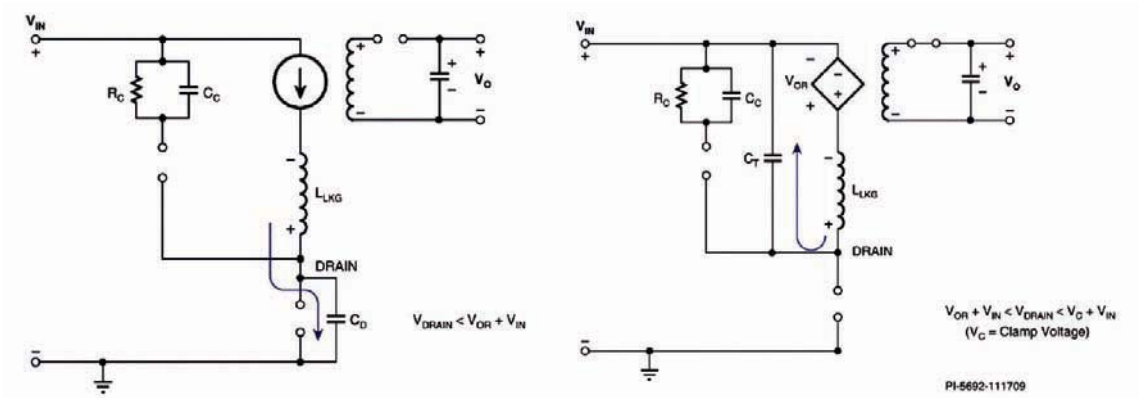
The RCDZ clamp is identical in operation to the RCD clamp except that the Zener diode in series with the resistor shares the dissipation (Figure 2). The Zener diode prevents the capacitor from discharging below the Zener blocking voltage. This limits power dissipation and improves efficiency, particularly at light loads.

The ZD clamp provides a hard clamp of the MOSFET voltage specified by the blocking voltage of the Zener. Finally, the RCD+Z clamp operates in the same way as an RCD clamp, with the added Zener providing a fail-safe hard clamp for the MOSFET voltage during transient conditions, along with the EMI generation characteristic of the RCD during normal operation.

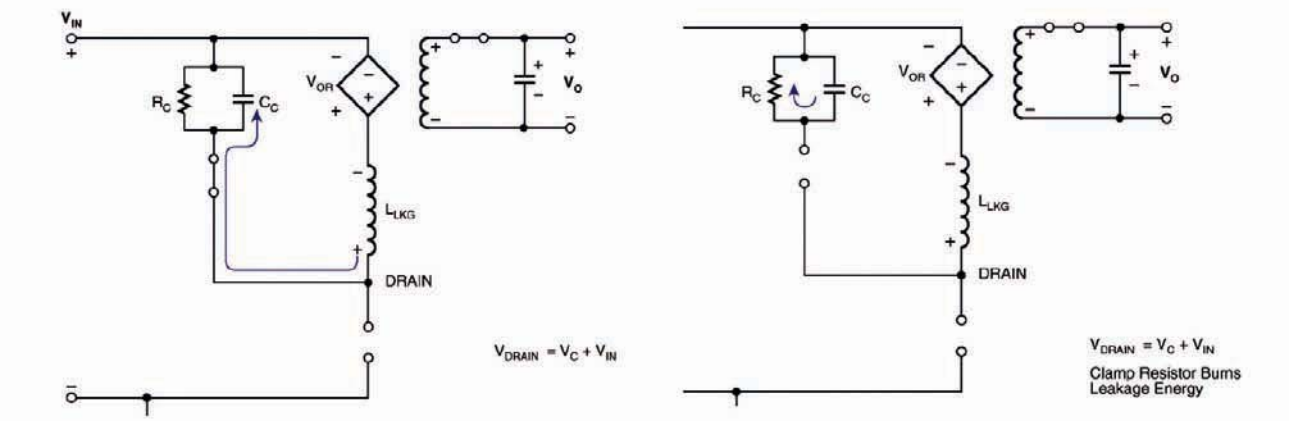
Clamp design must take into consideration the characteristics of both the transformer and MOSFET. If the minimum clamping voltage is below the VOR of the transformer, the clamp will act as a load, dissipating more than just leakage energy and reducing efficiency.

If the clamp components are undersized, they may overheat, fail to prevent dangerous voltages and create unnecessary EMI. Most importantly, the clamp must protect the MOSFET under all conditions of supply input voltage, load current and component tolerances.

A Clamp Sizing Design Guide (PI-DG-101) published by Power Integrations, Inc., provides a step-by-step procedure for sizing components in each of the four major clamp type circuits for a flyback power supply. The Design Guide is intended to be used together with PI Expert design software. PI Expert is an interactive program that takes a user's power supply specifications and automatically determines the



Figures 3a *(left) and* ***3b*** *(right): Primary side clamp*



Figures 4a *(left) and* ***4b*** *(right): Clamp operation*

critical components (including transformer specifications) needed to generate a working switch mode power supply. PI Expert will create a clamp design automatically, but the result will be slightly more conservative than that generated by following the algorithms in the Clamp Sizing Design Guide.

Sizing an RCD clamp

Below is a summary of the steps to follow when designing an RCD clamp. For complete details, please refer to the Clamp Sizing Design Guide. All values mentioned below not measured or defined by the user should be found in the PI Expert Design Results tab.

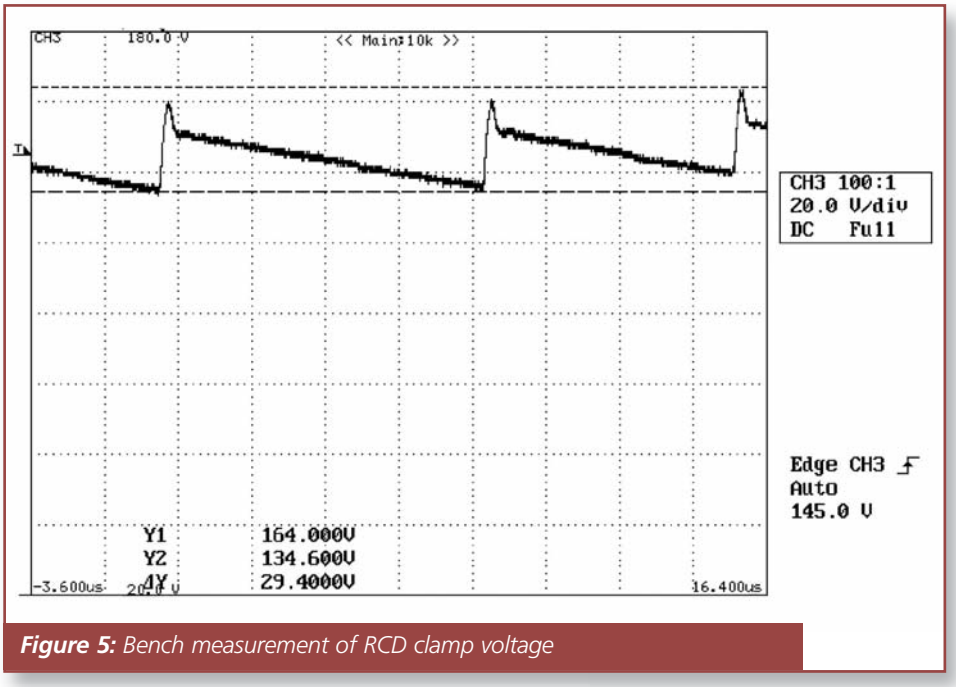


Figure 5: *Bench measurement of RCD clamp voltage*

1. Measure the primary leakage inductance of your transformer, L_L.
2. Check the switching frequency of your design, f_s
3. Determine the correct primary current, I_P, as follows:
   If your design uses power limit programming, $I_P = I_{LIMITEXT}$
   a. If your design uses external current limit programming, $I_P = I_{LIMITEXT}$
   b. For all other designs, $I_P = I_{LIMITMAX}$
4. Determine the total voltage allowed across the primary MOSFET and calculate $V_{maxclamp}$ as:
   $$V_{MOSFETmax} = (VAC_{HighLine} * \sqrt{2}) + V_{maxclamp}$$
   (Note: It is recommended that at least a 50V margin be maintained below BVDSS for a MOSFET, with an additional 30 to 50V margin to account for transient voltages.)
5. Determine the voltage ripple across the clamp circuit, V_{delta}
6. Calculate the minimum voltage across the clamp circuit as:
   $$V_{minclamp} = V_{maxclamp} - V_{delta}$$
7. Calculate the average voltage across the clamp circuit, V_{clamp} as:
   $$V_{clamp} = V_{maxclamp} - \frac{V_{delta}}{2}$$
8. Calculate energy stored in leakage reactance as:
   $$E_{LL} = \frac{1}{2} * L_L * I_P^2$$
9. Estimate energy dissipated in the clamp, E_{clamp}, as:
   $1.5\,W \le P_{out} \le 50\,W$ $\quad E_{clamp} = 0.8 * E_{LL}$
   $50\,W < P_{out} \le 90\,W$ $\quad E_{clamp} = E_{LL}$
   $90\,W < P_{out}$ $\quad E_{clamp} = E_{LL} * \left(\frac{V_{clamp}}{V_{clamp} - VOR}\right)$
10. Calculate the clamp resistor value as:
    $$R_{clamp} = \frac{V_{clamp}^2}{E_{clamp} * f_s}$$
11. The clamp resistor power rating should be more than:
    $$\frac{V_{clamp}^2}{R_{clamp}}$$
12. Calculate the clamp capacitor value as:
    $$C_{clamp} = \frac{E_{clamp}}{\frac{1}{2} * [V_{maxclamp}^2 - V_{minclamp}^2]}$$
13. The clamp capacitor voltage rating should be more than $1.5 * V_{maxclamp}$
14. A fast or ultra-fast recovery diode should be used as the blocking diode in a clamp circuit.
15. The Peak Inverse Voltage of the blocking diode should be more than $1.5 * V_{maxclamp}$
16. The forward peak repetitive current rating of the blocking diode should be more than: I_P
    If this parameter is not listed in the datasheet, the average forward current rating should be more than: $0.5 * I_P$
17. Size the damping resistor (if used) as:
    $$\frac{20}{0.8 * I_p}\Omega \le R_{damp} \le 100\Omega$$
18. The damping resistor power rating should be more than $I_p^2 * R_{damp}$

After the initial design, a prototype should be constructed to verify power supply performance, as transformer leakage inductance can vary significantly according to winding techniques. In particular, the average voltage V_{clamp} should be measured and compared with that calculated in Step 7 (Figure 5). Any significant deviation may be corrected by adjusting the value of R_{clamp}. If the results are significantly different from expected, the design must be iterated.

The procedures for sizing the other clamp types follow the same process, with steps for each additional component. Care must be taken in diode and Zener selection to ensure their power ratings are not exceeded. In almost all cases where a Zener function is required, a transient voltage suppressor type should be used to provide the necessary instantaneous peak power rating.

The power ratings of components should be verified by measuring body temperatures while the power supply is running at full load and lowest input voltage. If any component is operating above the manufacturer's recommended temperature limits, it should be resized and the design carefully evaluated against prototype results. ■

Channel Processing used in Mobile Satellite COMMUNICATIONS

In a series of three articles **Stojce Dimov Ilcev** of Mangosuthu University of Technology in Durban, South Africa, reviews the basic and state-of-art channel coding, decoding and error correction techniques as well as channel processing used in Mobile Satellite Communications

VOICE, VIDEO, data or telex information used in Mobile Satellite Communications (MSC) are transmitted in digital form through a channel that can cause degradation of these transmission signals. The noise, interference, fading and other obstacle factors experienced during transmission could increase the probability of bit error at the receiver of Mobile Earth Station (MES).

The subject of coding emerged following the fundamental concepts of information theory laid down by Shannon in 1948, which is the relationship between communication channel and the rate at which information can be transmitted over it. Differently to say, the data signal may be encoded in such a way as to reduce the likelihood of bit error. Anyway, the coding process uses redundant bits, which contain no information to assist in the detection and correction of errors. There are several methods of error corrections that reduce the number of redundant bits in speech, audio and visual signals in order to make more economic use of bandwidth.

Decoding

The complete transmission loop requires any type of encoder followed by modulation and transmitter via transmission channel to receiver, namely to demodulator and decoder. In such a manner, decoding is the reverse method of coding and every type of decoding on the transmit side needs the same convenient decoding method on the receive side.

The simplest means of decoding block codes is by a method of correlation whereby the decoder makes a comparison between the received code word and all permissible code words, selecting that word that gives the nearest match. Decoding of such codes will also depend on whether error detection or error correction is required. Decoders of block codes generally cannot use soft decision outputs from the demodulator, unlike the decoders for convolutional codes.

Convolutional Decoding

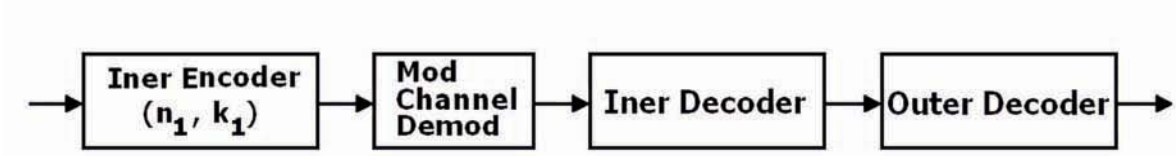
The effect of the transmission channel on the signal and the probability of detection of a 1 or 0 in the presence of Gaussian noise are important factors during detection. In such a manner, an output from the demodulator can be configured to give a correct decision regarding whether the incoming signal is 1 or 0. The process of decoding then depends on the two state inputs it receives.

An alternative demodulator configuration allows quantization of the predicted level which gives the decoder more necessary information regarding the probable state of the demodulator output. For example, if 3 bit (2^3 = 8 levels) quantization occurs then '0 0 0' would suggest a firm valuation of the level received as a 0. On the other hand, a '0 0 1' scheme suggests the 0 is received close to the threshold and this valuation as a 0 is made with less certainly. The reason for quantization is to provide the convolutional decoder with more information in order to correctly recover the transmitted information with better error performance probability.

Turbo Decoding

The turbo decoder operates by performing an interactive decoding algorithm, resulting in the partial transfer of an a priori likelihood estimate of the decoded bit sequence between the constituent decoders. Initially, the received information bits, which may be in some error due to the influence of the channel, are used to perform a priori likelihood estimates by the respective decoders. In a more precise sense, the decoders employ a 'Maximum A Posteriori' (MAP) algorithm to perform converge on the likely sequence of data transfer, after which the interaction

Figure 1: *Concatenated decoded system*



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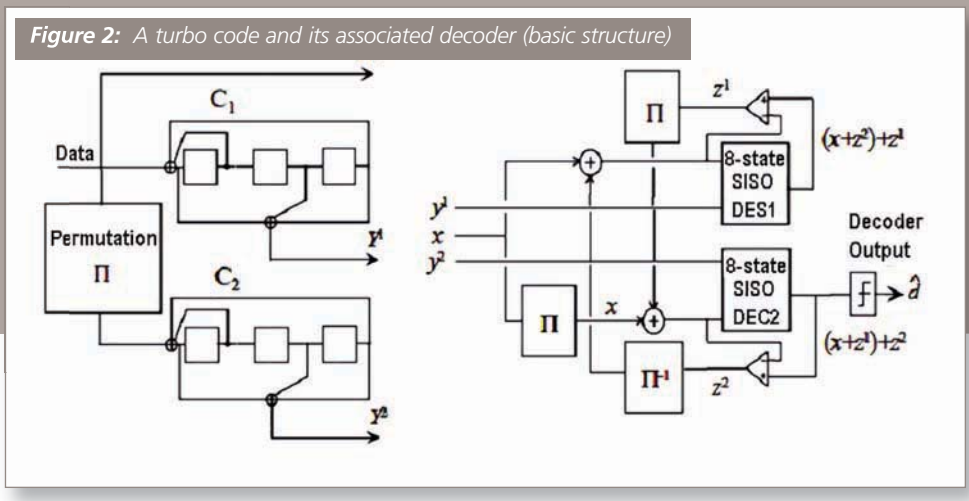

Figure 2: *A turbo code and its associated decoder (basic structure)*

between decoders ceases and the output sequence is obtained from one of the decoders.

An interleaver can be placed between the output of Decoder 1 and the input of Decoder 2, to provide an additional weighted decision input into Decoder 2; similarly, a de-interleaver is placed at the output of Decoder 2, to provide feedback to Decoder 1. The decoding time is proportional to the number of interactions between decoders.

Sequential Decoding

A sequential decoder may be used for convolutional decoding and it operates in a similar manner to the Viterbi decoder. On receipt of the incoming code word sequence this decoder will penetrate into the tree according to a decision made regarding the best path to follow.

For that reason, using a trial and error technique, the decoder will progress as long as the chosen path appears correct, otherwise it will backtrack to try a different route. At this point, either soft decision or hard decision decoding is possible with the sequential decoder, although soft decision would considerably increase the computational time and storage space required.

A major advantage of sequential decoding is that the number of states examined is independent of constraint length, allowing the use of large constraint lengths and low error probability. A disadvantage is the need to store input sequences while the decoder searches for its preferred route through the tree. If the average decodes rate falls below that of the average symbol arrival rate, there is a danger that the decoder cannot cope, causing a loss of input information.

Viterbi Decoding

Viterbi maximum likelihood decoding of convolutional codes provides the best possible results in the presence of random errors. Thus, in an attempt to match the output sequence received by the decoder, Viterbi's algorithm modells the possible state transition through a trellis identical to that used by the encoder. Accordingly, the Viterbi decoding algorithm is a maximum likelihood path algorithm that takes advantage of the remaining path structure of convolutional codes.

This method works by modelling the possible state transitions of the encoder and finding the output sequence that matches most closely to that received by the decoder. Its task is to realize that not all paths through the encoder states can contribute to the final decoded output and that many paths can be rejected after each frame is received, which keeps the problem to manageable proportions.

If the encoder remembers (v) bits, then there are 2^v possible memory states to be modelled by the decoder. Hence, this term dominates expressions for speed, complexity and cost of the decoder and currently imposes an upper limit of 8 to 10 on constraint length. By path maximum likelihood decoding means that of all the possible paths through the trellis, a Viterbi decoder chooses the convenient path, most likely in the probabilistic sense to have been transmitted.

Viterbi decoders easily make use of either hard or soft decision making. This decoding can incorporate soft decisions very simply, which will almost double the error correction power of the code and this can provide an additional gain of up to 3dB. Otherwise, the procedure for choosing the best Viterbi scheme is to maximize constraint length within the limits of cost and speed, to find a nonsymmetrical code with the best value of d_∞ and to use soft decisions. The maritime Inmarsat standard-B and multipurpose M standards utilize an 8-level soft decision Viterbi decoding in their channels (constraint length = 7).

Error Correction

There are several methods (such as ADPCM) that reduce the number of redundant bits in speech, audio and visual signals in order to make more economic use of bandwidth. First of all, it is necessary to consider methods that require the deliberate addition of redundant bits to messages. The added bits are very carefully chosen and error correction systems make it possible to achieve large savings in the power required to realize low BER.

At the receiver the additional bits are used to detect any errors introduced by channels. To achieve this technique in MSC are employed: FEC, ARQ and Pseudo-noise and Interleaving. In such a way, it is also possible to combine FEC and ARQ in an integration form known as a Hybrid Error Correction (HEC) transmitting scheme.

At this point, however, the HEC method is used to reduce BER and the number of retranslated blocks. Such an arrangement could also be used to provide feedback information to the transmitter regarding slow variations, such as a fading.

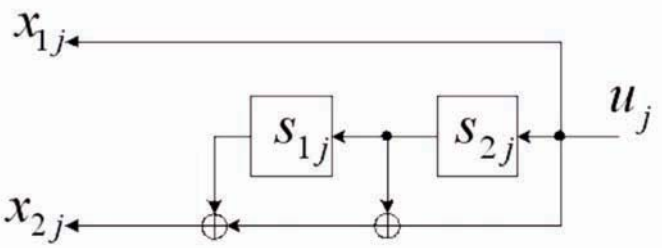

Figure 3: Decoding of convolutional codes (the Viterbi algorithm)

Forward Error Correction (FEC)

The FEC is a technique where errors are detected and corrected at the receiver. Thus, this scheme requires only a one-way transmission link, since the message contains parity bits used for detection and correction of errors. In such a way, it is working only on receiving Tlx mode in radio and satellite one-way transmissions. The basic FEC technique used in MSC can be classified into two major (already explained) categories such as Convolutional and Block codes. The FEC coding as a result of convolutional coding is used in Inmarsat standards for some voice, telex and signalling channels. For example, Inmarsat standard-B uses convolutional encoder of constraint length 7- and 8-level soft decision Viterbi decoder. The coding rate is either 3/4 or 1/2, while for voice channel the code rate 3/4 is used and is derived by puncturing the rate 1/2 with k = 7 convolutional code.

On the other hand, the association of both basic coding techniques results in an even more powerful FES scheme known as the concatenated coding system. This powerful FEC scheme has been introduced in recent years for a considerable increase of the service quality without appreciable expansion of bandwidth. While the inner code, with Viterbi decoding, can correct a large part of the random errors and very short error bursts, the residual errors at the outputs of the Viterbi decoder tend to be grouped in bursts. Thus, using a properly chosen interleaving that cuts the error bursts into shorter ones, a high rate Reed-Solomon code can be used as the outer code in order to correct most of these dispersed errors bursts to achieve a very low bit error rate. Thus, the introduction of concatenated coding and trellis-coded modulation into MSC is the most remarkable event in the domain. The list of FEC techniques along with their performance is introduced in **Table 1**.

An FEC scheme can improve the quality of a digital transmission link by the following two aspects: (a) A bit error rate reduction, closely related to the service quality criterion and (b) a saving in the E_b/N_0 or C/N_0 to be considered in the link budget. The E_b/N_0 or C/N_0 saving is often called the coding gain, expressed in dB as a difference at certain BER values, of the coded system and the reference noncoded one. In the comparison between different transmission schemes, E_b/N_0 is usually used because it is independent of the coding scheme, where the gain is given as follows:

$$\mathbf{G = (E_b/N_0)\ ref - (E_b/N_0)\ cod}$$

The merit of a coding system can also be appreciated in terms of the savings in C/N_0 and C/N, then, considering information rate (R_b) and information transmission bandwidth, the equations for carrier-to-noise density ratio (C/N_0) and the carrier-to-noise ratio (C/N) are:

$$\mathbf{(C/N_0) = (E_b/N_0) + \log R_b \text{ and } (C/N) = (E_b/N_0) + \log R_b - 10\log W}$$

A coding gain in Eb/N0 means in general a gain in C/N but the coding in C/N depends on the bandwidth expansion with respect to the reference system. It is however possible to have a coding gain without bandwidth expansions using Trellis Coded Modulation (TCM).

Automatic Request Repeat (ARQ)

The ARQ is a technique with which a high degree of data integrity is required and latency is not a significant factor. In reality, the ARQ scheme, based on error detection coding and a retransmission protocol, is well adapted to the situation where a two-way channel is available. Typical examples of such systems can be encountered in a computer data network using satellite links. However, it is worthy of notice that the ARQ and improved ARQ, as well as HEC techniques, are widely used in modern digital communications and storage systems.

The ARQ method requires a two-way link, since a receiver, detecting an error, does not attempt to correct it but simply requests the transmitter to retransmit the message. Thus, the ARQ scheme basically works with the following modus:

1. **Stop and Wait ARQ –** After each message block is sent via satellite link, the transmitter waits for acknowledgement. If the message block received is in error, the transmitter will retransmit that block but if this message is correctly received, the next message block is transmitted. A half-duplex link is required, transmission on the link is possible in both directions but not at the same time.
2. **Continuous ARQ with Repeat –** The transmitter sends and the receiver acknowledges message blocks continuously. Hence, any message block not correctly received causes the transmitter to return to the block in question (incorrect received block) and recommence continuous retransmission from there. A full-duplex link is necessary for transmission in both directions simultaneously.
3. **Continuous ARQ with Selective Repeat –** In this ARQ arrangement only the block received in error is retransmitted and the transmitter continues from where it left off at the last block, instead of repeating all the subsequent even correctly received messages. In such a manner, however, full-duplex link is also necessary for transmission in both directions simultaneously.

A major advantage of ARQ compared with FEC is that decoding equipment for error corrections can be simpler and the redundancy in the total message stream is less. The ARQ efficiency is good for low error ratios but for high ratios requiring retransmission of a large number of message blocks, the system becomes inefficient. A disadvantage of ARQ is the variability of the delays experienced from end-to-end of the link and so, the possible

requirement for large data stores of incoming data blocks.

The Inmarsat standard-C uses packets of data and each one transmitted contains a 16-bit checksum field. After that, the receiver completes an expected checksum for each packet and compares this with the actual packet received in order to verify that the packet has been correctly received. The ARQ method is used if the packet received is in error.

Pseudo Noise (PN)

The PN generator will produce a set of cyclic codes with good distance properties. Thus, the name of the sequence is given, because the sequence, although deterministic, appears to have the properties of sampled white noise. Furthermore, a PN sequence is easily generated using shift registers, and has a correlation function that is high packet for zero delay and approximates to zero for other delays. The PN sequence, being deterministic, is usually for synchronization purposes between a transmitter and receiver.

Some Inmarsat standards use a scrambler circuit before FEC encoding and a descrambler at the receive end following FEC decoding. For Inmarsat standard-B and M, for instance, the scrambler/descrambler circuits are PN generators using 15 stages. The scrambler/descrambler circuits are clocked at the rate of one shift per information bit. The first bit into the scrambler at the beginning of a frame is modulo-2, added with the output of the scrambler shift generator, corresponding to the initial state-scrambling vector. The initial state of the shift register is located at the beginning of a burst and a frame.

Considering the Inmarsat standard-M, the initial state of the scrambler shift registers at the LES (for SCPC channel operating in voice mode) and is sent to the LES by the MES at the start of a call as part of a call set-up sequence. The MES chooses any initial state (except all zeros) on a random basis for each call and signals this scrambling vector message (8D in hexadecimal form or 10001101) for implementation at the LES with the Least Significant Bit (LSB) in shift register No 1 and the Most Significant Bit (MSB) in shift register No 15 of the scrambler. The MES simultaneously sets the descrambler shift register with the same scrambling vector. Otherwise, for MES-to-LES channels, a fixed initial state default value of 6,959 in hexadecimal form or 110100101011001, is used in MES scramblers and LES descramblers.

Interleaving

As is well known, the MSC transmission channel introduces errors of a bursting nature. Hence, in the short term, the errors introduced by the channel cannot be considered to be statistically independent or memory less, the criterion upon which most coders (block and convolutional) optimally operate. In order to mimic a statistically independent channel, a technique known as interleaving is incorporated into the transmitter chain after the output of the encoder and from the interleaver the input signal passes via the modulator.

In reverse mode the output signal goes through the demodulator, deinterleaver and channel decoder. This circle presents the interleaver/deinterleaver segment within the transmission/reception chain in the satellite link. Hence, the role of the interleaver is to re-order the transmission sequence of the bits that make up the code words in some predetermined fashion, such that the effect of an error burst is minimized.

Interleaving can be performed for both block and convolutional codes. Block interleaving is achieved by firstly storing the output code words of the encoder into a two-dimensional array. Consider the case of an $(m \cdot n)$ array, where (m) is the number of code words to be interleaved and (n) is the number of code word bits. Thus, each row of the array comprises a generated code word. Once the array is full, the contents are then output to the transmitter but in this case, data is read out on a column-by-column basis.

Generally speaking, the transmission of each symbol of a particular code word will be non-sequential. Namely, the input signal goes via the input sequence into the interleaver block and after processing the output sequence would correspond to the chain starting with C_{11}, C_{21}, C_{31}, C_{41}, C_{51}, C_{61}, C_{71}, C_{12}-C_{72}... until C_{18}-C_{78}. At this point, the effect of any error bursts will have been dispersed in time throughout the transmitted code words. Convolutional interleavers work along similar lines, achieving performance characteristics similar to block interleaving.

At the receiver, the inverse of the interleaving function is performed by a deinterleaver and the original code words are reconstituted prior to feeding into the encoder. Namely, a burst of error affecting the transmitted bits indicated by the chain coming from interleaver block would be dispersed among the code words at the receiver. ■

If you missed Part 1 of this article you can order the digital copy of that issue by going on line at ***www.electronicsworld.co.uk***

CODE	DECODING TECHNIQUE	GAIN (BER=10-5)	GAIN (BER=10-8)	BIT RATE	COMPLEXITY
Convolutional	Threshold	1.5 – 3.0	2.5 – 4.0	Very High	Low
Convolutional	Viterbi (Soft Decision)	4.0 – 5.0	5.0 – 6.5	High	High
Convolutional	Sequential (Hard Decision)	4.0 – 5.0	6.0 – 7.0	High	Low
Convolutional	Sequential (Soft Decision)	6.0 – 7.0	8.0 – 9.0	Medium	Low
Concatenated (Convol./RS)	Viterbi Inner and Algebraic Outer	6.5 – 7.5	8.5 – 9.5	High	Medium
Concatenated (Short Block/ RS)	Soft Inner and Algebraic Outer	4.5 – 5.5	6.5 – 7.5	Medium	High
Short Block Linear	Soft Decision	5.0 – 6.0	6.5 – 7.5	Medium	High
Block (BSH/RS)	Algebraic (Hard Decision)	3.0 – 4.0	4.5 – 5.5	High	Medium

Table 1: *Performances of FEC techniques*

THE NEW MICRO-USB CHARGER

Paving the Way for Simplification

Huw Muncer

HUW MUNCER OF TYCO ELECTRONICS'S CIRCUIT PROTECTION BUSINESS UNIT IS ALWAYS ON THE ROAD. AS A SALES MANAGER, HE SEES WHAT ENGINEERS ASK FOR AND NEED, BUT ALSO HOW AN ENGINEER'S JOB HAS CHANGED OVER THE YEARS

THE DESIGN ENGINEERS I meet day to day have to stay on top of all the industry standards and regulations that come around at regular intervals. One such standard, the Micro-USB, is now hitting the headlines and causing quite a stir in the electronics industry. The adoption of this new standard will, I believe, have far reaching implications for electronics designers.

The new Micro-USB charger standard for mobile devices was initiated by the European Commission's 'Universal Charging Standard' for selected top-end devices. The idea behind the specification is to harmonise mobile devices by having one USB charger specification. Apple and at least 13 other leading manufacturers have already announced they will adopt Micro-USB on a global basis – and across all products – by 2012.

A key driver influencing the Micro-USB standard is the demand from environmental agencies to eliminate unnecessary e-waste. Not only is a USB charger smaller and more power-efficient in comparison to today's chargers, it also has strong environmental benefits since it will reduce the need for many different chargers that ultimately wind up in land-fill sites. In addition to helping the environment, consumers are also benefactors of this change. The one-plug scenario means that frantically searching to find the "right" charger for each cell phone or PDA will be a thing of the past.

"As I have seen in my 15-plus years as a components salesperson, changes in electronics standards are something that design engineers have to deal with on a regular basis"

So, how will this game-changing standard affect the electronics industry and, more to the point, the engineering designers who design the devices that require wired connectivity? I believe that this change will both help designers and offer opportunities to components manufacturers.

I remember when the IEEE 1284 standard was adopted in the early 90s. Before this standard defined parallel communications between PCs and other devices, having different standards ate up design time, forcing designers to consider the multiple variables and their influence on each design. Generally this meant that the designers would have proprietary FPGAs to control the numerous serial, USB and parallel ports sticking out the back of the device – all to accommodate the wide variety of user preferences. Ultimately adopting IEEE 1284 allowed printer manufacturers to build one less item into their product. This simplified the design process for electronics engineers and also paved the way for USB connectors.

Similarly, since Micro-USB is a "universal" charging specification, its adoption will simplify the connector for mobile devices. Mobile handset manufacturers will reduce costs by not having to supply a different adaptor for each product they produce. More importantly, this will allow designers to concentrate their design time and efforts on enhancing the functionality of the connected device versus the cable that it connects to. Now OEMs will be able to pick and choose from a wide variety of charging suppliers that can provide standard compliant chargers rather than relying on costly proprietary solutions.

As I have seen in my 15-plus years as a components salesperson, changes in electronics standards are something that design engineers have to deal with on a regular basis. As the new Micro-USB initiative moves forward, they will again be faced with both a challenge and an opportunity and I look forward to working with them in their development of strategic, creative and effective solutions.

So who's up for the wireless charging challenge? That's another story. ■

If you'd like to comment on this subject please write to the Editor at ***Svetlana.josifovska@stjohnpatrick.com***

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TESTING PORTABLE AUDIO PLAYERS FOR NOISE REGULATION COMPLIANCE

JOE BEGIN, DIRECTOR OF TECHNICAL SUPPORT AT AUDIO PRECISION (AP) GIVES ADVICE TO DESIGNERS AND MANUFACTURERS OF PORTABLE AUDIO PLAYERS AND HEADPHONES OF HOW TO BEST TEST THEIR PRODUCTS

MANUFACTURERS OF portable audio players and headphones must test their products against various regulations adopted around the world to protect users from excessively high sound levels. The regulations are a response to studies that have shown a high correlation between these excessive levels and permanent hearing loss.

In the 31 European CENELEC (Committee for Electrotechnical Standardization) member countries, products sold must comply with BS EN (British Standard / European Norm) 50332. It specifies that portable audio players with headphones (or earphones), whether packaged together or bought separately, shall not deliver a maximum sound pressure level exceeding 100dBA. It does not apply to acoustically open or acoustically closed headphones that are normally used with mains-operated home stereo receivers, nor does it apply to headphones used for medical purposes, or active noise cancelling headphones.

In this article, we'll delve into the procedures used to test to this standard. Note that other regions of the world may follow other standards that require different testing methods and have different limits.

Figure 1: *Testing headphones with a G.R.A.S. KEMAR 45BA mannequin and an Audio Precision APx526 analyzer*

Figure 2: *Ear simulators and microphones inside the head of the Head and Torso Simulator (HATS)*

The BS EN 50332 standard has two parts:

Part 1: General method for "one package equipment", covers portable audio players and headphones that are packaged together and sold as a unit.

Part 2: Matching of sets with headphones if either or both are offered separately, provides standard procedures for measuring:

- The maximum voltage that can be output by an audio player under standard test conditions, and
- The sensitivity of a set of headphones or earphones – a measure of what sound pressure level they will produce for a given input voltage, under standard conditions.

Head and Torso Simulator

A Head and Torso Simulator (HATS) is required for measuring the headphone sound levels. A HATS is a special mannequin (see **Figure 1**) used for sound quality assessment, engineered to have head and torso dimensions representative of a typical adult. In this article, we use a KEMAR 45BA mannequin, provided courtesy of G.R.A.S. Sound and Vibration.

The HATS is equipped with a pair of removable pinnae (the outer visible section of the ear), molded from a soft rubber-like compound, and mechanical couplers called Occluded Ear Simulators at the locations of the inner ears, to simulate the mechanical impedance of the ear to incoming sound (see **Figure 2**). Measurement microphones are situated at the location of the eardrum.

Measuring the sound pressure level at the eardrum is necessary to account for the interaction between the headphones and the ears. However, to correlate sound pressure levels measured at the

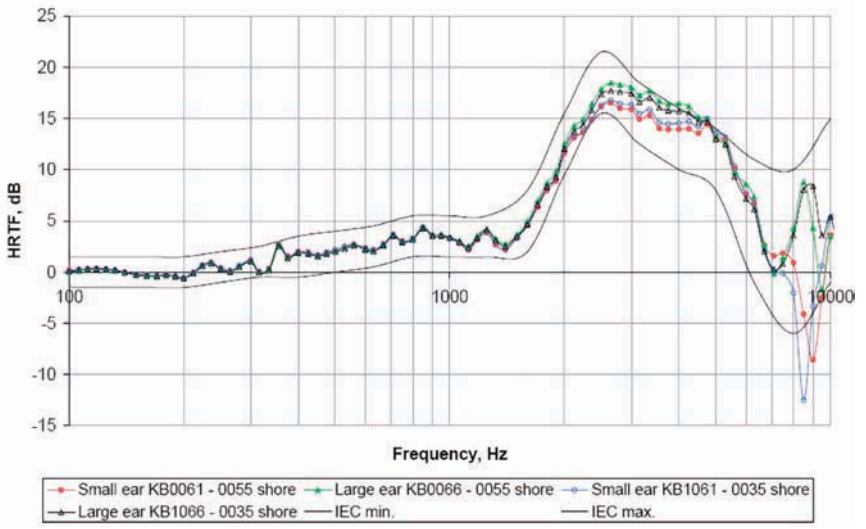


Figure 3: *HRTFs for the KEMAR 45BA mannequin with different styles of pinnae*

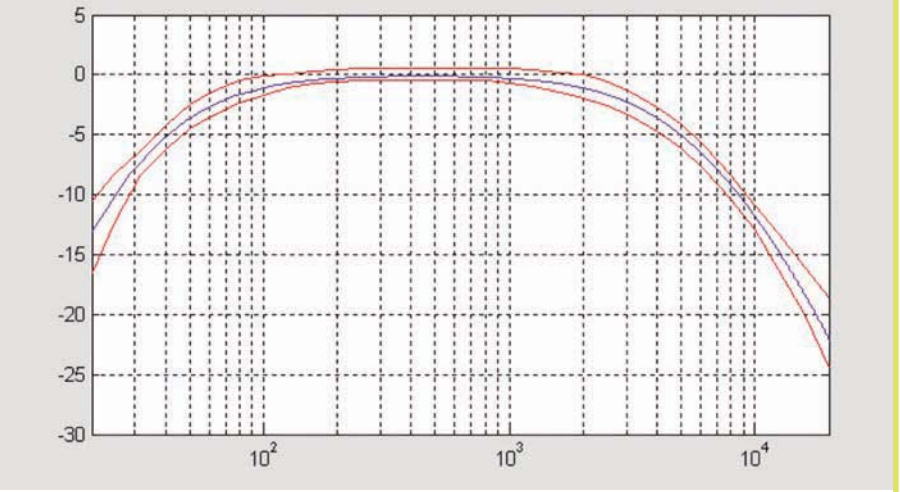


Figure 4: *Frequency response in dB of the program simulation noise filter*

eardrum with published data from hearing impairment studies and international standards, the raw data must be converted to free field values. This is accomplished using the free field frequency response of the HATS, which represents the difference, as a function of frequency, between the sound pressure level at the ear simulator microphones when the mannequin is present and when it is not.

The free-field frequency response of the HATS is sometimes referred to as the Head-related Transfer Function (HRTF). The graph in **Figure 3** shows HRTFs for the KEMAR mannequin with different styles of pinnae.

Test Signal

BS EN 50332 requires the use of a special test signal called "program simulation noise", whose spectral content is representative of music and speech. Real music cannot be used for the test signal because music continuously fluctuates in both level and spectral content. Pure tones cannot be used either, because the results would be inaccurate due to the considerable variations in the frequency response of typical headphones.

The program simulation noise can be created by passing pink noise through a special filter network defined in IEC 60268-1. BS EN 50332 adds an additional requirement – that the crest factor of the test signal (the ratio between the instantaneous peak level of the signal and its RMS level) be between 1.80 and 2.2.

We used Matlab to create a digital filter having the same frequency response as the analogue filter network described in IEC 60268-1. We then passed pink noise through the filter, adjusted its crest factor using a soft clipping algorithm and set its level to -10dBFS. The result is saved as a wave file, which can be played out through the generator section of the Audio Precision APx526 audio analyzer we used for the tests.

BS EN 50332-1

To make the measurements in Part 1, the program simulation noise is played on the portable player, with volume and tone controls set to maximum. The headphones are mounted on the HATS, and the sound pressure level measured by the two ear simulator microphones is averaged and plotted with 1/3 octave resolution. Then the HRTF (Head-Related Transfer Function) of the HATS is subtracted to derive the free-field response. The resulting curve is A-weighted and then the overall sound pressure level is calculated in dBA. This process is repeated five times, remounting the headphones on the mannequin each time to average out any variation in placement.

BS EN 50332-2

Part 2 of BS EN 50332 specifies how to test portable audio players and headphones that are not sold as a package. Unlike packaged sets, the sound pressure level that could be developed in this case cannot be specified in terms of a single metric. Instead, it requires two characteristics: the maximum output voltage (Vm) of the player and a characteristic called the "Wide Band Characteristic Voltage" for the headphones.

Audio Player Maximum Output Voltage

The audio player maximum output voltage (Vm) defined by the standard is the unweighted true RMS voltage at the load, measured using an averaging time of 30 seconds or more, using the program simulation noise signal. The player's volume and tone controls are set to maximum, noise reduction (if present) is turned off and the output is terminated with a resistive load of 32Ω.

Figure 5: *Calibrating the microphones*

Player	Headphones
Vm ≤150 mV	WBCV ≥ 75 mV

Table 1: *BS EN 50332-2 limits*

Headphone/Earphone Wide Band Characteristic Voltage

The Wide Band Characteristic Voltage (WBCV) is measured by driving the headphones with an amplifier (output impedance 2Ω or less) instead of with the portable audio player. WBCV is defined as the unweighted true RMS voltage measured at the headphones, when the sound pressure level at the HATS is 94dBA. If the headphones are known to be linear, then the test does not have to be conducted at 94dBA; instead the WBCV can be calculated from the measured sound pressure level and RMS voltage using the equation in the standard.

Limits

BS EN 50332-2 specifies limits (see **Table 1**) for the player maximum output voltage and the headphone Wide Band Characteristic Voltage. Note that headphones having the minimum allowed WBCV of 75mV driven by a player putting out the maximum allowed Vm of 150mV would be expected to develop a sound pressure level a factor of two (or 6dB) higher than the level of 94dBA at which WBCV is measured. This corresponds with the 100dBA limit of Part 1 for a matched set of player and headphones.

Running the Tests

To facilitate running the BS EN 50332 tests with our Audio Precision APx526 audio analyzer, we've created a special utility. The utility guides the user through the required steps for Parts 1 and 2 of the standard and produces a summary of the results along with detailed graphs. This makes it easy to quickly and reliably verify compliance with the standard. A sampling of tests we've conducted on a few portable audio players and headphones, including one matched set, are shown in **Table 2**.

We've presented here an overview of the procedures and equipment involved in testing portable audio player and headphone volume levels for BS EN 50332 compliance. Technote 107, available for download at ap.com, expands on this article and includes specific instructions for running the tests on our APx Series audio analyzers.

Joe Begin is Director of Technical Support at Audio Precision

If you missed any parts of this series you can order their digital issue copies online at ***www.electronicsworld.co.uk***

Device Tested	Player/headphone SPL per BS EN 50332-1 (dBA)	Player Vm	per BA EN 50332-2 (mV)	Headphone WBCV per BS
Portable audio player #1 with earbud type phones (matched set)	106.7*		255*	72*
Insert-type earphones				60*
Suprea-aural headphones				382
Closed circunaural headphones †				149
Open circumaural headphones †				188
Portable audio player #2			145	
Smart phone			179*	

Table 2: *Test results for various sample devices.* *† Value is outside BS EN 50332 limits*

The Differential Gain Stage DIF

Burkhard Vogel presents a series of short features with general remarks on triodes in audio applications

WIDELY USED IN professional applications differential (or symmetrical or balanced) amplification circuits increasingly conquer the HiFi enthusiast's audio equipment, thus, objectively improving signal-to-hum ratios drastically (= 1st advantage) and, according to many test magazines, subjectively improving the sound of the pre-amp/amp/ loudspeaker chain too. The price to pay: to get fully balanced equipment each amp-chain has to be doubled.

A typical differential gain stage is given in **Figures 1** and **3**. **Figure 2** shows the respective equivalent circuit. Gen1 in Figure 1 can be replaced by the Figure 3 alternatives. The shown two alternatives will influence the common mode rejection ratio (CMRR) very differently (see respective graphs).

V1 and V2 must be perfectly matched; hence a double-triode serves always best. Tiny imbalances of the circuit can be trimmed by a low-valued trim-pot P1. Rc, as part of the trim-pot, is the resistance between cathode and current generator of each valve. The current generator acts as short-circuit for the signal currents of each valve. That's why V1 and V2 can be taken as CCS gain stages (see Part 2 of this series). With $r_g = r_{g1} = r_{g2}$ = infinite, $r_a = r_{a1} = r_{a2}$, $\mu = \mu_1 = \mu_2$, $g_m = g_{m1} = g_{m2}$, $R_a = R_{a1} = R_{a2}$, $R_c = R_{c1} = R_{c2} = 0.5*P1$, $R_L = R_{L1} = R_{L2}$ and $R_o = R_{o1}+R_{o2}$ the basic R_L dependent gain equation becomes:

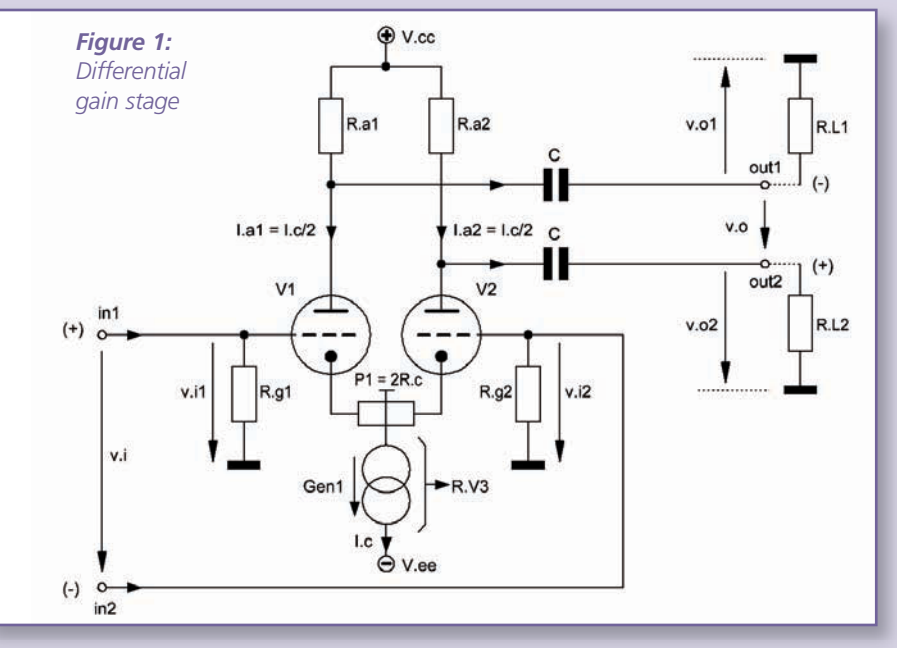


Figure 1: *Differential gain stage*

$$G_D(R_L) = \frac{v_o}{v_i} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = -\mu \frac{R_a}{R_a + [r_a + (1+\mu)R_c]\left(1 + R_a R_L^{-1}\right)} \quad (1)$$

and the output resistance Ro is thus:

$$R_o = R_{o1} + R_{o2} = 2\frac{R_a[r_a + (1+\mu)R_c]}{R_a + r_a + (1+\mu)R_c} \quad (2)$$

The second advantage of the DIF gain stage is the fact that the input capacitance $C_{i.D}$ becomes only half of the value of the input capacitance of one of the two CCS gain stages (C_{i1} or C_{i2}). With $C_i = C_{i1} = C_{i2}$ (for the calculation see Part 2) it becomes:

$$C_{i.D} = \frac{C_i}{2} \quad (3)$$

The same applies to the output capacitance $C_{o.D}$. With $R_g = R_{g1}+R_{g2}$ the magnitude of the DIF input impedance Zi.D(f) can be calculated by:

$$Z_{i.D}(f) = \left|R_g \| C_{i.D}\right| \quad (4)$$

The amplifier's third advantage is its ability to suppress unwanted common mode signals by a rather high common mode rejection ratio CMRR. Here, Figure 3 plays the main role. Gen1 can be taken as a resistance RV3. It could be a pure resistor R3 that creates a lower CMRR than, as the alternative, an active valve current sink with the differential resistance "$r_{a3}+(1+\mu_3)R_{c3}$", thus creating a much higher CMRR.

Figure 4 gives us the RL dependent common mode gain $G_{CM}(R_L)$:

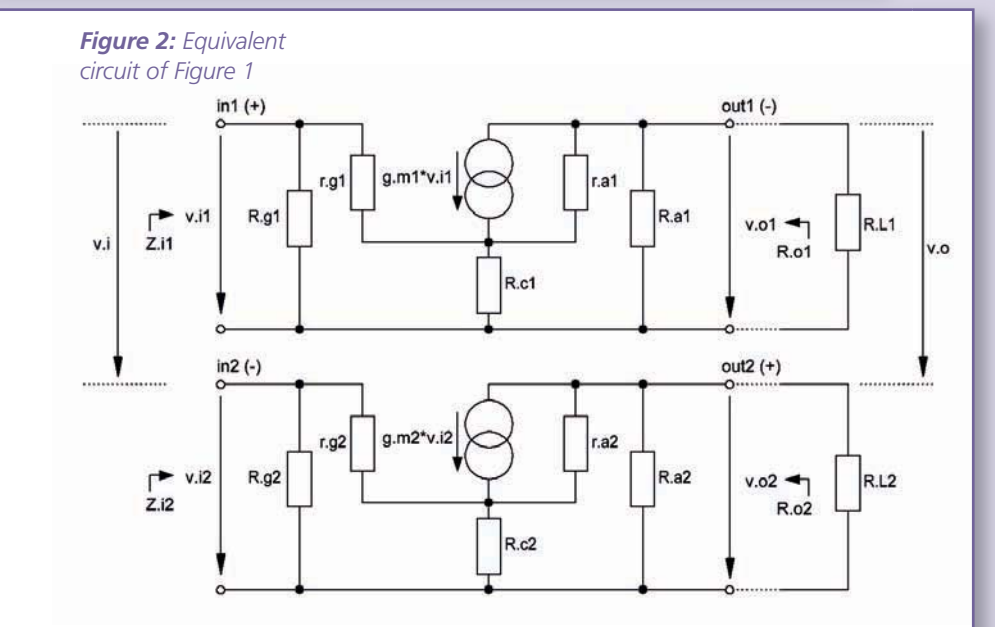


Figure 2: *Equivalent circuit of Figure 1*

Figure 3: *R_{V3} alternatives*

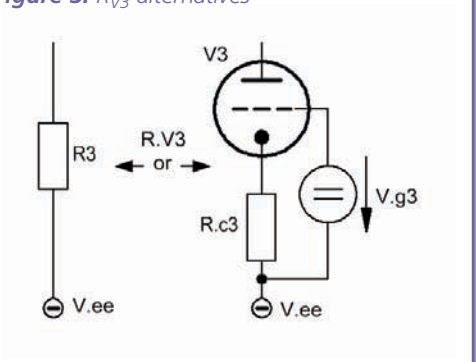


Figure 4: *Equivalent circuit for the common mode i/p voltage situation of V1 and V2 respectively*

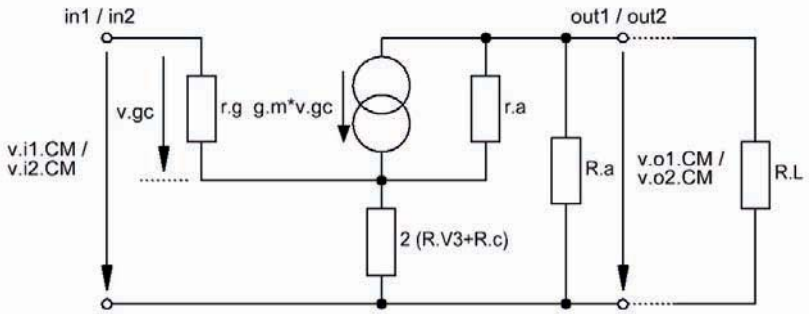


Figure 5: *DIF gain G_D vs. anode current I_a ($I_c = 2I_a$, $R_L = 1M\Omega$, $R_c = 50\Omega$) (in all figures only rather small result deteriorations will occur by halving the operating DC voltages)*

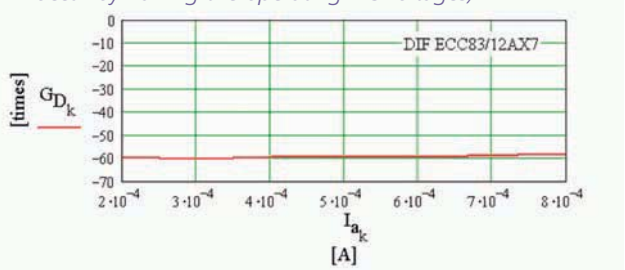


Figure 6: *DIF gains vs. R_L ($I_a = 0.6mA$, $R_a = 170k\Omega$, $R_c = 50\Omega$, $G1_{CM}$ with V3 and $R_{c3} = 82.5k\Omega$, $G2_{CM}$ with R3 = 250kΩ)*

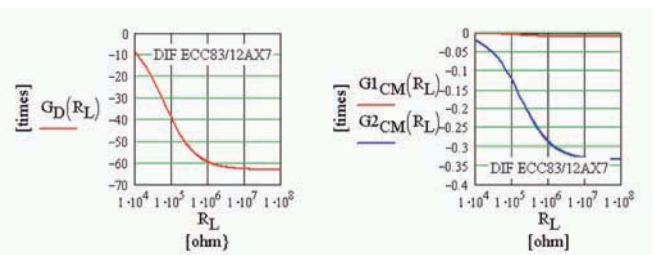


Figure 7: *DIF CMRR vs. I_a (CMRR1 with V3, CMRR2 with R3, R_L = 1MΩ, R_c = 50Ω)*

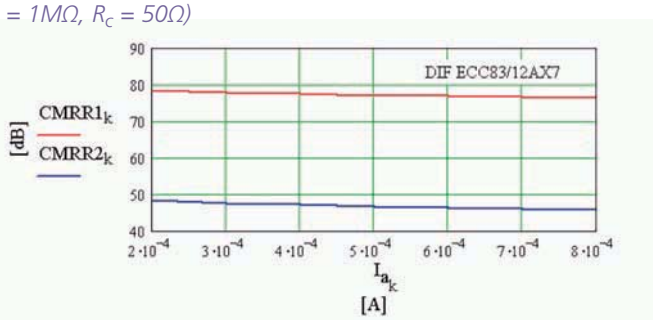
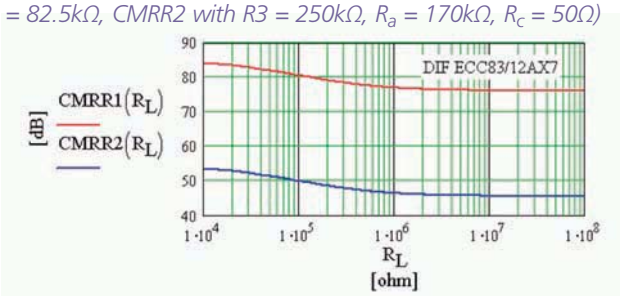


Figure 8: *DIF CMRR vs. R_L ($I_a = 0.6mA$, CMRR1 with V3 and R_{c3} = 82.5kΩ, CMRR2 with R3 = 250kΩ, $R_a = 170k\Omega$, $R_c = 50\Omega$)*



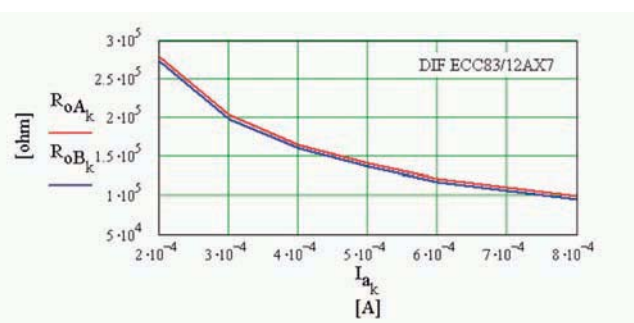
$$G_{CM}(R_L) = \frac{v_{o1CM} + v_{o2CM}}{v_{i1CM} + v_{i2CM}} = -\mu \frac{R_a}{R_a + [r_a + 2(1+\mu)(R_{V3} + R_c)](1 + R_a R_L^{-1})} \quad (5)$$

and, basically, for the CMRR we obtain:

$$CMRR = 20 \log\left(\frac{G_D}{G_{CM}}\right) \quad (6)$$

The graphs are based on the following assumptions: example valves for V1, V2: ECC83/12AX7, for V3: ½ECC83. With constant values for V_{cc} = 300V, V_{ee} = -300V, $V_{a1} = V_{a2} = V_{a3}$ = 200V we get **Figures 5** to **9** (note: a changing Ia automatically leads to a changing Ra and R3; "k" indicates the number of the six I_a values from 0.2mA to 0.8mA). ■

Figure 9: *DIF output resistances R_o vs. I_a (R_{oA}: R_c = 50Ω, R_{oB}: R_c = 0Ω)*



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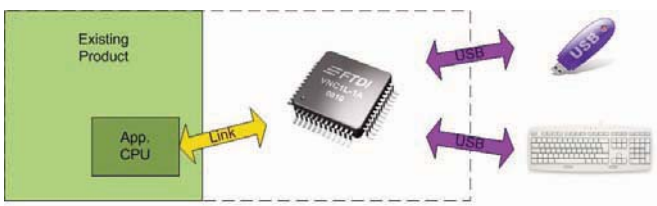
Adding a USB Flash Drive to a PRODUCT

John Hyde from Future Technology Devices International (FTDI) will implement a series of USB projects over the course of the following editions of Electronics World

Figure 1: *Vinculum-I operates as an attached device*

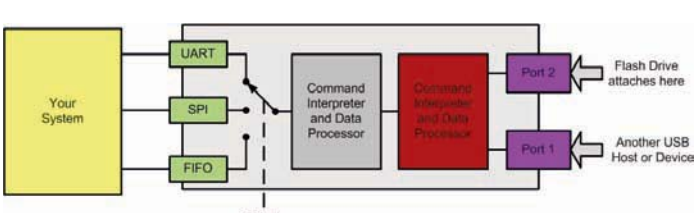


THE FLASH DRIVE is arguably the most successful USB product to date. Its density has increased almost logarithmically over the past decade, while its price has fallen at a similar rate. Today you can buy 4GByte drives for just a few pounds. Up until now, however, they have been excluded from embedded projects due to the complexity of interfacing.

The major issue here is that a Flash drive is a USB device and, therefore, controlling it calls for a USB host controller. The USB specification deliberately puts most of the communications complexity within the host controller, since there is only ever one in a system, and this enables USB devices to be simpler and therefore lower cost.

A Flash drive is a mass storage class device and, although these specifications are a free download from www.usb.org, they are not easy to read. This is not surprising because they are specifications and not implementation guides. Additionally, these mass storage class specifications only define basic track/sector, read/write operations so we also need to understand specifications of the FAT file system, as used on all commercial Flash drives, to be able to read/write user data. The amount of information required to understand how to just connect a Flash drive is becoming overwhelming. What we need is a component that implements these specifications for us – after all, they are industry standard specifications that we have almost no freedom to change anyway, we just want to use them.

Figure 2: *Options for adding USB*



The Vinculum-I dual USB host controller runs a firmware monitor that is controlled by an external application CPU using an SPI, FIFO or UART link. Several firmware versions are available that implement a variety of specific functions but all include the ability to read and write to a USB Flash drive.

Vinculum-I provides a DOS-like, command line interpreter, front-end to a Flash drive. A Vinculum block diagram is shown in **Figure 2**. Internally it is implemented as a microcontroller, with specialized IO devices, running embedded firmware, but we do not need to know this. Vinculum-I's command line interface is accessed via a UART, SPI, or a FIFO. The device actually supports two USB ports and each can be programmed to be a host or a device but in this article we will only discuss a single host port with a connected Flash drive.

We use the FT232R USB-to-serial cable to connect a PC running HyperTerminal at 9600 baud with an FTDI evaluation module called VMusic, as shown in **Figure 3**. Ignore the name for now, we won't use the "music" part until the second example; for now, this is a Vinculum-I mounted on a board with a convenient serial connector. Plug your Flash drive into the USB A socket of the board.

The board will sign on and offer a D:> prompt. Now, in HyperTerminal, enter "DIR" and the contents of the drive will be displayed. Now enter the following commands:

OPW test1
IPA
WRF 12
Hello World!
CLF test1

These commands first open a file called "test1" for write, then tell the Vinculum that 12 bytes of data are coming. "Hello World!" is the data that is written, and CLF closes the data file. Then remove the Flash drive and connect it to your PC/Mac/Linux system and open test1. Notice that the data written by the Vinculum is present.

Edit test1 to add a message "Hello from my PC, Mac or Linux", then reattach the Flash drive to the board and enter "RD test1". Voila, the new text is displayed.

We have thus written, read and exchanged data files between a PC/Mac/Linux system and an embedded system using a Flash drive. We did not have to learn USB, the mass storage class specification or even the FAT file system. It was as easy as entering DOS-like commands on a serial connection.

Vinculum-I powers up in Extended Command mode where all the

commands and data are ASCII; some of these commands are summarized in **Figure 4**. It can be switched into Short Command mode where binary commands/data can be exchanged. The VMusic board only provides access to the UART connection but this will be enough for examples here. Vinculum-I is also available in an OEM 24 pin DIP and this additionally provides access to the SPI port, parallel port FIFO and the other USB port.

I will present two types of project suitable for a Vinculum-1 plus Flash drive – data distribution and data collection. Typically, data to be distributed is created on a PC using specialist tools and then copied onto a Flash drive; an embedded system then accesses this information and presents it to a user or a machine.

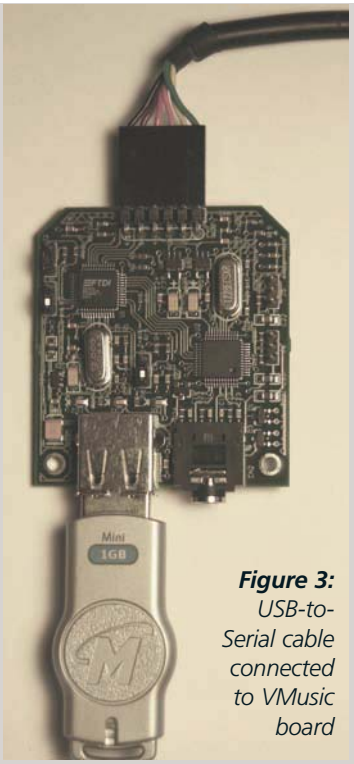


Figure 3: *USB-to-Serial cable connected to VMusic board*

My example is a small JPEG viewer and MP3 player. We will discuss the data collection example (a portable data logger) in the next part of this series. In both cases an application microcontroller is used to control the Vinculum-I since it is a peripheral device.

JPEG Viewer and MPEG Player

Here a Cypress Semiconductor PSoC serves as the application microcontroller since it has firmware-configurable hardware, allowing us to solve a wide range of problems with a single device. We can develop and debug using a high-end PSoC device that has ample analogue/digital resources then, near project completion, a lower cost device within the same family can be used. For the first example we shall use the Cypress PSoC development board (shown in **Figure 5**) with the VMusic evaluation board and a 1.5" x 1.5" micro-LCD display already attached to the breadboard area.

The PSoC reads image files off a Flash drive using commands sent to the Vinculum monitor, then sends this image to the display. If a matching MP3 file is also present on the Flash drive then we can command Vinculum-I to play it – this could be music or a person talking. A PC is used to create the image and MP3 files and these are copied onto the Flash drive. The PSoC/Vinculum-I based player then "runs the show". A JPEG viewer and MPEG player is the base example, but an interactive display that could be used in stores, museums, art galleries, etc. is a straightforward design extension. A series of Flash drives in English, Spanish, Japanese, etc. could be used to create a more universal solution.

The size of the display determines the complexity and choice of the PSoC. Since this example is about embedded Flash drive applications, the simplest display has been implemented – an inexpensive, serial interface, 128x128, micro-LCD. The micro-LCD module is a very capable subsystem that supports graphics rending and several fonts. This example uses about 5% of its capability as we just download images to it. These images are 128x128 by 16-bit colour and a PC application called Graphics_Composer can convert JPEG, BMP and GIF images into this format (this is included in the download package). In this example these images will be copied to a Flash drive and called nnn.img (nnn = 000 to 999). MP3 files are also created for each image and they will be called nnn.MP3 (these could be your favourite songs renamed).

From an application software perspective we have a PSoC interfacing two serial connections, a Vinculum-I and a micro-LCD connection. The application starts by looking for 001.img and copies it to the display. If it finds 001.MP3 then it will play it, or else it will wait for 60s before moving onto 002.img. The application keeps incrementing through filenames until one is not found then it starts at 001.img again. To change the photos and/or music/spoken words you just need to swap the Flash drive. It is easy to expand this design to add functions such as buttons and navigation.

If you missed any other parts of this series you can order their digital magazine issues by going on line at ***www.electronicsworld.co.uk***

Figure 4: *Some of the monitor's DOS-like commands*

	Directory Operations
DIR	Lists the current directory
MKD <name>	Creates a new directory <name> in the current directory
DLD <name>	Deletes the directory <name> from the current directory
CD <name>	The current directory is changed to the new directory <name>
CD ..	Move up one directory level
	File operations
RD <name>	Read file <name>. This will return the entire file
OPR <name>	Opens file <name> for reading with 'RDF'
RDF <size>	Reads <size> bytes of data from the current file
OPW <name>	Opens file <name> for writing with 'WRF'
WRF <size>	Writes <size> bytes of data to the end of the current open file
CLF <name>	Closes file <name> for writing
DLF <name>	This will delete the file from the current directory and free up disk space
VPF <name>	Play an MP3 file. Sends file to SPI interface then returns
REN <n1><n2>	Rename a file or directory

	Management Commands
SCS	Switch to the short command set
ECS	Switch to the extended command set
IPA	Input data values in ASCII
IPH	Input data values in Hex
SUD	Suspend the disk when not in use to conserve power.
WKD	Wake Disk and do not put it into suspend when not in use
SUM	Suspend Monitor and stop clocks
FWV	Get Firmware Versions
FS	Returns free space in bytes on disk

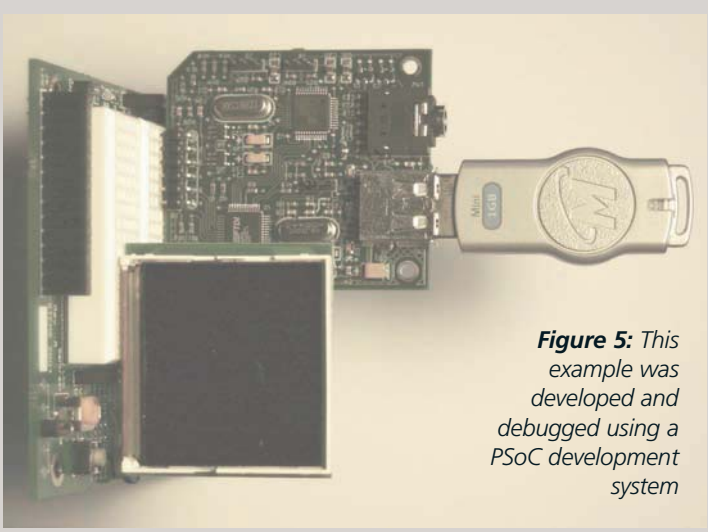


Figure 5: *This example was developed and debugged using a PSoC development system*

MISLEADING CONCEPTS

PLEASE EMAIL YOUR LETTERS TO:
svetlana.josifovska@stjohnpatrick.com

I read the Audio Tutorial by Dave Mathew ('*Test and Measurement System Grounding*' in EW December 2010, page 18) initially with interest, then with surprise and, finally, with incredulity. After a century of development of electronic systems, a rich fund of knowledge has accumulated on the subject. In spite of this, an experienced designer advocates the use of 'Star-Point Grounding' and warns against the creation of 'Ground Loops'.

Back in 1954, when building my first valve radio, I took advice from a more experienced engineer. He used very similar reasoning to that employed by Dave Mathew to recommend that I drill a hole near the centre of the chassis, fit a bolt with a number of solder tags and connect all the return leads to that point. The radio worked fine – apart from the fact that there was an ever-present hum from the speakers. This was due to coupling of interference from the valve heater supply to the amplifier stages. I never willingly implemented the single-point ground in any of my future designs.

Several projects in the aerospace industry could be quoted which suffered from troublesome interference due to the existence of a single-point ground in the system. These problems demonstrated conclusively that the concept was a thoroughly bad idea.

Nor is the concept supported by the theory of electromagnetics. Any search for the terms 'single-point ground' or 'star-point ground' in any book on EM Theory is guaranteed to be fruitless. The same is true of the term 'Equipotential Ground' and the recommendation to 'avoid earth loops'.

Engineers who have been seduced by these concepts have reasoned that EMC can be improved by removing the earth connection from the mains supply to some units of equipment. Not only is this modification counterproductive, it also creates a lethal hazard.

Anyone who believes that these concepts are perfectly valid and then tries to analyse and understand the phenomena of electromagnetic interference is faced with an insoluble conundrum.

If, however, these concepts are abandoned and a real attempt is made to relate EMI to electromagnetic theory, then it is possible to formulate a few simple design guidelines. One of the most important is to allocate a return conductor to every signal conductor and route the two conductors as closely together as possible.

A set of such guidelines, backed up by analysis based on Electromagnetic Theory and the results of practical tests, can be found in section 1.5 of the book '*Circuit Modelling for EMC*'. This book is freely available in portable document format (pdf) at **www.designemc.info**. The website contains a feedback page for comments. Of course, anyone who champions the concept of the 'Star-point Ground' or the concept of the 'Equipotential Ground' is also free to write to the editor of EW.

It might also be useful to bring their attention to section 8.3 of the book '*Circuit Modelling for EMC*'. This section illustrates how the single-point ground configuration creates a high level of intra-system interference and how the introduction of ground loops dramatically improves the situation.

Ian Darney UK

Audio Precision (AP) responds:

AP stands by its article. The key point is that "star grounding" is a macro concept that applies at a system level between a number of different sub-systems or devices that must be interconnected. It is not intended to be a design guideline at the individual circuit level as Mr Darney has apparently extrapolated.

AP will be the first to acknowledge that within a given sub-system or device, good design favours the minimization of susceptibility to external influences.

Stray magnetic fields are among the worst offenders in audio design, and Mr Darney's example of a valve heater supply is a good example. Other sources include the power transformer and certain display devices. Very careful attention needs to be paid to minimizing loop areas formed by critical signal paths within each circuit and its common or ground reference. Most seasoned engineers recognize that "star grounding" in this context is almost always inferior. One does not achieve the exquisite performance level of Audio Precision test instruments by accident, or by blindly following dogma.

However, when it comes to inter-connecting a number of different audio devices, each of which has its own safety ground, a much different situation arises. This is the reason balanced analogue I/O becomes mandatory in serious professional applications. It inherently allows one device to reject the unavoidable common mode ground potential differences that exist between different boxes.

With all due respect to Mr Darney's opinion, "star grounding" provides the minimum amount of ground potential differences between different products in most audio systems. Exceptions can arise when a major source of interference must be located close to or within the same system (for example, a device with a massive power transformer spewing a relatively large stray magnetic field). However, it has been our experience that even with these challenging circumstances, one can usually rearrange the physical relationship of the different devices to minimize the coupling of the stray magnetic field into the most sensitive devices.

If you would like to comment on this subject on any other that you have read on in Electronics World magazine, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com

The publisher reserves the right to edit and shorten letters due to space constraints

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NANOETXEXPRESS 2.0 CREDIT CARD-SIZED COM EXPRESS COMPUTER-ON-MODULES

Parallel to the nanoETXexpress Industrial Group, today Kontron announced the approval and release of the nanoETXexpress 2.0 specification for ultra small COM Express Computer-on-Modules.

The PCI Industrial Manufacturers Group (PICMG) identified the need to adopt the COM Express specification to the new capabilities for ultra-sized modules with latest processor technology. With the COM Express specification rev. 2.0, PICMG laid the groundwork for ultra-sized modules by adding the Type 10 pin-out, a next generation to the previously introduced Type 1 pin-out. Keeping in line with the COM Express specification, the nanoETXexpress specification rev 2.0 implements all relevant parts of the current COM Express specification. The definition of the new pin-out Type 10, which provides another evolutionary path for modular solutions in addition to Type 1, is the most impactful update to the nanoETXexpress specification as it puts more capabilities within reach for embedded application developers.

www.kontron.com

TWO-WIRE HALL-EFFECT UNIPOLAR SWITCHES

The new A1152/3/5/6 from Allegro MicroSystems Europe are a range of two-wire unipolar Hall-effect switches designed for automotive sensing applications in seat-belt buckle, seat position and steering lock applications.

The new devices are produced using the Allegro advanced BiCMOS wafer fabrication process and include improved high-voltage transient protection: a critical factor for automotive applications where external protection circuitry cannot be located close to the sensor.

These Hall-effect switches are factory trimmed to optimise the accuracy of the magnetic switch points and employ a patented high-frequency four-phase chopper-stabilisation technique to achieve magnetic stability over temperature and to eliminate the offset inherent in single-element devices, when exposed to harsh automotive environments. The advanced chopping technique also provides significantly reduced jitter and shorter power-on times.

Two-wire unipolar switches require one less wire for operation than the more traditional open-collector output switches and also offer diagnostic capability as there is always current present at one of two specified levels.

www.allegromicro.com

LOW-COST, ON-SITE MEASUREMENT OF SOIL THERMAL PROPERTIES

Labcell has introduced the Decagon Devices KD2 Pro soil thermal properties meter for civil engineering contractors that need to know the thermal properties of the soil backfill when laying electrical cables. Compared with traditional thermal properties analysers, the handheld, battery-powered KD2 Pro instrument costs around one-tenth of the price and can be taken on site to obtain readings in just two minutes with no calibration procedure necessary. Furthermore, the instrument is robust, with stainless steel housings and probes, and easy to use thanks to clear LCD displays and intuitive operator interfaces.

To avoid the risk of thermal runaway, it is important to check the native soil's thermal resistivity and calculate the cable's maximum current capacity. The KD2 Pro does this quickly and simply, giving a direct reading in m°C W^{-1}. Measurement ranges are 0.25 to 50m°C W^{-1} for thermal resistivity, 0.02 to 4 Wm^{-1} $°C^{-1}$ for thermal conductivity, 0.1 to 1.0mm^2s^{-1} for thermal diffusivity and 0.5 to 4MJm^{-3} $°C^{-1}$ for specific heat.

www.labcell.com

AMD DELIVERS THE WORLD'S FIRST AND ONLY APU FOR EMBEDDED SYSTEMS

AMD announced immediate availability of the new AMD Embedded G-Series processor, the world's first and only Accelerated Processing Unit (APU) for embedded systems. The AMD Embedded G-Series, based on AMD Fusion technology, delivers a complete, full-featured embedded platform and incorporates the new low-power, x86 CPU based on the "Bobcat" core with a world-class DirectX 11-capable GPU and parallel processing engine on a single piece of silicon.

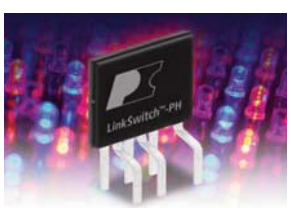
This new class of accelerated processor combines more compute capabilities on a single die than any processor in the history of computing and represents opportunity for major advancements in embedded systems. No solution with this level of advanced computing is available for the embedded market today. Numerous embedded systems based on the AMD Embedded G-Series are available today or expected to launch in the coming weeks from companies including Advansus, Compulab, Congatec, Fujitsu, Haier, iEi, Kontron, Mitec, Quixant, Sintrones, Starnet, WebDT, Wyse, and many others.

www.amd.com

LINKSWITCH-PH FAMILY OF LED DRIVER ICS FOR GENERAL LIGHTING NOW EXPANDED

Power Integrations announced seven new members of its popular LinkSwitch-PH family of LED driver ICs.

Optimized for industrial and commercial settings where high efficiency and system longevity are dominant requirements, the new devices (LNK413-LNK419) are suitable for lighting applications ranging from 3W bulbs to 55W replacements for fluorescent lighting fixtures. The devices, which can achieve up to 88% efficiency, feature a PWM-dimmable single-stage controller with both power factor correction (PFC) and accurate constant current (CC) power conversion functionality. The integrated PFC and CC functions allow multiple drivers to be connected in parallel to drive exterior and street area lights efficiently and with functional redundancy.



LinkSwitch-PH devices incorporate the PFC/CC controller, a 725V MOSFET and MOSFET driver into a single package, which simplifies layout and design and eliminates parasitic elements between the controller and MOSFET.

LinkSwitch-PH devices are available now starting at $1.11 each for 10,000-piece quantities.

www.powerint.com

HARWIN ADDS HORIZONTAL FEMALE HI-REL CONNECTOR TO DATAMATE FAMILY

Harwin has launched a horizontal female version of its popular high performance Datamate 2mm interconnection system, increasing design flexibility. The reverse gender right angle connector enables boards to be connected in parallel or side by side.

The dual row connectors are available in 6, 12, 14, 20, 26 and 34 positions with a 3mm pc tail. For complete mating security, a range of jackscrews are available. Longer (4.5mm) and SM solder tails will be available shortly.

Datamate connector systems are particularly suited to demanding applications such as military, aerospace, data communications, medical and industrial controls where failure is simply not an option.

The Datamate hi-rel interconnection system is already a very wide product family and the introduction of a horizontal female style further increases the possibilities open to creative and innovative design engineers who are continually looking for ways to increase performance and reduce system size and cost.

www.harwin.co.uk

NEW WSMS2908 POWER METAL STRIP METER SHUNT RESISTOR

Vishay's new power metal strip meter shunt resistor is industry's first to offer direct PCB mounting. It features low resistance values down to 100µΩ and 3W power capability in 2908 size package.

This is the industry's first with sense leads designed to be soldered directly to the PCB, eliminating the need for costly flexible leads. The WSMS2908 combines a 3W power capability in the 2908 size package with extremely low resistance values down to 100µΩ.

The resistor features a proprietary processing technique that produces low resistance values; it increases accuracy in current meter shunt applications and provides power companies with more accurate data to determine customer usage and to adjust billing terms. Product benefits also include tolerance of 5.0%, a 5-terminal design and an all-welded construction, very low inductance values of < 5nH, low thermal EMF of < 3µV/°C and is lead (Pb)-free and RoHS-compliant.

Among its market applications are current meter shunt applications for industrial and consumer single or multi-phase energy meters among others.

www.vishay.com/resistors-linear/power-metal-strip/

ITT ICS ADDS NEMESIS LIGHTWEIGHT MINI-CIRCULAR CONNECTORS TO WEBSITE

ITT Interconnect Solutions has announced that its innovative new Nemesis connectors are now available as models on its 3D dynamic modelling website which went live at the end of 2010. This online resource enables design engineers to utilise a single interface to search for ITT ITC's industrial, commercial, Mil-Spec and Hi-Rel interconnects, select from various output model formats and directly request the generation of a 3D model. Users can choose from a range of industry-standard CAD formats and receive the model as a downloadable zip file to import into their own CAD system for integrating into prototype system designs. This greatly increases flexibility and enables a number of different prototype designs be tried out to achieve an optimum solution more quickly and easily.

Providing optimum performance in harsh environments and fully-sealed to IP67 or IP68, Nemesis connectors suit applications where weight and size are critical. These include medical equipment, marine applications and handheld devices.

www.ittcannon.com

NEW COMPACTPCI SERIAL SYSTEM FEATURES HIGH-SPEED DATA TRANSFER CAPABILITY

New from electronics packaging specialist Schroff is a complete 4U, 9-slot subrack system based on the recently released CompactPCI Serial specification. The system takes full advantage of the specification's high-speed serial bus topology to deliver a data transfer rate of up to 32Gbit/s via PCIe, 10GbE, S-ATA, USB 2.0 or USB 3.0 interfaces.

Particularly suitable for applications in the process, industrial control, defence and transportation sectors, the new CompactPCI Serial system comprises a subrack, backplane, fan tray and power supply.

The shielded 19in. aluminium chassis is 4U high and has a depth of 275mm. Featuring a perforated top cover and base plate, it is supplied with front handles and a set of guide rails to enable it to be populated with 3U-high boards. The 9-slot backplane – providing one system slot and eight peripheral slots – conforms to PICMG CompactPCI-S.0 and can be specified with or without rear I/O.

www.schroff.co.uk

RUGGED, CUSTOMISABLE FOOTSWITCH IS INTRODUCED BY FOREMOST ELECTRONICS

Foremost Electronics, the Essex based specialist distributor of electromechanical components, announces the availability of the Marquardt Mechatronik GmbH foot switch.

Suitable for use in harsh industrial environments, including high dust and water areas, the footswitch is protected to IP 65 and IP 67 levels. Employing user-friendly ergonomics the footswitch is a compact robust design with clear tactile feedback and an anti-skid surface with a screw hole option for fixing to the floor.

The 2420 footswitch is a modern, attractive design with many colour choices available on demand, either painted or dyed plastic depending on volumes and customer specific logos may be printed on the rocker. The reliable snap action switching system has a proven high lifetime of over 100,000 operations and a wide range of switching options ranging from low level signals up to powerful 21A currents. The footswitch is available with or without a connecting cable.

www.4most.co.uk

ELEVEN PERFORMANCE-BOOSTING ENHANCEMENTS TO JTAG TECHNOLOGIES'S BOUNDARY-SCAN TOOL

JTAG Technologies has boosted the performance of its industry-leading ProVision suite of boundary-scan development tools with the addition of 11 enhancements. The first of these is the addition of all instructions handling (including private instructions) within ProVision's JTAG Functional Test (JFT) capability, now giving users easier access to device registers.

The second enhancement is the addition of 'netlist type autodetect', which automatically recognises netlist formats as belonging to their respective tool vendors. Thirdly, the WGL test vector format (as used for IC testing) is now supported through a ProVision plug-in.

The fourth enhancement is the ability to test (IEEE) 1149 dot 6 to dot 1 connections. The remaining seven enhancements are: support for FTDI USB to serial port peripheral devices; HTML reporting for TTR and BSD in AEX sequences; the ability to export and re-import AEX sequences; support for double-latching bus logic; boundary-scan register length check; support for multiple ID codes in BSDL; and 64-bit drivers for DataBlaster hardware.

www.jtag.com

NEW CLARE VISOR ENCLOSURES LAUNCHED FOR ENHANCED SAFETY TESTING

The Clare Visor enclosures from Seaward feature a modern ergonomic design to enable production personnel to carry out the safe and controlled electrical testing of a wide range of products in compliance with EN50191. Product is supplied fully wired, fully interlocked and can provide an out of the box solution which specifies safe working conditions for electrical testing.

Constructed from heavy duty insulating plastic, the new enclosure design incorporates a special pallet system to allow the fast and simple insertion of different fixtures to accommodate the testing of a wide range of appliances and electrical/electronic devices. The large clear visor provides a wide field of view and a counter balance lift mechanism provides fast access to the equipment being tested, while requiring minimum effort from the operator.

The enclosures can be fully interfaced with electrical testing instrumentation for automated production line routines and can also be incorporated in laboratory-type environments for testing during product design and development stages.

www.seaward.co.uk

HARTING APPOINTS ROWSE ELECTRICAL TO DISTRIBUTE HEAVY-DUTY CONNECTORS

Harting has appointed Rowse Electrical as a franchised distributor for the company's Han range of heavy-duty industrial connectors. Rowse, based in Plymouth, is well placed to service Harting customers in the South West of England.

John Rowse owner of Rowse Electrical said: "Our criteria for selecting electrical products for our customers have always been quality and depth of product range. Harting, as the market leader, easily meets our targets, and is a welcome addition to our product portfolio."

Simon Asbury, Director of Sales and Market Development for Harting, added: "We are delighted to join forces with Rowse Electrical on this popular connector family. Rowse can offer customers in the South West of England a high level of service with locally held stock, technical backup and a broad product offering. We look forward to a long-term relationship and enhanced developing of our sales programme with Rowse."

www.harting.com

AERCO SOLE ASSEMBLER FOR DEUTSCH 602 CONNECTORS

Under an exclusive agreement with Deutsch, Aerco is now the sole assembler for the popular, industry-leading Deutsch Pattern 602 connectors. By increasing stock levels and expanding its assembly capability Aerco now offers a 'one-stop-shop' for a full range of Pattern 602 connectors including EMC grounded versions, ribbed coupling nuts and orientated connectors. These connectors will be available either from stock or on a five working day lead-time and will be supplied without any minimum order quantities.

Pattern 602 connectors are lightweight, miniature bayonet connectors ideally suited for use in harsh environments in the civil, defence and aerospace industries. Aerco is qualified to supply parts under the Pattern 602 part number make up, Panavia specification (PAN6432-1 and PAN6432-4) or Deutsch proprietary RR series. All parts meet the requirements of MIL-C-26462 series 2.

The range is available in high strength aluminium with cadmium plating as standard and electroless nickel as an option.

www.aerco.co.uk

CHINA CONTINUES TO EXPAND ITS FOOTPRINT IN **THE GLOBAL SEMICONDUCTOR MARKETPLACE**

Throughout the last eight years of ups and downs in the semiconductor industry, the Chinese market has continued to outperform the rest of the world according to a new report from PwC, "*China's impact on the semiconductor industry: 2010 update report*".

Raman Chitkara, Global Technology Industry Leader at PwC said: "China now accounts for 41% of global semiconductor consumption, over 50% of global semiconductor initial public offerings, and employs 25% of the total global semiconductor workforce."

China continues to dominate electronic manufacturing with an increasing share of the global production of electronic devices. Led by this global domination in electronic manufacturing and supplemented by increasing domestic consumption by a growing middle class, China continues to grow its share of global consumption of semiconductors.

Another shining star in China's semiconductor industry is its rapidly growing fabless sector which grew by 17% in 2009 to reach a record $4bn.

Our panel of commentators says the following on this development:

IVOR CATT, ENGINEER AND SCIENTIST, UK:

I am enormously impressed by this news. I totally failed to foresee that the semiconductor activity in places like Korea would be merely the beginning. At some point, obvious problems in the environment of China would be overcome and by its sheer size it would swamp this very important market.

My failed attempts to innovate in the field of microelectronics will be reinforced if, as suspected, it is true that the Chinese are very conservative. If so, they will make no effort to deal with the "von Neumann bottleneck" – the separation of processing from memory. It will also become even more difficult to get going with array processors exploiting fault tolerant architectures, or with liquid cooling directly onto the surface of the microchip, which is necessary to properly exploit today's microtechnology. These are ideas which more than 30 years ago I thought should be the next developmental steps, but still today there is no sign of them being even thought about.

PROFESSOR DR DOGAN IBRAHIM, NEAR EAST UNIVERSITY IN NICOSIA, CYPRUS:

China's achievements in the semiconductor marketplace and her dominance of the worldwide electronic manufacturing should not be underestimated. The workforce employed in the semiconductor industry is increasing at an alarming rate of 10% per year, and currently accounts for a quarter of the global semiconductor workforce, despite the global economic difficulties.

It is clear that the current growth rate will continue as China offers the lowest labour costs in the world. What is also very important is that the Chinese are not "copying", but are actually inventing new electronic products. This is obvious as currently 22% of the newly issued patents in semiconductor industry are from China. Semiconductor companies in Europe should pay attention to what Chitkara said: "If a company wants to be a dominant player within the semiconductor industry then it should have a significant presence in China". Economically, this is probably not a good thing, as China is certain to become the semiconductor giant of the world, and almost all countries will depend on China alone for their electronic supplies, with no alternative sources.

BURKHARD VOGEL, MANAGING DIRECTOR, GERMANY:

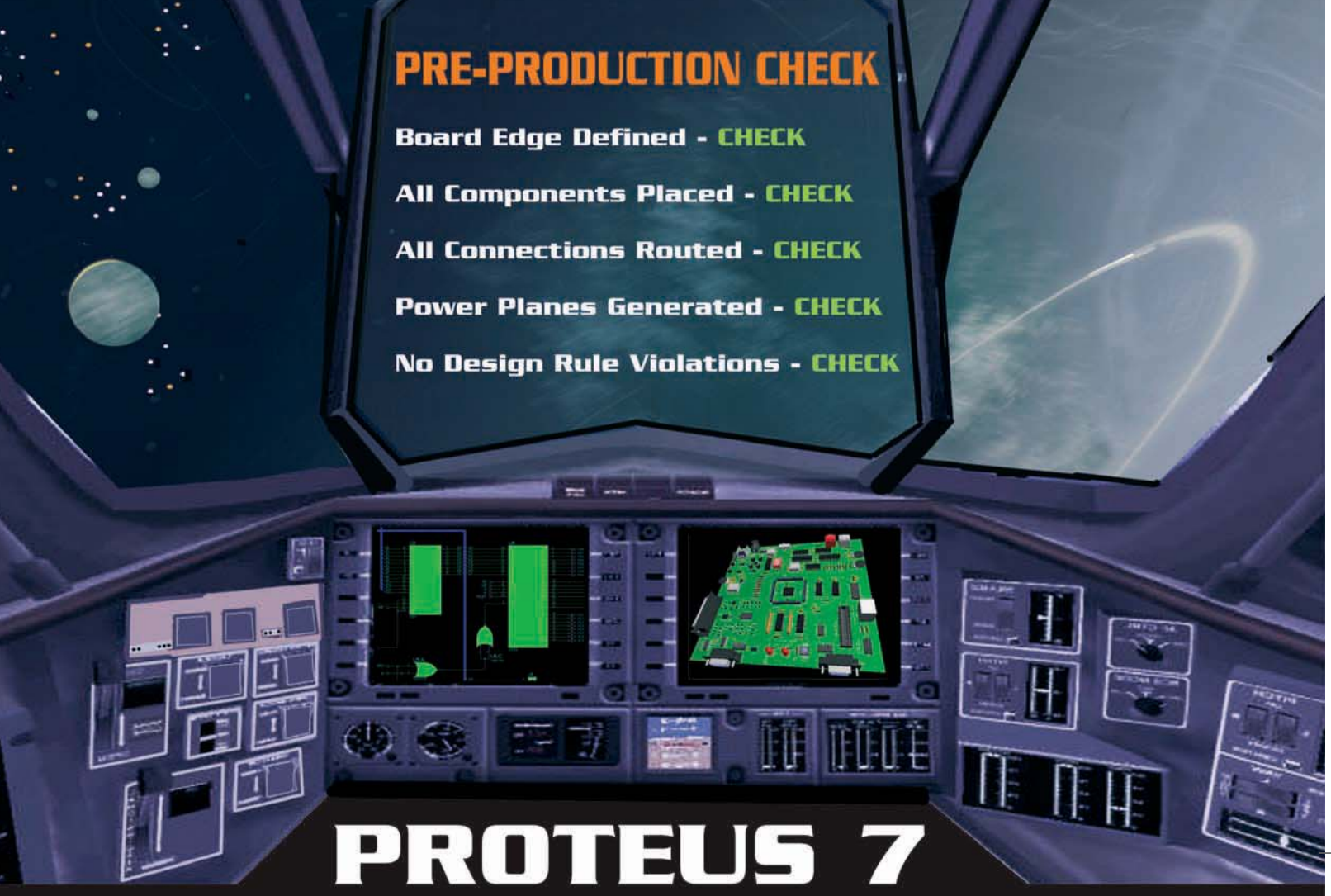
PWC's report on the situation of China's semiconductor industry is right and its recommendations are the right things to follow. China's growing importance on many markets is not threatening the established electronics world. In the '80s and '90s of last century the Japanese economy tried to conquer this part of the western economy too.

In the mid-90s I managed a software company with a big amount of manufacturing control software exports to China. This led to many discussions with Chinese officials on China's strategy to develop its economy. These strategies had also to do with simply copying the Japanese and Korean respective approaches, which, in fact, were not very big problems for them. Copying things has a long-lasting tradition in China (nevertheless, this is one of the major problems for us and it should be solved as fast as possible). A real challenge was – and still is – the advantage and power of our successful western professional training methods and education in modern management and professional skills. That's why we find so many Chinese students in western universities today.

The advantages still held by the western world can only be kept and extended by very much stronger investments in education and formation.

This was the right answer to last century's Japanese economic attack and it should work very well in the current situation too. The budgets of the western countries should reflect this need. I doubt it does. We need China as market for our products and vice versa. Besides the pure economic relationships it will never become a mistake investing additionally in human relations like learning the language, the exchange of students and professionals.

If you'd like to comment on this subject or want to become a member of our panel, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com



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