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***Svetlana Josifovska****, Editor, Electronics World*


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# FEATURES



# REGULARS



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More about Clock Tree Considerations for Base-Station RF Cards on pages 8-9



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# WHAT TO WATCH IN WIRELESS IN 2011!

BY FILOMENA BERARDI

## What will happen in 2011…

- NFC will finally come good. Aided by companies such as Samsung, Nokia, Google and Apple, over 40 million NFC-enabled handsets are projected to be sold in 2011. The long-deferred commercial volumes will finally be shipped.

- Over 85 million IEEE 802.15.4 ICs will be shipped. Driving factors include: the uptake of RF4CE in consumer electronics, displacing IR control; the growth of ZigBee in smart metering and factory automation; and the growing use of 802.15.4 ICs with proprietary software for a wide range of applications, ranging from commercial building automation to agricultural monitoring.

- 802.11 enters the peer-to-peer market in force. For the first time more than one million Wi-Fi-Direct devices are forecast to be sold. Bluetooth high-speed devices will also ramp up in 2H 2011, though many will only be 'Bluetooth high-speed ready' and will not be able to transfer data at true high speed.

- Smartphones will account for over 20% of mobile handsets sold worldwide. Consumer demand will lead handset manufacturers and operators to offer more entry-level smartphone models, using popular open operating systems such as Android. Shipments of this price tier (typically $199 - $299) will grow fastest, to pass 80 million.

- Machine-to-Machine (M2M) communications will grow quickly with nearly 43 million modules being shipped. Market drivers include the near-ubiquitous availability of cellular networks, government regulations, falling hardware prices and lower connectivity tariffs. Despite this, M2M modules will still account for only 3% of all cellular devices sold in 2011.

## And what will take longer...

- Volume shipments of devices using Bluetooth low energy. This will happen only in 2012, when a million are forecast to be shipped, ramping up to over 100 million forecast for 2015.

- LTE accounting for much of the cellular installed base. Of course, long-term it will be huge, but look to 2014 before even 1% of the world's cellular installed base uses it. In the meantime, most carriers will seek to recoup their existing investments in the W-CDMA (UMTS) & HSPA networks to meet increased consumer demand for data.

**Filomena Berardi is a Senior Analyst at IMS Research (www.imsresearch.com)**

> **"AIDED BY COMPANIES SUCH AS SAMSUNG, NOKIA, GOOGLE AND APPLE, OVER 40 MILLION NFC-ENABLED HANDSETS ARE PROJECTED TO BE SOLD IN 2011"**



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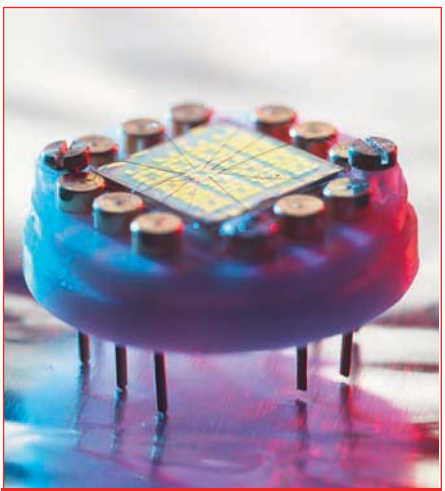
# New research shows how light can control electrical properties of graphene

**New research carried out by a team of scientists from the National Physical Laboratory (UK), Chalmers University of Technology (Sweden), University of Copenhagen (Denmark), University of California Berkeley (US), Linköping University (Sweden) and Lancaster University (UK) has shown how light can be used to control the electrical properties of graphene, paving the way for graphene-based optoelectronic devices and highly sensitive sensors.**



*A light-sensitive graphene/polymer heterostructure*

**When graphene is combined with particular polymers, its electrical properties can be precisely controlled by light and exploited in a new generation of optoelectronic devices. The polymers keep memory of light and therefore the graphene device retains its modified properties until the memory is erased by heating.**

**Light-modified graphene chips have already been used at NPL in ultra-precision experiments to measure the quantum of the electrical resistance. In the future, similar polymers could be used to effectively 'translate' information from their surroundings and influence how graphene behaves. This effect could be exploited to develop robust reliable sensors for smoke, poisonous gases, or any targeted molecule.**

**Graphene is a two-dimensional material made of a single atomic layer of carbon atoms. It is the thinnest material known to man and yet is one of the strongest ever tested. It does not have volume, only surface – its entire structure is exposed to its environment and responds to any molecule that touches it. This makes it in principle a very exciting material for super-sensors capable of detecting single molecules of toxic gases. Polymers can make graphene respond to specific molecules and ignore all others at the same time, which also protects it from contamination.**

# INITIATIVE LAUNCHED TO ACCELERATE THE DEVELOPMENT OF EMERGING TECHNOLOGIES UTILISING GOLD

The World Gold Council announced that it is to play a pivotal role in the transition of new gold-based innovations from 'lab' to 'market'. There has been an explosion of interest in the use of gold in science and technology, mainly driven by the emergence of nanotechnology, yet breakthroughs in research are slow to achieve commercial success due to lack of further targeted investment and support.

The World Gold Council's initiative will help bridge the gap between government-funded early stage research and venture capital-backed commercialisation through investing in gold-related technology in the fields of medical diagnosis and treatment, protecting the environment and renewable energy.


This announcement is accompanied by a new report, *Gold: The hidden element in innovation*, which details how the use of gold has led to the development of ground-breaking advances. As technology continues to progress, gold will be used in a multitude of new products and processes, and the World Gold Council expects these innovations will help address critical needs in medicine and the protection of the environment.

"The role of gold at the heart of many scientific advances is an untold story of innovation. Although little heralded, gold is the hidden element that has increased the efficiency, accuracy and effectiveness of many technologies," said Dr Richard Holliday, Director of Technology at the World Gold Council.

■ STMicroelectronics (ST) and Bluechiip Limited are to cooperate in the manufacturing of unique MEMS-based tracking tags aimed at a range of different markets, including healthcare.
As the bluechiip tracking tag is a mechanical device, it has the unique ability to both survive and read the ID of samples in extremely high and low temperatures, in addition to its immunity to gamma irradiation. This robustness provides significant advantages over more traditional identification or tracking solutions, such as labels, barcodes or RFID technologies, and provides the necessary high levels of data safety in the rapidly growing and labour-intensive healthcare markets, especially in biobanking.

■ The not-for-profit organisation NMI has announced it is to take the next developmental steps to enhance support for its members and encourage broader engagement with the electronic systems community. Building on its accomplishments for the semiconductor sector, the advance represents a natural evolution for the organisation as it seeks to create a more inclusive network across a wider spectrum.
Speaking about the change, Derek Boyd, NMI's CEO said: "We're formally announcing our long term interest to bring closer interaction between chip and electronic systems companies and continue to reach out into key application areas of greatest interest to UK business and R&D operations."


EW will soon not be available through news trade, but don't miss out

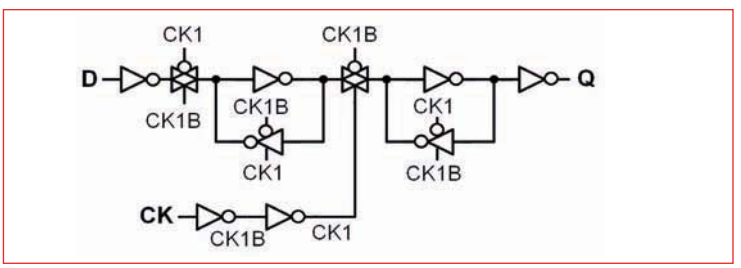
# Toshiba Develops New Energy-Saving Flip-Flop Circuit

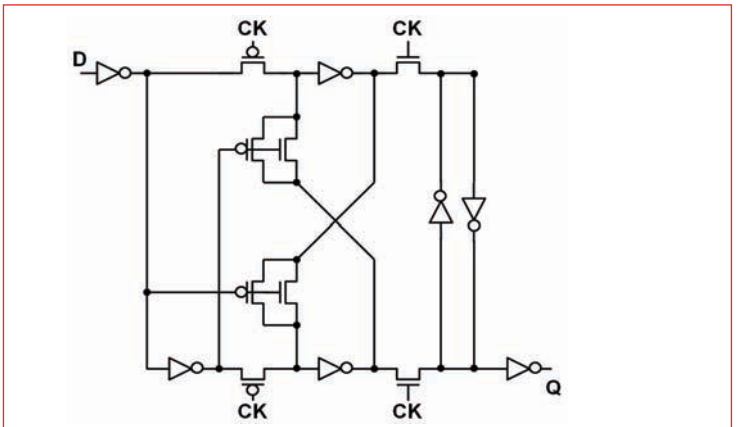
Toshiba said that it has developed a new flip-flop circuit using 40nm CMOS process that will reduce power consumption in mobile devices. Measured data verifies that the power dissipation of the new flip-flop is up to 77% less than that of a typical conventional flip-flop and that it achieves a 24% reduction in total power consumption when applied to a wireless LAN chip.

A flip-flop is a circuit that temporarily stores one bit of data during arithmetic processing by a digital system-on-a-chip (SoC) incorporated in mobile devices and other digital equipment. As a typical SoC uses 100,000 to 10 million flip-flops they are an essential part of SoC designs.

A typical flip-flop incorporates a clock buffer to produce a clock inverted signal required for the circuit's operation. When triggered by a signal from the clock, the clock buffer consumes power, even when the data is unchanged. In order to reduce this power dissipation, a power-saving design technique called clock gating is widely used to cut delivery of the clock signal to unused blocks. However, after applying the clock gating, the flip-flop active rate, a measure of data change rate per clock, is only 5-15%, indicating that there is still plenty of room for further power reduction.

In order to save power, Toshiba changed the structure of the typical flip-flop and eliminated the power-consuming clock buffer. This approach brings with it the problem of data collision between the data writing circuitry and the state holding circuitry in the flip-flop, which Toshiba overcame by adding adaptive coupling circuitry to the flip-flop. With a specific combination of nMOS and pMOS transistors, this circuitry adaptively weakens state-retention coupling and prevents collisions. Despite the addition of the adaptive coupling circuitry, overall simplification of the basic flip-flop configuration reduces the transistor count from 24 to 22, and the cell area is less than that of the conventional flip-flop.




*Conventional circuit configuration (above) vs circuit configuration of the new technique (below)*

IDT Integrated Device Technology

# Clock Tree Considerations for Base-Station RF Cards

Ian Dobson, Director of System Architecture, Integrated Device Technology

## INTRODUCTION

**There are a number of issues that need to be addressed by a clock tree for a fourth-generation (4G) Long-Term Evolution (LTE) or WiMax wireless base station radio card. In addition to the constraints imposed by the Orthogonal Frequency-Division Multiplexing (OFDM) protocols themselves, there are critical aliasing and filtering concerns for ADCs, DACs and RF mixers. These challenges around the modulation elements provide the focus of this article.**

## SIMPLIFICATION OF NETWORK DEPLOYMENTS AND UPGRADES

In order to support the simplification and economy of network deployments and upgrades, OEMs will look for radio card components that support software reconfiguration and can be re-used on multiple similar designs.

Because of the occasional need to support radio cards within a Remote Radio Head, most radio cards will be designed with a single input clock that may be recovered from the link to the base-station. These single input clocks may be poor in quality and significant jitter cleanup may be required in order to adequately generate other clocks on the radio card.

Thus, the core of a radio card clock tree must be a jitter attenuator with programmable output frequencies. The remainder of this article will discuss the performance attributes and why they are required, along with other clock tree requirements.

## RADIO CARD ARCHITECTURAL CONSIDERATIONS

Most radio card designs in base-stations today perform many of the manipulations required to build-up or tear-down the signal for a protocol like LTE or Multi-carrier GSM in the digital domain. It is much simpler to handle error-correction, channel-mapping and splitting the I & Q streams digitally.

The complex data stream of this composite signal also requires very careful filtering / signal processing in both the transmit and receive directions. Doing this in the digital domain avoids the expense of things like precise component-value matching.

Despite the extensive digital manipulations, at some point, the signal must be modulated onto a carrier that can range from 824Mhz – 2.62GHz and transmitted as an analog signal. Most base-station architectures that address multi-channel protocols including LTE, WiMax and multi-carrier GSM use a single stage analog conversion approach as shown in Fig 1.

On the transmit side, the individual sub-carriers are combined into a single stream digitally without being modulated first. This baseband signal is then converted to phase-offset analog I & Q streams by DACs and then up-converted to the transmission frequency via quadrature analog mixers. Variable and fixed gain amplifiers and a duplex filter are used along the path to boost the desired signal to the required strength in its transmission band while adding only a small amount of noise & distortion and simultaneously minimizing energy outside the transmission band to prevent interference with other RF channels.

On the receive side, the RF signal is usually amplified, filtered, and then converted via a mixer to a much lower intermediate frequency (IF) in the 75MHz – 250MHz range where it is further amplified by a variable amount, filtered and finally sampled by a pipeline ADC in accordance with the Nyquist criterion. Down conversion and demodulation of the sub-carriers are then handled in the digital domain. The goal with the receiver is to accomplish this signal conditioning prior to the ADC with a minimum of added noise and intermodulation distortion while avoiding exceeding ADC full scale.

Radio card architects prefer that the clock tree be as integrated as possible. Not only for the reasons described, but because each clock tree component comes with its own jitter contribution that can push the clock signal out of spec. With this integration comes the need to generate not just the RF & IF clocks for modulation, but the sampling clocks for the ADCs & DACs and the clocks for the other digital components such as CPUs, ASICs and FPGAs.

The clocks for these digital components usually have quite lax specifications in comparison to the clocks involved in the RF signal path; period jitter is most often the primary concern. When generating these clocks on the same chip as the more sensitive clocks, there are two issues. First of all, the digital clocks are rarely integer multiples of the incoming clock signal to the radio card and so must be generated with fractional feedback or fractional output divider

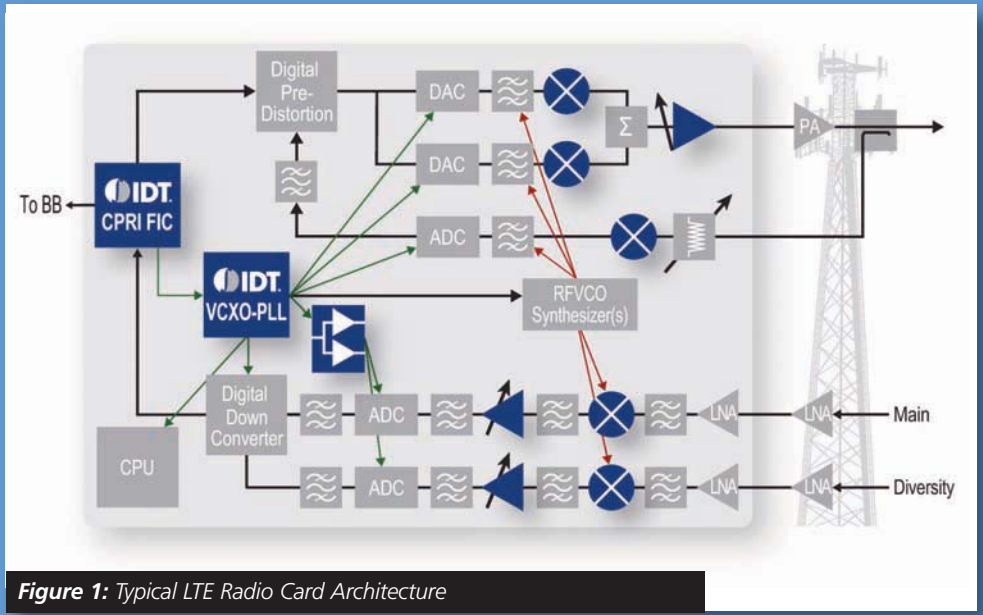



***Figure 1:*** *Typical LTE Radio Card Architecture*

techniques. Both these techniques however, introduce significant spur content within the clock chip and onto the clock outputs. Secondly, digital-chip clocks (or any spurs produced while generating them) that fall near the RF, IF or sampling frequencies can't be filtered out easily and so must be avoided. Even frequency components outside those regions of interest may degrade the SNR either as wideband noise or, if they are not filtered, by aliasing into the critical frequency ranges.

## FREQUENCY EFFECTS OF MIXERS, ADCS AND DACS

Mixers are the analog components used to convert a higher frequency signal to a lower frequency signal or vice-versa. In most base-station radio card designs they currently convert the signal from RF->IF or from Baseband->RF. The main issue of concern with respect to a clock tree design is the issue of frequency aliasing. When multiple frequencies pass through a non-linear device, those frequencies will interact with each other. These interactions are called inter-modulation products.

The function of a mixer is to take two input frequencies and produce an output frequency that is either the sum (up-conversion) or difference (down-conversion) of the two frequencies.

Present-day radio cards are designed to recover signals that are multi-carrier in nature. So, rather than a single tone line of desired signal, the ideal signal consists of a whole series of tone lines evenly spaced throughout the frequency band of interest. These lines represent the individual channels being recovered. Unfortunately as this multi-carrier signal proceeds through a non-linear element like a mixer, each of those channels will inter-modulate each other. The regular spacing of the channels will cause the odd order products to fall almost exactly on top of the channels being recovered. Filters placed before a mixer will be used to attenuate noise that will contribute to even-order products. Filters after the mixer will remove inter-modulation products that fall outside the frequency band of interest, however little can be done about the in-band odd-order products because they fall too close to the wanted signals.

While a band pass filter after the mixer can remove the undesired clean tone lines fairly well, any jitter on the sampling clock will turn those clean tone lines into a skirt as shown in Fig 2. The tails of the skirts from every undesired product will have some contribution within the pass band of the filter; this is referred to as wideband noise. Any clocks generated for the mixers (or ADCs or DACs) must have a very low noise floor in order to minimize their wideband noise contribution.

Unwanted signals called 'interferers' or 'blockers' that get into the mixer's input will have an effect on the specifications of clock signals. They can include other signals received by the antenna or signals internal to the system that get coupled into the receive signal path. While blockers that are widely separated in frequency from the desired signal can be significantly attenuated by the pre-filter, ones close to the desired signal's frequency will pass through. Furthermore, in a protocol like LTE where the wanted signal has a low average power, even a blocker attenuated by the filter may still contain enough energy to compete with the desired signal.

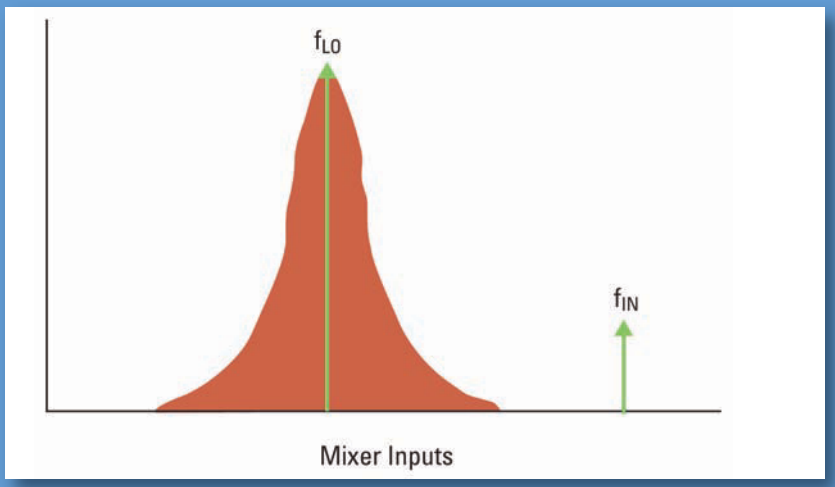



***Figure 2:*** *Effect of reciprocal mixing*

This effect is why the phase noise skirt of the clocks into the mixers must be kept as 'narrow' as possible. The spread of the reciprocally mixed phase noise on the blockers must be kept to a minimum. One of the main challenges in the radio card design is the selection of frequencies on the card with an eye to maximizing the separation of blockers and their inter-modulation products from the frequencies of the wanted signals.

## ADDITIONAL EFFECTS OF JITTER ON ADCS

Because ADCs are sampled data systems and are not perfectly linear in their translations, they too will suffer all the same effects of inter-modulation products between desired input signals, unwanted (blocker) signals and the sampling clock.

However, there is another effect driving the specifications of the sampling clock for the ADC. This is the aperture jitter effect illustrated in Fig 3.

The basic concept is that any uncertainty in the time that a sample is taken can be translated by trigonometry into an uncertainty in the amplitude for that sample. Uncertainty in amplitude results in degradation in the SNR of the ADC. Once the frequency of the input signal is known, a RMS jitter target can be determined for the desired SNR of the ADC. Once that target is arrived at then the intrinsic jitter of the clock tree within the ADC can be factored-out to determine the target RMS jitter spec for the sampling clock.

## EFFECTS OF CLOCK JITTER ON DACS

Digital-Analog Converters (DACs) are used in the transmit path to turn a digital representation of the baseband signal into an analog one for

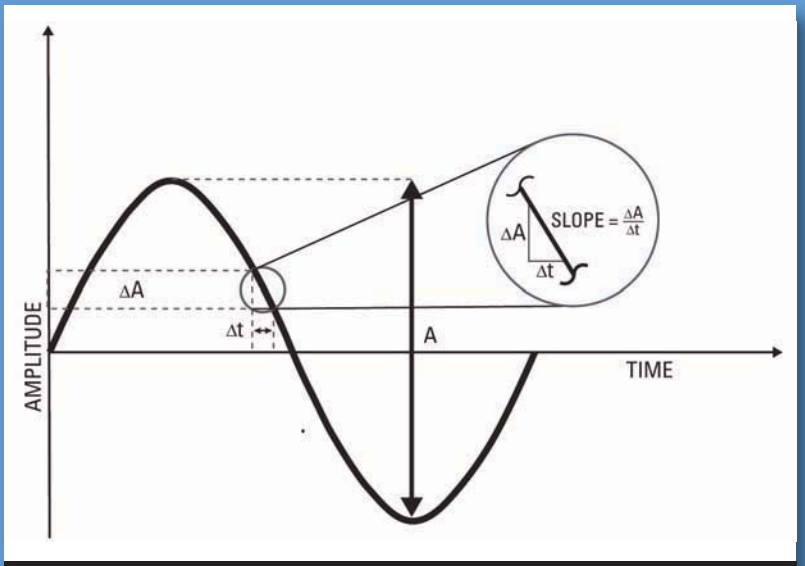



***Figure 3:*** *Aperture jitter in an ADC*

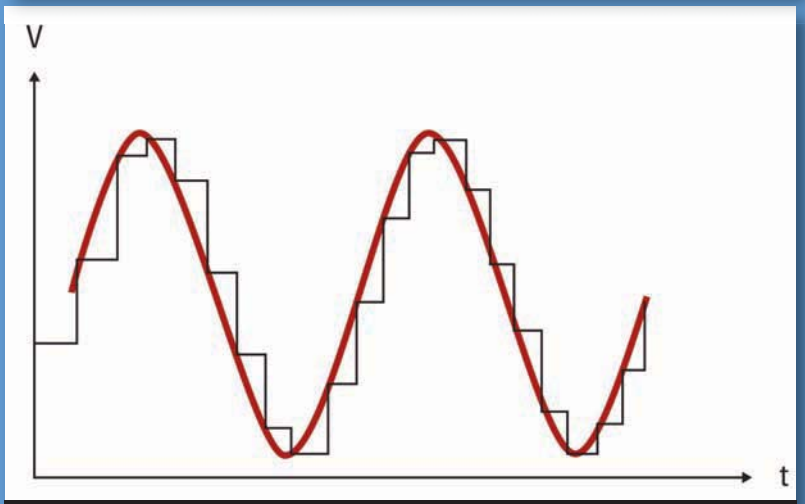



***Figure 4:*** *DAC output compared to ideal output (prior to reconstruction filter)*

subsequent conversion to the RF frequency and amplification to the desired transmit power. The radio card designer will take care in fixing the card's frequency plan to ensure that the sampling frequency of the DAC does not overlap critical frequency bands on the receive side of the card. This is important because DACs suffer from the generation of image frequencies from two potential mechanisms.

The first mechanism is identical to what happens in ADCs and mixers, the convolution of the sampling clock (fLO) and the input signal (fIN) to produce frequencies at N · fLO + M · fIN. This convolution results from non-linearities in the converter. The effects on the requirements for the sampling clock jitter are similar to the ADC.

The second mechanism is an unavoidable result of the way most DACs operate. As shown in Fig 4, at every edge of the sampling clock the DAC's output will switch very quickly to a new voltage level as represented by the digital sample value. This value will be held until the next sampling clock edge. The output only matches the desired waveform once per sample clock.

This results in error energy being introduced. Additionally, most DACs will suffer from some level of clock feed-through, resulting in further spikes at N · fLO. For this reason, the sampling clock frequency will often be considerably higher than required by Nyquist so that the feed-through spikes are well beyond the frequency of interest and so can be easily filtered.

The DAC output waveform will be passed through an analog reconstruction filter to remove as many of these unwanted frequencies as possible. Design of the filter will be easier and implementation will be less costly if the clock jitter and phase noise skirt can are well controlled.

In addition to requirements for specific phase noise levels at specific offsets on the sampling clock, there will also be a specification for RMS jitter integrated over a range of frequencies. This is due to clock jitter causing distortion on the output waveform from the ideal. This will degrade the Total Harmonic Distortion (THD) or Signal-to-Noise-plus-Distortion (SINAD) of the DAC and must be kept within specification to prevent degradation of the radio card's Error Vector Magnitude (EVM). On the transmit side, lower clock jitter can either directly contribute to better EVM or be used to relax the design constraints for Crest Factor / Peak-Average Power Ratio reduction circuitry.

## REQUIREMENTS FOR PHASE ALIGNMENT WITHIN A RADIO CARD

In addition to basic voice and data transmission services, many mobile users are demanding additional services. One example is precise location of the user via triangulation from a set of cell towers. Precise determination of location by radio triangulation is best achieved when all the antennas are transmitting and receiving signals in close phase alignment with each other. Some such services such are requiring separate base-stations to operate with less than 50 nsec of phase discrepancy between them. A radio card will be given a budget of how much phase discrepancy it may introduce relative to other radio cards in the same system. This is another reason why each radio card generates all its frequencies internally from a single clock input signal. It ensures that there is at least a common starting point for phase alignment for all the clocks on the card.

## SUMMARY

RF cards need to generate a variety of clocks from a single, often noisy, input clock. Several of these output clocks will not have an integer relationship to the input clock. All clocks must pay attention to their total noise contribution in order to prevent noise coupling into critical circuitry. Clocks specifically for mixing functions including ADCs and DACs will have tight specs on their RMS jitter as well as on their 'noise skirt' to avoid generating blocker signals in the RF signal paths. The frequencies for these clocks will be carefully planned for the specific implementation details of the card and so are usually unique to each design. Also, a variety of phase delay adjustments must be possible for many of those same clocks. The result of this is a need for a very high-performance clock tree whose specs are essentially custom for each card, ideally implemented in a single component. Devices such as IDT's Netcom timing devices are uniquely positioned to provide those very high-performance devices tailored to the individual RF card design requirements.

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# Scaling Intrusion Prevention Systems for 10G, 40G and Beyond

**Dan-Joe Barry, Napatech's vice president of marketing, takes a look at the distinctive features of Intrusion Prevention Systems (IPS) and how the performance of these systems can be increased to keep up with the relentless development on the bandwidth front**

**THE INTERNET IS** still growing, as we make the transition from Intrusion Detection Systems (IDS) to Intrusion Prevention Systems (IPS) – driven in part by the fact that IPS technology can scale to meet users' needs in the future.

Against this backdrop, we take a look at the distinctive features of IPS and how the performance of these systems can be increased to keep up with the relentless development on the bandwidth front.

Whilst many IT security professionals regard IPS to be a natural extension of IDS technology, the real answer is that IPS is actually another type of access control mechanism, rather than purely a sister IT security platform to IDS.

It may surprise you to know that the term IPS is actually a lot younger than IDS, and is a colloquial term first used by Andrew Plato, a technical consultant with a major IT security vendor that, way back in the late 1990s, developed the industry's first IDS platform.

In its purest form, an IPS makes a number of access control decisions based on the content of the application, rather than taking a traditional firewall approach of monitoring IP addresses, ports and other connective links.

Back in 1998, Andrew Plato opined that a good IPS should feature a sophisticated analytical engine, but one that generates as few false positives as possible. Provided this is the case, he said at the time, then a good IPS has a number of advantages over IDS, since it can sit in line with an IP traffic flow and analyse the data stream in real time.

In addition, most modern IPS solutions also have the ability to analyse Layer 7 protocols such as FTP, HTTP and SMTP, and make decisions on whether to allow – or quarantine – the IP packets as required, even if the data is encrypted.

But are today's IPS platforms up to the task of scanning IP traffic at the high speeds needed in a modern IT environment?

The problem facing IT professionals is that, with the Internet growing at between 40 and 60% a year (source: Atlas Internet Observatory) – and against the backdrop of a mobile data explosion – it's important that IPS technology can keep up with this data bandwidth growth and not become the bottleneck in the network.

It's also becoming clear that, on a typical network of today, users are placing a very load on each port of a multi-10G port system and, whilst there are IPS products available that are capable of supporting a multiple 10Gbps port topology, providing continuous 10Gbps throughput on these ports is a something of a challenge.

The most worrying part of this development is how IPS platforms can be scaled to meet the needs of 40G and 100G IPS technologies, which are set be introduced to the IT/networking mix in the next few years.

Until a few years ago, it could be argued that IPS platforms were up to the task, especially since most IPS platforms adopted a core five-stage real-time analysis process that steps through a number of stages as various IT threats are encountered when monitoring an organisation's data streams that flow both in and out of the IT resource.

> "THE MAJORITY OF [IT HACKING] ATTACKS TODAY ARE CARRIED OUT BY HIGHLY SOPHISTICATED CRIMINAL ORGANISATIONS ATTEMPTING TO STEAL DATA OR HIJACK COMPUTING RESOURCES FOR THEIR OWN ILLEGAL USE"

The first stage is to bandwidth throttle any suspicious IP traffic to give the organisation's IT security software a chance to analyse the data stream – let's take the example of an email message stream – and deal with suspect messages and/or attachments in real time.

If the data is found to be suspect, but does not conform to known infection signatures, then the second stage is for the message's header to be analysed and, if an infection etc., is found, the data can be quarantined.

The third stage in the analysis process involves performing user management and address validation, typically by applying a number of automated checks to verify whether the message comes from a source previously known to be dangerous.

The fourth stage involves applying an anti-malware and anti-hacking analysis engine for anything suspicious that has passed the first three analysis stages but does not pass muster.

The fifth stage, typically involves using the analysis engine to weed out anything that still looks suspicious for later, manual, analysis by the IT security staff concerned.

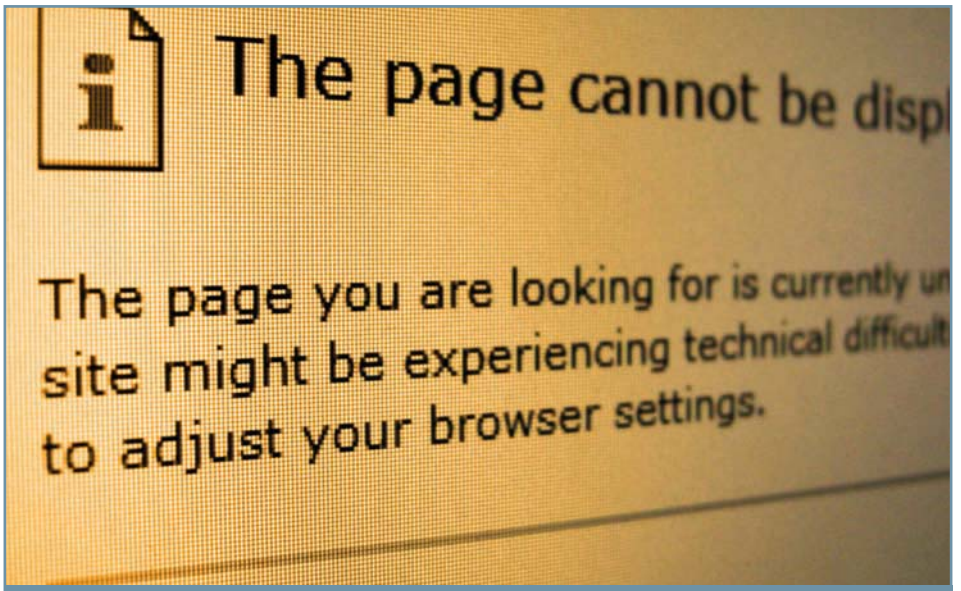
However, the increasing sophistication of malware, together with the recursive and obfuscated coding approach taken by an increasingly criminal hacking fraternity – and, of course, the higher network speeds seen on today's networking systems – means that IPS systems are under pressure to keep up, both in terms of handling the amount of data, but also in having the raw horsepower to run more sophisticated algorithms.

### How Serious is the Threat of an Intrusion?

A recent online poll carried out by Napatech found that a quarter of respondent firms have suffered a network intrusion.

The interactive poll amongst more than 300 attendees at one of our online events, found that 25% of respondents had experienced an intrusion incident, with 44% of these incidents occurring within the last 12 months.

The important thing to realise here is that network intrusion events are not just an irritation – as they were back in the early days of IT networking – but they can be commercially damaging. This is because,




*A typical error page*

unlike the altruistic 1980s – when the 'hackers' of yore tended to be fellow engineers who also had access to the dial-up modems, expertise and other IT resources that were required to gain access to other businesses' online assets – the majority of attacks today are carried out by highly sophisticated criminal organisations attempting to steal data or hijack computing resources for their own illegal use.

These Napatech online poll results were confirmed by a PricewaterhouseCooper-sponsored survey, details of which were announced at the recent Infosecurity Europe show in London. That survey showed that 83% of smaller organisations had experienced a security incident in the last year, compared with 45% two years earlier.

The PwC/Infosecurity survey also revealed that 90% of all organisations had increased their expenditure on IT security technology, whilst smaller businesses are now spending 10% of their IT budget on security issues, compared to 7% two years ago.

The report attributes the rise partly on the increasing use of cloud computing and social networks within enterprises. Delving into the study reveals that 15% of large companies noted IPS systems are under pressure to keep up, both in terms of handling the amount of data, but also in having the raw horsepower to run more sophisticated algorithms that their IT resources had been accessed by an unauthorised outsider in the last 12 months, and 25% had suffered a denial-of-service attack – double the number logged in the last survey carried out two years earlier.

The report also found that the rate of adoption of newer technologies has accelerated over the last two years, with most respondents now using wireless networking, remote access and VoIP technologies. In addition, the number of organisations allowing staff to have remote access to their systems has also increased with around 90% of large companies now offering this facility.

These figures confirm that our Napatech online poll is on track and that the number of intrusion incidents is definitely on the rise. This, in turn, is also forcing most organisations to increase the proportion of their IT budget they spend on security technologies.

## Raising the Security Game

Businesses are not just increasing their IT security budgets, however, they are also raising their game when it comes to security strategies. Given this scenario, the key challenge now is scaling these systems to keep up with the increasing bandwidth generated by richer content in emails and on Web sites, more video and teleconferencing and the transition to cloud computing already taking place.

The important thing to realise is that all these innovative services provide a new and high-speed avenue of attack for hackers. And because of this, network security systems need to react in real-time to contain the problem.

To keep up with these high-speed, real-time demands, the traditional approach of network security appliance vendors has been to invest in the development of customized, proprietary hardware. But, a new approach is emerging where off-the-shelf standard PC server hardware is being used negating the need for hardware development.

The Napatech poll revealed that the majority of network security appliances being used are still based on proprietary hardware, but for every three proprietary systems, there are now two systems based on standard PC server hardware.

In the past, PC servers have not been powerful enough to meet the demands of security applications like IPS, but the latest generation of PC servers provide significant processing power and a strong roadmap of increased performance to come.

Our researchers have discovered it has now become more economical to build network security appliances based on standard PC server hardware using Napatech's intelligent real-time network analysis adapters to ensure high levels of performance. But, one of the most compelling reasons for considering this approach is the ability to scale performance.

At various key IT events throughout this year, Napatech has demonstrated a full-throughput 10Gbps IPS system based on eight instances of a standard SNORT application running in parallel.

This technique takes advantage of the multiple CPU cores available in modern PC servers. Napatech can support up to 32 CPU cores, so as the number of cores increases and the power of each core ramps up, the ability to scale performance increases.

Indeed, it's worth noting that CPU chipmakers such as Intel and AMD are increasing the performance of their chips by as much as 50% on an annual basis. Can the vendors of proprietary network security appliances keep up with this kind of performance roadmap? Does it even make sense to try? If you ask us here at Napatech, we will tell you that the time has come to reconsider. ■

*A recording of the online Napatech webinar referenced in this article can be found online at: **http://bit.ly/9CmM6M** (registration required)*

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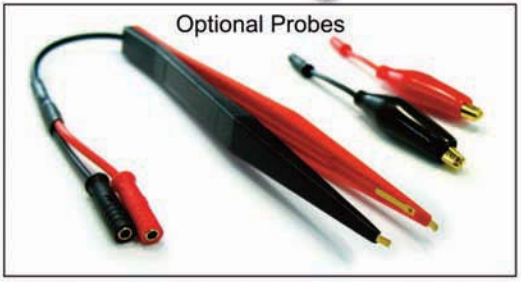



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# Going to the Fair

Myk Dormer

**INDUSTRY SHOWS**, from the small regional or niche market events to the biggest international spectaculars, have been a part of engineering life for decades – arguably since the great national exhibitions of the nineteenth century.

Most engineers have attended at least one such event as a visitor, wandering about for days from one interesting display to the next, but exhibiting at an industry show, organizing and manning a company stand is considerably more involved than just a "day at the fair".

The bare mechanics of running a booth are pretty obvious: hire the floor space and the furniture, arrange staff accommodation and travel arrangements, print promotional literature, turn up and watch the orders come rolling in. Easy?

In principle, yes, but in practice things are never quite so straightforward. While I cannot claim to be a world-class expert – some big companies employ staff who do nothing but organize events – I have attended and organised enough company booths to know what some of the pitfalls are:

1. **Investment.** It is vital to assign sufficient resources. A company presence at an event is a living advertisement. It provides a potential customer's first impressions, which can permanently colour their opinion of your organisation. So make sure it looks good.

   Plan ahead: be prepared to spend some money to get a big enough space, with the right furnishings. Make sure that documentation is professionally printed, that display models are well presented and that demonstrations are tried, tested and working beforehand. Assign sufficient staff to the event, so that rest-breaks can be had and the set-up and break-down tasks don't fall to one or two overworked people.
2. **Purpose.** Remember why you are there. Staff on a booth must be motivated, happy and focused, with a good spread of technical, commercial and interpersonal skills. It is definitely a place for 'volunteers only'. Understand that 'running the stand' is real full-time work and never attempt to combine a show with staff meetings or customer conferences. Such things can precede or follow an event, but they should never compete with it for time; your customers are at the event to see more than just you.

   There is no room to do other jobs, like answering emails or telephone queries, and no point assigning someone to an exhibition who really doesn't want to be there: it will show through their face and leave a bad image. A group of disinterested salesmen, standing with their backs to the customers, muttering about the cricket scores, or fiddling with a laptop, makes a bad impression that no amount of subsequent work will erase.
3. **Clutter.** No matter how many square meters have been rented, a stand is still a relatively small space. There is no place for any extraneous items: coats, personal luggage and packaging materials need to be stored elsewhere, litter must be rigorously collected and the displays and demonstrations must be kept in good order.

   There is never room for personal laptops and no-one should be eating their (greasy, crumb-making) meals on-stand. A half eaten kebab is never a good advert. There must be sufficient manpower that meal breaks and rest breaks can be properly allowed for without leaving an empty booth, while staff not 'on duty' need to find somewhere else to gather and chat.
4. **Focus!** Remember why the company is attending the event: to make contacts and to be seen. There needs to be plenty of promotional literature to hand out, ranging from lightweight flyers and cards to dense catalogues and datasheets; displays need to be clear, interesting and eye-catching; and the company name and website need to be written on everything – even free-gift pens.

   Staff on the stand need to be able to gather contact details easily (business card scanners are impressive, but an abundant supply of notepads can often do as well) and there needs to be a post-event debriefing/follow-up process planned in ahead of time. No potentially valuable customers can be allowed to "go missing".
5. **Clarity.** Everyone in a company will or should have a good idea of what the products or services it offers actually are and what they are for. The same cannot be said for a potential new customer, so the displays and demonstration models need to be informative, accessible and simple. It is possible to get "too clever" with advertising imagery and it is all too easy to vanish behind a smokescreen of industry-niche specific jargon.

   A company selling bolts probably needs some big pictures of bolts, not a stylized image of a wolf surrounded by lightning, or a display of flashing purple lights. Use simple language and avoid management or technical jargon. That can come later, when the customer is reading the datasheets.
6. **Fun.** The preceding comments make an industry show sound like a military boot-camp crossed with a submarine-cruise. It isn't. If properly organised it is a chance to make contact with customers and suppliers in a dynamic, positive environment. The 'feel' of a big show is unique and intoxicating, while the co-operation and hard work necessary to make a show "work" is better than any trendy "team building exercise".

   Furthermore, many of the events are in fascinating parts of the world, which you might otherwise never think to visit. An industry show is a valuable experience and, like many things in life, will yield rewards proportionate to the effort you put in.

Enjoy it! ■

*Myk Dormer is Senior RF Design Engineer at Radiometrix Ltd* **www.radiometrix.com**

# Driving LED Lighting Adoption

Author: Alistair Winning, Farnell

LED-based lamps consume around a quarter of the power of a conventional incandescent bulb for comparable light output, and are gaining acceptance from homeowners and businesses seeking to cut their energy bills as well as their carbon footprint. LEDs can also last up to 50,000 hours or beyond, depending on operating temperature, thereby delivering longer-term advantages such as lower replacement costs and reduced waste.

Multi-LED replacement bulbs in standard form factors such as MR16 provide immediate and cost-effective access to the new technology. In addition the small dimensions and relatively low operating voltages of power LEDs, which are available in several shades of white light as well as standard colours and colour-mix versions, allow lighting designers to create new styles and develop ever-more versatile and controllable applications.

## BACKWARDS COMPATIBILITY

The lighting industry knows that LED lamps must be easily implemented as direct replacements for conventional types to ensure rapid uptake, particularly by consumer markets. As end users and installers demand replacements that will interoperate with existing installed equipment; in particular, with triac-based phase-cut dimmers. These are already installed in many houses and commercial premises, for use with incandescent lamps, to save energy and improve end-user comfort.

The triac-based dimmer is designed for operation with a resistive load such as incandescent or halogen bulbs. Dimming is achieved by delaying the firing angle of the triac using an RC circuit, hence reducing the average power delivered to the load. An LC filter is used to reduce conducted EMI resulting from the sharp voltage rise at triac turn-on. The lamp's resistive load provides damping for this filter and also helps maintain a holding current to ensure the triac remains conductive, even at light loads.

The phase-cut waveform is not a suitable dimming signal for a conventional LED driver. Effects such as the sudden voltage rise and the reduced average voltage over the complete cycle can result in flickering of the LED lamp. The effective dimming range is also restricted.

A number of LED drivers capable of operating with conventional wall dimmers have emerged to overcome this challenge. Among these, the National Semiconductor LM3445 has internal angle-detect and dim-decoder circuits, which help translate the incoming phase-cut waveform into a constant-current signal to drive the LEDs at the desired brightness. The device also implements a bleeder circuit, which operates in conjunction with an external resistor, to ensure proper triac operation by emulating the ability of an incandescent load to maintain the triac holding current. A passive PFC circuit maintains a high power factor and minimises harmonic distortion by drawing current directly from the line for most of the cycle. This allows drivers built with the LM3445 to meet IEC 61000-3-2.

Other triac-dimmable devices such as the NXP SSL210x are also available, which integrate comparable functions to ensure correct operation of the triac while also improving power factor, distortion performance and efficiency.

## THERMAL MANAGEMENT

The light output from a power LED is known to decrease with increasing temperature and, since the power LED is a semiconductor device, its reliability is directly related to operating temperature. The component can also be destroyed by excessive internally generated temperatures. In practice, the lower the temperature, the more reliable and long-lasting the LED will be.

Over its lifetime, the light produced by a power LED shows a gradually diminishing trend. The device's end of life can be defined as the point at which the light output falls below a usable level, according to the application. This reduction in light output is termed lumen maintenance, and is described in manufacturer datasheets or application notes as a curve plotting light output against time. A number of curves may be presented, showing lumen maintenance at several operating temperatures. Using these curves, the designer can target a specified lifetime by determining the drive level for the required light output and then ensuring the operating temperature does not exceed that of the target lumen maintenance curve. This requires careful attention to thermal management.

Power LED packages are designed to minimise thermal resistance between the die and the edge of the package. In many cases the LED die is mounted on a large metallic heat spreader that is exposed on the outside of the package to allow soldering to the PCB.

PCB materials featuring an Insulated Metal Substrate (IMS) have high thermal capacity, and are effective in removing heat from the LED via the soldered-down heat spreader. In some applications this may be sufficient to maintain the LED temperature within acceptable limits. On the other hand, additional heatsinking may be necessary.

In general, the larger the heatsink, the lower the operating temperature will be. Heatsinks from manufacturers such as Lamina, Tyco and Wakefield are designed to provide the maximum possible surface area for cooling, within small form factors suitable for use in applications such as bulb replacement or original LED-based lamp designs.

element14 Farnell

# New Methodologies and Innovations Fuel System Realization

**Steve Brown** and **Raj Mathur** from Cadence explain the need for a new system design approach that allows both earlier software development and faster silicon development, along with earlier and more frequent system integration steps

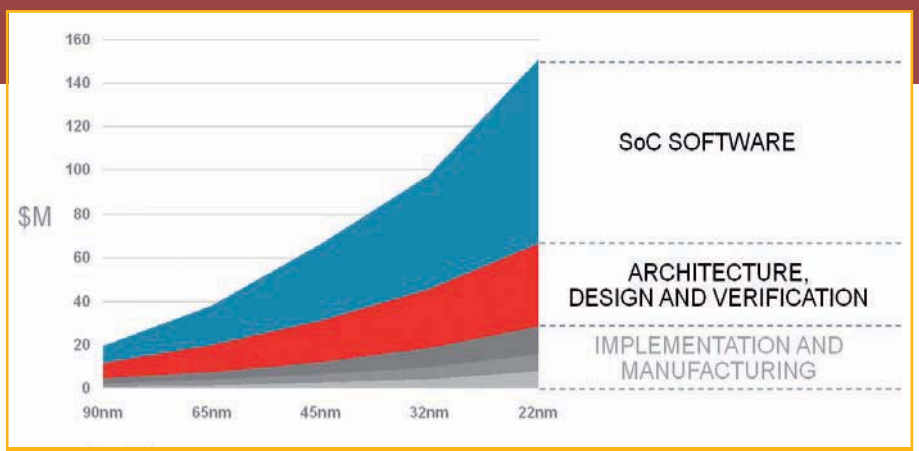


***Figure 1:*** *SoC development costs have soared from $20m at 90nm to nearly $100m at 32nm. Software is the fastest growing part of the cost [source: IBS Inc.]*

**FUELLED BY MASSIVE** functional capacity, high performance and low-power silicon processes, and exploding software application content, the pace and scope of electronics innovation is accelerating. The challenges of bringing together increasingly complex systems are also growing, confronting traditional approaches with out-of-control verification costs and missed market windows. What's needed is a new system design approach that allows both earlier software development and faster silicon development, along with earlier and more frequent system integration steps.

This new methodology must enable a unified hardware/software development and verification environment, and allow the specification, analysis and verification of constraints such as timing and power in the context of the software and the system. This article highlights recent advances in system design, transaction-level verification and software development that support this kind of unified environment. The article discusses the role of standards and explains the productivity gains behind a transaction level modelling (TLM)-to-GDSII design and verification flow.

Specifically, this article looks at the challenges and emerging methodologies behind System Realization, which is defined in the EDA360 vision paper as the development of a complete hardware/software platform that provides all necessary support for end-user applications. System Realization recognizes that the value and differentiation of new devices lies increasingly in the application software. The article concludes by noting some practical innovations, available now, that will help design teams build an effective System Realization flow.

## System Realization Productivity Challenges

The economy is motivating consumers to be more selective in their electronic product choices. Manufacturers must satisfy demands to increase application capabilities, provide longer battery operating lifetimes and hit a narrow consumer shopping season. Electronic system developers are coping with the consequences of exponential growth in software and are facing a need to accelerate all aspects of system development.

### *Shortening Project Schedules*

Short project schedules do not represent a new challenge, but the problem is becoming worse with rising complexity. With more and more software content in chips – whether embedded or application – RTL design and verification are no longer the main cost bottlenecks as a system-on-chip (SoC) goes to tapeout. System development, embedded software development and verification are rapidly becoming the key cost components of the electronic design process. As the cost rises, the need to shorten project schedules with methodologies that leverage trusted RTL simulation tools becomes paramount.

### *Increasing Task Complexities*

With software increasingly driving hardware content, verification teams are searching for ways to revise, or preferably augment, their current verification strategies. This is because current verification strategies are running out of steam. Current verification strategies lack a consistent verification methodology from ESL to GDS-II, lack interoperability of the different tools used in the entire flow, lack re-usability of the same or similar testbench to drive verification at different abstraction levels through the entire flow, and lack a common dashboard to monitor and capture key metrics from all verification tools used in the entire flow.

### *Growing Importance of Design for Power*

Power consumption has direct impact on product usage, heat, form-factor and economics. Battery life is a key differentiator for almost all mobile devices and can be as important as some of the functionality. Power consumption correlates with generated heat and can make a device expensive to cool, or too hot to operate. Lower power consumption can also enable miniaturization of devices such as hearing aids or other space-sensitive considerations. And power consumption costs money in wired or battery energy expenses.

The challenge is that power consumption has been an outcome of the design process, one that can't be measured until late in the project. What is

needed is a way to assess the power consumed by the device under different operating conditions, running different software application stacks, before building silicon. Even more valuable is the capability to use power estimates to make architectural choices early in the project, before a significant effort is expended.

## System Realization Methodology Trends

In order to meet the expectations and requirements of today's rapidly evolving electronics markets, devices must be designed from the perspective of the user applications, with all components designed to meet the required function, form-factor and performance characteristics. This is a dramatic change from the past where semiconductor innovations drove device design. The change in orientation of the design relationship is demanding changes from the design tools and methodologies used in the past. An emphasis is now being placed on the decomposition of the system at each level into sub-components, refining requirements for each sub-component, rapid creation and verification of each sub-component, re-integration of the sub-components and, finally, verification of the integrated capabilities. Several necessary innovations have emerged to enable the next wave of design methodologies and tools that automate these processes.

### *Earlier Software Development and Integration Testing*

Formerly it was possible to develop software by using early silicon device samples from the manufacturer. Early pressures on system development have led to a widespread use of pre-silicon emulation to perform the integration validation and support early software development. The significant growth in applying FPGA prototype boards for software development is another form of hardware-assisted verification using the design before samples from an ASIC process are available. Still, this stage is primarily only possible after RTL design is completed. In today's rapidly evolving electronics marketplace this doesn't advance software development early enough in the project schedule.

Some system developers today are using virtual prototypes of the system to enable even earlier software development. The idea is to model the device or board with a collection of executable models that are created much earlier than the silicon, and provide enough accuracy and performance to develop software and perform some verification. Different approaches are being applied using service-based modelling approaches, proprietary modelling languages and technologies, and standard SystemC.

Virtual prototype models are mostly used only for software development, and the creation of RTL remains a separate, duplicate modelling effort. High-level synthesis of C/C++/SystemC is emerging as a way to unify virtual prototype models with the silicon design flow. Most would agree it remains difficult to create such models early enough, economically enough and with enough performance and accuracy to feed into the RTL-based design flow.

### *Expanding Virtual System Model Opportunities*

Even project teams that are successfully using virtual prototypes are

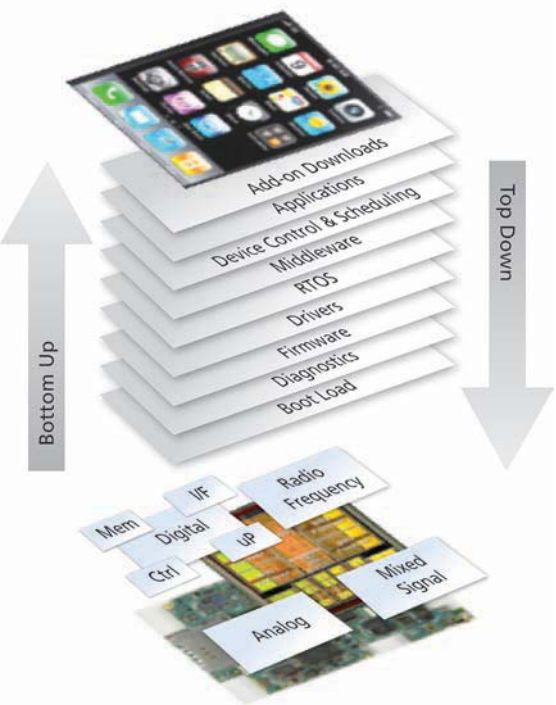


***Figure 2:*** *Increasing system complexity is creating exponential growth in design and verification complexity*

spending a great deal of effort to do so. In addition, they are often also utilizing an emulation approach, as well as building FPGA-based prototypes. Each of these systems provides different benefits in software development (see **Figure 3**).

In order to fully develop software and hardware in parallel, each of the solutions needs to enable early software development, find bugs earlier in the project and ensure high quality system validation.

### *Mixing of Multiple Abstractions for Verification*

Very few design teams can afford to start their designs from scratch. Derivative designs increasingly consist of components at multiple levels of abstraction. While some components may be new and can be defined initially at the ESL abstraction in a high-level language for fast model efficiency, other components may be available only in RTL form, while others may be available as gate-level descriptions with some pre-existing qualifications. These are all models of the system at different abstraction levels with varying degrees of model accuracy and pre-qualification.

A single verification environment that can accept the different model representations is required for application-driven system level verification. Driving the multi-abstraction 'design-under-test' with automated testbenches and that can be applied within a multi-abstraction verification environment will accelerate system level verification. If a single verification environment isn't readily available, then the next best option is a hybrid of verification engines coupled together cohesively with tool interoperability. The tools can include TLM simulation, RTL simulation and hardware-assisted verification.

### *Standardization of Design and Verification for Increased Reusability*

Increasing design reuse presents both opportunities and demands to define standards. RTL design code has been notoriously difficult to integrate into new SoCs. Reusability involves far more than a common structured

| | Execution Speed | Timing Accuracy | Bring-up/Debug |
|---|---|---|---|
| Virtual Prototype | ● | ● | ● |
| FPGA-based Prototype | ● | ● | ● |
| Emulation-based Prototype | ● | ● | ● |

***Figure 3:*** *Virtualization capabilities by technology*

approach to microarchitecture. As virtual platform methodology becomes more common, the ability to reuse models from different sources becomes an imperative, placing demands on modelling techniques, abstractions and coding styles. Enabling high-level synthesis flows also places standards requirements on the design methodology.

Design modelling standards such as SystemC, TLM1, TLM2 and the SystemC synthesizable subset are being driven by the Open SystemC Initiative (OSCI). Using multiple verification engines with testbench automation requires the Unified Verification Methodology (UVM) and Standard Co-Emulation Modelling Interface (SCE-MI) standards.

### *Expanding Use of Transaction-Based Methodologies*

One of the most important standardization trends is the use of transaction level modelling as the basic architectural concept for design and verification methodologies. Transaction level modelling is the core methodology that enables interoperability between virtual prototyping, high level synthesis, transaction-based acceleration and the integration into existing RTL design and verification approaches. This transition in methodology is needed to enable the modern technologies required for system design and verification.

The transaction modelling concept is required by virtual prototyping to enable quick model creation and fast simulation speeds needed for software development. Recent high-level synthesis tools and methodology enable direct use of those models for rapid creation of RTL designs. And transaction-level modelling is the underlying principle in the Unified Verification Methodology (UVM), enabling a single verification environment to be applied to TLM design simulation, RTL simulation and RTL acceleration.

Transaction-based acceleration is a technology that accelerates simulation using specialized hardware to speed the computation of instructions compiled by a simulator. Traditionally, the hardware has been driven with Verilog, VHDL, SystemVerilog or e based testbenches, but there is an increasing demand for the hardware to be directly driven from SystemC or C/C++ based testbenches, enabling software and firmware developers to accelerate their code verification. The utilization of hardware-assisted verification is further expanded as the industry embraces high-performance Universal Verification Methodology (UVM) and Metric Driven Verification (MDV) built on transaction based acceleration technology.

### *Moving to TLM Abstraction for Design and Verification*

The industry is moving to a higher TLM abstraction to increase productivity for creating new hardware IP. The reduction in lines of code speeds IP creation time, reduces the number of bugs that are inserted and speeds verification performance and turnaround time. Cadence Incisive Enterprise Simulator SystemC functional verification throughput can be as high as 10 times over RTL, enabling more exhaustive UVM-based verification of the device functionality before committing to RTL.

Designer productivity is increased by the faster creation of SystemC designs, as well as automated high-level synthesis with Cadence C-to-Silicon Compiler to produce the RTL. Describing IP at a higher level of abstraction also increases IP reusability and implementation in different process nodes. Design teams can leverage the synthesis tool to create optimal microarchitectures for different system specifications, rather than coding RTL by hand each time.

A comprehensive methodology guide is available from Cadence to lead engineers and teams through key decisions for modelling, UVM functional verification environment creation, IP reusability and synthesizability. The guide comes with examples that help with learning as well as a book, "*TLM-driven Design and Verification Methodology*".

The unique integration of C-to-Silicon Compiler with Cadence Encounter RTL Compiler enables automated closure on a microarchitecture that meets Quality of Results (area, timing, power) constraints. C-to-Silicon Compiler is built with a database that enables efficient ECO implementation and is integrated with the RTL Compiler ECO flow. This enables minimal netlist changes to be introduced even when functionality at the SystemC input is changed. This same database enables Incisive Enterprise RTL simulations to support SystemC source level debugging that is tightly synchronized with the RTL debugging and simulation.

### *Utilizing a Continuum of System Platforms*

Earlier software development is a key industry requirement for parallel hardware/software development. Using IEEE 1666 SystemC to model the design and executing with a fast Instruction Set Simulator of the processor, the Incisive Enterprise Simulator's fast SystemC execution enables early software creation, integration with hardware, and functional verification. The Incisive Enterprise Simulator provides a native simulation engine that delivers high speed execution of the TLM-2.0 virtual prototype standard, a fully integrated development environment and non-intrusive interactive debugging and analysis of the virtual prototype. It uniquely provides support for legacy RTL in virtual platforms, utilizing a single kernel simulation architecture and unified debugging environment.

For hardware-assisted verification, the Cadence Incisive Palladium XP Verification Computing Platform fuses three best-in-class verification engines into a single platform – namely, simulation, acceleration and emulation. Extended on top of these verification engines are unique methodologies such as Metric Driven Verification and low power design analysis and verification. With these capabilities, software and firmware integration testing are achieved with increased accuracy of real-world stimulus when running verification in either in-circuit emulation (ICE) mode or in a hybrid mode of ICE and transaction based acceleration (TBA). TBA is an optimized simulation acceleration mode that accelerates logic simulation by several orders of magnitude and uses message-level communication between the testbench components running on a workstation and the rest of the environment running on the Palladium XP platform.

Palladium XP further improves system level verification productivity by offering the fastest bring-up time, an easy-to-use flow, flexible simulation-like use models, scaleable performance and fast and predictable compilation for the best turnaround time. Supporting the Universal Verification Methodology (UVM), Palladium XP supports substantial re-use across multiple levels of abstraction with an advanced, automated verification environment with constrained-random stimulus, functional coverage and scoreboard checking.

### *Optimizing System Debug*

System-level debugging is challenging due to the scope of the problem, different domains of functionality, different logic representations (hardware, software), third party IP familiarity, the need for both

verification speed and debug visibility, and the confluence of engineers from multiple disciplines. The unique Cadence solution to this problem is an integrated debug and verification engine environment that provides the speed when needed, the debug visibility when needed and a unified debugging environment, presenting information and debug control in ways uniquely different for hardware and software engineers.

Hotswap is a key technology that allows simulation runs to 'swap' the underlying verification engine. With a stroke of a button, a simulation run can swap from a simulator to an accelerator or vice-versa. Typically, users initiate their run in the simulator in order to propagate through the Xs and Zs of a 4-state simulation engine, and then hotswap over to an accelerator running their verification cycles orders of magnitude faster in a 2-state hardware accelerator. In both verification engines, the simulation use models are maintained for easy adoption of hardware acceleration.

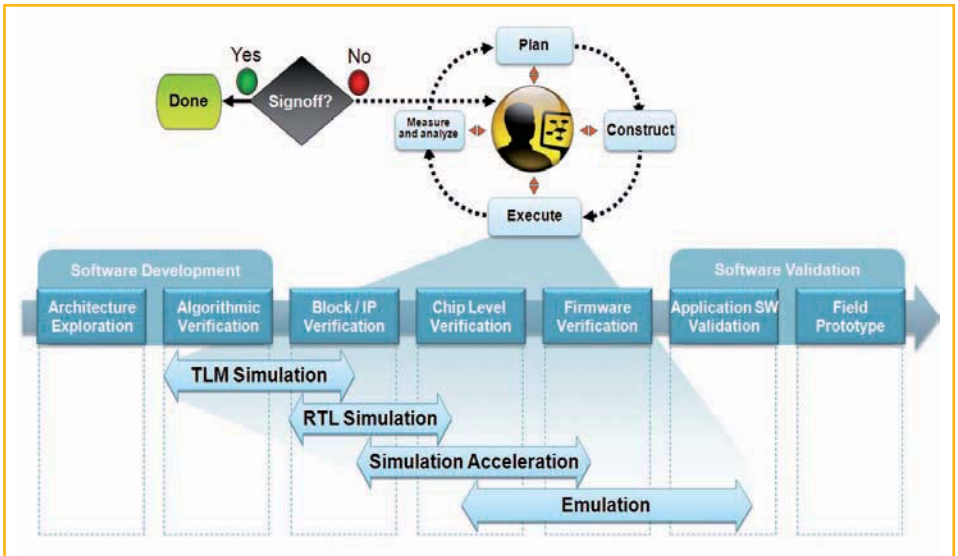


***Figure 4:*** *Planning and managing the system verification process*

### *Planning and Management of Complete Verification Flow*

Verification coverage metrics have traditionally been written for and collected from different verification engines, resulting in costly time-consuming manual integration and assessment of the impact on system level verification. With advanced metric-driven verification, metrics produced from multiple verification engines can be collected selectively from each engine or simultaneously in a hybrid verification environment – from TLM simulation, RTL simulation, acceleration and/or emulation.

A verification plan organizes the coverage metrics into system and schedule views. The metrics are collected into a database from each verification engine and presented in an integrated dashboard for easy viewing. Pass/failure analysis can be performed holistically at the system level as the metrics are back-annotated into the system level verification plan. The unification and integration of the different verification engines for metric driven verification takes the planning and management of the complete verification flow to the next level of end-user productivity.

### *Unified System to Silicon Power Planning and Verification Flow*

IP creation using a high-level language such as SystemC enables architects to explore different microarchitecture implementations and optimize across the area/timing/power spectrum more flexibly than with RTL. Once RTL is created, the microarchitecture is fixed and system optimization possibilities are limited. In contrast, microarchitectural tradeoffs can be rapidly explored using C-to-Silicon Compiler to explore scheduling and make resource sharing tradeoffs.

The use of multiple power domains is an increasingly common technique for optimizing system power. But this magnifies the functional complexity of the device, adding to an already complex functional verification problem. The complexity can be handled effectively by creating a power functional verification plan with the planning capability of Cadence Incisive Enterprise Manager that documents all the various power domains and the needed on/off transitions that must be verified. The verification plan is a high level, metric-based mechanism to organize and thoroughly specify the functional verification requirements for the project, from the system-level to the firmware and including the SoC level. This plan is used by Incisive Enterprise Manager to measure that tests have been executed to verify all the power shutoff/turn-on transitions of the system, along with the complete system functional verification.

### *RTL Based SW-driven Dynamic Power Analysis*

To verify that software driven system-level designs are optimized for low power, engineers require an automated process for identifying bugs and ensuring that all power-related logic is exercised. Cadence low-power verification and analysis technology integrates logic design, verification and implementation technologies with the Common Power Format (CPF), which represents power constraints and intent.

Cadence Incisive Palladium Dynamic Power Analysis (DPA) brings a system-level perspective to power budgeting for electronic devices. Using the high-performance Palladium XP engine, DPA lets users run long system-level tests, empowering SoC teams to assess the power consumption of a performance-sensitive function against requirements for an acceptable end-user experience. DPA helps engineers quickly identify peak and average power of SoCs with "deep" software cycles with real-world stimuli. Furthermore, with a successive-refinement approach, system designers can now make better decisions when selecting IP, an "adequate" package and cooling requirements, and they can react quickly to changes in the specification or environment. By testing against various operational scenarios and "what-if" analysis to make architecture tradeoffs, designers can make better decisions to save power.

Although power shutoff (PSO) techniques can drastically reduce SoC power consumption, power verification complexity increases. For large designs with multiple power domains, power verification may not be adequate with simulation alone due to performance limitations at the system-level. With Palladium XP's high-performance engine with deep trace capability, power sequences can be verified at the system level with complex trigger conditions for power on/off.

### High-Level of Abstraction

EDA360 System Realization requires a reversal of the historical design process. Instead of a bottom-up, silicon-first methodology, it calls for an application-driven top-down approach. Not only must the requirements be driven top-down, but the methodologies to design and verify sub-systems and silicon must each be more efficient, faster and more easily flow with the rest of the system development process. This is only possible through higher levels of abstraction, standardization, increased automation and special purpose verification computing platforms. ■

# A Recipe for Better System Block Design – Add SPICE

**Reza Moghimi**, Applications Engineering Manager from Analogue Devices, and **Natasha Baker**, Product Marketing Engineer for Multisim at National Instruments, explain that new tools provide a holistic approach to circuit design and validation

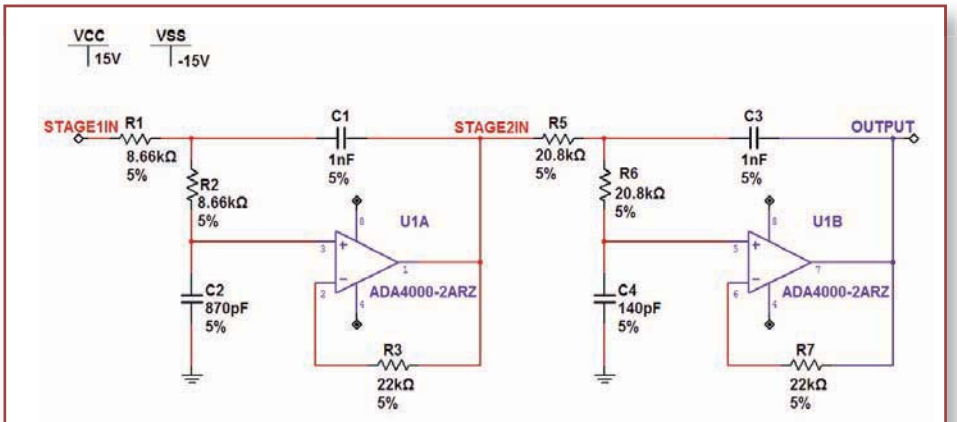


***Figure 1:*** *A 20kHz Butterworth filter in NI Multisim*

**IS THERE ANYTHING** more frustrating than having the board shop kick back an error-ridden design? Many designers today are under pressure to produce a prototype in weeks (if not days), and there's a limited margin for design iterations. Fortunately, the latest design tools improve productivity by providing a holistic and intuitive approach to circuit design and validation.

During the initial specification stage many semiconductor manufacturers provide tools to aid in the design of robust system blocks. Analogue Devices (ADI), for example, has an online filter design tool that guides users through the process of active filter synthesis and the selection of recommended op-amps based on those specifications. The tool then generates the final design topology, along with a bill of materials and SPICEnetlist. In the stages before prototyping, simulation environments such as those from National Instruments (NI) provide further optimization and validation using macromodels of the specified parts.

In this article, we will explore how this holistic approach can speed up and improve the often daunting task of filter design – a common building block in a range of electronics applications.

## Sim Basics

The most popular analogue circuit simulation tool is SPICE (Simulation Program with Integrated Circuit Emphasis). The life of SPICE dates back to the late 1960s when it was developed at the University of California, Berkeley. SPICE evolved into the industry standard for analogue circuit simulation and remains the world's most widely used circuit simulator. Over the years, more simulation algorithms, component models and extensions have been added. XSPICE, for example, developed at Georgia Tech, allows the behavioural modeling of components to accelerate the speed of mixed-mode and digital simulation. The NI Multisim environment supports both SPICE 3F5 and XSPICE simulation.

But why should designers bother with simulation? Simulation has become entrenched as an essential stage in the design process because it lets engineers

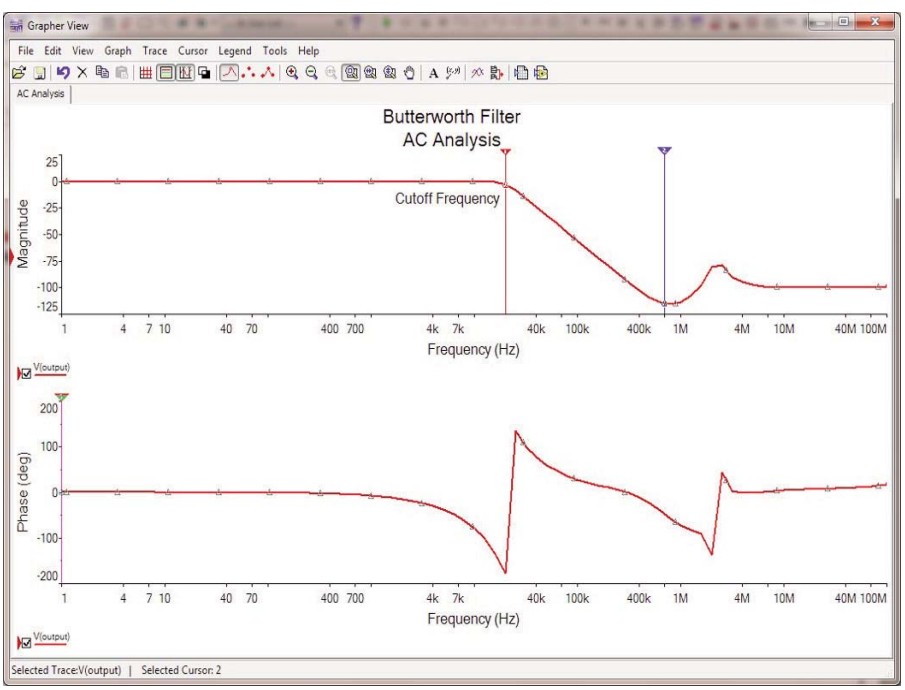


***Figure 2:*** *Frequency response of the Butterworth filter*

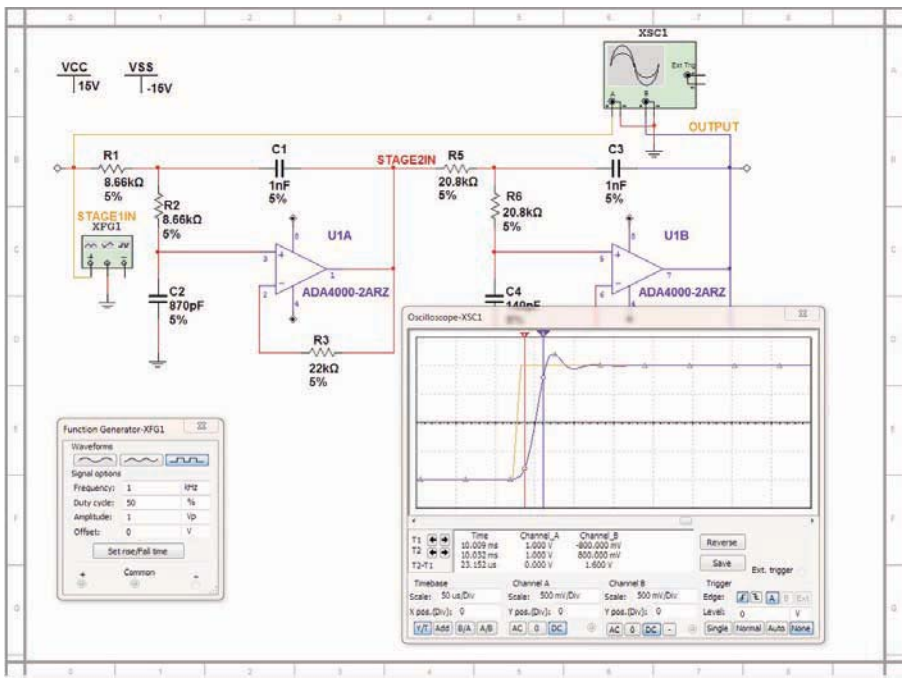


***Figure 3:*** *Investigating the time-domain response using virtual instruments*

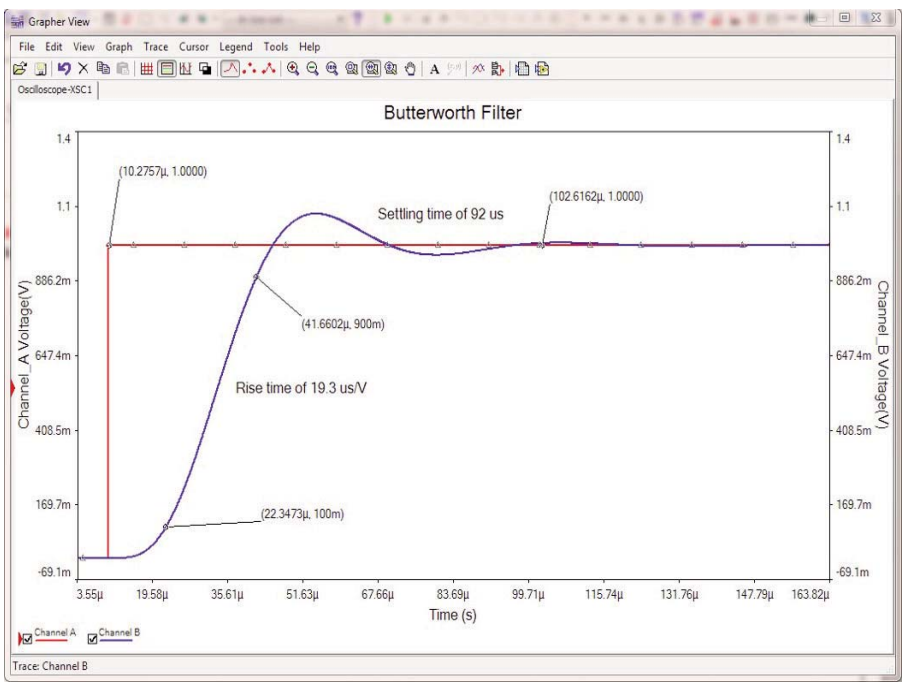


***Figure 4:*** *Documenting time-domain characteristics using the Grapher*

evaluate and validate circuit behaviour before prototyping. Simulation prevents design flaws from cascading through the design chain to fabricated boards where redesign becomes exponentially more expensive. Furthermore, through the exploration of a range of "what-if" scenarios, designers can improve the performance of their circuits in a virtual environment, risk-free.

One of the main benefits of using a circuit simulator is the ability to simulate macromodels that emulate real, orderable parts. Modern SPICE simulators are also taking an increasingly graphical approach to what has traditionally been a text-based process. For instance, NI Multisim incorporates more than 17,500 components, with many macromodels from leading semiconductor manufacturers; a text-based SPICE netlist is automatically generated upon capturing a circuit, and interactive measurement instruments, such as the oscilloscope or function generator, have displays and functionality that mimic their real bench-top counterparts. With these graphical extensions, designers no longer need to have expertise in SPICE syntax to leverage the benefits of simulation.

## Simulation and Filter Design

Filters are everywhere – from ultrasound equipment to pacemakers, where it is vital that only a specific range of frequencies be passed. Yet, while filters are a ubiquitous building block of electronics applications, filter design is little understood and often painful. What makes it so complex? Often the required filter order for a specific performance is not well understood by system designers whose strength is not analogue circuit design. There are many variations in filter types (Butterworth, Chebyshev, Elliptic, etc.) that are optimized for various specifications such as monotonic ripple or transition region width. Filter design also involves writing complicated math equations for identifying

pole/zero locations that change the filter shape. Another wrinkle is that the perfect components assumed during theoretical calculations do not exist; for example, manufacturing tolerances of resistors can affect expected circuit behaviour.

Design tools such as filter wizards greatly simplify this complex task, by helping designers understand the differences between the different topologies, as well as suggest parts for use in the design, without requiring complicated math. Graphical environments let designers observe how their circuit will operate across a wide range of component tolerances.

## Validating the Design of a Butterworth Filter

In our example, we will be validating the design of an active filter. The filter was designed using the ADI Filter Wizard and incorporates the ADA4000-2 dual precision op-amp, which has been selected for it fast slew rate and stability with capacitive loads, making it a perfect fit for filter design.

This op-amp's pico-amp bias current allows the usage of high value resistors to construct low frequency filters without needing to worry about adding to dc errors. Additionally, the high value used for R1 minimizes interaction with signal source resistance. Higher-order filters are possible by cascading more blocks, however sensitivities to component values and the effects of interactions among the components on the frequency response increase dramatically, making these choices less attractive. The signal phase is maintained through the filter (non-inverting configuration).

The filter was captured in NI Multisim for validation and further analysis, as shown in **Figure 1**. This low pass, 4th order, Butterworth filter was designed with a 20kHz cutoff frequency and the Sallen-Key implementation due to its ease of design, maximally flat frequency response and minimal component requirements.

Butterworth filters are monotonic in pass-band and stop-band; have optimal pass-band ripple and a wide transition region (i.e. region between the pass band and stop band). They are frequently used as anti-aliasing filters in data acquisition systems. A two pole version of this Sallen-Key filter topology is utilized on the EVAL-FLTR-SO-1RZ and EVAL-FLTR-LD-1RZ filter boards which can be ordered from ADI. The application note for this board is AN-0991.

When designing a filter, it is important to consider both the frequency and time-domain responses of the circuit. Let's investigate how we can validate these characteristics using NI Multisim:

**1. Validating Frequency Response:** **Figure 2** illustrates the results of an AC Analysis. The simulation results indicate a cutoff frequency (the frequency at which the gain drops by 3dB) of 20.1kHz, which closely approximates the 20kHz specification we set out for. We can see that beyond this corner frequency, the gain falls off at 80dB per decade (-20dB/dec or -6dBoct for each pole in the filter's transfer function). We also observe that the stop-band does not continuously decrease as we would expect from an ideal filter; the gain begins to increase at approximately 1MHz due to the loss in op-amp voltage gain. Using the cursors, we estimate this stop band to be approximately 700kHz.

**2. Validating Time-Domain Response:** We can investigate the step response using measurement instruments available in Multisim. The function generator will allow us to input a stimulus and the oscilloscope will allow us to observe our output waveform, both directly within the schematic environment. These measurement instruments mimic their bench-top counterparts. With the oscilloscope, for example, parameters such as the timebase and voltage divisions can be adjusted based on waveform characteristics. With measurement instruments, we can also change settings in real-time, such as the frequency set by the function generator, which would allow us to see how much our signal is being attenuated for a frequency beyond the 20kHz point.

We can measure characteristics such as rise time and settling time with the oscilloscope as shown in **Figure 3**, however, we can also view this data within the Grapher, an option that allows us to annotate and print the graphs for documentation purposes. The first characteristic we investigate is rise time (defined as the time from 10% to 90% of its final output value); using the cursors, we determine this to be 19.3us. We also see a settling time of approximately 92us. These characteristics have been annotated on the graph shown in **Figure 4**. (Note: Parameter TMAX will affect risetime, and was changed from the default for the purpose of this example).

**3. Taking Worst Case Scenarios into Account:** Another core benefit of simulation is the ability to account for non-ideal component values (i.e. tolerances). A Monte Carlo analysis, which can run multiple AC analyses using permutations of component values within the 5% component tolerance range, will allow us to see how a cutoff frequency is affected in the worst cases.

Some measurements require more post-processing than others. Tasks such as calculating rise time for example can become tedious if done repetitively. Fortunately, there are tools that solve that problem as well. NI LabVIEW is a graphical programming language that allows us to create a custom interface for visualizing and analyzing measurements within Multisim. This instruments automates the calculation of rise time, slope, overshoot and undershoot of a filter design based on its input and output waveforms. By creating a custom instrument, designers can automatically display accurate values of characteristics that would traditionally require manual post-processing. Custom instruments can be made for a broad range of applications, including the import of real acquired measurements into NI Multisim that incorporate real-world effects, such as noise, for even greater simulation accuracy.

In conclusion, today's system designers cannot afford to run with unverified ideas. With modern design tools, such as the ADI Filter Wizard and NI Multisim, they don't have to. Engineers can validate and improve circuit behaviour long before the prototyping stage, vastly improving design productivity. The end result consists of fewer costly redesigns, faster time-to-market and better design performance. ■

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# Advancing the Art of System Design

**Arun Mulpur**, Industry Marketing Manager for Communications, Electronics and Semiconductors at MathWorks, discusses the significant recent advances in modelling, simulation and code generation tools and methods

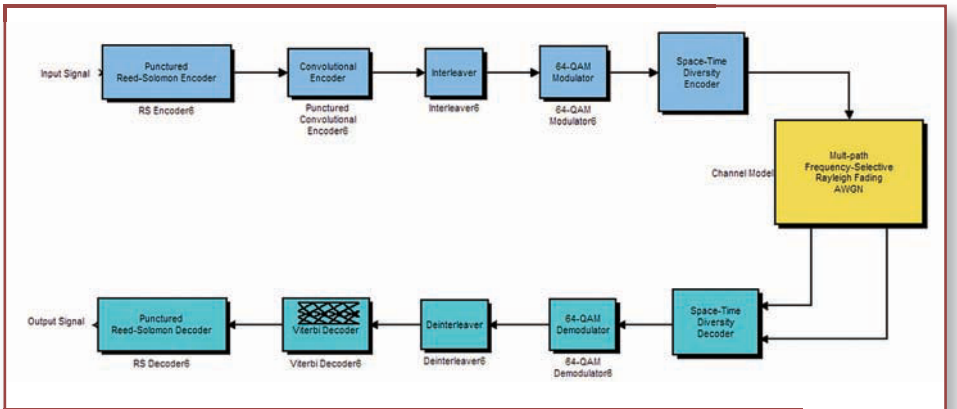



***Figure 1:*** *Block diagram representation of a typical communication system*

**DESIGN-FLOW** discontinuities are becoming increasingly disruptive and expensive in the development of complex signal processing and communications technologies. Shorter design cycles magnify the impact of these discontinuities. This article describes a few use cases – in algorithm design, system architecture and hardware design – that illustrate significant recent advances in modelling, simulation and code generation tools and methods.

For algorithm design, several hundred ready-to-use signal processing and communications System objects are now available in MATLAB and enable faster development of complex algorithms. System architects can now model RF and baseband system components in a unified environment and perform true multifrequency simulations. In hardware design, several new developments, including workflow advisor, critical path highlighting, distributed pipelining, back annotation and resource utilization reports, provide a framework for faster design iterations.

```
%% Load simulation parameters from a MAT file
clear
load mysystemobject.mat
%% Instantiate system objects to model the sequence of operations
% Transmitter
 hRSEncoder    =comm.RSEncoder(120,108);
 hConvEncoder=comm.ConvolutionalEncoder(poly2trellis(7, [171 133]),...
 'TerminationMethod','Truncated',...
 'PuncturePatternSource','Property',...
 'PuncturePattern', reshape([1 0 1 0 1;1 1 0 1 0], 10, 1) );
hInterleaver=   comm.BlockInterleaver('PermutationVector',...
  interleave_pattern);
hModulator = comm.RectangularQAMModulator(64,...
'BitInput',true,...
'SymbolMapping','Custom',...
'CustomSymbolMapping',constellation_pattern,...
'NormalizationMethod','Average power');
hMIMOEncoder = comm.OSTBCEncoder;
%% Channel model
hAWGN=comm.AWGNChannel('NoiseMethod','Signal to noise ratio (Eb/No)',...
'EbNo',10);
```

***Figure 2:*** *Communication system modelled in MATLAB using Communications and Signal Processing System objects*

## Algorithm Design for Streaming Systems

Many engineers begin the development of signal processing and communications algorithms in MATLAB using floating-point arithmetic. These algorithm developers can take advantage of the powerful signal acquisition and analysis capabilities of MATLAB, as well as built-in algorithm libraries of several toolboxes. In some organizations, however, these algorithms are then rewritten in C code to refine them for implementation, conversion to fixed-point or integer arithmetic, or to integrate them with other design elements. This rewriting step is one example of a potentially costly and disruptive discontinuity in the design flow.

System objects – an important new addition to MATLAB – enable engineers to design signal processing system models for streaming applications directly in MATLAB and utilize several hundred new library components for signal processing, image and video processing, and communications.

As an example, **Figure 1** shows a block diagram representation of a basic communication system with transmitter, channel and receiver components. To model and simulate such a system, some engineers write many thousand lines of C code and then look for ways to integrate the design with test equipment or analyze simulation results.

In contrast, to the several thousand lines of C code that are typically written, the MATLAB

code shown in **Figure 2** uses several available System objects from Signal Processing Blockset and Communications Blockset. For example, to model the transmitter, an engineer can instantiate and call the Reed-Solomon Encoder, Convolutional Encoder, Block Interleaver, Rectangular QAM Modulator and Orthogonal Space-Time Block Coder System objects from Communications Blockset in sequence, as shown in Figure 2. Additionally, unlike traditional functional programming styles, System objects in MATLAB are object-oriented implementations of algorithms; they implicitly handle indexing, buffering and state management, which makes the code much simpler to write, debug and maintain. The code structure enables engineers to easily compare it with the original specification or block diagram. Algorithm designers can rapidly combine this code with their existing MATLAB code and test the algorithms with live data acquired from measurement instruments.

Algorithms coded using System objects facilitate code reuse in the system design process. Floating or fixed-point MATLAB code can be included directly in a Simulink model as part of the system architecture, modelling and design process. Engineers can also generate C code automatically from MATLAB code that uses System objects, and then use that C code for simulation or integration with other C/C++ design elements, after proper verification.

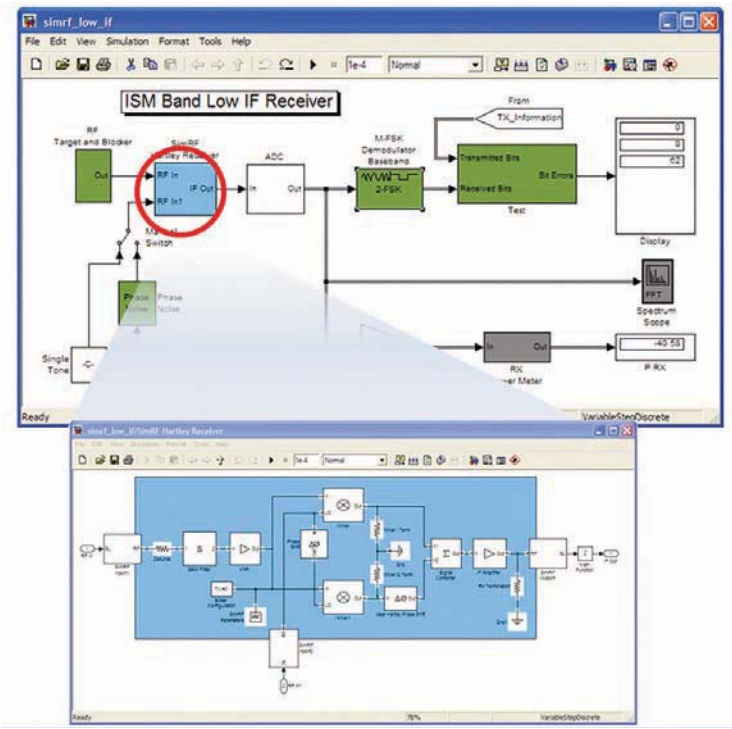
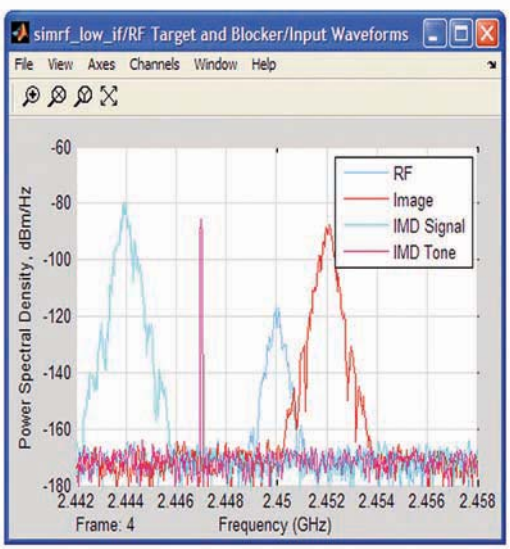



***Figure 3:*** *ISM band low IF receiver with digital and RF subsystems in one unified model (above) and detail of the Hartley receiver RF subsystem modelled in SimRF (below)*

## RF and Digital System Architecture

Static link budget calculations are a common first step in RF designs based on specifications for LTE, Bluetooth, ZigBee, Wi-Fi, or other technologies. These calculations provide a good starting point, but they do not account for input signal modulation, image effects and other real-world phenomena. To effectively model and simulate the effects of RF impairments on communication systems, system architects currently juggle multiple disconnected tools that support either digital or analogue/RF designs, but not both.

SimRF is a new circuit envelope simulation tool that enables simulation of multifrequency dynamics in RF receivers and three-port components such as mixers. SimRF and Simulink together provide a common environment for modelling and simulating RF and baseband subsystems in a unified design. Used in combination, these tools enable system architects to perform realistic simulations early in the development process and make informed trade-off decisions in designs that include digital and analogue/RF components.



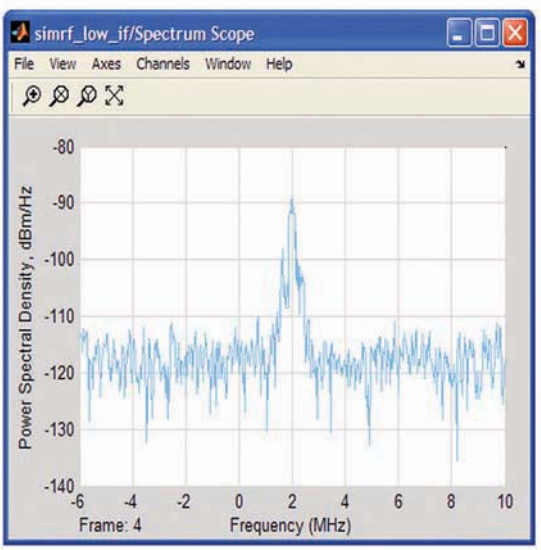




***Figure 4:*** *Input (left) and output (right) power spectral density plots showing the results of low IF image rejection*

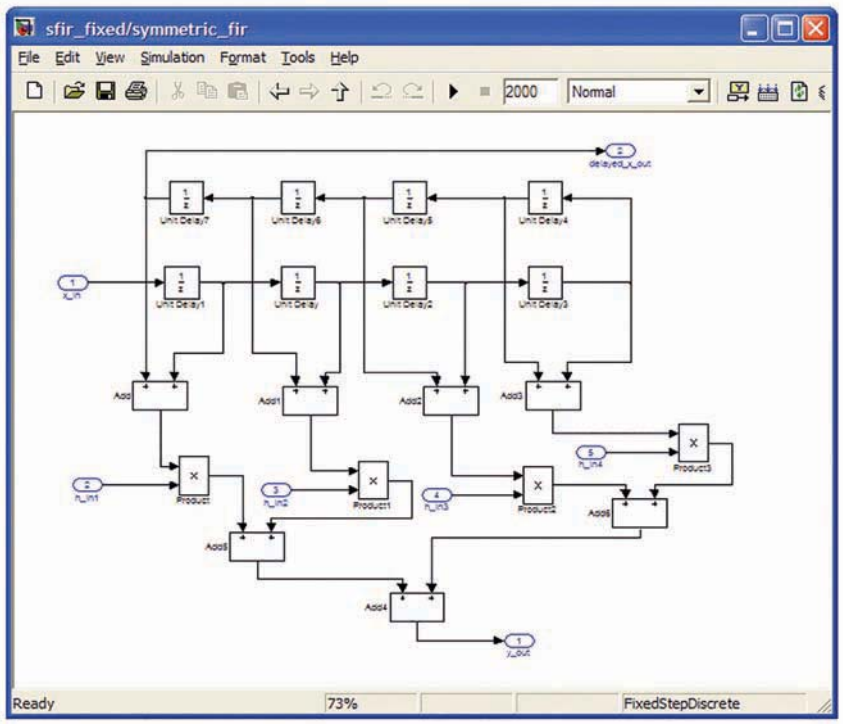



***Figure 5:*** *A symmetric fixed-point FIR filter modelled in Simulink*

**Figure 3** shows the overall system model of an ISM band low-IF receiver that includes both the digital signal processing components and the RF receiver subsystem. The details of the RF subsystem that implements a Hartley IF receiver are also shown. Unlike traditional methods of IF receiver modelling that use cascades of two-port elements and single-frequency approximations, the use of three-port elements simplifies the receiver model. The model also utilizes circuit envelope simulation technology and supports multifrequency modelling.

System architects can also explore the feasibility and relative merits of alternate approaches for image rejection such as super heterodyne or direct conversion architectures in the unified environment. In addition to simulating the effects of RF impairments, system architects can use the same system models used for design to perform the verification tasks in simulation that would normally be done on the lab bench.

## Hardware Design

After the algorithm design and system architecture are completed, the next step in many development cycles is FPGA implementation and verification of the digital portions. Among the primary sources of inefficiency in FPGA prototyping and implementation are the time-consuming design iterations that are required to find the proper balance of power consumption, performance and area.

**Figure 5** shows a symmetric FIR filter implemented in fixed-point arithmetic. To realize such a filter in hardware, engineers must carefully balance the throughput and latency and monitor the amount of hardware resources used. Critical path highlighting is a new capability that provides actionable information on potential bottlenecks in the system. Using the post-synthesis information generated by the Xilinx ISE synthesis tool, Simulink HDL Coder annotates the critical path timing in the Simulink model. Engineers can utilize this information together with pipelining techniques to partition their designs and the critical path latencies. **Figure 6** shows the same filter design, with the critical paths automatically highlighted, along with estimated latency for each path segment.

As mentioned above, pipelining is one of the key techniques that engineers utilize to address critical path latencies. One of the

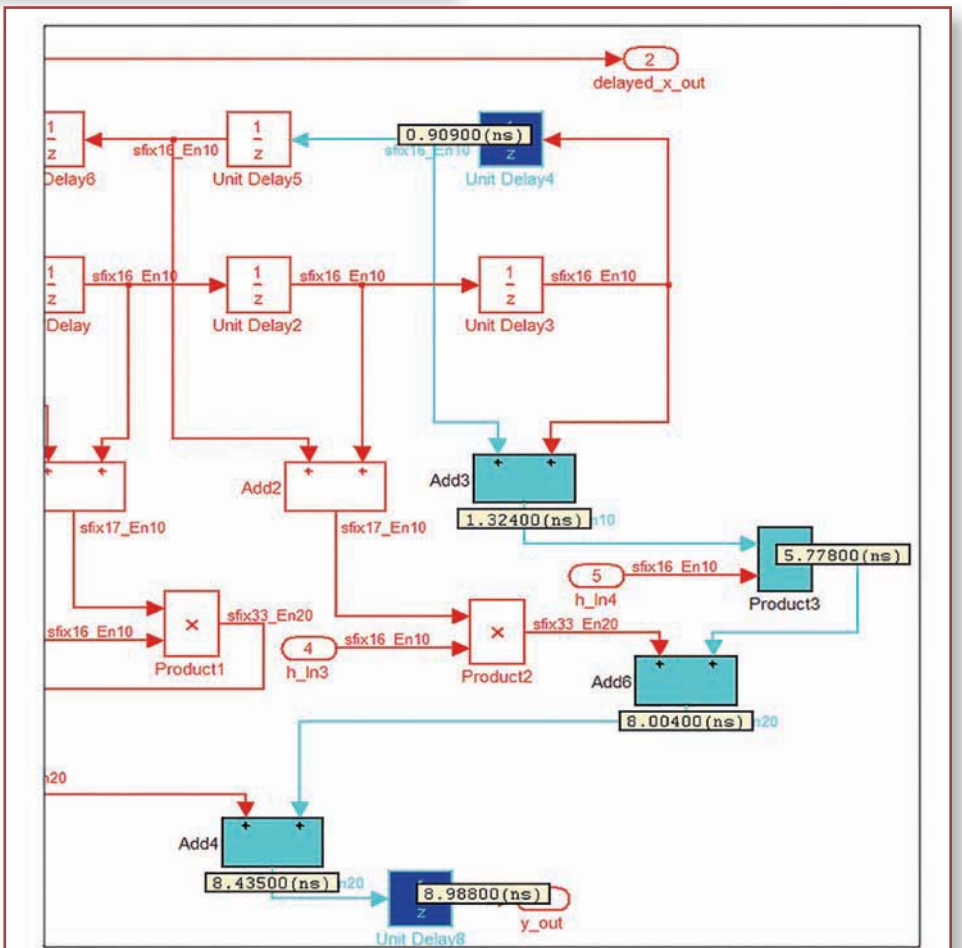



***Figure 6:*** *Symmetric fixed-point FIR filter showing critical paths and estimated latencies*

well-known challenges with pipelining is that parallel paths may have unmatched latencies, which can lead to unexpected or unwanted system behaviour. Distributed pipelining – a technique employed often to address this problem – can now be automated. By choosing this option, engineers can automatically retime the model and balance the latencies introduced by pipeline registers across relevant parallel paths.

In the past, these types of design iterations and trade-off evaluations have required a significant amount of time and effort. **Figure 7** shows a new workflow advisor console that enables engineers to go through design iterations much more quickly and in an intuitive manner. This is especially helpful to those that are not experts in HDL programming, but need to take advantage of FPGA processing. In addition to using critical path highlighting and distributed pipelining, engineers can also examine an automatically generated resource utilization report (like the one shown in **Figure 8**) to monitor the type and number of critical hardware components being used and determine the best architectural choice for a given situation by quickly iterating through several viable design options.

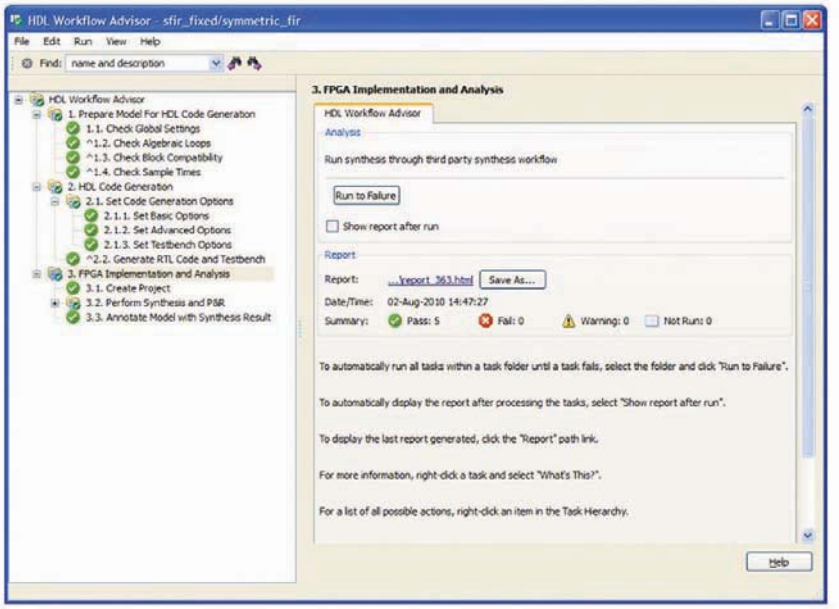



***Figure 7:*** *Workflow advisor console for performing quick design iterations in Simulink HDL Coder*

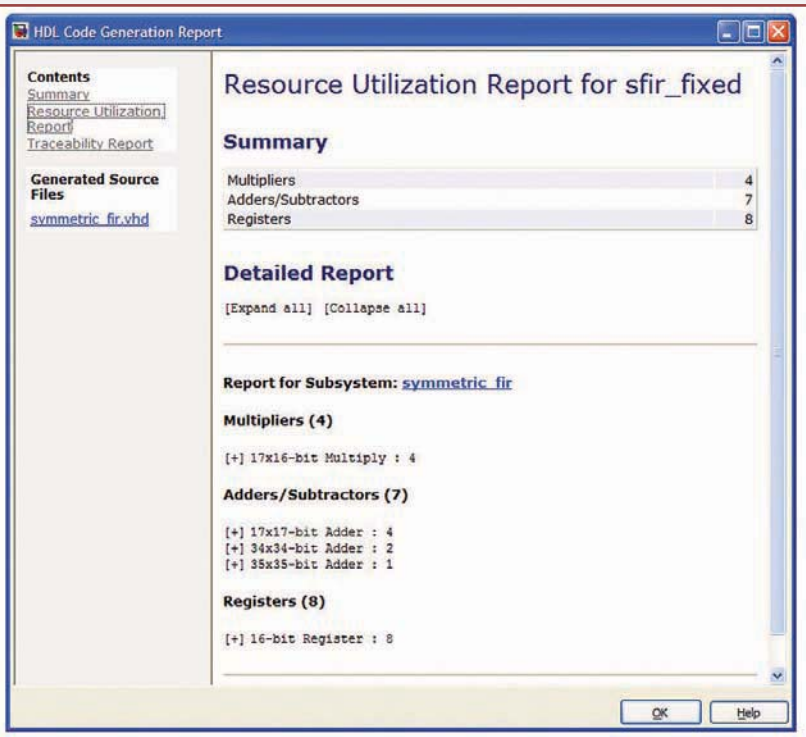



***Figure 8:*** *Resource utilization report indicating type, number and details of resources used*

## Accelerating Design Across Teams

Today's engineering managers face the challenge of coordinating geographically dispersed teams that are working on different parts of an overall system using different disconnected tools. In many cases, system-level designs are best done in graphical environments, while some lower level details are best expressed as text in MATLAB or C. This article presented some key new developments that improve efficiencies across various stages of the design flow.

For algorithm design, System objects are a key new development in modelling and simulating signal processing and communications systems. Several hundred ready-to-use signal processing and communications System objects are now available in MATLAB. Further, System objects support fixed-point arithmetic, and they can be integrated with Simulink or used in the automatic generation of C code.

SimRF, which features circuit envelope simulation technology, is an important new tool for more efficient system architecture flows. It enables engineers to model RF and baseband system components in a unified environment and perform true multifrequency simulations.

To improve the design iteration cycle times for hardware design, there are several new developments, including workflow advisor, critical path highlighting, distributed pipelining, back annotation and resource utilization reports, which provide a framework and critical actionable information on system performance and resources consumed.

Whether the teams are small or large, geographically distributed or located in the same office, engineering organizations that are struggling with discontinuities in their design workflow can apply these technologies to streamline and accelerate the development of complex signal processing and communications systems. ■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# Insights from the Couverture Project's R&D EXPERIENCE

*There's a constant demand for new functionality in products with safety critical components such as aircrafts, for example*

**COUVERTURE IS A** French R&D project that ended in October 2010 and which resulted in the addition of two tools to AdaCore's professional software product line aimed at the development of safety critical applications.

The first tool, GNATemulator, allows developers to replace target hardware boards by an emulation environment on the host for a significant part of the software testing activity. In addition, the tool can generate program execution traces for further analysis.

The second tool, GNATcoverage, uses these traces to produce structural coverage results, either at the machine instruction level or at the source code level. For the latter, GNATcoverage supports the source criteria specified in the DO-178B certification standard: Statement Coverage (SC) Decision Coverage (DC) and Modified Condition/ Decision Coverage (MCDC).

The Couverture project was made possible thanks to French public funds, awarded for a two-year time frame through the System@tic competitive cluster. The rest of this article provides insights and feedback on the project R&D experience, explaining in particular how Free Software and formal methods were key to the project's success.

## Project Background

The project ideas were based on recognizing a clear need for modern tools for safety-critical systems in light of several factors:

- Constant demand for new functionality in products with safety critical components (e.g. aircrafts, trains, nuclear plants),
- Increasing complexity of the software that manages all the components that make up these systems, and
- Continuing need to meet the relevant safety certification requirements.

These came at the same time as a number of developments in software methodology and certification standards, for example:

- Rise of lean/agile-like principles,
- Use of higher level abstraction facilities (e.g. Object-Oriented technology or models) to express application architectures and behaviour, and
- Evolution of the DO-178B standard towards DO-178C in the civil avionics domain.

In parallel, we were observing tangible progress in virtualization technologies, with solid Free Software options such as Qemu, and we were gaining new expertise in the safety critical certification processes.

In this context an opportunity appeared with respect to a common certification requirement: structural coverage analysis, which tells how much a given piece of an application program was exercised by a testing campaign.

Coverage analysis always relies on some sort of instrumentation, often achieved through additions to the original program or using hardware probes to track program execution on a target platform. A number of advantages and drawbacks go with each approach.

Program instrumentation is typically done at the source level so no dependence on a particular code generation toolchain is introduced. The changes are tied to specific programming languages, however, and the code exercised for coverage purposes is usually far from what is going to run on board. Target hardware probes alleviate these issues, but unfortunately require both the real target board and specialized extra components to monitor executions. This is often expensive, unavailable until late phases in the project schedules, inconvenient and source of bottlenecks because the setup cannot be replicated at will.

As a dynamic provider of Ada-related products and services, we were looking for solutions that could accommodate Agile development methodologies and handle recent revisions of the language (none were supporting Ada 2005 when the project started), as well as future evolutions.

Qemu was opening the possibility to implement the instrumentation at the machine instruction level within a robust and efficient simulation engine, which looked promising with respect to our objectives. Indeed, the coverage assessment process would remain language agnostic for the most part and be performed on target code

**Olivier Hainque,** senior software engineer at AdaCore, charts AdaCore's experience with the French R&D project called Couverture that resulted in two new tools for safety critical applications

very close to what is going to be embedded. It also would be extremely flexible, with setups running on development hosts and straightforward to replicate.

One potential drawback is the introduction of timing distortions by the simulation environment, which typically is a problem only for a very limited range of test categories. Another one is the need to interact with external devices, not always feasible directly from the simulation engine. Qemu is designed to be extensible on the latter front though and this also affects most source instrumentation technologies so many development teams know how to deal with this.

In addition to its technical merits, the approach presented an excellent opportunity to connect Free Software philosophy considerations with safety critical development, a prospect that we regarded as a fundamental value.

## Initial Directions

Targeting DO-178B-like certification processes upfront provided us with a few basic guidelines to follow. In particular, our framework from the start was intended to:

- Be adaptable to existing development environments, with continuous integration (scripting) capabilities for example,
- Come with open "qualification material", documents and requirements-based tests demonstrating that the tools may be used to fulfill the certification activity without requiring human verification of their assessment correctness,
- Support the coverage criteria mandated by the certification standards, up to the strictest levels of criticality.

The "open qualification material" idea quickly developed into an ambitious movement: the Open-DO initiative to encourage collaborative efforts for the open development of certification-oriented tools (**www.open-do.org**). This is a very lively pole of activity today, with an associated open development forge where the GNATcoverage sources and qualification testbase are hosted together with several other projects.

Regarding the support of the certification coverage criteria, we initially thought that we would be able to map simulation traces to them in a straightforward manner, with the help of standard debug information. This was not an obvious approach for DO-178, since the execution traces provide machine-level coverage information (this block was executed, that conditional branch was taken), while the standard objectives refer to source constructs only (*"statements", Boolean expressions known as "decisions", and atomic "conditions" in expressions*). We were targeting the highest criticality levels, however, and it was felt at the time that full object branch coverage (OBC) could be used as a replacement of the strictest criterion (MCDC) provided that the source program adhered to a few coding standard rules.

We wanted to validate this approach as part of our research effort, so we included activity in the project schedule to establish formal proofs of those assumptions correctness. As the following sections describe, we eventually came to devise a more ambitious scheme, with a much stronger source/object criteria separation and proofs of many more precise correspondence properties. This ultimately had a very positive impact on the whole project.

## Challenges and Resolutions

Attempting to rely on a straight mapping between object-level and source-level criteria turned out unsatisfactory in multiple respects.

First, even when sufficiently strong, an object level criterion typically calls for more testing – hence cost – than the associated source criterion would have required.

Consider the case of an integer modulo computation in Ada for example. While it is expressed as a single source statement like "X := Y mod Z;", this generates complex machine code for most architectures, with conditional branches and multiple path possibilities for variations on the operand signs.

By definition, a single execution of that statement is sufficient to cover it according to the statement coverage source criterion. Now, since that execution will only exercise a single set of Y and Z values, it will miss a number of machine instructions and cover some branches only partially. Indeed, simply achieving object instruction (not even branch) coverage will require multiple executions of the statement with carefully chosen values for Y and Z.

Putting costs aside, one could argue that this scheme leads to more confidence in the software, and therefore it is justified. However, it also became clear that some object coverage criteria require adherence to very restrictive coding standards in order to effectively guarantee coverage compliance at the associated source level. This is most evident in the OBC/MCDC case, as shown by counterexamples in "Object Oriented Technology Verification Phase 3 Report - Structural Coverage at the Source Code and Object Code Levels", Federal Aviation Administration, June 2007, DOT/FAA/AR-07/20, **http://www.faa.gov/aircraft/air_cert/design_approvals/air_software/research**, and then by our first formalization results which exposed a family of expressions with an arbitrarily large number (N) of conditions for which OBC can be obtained with three executions while MCDC requires a minimum of N+1.

The logical course of action from there was clear:

- Acknowledge the source level criteria as "first class citizens", keeping a strong distinction from object level assessments, and
- Continue with the formalization effort, which had proved invaluable already.

We were well rewarded by both directions,

which led to significant functional improvements and proofs of several useful properties, some never before published, and all providing strong confidence in our tool operation correctness. Formalizing also led us to a deeper understanding of many aspects of the problem space, with obvious benefits to the project as a whole.

## Source Coverage Obligations

The support of separate source level criteria without program instrumentation was no small undertaking. We introduced the notion of Source Coverage Obligations (SCOs) for this purpose.

A SCO is a piece of information describing the location in a source of a particular entity potentially relevant to coverage objectives, for example "statement at line 4 column 12" or "decision at line 4 column 24". We have implemented the generation of SCOs for Ada within the GNAT compiler, grouping all the SCOs for a source unit in a separate table, and we use the DWARF debug information to discharge SCOs from instruction execution traces. Roughly:

- The execution of an instruction discharges the statement for which this instruction was generated,
- The coverage status of source conditions is inferred from information about machine branches testing condition values (branch taken, not taken, or both).
- Decision and MCDC assessments are built from condition status consolidations, reconstructing observed decision evaluation "vectors" (sets of condition values and decision outcomes).

While the general principle is simple, a number of subtleties come into play regarding the decision and MCDC assessments.

First, we need to make sure that conditional branches indeed are generated for all the source conditions of interest and that we can locate those branches. The former is not a given for an industrial strength compiler, and the latter is not straightforward with complex operands potentially involving numerous internal tests. This eventually called for:

- Significant changes in the compiler debug information and code generation schemes, relying on the use of short-circuit operators, and
- Sophisticated heuristics in the analysis tools to map the machine code control flow onto the Binary Decision Diagrams (BDDs) of source expressions.

Second, even though we most often can deduce everything we need from local information about each condition (whether it has been evaluated both ways), we need to keep track of decision vector histories in a number of cases and thus we had to devise schemes to prevent excessive growth of execution traces.

Third, this all gets much more difficult with compiler optimizations turned on, which we aim at supporting so that coverage assessments can be performed on more cases of production embedded machine code.



## Source/Object Coverage Formal Properties

Our use of machine-level execution traces to infer source coverage criteria led us into a large OBC/MCDC-relationships formalization effort to establish solid grounds for our assessments. A number of these formal results have scientific value by themselves, worthy of publication (ongoing work here), and thus provide excellent value for the project's visibility. We complemented these proofs with Alloy (**http://alloy.mit.edu**) model checking to confirm the absence of counterexamples on subsets of the problem space, which provided an opportunity to look at the issue from a different angle.

Beyond their theoretical value, some of the demonstrated properties have important practical impacts on our tools, for example:

- Characterize situations in which we can rely on local OBC information to assess MCDC for a decision without vector histories, a major factor to reduce the execution trace sizes; or
- Let us implement a very efficient scheme to assess the "masking" variant of the MCDC criterion ("*An Investigation of Three Forms of the Modified Condition/Decision Coverage (MCDC) Criterion*", Federal Aviation Administration, April 2001, DOT/FAA/AR-01/18 **http://www.faa.gov/aircraft/air_cert/design_approvals/air_software/research**), thanks to possible shortcuts in the condition independence pairs identification process.

And as mentioned earlier, formalizing helped us gain a deep understanding of a number of subtle issues, with positive effects on the project as a whole. An example is the difficult area of "coupled conditions", when changing the value of one condition might influence the value of another, e.g. with "X >= 2 and then X <= 5", where changing X to exceed 5 necessarily makes X exceed 2 as well. We now understand what we can or cannot do in this domain and have expanded the qualification testbase accordingly.

This all resulted in an overall improved framework, which now scales up to industrial needs and is built on very robust foundations.

## In Retrospect

The Couverture project is a software R&D effort that has resulted in industrial products qualified for safety-critical development cycles. These products have already been adopted in real applications, and expanded usage is envisioned.

Four partners were involved in the project. On the industrial side: AdaCore to coordinate the efforts and provide a core set of qualified tools based on Qemu for traditional target architectures, and OpenWide to develop a first set of Qemu extensions widening the range of simulated board capabilities. And on the academic side: the LIP6 lab, exploring the use of similar ideas for Caml virtual machines, and Telecom ParisTech to investigate applications in the area of distributed or partitioned systems.

A number of factors have been key to Couverture's success:

- Timely public funds from the French administration and support from the System@tic competitive cluster made the project possible at all,
- The formalization effort, a natural component of a research activity, had both intrinsic scientific value and significant impact on industrial applications in the end (robustness, efficiency, scalability),
- Our fundamental trust in the Free Software philosophy drove us in constructive and beneficial directions, allowing use of open technology and contribution of results back to the community.

The last point is well illustrated by our use of Qemu, essential to the project elaboration as the main provider of execution traces, allowing coverage analysis on uninstrumented target code. The sources of our operational version are available from our open development forge and we plan on contributing these changes upstream.

The project pioneered the idea of setting up open environments for the development of tools aimed at safety-critical software certification activities, now possible on a much wider scale through the Open-DO initiative. ■

# Medical Device Software: Why has it gone code red?

**Nat Hillary**, Field Applications Engineer with LDRA Technologies, explains that other industries, such as avionics, have shown that seeking certification of a safety-critical software project drives the adoption of repeatable software development processes; this applies to developers of medical devices too

**THE TYPICAL MEDICAL** device software engineering process often suffers from gaps in repeatability. These gaps present enormous legal and financial risks to suppliers, as well as health and safety risks to patients. The use of application lifecycle management within a project can effectively mitigate these risks.

An FDA analysis of 3140 medical device recalls conducted between 1992 and 1998 reveals that 79% of software-related recalls were caused by software defects introduced when changes were made to the software after its initial production and distribution. The primary cause of these critical failures: repeatability. A software development process with a lack of repeatability is destined to failure.

All software contained in medical devices with a level of concern of major or moderate are inherently safety critical (see **Table 1**), so when submitting a device for certification, manufacturers must show that hazards are appropriately identified with risks managed effectively, in addition to providing traceability to link together design, implementation, testing and risk management.

In addition, to address both domestic and international markets, manufacturers are subject to laws and regulations that further complicate this task, such as the International Standards Organization (ISO) standards ICS 11.100.20 and 11.040.01 for medical devices. The International Electrotechnical Commission (IEC) standard IEC 62304 for medical software and the FDA guidance published against the *Code of Federal Regulations; 21 CFR Subchapter H – Medical Devices*. It is not surprising that medical device manufacturers complain that 80% of their software development budget goes into documentation and testing.

A repeatable process for medical device software ensures that the same levels of software quality are met for the initial product certification and any subsequent release. Criteria for software quality take into account not only the core functionality of the device, but also the device safety integrity level classified by the FDA as the Software Level of Concern. It would not be economically viable, for instance, to apply the same software development rigour in the development of a cardiac defibrillator (major level of concern) to the development of an electronic thermometer (minor level of concern).

The FDA classifies medical devices according to the software level of concern; an estimate of the severity of injury that a device could permit or inflict on a patient or operator as a result of device failures, design flaws, or simply by virtue of employing the device for its intended use. A major level of concern applies to a device such as a heart lung machine, where failure of the device would result in the patient's loss of life.

| SOFTWARE LEVEL OF CONCERN | DESCRIPTION |
|---|---|
| Major | A failure or latent flaw could directly result in death or serious injury to the patient or operator, or a failure or latent flaw could indirectly result in death or serious injury of the patient or operator through incorrect or delayed information or through the action of a care provider |
| Moderate | A failure or latent design flaw could directly result in minor injury to the patient or operator, or a failure or latent flaw could indirectly result in minor injury to the patient or operator through incorrect or delayed information or through the action of a care provider |
| Minor | Failures or latent design flaws are unlikely to cause any injury to the patient or operator |

***Table 1:*** *Different levels of Software Level of Concern*

Guidance for establishing a repeatable process that addresses the quality and safety concerns of medical devices that meet or exceed international standards can be obtained from both the FDA and the international community. In its document *Guidance for the Content of Premarket Submissions for Software Contained in Medical Devices* issued on May 11, 2005, the FDA clearly outlines the documentation that is required for the certification of a medical device to include software requirements specification, software design specification and traceability.

It's also necessary to produce a software development environment description, a document that outlines the software development process(es) used for the device. For this, the FDA recognizes as a consensus standard the international standard IEC 62304 *Medical Device Software – Software Lifecycle Processes*, so any compliant software development process meets the FDA requirement.

Defining a repeatable software development process is vitally important. **Figure 1** describes the software development process advocated by IEC 62304 for medical device software. This standard defines a rigourous software development process that incorporates the concept of risk (or safety) throughout the software development process and incorporates the need for both configuration management and defect tracking (i.e. problem resolution) systems.

Layered on top of the IEC 62304 software development process must also be the FDA requirement for traceability, which is a key factor in defining a repeatable software

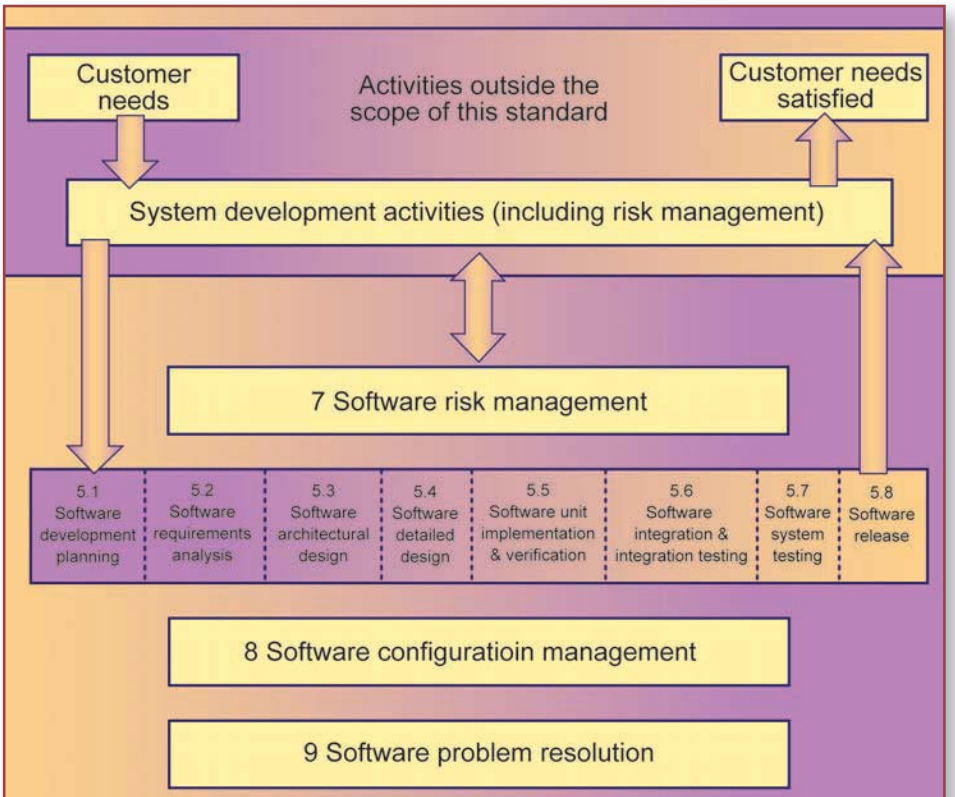



***Figure 1:*** *The International Electrotechnical Commission developed the IEC 62304 software lifecycle processes for medical device software*

development process. Traceability ensures that each high-level requirement originating in the system development activity step (pictured in Figure 1) is traced through the requirements decomposition tree down through the software design process and is then implemented and traced to code. This traceability must also map to the validation and verification activities used to ensure that the medical device software meets its functional and safety requirements. This yields a traceability matrix, where all of the traceability information is captured into a single document or database.

A traceability matrix maps the decomposition of each requirement into one or more sub-requirements, design elements, code and validation and verification activities. From this, the reverse is also true, so that any validation and verification task, design element or sub-requirement can be mapped back to its original requirement(s), whether primary or derived.

Maintaining a traceability matrix has two significant benefits. First, it helps in the certification process by providing clear documentation of how high-level requirements translate to code. Second, it assists in assessing the impact of any requirements, design or software changes. This latter point is especially important when it comes to post-release software, as the impact of any changes can be accurately assessed by determining how many system requirements, design, code and validation and verification activities are affected.

Where requirements are concerned, careful consideration must be made of the two primary sources of requirements; 'primary' requirements that come from the system functional definition, and 'derived' requirements that are inferred or derived from a primary requirement. For instance, a primary requirement may state that a system "differentiate between blood types O and B", and a derived requirement might be the proprietary laboratory technique, including any necessary preconditions used to determine this. A traceability solution needs to accommodate both primary and derived requirements.

For all but the most simple medical device software projects, manually creating and maintaining a traceability matrix is an arduous and error-prone task when done between high-level and low-level requirements. In a typical project, the number of system level and operating requirements multiplies up to five times when decomposed into sub-requirements, so a project of 100 primary system and operation requirements would decompose into 500 sub-requirements.

When you add derived requirements and map all of these to the design and code implementation, the complexity of manually creating and managing the traceability matrix magnifies. Extend this manual traceability to incorporate validation and verification activities, and you multiply both the effort and the possibility of introducing an error by an order of magnitude.

In a conservative example, if each high-level requirement traces to 5 sub-requirements, each of which maps to a single procedure in code and each procedure requires a set of 5 test cases for validation and verification (known good inputs, known bad inputs and 3 input parameter bounds tests), then it becomes immediately clear how challenging such an endeavour is. The traceability matrix would need to track the one-to-one, one-to-many and many-to-one mappings from the original 100 requirements through the decomposition to 500 sub-requirements to 500 procedures in code, and then onto 2,500 test cases.

Although it's tempting to simply ignore such a step, the impact of maintaining this mapping from high-level requirements through the decomposition, design, implementation and validation and verification processes is so significant, especially for certification, that it cannot be ignored.

This is where Application Lifecycle Management (ALM) solutions step in, providing a way for a development team to get their arms around the need to manage the myriad of details in a way that is cost-effective. Given that all medical device projects containing software include at least one processor, an IDE, an RTOS and other development tools, medical development teams should seek an ALM solution that addresses the extensive microdetail of embedded devices to ensure that a repeatable software development process can be developed and maintained.

## Application Lifecycle Management (ALM)

ALM is made possible by tools that facilitate and integrate software development activities such as requirements management, traceability, coding, software analysis, testing

and configuration management. Whether it is a requirement, line of code or test case, each artifact in the development process has its own lifecycle and workflow. It is the job of an ALM solution to provide a framework that supports the creation and evolution of each artifact through its lifecycle as a component of a complete product.

In **Figure 2**, the role of an ALM solution, such as the Embed-X solution from LDRA, within a typical embedded software development lifecycle can be understood.

Whether a new product or a new version of an existing product, the process normally starts with requirements capture, something that is handled by either a formal requirements management solution or using standard office editing tools. As requirements are developed and evolved, requirements decomposition occurs whereby high-level requirements are translated into subrequirements. It is also at this phase that derived requirements start to appear. An embedded ALM solution supports both requirements management and the ability to trace the evolution of requirements through the decomposition process, including the translation of requirements into the software design phase.

Once the code creation part of the process is reached, the ALM traceability solution extends to the software itself, creating a mapping from the high-level requirements through design and onto the actual code. At this phase, the code validation and verification tasks can be performed.

The validation and verification of safety-critical embedded software incorporates a number of different phases, starting as soon as the code is first created. An embedded ALM solution assists in the process of building quality into the software from code creation onwards, combining static analysis, unit and module testing, and dynamic code analysis.

Static analysis assesses the code under development without executing it, ensuring that errors and defects can be identified in code at the point of creation. A number of coding standards have been developed by industry groups specifically for high reliability software. Medical developers could borrow from these disciplines and use other safety-critical standards such as the Motor Industry Software Reliability Association (MISRA) standard MISRA-C:2004 or MISRA C++. These standards identify code constructs that are known to introduce latent defects in software, compromising dependability, and should therefore be avoided. Static analysis tools enforce these standards, in addition to identifying other issues in software, such as unnecessary complexity, that may affect code testability or maintainability.

Once the medical device code has been verified to meet the selected code standard, it is ready for unit and module testing. Incorporating a unit and module testing tool into an Embedded ALM solution enables the generation of requirements-based tests. The beauty of the integration inherent in an ALM solution ensures that the pass/fail results of these tests map back to the original requirements so that the project manager can monitor the current status.

While executing the code for either unit, module or system tests, it is then possible to perform dynamic analysis on the code under test. For example, it is possible to use coverage analysis to assess the effectiveness of the testing to date. Once again, the ALM integration tests completeness of the information all maps back to the requirements in order that the project manager can monitor status.

Not only does an ALM solution enable the monitoring and management of software through the development process, but the traceability of requirements through the development process to code and the associated verification activities and results makes documentation for project status and/or certification as straightforward as pushing a button, eliminating months of effort when a manual traceability process is used.

## Seeking Certification

Experience in other industries, such as avionics, has shown that seeking certification of a safety-critical software project drives the adoption of repeatable software development processes. The value of the concept and application of an Application Lifecycle Management tool suite within an avionics development process has proven time and again within the avionics community.

By adopting the software development processes advocated by IEC 62304, the medical device software development community ensures that software-related defects attributed to software maintenance can all but be eliminated. At the same time, by managing the evolution of project from requirements through design, coding and validation using and embedded ALM solution, they can make a significant dent in the 80% of development time typically spent on documentation and testing. ■

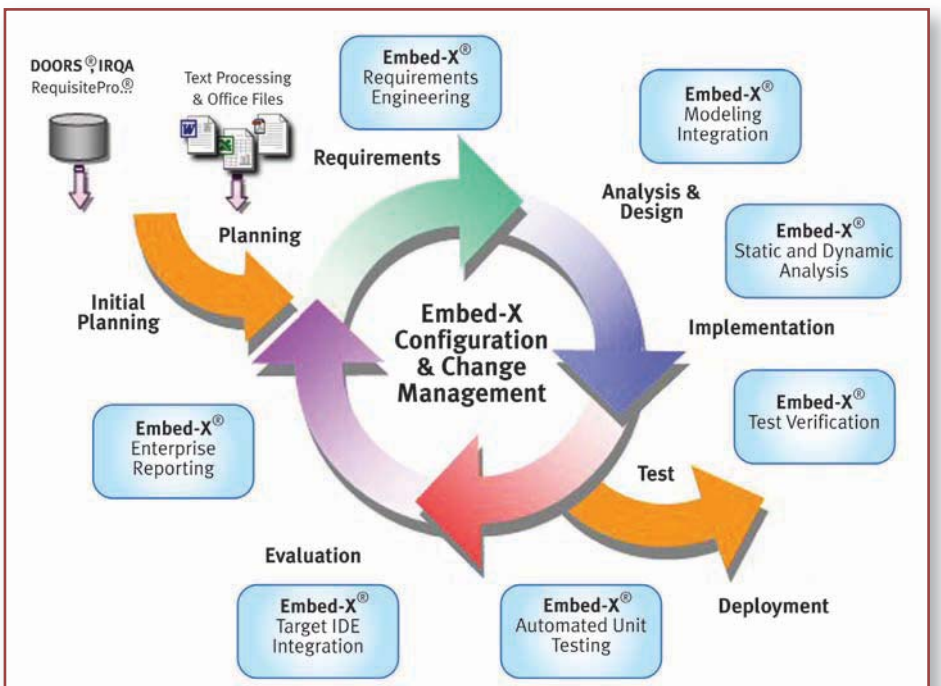



***Figure 2:*** *Embed-X, LDRA's application lifecycle solution, automatically feeds data back and forth through the phases of development*

# Channel Processing used in Mobile Satellite COMMUNICATIONS

In a series of three articles **Stojce Dimov Ilcev** of Mangosuthu University of Technology in Durban, South Africa, reviews the basic and state-of-art channel coding, decoding and error correction techniques as well as channel processing used in Mobile Satellite Communications

**CHANNEL PROCESSING** is composed of special activities, which can improve the transmission techniques of Mobile Satellite Systems (MSS), between Mobile (MES) and Land Earth Station (GES), throughout onboard satellite channels in connection with gain, errors, noise, interference, concentration and authenticity.

The system for digital speech concentration (interpolation) uses the activity factor of telephone channels in order to reduce the number of satellite channels required to transmit a given number of terrestrial channels. The Digital Speech Interpolation (DSI) technique is based on the fact that in a normal telephone conversation each participant monopolizes the circuit for only around half the time. As the silence between syllables, words and phrases increases so does the unoccupied time. Hence, on average, the activity time of a circuit is from 35% to 40% of the connection time.

By making use of the actual activity of the channels, several users can be permitted to share the same telephone circuit. Certain numbers of terrestrial satellite channels require only half the satellite channels and the gain is about 2. By adding a low rate encoder to the digital speech concentrator, the gain can be further increased. For example, with encoding at 32Kb/s a gain increases by a factor of 2 can be obtained in voice channels used alternately for speech or data transmission. The theoretical DSI gain is defined by the ratio between the actual number of speakers (input trunks) and the number of transmission channels (bearers) required to service them.

On the other hand, the function of the Digital Circuit Multiplication (DCM) equipment is to concentrate a number of input digital lines (trunks) onto a smaller number of digital output channels (bearers), thereby achieving a higher digital efficiency of the link or channels. This technique is qualified by the circuit multiplication gain, which is defined as the ratio of the input channels number over the number of DCM output channels. It is used in digital circuit multiplication equipment of the Intelsat/Eutelsat system.

## Channel Encoding

The two fundamental problems related to reliable transmission of information via channels were identified by C E Shannon as follows:

**1)** The use of minimal numbers of bits to represent the information given by a source in accordance with a fidelity criterion. In reality, this issue is usually identified as a problem of inefficient MSC, to which the source coding provides most practical solutions.

**2)** The recovery as exactly as possible of the information after its transmission through a communication channel in the presence of noise and other interference. This is a problem of unreliable MSC, to which channel (error) coding is the basic solution.

Shannon proved that by proper encoding these two objectives can always be achieved, provided that the transmission rate ($R_b$) verifies the fundamental expression $H < R_b < C$, where H = source entropy and C = channel capacity.

The Bit Error Rate (BER) of a digital system may be improved either by increasing $E_b/N_0$ or by detecting and correcting some of the errors in the received data. For the Additive White Gaussian Noise (AWGN) channel, the Shannon Hartley law states that capacity of a channel is given by the following relation:

$$C = B \log (1 + C/N)$$

where B = channel bandwidth in Hz and S/N = signal-to-noise ratio at the receiver. Thus, the channel capacity is the measure rate of the maximum information quantity that two parties can communicate without error via a probabilistically modelled channel. Namely, this chain of channels is composed of information data on input rate ($R_b$), channel encoder with redundancy data (r) and encoded data symbols on output rate ($R_c$).

A reverse channel model contains input encoded data symbols, channel decoder and output information data symbols. According to Shannon, if information is provided at rate R, which is less than the capacity of the channel, then a means of coding can be applied such that the probability of error of the received signal is arbitrarily small. If this rate is greater than the channel capacity, then it will not be possible to improve the link quality by means of coding techniques. Indeed, its application could have a detrimental effect on the link. Rearranging the above equation in terms of energy-per-bit and information rate, where the information rate is equal to the channel capacity, results in the following:

$$C/B = \log (1 + E_b\, C/N_0 B)$$

where $E_b$ = information bit rate; $E_b$ = related to the carrier power and the

– PART 3

**Figure 1:** *Cyclic decoding system*

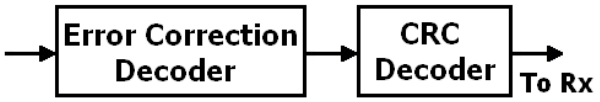



**Figure 2:** *Transmission scheme with insertion of interleaver into a serial concatenation of convolutional codes (convolutional coding and decoding)*

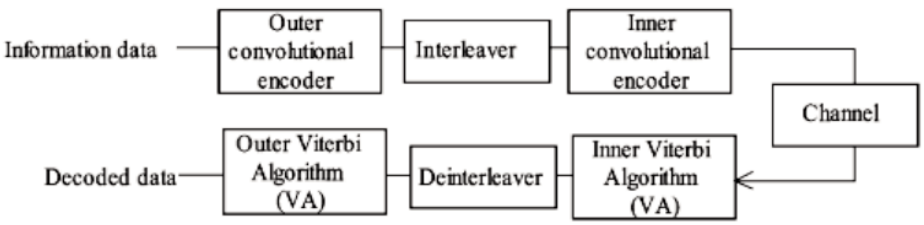
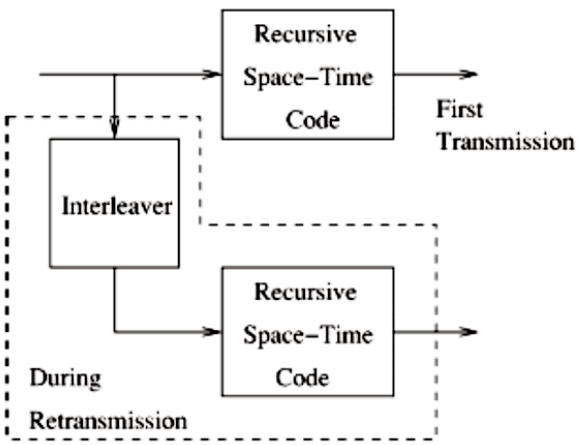



**Figure 3:** *Encoder structure for ARQ system*




information bit rate and $C/N_0$ = carrier-to-noise density ratio. Moreover, the above expression can be utilized to derive the Shannon limit, the minimum value of $Eb/N_0$ below which there can be no error-free transmission of information. As C/B tends to zero, this can be shown to be equal to -1.59dB ($1/\log_2 e$). The code rate and input rate can be defined as:

**$c = n/n + r$ and $R_c = R_b/n$**

The capacity of the channel is independent of the coding/modulation scheme used. Hence Shannon's channel coding theorem exactly stated that, for a given carrier-to-noise ratio, the error probability could be made as small as desirable, provided that the information rate ($R_b$) is less than the capacity (C) and a suitable coding is used. In any case, in MSC systems, channel coding is especially interesting because of the severe power, bandwidth and propagation limitations. Moreover, the considerable progresses in multiple access modulation schemes, resource assignment algorithms, signal processing techniques and advanced error control coding provide the most efficient means to realize highly reliable information transmission.

## Digital Compression

Digital transmission in general uses compression techniques for data and video signals. The effective data transfer via the Inmarsat MSC system can be significantly increased by using data compression software. Essential results were provided on PC by the PKZIP/PKUNZIP program developed by US-based PKWARE, which in a fraction of a second gives a 2 to 3 times reduction in size of ASCII files and 1.5 times for many types of binary files.

The ARJ compression software from Robert K Jung is slower but more effective than PKZIP. It can also be recommended for the compression of data files containing graphic information. Thus, the real-time data compression incorporated into the most advanced modems can also increase the effective data rate of ASCII files transmission but for transmission of already compressed files with information it is better not to use the compression in the modem.

Their use in compressed video systems, where a TV Receive Only (TVRO) can also receive many channels of video from one transponder (about 6 to 8), has become very widespread, first in the US and then in Europe. The compression system that has now become standard refers to a Moving Picture Expert Group (MPEG), formed under the auspices of the ISO and the International Electrotechnical Commission (IEC). In such a system a number of digitized videos are combined into a single bit stream in a source coder. That bit stream is then sent to a channel coder for FEC and then to a QPSK modulator, an up-converter, amplifier and an antenna for up-linking to the satellite transponder. Since only one signal is present in the spacecraft transponder at any on time, there is no need for back-off and full transponder power is used.

At the reverse side, the compressed video downlink comprises a line in the chain of an antenna, tuner including down-converter and QPSK demodulator, then FEC detector, demultiplexer and MPEG decoder. Therefore, the MPEG is determined to provide standard

compression that allows video and accompanying audio signals to be compressed in channel width.

The packetizer function is to enter a suitable code in the bit stream for the individual digitized TV program so that it can be separated in the receiving chain, allowing the enabled user to select the desired program. Thus, the BER is determined from the ($E_b/N_0$) obtained for a combination of whatever transponder EIRP, FEC coding, transmission symbol rate and receiver system are used. If a plot of that FEC system is not available, then the Viterbi mode FEC coding performance could be used for a good estimate of results. This type of compression has effects like: MPEG-2 compression results in the removal of most audio and video redundancy; the FES utilization scheme resulting in a rapid BER increase and the resultant ($E_b/N_0$) should be high enough to achieve a BER of $10^{-6}$ for a TVRO.

## Voice Encryption

Encryption is used when it is wished to prevent exploitation or tampering with transmitted messages or voice conversation by unauthorized users, in the form of algorithmic operation in real time, bit-by-bit, on the binary stream. Thus, the set of parameters, which defines the transformation, is called a key. Its use is often associated with military communications but commercial satellite systems are increasingly induced by customers to propose encrypted links, particularly for administrative and government sectors. In fact, due to the extended coverage of satellite networks and the easy access to them by small MES, eavesdropping and message falsification are potentially within the reach of a large number of agents of modest means.

The encryption transmission chain is composed of an encryption unit with plain text input, satellite channel with intruder and key distribution for retransmission of cipher (encrypted) text and de-encryption with a unit for production of plain output text. The encryption and de-encryption units operate with a key provided by the key generation unit. Acquisition of a common key implies a secure method of key distribution. This key is entered into the encryption unit through a key injector about the size of a matchbox. Without this key, a potential eavesdropper attempting to listen in on the conversation would hear nothing but a noise made up of digital signals.

The technique used for most voice encryption consists in speech compressing and digitizing, using a very complicated coding process. In such a way, the voice signal is sliced into small bits, which are processed by an algorithm into bits of voice with a very complex structure. At the other end of the process, using the same key pattern, the voice is reproduced as it was before the encryption.

A typical example of voice encryption for MSC is Satsec A1 for secure voice transmission, of Inmarsat standard-A MES. This unit is housed in a modern smart telephone, which uses a very sophisticated Swiss encryption technique. The Satsec A1 features include full digital voice and facsimile encryption and LPC voice compression, using full duplex operations CCITT V.22bis and V.27 Modem with a rate of 2400b/s, giving business users a security level comparable to that used by government agencies. In case of transmission only in half duplex mode, the unit automatically falls back to the built-in VOX-controlled quasi-duplex operational mode. Hence, this device should not be confused with a voice scrambler, even a digital one, which is no longer a competitive alternative to high level encryption. The unit digitizer uses linear predictive coding and has, unlike self-synchronizing stream ciphers, no bit error multiplication. In a more general sense, under the same circumstances, this device may even have an enhanced effect on the channel is quality of transmission.

The aspects of encryption are confidential to avoid exploitation of the voice/message by unauthorized persons and to provide authentic protection against any modification of the message by an intruder. This system uses the following technique:

**1. On-line encryption (Stream Cipher).** Each bit of the original binary message stream (plain text) is combined using a simple operation, for example modulo-2 addition, with each bit of a binary stream (keystream) generated by a key device. Otherwise, the latter could be a pseudorandom sequence generator whose structure is defined by the key.

**2. Encryption by Block (Block Cipher).** The transmission of the original binary stream message into an encrypted stream is performed simply block-by-block, according to the logic defined by the key.

Besides, encryption is commonly used in direct TV broadcasting to avoid illegal reception and military applications to minimize the probability of message interception.

## Going Forward

In this series we reviewed basic and state-of-art coding, decoding and error correction techniques for MSC. Those techniques have been used extensively in digital MSC, because they are providing cost-effective solutions in achieving efficient and reliable digital transmissions. Coding now plays an important role in the design of modern MSC and forthcoming generations of technology are expected to continue this trend with development more complicated, but more economic coding schemes.

Future Mobile and Fixed Satellite Communication Systems cannot be totally separated from development of terrestrial broadband and broadcast communication systems. In this perspective, development of new satellite systems and techniques tends to align with that of terrestrial communications and to provide full integration between two networks, which will allow high data-rates and high quality of service, anytime and anywhere.

Looking at this framework it will be necessary to highlight some of fundamentals of coding, decoding and error correction technologies, developments and their evolution. In particular the improvement of communication links and modelling of channels for MSC need design and implementation of modern coding and interference cancellation techniques.

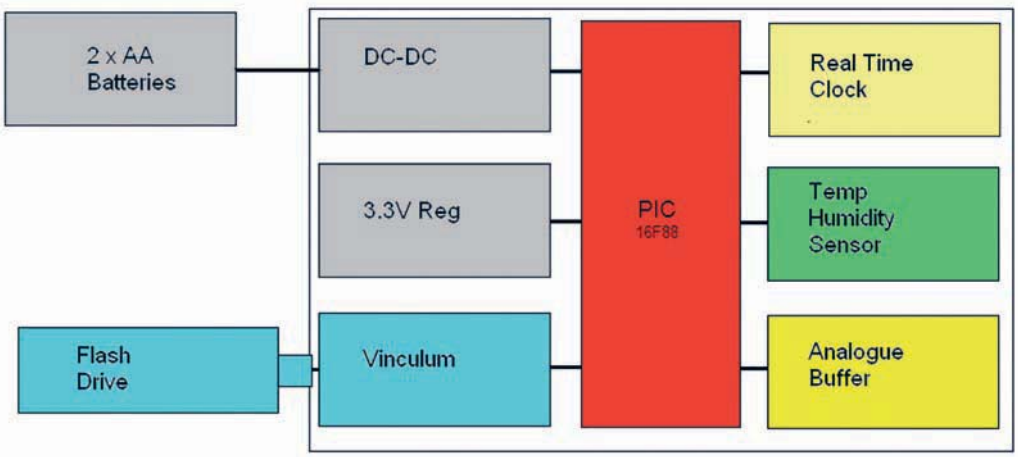
In this innovative age of ICT it is becoming essential to provide communications of information to people on the move at sea, on the ground and in the air, having sometimes difficulties to locate some of them precisely. Therefore, the deployment of channel coding and interleaving will enhance the bit-error performance of MSC links addressed for digital speech and data transmissions. ■

*If you missed Part 1 or 2 of this article you can order the digital copy of that issue on line at* ***www.electronicsworld.co.uk***

# Adding a USB Flash drive for data distribution

**John Hyde** from Future Technology Devices International (FTDI) will implement a series of USB projects over the course of the following editions of Electronics World

***Figure 1:*** *Block diagram of a battery-operated data logger*




**AS DISCUSSED IN** the last part of this series, the Vinculum-I dual host controller can be employed in a variety of applications. We investigated a data distribution system last month, this month we investigate a portable data logger which is capable of collecting field data for later analysis by a PC. In this particular example we will use a member of the popular MicroChip Technology PIC microcontroller series, employing the CCS toolset to create the necessary application program.

I have argued that a compiler would always generate larger object code than my tuned assembler code, but as these microcontroller devices are now available with 16kB, 32kB and beyond, of Flash memory, what is the point of saving a few hundred bytes when you still have over half of the Flash space as unused? C code is also much easier to write, debug and maintain when compared with assembler code.

The CCS compiler was specifically designed to create optimized code for the PIC family of microcontrollers. As well as all of the standard features that you would expect from a quality C compiler, it includes built-in functions to support the on-chip features of a PIC microcontroller. A good example is the #use RS232 directive: here you specify that you need to use a serial port and give the compiler details such as baud rate and the IO pins that will be used for TX and RX. If the chosen PIC device has hardware UART then the compiler will use this for printf and scanf functions, otherwise it will include subroutines to manage the low-level bit manipulations for you. Your main program uses printf statements as before. The CCS compiler also contains built-in functions to drive the on-chip analogue to digital converter and the real-time clock. This makes it possible to focus fully on what your program is doing and not on how it is doing it.

The block diagram of a battery-powered data logger is shown in **Figure 1**. DLP Design manufacture and sell an evaluation board, shown in **Figure 2**, and this DLP-VLOG board demonstrates the capabilities of the Vinculum-I dual USB host controller. The example program uses a serial connection to control the Vinculum-I, which writes data to the Flash drive. The hardware connection is a standard 4-wire serial port using TX, RX, RTS and CTS. The PIC microcontroller runs an application program that has access to a Flash drive using the Vinculum-I device, a real-time clock, a temperature and humidity sensor, plus two analogue input channels. A connector for the ubiquitous TTL-232R cable is included, as is a connector for a PIC debugger such as the CCS ICD-U40 unit.

The application program first checks to see if a Flash drive is present and if one is not found then the PIC goes back to sleep, since there is no point collecting data if there isn't anywhere for it to be stored. Once a Flash drive is found the PIC will start a collection cycle. It first reads the real-time data from the Dallas/Maxim DS1302 timekeeping chip, then the two analogue signals and the battery voltage, followed by the temperature and humidity sensor. This data is then written to the Flash drive and the system goes back to sleep so that it can save its remaining battery power. This cycle is repeated while a Flash drive is present and the battery is charged. The Flash drive may be removed at any time and the collected data may then be analyzed using a PC. The source code for the application is available with the development kit so that you can customize the data collected and the time interval between samples.

This, and the example in last month's article, explains how to implement embedded Flash drive designs in a quick and simple manner. The Vinculum-I controller implements all of the required industry standard specifications and presents a simple DOS-like command line interface that is accessed via a serial port (or SPI or

parallel FIFO). It is just a simple matter of adding your specified microcontroller with an application program to control the Vinculum-I peripheral.

Hopefully, the examples presented in this and the preceding article will help to fuel your imagination. These examples used in turn a Cypress PSoC and a Microchip PIC but the code is readily ported to different microcontroller architectures too. Your project can collect data that is later analyzed on a desktop PC system or it can be used to redistribute data that was created on a desktop system via lower cost platforms. Project data may be updated by simply swapping Flash drives.

If you can read and write to a serial port then, with a Vinculum-I controller, it is possible for you to read and write data files onto a Flash drive.

Next month we will discuss FTDI's latest dual host controller product, the Vinculum-II which has more RAM, Flash memory and IO capabilities but, most important for us, is that it is user programmable. This will allow us to run the application program on the Vinculum-II itself and we will not need an adjacent microcontroller. More capability for less cost – isn't silicon wonderful!

*If you missed any other parts of this series you can order their digital magazine issues by going on line at* ***www.electronicsworld.co.uk***


***Figure 2:*** *The DLP-VLOG showcases Vinculum-I's capabilities*

# PAK Series AC-DC Power Supplies from 650W to 3000W

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- Intelligent LED indicator shows output status & fault conditions
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- Full safety approvals and EMC conformity

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| | |
|---|---|
| PAK650 | 41 x 127 x 249mm |
| PAK1000 | 41 x 127 x 283mm |
| PAK1500 | 63.5 x 127 x 280mm |
| PAK3000 | 127 x 127 x 280mm |

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# TIP 1: BATTERY CONDITIONER EXTENDS THE LIFE OF LI-ION BATTERIES

*By George H. Barbehenn, Senior Applications Engineer, Linear Technology*

**LI-ION BATTERIES** naturally age, with an expected lifetime of about three years. But, that life can be cut very short – to under a year – if the batteries are mishandled.

It turns out that the batteries are typically abused in applications where intelligent conditioning would otherwise significantly extend the battery lifetime.

Modern Li-Ion batteries are constructed of a graphite negative terminal, cobalt, manganese or iron phosphate positive terminal and an electrolyte that transports the lithium ions.

The electrolyte may be a gel, a polymer (Li-Ion/Polymer batteries) or a hybrid of a gel and a polymer. In practice, no suitable polymer has been found that transports lithium ions effectively at room temperature. Most 'pouch' Li-Ion/Polymer batteries are, in fact, hybrid batteries containing a combination of polymer and gel electrolytes.

The charge process involves lithium ions moving out of the negative terminal material, through the electrolyte and into the positive terminal material. Discharging is the reverse process. Both terminals either release or absorb lithium ions, depending on whether the battery is being charged or discharged.

The lithium ions do not bond with the terminals, but rather enter the terminals much like water enters a sponge; this process is called 'intercalation'. So, as is often the case with charge-based devices such as electrolytic capacitors, the resulting charge storage is a function of both the materials used and the physical structure of the material. In the case of the electrolytic capacitor, the foil is etched to increase its surface area. In the case of the Li-Ion battery the terminals must have a sponge-like physical make-up to accept the lithium ions.

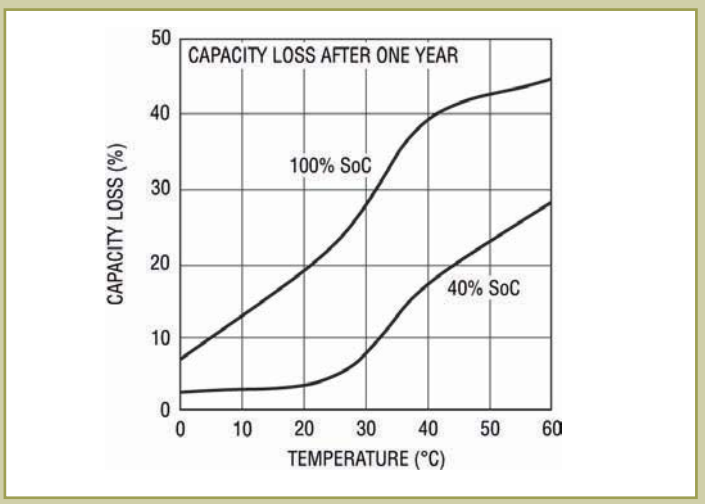



***Figure 1:*** *Yearly capacity loss vs temperature and state of charge for Li-Ion batteries*

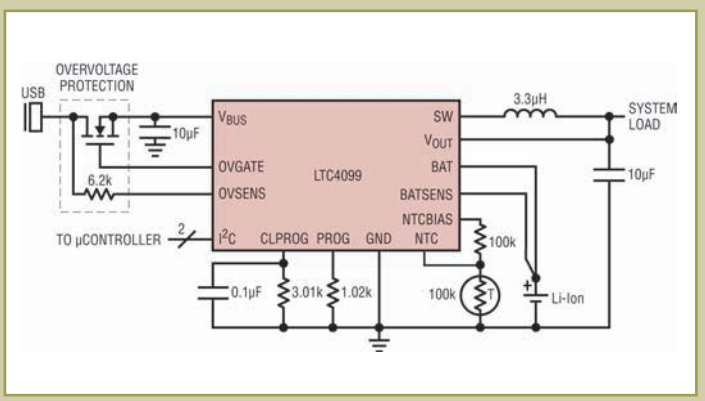



***Figure 2:*** *The LTC4099 with I2C controlled battery conditioner*

The choice of positive terminal material (cobalt, manganese or iron phosphate) determines the capacity, safety and aging properties of the battery. In particular, cobalt provides superior capacity and aging characteristics, but it is relatively unsafe compared to the other materials. Metallic lithium is flammable and the cobalt positive terminal tends to form metallic lithium during the discharge process. If several safety measures fail or are defeated, the resulting metallic lithium can fuel a "vent with flame" event.

Consequently, most modern Li-Ion batteries use a manganese or iron phosphate-based positive terminal. The price for increased safety is slightly reduced capacity and increased aging.

Aging is caused by corrosion, usually oxidation, of the positive terminal by the electrolyte. This reduces both the effectiveness of the electrolyte in lithium-ion transport and the sponge-like lithium-ion absorption capability of the positive terminal. Battery aging results an increase of the battery series resistance (BSR) and reduced capacity, as the positive terminal is progressively less able to absorb lithium ions.

The aging process begins from the moment the battery is manufactured and cannot be stopped. However, battery handling plays an important role in how quickly aging progresses.

## Conditions That Affect the Aging Process

The corrosion of the positive terminal is a chemical process and this chemical process has an activation energy probability distribution function (PDF). The activation energy can come from heat or the terminal voltage. The more activation energy available from these two sources the greater the chemical reaction rate and the faster the aging.

Li-Ion batteries that are used in the automotive environment must last 10 to 15 years. So, suppliers of automotive Li-Ion batteries do not recommend charging the batteries above 3.8V. This does not allow the use of the full capacity of the battery, but is low enough on the activation energy PDF to keep corrosion to a minimum. The iron phosphate positive terminal has a shallower discharge curve, thus retaining more capacity at 3.8V.

Battery manufacturers typically store batteries at 15°C (59°F) and a 40% State of Charge (SoC) to minimize aging. Ideally, storage would take place at 4% or 5% SoC, but it must never reach 0%, or the battery may be damaged. Typically, a battery pack protection IC prevents a battery from reaching 0% SoC. But pack protection cannot prevent self-discharge and the pack protection IC itself consumes some current.

Although Li-Ion batteries have less self-discharge than most other secondary batteries, the storage time is somewhat open-ended. So, 40% SoC represents a compromise between minimizing aging and

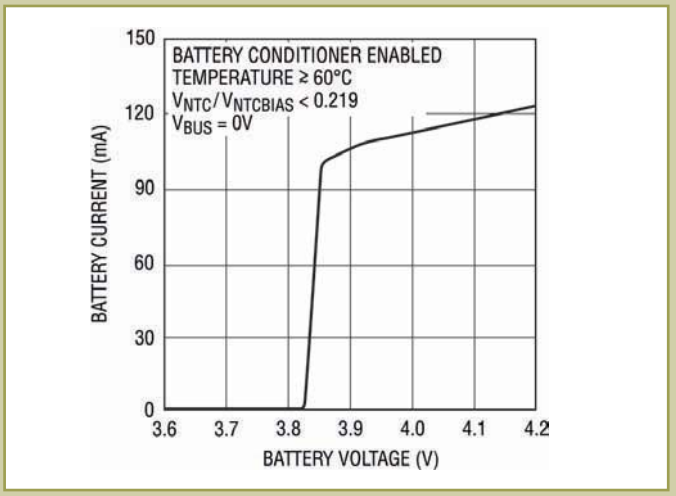



***Figure 3:*** *Battery discharge current vs voltage for the LTC4099 battery conditioning function*

preventing damage while in storage (see **Figure 1**).

In portable applications, the reduction in capacity from such a reduced SoC strategy is viewed negatively in marketing specifications. But it is sufficient to detect the combination of high ambient heat and high battery SoC to implement an algorithm that minimizes aging while ensuring maximum capacity availability to the user.

## Battery Conditioner Avoids Conditions that Accelerate Aging

Linear Technology has the LTC4099 battery charger and power manager contains an I2C controlled battery conditioner that maximizes battery operating life, while also optimizing battery run time and charging speed (see **Figure 2**).

It has a built-in battery conditioner that can be enabled or disabled (default) via the I2C interface. If the battery conditioner is enabled and the LTC4099 detects that the battery temperature is higher than ~60°C, it gently discharges the battery to minimize the effects of aging.

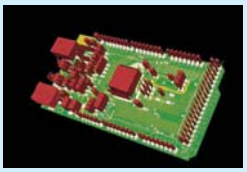
The LTC4099 NTC temperature measurement is always on and available to monitor the battery temperature. This circuit is a micropower circuit, drawing only 50nA while still providing full functionality.

The amount of current used to discharge the battery follows the curve shown in **Figure 3**, reaching zero when the battery terminal voltage is ~3.85V. If the temperature of the battery pack drops below ~40°C and a source of energy is available, the LTC4099 once again charges the battery. Thus, the battery is protected from the worst case battery aging conditions.

Although the aging of Li-Ion batteries cannot be stopped, the LTC4099's battery conditioner ensures maximum battery life by preventing the battery-killing conditions of simultaneous high voltage and high temperature. Further, the micropower, always-on NTC monitoring circuit ensures that the battery is protected from life-threatening conditions at all times. ■

## NEW IN APRIL

**National Electronics Week (NEW) is taking place between the 12th and 13th of April at the NEW Pavilion in Birmingham, UK. International Exhibitors come from all aspects of embedded and electronics technologies. There will be a full programme of free seminars and workshops covering current topics and industry trends, as well as hands-on workshops featuring rapid prototyping and a live on the show features, including the 'Future Proof Assembly Line'. To find out more or register go to www.new-expo.co.uk**



### RS COMPONENTS UPGRADES DESIGNSPARK PCB WITH 3D VERSION 2

RS Components has announced the release of DesignSpark PCB version 2, its free PCB design software package. Working in partnership with Number One Systems, new features in DesignSpark PCB include unique 3D visualisation of PCB layouts and increased library management functionality. The upgraded version 2 software is free to download for new users at www.designspark.com/pcb and existing users will be alerted to the upgrade via release alerts in the tool.

DesignSpark PCB has been strengthened in three key areas. A 3D viewer has been added to the tool. This enables engineers to see a three-dimensional representation of their board at any stage during design, allowing fast evaluation of mechanical design requirements within their existing eCAD package.

**www.designspark.com/pcb** **Stand 311**

### SMART CHARGER FROM POWERSOLVE CAN DETECT UP TO 12 NIMH/NICD CELLS

Among the many new and innovative power supply products that Powersolve will be showing is the PSCH15, an intelligent battery charger that can automatically detect and charge up to 12 NiMH or NiCD cells. It is "clever" enough to identify from 2 to 12 cells in series and provide the necessary output to fully charge the cells and then turn itself off.

Output voltage which varies depending on load is from 2.4 to 14.4V and output current is from 500mA to 1A. Safety ground leakage current is < 0.5mA. Overvoltage and short circuit protection is standard as is protection against reverse polarity. An LED status indicator confirms standby, charging and fully charged states.

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In 2009, Farnell launched element14, the first, innovative information portal and eCommunity specifically built for electronic design engineers. It attracts more than 24,000 visitors a week providing them with product data, design tools and technology information, whilst incorporating Web 2.0 functionality to facilitate communication, interaction, collaboration and information sharing between colleagues around the world. Users can consult experts, discover trends, post blogs, articles and comments in this worldwide forum.

**www.farnell.co.uk**
**www.element14.com** **Stand N621**

### AGILENT TECHNOLOGIES INTRODUCES OSCILLOSCOPES WITH BREAKTHROUGH TECHNOLOGY

InfiniiVision 2000 X-Series offers 70MHz to 200MHz bandwidths, the fastest waveform update rate in its class for superior viewing of signal detail and capture, and optional integrated function generator offers more capabilities to engineers and educators with constrained equipment budgets.

InfiniiVision 3000 X-Series scopes offer a stepped-up performance, offering 100MHz to 500MHz bandwidths and industry-leading waveform update rates.

Find out more on Agilent's InfiniiVision 2000 and 3000 X-Series at:

**www.agilent.com/find/InfiniiVisionX-Series** **Stand N331**

## LECROY INTRODUCES THE REVOLUTIONARY WAVERUNNER 6 ZI OSCILLOSCOPE PLATFORM

LeCroy Corporation has launched WaveRunner 6 Zi oscilloscopes with a powerful feature set. The new family features a pristine signal path that offers unmatched signal fidelity with low noise. This performance is augmented by a huge offset and timebase delay adjustment to allow easy signal and amplifier performance assessment and zooming on vertical and horizontal signal characteristics. With deep memory up to 128Mpts, up to 40GS/s sample rate, low noise, fast operation, a full line of probing solutions, and extensive serial data analysis tools, they are the most versatile oscilloscopes in the 400MHz to 4GHz class.

LeCroy is also pre-announcing the first product line of 12-bit oscilloscopes with 400MHz bandwidth, 2GS/s sample rate and up to 256Mpts to be launching in the coming months.

In addition, LeCroy has designed the WaveRunner 6 Zi with a pivoting display that permits viewing signals vertically as well as horizontally to obtain more detail for optimum analysis.

**www.lecroy.com**

## KONTRON EXPANDS VPX ECOSYSTEM WITH SECOND GENERATION INTEL CORE I7 PROCESSOR SUPPORT

Kontron expanded its VPX ecosystem with the new Kontron 3U VPX CPU board VX3035 based on the second generation Intel Core i7 processor. Integrating the Intel Core i7 2655LE processor, Intel HD graphics and features such as Intel Turbo Boost technology and Intel Advanced Vector Extensions (Intel AVX), the new 3U VPX CPU board defines a new performance class for SWaP (size, weight and power) optimized high-performance embedded computing applications.

OEMs will benefit from the Kontron 3U VPX CPU board VX3035 due to its outstanding versatility and x86 technology, coupled with high vectorial and parallel computing power. System developers can develop extremely compact and light applications with high parallel computing power, such as video and image processing, radar, sonar or signal processing in software-defined wireless equipment.

The new VPX board also supports established APIs such as Open CL, which simplifies and speeds up application development.

**www.kontron.com**

## EXPANDED INDUSTRIAL ECOSYSTEM FOR SMARTFUSION MIXED SIGNAL FPGAS

Microsemi Corporation announced an expanded industrial ecosystem for SmartFusion intelligent mixed-signal FPGAs. This new ecosystem strengthens the current SmartFusion device ecosystem and includes further support by Microsemi partners. Customers now have a broader choice of operating systems and communication protocols for implementation on SmartFusion FPGAs, enabling the acceleration of their designs in industrial and networking applications.

The range of peripherals SmartFusion devices offer for the ARM Cortex-M3 processor and the flexibility of their FPGA fabric make them an ideal choice for industrial automation and networking.

Each uniquely capable section of the SmartFusion intelligent mixed signal FPGA device enables targeted solutions addressing multiple aspects of an integrated industrial automation system. The SmartFusion FPGA Ecosystem features include the first port of uClinux to the SmartFusion device including a development platform available for purchase online; CAN core for SmartFusion, supported on the SmartFusion Development Kit; FreeRTOS as a reference design on both the SmartFusion Evaluation Kit and the SmartFusion Development Kit and others.

**www.microsemi.com**

## SIMPLE, COST-EFFECTIVE SMT COIN CELL HOLDER

Harwin has expanded its range of EZ BoardWare products with the introduction of a single piece surface mountable coin cell holder which ensures coin cells are securely retained in place while cutting assembly time. EZ Coin Cell Holders can accommodate 12.5mm diameter x 2.5mm thick BR1225 and CR1225 coin cells and are available in Tape and Reel packaging making them ideally suited to automatic placement systems.

Low profile EZ Coin Cell Holders provide a cost-effective solution to the problem of battery mounting. Coin cells are securely held in place, yet they can be quickly and easily removed when they run down.

Manufactured in phosphor bronze and tin plated, the clips employ a twin beam contact system, resulting in a mechanically strong product. EZ Coin Cell Holders is promised to enable companies to reduce manufacturing costs while achieving a very secure solution.

The product will suit most markets, with typical applications including on-board power supplies to drive memory circuits.

**www.harwin.co.uk**

## MAXIM'S DIGITAL AMBIENT-LIGHT SENSORS CUT POWER CONSUMPTION

Maxim Integrated Products is introducing the MAX44007/MAX44009 digital ambient-light sensor (ALS) ICs with a unique adaptive-gain block. Designed using the company's proprietary BiCMOS technology, these ICs integrate two optical sensors, an ADC and digital functionality into a tiny 2mm x 2mm x 0.6mm package.

The MAX44007/MAX44009 consume 100x less power than the nearest competitive product, significantly extending battery life. They offer a unique interrupt function that constantly measures the amount of light and reports to the microcontroller when the measurement passes the threshold. This functionality extends power savings by reducing the frequency of I2C communications.


In light-sensing systems, any variance along the path that the light travels results in different measurements. These variances are caused by where the sensor is placed, the distance tolerance between the top of the sensor and the glass surface, the transmission characteristics of the glass covering the sensor and others.

**www.maxim-ic.com**

## PRECISION POWER ANALYSER OFFERS INNOVATIVE MEASUREMENT FUNCTIONS

The Yokogawa WT1800 precision power analyser is the latest addition to the company's highly successful range of digital power measuring instruments.

Replacing the WT1600, an industry standard for many years, the WT1800 offers innovative measurement functions which benefit the engineer with electrical power and efficiency measurements in a range of industries from inverter and drive design to alternative energy systems.

The WT1800 is capable of performing up to six power input measurements, which makes it possible to perform efficiency tests between the input and output of products such as inverters. With its high-resolution 8.4-inch XGA display, the instrument is simple to set up and display up to 12 different pages of measurement items in formats such as numeric, waveforms and trends. A vector display is available for voltage and current phase analysis.

To measure highly distorted voltage or current waveforms with high harmonic content accurately, the WT1800 uses high-resolution 16-bit analogue-digital converters with a digitising rate of 2MS/s.

**www.tmi.yokogawa.com/ea**


EW will soon not be available through news trade, but don't miss out

## DIN 41612 CONNECTOR WITH SHELL HOUSING

Harting has expanded its range of DIN 41612 products with a new type 2C/2R crimp female connector with a shell housing.

Tested according to IEC 60603-2, the connector can be populated with up to 48 contacts. Because of its space-saving half size, the connector is ideal for use with compact PCBs or assemblies.

Special consideration has been given in the design to incorporate features that simplify the cable assembly process. The hood features three different cable entry options with predetermined breaking points, allowing them to be easily opened according to customer preference.

The locking levers are moulded into the top half of the shell housing, avoiding the need to fit separate levers. The pre-moulded design offers the additional benefit of fewer individual piece parts, thereby reducing the risk of lost components.

Secure and reliable strain relief is realised with a cable tie that fixes the cable to the shell housing.

**www.harting.com**

## VERY LOW PROFILE ILLUMINATED TACT SWITCH

Foremost Electronics announces the availability of the Marquardt 3006 series of low profile, short-travel, LED Illuminated TACT switches.

The 3006 TACT switch series offers users a superb tactile "feel" using Haptic technology. Haptics is a tactile feedback technology that takes advantage of the user's sense of touch to provide reassuring or relevant feedback on operation of the switch. Common uses of Haptics are arcade games and home games consoles and controllers, frequently taking the form of vibration or force-feedback in joysticks and controllers.

The key to the advanced design of the 3006 TACT switch family is a damped snap action disc, a mixture of switching mat and snap action disc, which allows very flat control elements with a fine tactile response and a clear user feedback signal with minimum travel. The design of the LED illumination makes backlit symbols (pictograms) visible even at night.

The 3006 series short-travel TACT switch has a very low profile at just 3.95mm while still providing a 1.1mm actuator travel.

**www.4most.co.uk**


## APACER CONSOLIDATES ITS INDUSTRIAL PATA SSD PORTFOLIO

Apacer is consolidating its offerings of PATA solutions by launching its new 2.5/1.8-inch high-speed and capacity AFD (ATA-Flash-Drives) SSDs. The SLC (Single-Layer-Cell) Flash AFD 255 comes in 2.5inch 44-pin connectors at 32 and 64GB, while the SLC 1.8inch AFD 185 supports ZIF connectors and offers a maximum capacity of 32GB.

With sequential read/write speed of up to 125/110MB/sec respectively, both can enhance computer performance and meet user's needs for highly stable and reliable storage solutions.

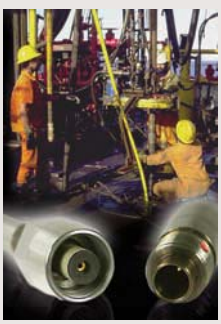
Furthermore, the SLC PATA SSD series support wide temperature range -40/+85degC. Also introduced with MLC (Multi-Level-Cell) flash, the AFD 255-M and AFD 185-M have maximum capacities of 256GB and 128GB and sequential read/write speed up to 120/90MB/sec, respectively.

Both new series feature built-in S.M.A.R.T. technology and intelligent power failure recovery function to safeguard data and enhance product stability.

**http://eu.apacer.com/business/industrial-ssd/pata/**

## NEW PERMANENT DOWN-HOLE GAUGE CONNECTOR

ITT Interconnect Solutions has announced a new Applications Note detailing the use of its new permanent downhole gauge connectors designed specifically for use in today's demanding exploration and production projects. The cost of exploration continues to rise steeply year on year as wells have to be drilled ever deeper, increasing demands on the equipment used in this challenging environment.



Maximising production efficiency is critical for cost-effectiveness and with conventional gauge connectors no longer proving robust enough, ITT ICS set out to engineer a solution – connectors and gauges that can operate at the maximum limits of metal clad cables, remaining operational at up to 200degC and up to 10,000psi pressure. The challenge was to design and manufacture a field-attachable connector with sealing that could be checked on-site before operational deployment in the well.

ITT ICS's solution was a new Permanent Downhole Gauge Connector which protects expensive gauges from damage arising from failure of metal clad cable sheathing and fits wells with small casing sizes.

**www.ittcannon.com**

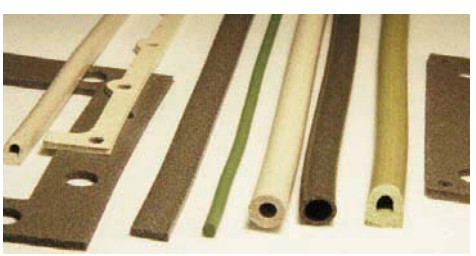
## CONDUCTIVE ELASTOMERS FOR RFI/EMI SHIELDING

Kemtron manufacture a range of conductive Elastomers as gaskets and gasket strip for emi shielding of electronic devices. The base Elastomer is silicone for normal environments and Fluorosilicone for fuel and oil resistance, both offer a wide temperature range of -40degC to +160degC and up to +200degC for some grades. The conductive fillers available are silver plated aluminium, silver plated copper, pure nickel and nickel coated graphite. Other fillers such as silver-plated nickel are available to special order.

The manufacture of a conductive Elastomer is a balance of conductive particle loading and distribution throughout the silicone base, the distribution must be sufficient to ensure that the particles are in contact with each other to ensure a good conductive path through the Elastomer.

The conductive Elastomer has a shore A hardness of between 60 and 75 depending on grade and still maintain good tensile strength.

**www.kemtron.co.uk**



## USER-PROGRAMMABLE HALL-EFFECT SWITCHES FOR AUTOMOTIVE APPLICATIONS

The A1190/2/3 family is new from Allegro MicroSystems Europe and is a range of user-programmable Hall-effect switches that complement the company's existing family of devices used in automotive seat-belt buckle, seat position and gear-shift selector applications.

These new devices incorporate enhanced high-voltage transient protection: a critical feature for automotive applications that do not allow protection circuits to be located close to the sensor.

The two-wire unipolar Hall-effect switches can be trimmed by the user to optimise magnetic switch point accuracy in the application. These devices are produced by the Allegro advanced BiCMOS wafer fabrication process, which implements a patented high-frequency 4-phase chopper-stabilisation technique. This technique achieves magnetic stability over the full operating temperature range, and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh application environments.

Two-wire unipolar switches are particularly advantageous in cost-sensitive automotive applications, because they require one less wire for operation than the more traditional open-collector output switches.

**www.allegromicro.com**

## OMICRON'S DIRANA ACCURATELY DETERMINES INSULATION MOISTURE CONTENT

DIRANA (DIelectric Response ANAlyzer) from Omicron determines in a simple and efficient way the moisture content of liquid filled transformers. Accurate knowledge of the moisture content is a crucial factor in the condition assessment of power transformers. High moisture levels accelerate insulation decomposition, decrease dielectric strength and may cause bubbles to form at elevated temperatures. Additionally, the condition (water content) of the oil is determined.

The DIRANA is also applicable to the condition assessment of bushings, instrument transformers, cables and rotating machines. Other applications include verification of proper drying for a new transformer at the factory or confirmation that the transformer is properly dried out after field assembly, repairs or oil processing.

Unique to DIRANA is the combination of the two measurement techniques: Polarization Current Measurement (PDC) and the Frequency Domain Spectroscopy (FDS). This allows for accelerated measurements, even in the very low frequency ranges which are often required for measurements on transformers that are new, cold and dry.

**www.omicron.at**

# UK GOVERNMENT ANNOUNCES SPECIFIC **PHYSICS TEACHER TARGET**

The Secretary of State for Education in the UK, Michael Gove, has asserted the need to provide a specific allocation for the training of 925 specialist physics teachers in 2011-12. In contrast to recent years, this new target for teachers in each of the three main sciences will go some way towards redressing the serious issue of too few specialist physics teachers.

Professor Peter Main, director of education and science at the Institute of Physics (IOP), said: "With physics making up one-third of the science school timetable, an ideal situation would see one-third of all science teachers having a strong physics background. At present, only 19% of science teachers are specialists in physics, leaving many students gaining their first impression of physics from biologists and chemists, who may lack confidence in the subject. In fact, more than 500 schools across England don't even have a single physics specialist on their staff."

"Our calculations show that to redress the balance between scientific subjects, we need to recruit around 1,000 new specialist physics teachers each year for 15 years."

## Our panel of commentators says the following on this development:

**PROFESSOR DR DOGAN IBRAHIM, NEAR EAST UNIVERSITY IN NICOSIA, CYPRUS:**

Physics is one of the most important fields of science and is fundamental to any engineering study. Physics should be taught by teachers trained specifically in the subject who can give confidence and motivate students taking the subject. It's been reported recently that almost one in four secondary schools in England no longer have any specialist physics teachers. The problem seems to be much greater in inner London where half of the schools do not have specialist physics teachers. The problem seems to be because more physics teachers are retiring than are being recruited and young people are not choosing to study physics. In the short-term, the solution seems to be to offer specialist physics training to those already teaching science subjects and who do not have physics qualifications. But, it is good news to hear that the Government has recognised this important problem and is investing for the training of new physics teachers.

**BURKHARD VOGEL, MANAGING DIRECTOR, GERMANY:**

I wonder why mathematics is not on the list of the important sciences that should be supported. Without maths the three sciences (physics, biology and chemistry) won't work. Besides the very good goal of increasing the amount of physics oriented teachers there should also be made every effort to improve and enlarge maths education.

It is not a single UK problem. In the EU we have to strengthen massively the respective efforts too; especially among the young female population.

**BARRY MCKEOWN, RF AND MICROWAVE ENGINEER IN THE DEFENCE INDUSTRY, AND DIRECTOR OF DATOD LTD, UK:**

It is my understanding that it is the Financial Services industry which has siphoned up large numbers of the physics graduates for their analytical reasoning abilities. But this target should be achievable in the current economic climate so the issue thereafter shall be one of retention. However, dedicated physics teachers are essential to motivate pupils, especially when they are considering making their subject choices between the harder science and mathematics subjects rather than opting for the softer 'waffle' subjects such as politics and economics, particularly as pupils know which teachers they wish to study with and can be motivated by.

**IVOR CATT, ENGINEER AND SCIENTIST, UK:**

It is most important to try to ensure that physics, being such a brittle subject, is taught by those with competence in physics rather than in the softer subjects of chemistry and biology. However, the problem can go deeper. Many years ago, when I was drawn into teaching because of the desperate shortage of maths and physics teachers, I found myself teaching biology most of the time, in which I was incompetent. Having been brought up in Cape Town, I did not know the most obvious English flora.

**HAFIDH MECHERGUI, ASSOCIATE PROFESSOR IN ELECTRICAL ENGINEERING AT THE UNIVERSITY OF TUNISIA:**

The British government's idea to train professors in physics is founded on the current need to present knowledge for the profit of the whole community.

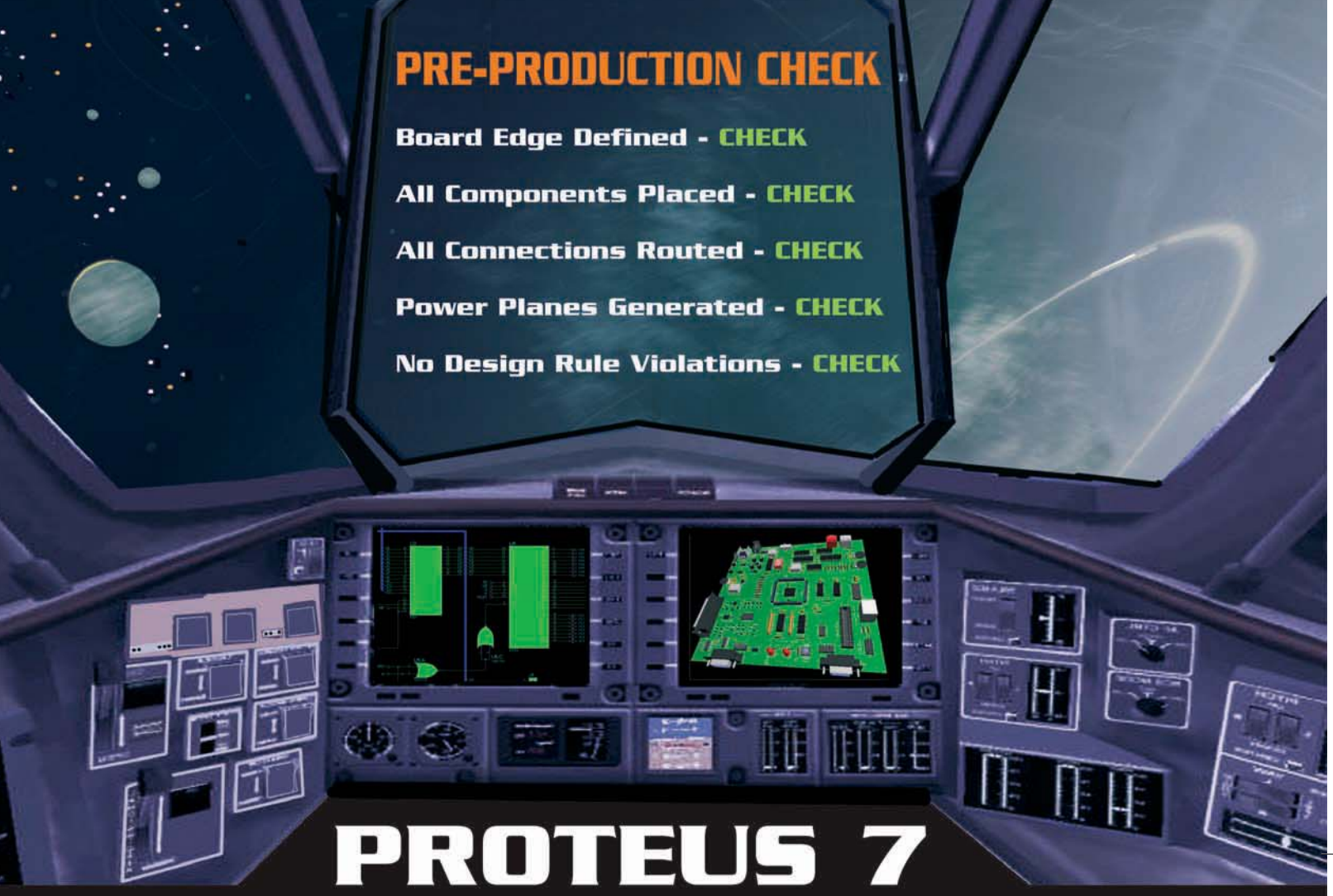
Physics covers a very wide field of theoretical and practical subjects in modern technology. Thus to create the foundations of best knowledge it is necessary to have specialist teachers capable to manage and transmit the fundamental theories that can also easily correlate to the other fields of science. Let's not forget that the fundamental theories of physics are the basics of the great scientific innovations.

I think that this broadness of outlook is extremely significant for the country scientists.

**MAURIZIO DI PAOLO EMILIO, TELECOMMUNICATIONS ENGINEER, INFN – LABORATORI NAZIONALI DEL GRAN SASSO, ITALY:**

Since all three scientific disciplines are taught in schools, one might expect that one third of all science teachers should be physics teachers. School students should not be getting their first taste of physics from a biology graduate who last studied the subject at the same age as them. Physics is a strategically important subject that underpins much of engineering and other science subjects. If it is not introduced to youngsters by well-versed, confident and inspiring teachers, enormous potential will be wasted. Much more could and should be done to entice a greater number of physics graduates into teaching.

*If you'd like to comment on this subject or want to become a member of our panel, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com*

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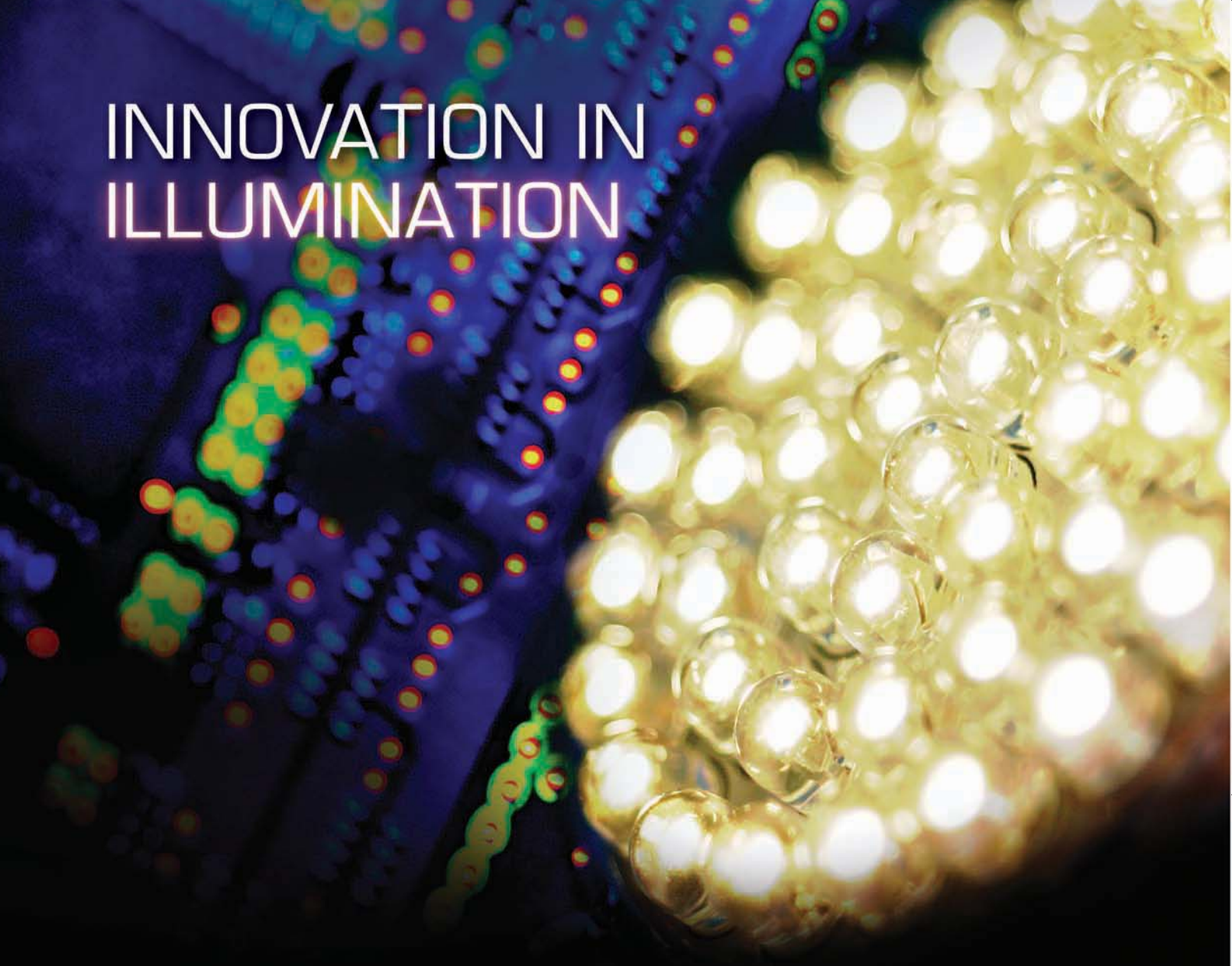


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