

July 2011
Volume 117
Issue 1903
£4.60

Electronics WORLD

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Embedded Platform Concept

Meeting the increasing
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Technology

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Focus

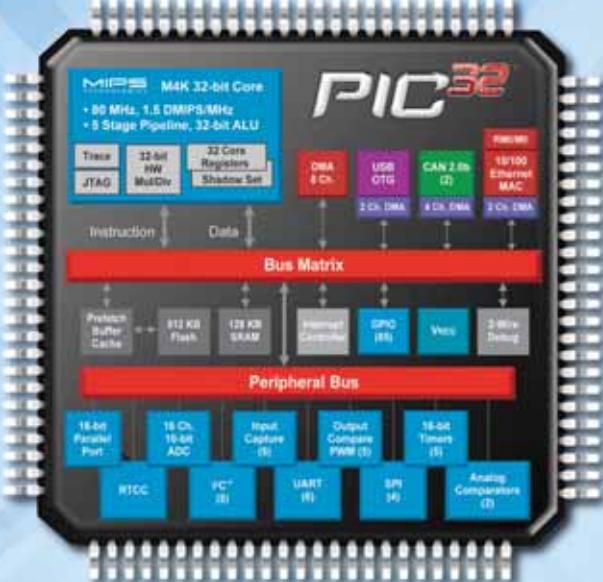
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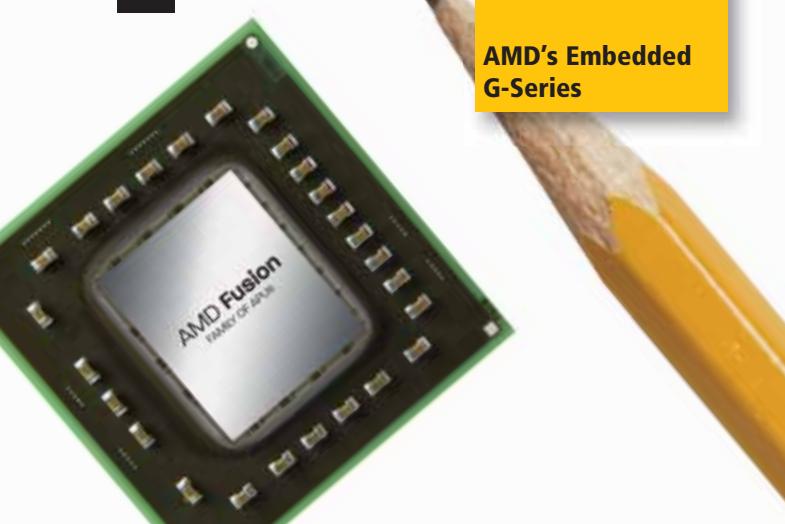
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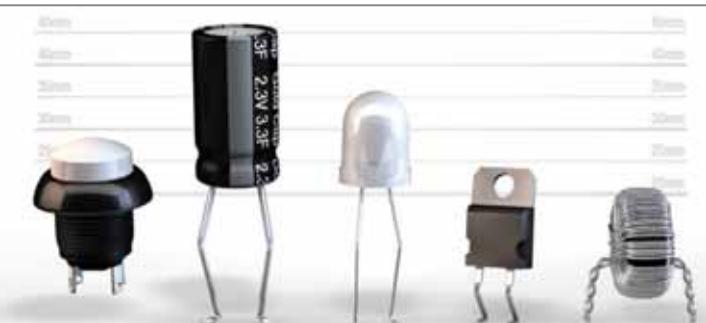
THE ELECTRONICS BEHIND LIGHTING – PART 2

I.Hakki Cavdar prepares this five-part series on lighting electronics – the fundamentals, the topologies and the types of ballast circuits used. This second part details the main converter structures used in lighting electronics

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Assembled Order Code: AS3166v2 - £33.95



Controls the speed of most common DC motors (rated up to 32Vdc, 10A) in both the forward and reverse direction. The range of control is from fully OFF to fully ON in both directions. The direction and speed are controlled using a single potentiometer. Screw terminal block for connections.

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Control the speed of almost any common DC motor rated up to 100V/7.5A. Pulse width modulation output for maximum motor torque at all speeds. Supply: 5-15Vdc. Box supplied. Dimensions (mm): 60Wx100Lx60H. Kit Order Code: 3067KT - £19.95
Assembled Order Code: AS3067 - £27.95



Control the speed of almost any common DC motor rated up to 100V/7.5A. Pulse width modulation output for maximum motor torque at all speeds. Supply: 5-15Vdc. Box supplied. Dimensions (mm): 60Wx100Lx60H.

Kit Order Code: 3067KT - £19.95
Assembled Order Code: AS3067 - £27.95

Most items are available in kit form (KT suffix) or assembled and ready for use (AS prefix).

Controllers & Loggers

Here are just a few of the controller and data acquisition and control units we have. See website for full details. Suitable PSU for all units: Order Code PSU445 £7.95

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Assembled Order Code: AS3180 - £64.95

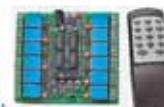
DTMF Telephone Relay Switcher

Call your phone number using a DTMF phone from anywhere in the world and remotely turn on/off any of the 4 relays as desired. User settable Security Password, Anti-Tamper, Rings to Answer, Auto Hang-up and Lockout. Includes plastic case. Not BT approved. 130x110x30mm. Power: 12Vdc. Kit Order Code: 3140KT - £79.95
Assembled Order Code: AS3140 - £94.95

Assembled Order Code: AS3140 - £94.95

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Assembled Order Code: AS3149E - £59.95



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USB PIC programmer for a wide range of Flash & OTP devices - see website for details. Free Windows Software. ZIF Socket and USB lead not included. Supply: 16-18Vdc. Assembled Order Code: AS3150 - £49.95

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JDSU ANNOUNCES TOP TECH TRENDS FOR 2011

JDSU announced 2011 technology trends for the markets it serves, from the emergence of 4G to advancements in gesture recognition and clean energy solutions. These include:

MOBILITY GETS FITTER AND FASTER TO SUPPORT NEW APPLICATIONS

The smart phone boom and resulting migration to faster and higher-performing wireless networks will continue to be a big focus as mobile traffic grows dramatically in 2011.

"As new wireless network architectures emerge, expect them to better support demanding applications such as mobile video blogging, advanced games and professional services," said Jay Stewart, director of Ethernet Service Assurance at JDSU.

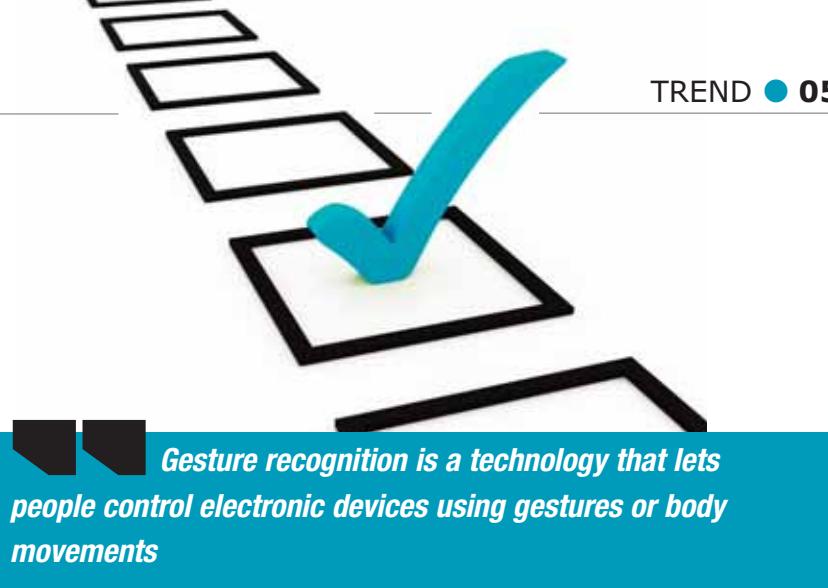
ONLINE VIDEO PUSHES THE INTERNET TO BECOME MORE SELF-AWARE

The Internet will continue to grow as a key utility in people's lives in 2011 with millions of people expected to watch full-length TV episodes and movies online, consuming a large portion of bandwidth during peak viewing hours.

"As fast as engineers can create on-demand applications, people are adopting them," said Sinclair Vass, senior marketing director of Communications and Commercial Optical Products at JDSU.

GESTURE RECOGNITION TECHNOLOGY MOVES BEYOND GAMING

Gesture recognition is a technology that lets people control electronic devices using gestures or body



Gesture recognition is a technology that lets people control electronic devices using gestures or body movements

movements. It made a big debut in 2010, in gaming, but has since been picked by various companies and collaborations for new uses to help people use technology in a more natural way.

"Picture relaxing on your couch and waving your hand to select a movie, order a pizza, or take a video call from your TV without having to fumble for a remote," said Andre Wong, product manager at JDSU. "Or imagine typing or surfing the web using hand movements in the air on a virtual keyboard projected from your smart phone – the possibilities are exciting."

CLEAN ENERGY MARKET LEVERAGES NEW CPV TECHNOLOGY FOR SOLAR

In 2011, countries will further invest and implement clean energy solutions using new approaches, such as concentrated photovoltaic (CPV) technology to efficiently convert sunlight into electricity within solar panels.

"More systems integrators will deploy CPV technology over the next few years, as companies like JDSU produce concentrator chips in mass volumes that will drive lower costs, which is the key to widespread implementation of solar," said Jan-Gustav Werthen, director of CPV technology at JDSU.

AUTHENTICATION TECHNOLOGY AIDS IN THE FIGHT AGAINST COUNTERFEITING

In the coming year, counterfeiters will increasingly target a wide range of

products for criminal activity, including pharmaceuticals, automotive parts, designer clothing, electronics and software. To fight this threat, brand owners will turn to integrated solutions that combine optical, stealth and digital technology to authenticate products.

"Brand owners and consumers are very concerned about the financial, liability and safety threats posed by counterfeiting," said Scott Magnacca, sales director of Authentication Solutions at JDSU.

COLOUR HELPS TO SELL PRODUCTS

Every year, JDSU publishes an annual colour trends report and provides pigments to help brand owners and designers better differentiate products through the use of popular colours. Colour trends for 2011 include blue replacing green as the colour that represents the environment, white signifying technology and yellow and pink signaling hope and optimism as the economy recovers.

"Colour plays an important role in the buying process and many consumers are willing to pay extra for a desired colour on products such as cars or electronics," said John Book, product manager of Custom Colour Solutions at JDSU.

A supporting video highlighting the trends picked by JDSU is also available at <http://www.jdsu.tv/techtrends>.

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SUBSCRIPTIONS:
Saint John Patrick Publishers
PO Box 6009,
Thatcham,
Berkshire, RG19 4QB

Tel: 01635 879361 Fax: 01635 868594
Email: electronicsworld@circdata.com

SUBSCRIPTION RATES:
1 year: £46 (UK); £67.50 (worldwide)
MISSING ISSUES:
Email: electronicsworld@circdata.com

PRINTER: Pensord Magazines & Periodicals, Pontllanfraith, UK.

ISSN: 1365-4675

 John Patrick Publishers

SKiN technology uses flexible foil and sintered connections rather than bond wires, solders and thermal paste

NEW PACKAGING TECHNOLOGY DOUBLES CURRENT DENSITY IN POWER SEMICONDUCTORS

flexible foil and sintered connections. Current density is doubled to $3\text{A}/\text{cm}^2$ compared with the typical $1.5\text{A}/\text{cm}^2$ achievable with

Wire bonding has been the main method of connecting the chip top-side connection to a Direct-Bonded Copper (DBC) substrate for the past 25 years. However, wire bonding cannot meet the need for higher current densities that has resulted from recent technical

advances, which means that reliability is being impaired.

In the new packaging, a sintered foil replaces the wire bonding on the chips and the underside of the chip is sintered to the DBC. As sintered layers have a lower thermal resistance than

solder equivalents, this results in optimum thermal and electrical chip connection. The sintered foil connects the chip across its entire surface, whereas bond wires connect the chips at the contact points only.

The new packaging technology has a high load-cycle capability offered which allows for higher operating temperatures, which will prove necessary as the move towards new materials, such as SiC and GaN, will increase the need for these elevated temperatures.

Semikron has developed a revolutionary packaging technology for power semiconductors, which removes the need for bond wires, solders and thermal paste.

The new SKiN technology is based on the use of a

standard wire bond technology. Converter volume can therefore be reduced by 35%. This results in a higher current-carrying capacity and ten times the load cycle capability – unthinkable with the wire bonding used in power electronics in the past.

Viewing Devices Nondestructively in 60-Micron Slices

US maker of acoustic micro imaging systems, Sonoscan, has demonstrated the single-scan imaging of a sample at 50 different depths, or gates. The technique, called PolyGate, yields 50 images that show internal features at each depth.

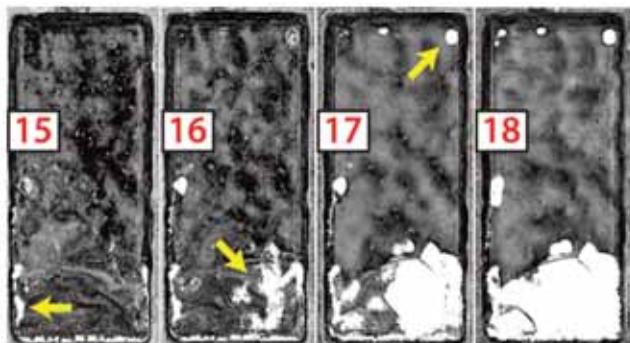
In conventional imaging, much wider gates are used to confine imaging to a single depth of interest such as the die face or lead frame depth. The ability to set multiple gates that are imaged simultaneously

during a single scan gives the system user the ability to see internal features at each gate and to see how features, including defects, change from one gate to the next.

Shown in the image on the left are gates 15 through 18 (out of 50) imaging downward from the top surface of a ceramic chip capacitor that is 3.18mm thick. Each gate is about 60 microns thick. PolyGate can set up to 200 gates, and Sonoscan has

demonstrated 5-micron gates in some materials.

The bright white regions in the acoustic image are defects. Small edge delaminations exist at Gate 15, but at Gate 16 a larger defective area appears in the lower right. In Gate 17 this area blossoms into a large delamination or void, and small voids appear at the top. The abruptness with which the large feature appears in Gates 17 and 18 suggests that the feature is very flat.



Depths 15 to 18 (of 50 depths) in a ceramic chip capacitor that is 3.18mm thick, imaged acoustically and simultaneously with Sonoscan's automated multi-gate system. Each gate is about 60 microns thick

NEWS IN BRIEF

■ Freescale Semiconductor has announced the Make It Challenge design contest, which is set to take place at the Freescale Technology Forum (FTF) on June 20-23 in San Antonio, Texas. The contest will challenge attendees to develop and submit a unique sensor robotic or system design based on Freescale's latest sensor development kit in the form of a walking robot or the Freescale Tower System. Freescale will also show its nine-inch tall, bipedal walking Mechatronic robot, with a 32-bit 'brain' and a three-axis accelerometer for balance.

■ SparkFun Electronics of the US, specializing in helping electronic enthusiasts get the parts and resources they need, is announcing a new department – the Department of Education.

The firm has always focused on providing extensive online resources, as well as offering a variety of in-house workshops and events. The recent development of a new Department of Education emphasizes its passion and commitment to providing individuals with the tools they need to explore the world of embedded electronics. "Our primary goal is to make electronics education exciting, accessible and affordable," said Lindsay Levkoff, Head of the department.

Ready, set, change!

It's been called the box that changed the world and yet the industry that transformed the face of global trade and transport in the space of just 50 years now stands on the brink of another era-defining moment: whether to continue with entrenched habits, or rediscover its desire and capacity for innovation and change.

Our industry and our customers benefit every day from the time, effort, money and sheer belief in the future that went into building the global container transport system as we know it today. When containers came along, we had to change everything and we believe the time has come to make that change again.

Maersk Line has identified three key challenges that we believe the whole container shipping industry must now address to ensure that it has a prosperous future: on-time delivery, ease of business and environmental performance.

We want to start the debate that will redefine our future and help us add tremendous new value to our customers' supply chains worldwide. We have to become an integrated part of our customers' promise to their customers to act as responsibly as possible in the marketplace. But why wait to be asked? Why not lead the way?

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EFFICIENT Software Embedding



ARROW ELECTRONICS

For many years, software development for embedded systems has been gaining increasingly in importance. While the first microcontrollers were initially used from the 1970s onwards to replace complex circuits made up of discrete logic gates, they have long since become a permanent fixture in all manner of electronic equipment. Through the integration of increasingly complex peripheral functions and the continuing rapid growth in the number of microcontroller ranges available that are based on many different processor architectures, a suitable microcontroller can now be used for virtually every application in order to ensure the most compact and efficient implementation possible.

As a replacement for logic, the microcontroller only required a little program code at first, which initially was generally programmed directly in the relevant assembler command set. Since then, however, due to the constantly growing flexibility, functionality and clock frequency, the proportion of other mechanisms defined by software has also increased drastically in all applications. On the one hand, free programmability has enabled greater differentiation between competitor products, while on the other there is an increasing expectation to see in embedded systems the established standard interfaces for communication and user interaction used in the field of consumer electronics. Whereas

back in the early days these included RS232, RS485, LEDs and 7-segment displays, some buttons and - as mass storage in special cases - floppy disk or tape drives, today USB, Ethernet, graphic displays with touch screens and Flash memory cards are practically indispensable. To these must be added the most important wireless standards: Bluetooth, ZigBee and WLAN.

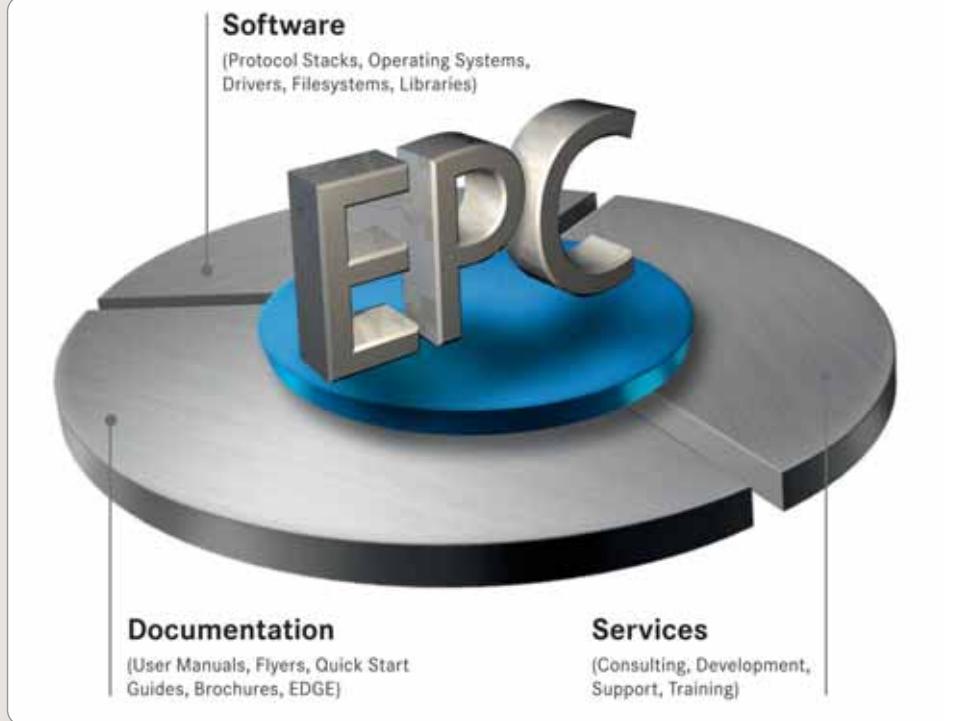
In contrast to the early interfaces that are now commonly referred to as legacy interfaces, software libraries are used for all modern interfaces; these are usually created in ANSI-C for maintenance and portability purposes. These libraries provide communication protocols, server services, file systems, character sets, graphics functions, filter and error correction algorithms and

many more mechanisms. As recently as ten years ago, it was often the aim to develop a custom software library when using one of the modern interfaces for the first time. In most cases this decision was driven by the desire to be able to master the relevant technology yourself - this had been common practice in the past and became standard over the years.

INCREASING REQUIREMENTS FOR INTERFACE FLEXIBILITY

Over the past decade, however, the situation has fundamentally changed: The stellar success of notebooks, smartphones and tablets has meant a rapid growth in market pressure for a wide range of new interfaces. At the same time, powerful microcontrollers with 32-bit processor cores and a wide range of integrated interfaces from various semiconductor manufacturers have become available at very attractive prices. Today, Ethernet and USB can be implemented even in simple and inexpensive devices, and to deprive the end customer of these options represents a significant risk with regard to competitive edge. As soon as more complex computing and/or time-critical mechanisms are required, this is the point where in many applications it also becomes necessary to use an operating system for the first time. Due to the global competitive situation, even in the industrial sector product cycles are shorter, and distinguishing features have become more important than ever before. In this environment it is often no longer justifiable to use any of your own development resources beyond those of your core competences when it comes to developing complex standard mechanisms. You simply have to source these elsewhere.

However, aside from deciding between internal development and external solutions, there are other factors to consider. Should all



required mechanisms be integrated in the form of individual, special libraries, or is an operating system which contains all the necessary functions preferable? Can open source solutions be used - indeed, must they be - or will the supplier of a commercial software product have to provide a warranty and support? What are the resulting requirements of these options in terms of the properties of the processor system, and what amount of work will be required for integration, adaptation and optimisation? How can the various solutions available on the market or the different licence models actually be compared with one another so that the chosen product is at least suitable from both a technical and commercial point of view and, where possible, is indeed more or less the ideal choice?

CHOOSING THE RIGHT SOFTWARE

The experience needed to answer these questions is in many cases still lacking in-house, which means that external support is also helpful here. In addition, the aim is often to evaluate various approaches, which can result in a huge amount of work. The following basic guidelines can help to avoid unnecessary risks and excessive evaluation work:

- Purchasing a professional software package is always cheaper than implementing the same functionality yourself.
- In many cases, particularly for standardised protocol stacks and file system drivers, there is hardly any advantage to be had in mastering the corresponding technologies down to the last detail. On the contrary, this specialist knowledge is soon forgotten or can only be kept partly up-to-date through continuous investment.
- When comparing open source solutions with commercial packages, you should always try to base the comparison on an assessment of the total cost of ownership. In such an assessment, and depending on the requirements of the relevant application, the following should also be taken into consideration: the support, training and development services on offer; the performance and efficiency of implementation; typical update mechanisms; the warranty offered; resulting hardware requirements; the scope of available software functionality; software security; and the amount of programming and test work in series production, amongst other factors.
- All serious suppliers will usually provide support for software evaluation. This may

be anything from a demo application that runs on standard hardware to an evaluation license enabling you to access the source code. In this way it should be possible for a potential user to research the functionality and performance of the product.

- Embedded software products are often offered in relation to reference hardware. Together with this reference hardware, all product features are guaranteed as present in the purchase contract or the terms of licence. This procedure helps to differentiate between errors resulting from using the product (user errors) and defects in the product itself (bugs) and to decide on the most efficient measures to eliminate the malfunction.
- Before making a purchasing decision, the range of services offered by the supplier or their service partner can be utilised on a trial basis. Here training or a workshop is offered, or even a feasibility study or test adaptation of a demo application to the requirements of the target application.
- Even without a service contract a software supplier should at least offer in-depth technical consultation, if only to determine the functions, protocols and products required. In special cases this consultation may be very complex and warrant a clearly defined service contract. If only an "all-round comprehensive package" is offered, you should at the very least question whether a tailored package might not be more efficient for the specific application in question.
- The discussion of possible problems or hurdles when using software resources for a special application should be included in the consultation. Challenges are always encountered in any embedded application with complex software architecture. If the software supplier underplays or is tight-lipped about these points, be very suspicious!
- Physical proximity to the software supplier is often a real advantage, but must not be overvalued. It certainly is an important element to consider if you are also reliant on the services of the supplier.

● The experiences of other market players with the relevant software products can also contribute valuable information to the decision-making process. Naturally this will involve other customers, but semiconductor manufacturers, distributors or module manufacturers can also be asked for recommendations and even critical reviews.

In order to provide the most helpful recommendations for software resources, and as part of its Embedded Platform Concept (EPC), Arrow has formed a partner network of suppliers of embedded software solutions. The software solutions of all these partners can be easily tried out on EPC hardware and compared with alternative solutions. Successful projects for Arrow customers have already been implemented with all EPC partners. The resulting findings can be used at any time in an open discussion based on the relevant product requirements in order to ensure the evaluation work and the development risk involved are minimised on a permanent basis. Customers' own software developers are thus safe in the knowledge they can concentrate primarily on their core competences, thereby ensuring best possible differentiation from their competitors.

In addition to assistance in the area of embedded software, the Embedded Platform Concept from Arrow also includes many resources covering hardware, services, training and IP. EPC hardware comprises a modular kit system, which covers the function areas of processor systems, power management and interfaces, and seamlessly integrates the EPC software and IP resources. For all EPC resources, workshops and seminars are offered on an ongoing basis in association with partner companies; these can also be tailored to special applications or market requirements on request. As a supplement to the Embedded Platform Concept when used as a development support tool, the software, module and display solutions of the Embedded Solutions segment at Arrow can be integrated in order to further optimise development work. ●

ABOUT ARROW

THE LOCAL SALES CONTACTS CAN BE CONTACTED IN RELATION TO ANY QUERIES REGARDING ARROW'S EMBEDDED PLATFORM CONCEPT.

In particular, application engineers are kept up-to-date with new information and can access those EPC specialists directly who worked closely on the development and integration of all EPC functions. Contact can similarly be established with representatives from all EPC partner companies or an individual EPC workshop can be planned.

Implications for employers of the abolition of the default retirement age

DAVID REGAN TACKLES THE QUESTION OF HOW TO DEAL WITH OLDER MEMBERS OF STAFF, PARTICULARLY THOSE WHO HAVE WORKED FOR A BUSINESS FOR A LONG TIME

The question of how to deal with older members of staff, particularly those who have worked for a business for a long time, is a difficult one for managers. At present, employers must follow a fairly strict retirement process which penalises them for failing to comply, but which does allow them to choose to retire an employee without the employee having any say in the matter. With effect from 6th April 2011, this process has started to fall away and, from 1st October 2011, it will be age discrimination to dismiss someone by reason of retirement.

Difficulties Following the Abolishment of the DRA ***Succession planning***

The most obvious difficulty for employers will be that there is no longer a ready-made timetable for retirement, meaning the path to senior positions could be blocked. Employers may also feel unable to ask when an employee is intending to retire, leading to 'shock' retirements that leave the employer without a proven successor.

Employee Relations

Employers may also find it difficult to start discussions about retirement with employees as detailed above. Even if they do, many employees may not take kindly to the idea that they should retire if they are not ready to do so. In addition, under the 'old' law, employees have often been allowed to continue to retirement with



The abolition of the default retirement age has the potential to have a large impact on businesses, as staff may choose to remain in their position longer

managers overlooking lapses in judgment or incremental changes in performance, which can be attributed to an employee's age. Moving forward, employers will be faced with the unpleasant task of performance managing longstanding, cherished employees if they are not up to task rather than allowing them to continue with the knowledge that retirement is just around the corner.

With effect from 6th April 2011, this process has started to fall away and, from 1st October 2011, it will be age discrimination to dismiss someone by reason of retirement

What is a 'Legitimate Aim'?

Cases under the 'old law' have found legitimate aims to be workforce planning, enabling recruitment and retention of younger employees, avoiding adverse impact on pensions and benefits, ensuring continued competence and having an age balanced workforce ensuring job opportunities amongst the generations. However, employers will need to be careful when implementing a normal retirement age and will need to show that they have balanced the employee's rights and dignity against the needs of the business.

Flexible Working

In practice some employers may be



happy to allow an employee to continue working as long as they choose, and many employees will most likely want to at least reduce their hours, if not finish working completely, as they age. It is important to note that the abolition of the default retirement age has no effect upon the flexible working law which is currently in place, and employers will not be under a duty to allow older employees to work reduced hours unless they are eligible for flexible working in the usual way.

Performance Management

In addition to the employee relations issues highlighted above, managers must

ensure that performance management processes are implemented fairly across the entire range of employees in order to avoid any accusations of age bias, or trying to force out the older members of staff. In addition, managers will need to watch for age related disabilities and, if any disability is found, will need to consider whether or not any reasonable adjustments may need to be made in relation to the employee and their employment.

Exceptions

There are two exceptions to the abolition of the default retirement age:

1. It does not affect occupational pension schemes and the setting of a "normal retirement age" for the purposes of occupational pension schemes.
2. Employers may withdraw benefits for employees at or over the age of 65 (with the age at which withdrawal will be legal rising in accordance with the state pension age). This exemption deals with a key concern of employers, namely that the rising costs of benefits and insurance for employees over the state pension age could make the provision of these benefits prohibitively expensive.

Confusion Over Last Date for Retirement

As stated earlier, the last date on which a

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ALTERNATIVES TO THE DEFAULT RETIREMENT AGE

Employers are still free to choose to set a retiring age for their business, provided that they are able to justify this

notice of intended retirement date can be issued is 5th April 2011 – provided the employee has reached 65, or the relevant normal retirement age by that date. Any such notice can be for up to 12 months. An employee can then ask for an extension to that notice, which can be for up to six months; any longer extension would require a new notice of intended retirement to be issued, and one cannot be issued post 5th April 2011.

Some debate has arisen amongst employment lawyers as to the correct dates for these matters. On strict interpretation, if notice is given on 5th April 2011, it would start with effect from 6th April 2011 and would then expire on 5th April 2012. Any extension would be for six months from this point. The question that is open for interpretation is whether or not the extension is for an additional six months from this point, so ends on 4th October 2012, or whether the extension takes effect the day after the expiry of the original 12 month period, and then ends on 5th October 2012.

1. SPEAK TO THE EMPLOYEE 'OFF THE RECORD':

Whilst this option is tempting, trying to speak with an employee 'off the record' is fraught with difficulty. In brief, simply saying "this conversation is 'off the record', or 'without prejudice'", does not mean that the employee cannot use the conversation against the employer. Therefore, an employee could argue that these discussions are an attempt to force them out on the grounds of their age, and consequently sue for age discrimination.

2. SPEAK TO THE EMPLOYEE 'ON THE RECORD':

The best time to do this is during annual appraisals, or at regular meetings. Indeed, it may make sense for employers to discuss future plans with all employees at appraisal time, as this will give the employer a better idea of who is looking for advancement, who is happy within their role, who is considering retiring, and plan accordingly.

3. KEEP A CLOSE EYE ON PERFORMANCE:

Many employers are concerned that the change in law means that they will be stuck with staff members who cannot perform and who cannot be retired. This is not the case. In fact, under the new law, employers will have to keep a closer eye on who is performing well and manage all employees' performance equally, regardless of age or length of service.

4. SET A CORPORATE 'NORMAL RETIRING AGE':

Contrary to popular belief, employers will still be able to set a 'normal retiring age' for employees. Although this will be age discrimination, this will be justifiable if the decision can be shown to be a proportionate means of achieving a legitimate aim.

There is also some debate about whether the original notice has to be given with effect from 5th April 2011, or has to start on 5th April 2011, in which case the question would be whether or not the last date for retirement could be 3rd or 4th October.

The Department for Business, Innovation and Skills holds the view that 5th October 2012 is the last date upon which any notice (with an additional extension) could take effect, and this

view, taking the strict legal interpretation into account, makes the most sense. However, it is worth noting that there are competing views out there. Hopefully definitive guidance will be published prior to the Regulations coming into force.

Impact on Businesses

The abolition of the default retirement age has the potential to have a large impact on businesses, as staff may choose to remain in their position longer, hindering succession planning, and employers and managers will be forced in many cases to invoke disciplinary procedures to manage the performance of longstanding employees, with a subsequent negative effect on morale.

However, where there is clear ongoing dialogue between managers and staff, and all parties are open to sensible communication, there is no reason why employees continuing to work past the current default retirement age should prove to be a problem. Indeed, managers may find that retaining the services of a valued, longstanding employee for a reduced number of hours during the working week may allow more junior members of staff to learn from someone who would otherwise previously have retired and to gradually take over their role as they ease towards the date at which they intend to retire.

In addition, employers are still free to choose to set a retiring age for their business, provided that they are able to justify this. ●

THE KEY CHANGES TO THE LAW ON RETIREMENT ARE AS FOLLOWS:

- Notices of intended retirement date cannot be issued from 6th April 2011 onwards.
- The default retirement age will be abolished with effect from 6th April 2011, although compulsory retirement will still be permitted in certain circumstances until 5th April 2012.
- Employees will be able to request to carry on working using the current statutory procedure until 4th January 2012.
- Any extensions as a result of such request must be less than six months and therefore must expire on 5th October 2012 at the latest (although there is some discussion about this date, see below).

What Does This Mean for Employers

Notices of intended retirement can now only be issued for employees who are 65 or over (or will attain the company's default retirement age, if different from 65) on or before 30 September 2011, and the notice of intended retirement date for that employee must be issued no later than 5 April 2011.

The notice given can be up to 12 months, so can take effect up to 5th April 2012. Employees can then make a further request to carry on working provided that this is submitted no later than 4th January 2012. If a new retirement date is set as a result of this request, it must expire no later than 6 months following the previous intended retirement date if it is not to be discriminatory under s.13 of the Equality Act 2010 (although the defence of objective justification will still apply).

CHANGES TO RETIREMENT

PREMIER FARNELL'S WAVE OF INNOVATION CONTINUES with the launch of the element14 knode

the world's first interactive design automation hub

Last month in line with the Group's focus on providing engineering design solutions, driving business to the web and growth in emerging markets, Premier Farnell plc (LSE:pfl), announced the launch of the element14 knode, a revolutionary online design platform that is exclusively focused on the needs of electronic design engineers.

In the course of creating electronic products, design engineers visit multiple sites to gather relevant technical information and to begin assembling the correct hardware and software solutions for their design.

The element14 knode is unique in providing a single on-line platform for performing all of these activities. Based on an engineer's initial specification it automates the creation of explicit dependencies and inter-relationships with other system level components to quickly build a custom design flow - whether it be development kits, design tools, operating systems and stacks, Intellectual Property or services such as PCB design and manufacture. These have all been integrated into one convenient place: the element14 knode – KNOWledge for Design Engineers.

"The element14 knode offers a world of solutions in one single interface and is another exciting industry first for us offering a new and different approach to design solutions. Innovation is vital for design engineers and as their partner in innovation, we are re-defining the delivery of the solutions they need," commented Harriet Green, CEO of Premier Farnell.

The services offered in the element14 knode v1.0 release include:

- search automation and configuration for project specific design flows
- development platforms and kits
- operating systems and stacks
- development and CAD tools
- PCB services; and test solutions
- an online 'Learning Centre'

THE ELEMENT14 KNODE – AN OVERVIEW

SEARCH LIKE NEVER BEFORE

An engineering-focused alternative to standard search engines, the knode search function helps engineers find relevant design

information and the latest technology quicker than ever before. Designers can use the element14 knode to quickly research, evaluate and purchase solutions, software and services. The availability of reliable technical information and solutions can save the designer hundreds of hours typically spent in searching and validating information. Further, the innovative search engine returns all relevant and related contents for the search performed – in one click. The search bar allows users to enter keywords by supplier, architecture or part number, while Search results can also be refined using categories and tag filters such as core architecture and silicon manufacturers.

EXPERT LEARNING CENTRE

The element14 knode Learning Centre provides a library of rich content to help a user research various technologies, platforms and associated core components. This includes "How To" videos, application notes, technical documentation and much more. Forums host discussions in areas ranging from product/technology and applications to design recommendations, and technical support and designers can post questions to subject matter experts from element14's enhanced technical support team and from suppliers across a number of industries and design environments.

DEVELOPMENT PLATFORMS AND KITS

A wide variety of development platforms and kits are available including:

- Pre-built boards to test the latest technology and protocols
- Hardware solutions to accelerate the design process
- Search for instant prototypes for embedded systems
- New technology and industry exclusives such as the Freescale™ XL Starboard



OPERATING SYSTEMS AND STACKS

Access Operating Systems, RTOS, Stacks and middleware for application software execution and interoperability.

DEVELOPMENT TOOLS

The element14 knode provides access to a comprehensive suite of software development tools for embedded systems: These include Integrated Development Environments (IDEs), compilers and debuggers and the latest software design solutions from leading technology providers.

CAD TOOLS

Through the knode, PCB design tools are available that enable designers to develop PCBs within a highly productive, scalable and easy-to-use environment. Solutions cover the spectrum of PCB development, from schematic entry to manufacturing. PCB Tools include the award winning CadSoft EAGLE. This powerful and easy to use PCB software offers high-end functionality in a schematic editor, layout editor, and autorouter.

PCB SERVICES

The element14 knode delivers high quality, low risk solutions for PCB fabrication and assembly in partnership with industry leaders. element14's partners not only provide rapid turn-around manufacturing using advanced technology and the application of state-of-the art design for manufacture (DFM) and test software, but they also deliver fabrication services at globally-competitive, affordable prices.

TEST EQUIPMENT

The element14 knode offers leading hardware analysis solutions for embedded systems or prototypes including oscilloscopes, multi-meters, signal generators and more.●



Wireless networks:

Another look from a different perspective

MYK DORMER IS SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
WWW.RADIOMETRIX.COM

If the low power radio marketplace has a favorite phrase, to be misused, misunderstood and over-sold throughout the sector, then that phrase must be “wireless network”. Whenever more than two radios are communicating, it seems that the result gets described as a “network”, and all sorts of buzzwords and (expensive) proprietary architectures get trotted out, promising almost magical guarantees of success.

But what is even meant by a “wireless network”?

I suggest we look at this subject from first principles: The simplest possible data communication system will be a link between two radios. Information is coded to produce a viable baseband signal, which is then modulated onto an RF carrier, transmitted between the radios and, at the receive end, demodulated and decoded to recover the original data. The information can be a continuous data stream but (more practically) it is likely to consist of discrete “packets” of data, including synchronization sequences, error handling codes, such as checksums, and often “address” information (to discriminate between co-sited systems, or to select a specific recipient unit).

Multiple receivers can recover the signal from a single master transmitter

(simultaneously in a “broadcast” arrangement, or selectively in an addressed “star” configuration), or multiple transmitters can (at different times) send to a single receiver. If transceivers are used, then a master can acquire data from any one of a number of slave units by sending a request message, and then listening for a reply (a ‘polled’ system) or by sending a synchronising message and allowing the slave units to reply in time-sequence order (a ‘beacon synchronised’ system), but in all these cases the basic topology is the same, in that the information passes once over a single radio link.

These simple “single hop” systems are still sometimes referred to as “networks”, but this can be misleading. It is more meaningful to use the term “network” to discriminate between these point-to-point (or star) systems and the next level of sophistication.

A point to point link is necessarily limited by the range of the radio link hardware used; in any given situation, there will be absolute limits to the range of the basic radio link, either regulatory limits on aerial type and transmitter power, or simple physical or financial restrictions. To exceed this, either to increase the linear range, or improve coverage in complicated terrain, it is necessary to use multiple links.

This introduces the idea of a “repeater”,

an intermediate unit which receives the signal and re-sends it, potentially doubling the range. To gain additional increments, further repeaters can be added, each responding to the signal from the previous one, in a long chain. The data packet passes down the chain of repeaters in a sort of electronic “Mexican wave”.

In our example a repeater consists of a receiver, sufficient memory to store a complete packet and a transmitter. Strictly speaking I am dealing here with a specific sub-type of repeater, known as a “store and forward” repeater, but this is the type most applicable to low power wireless data operation. “Transmit through” repeaters also exist, where the transmitter takes the receiver baseband and resends it in real-time, either on a different frequency or by the use of highly directional aerials. Amateur radio service voice repeaters are usually of this type, as are some microwave link regenerators.

A further sophistication that can be added to our hypothetical network is the facility for any of the devices to operate as repeaters, in addition to their primary function – rather than limiting the design to dedicated masters, slaves and repeaters. This concept of a more generalised network “node” is central to the “mesh network” architectures currently popular in low power radio circles, but does not really change our discussion, since nodes operating as repeaters and dedicated repeater units are functionally interchangeable.

Adding repeater(s) to a simple point to point link introduces a new layer of complexities: **Network delays** (or maybe better: “aggregate data throughput”).

Whenever more than two radios are communicating, it seems that the result gets described as a “network”, and all sorts of buzzwords and proprietary architectures get trotted out, promising almost magical guarantees of success

Always remember that before a repeater can re-transmit a packet, it must receive and decode the whole thing. This imposes a ripple-through delay on each data packet, as each repeater receives and re-transmits the data.

Compared to more familiar point to point designs, this time delay can be significant; networks of many repeaters, with many hops, are well suited to slow, infrequent data gathering tasks, as witnessed by Zigbee's good penetration into the wireless sensor network market. On the other hand, such set-ups are completely inappropriate for time critical alarms or real time control tasks.

This delay is inherent to the architecture, and has no 'work around'. The users must simply be aware of the limitation, and select their methods accordingly.

In systems where events must occur with any degree of synchronisation, it will become necessary to embed real-time clock information into the burst, to allow the recipient devices to act together, rather than at the time that the network delivers a packet to each of the devices in question.

Overlapping coverage issues. In an idealised repeater network, the sender, recipient and each repeater are in fixed locations, and their areas of coverage do not overlap (the sender is in range of only the first repeater, the second repeater can hear only the first, and then so on until the recipient is in range of only the last repeater).

While this is the case in a few simple situations (a transmitter in a valley, a repeater on a hilltop and the receiver in an adjacent valley), in real world applications the situation is far more complex. In most applications the coverage areas of the sender and the repeaters will overlap, and the recipient device will be in range of more than one transmitter. Frequently, one or more of the devices will be mobile and the radio environment itself will be subject to random changes, such as reflections from vehicles or clouds, weather related changes in path loss and, hence, range.

This introduces further problems:

Multiple burst reception. If it is in range of two or more transmitters (let us consider the simplest case: the master and a repeater) then it will receive (and act on) the same data burst twice.

Repeater loop instability. In a system with two repeaters, the re-send from the second repeater will be received by the first, which will then in turn re-send that data, which will be picked up by the second one again, and re-sent ... ad infinitum. Add further repeaters (in range of each other) to

Repeaters (or "nodes" acting as repeaters) will always re-send the packet identifier without changing the sender ID code or the burst identifier byte

the system, and things get worse, as the entire network grid-locks with unnecessarily repeated copies of the same original packet.

These problems can both be addressed by the addition of some further information to the packet structure. A unique "burst identifier" (usually a single byte) is added to each packet by the original sender. Subsequent bursts will have a different identifier (incrementing it after each transmission is the simplest method, although some systems use their real time clock value as an ID). All receiving devices will then record the identifier of a packet received and discard any subsequent packets with the same ID value.

In a network where there can be multiple originating senders (such as one where a master requests a reply from a specific slave, or where there are multiple possible masters), the unique identity code of the original sender must be added in as part of the burst identifier too (so the network repeaters will respond to the reply packet too).

Repeaters (or "nodes" acting as repeaters) will always re-send the packet identifier without changing the sender ID code or the burst identifier byte.

Transmitter burst collisions. If two or more simple store and forward repeaters are in range of the same sender (either the master, or another repeater) then they will both receive and re-transmit the packet at the same time. In the overlap of their coverage areas a recipient device will be unable to receive the data packet.

There are several methods of dealing with this issue, depending a lot on the implemented hardware:

1. It is possible to phase lock the transmissions of multiple transmitters, so the destructive interference in the overlap zones never occurs. In such a network, all repeaters will transmit in exact simultaneous lock step. This can, however, require some very complex radio hardware.
2. Repeaters can be assigned specific time slots (each slot equal to the length of a single packet), depending on their unique

ID. In this case, the two previously interfering transmitters would re-send at different times (timed from the arrival of the original burst). This method provides an absolutely deterministic timing for packets propagating through the network, but increases the delay time even further, as the transmit frame must be long enough to provide slots equal to the maximum number of repeaters in the system, and all repeaters must wait until the end of the frame before timing their re-transmission (the packet must also then include a field identifying the previous repeater, to allow frame timing to be regenerated).

3. Collisions can be accepted, with each packet being re-transmitted a number of times (with a long, randomly generated time delay between transmissions) to statistically reduce the likelihood of every copy of the packet being corrupted by a collision. This is a low throughput, low duty cycle technique, with a non-deterministic through-network packet delay time. It is simple to implement, but eye-watering to model accurately.
4. Routing. Instead of every repeater potentially transmitting to every other one, it is possible to use an addressing scheme (by which certain repeaters and/or recipients respond only to certain others) to implicitly control the path through a network of each packet. A simple example of this would be a master (low powered, maybe handheld), sending only to a (high powered) main repeater, which then communicates to the slave units. This technique is best suited to fixed location repeaters with known coverage areas. It is most obviously implemented by manually planning the network (in the same fashion as a cellular network), although there are network architectures which execute the "routing" algorithms autonomously (trading a protracted network setup time for better efficiency in normal operation).

As can be seen from the very brief discussions above, this is a subject with some very involved issues in its implementation. The methods and techniques I have discussed are very much the tip of the network iceberg (for example, one proprietary network stack uses a hybrid of the time slot and collision/multiple re-send methods), but I hope that I've shed enough light on the subject to encourage some experimentation, and possibly the implementation of some simple "radio networks", without slavishly buying into an over complex proprietary product. ●

PHOTOVOLTAIC POWER SUPPLY FOR EMBEDDED SYSTEMS

WOJCIECH GELMUDA AND ANDRZEJ KOS FROM THE AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY IN POLAND, EXPLAIN THAT SOLAR PANELS CAN ALSO BE IMPLEMENTED INTO EMBEDDED SYSTEM POWER SUPPLIES, AND DISCUSS A SOFTWARE PACKAGE THAT EXISTS SPECIFICALLY FOR SUCH DESIGNS

Electronic devices are practically everywhere: houses, workplaces, cars, factories, shops etc. New things that are designed are often "filled" with electronics.

Electronic devices such as sensors for example, go into old objects too, like old buildings, to check their overall conditions, to monitor cracks in the walls and, if necessary, to raise an alarm. We could say that the 20th century initiated the electronic era and the 21st century is being sucked into it.

Due to the unstoppable progress of electronics – but also of systems requiring a lot of energy – we are seeing a growing hunger for energy which raises the total global consumption. This is why all nations around the globe worry about the near future, especially in respect to the environment. There are some EU resolutions on the use of renewable energy sources which have been put into place to decrease carbon dioxide emissions but also decrease the dependence on gas, oil and coal – resources that are limited. This is also the main reason why electronic system designers should take into consideration implementing a renewable energy source power supply in their projects. The other aspect worth mentioning is a wider range of the application areas. Sometimes there is a need for deployment of systems in remote areas with no access to a power grid. Using a battery pack is always an option, but not every application is suited to it. In a wireless sensor

network, where each node is in sleep mode and only "wakes up" from time to time to send data, nodes can work on battery supplies only. Nevertheless, despite using low-power circuits and sophisticated sleep modes, some applications still consume too much power. In many cases frequent battery replacements would be impractical.

When we hear or read about renewable energy systems, we usually think of big wind turbines or large area solar farms. However, once we focus our attention on finding these kinds of systems but on a smaller scale, it is surprising in how many of them there are, some of which are small photovoltaic systems.

There are also big solar panels, supplying power to street lights at pedestrian crossings, they can be spotted on rooftops, but the smaller ones are used in systems such as parking ticket machines, variable signposts on motorways and smaller

We could say that the 20th century initiated the electronic era and the 21st century is being sucked into it

battery chargers or in garden lights.

In the past few years, mass production and the constantly improving manufacturing techniques of photovoltaic cells and panels have yielded a significant decrease in their prices. End customers are now able to buy solar panels in any hardware store for less than \$2-4 per watt (a 50W monocrystal photovoltaic panel). At such prices an electronics engineer should at least consider employing a solar system power supply in the application, if possible; and not only in large systems, but even in small embedded devices.

Goals

In order to design a good photovoltaic power supply of a device, especially an embedded system, one must know the device by heart. It is always a good habit to first minimize energy consumption of the device. Some energy-debugging techniques come in handy. It is all about knowing the total power demands at various periods of time, i.e. in an hour, a day, a week etc. Once this is established, we can proceed to the solar system design.

To build a simple photovoltaic DC power supply, a solar panel (or a solar cell), a battery and a control device (which, for example, protects the battery from overcharging) are needed. Choosing suitable elements can be difficult and tricky. As we all know, the total energy amount coming from the Sun to the certain places on Earth varies. It depends on localization (latitude, longitude), season of the year,

roads, mobile robots and so on. Even very small photovoltaic panels (including those which consist only of one cell) are used as mobile phone

time of the day, local climate, the weather, inclination, etc. Knowing this information and also how these factors affect the amount of power coming from the Sun per square meter is of key importance.

There are some meteorological databases that a designer can easily have access to and use. However, there are also some tools made only for designing photovoltaic systems. One of these is a PC software package – PVsyst, aimed at solar systems designers, engineers, users and also students and academia.

It is a remarkable tool. Despite the fact that it is complex and comprehensive, it is very easy to use. With the help of this application, one is able to design a solar system that is either connected to a power grid (there is even a DC grid option) or a standalone system.

The PVsyst is equipped with numerous useful modules. The Meteo Database is embedded for computational purposes, but there is also an option where meteorological data can be uploaded from other databases. All of the data can be displayed in graphical mode. There is a way to visualize Sun paths and incidence angles for the specific location, time and day, or the electrical behaviour of solar panels in unsuitable conditions like partial shading, mismatch or double-orientation. There is also a large component database which holds models of real solar panels, batteries, regulators and other devices from many manufacturers. All of these devices can be customized.

Example

The best way to check how the PVsyst works is to go through an example. Before we proceed, let's create a hypothetical problem to solve:

There is a device which consists of a microcontroller, a GSM/GPRS modem, various sensors, an EEPROM, an SD memory card and a DC-DC step-down converter (with multiple LDOs). Every minute the device collects data from the sensors, pre-processes them and saves them in the EEPROM. When the EEPROM is full, the data transfer from it to the SD memory card occurs. The usage of the two different memories helps to save on power consumption.

The EEPROM uses far less energy

Figure 1: World energy consumption (past, present and projections) in quadrillion BTU [data source: United States Energy Information Administration]

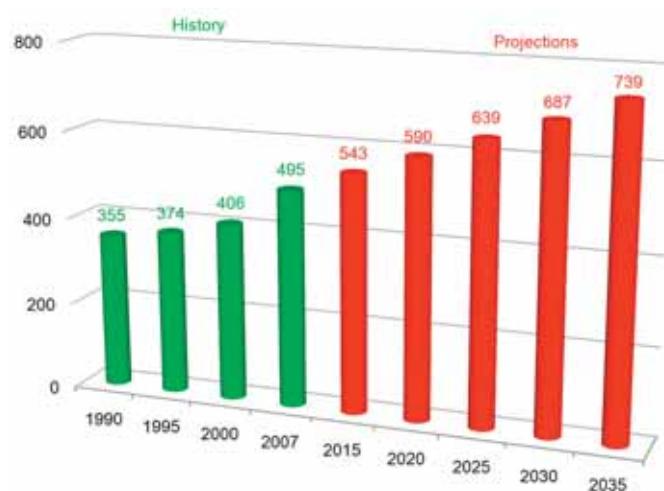
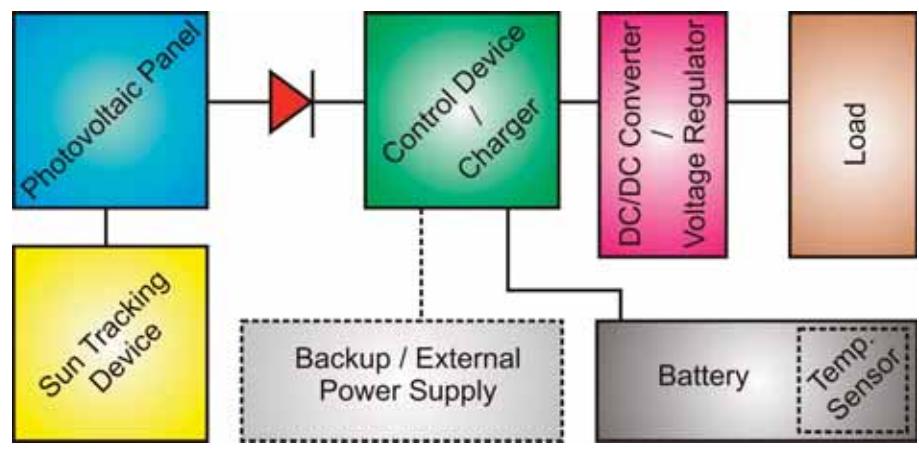


Figure 2: Photovoltaic power supply block diagram



than the SD memory card in stand-by mode. There are lots of data and approximately once a day this EEPROM-to-SD data transfer occurs, so the SD memory card becomes active only once a day for a short period of time, and then its power supply (LDO) turns off. Furthermore, every hour the device sends the updated data to the server via a GPRS modem connection.

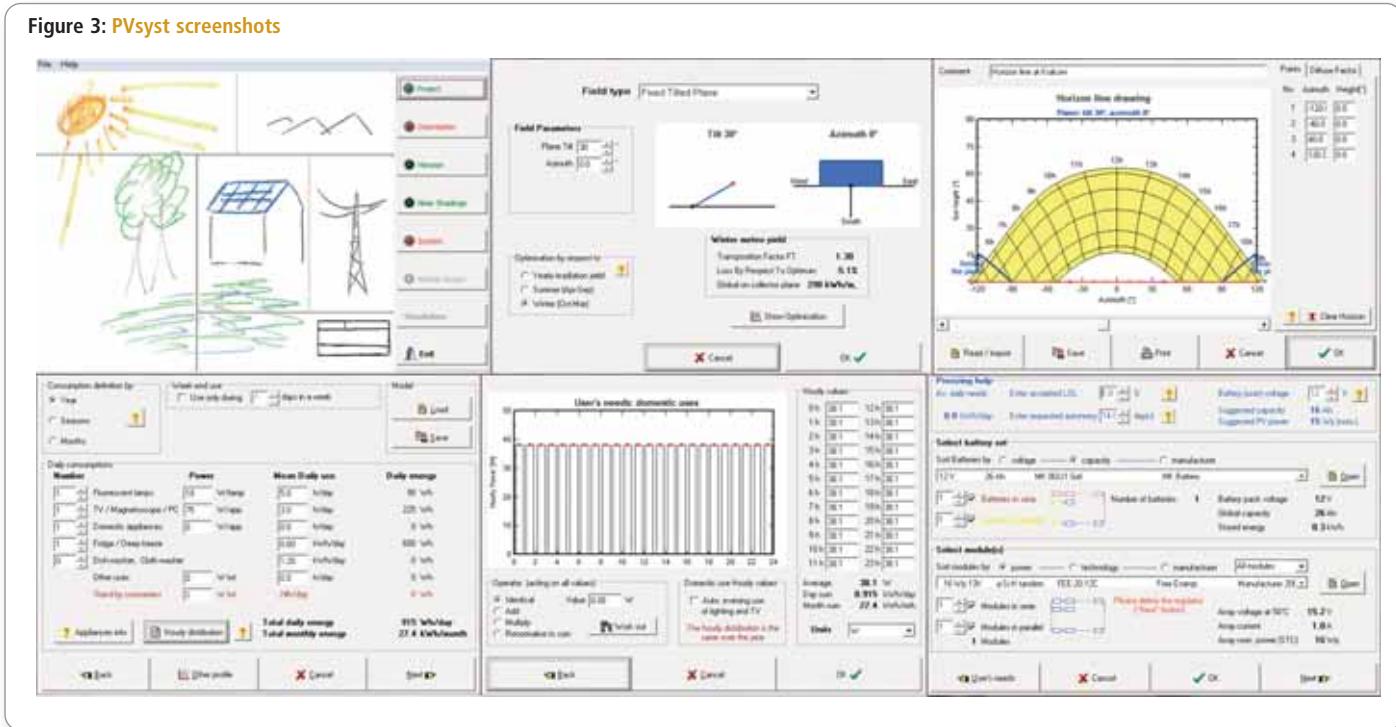
The average current consumption of this device was calculated using a current logger (powered from a 12V battery) and it amounted to 40mA, which is equivalent to 0.5W energy consumption. The device is to be deployed in some remote location with

no power grid available. The current consumption is too large to operate on the battery itself. One of the solutions is to apply a solar system. To design it, let's use the PVsyst software.

When the program starts, choose the "Project design" option and then the "Stand alone" system; hit "OK". Click on "Project". The next thing to do is to put the project description data and hit "Site and Meteo". Choose the appropriate location and the meteorological data file, and then hit "Next". Now, change the albedo values and solar panel temperature parameters if necessary; click "OK". Name the project and save it. Click "Back

Despite using only low-power circuits and sophisticated sleep modes, some applications consume too much power

Figure 3: PVsyst screenshots



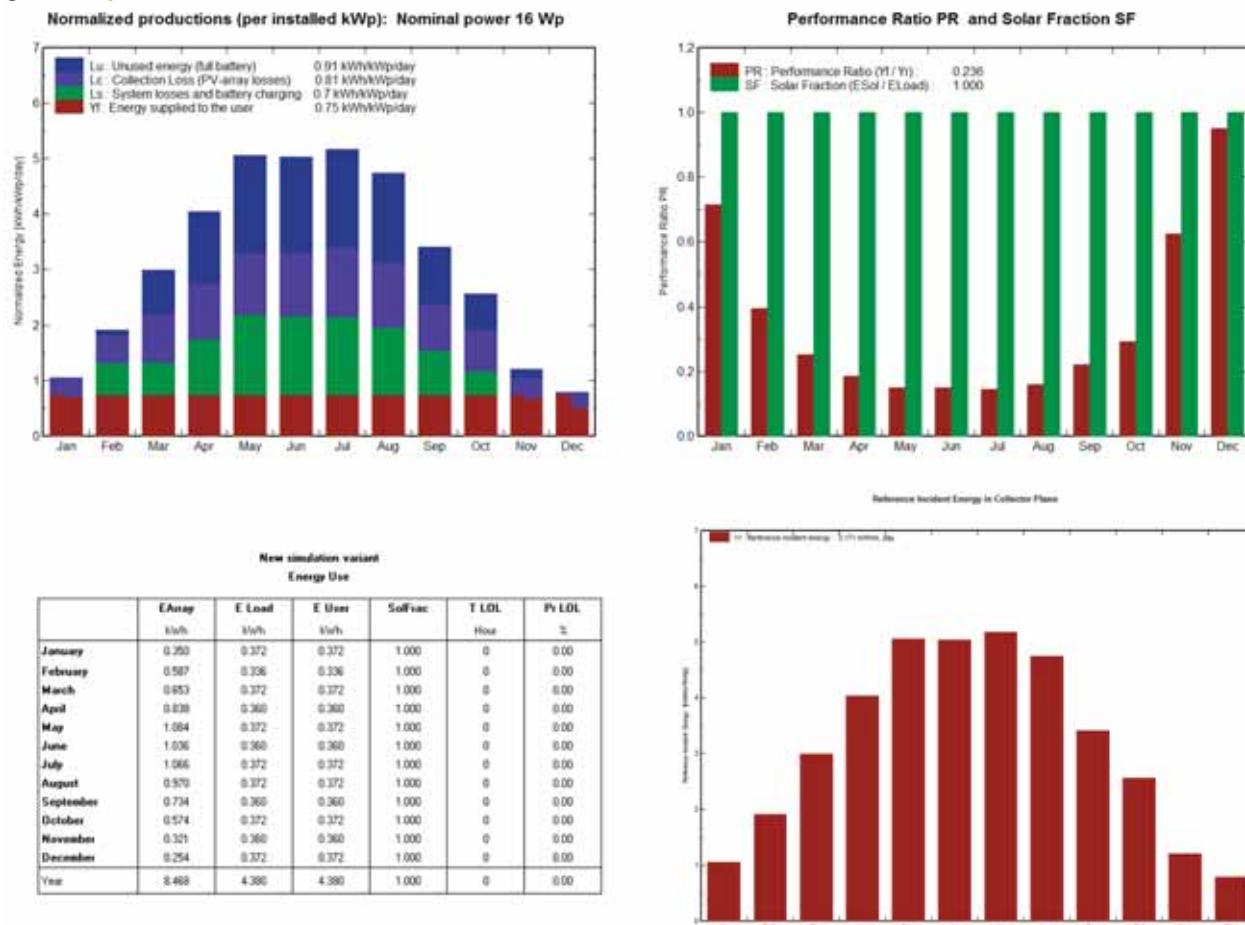
(Calculation)" and then "Orientation".

There are multiple options for setting the photovoltaic panel in relation to the

Sun. For now choose "Fixed Tilted Plane" with "Plane Tilt" set to 30 degrees and "Azimuth" to 0 degrees.

These settings are optimized for European localization for the full year. Hit "OK". If necessary, adjust

Figure 4: PVsyst simulation results



KEY ASPECTS OF DESIGNING WITH SMALL PV PANELS

THE NEED AND LOW PRICE ARE A ‘PULL’: Despite the low prices of photovoltaic panels, it is still much cheaper to use the grid power supply than to build standalone solar systems. However, from time to time there is a need to use photovoltaic conversion.

The good thing is that nowadays the cost of a small photovoltaic system is not an issue. Even hobbyists can afford a small system, even just for testing.

DON’T GUESS – SIMULATE: During the design process, instead of guessing the solar panel power and the battery capacity, it is a good idea to use some simulation software, i.e. the PVsyst. This application not only can help select the optimized photovoltaic panel power and battery capacity in relation to the location and the local climate, but it also has multiple tools to analyze and simulate weather conditions and other many other useful features, not to mention the large device model database.

LEARN SMALL, APPLY BIG: Once the knowledge of designing solar system power supplies for small embedded system devices is attained, it can easily be used in larger power photovoltaic systems.

EXPERIMENT: It is always good to experiment with the solar system design, trying to improve its conversion process, either on a simulation or a real device level. Implementing a monitoring subsystem (power consumption, photoelectric conversion) could be really helpful for that.

USE THEM EVERYWHERE: The solar panels are not only made to be used as large power plants. There is nothing wrong with implementing them into embedded system power supplies.

parameters in the “Horizon” and “Near Shadings” menus. Now it is time to put the system energy consumption data. Click “System”. Set the consumption defined by “Year” and clear all the numbers from devices, i.e. fluorescent lamps, etc. To set the 0.5W energy consumption, set “other uses” to 1W total for 12h/day and hit “Next”.

Now the solar system parameters have to be set. The LOL (Loss-of-Load) parameter describes how long a device could be inaccessible for, i.e. because the battery voltage is too low. Let us assume that the data from the sensors is very important, so we set the LOL to only 1%.

The other parameter – autonomy describes how many days the device could be operational for, if suddenly the photovoltaic panel was disconnected and the battery is full. Let us set this parameter for 14 days. Set the battery voltage to 12V. The calculations should be done automatically.

Now select the battery set and module according to the “Suggested capacity” and the “Suggested PV power”, click “Next”. Choose the “Default regulator” with the “DC-DC converter” option, hit “OK” and then “Simulation”. Choose desirable dates for the simulation, hit “Next”. After the simulation is finished, click “OK”.

There are numerous results which can be displayed and saved in many forms. I would highly recommend checking all of them – even for educational purposes.

Sometimes, we have to deal with problems where, for instance, the panel size is too big for its suspension or we need to get more energy out of it each day. One way of dealing with these problems is to design and implement a Sun-tracking device for the photovoltaic system. There is a chance that the photoelectric conversion will produce over 30% more energy per day.

However, we have to have one thing in mind – the amount of energy gained thanks to the Sun-tracking solar panel has to be greater than the amount of energy used for the photovoltaic panel positioning. How much energy can be gained with the Sun-tracking panel can be easily simulated with the PVsyst in the “Orientation” menu. ●

Figure 5: Photovoltaic power supply with sun-tracking for remote ambient temperature reading station



MORE ABOUT PVSYST

THE 15-DAY-FULLY-CAPABLE EVALUATION VERSION (after 15 days it goes to the demo mode) can be downloaded from the website www.pvsyst.com

THE FIRST EMBEDDED PLATFORM WITH FUSION TECHNOLOGY

NEW APPLICATIONS IN VARIOUS FIELDS ARE REQUIRING MORE COMPUTING POWER BUT ALSO BETTER GRAPHICS PERFORMANCE, WHICH MAKES YESTERDAY'S PROCESSORS STRUGGLING. HOWEVER, THERE ARE WAYS TO DEAL THESE TOUGH DEMANDS, SAYS CHRISTIAN EDER, SALES AND MARKETING MANAGER FOR EMEA AT CONGATEC

The AMD Fusion technology presented in January this year is a completely new type of processor architecture for the embedded market. It combines the computing power of processors and graphics cores into one compact package. Users benefit from high CPU and graphics performance, an excellent performance-per-watt ratio and flexible task allocation on the CPU and GPU.

Embedded computing tasks are becoming increasingly demanding in all types of applications. In addition to high, mostly serial processing power of x86 CPUs, there is a growing need for dedicated, often parallel, performance for the processing of complex algorithms – be that for the encoding and/or decoding of high definition videos, the processing of raw data such as industrial image processing, or complex vectorial calculations in diagnostic imaging procedures in medical technology. Up until now, if these tasks were to be processed using a x86 design requiring a large amount of processing power combined with high clock speed frequency, the end result was high energy requirements that produced a lot of heat. Multi-core technology, as well as continual increases in the efficiency of processor technology, can somewhat ease

Figure 1: The AMD Embedded G-Series platform architecture in detail

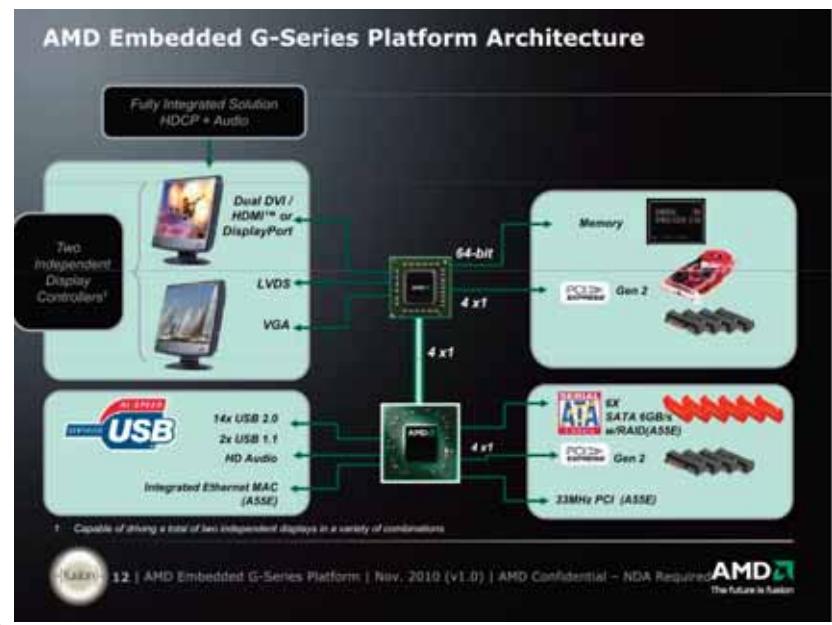


Figure 2: Tests show that the graphics performance of the new AMD Embedded G-Series platform is one of the best around



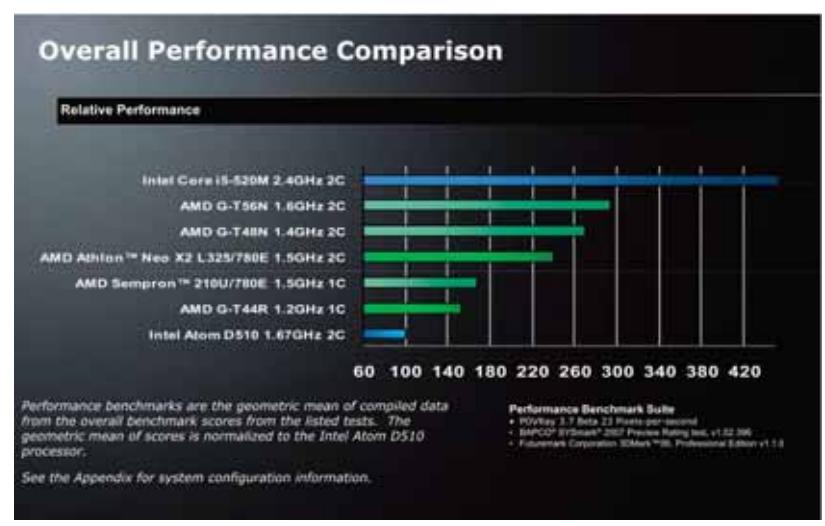
this pressure; however, the fact still remains that the clock rate of faster processors cannot fulfil all requirements on its own.

Mixing In Graphics Performance

In the meantime, graphics performance

is becoming an increasingly important factor in the embedded sphere. So far, long-term availability, compact design, high energy-efficiency and robust design have been the most important requirements of embedded designs, but now high graphics

Figure 3: AMD G-T56N 1.6GHz Dual Core APU performance comparison



performance is added to the mix.

This can already be seen with small displays for mobile devices. In the consumer market, resolutions of 400 x 800 pixels for screen sizes of 3.5 inches, for example, are already considered mainstream. The larger monitors become, the higher the resolution offered. This obviously means that even in embedded fields, small and medium-size screens up to 15 inches will offer higher resolution and, therefore, additional user benefits.

The performance requirement is also supported by two additional trends. On the one hand, capacitive touch sensors are required, among other things, for robust, highly accurate touch solutions as well as innovative multi-touch technology, which has overtaken resistive technologies according to a study from VDC about touchscreen sensors and displays. On the other hand, large-sized touchscreens (> 15") for applications such as POI and interactive context sensitive digital signage solutions rank among the most profound progressive solutions. Given the resolution requirements, excellent graphics performance is a must for all of these applications.

It's not only higher screen resolutions that require more graphics performance; it is also required by innovative operating concepts that utilize a modern high-quality GUI. Examples can be seen in the medical, industrial and building automation, gaming,

kiosk, POS/POI, infotainment and (interactive) digital signage segments. Here, 3D performance for appealing animation and visualization as well as fluid playback of HD content is needed. In these applications high 3D performance is not only useful for delay-free display and animation of images; but it also improves the user experience and operating reliability of touchscreen-based applications.

Last but not least, the graphics core also needs to ease the workload of the CPU during HD video decoding, which is, for example, very important in medical (4D ultrasound or endoscopy) and infotainment applications.

High graphics performance is not only needed for large screens since even small and medium-size screens require more graphics performance capabilities with increasingly higher resolutions. Moreover, the closer embedded applications are to the consumer sector, the higher the expectations of the user. Good examples are gaming applications or POS/POI terminals. As a consequence, many embedded applications are becoming more and more demanding with regard to graphics performance.

Addressing Task Distribution

Up until now, the graphics performance of embedded solutions has increased proportionally to CPU performance. The more graphics

FUSION ON CONGA-BAF

CONGATEC'S COM EXPRESS BASIC COMPUTER-ON-MODULE CONGA-BAF

is one of the first platforms that implements AMD's new Embedded G-Series platform with Fusion technology.

performance required, the higher the CPU had to be clocked. But this dependency is not actually irrevocably linked: It is also true to say that the more tasks the GPU takes on, the more the CPU is relieved. Theoretically, it can therefore also be underclocked the more powerful the GPU is.

However, this was previously not required since demands have always increased in both spheres. But such isolated advancement of CPUs and GPUs makes less and less sense now. Hence, AMD has combined both technologies into one package with the Embedded G-Series platform. Now, users can benefit from an extremely high-performing graphics core with a broadly scalable processor performance at an extremely compact footprint of only 19mm x 19mm. Fusion also goes an important step beyond mere hardware integration: The APU combines the serial computing power of the processor core with the parallel computing power of the graphics card. This leads to a merging of

 The fact still remains that the clock rate of faster processors cannot fulfil all requirements on its own

the previously existing software engineering task distribution of the processor and graphics core. Simply put, the graphics core can relieve the processor cores during parallel tasks thereby increasing total system performance far beyond of what was previously possible. But how does this work and what does it mean for embedded applications?

Graphics Core as a "Co-Processor"

First, one must understand how the graphics core functions: Geared by the consumer market, the efficiency of the graphics core has steadily increased. In particular, the 3D representation of virtual worlds has advanced the specialization of the graphics card to the highest parallel computing power. Due to the variety of graphic data, such as computations of textures, volumes and 3D modelling for collision queries, as well as Vertex Shader for geometry computations, the functionalities are no longer cast firmly in hardware, but rather can be programmed freely. Thereby, modern graphics cores offer an enormously flexible performance potential. With the aid of the so-called GPGPU (General Purpose Graphics Processing Unit) one can use this potential

not only for graphics computation and representation but also for data processing.

Examples can be seen in the computation of 3D ultrasounds in medicine; in face recognition in the field of security; in image processing in industrial applications; or, in the encoding and decoding of data. Certain data forms, for example from sensors, gauge heads, transceivers or video cameras, are processed more efficiently and faster with dedicated processing cores than with the generic, serial computing power of x86 processors. With the GPGPU it is irrelevant if program code data is produced virtually or forwarded from external sources. There is, therefore, a lot to be gained from uniting the CPU and GPU in an APU (Accelerated Processing Unit) in order to create an even stronger team.

APU Performance is Crucial

As a consequence OEMs and users must say goodbye to the phrase "outstanding CPU performance" since it is no longer the case that only the CPU defines computing power. The graphics core also plays a crucial role. Apart from pure graphical representation, this is already being employed in mass applications, for example in filter algorithms of image editing software programs, such as

THE AMD G-SERIES EMBEDDED PLATFORM IN DETAIL

THE FIRST AMD FUSION PRODUCT

is the long-term available Embedded G-Series platform and the AMD A55e controller hub, which has been designed for the special requirements of the embedded market. The AMD A55e only implements the PCI, USB, SATA and audio interfaces. To that end, the accustomed three-chip solution of processor, northbridge and southbridge is reduced to a compact two-chip solution with an Advanced Processing Unit (APU) and controller hub. This saves both space and costs.

The power consumption of the AMD G-Series platform, depending on clock rate and the quantity of cores, ranges between 9W and 18W TDP. Thanks to the compact footprint of the embedded modules, OEMs profit from a simplified SFF design. Additionally, the module's low TDP simplifies the thermal design of the embedded solution and, therefore, makes it possible to develop robust applications with less design effort even faster.

A Multitude of Variants

At present, the AMD Embedded G-Series platform is available on COM Express module conga-BAF in five variations, from the 1.2GHz AMD64 processor core with a 512KB cache to the two 1.6GHz clocked AMD64 processor cores, each with 512KB cache. Beyond that, the APU implements four generic PCI Express Gen 2.0 Lanes for application-specific enhancements, as well as for PCI Express Gen 2.0 Lanes to the embedded fusion controller hub. As with previous AMD products, the memory is directly connected to the APU and, therefore, provides instant memory access without delay.

The AMD G-Series platform activates up to two single channel RAM modules over a 64-bit DDR3-1333 interface. The integrated graphics core with the Universal Video Decoder 3.0 for the liquid processing of BluRays with HDCP (1080p), MPEG-2, HD and DivX (MPEG-4) videos supports DirectX 11 and OpenGL 4.0 for a faster display of 2D and 3D images as well as OpenCL 1.1 and Microsoft DirectCompute for the programming of the parallel arithmetic units of the graphics core. On the graphic interfaces, using dedicated outputs for VGA, Single-Channel LVDS, as well as DisplayPort and DVI/HDMI, two independent displays can be directly controlled.

The 3D representation of virtual worlds has advanced the specialization of the graphics card to the highest parallel computing power

Photoshop; programs for encoding and converting video data; as well as in the Adobe Flash Player. However, developers had to struggle with the fact that traditional CPU architectures and programming tools were not suitably qualified for vector-based

data with parallel multithreads. These hurdles can be overcome with the Fusion technology. With the help of easy-to-use APIs, for example DirectCompute by Microsoft or OpenCL, which are supported by AMD's Fusion technology, application software developers can efficiently use the potential of the APU graphics core for various tasks apart from the original purpose of graphical representation. Naturally, the graphics core must support this. AMD's Embedded G-Series platform is the first to fulfil this requirement. AMD

therefore already provides SDKs, which help to simplify the introduction of the new type of data processing.

"Simple" Embedded Computing

The positioning of the Fusion technology is not only suitable for special applications. Rather, the G-Series platform can be used across the entire spectrum of embedded computer technology. With a broadly scalable performance, from economic single core variants with 1.2GHz to variants with 2 x 1.6GHz dual core processors, the new AMD platform covers around 80% of all application requirements in the embedded market, from low-power to high-performance applications. In order to break down the performance spectrum to known standards, one can also say that the AMD Embedded G-Series platform is scalable for solutions that have the requirements profile of an Intel Atom processor up to the Intel Core i5 dual core performance (1st generation). This is coupled with a competitively superior graphics performance, which, thanks to GPGPU, can also be used for embedded computing tasks. This, however, has not yet been incorporated in the performance calculation; so, depending on the application, the

Figure 4: conga-BAF is the world's first COM Express basic Computer-On-Module which is based on the new AMD Embedded G-Series platform



performance potential can still be significantly increased. Regardless of which segment, OEMs can therefore implement their full product range on the basis of a single processor architecture. This not only reduces development costs and time, but also simplifies supply chain and lifecycle management along with the associated costs. The use of Computer-On-Modules is recommended for OEMs and developers who prefer to directly use the core computing components without a lot of design effort and who also wish to further optimize their supply chain management with as flexible a COTS platform as possible.

An Ideal Technology Medium

Computer-On-Modules are embedded PCs with enhanced core functionality that can easily be attached to the carrier boards. Only the customization of the carrier board with I/Os required for the customer's application must be developed. This way, the development and the design-in-phase of embedded systems are simplified considerably. Since support and development engineers already support the customers with product ideas, system costs and system integration can be optimized from the outset.

Due to interchangeable computer modules, both the processing power and the support of interfaces become scalable. By using computer modules the brand new AMD G-Series platform can quickly be designed into existing applications as well as new designs.

The world's first Computer-On-Module to be equipped with this new processor technology is congatec's COM Express basic Computer-on-Module conga-BAF. As one of the first designs, the new conga-BAF with AMD Fusion offers OEMs a combined computing and graphics performance which, up until now, was either not possible at all or only possible with a significantly higher TDP (Thermal Power Design).

The conga-BAF is based on the COM Express Basic (125 x 95mm) form-factor. It is scalable across the total bandwidth of the available AMD G-Series platform APUs: From the 1.2GHz single-core APU to the 2 x 1.6GHz faster dual-core variation. This

allows OEMs to finely calibrate the computing power to the performance demands. Two memory sockets for up to 8GB of the fast DDR3-RAM are supported, which speeds up memory-intensive applications even more.

Compliant with the new COM Express Specification COM.o rev. 2.0, it implements 6x PCI Express x1 lanes Gen 2.0, 4x SATA 3, 1x PCI, Gigabit Ethernet, 8x USB 2.0 and EIDE interfaces. In particular, developers will benefit from the dedicated digital display interfaces with 2x DisplayPort, 2x HDMI or DVI allowing for a faster and more flexible integration of all types of monitors currently available on the market.

Needless to say, VGA (2560 x 1600) and LVDS (1920 x 1200) are also supported. In total, two independent displays can be controlled. Especially for safety-critical applications, the new module provides a discrete, trusted platform with the highest level of security in authentication and data integrity. ●

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THOMAS CARMODY, CSR'S HEAD OF CONNECTIVITY MARKETING FOR AUTOMOTIVE APPLICATIONS, SHARES HIS VIEW ON WHY REAR-SEAT ENTERTAINMENT IS NOT YET TAPPING INTO ITS FULL POTENTIAL

TAKING A BACK SEAT

The automotive industry has always been a breeding ground for technical innovation, embedding the latest standards to enhance vehicle security, comfort and entertainment.

Rear Seat Entertainment (RSE) holds much potential to bring high quality audio and video devices into the cabin.

Over the last decade a lot has changed in the RSE market. While originally it was primarily targeted at high-end vehicles, RSE has now made an impact on smaller and more medium-end vehicles. Manufacturers and OEMs have long understood the advantages and opportunities here, and Audi and Renault are two of the many car manufacturers that have made recent

announcements to attempt to align with this, offering factory-installed RSE systems as standard. Pushing the latest entertainment devices forward creates an opportunity to differentiate and to promote a brand's reputation for technological innovation.

And it's a growing market. In a recent Market Playground report (see Market Reports box), car maker GM has admitted to examining the industry closely. iSuppli has also made predictions that the market for RSE will almost double by 2015. We're likely to start to see more screens, MP3 players and multipurpose Internet connectivity devices making their way into cars as factory-installed devices will be appearing in new vehicle models in the high and medium vehicle segments.



Wi-Fi is Making a Foray into Vehicles Too

In the near future, it seems likely Wi-Fi will become more and more widespread in in-vehicle applications and the extended use of wireless technology will deliver the basis for cloud and media services including Internet access, films, games and music content. The next step for companies in the automotive sector is to future-proof their audio technology as more high quality formats, such as Blu-ray players and HD audio music files, will find their way into cars sooner rather than later.

However, one obstacle to this trend is that there are some issues to be overcome in the delivery of wireless audio. One of the keys to enjoying RSE systems to their full extent is the availability of high-quality, low latency audio.

For good reason audio in RSE has been predominantly delivered by Bluetooth, which has been the preferred means of wireless audio delivery to stereo headsets due to its cheapness, standardisation and low power consumption. Wi-Fi has proven to be suitable for some streaming applications where power consumption and latency are not such an issue. Yet Bluetooth, with its lower overheads, attesting to get the same result with much less latency and better power-consumption, which makes it far more appropriate for battery-powered wireless entertainment devices.

There is, of course, always the option of proprietary wireless audio; but I think the market decided on that one a while ago. Rather than limiting themselves to a single supplier, or a much smaller base of suppliers, most people prefer to opt for standardised technologies. And unlike many proprietary technologies Bluetooth can, at least, support multiple connections to different devices at the same time.

So what's been the problem? Well, as mentioned, the key requirements to ensure seamless and enjoyable RSE are wireless audio quality and latency; areas where Bluetooth has hitherto been lacking.

To put things in context, automotive decision makers generally desire certain

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minimum quality standards in RSE systems: Firstly, they are aiming for CD-quality audio – ideally 16-bit data, with a sampling frequency (Fs) of 44.1kHz or 10Hz to 20kHz frequency bandwidth. Another factor that is crucial is to achieve 'lip sync' so that the latency is typically fewer than 40ms, which is the rough duration of a single (1/24th) frame of film. This latency figure becomes particularly important for delivering seamless audio in games and videos, and it is acknowledged that latency should really be brought closer to 30ms.

So far, the Bluetooth A2DP profile has been regarded as a reliable option for audio streaming, assigning the Sub-Band Coding (SBC) CODEC for use within the transport layer. However, there are a number of issues here.

For starters, at around 100ms delay,

SBC-encoded audio is rather 'laggy'. This is because SBC's compression is based on a frame of samples. This really doesn't work well as far as audiovisual material is concerned.

What's more, the majority of implementations of A2DP default to a "medium" quality option using a Bit Pool of 32. What you actually get at the end, with 32kHz Fs or 10Hz to 1Hz bandwidth, is actually something closer to FM quality than CD-quality.

In many cases these perceived restrictions have forced automotive OEMs away from standards such as Bluetooth to more rigid and limiting solutions.

RSE's Future

The future has already begun, and the potential of RSE is now one of the keys to providing differentiation within the

automotive industry. OEMs are looking to ways of helping us enjoy ourselves during our journey, and of allowing us to integrate our personal devices such as smartphones and tablets with the car's wider ecosystem.

The demands and expectations for optimised Rear Seat Entertainment systems are very high but knowing the forward-thinking nature of the automotive industry, it is more than ready to face and master this challenge. ●

WHAT'S CSR DOING?

MY COMPANY CAST AROUND FOR A SOLUTION A WHILE AGO:

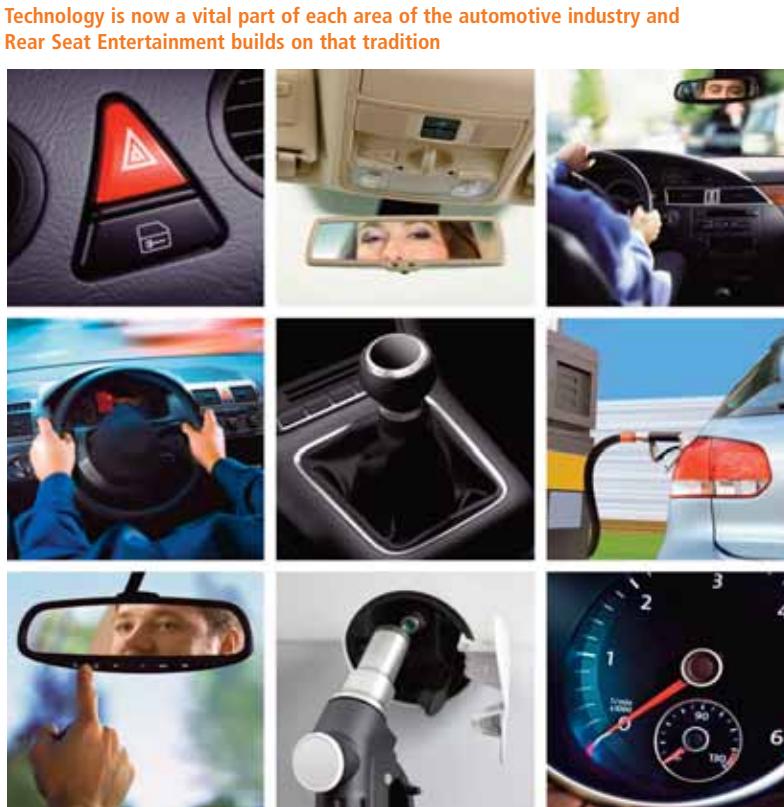
an alternative to A2DP that addressed some of these issues. We discovered the aptX CODEC, which has already made a huge difference in the professional audio sector for nearly 20 years. Cinema, TV and music sectors have already adopted it for streaming and storing applications, as well as for low-latency transport of broadcast-quality audio from studio to transmitter. The aptX CODEC is now implemented with most of the 44,000 public and commercial radio stations worldwide.

Basically aptX achieves a non-destructive compression process through innovative procedures embedded within a wider ADPCM process. Using a gentle 4:1 compression ratio, aptX can deliver CD audio quality that is indistinguishable from the PCM original with a coding latency of only 1.92ms. CSR found this to be the only CODEC for Bluetooth A2DP that could achieve the combination of quality and efficiency that it required in order to solve these RSE issues.

In terms of audio quality, empirical data on this CODEC indicated an average figure of -0.067 using ITU-R BS-1116-1 test standards for judging the performance of high quality audio CODECs. This method uses a scale from 0 to -5, where -1 is deemed to be imperceptible from the original source content.

Thanks to its novel sample-based architecture and 4:1 compression ratio, aptX's granularity in terms of editing points can be brought down to 4 samples. The packets within any given transmission can be populated more efficiently as result of being able to slice the CODEC so thin. This in turn reduces latency through a decreased need for buffer space. In the end, while maintaining RF robustness, latency in this CODEC has been brought down to 32ms; more than enough for multimedia applications.

The rear seat cabin is a blank canvas for OEMs with limitless opportunities to entertain the passengers



HIGH-END GRAPHICS PERFORMANCE FOR LOW-POWER SMALL-FORM-FACTOR (SFF) DESIGNS

NORBERT HAUSER OF KONTRON LOOKS AT THE BOARDS AND MODULES CURRENTLY AVAILABLE TO DESIGNERS THAT ARE BASED ON THE AMD'S EMBEDDED G-SERIES PLATFORM FOR GRAPHICS-INTENSIVE SFF APPLICATIONS

Huge advances in the semiconductor industry have meant that the number of transistors on a given area of silicon has practically doubled every two years.

This increase in efficiency has paved the way for engineers to add additional x86 processor cores and further functionalities to the processor dies, making today's CPUs the fastest, most versatile and energy-efficient processors ever. These enhancements also are the foundation for the now almost ubiquitous use of x86 embedded computing technology in an ever-growing range of vertical markets and applications.

Even with these enormous improvements in computing performance and power consumption,

DirectX11), OEMs have had to search for solutions that meet these stiff requirements so as to create rich visual experiences for users.

But, one such suitable solution that's available now is the new AMD Embedded G-Series platform, which integrates energy-efficient processor cores and an advanced DirectX 11-capable graphics processing unit into a new class of embedded processor: the Advanced Processing Unit (APU). AMD's "Fusion" technology enables OEMs to increase the performance, efficiency and mobility of their small-form-factor applications to attain a new level of user experience.

New Processing Units

Embedded boards and modules equipped with the new AMD Embedded G-Series platform provide all of these needed features within an extremely small footprint and at a low-power envelope. The AMD Embedded G-Series is the first one to integrate the new Fusion Accelerated Processing Unit (APU) that merges the computing capabilities of x86 technology with the parallel computing power of a general-purpose graphics processing unit (GPGPU) in a single computing unit. This allows OEMs to develop low-power SFF applications that had previously been the domain of high-performance multicore designs. Not only do these new solutions include a single or dual-core AMD 64 processor, the highly integrated APU incorporates a powerful DirectX 11-capable discrete-level graphics and parallel processing engine, UVD 3.0 (the dedicated high-definition video acceleration block), as well as a

As the advantages of embedded technology make gains in new vertical markets, OEMs have had to search for solutions that meet these stiff requirements

one area of the embedded computing sector has until now not been able to keep up with the rapid advancement pace: graphics performance. As the advantages of embedded technology make gains in new vertical markets, such as multi-media content delivery applications, kiosks, POI/POS and the professional gaming arena, all of which make extremely high demands on graphics performance and require support via the latest APIs (like



Figure 1: Within the compact footprint of only 19mm x 19mm, the new AMD embedded G-Series APU integrates a single-core or dual-core CPU, a programmable GPU, plus a video decoding unit and a memory and PCI Express controller on a single die

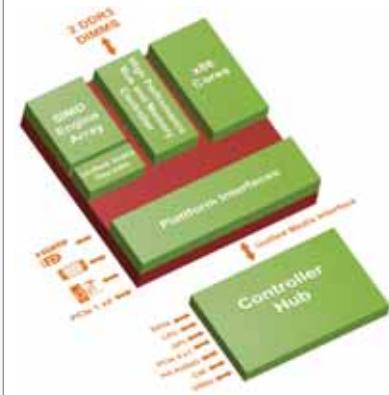


Figure 2: When paired with the A50M I/O controller hub with support for advanced interfaces such as 6Gb/s SATA, Generation 2 PCI Express and HD Audio, the AMD Embedded G-Series platform delivers a low-power, value-oriented solution for applications requiring a better balance of CPU and multimedia performance. For high-end, full-featured platforms, the A55E I/O controller hub is an alternative pairing choice with added features such as Gigabit Ethernet MAC, RAID (0/1/10) support with FIS-based switching, and PCI Local bus support

DDR3 memory controller and a PCI Express 2.0 controller round out the complete package.

The AMD Embedded G-Series APUs include five different performance versions, ranging from the AMD T44R with a 1GHz single-core AMD 64 CPU and 9W TDP to the AMD T56 N with a 1.6GHz dual-core CPU and 18W TDP.

This broad span of performance – all within a single platform – enables OEMs to adjust the performance and power consumption to the precise “sweet spot” of the application.

Additionally, those customers who wish to build a complete product line from



Figure 3: The Kontron microETXexpress-OH is a COM Express compact, Pin-out Type 6-compatible Computer-on-Module with CPUs from the new AMD G series range COM Express Computer-on-Modules

entry level up to high-performance can do this on a single embedded platform. They don't need to adapt the OS and software to different chipsets, but can simply use the same configuration on any device. This reduces the amount of development effort required, minimizes a product's time to market and reduces the total cost of ownership.

Owing to its extremely low thermal design power of just 9 or 18W, the AMD G-Series is ideally suited for fanless and rugged low-power applications, such as outdoor infotainment and kiosk systems or advertising panels. For mobile applications, such as the panel PCs, commonly used in medical or manufacturing environments, the APU's power-saving features help to greatly reduce the amount of power the devices consume. These features include the processor as well as the graphics engine to maximize their effect.

Discrete Level Graphics Performance

Common to all the performance levels of the new boards and modules based on the AMD Embedded G-Series platform are their discrete-level graphics capabilities. Providing support for the latest DirectX 11 API, they enhance all conventional graphics-intensive, small form-factor applications. The integrated AMD Radeon HD6310 supports DirectX 11, as well as OpenGL 4.0 and gives

users a superior 2D or 3D graphics experience with top frame rates and resolutions (of up to 2560 x 1600 pixels). This is discrete-level graphics performance and enables cost-effective, space-saving systems to be designed without a dedicated graphics card, yet with the same performance.

Furthermore, by integrating the Universal Video Decoder 3.0 that unloads the CPU when decoding video streams, boards and modules equipped with AMD's new Fusion processors have set a new benchmark in their power range. They can decode 1080p BluRay videos with HDCP as well as HD MPEG-2 and DivX (MPEG-4) videos.

The new AMD platform even supports decoding of up to three HD videos in parallel. Up to four displays are supported by a rich variety of interfaces, including DisplayPort, DVI and HDMI, as well as the embedded interfaces LVDS and VGA at a maximum resolution of 2560 x 1600 pixels. This enables cost-efficient multi-monitor systems to be set up. This unprecedented level of graphics integration creates a new foundation for delivering high-performance multimedia content in a small-form-factor, power-efficient platform suitable for a broad range of low-power designs in embedded applications, such as x86 set-top boxes, IP-TV, thin clients, information kiosks, points of sale appliances and gaming systems.

Supercomputer-Like Performance

Another area that is well-suited for boards and modules with the new AMD Embedded G-Series APUs are applications requiring increased parallel computing capabilities. Take real-time pattern recognition in quality control, sonar or radar data analysis, video surveillance, or medical imaging applications, like the reconstruction of 3D X-ray images and the detection of anomalies, for instance. These applications require multiple processing cores that can handle vast amounts of data in parallel. Hundreds, if not thousands, of individual threads need to be processed to manipulate the high-volume data streams. However, traditional CPU architectures and application-programming tools are optimized for scalar data structures and serial algorithms. As such, they are not the best match for these data-intensive vector-processing applications. But how



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can an integrated graphics card help to boost computing performance?

Driven by the thirst for 3D gaming in consumer electronics, current graphics processing units (GPUs) have evolved into powerful, programmable vector processors that can speed up a wide variety of software applications. These "general-purpose GPUs", as they are known, are no longer limited to the consumer market. They are making their entrance into the embedded market with the arrival of the new AMD Embedded G-Series platform. Powerful APIs such as DirectX and OpenGL have made the utilization of these additional resources an easy thing for developers of graphics-intensive applications.

Lately, new software tools like DirectCompute and OpenCL have enabled developers to unlock the computing power of the programmable GPU cores in their applications. Before today, application developers have had no access to embedded solutions that

make use of this innovative technology. Now, with the new AMD Embedded G-Series platform, this efficient way of processing data is supported. OEMs can now add the parallel processing power of the AMD Radeon 6310 GPU to their applications. By doing this, it's possible to add supercomputer-like performance to small-form-factor embedded designs and obtain a previously unachievable performance-per-watt ratio.

Building Blocks for Graphics-Intensive SFF Devices

This highly attractive feature set makes these new boards and modules an ideal substitute for many existing platforms. But not just that; they can also be employed for completely new designs and application areas for SFF designs.

Kontron simplifies and accelerates the integration of Fusion technology by supporting it on the most popular form factors for graphics-intensive SFF applications that come with dedicated,

market-oriented feature sets. By implementing the new AMD APUs on the most common form factors for graphics-intensive applications, such as computer-on-modules and small-form-factor SBCs and motherboards, the benefits of this innovative architecture are made readily available for application development. Additionally, with the support for OpenCL 1.1 and Microsoft DirectCompute, parallel processing executed by the graphics core will speed up vector processing applications such as situational awareness and video surveillance in the industrial automation, military and medical markets. OEMs and system integrators can take full advantage of highly scalable validated platforms that deliver advanced capabilities while reducing the amount of development effort needed and lessening the design risks and time to market for both graphics-intensive and data-parallel applications. ●



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ACCELEROMETERS IN EMBEDDED
MICROCONTROLLER APPLICATIONS
AND GIVES THE DESIGN OF AN
INCLINOMETER WITH LCD OUTPUT,
BASED ON AN ACCELEROMETER
AND A MICROCONTROLLER

Accelerometers are tiny electronic chips used to measure the static or dynamic acceleration directly. By measuring the static acceleration due to gravity for example, we can find out the tilt angle of a device with respect to the Earth.

By measuring the dynamic acceleration, we can analyse the way the device is moving. For example, in addition to measuring the acceleration we can determine the speed of the device by integrating the acceleration data and, also, the position of the device by double integrating the acceleration data.

Accelerometers provide outputs in units of "G", where 1G is equal to 9.81m/s^2 (or 32.2ft/s^2), which is Earth's gravity at sea level. Some typical G values are given in Table 1 for reference.

Accelerometers are used to measure one or more of the following physical entities:

- Acceleration
- Rotation
- Tilt angle
- Vibration
- Collision
- Gravity

Many embedded consumer products nowadays contain accelerometers. Table 2 gives a list of some of the common consumer application areas of accelerometers.

Accelerometers are recently used in laptops to protect hard drives from damage. If, for example, the laptop is dropped accidentally, the accelerometer detects the sudden fall and switches the hard drive off to lock the heads so that they don't crash on the platters.

Accelerometers are used in car airbag trigger mechanisms to detect sudden deceleration of the car, as is the case in car crashes, and then cause activation of the airbags at the right instant of time to protect the passengers.

USING ACCELEROMETERS IN EMBEDDED APPLICATIONS

Most good quality digital cameras and camcorders use accelerometers for image stabilization to reduce blurring associated with the motion of the camera during exposure. Camera shake is usually problematic at slower shutter speeds or with telephoto lenses. Image stabilization permits the use of 2-4 stops slower shutter speeds thus eliminating the problems caused by camera shake.

The navigation of mobile robots is usually based on GPS and dead-reckoning techniques. Dead-reckoning is used at places where there are no GPS signals, such as indoors, in forests or in dense urban areas where tall buildings obstruct the GPS signals. In dead-reckoning, accelerometers are used to estimate the speed, position and rotation of the robot from a known starting point.

Some expensive cell phones (e.g. Apple iPhone, Motorola Milestone, Sony Ericsson X10, Samsung Galaxy etc) are equipped with built-in accelerometers so that movements of the phone can be detected in real-time. These accelerometers provide realistic game

capabilities to the phones. For example, there are many car-racing, boat-racing or flying-machine games where movements are mapped to the phone accelerometer, thus enabling the user to control the machines closely by simply tilting the phone. Examples of some popular accelerometer-based cell phone games are given below.

In the classical game Labyrinth the user can control the position of a steel ball by tilting the phone so as to avoid the holes. BiiBall is another accelerometer-based game with the goal of navigating a rolling ball across

DESCRIPTION	G VALUE
Earth's gravity at sea level	1
Elevator accelerating up	1.5
Commercial airline at take off	1.5
Passenger car cornering	2
Amusement park rides (max)	3.5
Sprint missile	100
9 mm handgun bullet	31,000

Table 1: Some typical G values

CONSUMER PRODUCT	FUNCTION
Cell phones	Menu scroll, pedometer, image rotation, realistic games
Digital cameras	Image stabilization
PDA	Navigation, games
Camcorders	Image stabilization, HDD protection
Laptops	HDD protection, dead-reckoning navigation
MP3 players	HDD protection
Vehicles	Shock (car crash) detection, tilt angle sensing, acceleration sensing, alarm systems
Gaming devices	Realistic motion, gyroscope, pedometer, tilt angle detection
Robotics	Dead-reckoning navigation, tilt angle detection, collision detection
Instrumentation	Tilt sensors, spirit-level sensors, hand-held accelerometers
Medicine	Patient monitoring

Table 2: Use of accelerometers in embedded consumer products

ACCELEROMETER	MANUFACTURER	OUTPUT	RANGE	AXIS	SUPPLY VOLTAGE
MXD2020E	Memsic	Digital PWM	$\pm 1G$	2	2.7V to 3.6V
MXD6025	Memsic	Digital PWM	$\pm 2G$	2	2.7 to 3.6V
ADXL202	Analogue Devices	Digital PWM	$\pm 2G$	2	3V to 5.25V
ADXL213	Analogue Devices	Digital PWM	$\pm 1.2G$	2	5V
ADXL330	Analogue Devices	Analog	$\pm 3G$	3	1.8V to 3.6V
LIS244AL	STMicroelectronics	Analog	$\pm 2G$	2	2.4V to 3.6V
Model 2420	Silicon Designs	Digital	$\pm 2G$ to $\pm 200G$	3	5V
SMB482	Bosch	Digital	$\pm 120G$	1	5V to 11V
MMA7455L	Freescale Semiconductor	Digital SPI/I2C	$\pm 2G$ to $\pm 8G$	3	2.4V to 3.6V

Table 3: Some accelerometer chips

landscape to avoid obstacles, where the ball is controlled by tilting the phone.

Accelerometer Basics

Accelerometers used to be large, clunky and expensive instruments and it was not practical to use them in robotics and embedded

microcontroller-based applications. With the advent of the MEMS (Micro-Electro-Mechanical-Systems) technology it is now possible to manufacture accelerometer chips with footprints of less than 1cm^3 . Acceleration is sensed either on 2-axis or 3-axis principle. 3-axis devices measure the acceleration on

forward-backward, left-right and up-down.

There are many types of accelerometer chips. Some of the commonly used ones are based on the principles of capacitive, piezoelectric, piezoresistive, magnetoresistive or heat transfer mechanisms. Table 3 gives a list of some of the accelerometer chips available in the market.

There are a number of factors that should be considered before selecting an accelerometer. The range of the sensor should be at least ± 1 , preferably $\pm 1.5G$. Another important consideration is the output signal configuration which dictates the level of interface complexity. The three most common outputs are analogue, pulse-width-modulated (PWM) and digital. The analogue output requires A/D converter, while the other two outputs can be connected directly to digital ports of a microcontroller. Number of axes is also an important consideration. For simple acceleration or tilt angle measurements 1-axis or 2-axis sensors can be used. For three dimensional movement and acceleration measurements, a 3-axis sensor should be chosen. It is also important to realise that most sensors operate with a voltage in the range 2.7V to 3.6V and thus can not be connected directly to +5V supply.

ADXL202 and ADXL330 from Analogue Devices are very popular accelerometer chips and their operations are described here briefly.

ADXL202 is a solid-state 2-axis accelerometer in an 8-pin package, 10 x 9.9 x 5.5mm in size, and measuring acceleration in the range $\pm 2G$. It is based on capacitive principle where a polysilicon structure is suspended over a silicon wafer using polysilicon springs. A differential capacitor measures the deflection of the structure and this is translated into a pulse-width-modulated output signal. Figure 1 shows a typical output signal of the accelerometer. The acceleration is expressed as a ratio between times T1 and T2 and is given by:

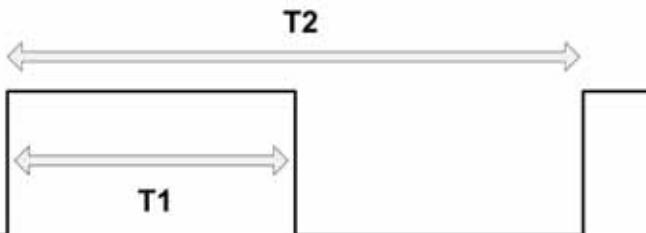
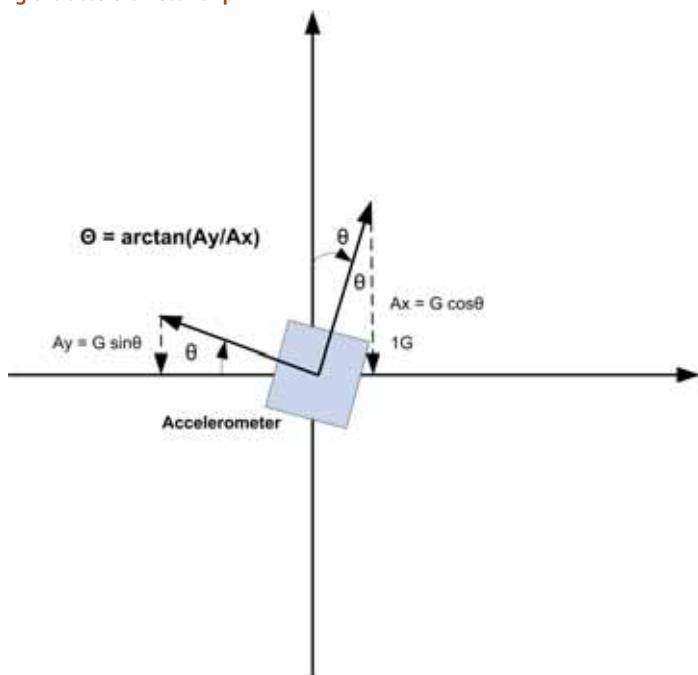
Figure 1: Pulse-width-modulated accelerometer output**Figure 2:** Tilting the accelerometer chip

Figure 4: The AccelBoard



$$\text{Acceleration} = 8(T_1/T_2) - 4 \quad (1)$$

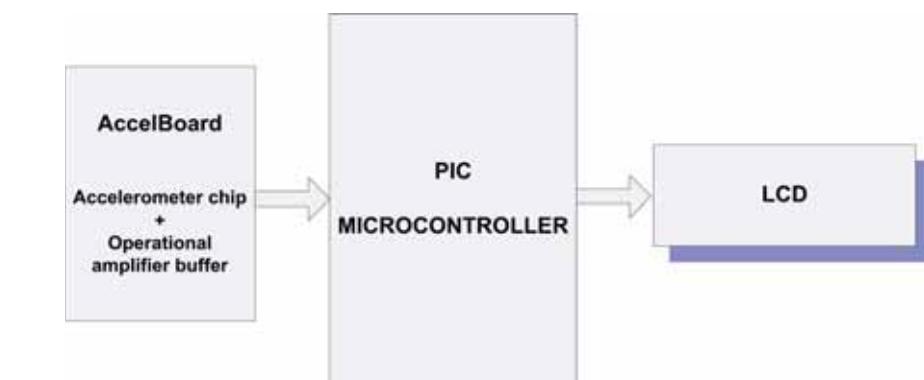
When $T_1 = T_2 = 0.5$, the acceleration is nominally 0G. In microcontroller-based applications, times T_1 and T_2 can easily be measured using on-chip timers. Because the ADXL202 is a 2-axis accelerometer, acceleration perpendicular to the 2-axis can not be detected. To measure acceleration in three dimensions, additional 2-axis accelerometers should be mounted at an angle to each other.

ADXL330 is a 3-axis solid-state accelerometer with a range of $\pm 3G$. The chip provides three analogue outputs, one for each axis, and is available in $4 \times 4 \times 1.45\text{mm}$ 16-pin package. ADXL330 is a very low-power chip and operates with a supply voltage in the range 1.8V to 3.6V. The bandwidth of the device can be selected by connecting external capacitors to the output pins.

The ADXL330 output is ratiometric, meaning that the sensitivity varies proportional to the supply voltage. At $V_s = 3.6\text{V}$, the output sensitivity is typically 360mV/G. At $V_s = 2\text{V}$, the output sensitivity is typically 195mV/G. The 0G output is also ratiometric, so the zero G output is nominally equal to $V_s/2$ at all supply voltages. It is recommended to calibrate the output at the working voltage for accurate results.

The outputs of the ADXL330 are normally connected to the A/D converter inputs of a

Figure 3: Block diagram of the inclinometer device



microcontroller. Then, knowing (or calibrating) the sensitivity of the device we can calculate the actual value of the measured acceleration in units of G. One of the methods of calibrating an accelerometer is known as the "Four Point Tumble". In this arrangement the accelerometer is mounted on a motor (or some other rotating apparatus) which rotates the accelerometer in 90-degree steps so that the acceleration at different axis can be measured and used in future calculations.

Although accelerometers measure the acceleration due to gravity directly, we can use them to measure the speed and position of a moving object, or the tilt angle of an object.

The speed can be measured by integrating the measured acceleration data, using a numerical integration technique. For example, using the trapezoidal rule, we can calculate the change in speed as follows:

$$v(t) = 0.5 * [G(t) + G(t-1)] * t \quad (2)$$

where t is the time, $v(t)$ is the change in speed, and $G(t)$ and $G(t-1)$ are the acceleration values at times t and $t-1$ respectively. An example is given below to show how the speed can easily be

determined from the measured acceleration data.

Example

Assume that the acceleration of a robot is measured using an ADXL330 accelerometer and the data values are as given in Table 4. Calculate the speed of the robot using numerical integration.

Using Equation 2 step by step we obtain the speed as shown in Table 5.

Once we obtain the speed, we can determine the position by integrating the speed data. It is important to realise that the sensor errors can accumulate and cause large errors in position calculations, making the double integration useless without an independent position check and position correction method.

Another important application of accelerometers is in the measurement of tilt angle. Assuming the accelerometer chip is tilted in the x-y plane by θ degrees (see Figure 2), we can determine the tilt angle by measuring the acceleration G_x in the x direction and G_y in the y directions using the following equation:

$$\theta = \tan^{-1}(G_y / G_x) \quad (3)$$

TIME (SECONDS)	ACCELERATION (CM/S ²)
0.0	0
0.1	100
0.2	110
0.3	120
0.4	130
0.5	135
0.6	140
0.7	145

Table 4: Acceleration of the robot

TIME (SECONDS)	ACCELERATION (CM/S ²)	CHANGE IN SPEED(CM/S)	SPEED(CM/S)
0.0	0	-	0
0.1	100	5	5
0.2	110	10.5	15.5
0.3	120	11.5	27
0.4	130	12.5	39.5
0.5	135	13.25	52.75
0.6	140	13.75	66.5
0.7	145	14.25	80.75

Table 5: Speed of the robot

Figure 5: Circuit diagram of the AccelBoard

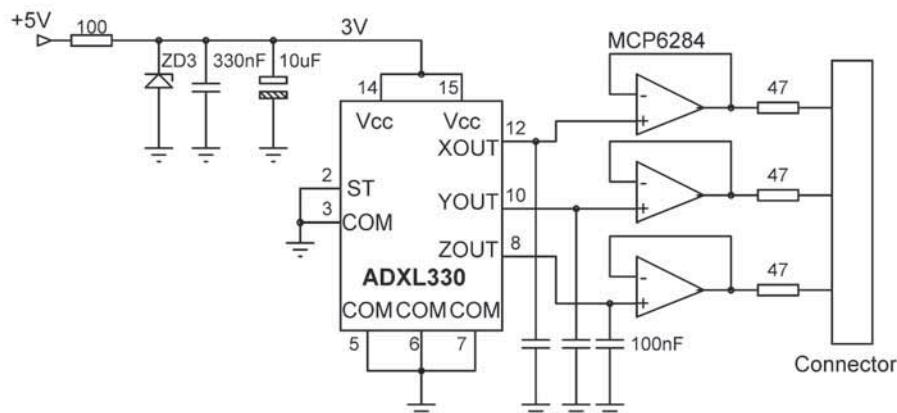


Figure 6: Circuit diagram of the inclinometer

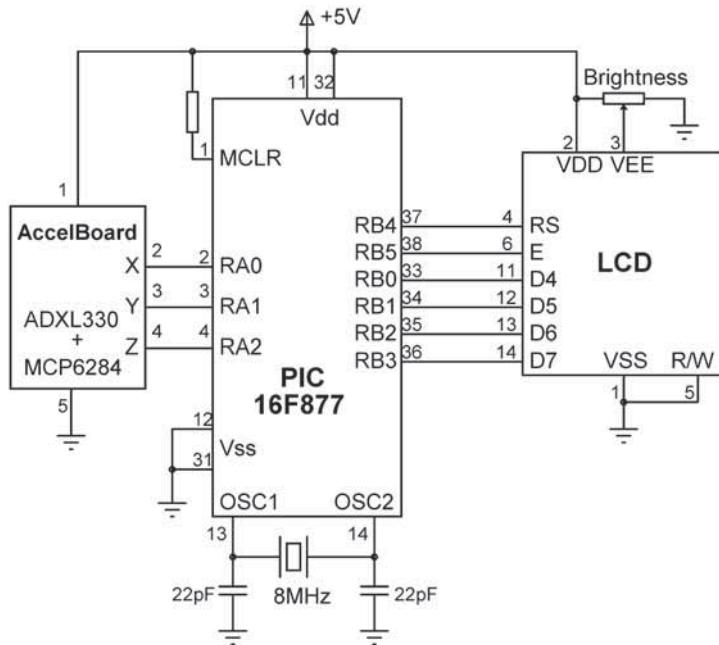
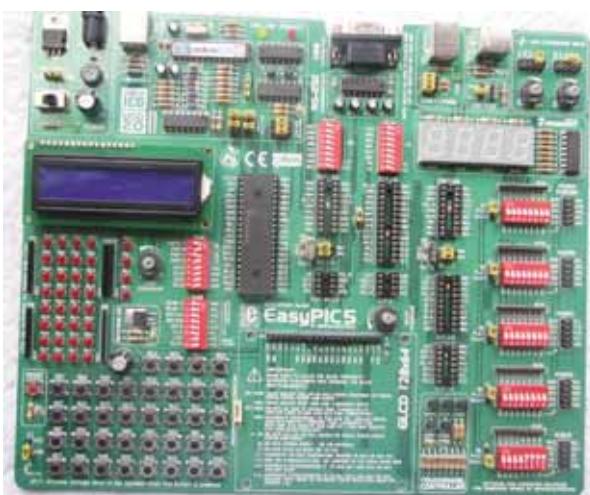


Figure 7: The EasyPIC 5 development board



Equation 3 is used in the inclinometer device whose design is discussed here.

Design of a Microcontroller-Based Inclinometer

This section describes the design of a microcontroller-based inclinometer device using the ADXL330 accelerometer chip and with LCD display. The device can easily be used to measure tilt angles.

The block diagram of the inclinometer device is shown in Figure 3. A small board known as AccelBoard (see Figure 4) is used to sense acceleration in 3-axis. This board, manufactured by mikroElektronika (www.mikroe.com), contains an ADXL330 type accelerometer chip and MCP6284 type (www.microchip.com) operational amplifiers, configured as a voltage follower buffers. Use of the AccelBoard greatly simplifies the design of accelerometer-based projects. Figure 5 shows the circuit diagram of the AccelBoard. Note that the ADXL330 accelerometer chip operates with a voltage in the range 1.8V to 3.6V and this voltage is obtained from +5V using a Zener diode on the AccelBoard.

A PIC microcontroller receives analogue data from the AccelBoard and calculates the tilt angle of the board. This angle is then displayed on the LCD. The hardware of the inclinometer device is relatively simple. The circuit diagram of the device is shown in Figure 6. The x,y and z analogue outputs of the AccelBoard are connected to A/D input pins RA0, RA1 and RA2 of a PIC16F887 type microcontroller respectively. The microcontroller is operated from an 8MHz crystal. A 2 row by 16 column LCD is connected to PORT B of the microcontroller to display the measured tilt angle.

The Construction

The inclinometer device was constructed using the EasyPIC 5 development board (see Figure 7), manufactured by mikroElektronika. EasyPIC 5 is a popular low-cost PIC microcontroller development board with the following basic features:

- On-board USB microcontroller programmer
- In-circuit debugger
- RS232 interface
- 36 LEDs
- 36 push-button switches
- 7-segment display
- Sockets for LCD and GLCD
- Support for 8 pin to 40 pin PIC

Figure 9: The program of the inclinometer

```

ACCELEROMETER BASED INCLINOMETER

The program is based on using a PIC16F887 microcontroller and a ADXL330 type
accelerometer chip. The inclination angle is measured and displayed on an LCD.

Author: Dogan Ibrahim
Date: July, 2010

// Lcd pinout settings
sbit LCD_RS at RB4_bit;
sbit LCD_EN at RB5_bit;
sbit LCD_D7 at RB3_bit;
sbit LCD_D6 at RB2_bit;
sbit LCD_D5 at RB1_bit;
sbit LCD_D4 at RB0_bit;

// LCD Pin directions
sbit LCD_RS_Direction at TRISB4_bit;
sbit LCD_EN_Direction at TRISB5_bit;
sbit LCD_D7_Direction at TRISB3_bit;
sbit LCD_D6_Direction at TRISB2_bit;
sbit LCD_D5_Direction at TRISB1_bit;
sbit LCD_D4_Direction at TRISB0_bit;

signed int x_acc,y_acc,z_acc;
signed int ZeroGx,OneGx,ZeroGy,OneGy;
signed int Counts_PerG_x, Counts_PerG_y;
float Gx,Gy,angle;

// Read acceleration (G) in 3-axis
// Read_Acceleration()
{
    x_acc = Adc_Read(0);
    y_acc = Adc_Read(1);
    z_acc = Adc_Read(2);
}

// Initialize the A/D converter
// Init_ADC()
{
    ANSEL = 0x07;
    ANSELH = 0;
    TRISA = 0x07;
    ADCON0 = 0x81;
    ADCON1 = 0x80;
}

void main()
{
    unsigned char txt[]="Angle= ";
    Init_ADC();                                // initialize A/D converter
    Lcd_Init();                                // Initialize LCD
    ZeroGx = 384; OneGx = 465;                  // define accelerometer parameters
    ZeroGy = 380; OneGy = 460;                  //
    Counts_PerG_x = OneGx - ZeroGx;            //
    Counts_PerG_y = OneGy - ZeroGy;            //

    for(..)                                    // Endless loop
    {
        Read_Acceleration();                  // Read acceleration
        Lcd_Cmd(LCD_CLEAR);                  // Clear LCD
        Lcd_Out(1,1,"Inclinometer");        // Display "Inclinometer" on row 1
        Gx = (float)(x_acc - ZeroGx)/Counts_PerG_x; // Calculate Gx
        Gy = (float)(y_acc - ZeroGy)/Counts_PerG_y; // Calculate Gy
        angle = atan2(Gy,Gx);                // Tilt angle in radians
        angle = angle*180.0/3.14;             // Convert to degrees
        FloatToStr(angle,txt+6);             // Convert to string
        Lcd_Out(2,1,txt);                   // Display Tilt angle
        Delay_Ms(500);                     // Wait 0.5 seconds
    }
}

```

Figure 8: Operation of the inclinometer device

```

BEGIN
    Initialize A/D converter
    Initialize LCD
    Define accelerometer parameters
    DO FOREVER
        Read x,y,z acceleration
        Clear LCD
        Display "Inclinometer" on 1st row
        Calculate tilt angle in degrees
        Convert tilt angle to string
        Display tilt angle on 2nd row
        Wait 500ms
    ENDDO
END

```

microcontrollers

- PC keyboard connector
- Connectors for external port interfaces.

EasyPIC 5 is a fully integrated development board where a program can be developed and compiled on a PC and then downloaded to a PIC microcontroller via the on-board USB programmer. The board also incorporates an in-circuit debugger hardware, making it easy to debug software during the development cycle.

The AccelBoard was connected to the EasyPIC 5 development board via 10-way IDC connector positioned on the top right-hand side of the board.

The Software

The inclinometer software was developed using the mikroC compiler. Before developing the software it was necessary to calibrate the accelerator chip for accurate results. The calibration process can be done as follows:

- Connect the AccelBoard to analogue inputs of a microcontroller and connect an LCD to the microcontroller.
- Write a program to display the A/D output from all 3-axis on the LCD.
- Place the AccelBoard parallel to Earth's surface. This arrangement will give 0G values for x and y, and 1G value for z-axis. Note the x, y, z readings and call them ZeroGx, ZeroGy and OneGz respectively.
- Place the AccelBoard such that x-axis is vertical with x-label up. This arrangement will give 0G value for z-axis and 1G value for x-axis. Call the readings ZeroGz and OneGx respectively.
- Place the AccelBoard such that the y-axis is vertical with y-label up. This arrangement will give 1G value for y-



Figure 10: A typical output from the inclinometer

axis. Call this value OneGy.

- Calculate the “counts/G” in each axis as per:
 $\text{Count_Per_Gx} = \text{OneGx} - \text{ZeroGx}$
 $\text{Counts_Per_Gy} = \text{OneGy} - \text{ZeroGy}$
 $\text{Counts_Per_Gz} = \text{OneGz} - \text{ZeroGz}$
- The acceleration along an axis in terms of G can now be calculated by reading the A/D value (ADC), subtracting the oG value and then dividing by the “counts/G” value. As an example, the acceleration in x-axis at any time can be calculated from:

$$\text{Gx} = (\text{ADC} - \text{ZeroGx}) / \text{Counts_Per_Gx}$$

The tilt angle (in radians) is easily calculated by finding the acceleration in x and y directions and then by using the function “atan2” to calculate the angle:

$$\text{Tilt_Angle_Radians} = \text{atan2}(\text{Gy} / \text{Gx})$$

or:

$$\text{Tilt_Angle_Degrees} = \text{Tilt_Angle_Radians} * 180.0 / 3.14$$

Figure 8 shows operation of the inclinometer device as a PDL. The program of the inclinometer is given in Figure 9. At the beginning of the program the A/D converter is initialised by calling to function `Init_ADC()` and port pins RA0, RA1, RA2 are configured as analogue inputs. Then the LCD is initialised by calling function `LCD_Init()`. The accelerometer parameters calculated earlier during a calibration process are then defined. The program then enters an endless loop.

Inside this loop the acceleration data is read from all 3-axis by calling to function `Read_Acceleration()`. The acceleration in x

direction (Gx) and the acceleration in the y-direction (Gy) are calculated as described earlier. The tilt angle is calculated in radians using Equation 3 and function `atan2`. This angle is converted into a string in degrees and is displayed on the second row of the LCD by calling to built-in function `Lcd_Out()`. The program waits for 500ms and then the above process is repeated forever.

A typical output from the inclinometer is shown in **Figure 10**.

Applications

Accelerometers are currently used in many domestic, commercial and industrial applications. The device described in this article can be used to measure tilt angles easily and accurately.

In commercial and practical applications the calibration process can be offered as an option to the user and the calibrated parameters can be stored in the non-volatile EEPROM memory of the microcontroller. ●

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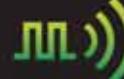
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THE ELECTRONICS BEHIND LIGHTING – PART 2

HAKKI CAVDAR FROM THE KARADENIZ TECHNICAL UNIVERSITY IN TURKEY PREPARES THIS FIVE-PART SERIES ON LIGHTING ELECTRONICS – THE FUNDAMENTALS, THE TOPOLOGIES AND THE TYPES OF BALLAST CIRCUITS USED. THIS SECOND PART DETAILS THE MAIN CONVERTER STRUCTURES USED IN LIGHTING ELECTRONICS

The electrical characteristics of various lamps are different from each other. Each type of lamp, however, needs operating voltage, certain wattage, frequency, alternating or direct current, even though these may differ from one another. For example, although fluorescent lamps work with AC current, LED lamps work with DC current; HID need AC current with low frequency, but halogen lamps need high frequency.

Lighting electronics circuits belong to the power electronics group, since they include power converters, of which the DC-DC group or converters are widely used. They convert the unregulated DC input into a controlled DC output at a desired voltage, current and power level.

The main circuit groups in lighting electronics can be divided into to three groups:

- 1) DC-DC converters: Buck, Boost, Buck-Boost, Cuk, Sepic.
- 2) DC-AC inverters: Half Bridge converter, Full Bridge Converter.
- 3) AC-DC inverters: Flyback switching mode power supply (SMPS).

With all converters and inverters, the average DC output voltage or current is controlled by adjusting the switching durations: switch on and switch off, using closed feedback loop. A method that controls the output voltage employs switching at a constant frequency, called PWM (pulse width modulation). PWM is the main control technique used in power and industrial electronics, but in lighting electronics also.

In PWM, the switching element (a power MOSFET, transistor or IGBT) is driven with a PWM signal which includes adjustable duty ratio at the constant switching time period

$$D = \frac{t_{on}}{t_{on} + t_{off}}$$

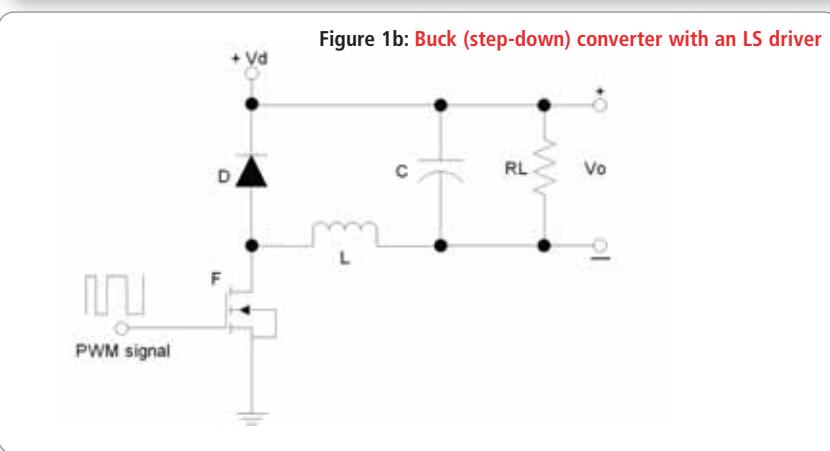
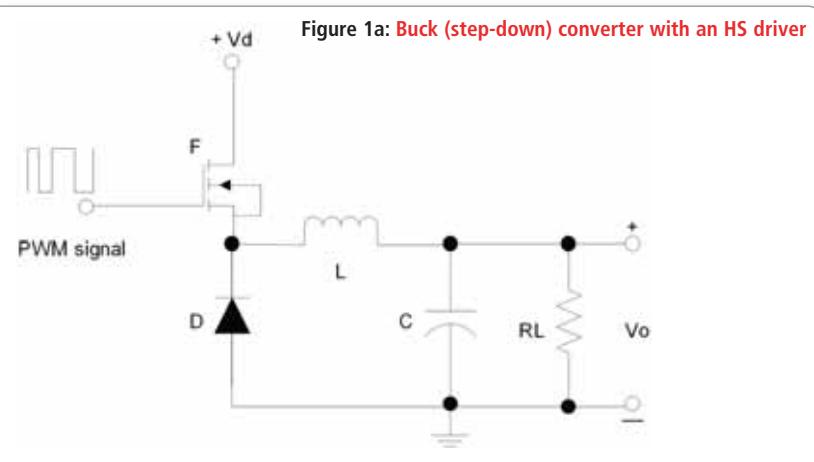
All converters and inverters must include a Low Side (LS) driver or a High Side (HS) driver, as the switching process needs a low-side or a high-side switch. If the switching

element is in between the load and the ground terminals, it is a low-side switch and it needs an LS driver. This type is easier to drive than an HS driver, as the ground level, or terminal, of the control circuit and the power converters is the same.

When the switching element is in between V_d (the DC voltage source) and the load, this then is an HS switch. This driver type is more difficult to control than an LS driver due to the different ground levels used for the control and power circuits.

Buck (Step-Down) Converter

Step-down (Buck) converters produce a lower average output voltage than the DC input voltage, V_d . The basic Buck converter



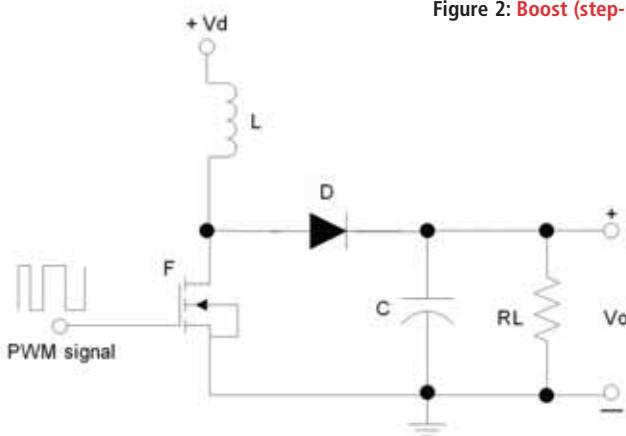


Figure 2: Boost (step-up) converter

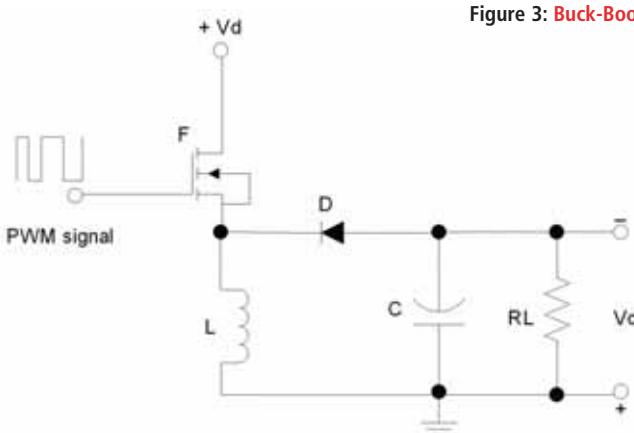


Figure 3: Buck-Boost converter

with a power MOSFET is shown in Figure 1.

A Buck converter has an HS switch and needs an HS driver (shown in Figure 1a, whilst an LS driver is shown in Figure 1b).

An HS or LS driver may be designed using a closed feedback loop PWM. Although the topology used in Figure 1a has the advantage of having the same common terminal between V_d and V_o , it still requires an HS driver. Likewise, the topology in Figure 1b needs the LS switch and the LS driver, but the common terminal is different between V_d and V_o .

If the power MOSFET is on for a time duration t_{on} , the MOSFET conducts current through to the inductor L, and the diode becomes reverse-biased. When the MOSFET is turned off, due to the inductive energy storage, the inductor current continues to flow in the same direction via the forward-biased diode, D. So, the current continues in the same direction and the output voltage has the same polarity for both modes. This means that the output voltage is the DC. The output voltage V_o is given in Equation 1. The capacitance value C is chosen to be large enough so that the output voltage has a low ripple. The required L and C can then be calculated using Equations 2 and 3.

$$V_o = [DV_d + (1 - D)V_{Don}] / (1 + r_{DSon} / R_L) \quad (1)$$

$$L = \frac{D(1 - D)[R_L(V_d - V_{Don}) + kV_o r_{DSon}]}{kV_o f_s} \quad (2)$$

$$C = \frac{D(1 - D)(V_d - V_{Don})}{8f_s \Delta V_o [Lf_s - D(1 - D)r_{DSon}]} \quad (3)$$

where V_{Don} is the diode's voltage and r_{DSon} is the resistance of the MOSFET in the ohmic mode; k is the fraction on the ripple of the output current and f_s is the switching frequency; ΔV_o is the ripple factor at the output voltage.

A Buck converter is suitable for applications using LED drivers and HID lamps, as both lamps operate at the voltage level which is smaller than the rectified main AC supply voltage levels.

Boost (Step-Up) Converter

The output voltage is always greater than the input voltage. When the MOSFET is on, D is reverse-biased, thus isolating the output stage. The input supplies energy to the inductor. When the MOSFET is off, the output stage receives energy from the inductor, as well as from the input.

A Boost converter uses an LS switch, so it needs an LS driver. A well-known application for a Boost converter is a power factor corrector (PFC), but at the same time it is also used in lighting electronics if the DC supply voltage is smaller than the lamp voltage. For example, DC batteries and solar cells produce low voltage levels, so the supply voltages must be increased via Boost converters.

A Boost converter is shown in Figure 2. The values of the components in this circuit can be calculated using Equations 4-6.

$$V_o = \frac{V_d [1 - (1 - D)(V_{Don} / V_d)]}{(1 - D)[1 + (r_{DSon} / R_L) / (1 - D)^2]} \quad (4)$$

$$L = \frac{D(1 - D)[(1 - D)(1 + V_{Don} / V_o)R_L + kr_{DSon}]}{kf_s} \quad (5)$$

$$C = \frac{V_o D T_s}{\Delta V_o R_L} \quad (6)$$

where T_s is the period of the switching frequency and the other parameters are the same as with the Buck converter discussed earlier.

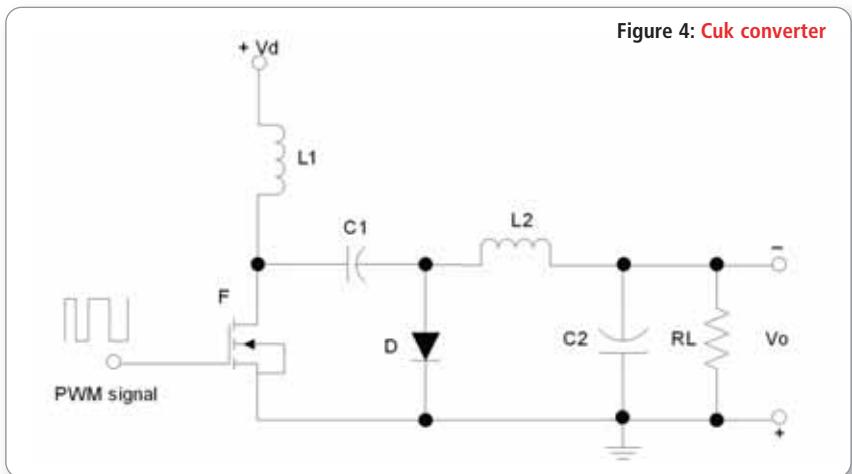


Figure 4: Cuk converter

Buck-Boost Converter

The output voltage (V_o) can be adjusted to be either lower or higher than the input voltage (V_d) (a Buck-Boost converter is shown in Figure 3). This converter behaves as a Boost converter if $D > 0.5$ and as a Buck converter if $D < 0.5$. It has a negative polarity output in respect to the common terminal. It can be used for loads that need to have time-variable voltages.

Sometimes the load voltage needs to be higher or lower than the input DC voltage. In lighting electronics, HID lamps need variable operating voltage at the triggering period. Also, LED drivers can be designed with their output voltages to be higher or lower than the input DC voltages.

A Buck-Boost converter needs an HS driver. The values of V_o and L can be calculated by using Equations 7 and 8. The capacitance C is the same as the value used in the Boost converter. Q is the quality factor of the inductor.

$$V_o = \frac{-DV_d[1 - (1 - D)(V_{Don}/V_d)/1/D]}{(1 - D)[1 + (r_{DSon}/R_L(1 - D))/(1/(1 - D))]} \quad (7)$$

$$L = \frac{D(1 - D)[kr_{DSon}V_0 - (1 - D)R_L(V_d - V_o + V_{Don})]}{kV_o f_s [Q - 2\pi D(1 - D)]} \quad (8)$$

Cuk and Sepic Converters

The specifications of the Cuk converter (see Figure 4) are similar to that of the Buck-Boost converter. It also has negative polarity regulated output voltage. The main advantage here is that it needs an LS switching-power MOSFET compared to a Buck-Boost converter.

A Sepic converter is a type of DC-DC converter that allows the output voltage to be greater than or less than the input voltage. A Sepic converter is similar to a traditional Buck-Boost converter, but has the advantage of having a non-inverted output. The output voltage is of the same polarity as the input voltage.

Cuk and Sepic converters are useful in applications where a battery voltage can be above or/and below that of the regulator's intended output. Both converters do not find large uses in lighting electronics, so we will not go into a detailed explanation. However, to find out more about these, you can pick up any literature describing designing steps and realization.

Half Bridge Inverter

A Half Bridge (HB) inverter is one of the most popular methods in inverting DC to AC. The AC output voltage can be designed at any desired frequency which is determined by a triggering signal at the FETs' pins.

F1 is the high switch and F2 is the low switch. Both power MOSFETs should be driven with different logic levels at the same time instant (Q and \bar{Q}). So a half-bridge inverter needs a driver that produces both HS and LS signals. The output voltage level is adjusted by the L , C and R_L elements. The transfer function of the HB inverter

in the s-domain can be calculated with Equation 9.

$$\frac{V_o(s)}{V_i(s)} = \frac{sR_LC}{s^2LC + sR_LC + 1} \quad (9)$$

An HB inverter is a most known candidate topology for the fluorescent lamps. Fluorescent lamps operate with a high frequency AC voltage and the different voltage level related to the lamp specifications.

Finally, the voltage across the RL has the high frequency and pure sine wave with a 1.41 crest factor. HB inverters may be used for the fluorescent lamp ballast, halogen lamps and the HID lamps, especially HF-HID ballasts.

Full Bridge Inverter

A Full Bridge (FB) inverter is shown in Figure 6. It has four power MOSFET switches, of which two are LS and the others are HS. F1-F4 and F2 and F3 are all driven with the same logic, but differently from each other.

The circuit includes an R-L-C serial resonance section as with an HB inverter. The output voltage of FB is twice that of an HB inverter. The voltage transfer function and resonance frequency are the same with an HB inverter. This topology can be used with HF fluorescent and halogen lamps, and HID ballasts. On the other hand, it can also be useful for DC-AC inverting applications.

Figure 5: Half-Bridge inverter with power MOSFET switches

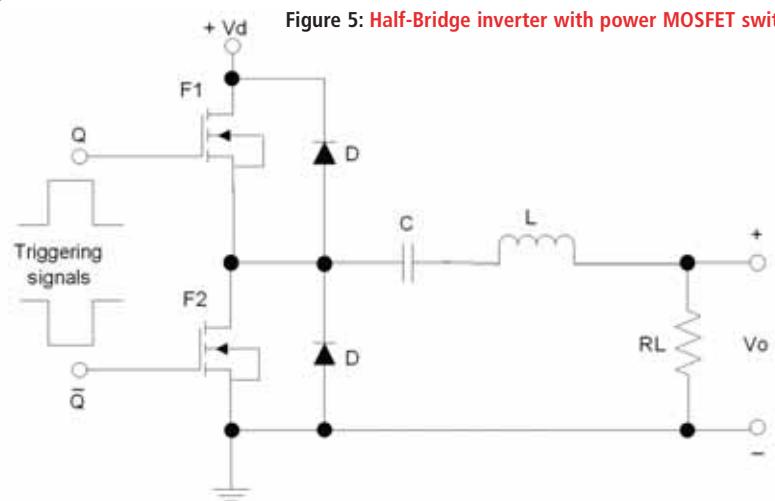
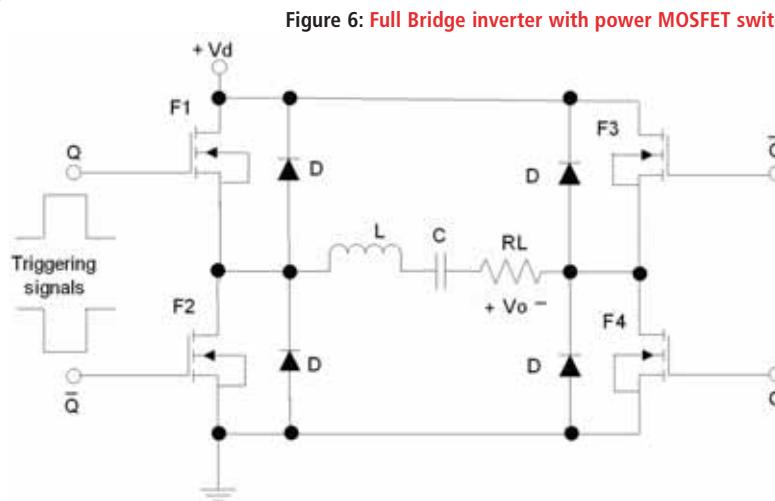


Figure 6: Full Bridge inverter with power MOSFET switches



Flyback Switching Mode Power Supply

Flyback is the most popular topology in switching mode power supply (SMPS) applications. It switches the DC voltage over the primary winding of the transformer using an LS type power MOSFET switch. The output voltage is taken from the secondary winding of the transformer.

Due to using the transformer's output, it has to be isolated from the mains. This is the main advantage of the flyback topology and, as such, it is used in isolated ballasts in lighting electronics, for example indoor LED lamp applications. The output may be selected in constant voltage (CV) or constant current (CC) mode.

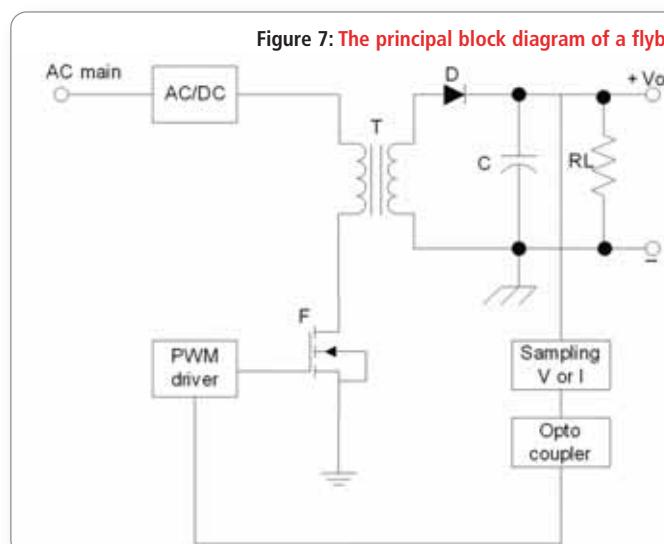
The output voltage or current levels, or both, can be adjusted using a closed loop-PWM controller. An output sample can feed into a PWM driver via the optocoupler, as the common terminals, mains and output side are not at the same reference.

The design of the transformer T is of importance here; it should be designed using the optimum switching frequency, turn ratio and power rates, but also the magnetic materials used should be considered too. The principal block diagram of a flyback SMPS is shown in Figure 7.

Detailed Design Information

Every topology needs detailed design information. We've looked at several topologies with their basic specifications. In the design stages, the specifications of the power MOSFETs, diodes and, even, magnetic materials are very important. Also, some protection circuits, such as a snubber, should be added to these circuits.

Figure 7: The principal block diagram of a flyback SMPS



On the other hand, the analog and digital IC manufacturers have been producing very useful components for power converters, used specifically in lighting electronics applications. The main manufacturers include Texas Instruments, ST Microelectronics, Linear Technology, Supertex, ISYS, Power Integrations, IXYS, International Rectifier, ON Semiconductor, Philips, National Semiconductor, Micrel, Fairchild, Maxim and Macroblocks among others. ●

This series continues in the next issue. If you missed Part 1, you can order the digital copy of this issue on line at www.electronicsworld.co.uk

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Device User EXPERIENCE

IN THIS THREE-PART SERIES MIKE HALL OF MICROSOFT DISCUSSES THE CURRENT TRENDS IN HARDWARE, SOFTWARE AND EMERGING TECHNOLOGY THAT AFFECT THE EMBEDDED DEVICE DEVELOPER

In the last two issues of Electronics World magazine we already talked about some of the challenges with getting a device “connected”, and how trends in silicon, hardware and software can cause challenges for developers wanting to bring smart, connected devices to market. In this article, we will focus on the device user experience.

User experiences have evolved over time, from command line input, through 2D graphical interfaces with simple input/output devices, to devices that support voice input, touch and multitouch and gesture, and 3D user interface. Users expect their device user experiences to be responsive, animated, fluid, immersive and intuitive. Note that we’re talking about the user’s experience, not just the user interface. The overall experience obviously includes the user interface (what the user sees), but also includes how the user interacts with the device, the device navigation model (using input and output devices) and how the user configures settings/preferences and connects to other devices.

The first view a user has of a new device is probably the device’s shell or application launcher (note that some

devices boot to a single application, which could be thought of as the shell). The application or shell can be divided into two discrete technology blocks. These are the user interface (what the user sees) and the application logic (the glue or business logic of the application).

Separating user experience from underlying logic is not new; the concept of Model View Controller has been around for some time and can be clearly seen exposed through programming models such as Microsoft Foundation Classes, which divides an application into a series of discrete classes: Application, Document, View, Frame, etc, and Silverlight, which cleanly separates user interface design and underlying application development to the point where the designer and developer tool chains also stand alone.

By cleanly separating user interface design and application code development, we can create two parallel development paths, one for user experience and one for underlying application/business logic. This has the benefit of enabling designers to work on the look, behaviour, brand and emotional connection for the given user experience, and the software developer to focus on the underlying functionality

for the application/shell. This would include connectivity, including working with Web Services, deployment, security and, of course, interaction with the user interface layer. Note that the software developer wouldn’t be creating or displaying user interface elements directly, but would be using elements of the user experience, which have been developed and exposed by designers.

Enabling designers to work independently from the software development process requires a set of tools that enables the designer to create the user interface elements in a form that can be easily consumed by the software developers, and as designers iterate on the design, make it easy for the developers to consume these changes and updates.

Let’s use Windows Embedded Compact 7 as an example of how designers and developers can work independently and, at the same time, “work together” to design and implement an immersive user experience. Designers would use Expression Blend to create a Silverlight project. The project would define the user experience without the designer needing to worry about the underlying code – the designer focuses on the look and feel of the experience, timelines,

Synchronous coding methods can block the user experience and make a device appear to be nonresponsive, which wouldn't be a great end-user experience

events, and animations and UI resources.

The developer is primarily interested in the events exposed from the user experience, and the callbacks exposed from the user interface that the developer can use to provide information to the end user. For example, the designer may create an animation that can be displayed to a user when a time-consuming process is taking place, such as pulling content from a Web service or parsing data to be displayed to the user. The developer

simply needs to know that the animation exists and then call into it. The developer would use tools such as Visual Studio and Platform Builder to integrate the designer-generated project into his or her embedded design.

For many devices, user experience and connectivity are tightly coupled. A device that relies on connectivity to pull data from Web services isn't particularly useful when there isn't a data connection, so the ability for a device to cache data locally can be important for partially connected devices.

We've already described that a clean separation of user experience (designer work) and the underlying application code (developer work) is important to provide the rich, immersive experience that end users demand. It's also important for developers to consider

how their code and the user experience work together: Synchronous coding methods can block the user experience and make a device appear to be nonresponsive, which wouldn't be a great end-user experience. It's better for a developer to consider using asynchronous coding methods to keep user experiences responsive and "alive". This is especially important as more of the applications and services that we use move to the cloud. ●

ABOUT MIKE HALL

MIKE HALL IS A PRINCIPAL SOFTWARE ARCHITECT in the Windows Embedded Business at Microsoft, working with Windows Embedded Compact and Windows Embedded Standard.

WHAT THE READERS SAY

THE CRYPTIC 'NEWSTRADE'

The March issue of EW (on sale here in Western Australia) has on Page 3 a somewhat cryptic note entitled "Dear Readers". I can only assume that "newstrade" is a UK organisation that distributes to retail newsagent shops, which implies that EW will no longer be available in UK shops and will only be available to UK readers via direct subscription.

Will this apply in Australia and other countries, or will it continue to be available in newsagent shops outside the UK?

Secondly, you have recently published material by the infamous Ivor Catt. I strongly suspect that many of the silent majority were induced to just stop buying Wireless World/Electronic World when Mr Catt's drivel was published extensively some years ago.

However, your recent article (in two parts) contributed by Mr Catt are one thing. In the March issue's Last Note (page 50) you have people commenting on the continued growth of the Chinese semiconductor market. Burkhard Vogel's comment is interesting, thoughtful and relevant. It adds value to the magazine. Dr Ibrahim's comment is also relevant and is value adding.

However, Mr Catt's comment is off on a tangent about ideas of his – his usual chip-on-shoulder whinge. We've seen it all before, it's not relevant to the topic and it lowers the value of the magazine.

If you can get something new out of Ivor Catt, and it's not about the World being too stupid to recognise his brilliance, fine. If not, please leave him out.

Alan Hampel

EDITOR REPLIES:

Indeed our magazine has now stopped being distributed by newstrade. That includes Australia and all other countries we publish into.

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Is the EV market finally TAKING OFF?

HUW MUNCER OF TE CONNECTIVITY IS ALWAYS ON THE ROAD. AS A SALES MANAGER, HE SEES WHAT ENGINEERS ASK FOR AND NEED, BUT ALSO HOW AN ENGINEER'S JOB HAS CHANGED OVER THE YEARS

In the electronics industry products are constantly evolving and presenting new challenges for design engineers, my customers. Sometimes applications, such as mobile phones, take off right away but others are slow to catch on. Take the case of the electric vehicle, or EV, market. Despite the fact that electric vehicles have been around for over a century, it is only now that EVs are becoming more common and that components are being specifically designed for them. When I began my career as an electronics salesman over 17 years ago, one of my first customers was designing EVs. I find it surprising how long it has taken to get a viable EV on the road.

I find that the main inhibitor for the speed of adoption of EVs is the lack of easy access to battery charging stations. I see it as a chicken-and-egg analogy; we won't really see EVs proliferate until we can find a charging station at every petrol station, supermarket and business premises and, of course, when we can use the same charging plug at any of these.

This brings up the issue of creating charging standards for EVs to help speed the growth of the market. Hopefully the EV market will apply lessons learned from the mobile apps market where electronics designers had to keep up with the requirements of ever-changing USB specifications (e.g. USB2.0,

USB3.0, etc.), which frustrated consumers who had to carry around different chargers for their cell phones, laptops, tablets, etc. As we are now seeing, this USB charging issue is being solved by the introduction of the universal USB Charging Specification V1.2 that allows consumers to use a single charger to power all mobile devices and helps design engineers develop devices for a single type of USB connector.

Similarly, although the EV market is creating standards for battery charging, EVs present further complications since not only the charging plugs but also the charging stations must be similar in a given country or

Household power of 120V (Level 1) is mostly found in North America, Japan and some areas of South America, and is non-existent in other parts of the world. Europe, Africa and Australia have 200-240V single-phase power for homes and businesses, which means that Level 2 charging can be done with a domestic plug. In parts of London, for instance, EV owners can use a domestic plug with a user-supplied 240V extension cord that requires no special connector.

In Europe, the Mennekes connector is the accepted standard EV connector. In North America the Society of Automotive Engineers (SAE) created the J1772-2009 standard connector. The Nissan Leaf and Chevy Volt are using a standardized plug and are participating in the US government's EV Project to install charging stations in major metropolitan areas.

Although inroads have been made, EV charging standards are still evolving and future connector formats may complicate things. And charging standards are just one type of roadblock to the growth of the EV market, other issues include:

- Cost of manufacturing the battery
- High cost of EV
- Charging range
- Recharging time
- Environmental concerns (recharging with “clean” renewable energy)
- Demographics
- Purchase behaviour
- Government policies

But for now, designers of electronics devices for EVs should welcome the news that governments, automakers and battery manufacturers are working together to develop EV charging guidelines. I hope I don't have to wait another 17 years to see this market finally take off! ●

OVERVIEW
OF THE DIFFERENT
TYPES OF CHARGING LEVELS can be
 found at CarStations.com. “*Electric Vehicle Charging Standards*” by Chase Ballew, December 4th, 2010
 (<http://carstations.com/electric-vehicle-charging-standards/>)

region. A 2010 article on the blog carstations.com provides a nice overview of the different types of charging levels that can be used for EV charging:

- Level 1 – You can plug into a 120V, 15 or 20A household electrical socket, usually used for golf carts and Neighbourhood EVs (NEVs).
- Level 2 – You can plug into a 208-240V household outlet for faster charging of EVs.
- Level 3 – You can charge a vehicle such as a Nissan Leaf to 80% in 28 minutes. Operating at up to 480V DC and 125A, it’s also known as DC Fast-Charge or DC Quick-Charge. This type of charging is now appearing in North America.

WHAT THE READERS SAY

WHAT ABOUT THE MATHEMATICS?

I note various readers' comments on Ivor Catt's series of articles in your May edition and that none of them are questioning the mathematics itself instead of the physics – why do you think this is?

Barry McKeown

Help Needed with Circuit

I have an old Realistic DX-160 Communications receiver with dial and pointer tuning. I want to incorporate an external frequency meter with a digital read-out. If I could buy one that would be fine; otherwise I'll have to make my own.

Can you recommend one I can buy? Otherwise can you supply me with a circuit to make my own?

Also, where in the receiver should I connect it?

N. Dewhurst

ELECTRONICS
WORLD
SURVEY

WE CONTINUOUSLY STRIVE
TO KEEP THE
MAGAZINE

AND ITS CONTENT OF HIGHEST
STANDARDS AND AS PART OF
THIS EFFORT WE'D LIKE TO MAKE
THIS PROCESS INTERACTIVE WITH
OUR READERS.

So, we have prepared a short survey that will help us see how we are doing but also which topics you would like to see discussed in detail in the future issues of Electronics World. To take part, please go online at <http://www.surveymonkey.com/s/XTN5VTK>.

To say 'Thank You' for participating, your name will be automatically entered into our prize draw to receive a free print subscription to Electronics World for a 12-month period. All successfully completed survey respondents will be entered into the prize draw and the winner chosen at random.

Playing with Figures

I very much enjoyed Ivor Catt's recent articles in the January and February editions of Electronics World magazine and the correspondence in the May issue (Letters) because we are getting close to a clear picture of what is needed to supplant the outmoded theories, and correspondents would like to see the best theory in EW because of the efforts of many over so many decades.

Of course, there is a lot more that we can write about, but I wanted to get to the essence as clearly as possible. I hope I have been able to do this effectively in an interesting way.

The oscilloscope photographs in Ivor Catt's articles in the January and February editions of Electronics World show clear evidence of bifurcation and period doubling, which are features of deterministic chaos in rotating fluids. New frequencies are produced every time a bifurcation occurs, and these accumulate up to infinity.

Libchaber and Maurer showed (1979) that the frequencies are multiples of the fundamental, but they did not state what this is. It is, in fact, Cvitanovic's constant, which has the negative value -1.865 510 774 712 034 3. When this value is used in $2\pi f$ it gives -11.721 349..., which is slightly higher than the value quoted for Planck charge 11.706 237 639 8 e^{-} . This makes sense because charge trajectories are not strictly circular; they are similar to the geometry of a coil of wire on a cylindrical former or a torus. The curvature can be evaluated by equating the square of $2\pi f$ to the reciprocal of the fine structure constant, which has the value 137.035 999 084 (Gabrielse and Hanneke, Physical Review Letters, 100, (120801), 2008). This gives a value for π of $\pm 3.137\ 542\ 214\ 307$

769 6, which is 0.13% lower than Ludolph's value 3.1415926...

When the lower value is used in $2\pi f$, however, it gives $\pm 11.706\ 237\ 613\ 809\ 798$ radians per second, which agrees with the figure above to 10ppb and is within the range ± 2 ppb.

Comparing signs, coefficients and units suggests that the units of charge are radians per second rather than Coulombs, which may presage the end of charge as we have come to know it. More alarming is the possibility that the fine structure coefficient has units, which suggest acceleration!

Current is a problem for several reasons, including renormalisation and the confusion created by relying on rationalised units like Planck units (see Google/Planck units (uselessness of!)). Cvitanovic units are far preferable, perhaps?

We can be confident of the analysis because the strength of coupling between an electric charge and a photon has been measured to be -0.085 424 55 (see Richard Feynman's book '*The Strange Theory of Light and Matter*', 1985), which is the reciprocal of -11.706 237 639 8. Feynman, like Feigenbaum, looked to see if π and e (Napier's) were involved in their respective areas of interest, but could not find any. This analysis has found π in both, and how they are related.

Readers interested in this area might like to play around with these figures, remembering that Feigenbaum made his stunning find using little more than a HP hand calculator. For example: when a trajectory bifurcates, what angles are involved? Try $\text{arcsecant } 1.865\ 510$, $\text{arcsec } (1.865\ 510)^2$; or see how 1.865 510 works in Planck's Law for electromagnetic radiation.

Tony Callegari

IF YOU WOULD LIKE TO COMMENT

on this subject or any other that you have read on in Electronics World magazine, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com

The publisher reserves the right to edit and shorten letters due to space constraints

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DEVELOPING VINCULUM-II BASED APPLICATION PROGRAMS – PART 2

JOHN HYDE FROM FUTURE TECHNOLOGY DEVICES INTERNATIONAL (FTDI) WILL IMPLEMENT A SERIES OF USB PROJECTS OVER THE COURSE OF SEVERAL EDITIONS OF *ELECTRONICS WORLD*

In this article we look a little deeper into the Vinculum-II RTOS and VOS, and develop some techniques for creating application programs for the Vinculum-II. I also introduce a Thread Activity Monitor that gives us a visual representation of VOS operation and will aid us in this endeavour.

Stage 4: The Mutex

The mutex is an RTOS mechanism used to provide MUTual EXclusion and, thus, stop multiple threads from accessing the same resource. The function `vos_lock_mutex` checks if a mutex is locked and, if it is locked, it waits for it to unlock before locking it again. If the mutex is not locked then the function locks it and returns. I insert a mutex into the `dprint` routine.

So what happens differently now that we have a mutex? Recall that the `HelloWorld` thread (see last issue of *Electronics World* magazine) was executing the `dprint` procedure when it was pre-empted by a timer interrupt; the `Blink` thread starts to run and it calls `dprint`. The `Blink` thread tries to set the mutex but discovers that it has already been set (by the `HelloWorld` thread, when it started executing the `dprint` routine). The `Blink` thread is blocked by the locked mutex so VOS starts `HelloWorld` running again. `HelloWorld` finishes its `dprint` operation and unlocks the mutex. VOS will now restart the `Blink` thread which sets the mutex again and continues with its execution of the `dprint` routine.

Stage 5: Thread Activity Monitor

We have covered some key concepts such as threads, priority, semaphores, pre-emption and mutexes. But most of the activity is happening within VOS and we don't get to see it! I created a Thread Activity Monitor to see the real time operation of VOS. The concept is simple: I will use an 8-bit IOPort and assign a bit to each thread. When the thread is running it will set this bit and when it passes control to VOS it clears this bit. I then attach a logic analyzer to this IOPort and I can capture thread activity in real time.

Using a Logic Analyser

I have used the USBee line of products (see www.USBee.com) for many years. In this article I will use the DX tool in logic analyzer mode to trace 8 signals initially (the DX supports 16 digital inputs and 2 analog inputs) and these are connected to the V2Eval board as shown in Figure 1. The DX collects



Figure 1: Connecting the USBee DX to the V2Eval board

data up to 24MHz and you can view this as say, 6 seconds across the screen or zoom in to show 6µs across the screen, choosing the zoom level to allow you to focus upon the level of detail important at the time. The trace can also be saved as a file and emailed to someone who then uses the USBee DX software as a viewer. I have used this ability countless times to show both clients and vendors some timing issue with a product.

We have driven IOPorts before and know that this requires the IOMUX and GPIO device driver. The LA pins need to be bidirectional since we do a read-modify-write operation to set or clear individual bits. So how do we handle bi-directional signals on a Vinculum-II? We have two choices: we could use a single IOPort and switch its direction at run-time (set IO to input for a read, then set to output before a write), or we could use two IOPorts with one set as a input and the other set as output. I tried both methods and concluded that using two IOPorts resulted in smaller code that was easier to explain. The Vinculum-II has five 8-bit IOPorts and, so far, I have only used 1 bit on one of the ports, so I decided that using two of the IOPorts for my LA function was OK.

Each thread is assigned an ID (how is described later) which is a single bit: 1, 2, 4, 8, 16, or 32 is enough for 6 threads. The `ThreadRunning` procedure will set the corresponding bit on the Logic Analyser port and the `CallVOS` procedure will clear it. I chose IOPorts C and D for my LA function and the pin routing is added in the `InitDevices` procedure within `initialize.c` and the attachment of two GPIO device drivers is covered in the `StartupDevices` procedure. You should review these now and note that this is 'more-of-the-same'. Yes, the bi-directional aspect is new but it follows the same format as previous IOMUX commands.

Open the Chapter8/Stage5 project and view `TAM.c` since this is the core of the Thread Activity Monitor. I show part of this code in Figure 2 (below) for convenience.

```
void ThreadRunning(BYTE ThreadID) {
    // The thread now has the CPU
    BYTE PortData;
    vos_dev_read(hDevice[LA_In], &PortData, 1, NULL);
    PortData |= ThreadID;
    vos_dev_write(hDevice[LA_Out], &PortData, 1, NULL);
}
```

Figure 2: The Thread Activity Monitor toggles IO pins

I felt it important that we understand the effect of TAM routines on the overall program performance. We are adding to existing code to increase observability and, as Hiesenberg stated, this will change the system that we are trying to measure. We don't want to change it significantly so we should measure the impact of the added code on system operation. Check that the first line of main.c is: #define Test_TAM 1.

This causes only the TAM_Test thread to be created, see line 96 to 102 of main.c. The vos_create_thread system call allows parameters to be passed into a thread; the fourth value is the byte count of values (we are just passing a byte) and the fifth and subsequent values are passed into the thread as parameters (we pass in a 1). The TAM_Test thread, also shown in Figure 3, simply calls our two TAM routines.

```
void TAM_Test(BYTE ThreadID) {
    // Test VOS response times just toggling the LA signals
    // Other tasks are not running for this test
    StartupDevices();
    while (1) {
        CallVOS(ThreadID);
        ThreadRunning(ThreadID);
    }
}
```

Figure 3: A test to understand the impact of the TAM code

Build, download and run Stage 5 and capture the activity on the IOPort using the USBee DX (or similar Logic Analyser). Figure 4 shows a close-up of the waveform I collected and also a view covering about 1.5ms. As seen, the thread activity signal is toggling at about 40µs – small enough such that it can be considered an insignificant impact to our program.

It is now time to look at the activity of our threads so stop the program and change the first line to be #Define Test_TAM 0. This will enable a new thread that I created for illustration purposes. MyIdleTask is a thread that uses 100% of the CPU – it toggles bit 7 of the LA port to show activity. I set the priority of this thread to be the lowest value, 1, so that it can be pre-empted by any other task. The VOS IdleTask has a priority of 0 and will not have the opportunity to run due to MyIdleTask. I have effectively replaced the VOS IdleTask with mine. Therefore, toggling on bit 7 of the LA trace will indicate that VOS is running MyIdleTask. Now check inside the 'do forever' loops of the Blink and HelloWorld threads. I added TAM instructions to produce activity on the LA port. I also added additional instructions within display.c to show when the mutex lock was ON and OFF – we will see the result in a moment.

Figure 5 shows a zoom-in detail of thread 1 = Blink operation. Note the time between the X1, X2 cursors is about 1ms. I saved this USBee file in the examples directory so that you can study it.

An overview would show that the program is spending > 99% of its time in the IdleLoop – we should expect this for such a simple example. The zoom-in detail shows that Blink started as a result of a timer interrupt and it locks the mutex while writing its data to LocalBuffer and then sending this on to the UART driver.

Stage 6: Adding Buttons

The V2Eval board has four user buttons and I chose SW3 and SW4. SW3 is connected to pin 14 of a 64-pin device which is IOBUS3 so this needs to be attached to bit3 or bit7 of an IOPort. Similarly SW4 is on pin 32 which is IOBUS20 so this needs to be attached to bit7 or bit3 of an IOPort.

The Vinculum-II has five 8-bit IO ports but note that PortB and PortA have additional capabilities with respect to interrupts. PortB includes the ability to wait for a rising, falling or changing edge on any of the 8 bits, so I chose PortB to handle my two buttons. Load the Stage 6 project and view initialize.c. Note

the added pin routing for SW3 and SW4 in InitDevices and the attachment of another instance of the GPIO driver to manage the buttons.

We now have four instances of the GPIO driver – VOS uses the same code block in each instance but will allocate a separate data area for each. Now view main.c, where I have added a Faster thread to manage SW3 and a Slower thread to manage SW4. I also removed the HelloWorld thread and the TAM_Test thread since they are not needed any more. The Vinculum-II has five interrupts that can be waited upon, four for individual bits on PortB and one for a change on PortA. If you have up to 4 buttons then connect them to PortB. The next eight buttons would be connected to PortA and some polling software will need to be added to discover which of these additional 8 buttons was pressed.

The Faster and Slower buttons modify a global variable, called Delay, that Blink uses as a parameter in vos_delay_msecs. Press SW3 and then SW4 to see the blinking period of LED3 change. You should also capture several seconds of LA trace and observe the running threads. My capture showed that the IdleTask still dominates – there is ample CPU power to do many more things.

I trust that this gives you some insight into the techniques of writing Vinculum-II based application programs. The integrated VOS forces a structure to the application program which makes it easier to modify and expand – we will see a linear growth in complexity of the applications in upcoming articles. ●

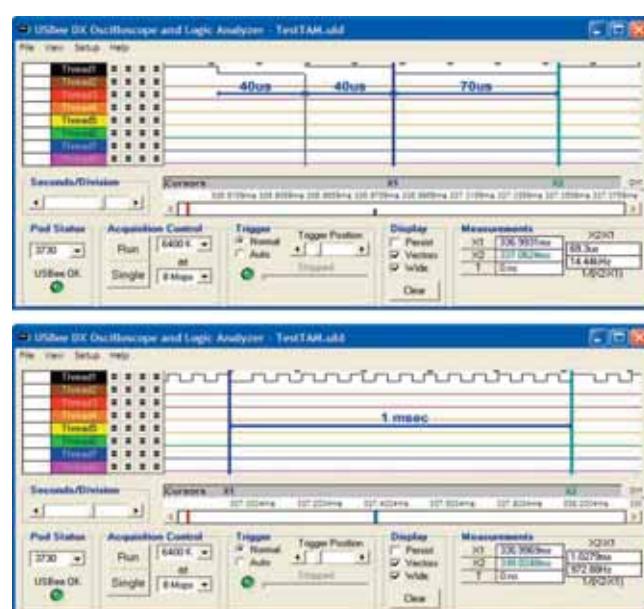


Figure 4: The TAM code is a minimal impact on performance

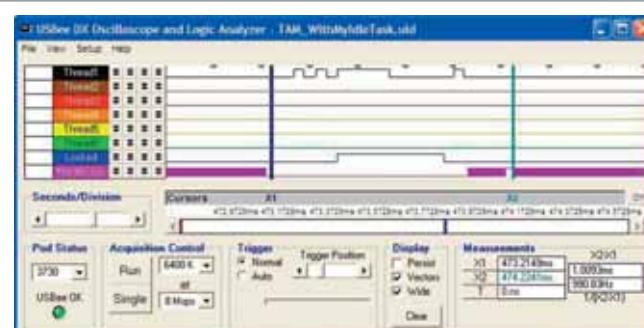


Figure 5: Detailed view of thread execution

New Smallest Double Pole Rotary Switch from knitter-switch

The MRS 8000 series from knitter-switch is a tiny rotary switch said by the company to be the smallest double pole rotary switch currently available.

Measuring just 9.9 x 9.9 x 4.5mm (L x W x H), the MRS8000 series is ideal for many applications including medical devices,

industrial automation control systems and measuring instruments.

The new MRS 8000 series switches are available with up to four positions in double pole configuration and up to eight in single pole. Customers can

specify horizontal or vertical shaft versions which can be flush or extended and knitter-switch can supply a wide variety of optional control knobs.

Versions of the MRS 8000 rotary switch are available for surface mount or for through-hole application and all feature gold-plated contacts, an operating temperature range of -40 to +85/+125°C (SMD) and a lifetime of 20,000 steps.

www.knitter-switch.com



HIGHLY INTEGRATED AUIR3330S INTELLIGENT POWER SWITCH

International Rectifier (IR) has introduced the AUIR3330S Intelligent Power Switch (IPS) with a proprietary active di/dt control feature that significantly reduces conducted EMI and switching losses to simplify design and reduce overall system cost in automotive motor drive applications.

The new 40V high-side device combines bootstrap regulator, charge pump and high-side driver into a single package to offer a highly integrated solution. The load can be driven up to 40kHz at 100% of duty cycle. Additionally, the AUIR3330S features

programmable over-current and over-temperature protection required by applications operating in harsh automotive environments such as pumps and fans. The AUIR3330S also features current sensing feedback, a diagnostic function, very low current consumption in sleep mode and ESD protection.

IR's innovative active di/dt control drastically reduces conducted EMI on the input supply without increasing switching losses, enabling a reduction in the size of the EMI filter and the heat sink for more efficient compact motor systems.

www.irf.com

Lane Electronics Announces "Break-Away" Fastening Micro38999 Connectors

Lane Electronics announces the 8BA series micro38999 circular connectors designed to suit the most demanding applications. Part of Souriau's new micro38999 family, these "Break-away" fastening connectors satisfy the increasing need for more compact, lighter connection solutions for military, aerospace and industrial applications.

The new micro38999 connectors are said to combine high performance and small size together with weight savings of as much as 50% when compared with regular MIL-DTL38999 Series III connectors.

Other models in the micro38999 range have screw and bayonet fastening systems.

The new connectors have removable crimp contacts which allow them to be wired or unwired on-site. Up to 26 contacts can be accommodated in a choice of five layouts.

Lane Electronics has available product in the classic Cadmium, Electroless Nickel and with non-reflective black zinc nickel protection to satisfy the latest RoHS directives.

www.flane.com



NATIONAL INSTRUMENTS INTRODUCES HIGH PERFORMANCE PXI DIGITISERS

National Instruments (NI) has released what it claims is the industry's highest bandwidth PXI digitiser, complementing the rapidly expanding suite of performance instrumentation available in PXI. Co-developed with Tektronix, the world's leading manufacturer of oscilloscopes, the NI PXIe-5186 digitiser employs *Tektronix Enabling Technology* to achieve up to 5GHz bandwidth and 12.5GS/s sample rates.

The company also announced the NI PXIe-5185, which delivers 3GHz bandwidth along with 12.5GS/s sample rate. Both digitisers are part of the National Instruments PXI-based hardware and software platform, which provides optimised performance for automated test applications.

Proprietary Tektronix performance oscilloscope ASICs in the



new digitisers provide the foundation for high-speed signal acquisition with low noise and high linearity, and are based on the highly-reliable IBM 7HP SiGe process. Whereas, National Instruments's proprietary technology delivers high-data throughput for faster test execution and precision multimodule timing and synchronisation for building high-channel-count, integrated test systems.

www.ni.com



Open-Source IDE with support for Linux, Mac OS and Windows Users

Microchip Technology launched its next-generation, open-source integrated development environment – the MPLAB X IDE – with cross-platform support for Linux, Mac OS and Windows operating systems.

There are number of high-performance features added to the new IDE, including the ability to manage multiple projects and tools with simultaneous debugging, an advanced editor, visual call graphs and code completion. In addition, MPLAB X supports the entire portfolio of 8, 16 and 32-bit microcontrollers – including all 800+ PIC microcontrollers, dsPIC digital signal controllers and memory devices.

MPLAB X is based on the Oracle-sponsored open-source NetBeans platform, which has an active user community that can contribute a wide range of enhancements and third-party plug-ins. In fact, Microchip customers can take advantage of a host of free NetBeans software components and plug-ins that exist today. Additionally, the NetBeans platform allows MPLAB X users to customize the IDE to suit their individual development needs.

www.microchip.com

LED BACKLIGHT DRIVER IC FOR MEDIUM AND LARGE DISPLAYS

Now available from Allegro MicroSystems Europe is a new multi-output WLED/RGB driver for backlighting LCD monitors and televisions.

The A8516 is a versatile and economical LED driver IC that will enable system designers to reduce component count and overall system cost. The device integrates a boost controller to drive an external MOSFET and six internal current sink channels capable of up to 80mA each, and channels can be combined together to achieve even higher currents.

The boost converter operates in constant-frequency (programmable) current-mode control.



The LED sink current is set by an external resistor (R_ISET), and PWM dimming allows LED currents to be controlled.

The A8516 incorporates protection against overvoltage, open or short-circuited LED string, and over-temperature conditions. A dual level cycle-by-cycle current limit function provides soft start and protects against overloads.

The A8516 is offered in a 24-pin TSSOP package (LP) or a 24-pin SOICW package (LB), with internally fused pins for enhanced thermal dissipation.

www.allegromicro.com

AEROFLEX ADDS AVIONICS WAVEFORMS TO S-SERIES SIGNAL GENERATORS

Following in the footsteps of the Aeroflex industry-standard 2030 Series avionics signal generator, Aeroflex Limited announces the addition of popular avionics waveforms to its S-Series signal generator family. All avionics authorities (civil or military), airfields, airframe manufacturers, aircraft systems manufacturers and military sub-contractors use avionics-specific signal generators to test important navigation functions.

The Aeroflex SGA analog signal generator with Option 6 adds internal generation of waveforms required for testing avionics functions. The new option includes waveforms for Instrument Landing Systems (ILS), VHF Omni-directional Radio (VOR), marker beacons and COM ID tones for airport identification. Avionics parameters are presented in the same form as described in the International Civil Aviation Organization (ICAO) standards.



The SGA with Option 6 offers an ideal single instrument solution for testing avionics receivers and airfield alarm monitors. Digitally generated modulating waveforms ensure excellent accuracy and stable performance under all operating conditions.

www.aeroflex.com

Amplifier Meets Performance Criteria for Best-in-Class Data Converters

Analog Devices introduced a differential RF/IF (radio frequency/intermediate frequency) amplifier for driving high-speed 12-bit to 18-bit A/D converters. The ADL5565 differential amplifier features 3dB bandwidth of 5GHz and achieves unprecedented distortion, noise and IP3/IP2 performance out to 300MHz. The ADL5565 amplifier is optimised for wide bandwidth, low distortion and low noise, and achieves industry-best HD3 and OIP3 distortion levels (-103dB and 51dBm at 100MHz; -95dB and 47dBm at 200MHz). The excellent distortion performance makes the ADL5565 ideal for applications in which high linearity and low noise are critical, including IF sampling receivers in wireless infrastructure applications, industrial instrumentation and defense electronics. The ADL5565 amplifier drives best-in-class high-speed converters, including ADI's new 16-bit, 250-MSPS AD9467 data converter, with little or no impact on overall A/D converter SFDR (spurious-free dynamic range) or IMD (inter-modulation distortion) performance. The device gain is pin-programmable using internal gain resistors, which allows for fixed gains of 6dB, 12dB, or 15.5dB. With only two external input resistors, any gain between 0dB and 15.5dB can be easily realised, making the new amplifier easier to configure and more cost effective than traditional operational amplifiers.

www.analog.com/rf

New 1.0mm Pitch Interconnects from Harwin Save Space on PCBs

Harwin is introducing a brand new range of 1.0mm pitch interconnects. The new M40 series consists of surface mount pin headers and sockets, providing a new cost-effective solution for secure and highly reliable PCB to PCB connections. Benefiting from a low profile design and a dual-beam contact system, the devices are aimed at design engineers seeking to reduce PCB sizes whilst not sacrificing connector reliability.

M40 series 1.0mm pitch interconnects are available in dual row format and feature gold plated phosphor bronze contacts, surface mount solder tails and location pegs. Contact counts range from 2 x 3 up to a maximum of 2 x 25 positions. All components come packaged in tape and reel format for fully automatic pick and placement.

A typical application for the new pin headers and sockets are mezzanine PCB assemblies. The small contact spacing of 1.0mm makes the interconnects ideal for use in confined spaces, such as handheld devices.

www.harwin.co.uk

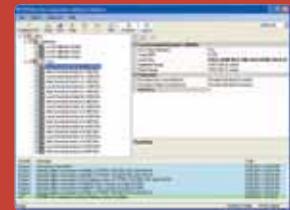
INDUSTRY'S FIRST COMPLETE MIPI M-PHY TEST SUITE

Agilent Technologies announced a comprehensive MIPI M-PHY test solution for mobile computing customers. The Agilent solution suite helps design engineers turn on, debug and validate all layers of their M-PHY devices, including physical and protocol layers, at speeds up to 5.8Gb/s.

The Mobile Industry Processor Interface (MIPI) Alliance is finalizing the M-PHY specification to allow development of faster, more reliable high-speed interfaces for mobile devices. M-PHY technology supports a broad range of applications, including interfaces for monitors, cameras, audio and video equipment, memory, power management and communication between baseband and RFIC components. The Agilent solution consists of oscilloscopes, protocol analyzers and exercisers, and bit error-rate testers (BERTs) using custom M-PHY stimulus software. Each instrument comes with custom M-PHY-ready software to support design teams through the entire product design process.

Accurate and automated MIPI M-PHY receiver testing is supported by Agilent's high-performance ParBERT 81250A for multi-lane testing and J-BERT N4903B for single-lane testing.

www.agilent.com/find/MIPI



Available from Microlease: Agilent Technologies's U8903A Audio Analyser

Available now to rent or lease from Microlease is the U8903A audio analyser. The system combines the functionality of a distortion meter, SINAD meter, frequency counter, AC voltmeter, DC voltmeter and FFT analyser with a low-distortion audio source.

On the bench or in a test system, its accuracy and versatility will help make an audible difference in the end product.

The U8903A is the next-generation replacement for the widely used 8903B audio analyser. To further ease the transition process, the U8903A audio analyser features a built-in code emulator which allows the U8903A to read the old R2D2 programming codes of the 8903B.

For more information, call +44 (0)20 84 200 200 or visit.

www.microlease.com



TE CONNECTIVITY OFFERS 0.6MM CL HIGH-SPEED CHAMP DOCKING SERIES CONNECTOR

To meet the increasing market demand for hybrid I/O connectors, TE Connectivity (TE) has introduced a 0.6mm CL (centerline) high speed CHAMP docking series connector.

The docking series connector is designed for high-density, low-profile (3.8mm) shield applications featuring two rows of contacts on a 0.6mm pitch centerline. Contacts on a 0.6mm centerline can save 30% linear board space and the 3.8mm low-profile housing reduces connector height by approximately 25%. Multiple options are available including right-angle receptacles, right-angle offset receptacles, and vertical plugs for both dock and cable applications.



TE's 0.6mm CL high speed CHAMP docking series connector is designed to meet various industry transmission standards including USB 3.0, HDMI (high definition multimedia interface) 1.4 and DisplayPort 1.2. The product can be applied in such industries as PC (including laptops and tablets) and mobile devices.

www.te.com



TTI, Inc. named TE Connectivity's Global Distributor of the Year

TTI, Inc., the global distributor of passive, interconnect, relay and switch, and discrete components, has been recognized for the second consecutive year as the Global Distributor of the Year for TE Connectivity (formerly Tyco Electronics).

Speaking at the TE Connectivity 2011 Global Distribution Channel Summit awards dinner in San Francisco, Dave Redfern, TE Connectivity's VP of Global Distribution recognized the specific performance of TTI in Europe.

Glyn Dennehy, Senior Vice President and General Manager for TTI Inc, Europe, said: "In 2010, we have grown the TE business overall by over 120%. TE is TTI's largest connector supplier in Europe and it has a comprehensive portfolio of connector and other electromech components as well as passives – a profile with which TTI is totally aligned. We believe our success with TE Connectivity is due to a very close working partnership complemented by the enhanced service levels we offer and supported by industry's broadest stocking profile which we continue to hold and develop".

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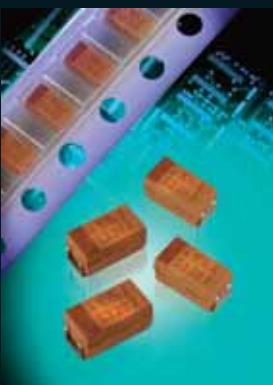
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AVX ANNOUNCES INDUSTRY'S FIRST 125V TANTALUM POLYMER CAPACITOR

AVX Corporation has announced the capability to manufacture a 125V tantalum polymer capacitor, more than twice the rated voltage of similar products on the market today. Passing the 100V milestone for the first time represents a significant development in the field of high voltage tantalum capacitors and extends the range of such devices available to engineers for new consumer product applications such as telecommunications equipment, LED TVs and power supplies for notebook computers, as well as a host of industrial applications.



AVX developed the new high voltage tantalum capacitor by optimizing processes which enhance capacitor performance and working in close co-operation with polymer suppliers. Conductive polymer has been proven to provide low ESR and reduced ignition failure mode solution. In addition, due to the nature of polymer capacitors surge robustness, lower derating of 20% can be used. However, the working voltage of tantalum-polymer capacitors was limited until now due to the maximum achievable breakdown voltage.

www.avx.com

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GREENER COMPUTERS EXPLORED AT QUEEN'S UNIVERSITY

Technology experts from around the world have gathered at Queen's University in London to explore new ways to make computers more efficient and greener.

Computing is now recognised as being responsible for significant electricity consumption and wastage around the world. Statistics indicate that computing consumes more than 3% of the global electricity consumption – performing two Google searches from a desktop computer can generate about the same amount of carbon dioxide as boiling a kettle. As limitations on computing memory and energy waste increases, international experts are hoping to develop alternatives to reduce and prevent future waste.

Professor Roger Woods from Electronics, Communications and Information Technology (ECIT) at Queen's University said: "The problem of computing electricity inefficiency is getting worse as computers pervade our lives. This group's gathering looks to tackle the problem head on by developing new computer architectures to allow us to reduce the energy budget and perform the high levels of computation needed in many new applications."

IVOR CATT, Engineer and Scientist, UK: I find the idea of greener computers hilarious and extremely 'politically correct'. The industry has demonstrated conclusively that even thought and discussion of migration from the standard Von Neumann architecture (with its Von Neumann Bottleneck) is not permitted. The proper migration to Content Addressable Memory and then to Array Processing in around 1980 did not occur, and today's computercrats don't even know about the alternative non-Von Neumann architectures discussed 40 years ago. Computing consumes power whereas memory does not. However, one deviation from the latter is the conventional DRAM, which does consume refreshing power. Staying within the self-imposed restraint that no departure from Von Neumann, with a single processor, is allowed, the only reduction in power consumption I see is in reducing the refresh rate of DRAMs, which is not a change in architecture.

Curiously, the basic weakness in my "Kernel Machine", with its one million processors, is its massive power consumption. Processing unavoidably causes power consumption. However, since it deviates from Von Neumann, it will never be built, or even discussed, although it was described in Electronics and Wireless World in March 1989.

Discussion of the embargo on change in architecture is in my article "Dinosaur Computers" in Electronics World, June 2003.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: The spectacular revolution of the data processing world contributed much to development of all practically scientific fields. Unfortunately, this took part in ecological degradation. It is time to think – seriously – of manufacturing computer equipment that is less polluting and comprising of less toxic substances.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: I feel that we should be more careful in our daily use of computers and help protect the planet. The blame for not using greener computers lies with both PC users and manufacturers. There is a lot that both groups can do to reduce carbon dioxide emissions and make computers greener. For example, users can turn off monitors and PCs when not in use, go paper-free and not print unless absolutely necessary, use reduced monitor brightness, dispose of old computers responsibly as they may contain material toxic to the environment and so on. According to a study by Fujitsu, the UK wastes £123m a year powering PCs left on out of hours. Manufacturers can also help by using energy efficient electronic components, and using re-cycled products for the casing, keyboard, mouse, monitor case and others.

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, INFN – Laboratori Nazionali del Gran Sasso, Italy: Like all electronic devices, computers have an impact on the environment. They use materials that require energy to manufacture, and many of the materials included are hazardous. They require electricity to run and are difficult to recycle. However, it's not difficult to make your computer greener, or to manufacture a greener computer.

Companies today are finding that 'going green' is not only environmentally responsible, it is also fiscally smart. Decreasing the amount that organizations consume and dispose of helps reduce company carbon footprints and costs. Therefore, facilities, operations and energy managers are looking for verifiable ways to save energy.

It is possible to build a green computer that actually functions better, with more power and ability, than many other computers. Much of the newer computer technologies, such as dual-core processors, are actually more efficient as well as more powerful than older models.

As concern about environmental issues continues to rise, green computers are expected to become more popular. As new computer technology is developed, all computers will probably become more efficient and more green. As companies seek to decrease waste, computers may also become longer-lasting and more durable.

BURKHARD VOGEL, Managing Director, Germany: Inefficiency of computers should not be explored for future purposes only. There is still an immense field of tasks of coping with the difficulties concerning the waste production of existing computers. The finding of efficient methods to cannibalize computer and electronic waste is as important as the avoidance of future waste.

One of the key methods will be biomining, a method that is currently tested in Finland on a large scale basis. The outcome will be a rather big percentage of the initially used elements in computers and electronics, like gold, silver, lithium, etc.

On the other hand, I expect that graphene-based transistor technology will save a lot of energy because it will work with lower currents and it produces its own self-cooling effect (University of Illinois in 'Nature Nanotechnology'), thus, saving energy additionally.

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