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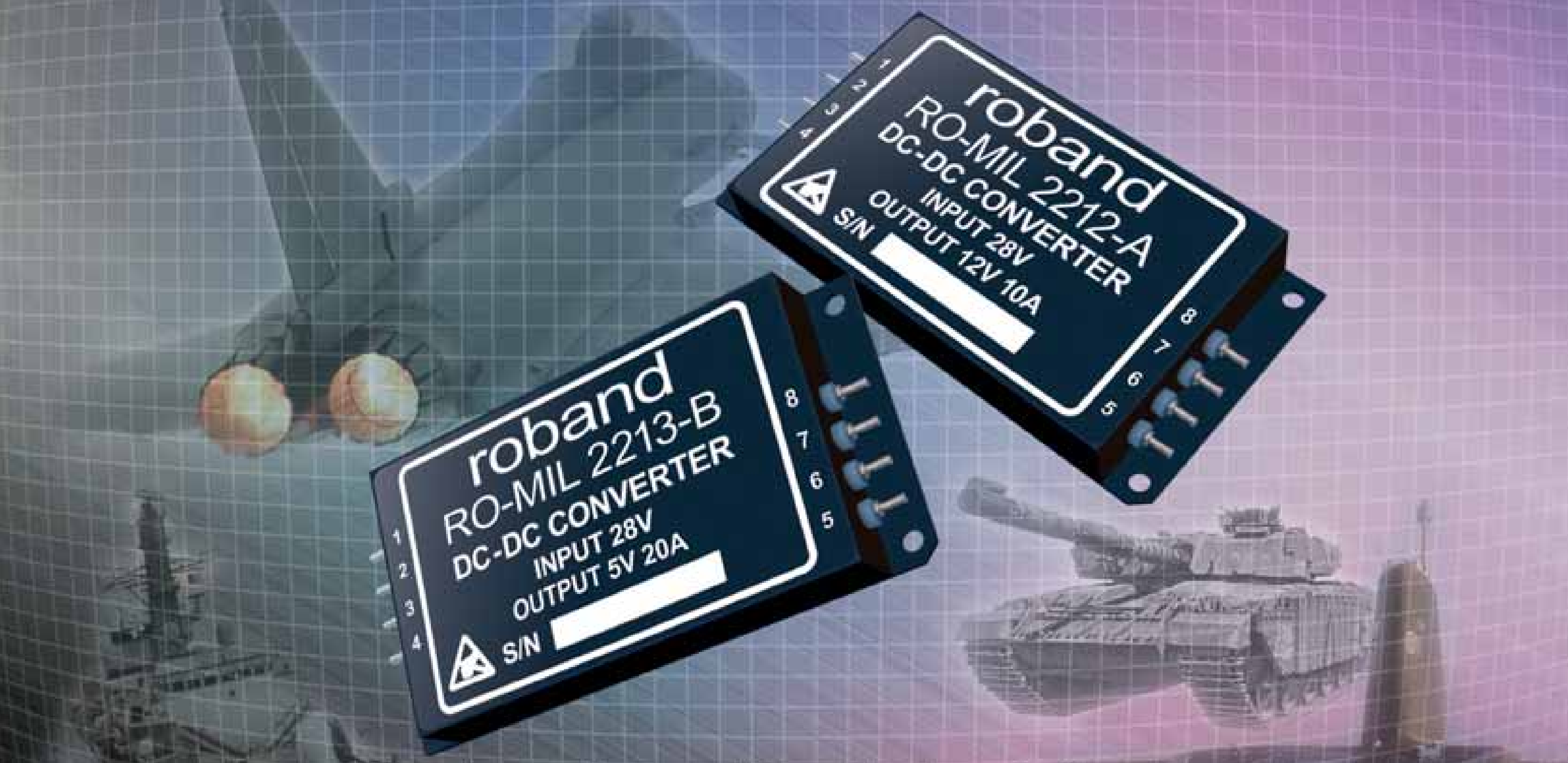

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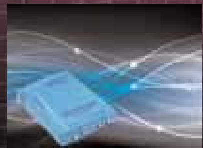
Redefining the Kilogram and the Ampere

Focus
Tackling Security Early In Design



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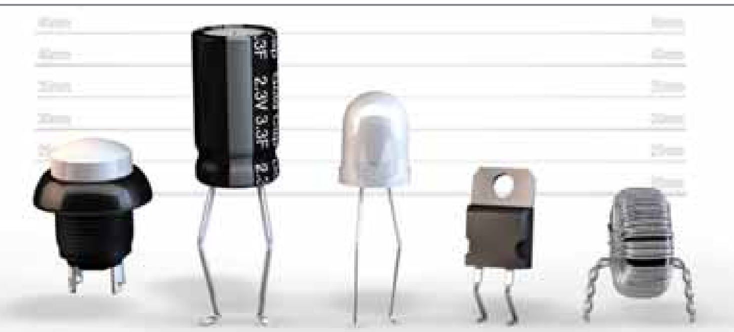

TRENDS IN RF/MICROWAVE APPLICATIONS

Ever since the pioneering days of Guglielmo Marconi and Nathan B. Stubblefield et al in the late 19th century, the race has been on to garner the use of Radio Frequency devices to an ever-expanding portfolio of applications.

The traditional use of RF/Microwave technology in commercial telecommunication and data communications, military systems, telephony, television and radio etc. is undoubtedly holding up well despite the 'economic climate'. Our insatiable hunger for new ways to watch, listen, defend, attack, learn, cure and generally *communicate*, will ensure that that this demand will continue for a good while yet!

There are an enormous number of exciting new applications and methodologies for delivering RF technologies with the trend towards smaller and smaller platforms and higher and higher frequencies, providing fascinating challenges for RF and Microwave engineers.

Important trends in RF construction and use include 'waterproofing' and 'ruggedising' of many traditional products to cope with weather, water or dust ingress, harsh environmental situations or safety considerations. Many more applications are now calling for IP (Europe) or NEMA (USA) ratings which define the protection against ingress of water and dust for a particular piece of equipment. Miniaturisation is reaching astonishing levels, with coaxial cables now available with a diameter of significantly less than 1mm and with some cable to board connectors having a mated height of less than 2mm. Frequency ranges are also pushing the envelope with RF cables and connectors now available which will work at over 110GHz.

Intelliconnect is the only UK manufacturer of 50Ω RF connectors and has a US-based design and manufacturing facility. It offers a continually increasing range of standard coaxial and triaxial products. Intelliconnect offers one of the fastest turnarounds in the industry – from drawing to delivered product in just 7 weeks for custom-designed RF connectors and components.

In terms of new applications, the Medical field is possibly the most exciting of all, because of the plethora of new product innovations using RF technology. Whilst RF has been used in the medical field for over 75 years, new advances have meant that is now used extensively in a multitude of treatments and back-up applications. Because RF is virtually painless and able to penetrate the skin and be absorbed locally into organs which are buried deep within the body, it is now often used to replace much more invasive and painful laser surgery techniques.

Another fascinating development is the use of RF in neuro-

Miniaturisation is reaching astonishing levels, with coaxial cables now available with a diameter of significantly less than 1mm

stimulation, most particularly cochlear implants which help many partially and profoundly deaf patients hear almost perfectly. These along with corrective eye surgery, sleep apnea treatment, cosmetic surgery, radiation dosimetry and detection, and prostate surgery are some of the many applications emerging for RF technology in the medical arena.

In the Military/Aerospace sector the well entrenched use of RF and Microwave technologies is set to continue with increased focus on personal, soldier carried communications, locators and jamming systems. The emphasis continues to be on small, lightweight, simpler-to-use platforms designed to enable personnel to be able to carry and use more sophisticated equipment. Again, miniaturisation and harsh environment protection are key factors. Drones used in electronic countermeasures are becoming more prevalent as are remote sensors for signal intelligence. Homeland Security is an area which has seen massive growth in the last ten years with applications such as radiation detection, counter IED equipment and mobile phone jammers.

Increasingly sophisticated safety and security equipment in many areas is also using RF technology to enhance the effectiveness of its performance. Some examples include the use of RF corrosion monitoring systems in applications varying from marine craft to oil refineries, public traffic and surveillance systems, onboard telemetry on trains and personal locator beacons for use in loss at sea situations.

It is heartening that the UK is at the forefront of many of these new developments in RF/Microwave technologies. The potential income for UK Plc is vast and many now see these types of technological advances, along with specialist manufacturing, as being in the forefront of our economic recovery.

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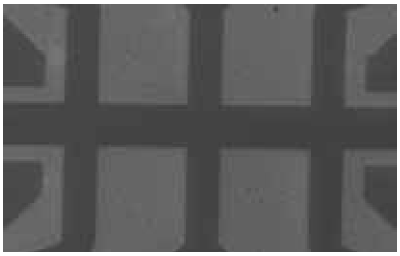
Redefining the SI units: the Kilogram and the Ampere



Scanning electron micrograph picture of graphene device. The dark area is monolayer graphene and the light areas is the silicon-carbide substrate

We could be on a course of redefining two SI units (Système Internationale d'unités) thanks to a groundbreaking research by the National Physical Laboratory's (NPL) Quantum Detection Group. The research using graphene presents the most precise measurements of the quantum Hall effect ever made, one of the key steps in the process of redefining the units such as the kilogram (mass) and the ampere (electric current).

Presently the kilogram is defined by a physical lump of platinum-iridium and the ampere is defined via the force produced between two wires, but the goal is to define the kilogram in terms of the Planck constant (h) and the ampere in terms of the electron charge (e). Making this change relies on the exactness of the relationships that link these constants to measurable quantities. The quantum Hall effect defines a relationship between these two fundamental physical constants.

Until recently the effect was exclusively observed in a few semiconductor materials. A few years ago the quantum Hall effect was also observed by the same team in graphene, a completely different type of material with a very different electronic structure. But NPL's latest research directly compared the quantum Hall effect in graphene with that observed in a traditional semiconductor material. Graphene is hotly tipped to surpass conventional materials in many important applications, partly due to its extraordinary electrical properties.

The results confirmed that the quantum Hall effect is truly universal with an uncertainty level of 86 parts per trillion, supporting the redefinition of the kilogram and ampere. The quantum Hall effect in graphene is so good that it should be the material of choice for quantum resistance metrology.

"It turns out that the quantum Hall effect in graphene is very robust and easy to measure – not bad for a material that was only discovered six years ago," said JT Janssen, NPL Science Fellow.

ZINC OXIDE MICROWIRES IMPROVE LED PERFORMANCE

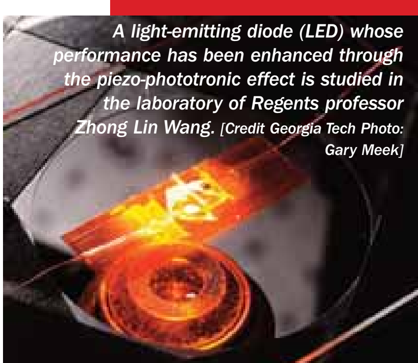
Researchers have used zinc oxide microwires to significantly improve the efficiency at which gallium nitride light-emitting diodes (LED) convert electricity to ultraviolet light. The devices are believed to be the first LEDs whose performance has been enhanced by the creation of an electrical charge in a piezoelectric material using the piezo-phototronic effect.

By applying mechanical strain to the microwires, researchers at the Georgia Institute of Technology created a piezoelectric potential in the wires, and that potential was used to tune the charge transport and enhance carrier injection in the LEDs. This control of an optoelectronic device with piezoelectric potential, known as piezo-phototronics, represents another example of how materials that have both piezoelectric and semiconducting properties can be controlled mechanically.

"By utilizing this effect, we can enhance the external efficiency of these devices by a factor of more than four times, up to eight percent," said Zhong Lin Wang, a Regents professor in the Georgia Tech School of Materials Science and Engineering. "From a practical standpoint, this new effect could have many impacts for electro-optical processes – including improvements in the energy efficiency of lighting devices."

Because of the polarization of ions in the crystals of piezoelectric materials, such as zinc oxide, mechanically compressing or otherwise straining structures made from the materials creates a piezoelectric potential – an electrical charge. In the gallium nitride LEDs, the researchers used the local piezoelectric potential to tune the charge transport at the p-n junction.

The effect was to increase the rate at which electrons and holes recombined to generate photons, enhancing the external efficiency of the device through improved light emission and higher injection current. "The effect of the piezo potential on the transport behaviour of charge carriers is significant due to its modification of the band structure at the junction," explained Wang.



A light-emitting diode (LED) whose performance has been enhanced through the piezo-phototronic effect is studied in the laboratory of Regents professor Zhong Lin Wang. [Credit Georgia Tech Photo: Gary Meek]

NEWS IN BRIEF

Figures released from the UK's Department for Business, Innovation and Skills (BIS) show apprenticeships are on the increase, with 442,700 courses beginning in the 2010/11 academic year. However, concerns abound about the future of apprenticeships as businesses evaluate their training spend.

Sarah Thwaites, Deputy Chief Executive of Financial Skills Partnership, said: "The steady increase in the number of people beginning apprenticeships is encouraging, but worryingly, some businesses plan to reduce the number of apprentices they take on next year. If the number of available apprenticeships were to regress over the next year, the skills picture and the jobs market would be severely tarnished."

A new strategy to grow the UK's power electronics industry and increase its share of the £135bn global market was published last month by Business Minister Mark Prisk. The new five to ten year strategy, which has been created by the industry and academia, and supported by the Government, aims to address the main problems in the sector and establish a foundation for ambitious but sustainable long-term growth.

"The UK manufactures 3.1% of all power electronics products made across the globe. We have world leading, globally recognised companies working on power electronics here in the UK, but it's not recognised as one of our strengths, I want to make sure we change that," said Prisk.

Power Electronics plays to the strengths and aspirations of the UK. It is a high-growth, high-added-value and high-value per employee technology. It demands highly skilled teams of engineers to meet the demands of the complex integration challenges this presents – a capability in which, it could be argued, the UK leads the world.

The University of Westminster has been awarded a grant of £507,000 from the UK Energy Research Centre (UKERC) to support research into smart grids.

The aim of smart grids is to improve the flexibility of today's electricity networks to manage increasing demand from consumers and industry, to enable increasing amounts of renewable generation to be connected, and to improve the monitoring and operation of the equipment that makes up the networks. Spin-offs for consumers may include more accurate metering and billing. By making the UK's energy networks fit for the 21st century, smart grids can help make UK business and industry more competitive internationally.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LPRS inspires you to realise your wireless design ideas with an amazing challenge and total prize money of $10,000 USD

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IQRF innovative wireless network components are fully integrated modules with pre-programmed micro controllers and are intended to speed up time to market of reliable wireless mesh networks. The extensive IQRF product range offers transceiver modules with an embedded operating system through to IP accessible control panels and Ethernet gateways. Everything you need to quickly develop your idea to prototype stage and beyond.

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ABOUT IQRF

WHAT IS IQRF?

IQRF is a complete modular platform for wireless peer to peer or network connectivity

WHY MESH NETWORK?

To offer extended range – packets can be delivered via intermediate points (routers) to the destination (hopping) at up to 700 metres per hop
Avoiding obstacles – routing mechanisms have a capacity to detect temporary failures and use alternative paths
Lower RF output extends battery lifetime and generates less noise

WHAT TYPES OF APPLICATIONS ARE POSSIBLE WITH AN IQRF MESH NETWORK?

Due to their extremely low power consumption and ease of use IQRF Transceivers are ideally suited to, and easily integrated into, Smart Meters and Grids. For much the same reason the “Smart House”, Home Area Networks and Building Automation are ideal application areas for Mesh Networks
A broader arena for using wireless networks is the creation of the “Smart City” and Controllable Street lighting using bidirectional communication, routing up to 700 metres per hop and dynamic timing for fast responses.

WHAT ELSE CAN IQRF DO?

For more information about IQRF please visit www.iqrf.org

Best Practices for Tackling Security Early in Development

RUTUL DAVE, SENIOR DEVELOPMENT MANAGER AT COVERITY, SAYS THAT SECURITY MUST BE ADDRESSED EARLY IN THE SOFTWARE DEVELOPMENT LIFECYCLE TO MINIMIZE PROJECT AND BUSINESS RISK AND COST, BY ADAPTING SECURITY TO THE WAY THE DEVELOPERS WORK, NOT THE OTHER WAY AROUND

According to a 2009 survey from Software Productivity Research LLC, poor software quality costs more than $500bn per year globally in financial, competitive and brand equity losses. Software is at the heart of operating many of the products that we use in our daily lives and is a source of competitive differentiation for companies in a variety of industries.

Whether direct and obvious, or indirect and hence harder to realise, there is real business value associated with software quality. The news headlines related to security breaches, stolen user data and unauthorized access can often be traced back to common programming mistakes and defects in code introduced during software development. Errors, bugs and defects can add up to major financial and business costs that just cannot be ignored.

In addition to the software created internally, a big source of unsecure code is from different sources of third-party software. Consequently, software organizations are realizing that it is crucial that the software they develop in-house or acquire from third parties must be secure.

> *Security breaches in software and mobile devices are making headline news and costing companies millions in lost revenue and damage to brand equity*

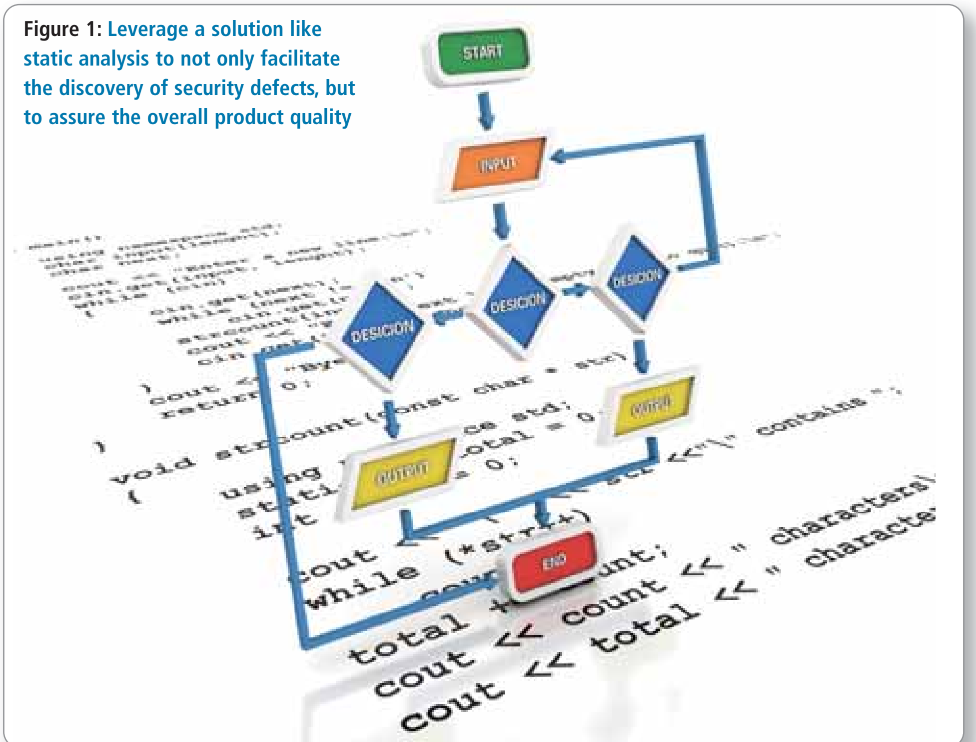


Figure 1: Leverage a solution like static analysis to not only facilitate the discovery of security defects, but to assure the overall product quality

Developing, deploying and using software without addressing the security vulnerabilities is a big risk not worth taking, especially considering the cost-effective options available.

In a recent webinar discussing the best practices for tackling security early in development, speakers Robert Seacord who leads the secure coding initiative at CERT, Yinian Mao, Engineering Lead at Qualcomm, and Michael White from Coverity presented recommendations and answered questions on the topic of what development teams can do to address security. The three speakers brought up several interesting points about the increased exposure that comes with global connectivity and best practices organizations should consider to minimise that risk:

- Security should be integrated into the product lifecycle. Quality improvement is the end-result.
- Management needs to be aware that security is a serious commitment and investment.
- Adopt secure coding standards for your target development language and platform.
- Leverage a solution like static analysis to not only facilitate the discovery of security defects, but to assure the overall product quality.

Security Integration into the Product Lifecycle

Security integration into the product lifecycle was by far the most important issue addressed. As we all know, security breaches in software and mobile devices are making headline news and costing companies millions in lost revenue and damage to brand equity. As more people conduct increasingly sophisticated and sensitive transactions on their mobile devices and over the web, the stakes around software security are rising. Plus, the software and platforms themselves

Figure 2: To properly address security issues early in the development lifecycle, developers need an automated approach for identifying defects that lead to vulnerabilities

are becoming increasingly complex with multiple components coming from multiple providers. Companies often have little visibility into the security or quality of the third party code which can introduce multiple points of failure and blame. Traditional approaches to security are no longer sufficient.

For too many organisations, security is left to an isolated security audit team with limited resources and is conducted at the end of the software development lifecycle. And the later the issues are raised in the lifecycle, the more expensive and time-consuming they are to address. Compounding this issue is the fact that security audit and development teams have different goals. Security audit teams are focused on risk-meeting audit and compliance requirements by ensuring vulnerabilities are identified and remediated prior to release. Development teams, on the other hand, are driven by speed and innovation, and deliver new products to market, fast, at the least possible cost. This is what all too commonly happens: a security audit is performed at the end of the development cycle, with tools purpose-built for a security auditor. Then, a PDF report, containing a long list of security vulnerabilities – without context or guidance of where they exist in the code and how to fix them, makes its way to the developer's desk as they are racing to get the product out the door on-schedule. If the information isn't actionable, isn't presented in the developer's workflow and isn't addressed throughout the development cycle as the code is being written, security isn't going to be effectively addressed. To properly address security risks and vulnerabilities without jeopardizing speed or cost, companies must bring security into the development process in the same way quality defects are managed today. This means adapting security to the way the developers work, not the other way around.

Software Assurance through Automated Code Testing

To properly address security issues early in the development lifecycle, developers need an automated approach for identifying defects that lead to vulnerabilities. Existing testing methods and manual processes are no longer sufficient alone to solve the problem given the increasing size and complexity of codebases. Automated code testing via static analysis provides developers with an automated solution for code assurance that is beneficial in multiple ways. Firstly, it enables them to test for security, quality and safety defects through a process that is automated and a part of the development workflow. Secondly, they are not required to write unit tests to specifically check for security vulnerabilities. And finally, they have an actionable way to find, understand and fix the defects that lead to security vulnerabilities without needing to be experts on the subject.

Companies often have little visibility into the security or quality of the third party code which can introduce multiple points of failure and blame

Static Analysis

Static analysis is done by an automated engine, without actually executing programmes built from that code. As the code is being compiled, the analysis engine identifies execution paths and patterns that could result in unintended system behavior, system crashes or security vulnerabilities.

Mainstream adoption of static code analysis is gaining speed across industries using software to run their businesses and equipment. In some cases the analysis process is close to becoming a legislated requirement. Take for example the growing number of highly sophisticated medical software that is operating across hospitals to help patients and potentially save lives. The technology is so advanced and complex that in America the FDA has identified the use of static code analysis as a means of improving the quality of software.

What's also great about this technology is that the nature of static analysis means that as soon as the code has been written, developers potentially start analyzing it and identifying defects/vulnerabilities.

Contrast this with dynamic testing approaches – an expert would need to have to have at least a partially working/executable test harness, some dependencies, perhaps a set of test data to feed it as input and potentially a working test environment which mimics what the 'real world' will look like.

Of course, there will still be certain classes of bugs that depend upon runtime or environmental factors, which is why it's still important to have a solid dynamic testing strategy too.

Addressing Security Early On

Security must be addressed early in the software development lifecycle to minimize project and business risk and cost. One of the most effective ways to do this is to bring security to the developer, not the other way around, in the same way they manage software quality today. This means presenting developers with actionable information in their existing workflow, so they can fix vulnerabilities in the same way as quality defects – as the code is written. While the security audit team should perform its audit throughout the development project, waiting until the end of the development cycle to identify vulnerabilities and pass them back to developers who are under time-to-market pressure, is ineffective. In addition, with the increasingly complex software stack and reliance on third party suppliers, companies need better visibility into the security, quality and safety of their code. ●

The Middle: the place that fails to join the ends

MYK DORMER IS SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
WWW.RADIOMETRIX.COM

An awful lot gets spoken (or rather, preached) about technical education, and its many failings. Depressingly few of these sermons fail to spend much of their word-count talking about "the basics", and the supposed absence of tuition (or ability) in them. Usually, this nebulous categorisation of knowledge stretches from basic English and mathematics to fundamental engineering principles such as Ohms law, basic Newtonian mechanics or Boolean algebra. Occasionally the critic will wax lyrically about the value of higher mathematics, of calculus or Eigen vectors.

I cannot agree. In a couple of decades in the RF industry, it is not a lack of basic knowledge that I have seen inconveniencing either interviewees or customers; all that I have encountered are literate and numerate, and possessed an appropriate level of engineering education. It is an absence of information and experience in the "middle".

To explain: I know many software engineers with highly advanced programming skills in abstracted languages, such as Java or Python, who are unaware of the basic machine architecture, and who would be lost if presented with an assembler, or a binary core-dump. I have worked with "RF" engineers who can adroitly assemble integrated building blocks (or utilise "complete system on chip" products) but who could not design a mixer, an AGC amp or a Blumlein switch out of discrete parts. I have sold radio modules to hardware engineers who routinely assemble mixed-signal designs using op-amps and microcontrollers but who would be adrift if tasked with the design of a Schmitt trigger, or the logic networks of an ALU.

I suggest that there is neither shortage of fundamental theory level training nor end-product application experience. Where the gap can be found is in the intermediate complexity area that links the two and which is absolutely vitally necessary for a genuine understanding of the eventual, target design.

It may be argued that, in an era of highly integrated digital (or analogue) chips, there really is no reason to study old fashioned "discrete component" design methods anymore, but in my experience you cannot understand the behaviour of more complex systems without familiarity with the simpler sub-systems from which they are made up.

For example, when a multi-stage RF power amplifier starts misbehaving on the bench neither textbook single stage parameter analysis nor familiarity with any number of IC data sheets will help. It is necessary to understand how the basic circuit is configured and what it will do, and how the various parts of it inter-relate and interact. The only way to gain that experience is to have designed and built such circuitry up from the individual parts and tested it.

> *I have worked with "RF" engineers who can adroitly assemble integrated building blocks but who could not design a mixer, an AGC amp or a Blumlein switch out of discrete parts*

Additionally, there are still many instances where the cunning use of a handfull of discretes will do the work of a far more expensive (and, in these days of long lead-times and frequent product withdrawals, often hard-to-source) integrated circuit, or where the discrete component approach outperforms on-chip equivalents (frequently the case in high performance RF designs, but also seen in high-end audio circuits).

I am not arguing for a Luddite rejection of our current state of the art, and neither am I favouring nostalgia over rational modern design decisions, but when we use these complex, integrated solutions we also must not lose track of what they are made up of.

It is not difficult to research the discrete circuitry methods of the past few decades (the Internet is a fabulous resource for this, as are public libraries with their inevitably slightly out-of-date engineering sections) and hang together a few dozen parts into something that is both functional and understandable. Construct a bench power supply, an AM radio, or even something as trivial as a doorbell. It fills in the gap between the theory taught at school and university and the often abstracted nature of our current state of the art.

It's fun too. but with another node. Now give each node the ability to operate as a repeater (to store data received in one frame for re-transmission in the next) and we have the basic framework for a mesh network – which is a whole new subject! ●

PICO TECHNOLOGY RELEASES NEW USB MIXED SIGNAL OSCILLOSCOPE

The new PicoScope 2205 MSO is a 2 channel oscilloscope combined with a 16 channel logic analyser, all in one compact, portable USB instrument. So, now you can view analog waveforms and digital data on the same screen with the efficient and easy-to-use PicoScope software (a SDK is also provided).

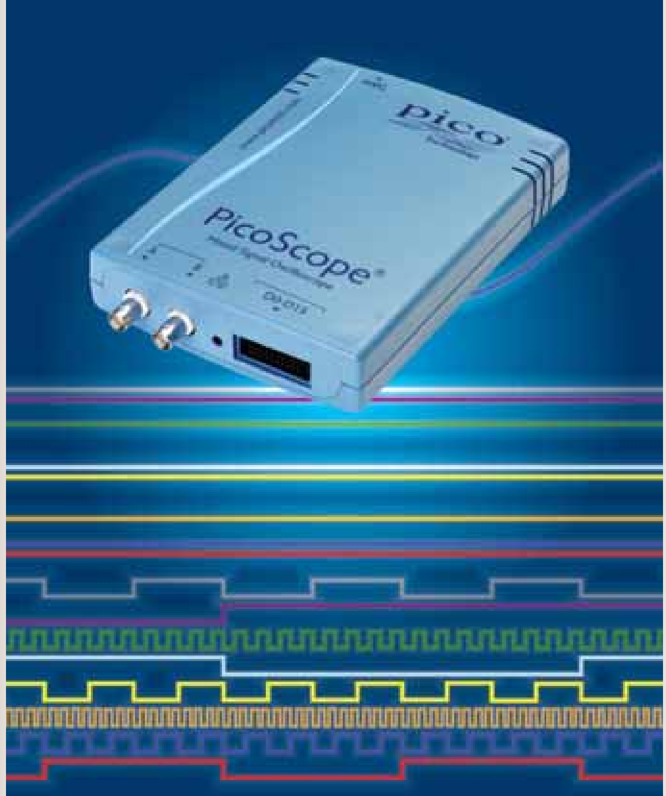
With 25 MHz analog bandwidth, analog sampling rates up to 200 MS/s and 100 MHz maximum digital input frequency, the PicoScope 2205 MSO is suitable for general purpose analog and digital circuit design, testing and trouble shooting.

The new PicoScope 2205 MSO is available now, priced at only £349 for a kit with two passive x1/x10 probes, a logic cable and test hooks. A generous 5 year warranty is also included. If you purchase a kit and are then the lucky one who wins their competition, they will refund your money. So don't delay as stocks are limited!

To celebrate the launch they are running a competition to win one of their new MSO kits worth £349!

Make sure you enter code EWE1 when you submit your answers. For your chance to win just follow this link: http://www.picoscopemso.com

The lucky winner will be announced in January's Pico newsletter. Join their newsletter on the following link http://www.picotech.com/maillist.html



CLOCK AND SIGNAL INTEGRITY FOR TESTING HIGH-SPEED ADCS

HIDEO OKAWARA, PRINCIPAL CONSULTANT OF MIXED SIGNAL TEST APPLICATIONS IN THE CENTRE OF EXPERTISE IN VERIGY JAPAN K.K., DESCRIBES THE TESTING OF MID-RANGE ADCS OF 10 TO 12 BITS RESOLUTION FOUND IN APPLICATIONS SUCH AS VDSL, WIRELESS LAN, DIGITAL TV SETS AND SET-TOP BOXES

You can find many A/D converters (ADCs) implemented in consumer devices such as personal computers (PC) and mobile phones. PC and mobile phones are different appliances, but there are similar elements found inside. For instance, hard/optical disk drive read-channels, wireless blocks, built-in TV and cameras contain ADCs.

Digital cameras contain relatively slow speed but high bit-count ADCs. Disk drive read-channels contain extremely high-speed but low bit-count ADCs. In the speed area from 10Msps to 100Msps, there are lots of applications such as VDSL, wireless LAN, digital TV and set-top box, in which most ADCs have 10 to 12 bits resolution. This article describes testing of these mid-range ADCs.

ENOB: ADC Performance Indicator

When testing an ADC by ATE, four functional resources are required, as Figure 1 illustrates. The DC power is fed by a device power supply; the test signal is supplied by an analog signal source, which is usually an arbitrary waveform generator (AWG); the sampling clock is supplied by digital pin electronics; and the ADC output codes are captured by digital capture functions in digital pin electronics. In order to pull out the maximum device performance, each one of the resources should be carefully selected and arranged appropriately. The sampling clock and the test signal are particularly the most sensitive factors of all for testing high-performance ADCs so that in this article these two resources are highlighted and analyzed from the jitter's point of view.

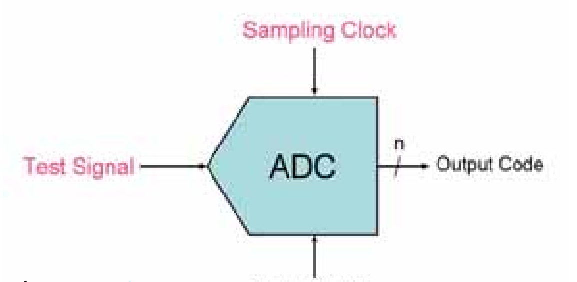


Figure 1: ADC test

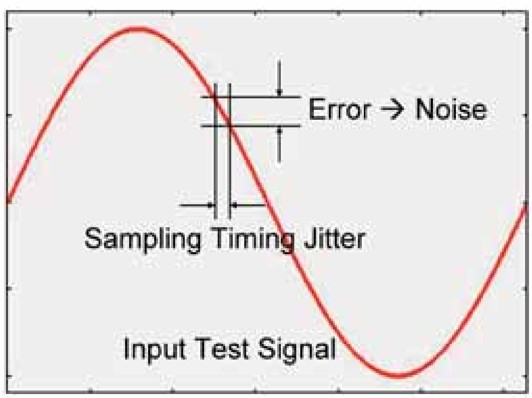


Figure 2: Effect of sampling clock jitter

The key performance of ADC is linearity and dynamic range. Poor linearity creates harmonics distortion so that it is characterized as THD or total harmonics distortion. Since ADC quantizes an analog signal, it essentially generates a quantization error based on its number of bits. This error is interpreted to quantization noise in the output codes. More over there may be various spurious noise caused by the interference of complex activities inside the device. Distortion and noise decide the dynamic range of the ADC.

If an ideal, linear n-bit ADC generates quantization noise, the ultimate SNR of the device is known as follows:

$$SNR[dB] = 6.02 \times n + 1.76 \quad (1)$$

In actual device testing, the ADC output contains the signal and all of disturbances such as distortion, thermal noise, quantization noise, spurious noise and so forth. Therefore, the most typical characteristic parameter is SINAD or signal to noise and distortion ratio. SINAD can clearly indicate the total performance of the device. It is calculated as the ratio of the power of fundamental tone over the rest of all power. SINAD value is always worse than the SNR value defined by Equation 1.

The effective number of bits, or ENOB, is calculated by the measured SNR, which is SINAD, as follows:

$$ENOB[bits] = \frac{SINAD[dB] - 1.76}{6.02} \quad (2)$$

Therefore, ENOB is always smaller than the number of bits n. ENOB describes the true performance of the tested ADC so that it is a convenient performance indicator.

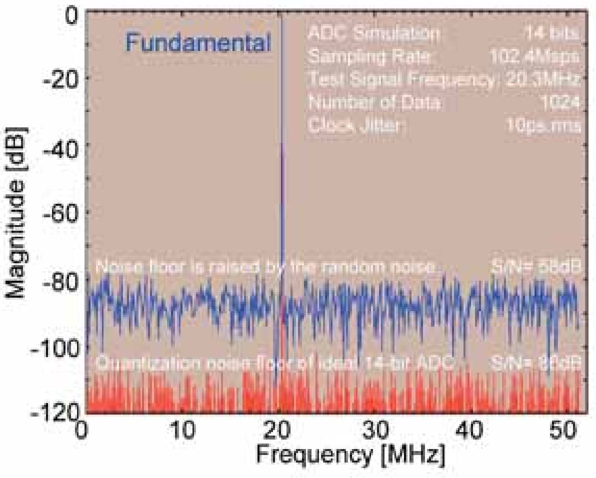


Figure 3: Effect of sampling clock jitter (simulation)

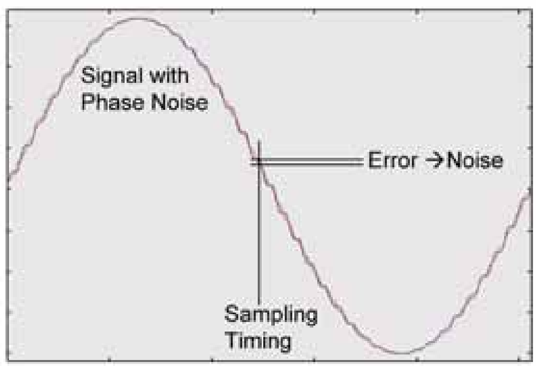


Figure 4: Effect of test signal phase noise

Effect of Sampling Clock Jitter

An ADC samples the instantaneous level of the signal at the moment that the sampling clock edge crosses over the threshold, compares the captured level with the quantization thresholds and decides a specific output code. If the sampling clock edge contains some fluctuation that is jitter, the ADC picks up slightly different level than the original level to be sampled, as Figure 2 illustrates. Therefore, even if the test signal is an ideal sinusoid, when the sampling clock contains jitter, sampled data produces more errors than the quantization error. The additional conversion error can be seen as additional noise over the native quantization noise.

Let's define the test signal v(t) as follows:

$$v(t) = A\sin(2\pi F_{signal} t) \tag{3}$$

where A and F_{signal} denote the amplitude and the frequency of the signal respectively. The differential dv/dt derives the way that the timing fluctuation Δt can be converted to the voltage error Δv as follows:

$$\frac{dv}{dt} = A \cdot 2\pi \cdot F_{signal} \cos(2\pi \cdot F_{signal} \cdot t) \tag{4}$$

$$\Delta v = A \cdot 2\pi \cdot F_{signal} \cdot \cos(2\pi \cdot F_{signal} \cdot t) \cdot \Delta t \tag{5}$$

Then the RMS timing error is denoted $\Delta t|_{rms,}$ which is the jitter and is converted to the RMS error voltage $\Delta v|_{rms}$ as follows:

$$\Delta v\big|_{rms} = \frac{A \cdot 2\pi \cdot F_{signal} \cdot \Delta t\big|_{rms}}{\sqrt{2}} \tag{6}$$

Now that the noise voltage based on the sampling clock jitter is derived as Equation 6, the SNR based on the jitter can be calculated as the ratio of the RMS signal to the RMS noise as follows:

$$SNR = \frac{\frac{A}{\sqrt{2}}}{\Delta v\big|_{rms}} = \frac{1}{2\pi \cdot F_{signal} \cdot \Delta v\big|_{rms}} \tag{7}$$

$$SNR[dB] = -20\log(2\pi \cdot F_{signal} \cdot \Delta v\big|_{rms}) = -20\log(2\pi \cdot F_{signal} \cdot JitterRMS) \tag{8}$$

Finally Equation 8 shows the effect of the sampling clock jitter *JitterRMS*. One of the important points is that this jitter-based SNR value depends on the test signal frequency $F_{signal.}$ We are often apt to think that the higher the sampling rate is, the more influence the jitter impacts on the SNR; however, it is not true. As you see, there is no sampling frequency term found in Equation 8. The sampling rate has nothing to do with the jitter-based SNR value. Therefore, you should always watch out the test signal frequency; especially when you deploy under-sampling in device testing, you should be aware of the test signal frequency and you should arrange an appropriate sampling clock source.

ADC has essentially quantization noise in the frequency spectrum based on the resolution. Equation 1 represents the theoretically ultimate SNR value. The noise is usually distributed all over the entire spectrum bins so that the quantization noise floor is located about SNR+10log(N/2) [dB] below the full-scale signal level, where N is the number of sampling points.

The ADC sampling clock jitter is transformed to noise in the conversion result. Jitter is classified as random jitter and deterministic jitter. Random jitter has no frequency dependency so that the noise influence would raise the entire noise floor.

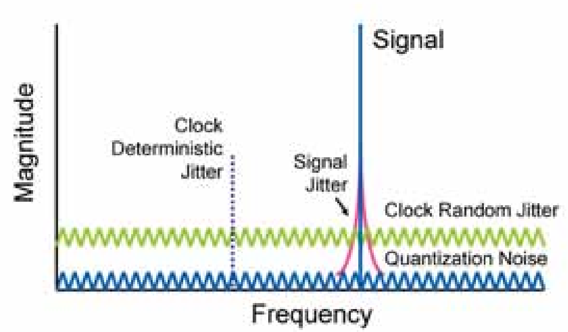


Figure 5: Jitter influences

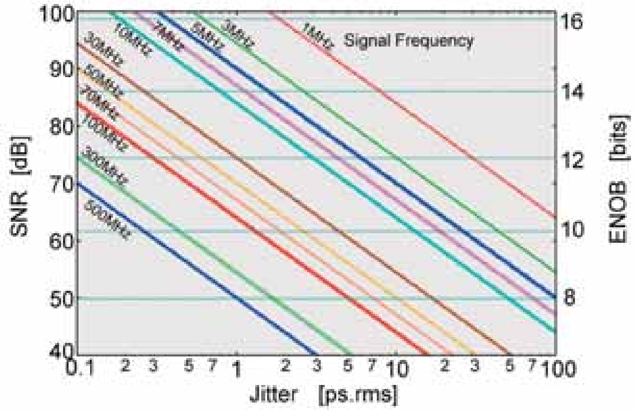


Figure 6: SNR (ENOB) vs jitter

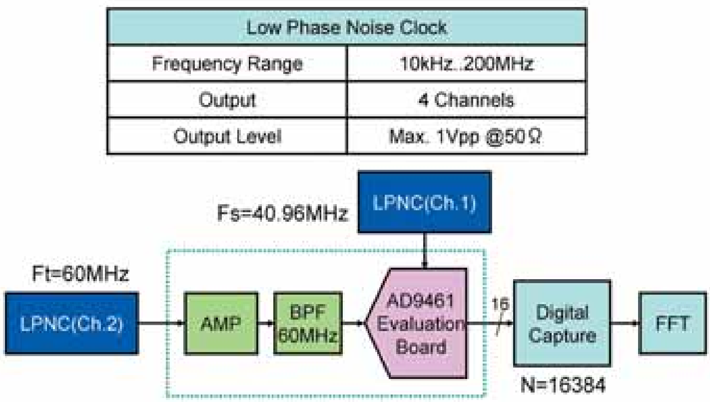


Figure 7: Specification of LPNC and experimental configuration

A simulation is performed about a 14-bit ADC running at the rate of 102.4Msps. The test signal is a full-scale sinusoid of 20.3MHz. The ADC captures 1024 points of data and its FFT spectrum is illustrated in Figure 3. The spectrum coloured red shows the ideal quantization noise floor which is located around -113dBc. The calculated signal to noise power ratio is 86dB, which equals to the value calculated by Equation 1. When the sampling clock is supposed to contain 10ps rms random jitter, the noise floor rises as coloured blue. The calculated SNR is 58dB equals the value calculated by Equation 8. If the sampling clock jitter is deterministic, it has specific frequency characteristics so that it would become specific spurious noise instead of the increase of noise floor.

Effect of Test Signal Phase Noise

If the ADC input signal contains phase noise, the signal trace fluctuates as Figure 4 illustrates.

Let's denote $\Phi(t)$ to a tiny phase noise in the test signal sinusoid. If the signal $v(t)$ contains the phase noise, it is described as follows:

$$\begin{aligned} v(t) &= A\sin(\omega_{signal}\cdot t+\phi(t)) \\ &= A\cos\phi(t)\sin(\omega_{signal}\cdot t)+A\sin\phi(t)\cos(\omega_{signal}\cdot t) \\ &\approx A\sin(\omega_{signal}\cdot t)+\phi(t)A\cos(\omega_{signal}\cdot t) \\ &= Signal + Noise \end{aligned} \quad (9)$$

where $\cos\Phi(t) \sim 1$ and $\sin\Phi(t) \sim 0$ are applied based on $\Phi(t) \sim 0$.

Equation 9 shows that the noisy signal $v(t)$ is finally separated to the original signal and the noise components. When Φ_{rms} denotes the RMS phase noise, it can be interpreted to the RMS jitter *JitterRMS* which has the dimension of time by $\Phi_{rms}/\omega_{signal}=\Phi_{rms}/2\pi F_{signal.}$ Consequently the signal-to-noise ratio based on the phase noise can be described as follows:

$$SNR = \frac{Signal|_{rms}}{Noise|_{rms}} = \frac{\frac{A}{\sqrt{2}}}{\phi(t)|_{rms}\frac{A}{\sqrt{2}}} = \frac{1}{\phi_{rms}} = \frac{1}{2\pi\cdot F_{signal}\cdot JitterRMS} \quad (10)$$

$$SNR[dB] = -20\log(2\pi\cdot F_{signal}\cdot JitterRMS) \quad (11)$$

Finally, the SNR is expressed as Equation 11, which looks the same as Equation 8; however, the jitter source is the sampling clock in Equation 8 and the signal source in Equation 11. Here again you should be aware that jitter-based SNR depends on the test signal frequency, not the sampling clock rate in Equation 11 as well.

As discussed in the previous section, when the sampling clock contains random jitter, it would raise the noise floor. When the sampling clock contains deterministic jitter, it would appear as specific tones; however, they are phantom spurs on the FFT display; no such real noise exists in the signal. The test signal phase noise would manifest as the residual phase noise skirt around the fundamental tone in the spectrum. Figure 5 summarizes these influences.

Figure 6 visualizes Equations 8 and 11, illustrating the relationship of SNR (and ENOB) vs RMS jitter with the parameter of test signal frequency. For example, when the test signal is 100MHz and you need to test an ADC with 10-bit ENOB, you must provide a very fine sampling clock with better than 1.5ps rms jitter and very high quality test signal, which is not only very low distortion but also extremely low jitter, better than 1.5ps rms jitter.

Experimental Result

The DUT is AD9461 (Analog Devices), whose ENOB is approximately 12 bits. The actual test utilizes the evaluation board of AD9461. The required interface circuit is already fully equipped on the board besides the DUT. The sampling clock is set 40.96MHz and the test signal frequency is 60MHz; this is an under-sampling condition and typical in video applications. The video application needs 11-bit of ENOB, which is a very challenging value while using regular digital resources and an AWG in a mixed signal ATE. The experiment is performed with employing the low phase noise clock (LPNC) N2397, which is an excellent clock source in the Verigy V93000 SOC test system.

Figure 7 illustrates the experimental configuration including a part of the specification of the clock module. The LPNC generates very low jitter sinusoidal signals so that it is very suitable for testing a high-speed midrange ADC. This is a system evaluation to verify that the system is capable to test a consumer video application ADC. The LPNC provides four channels of independent outputs so that two channels are used for this experiment. One channel is assigned to the signal source and another channel takes care of the sampling clock. For the signal source, the output sinusoid needs to be refined by using an extra band pass filter (BPF) and an amplifier on the DUT board. For the sampling clock source, sinusoidal waveform is not appropriate in terms of the noise-to-jitter sensitivity; however, this particular device accepts differential mode clock and diode limiters implemented in the clock path on the board so that the LPNC output is supplied to the clock input port in differential mode with maximum swing.

Figure 8 shows the measurement result. Since the test signal is 60MHz and the sampling rate is 40.96MHz, the fundamental tone is aliased at 19.04MHz in the display. The performance is parameterized as SINAD = 72.7dB so that ENOB = 11.6 bits. Consequently, the V93000 system with the LPNC module is verified to be capable of testing the video application ADC.

Based on Equation 8, SINAD = 72.7dB can be interpreted as 0.9ps rms of jitter for the sampling rate of 40.96MHz. Both the signal and clock are supplied by the LPNC, and their frequencies are relatively close to each other in this experiment so that the actual jitter performance of the LPNC may be approximately 70% of this number, that is 0.6ps rms.

As previously mentioned, the LPNC generates sinusoidal waveform. As a sampling clock, the slew rate may be insufficient from the low jitter's point of view. So usage of the differential mode would be preferable. A clock interface circuit such as diode limiters may be required for full-scale swing. As a test signal, the harmonics distortion should be carefully suppressed. Good BPF is indispensable on the board. A signal interface circuit may be required for successful results.

Testing High-Speed ADCs for Consumer Devices

The discussion is about testing of high-speed ADCs for consumer video applications. The sampling clock jitter and the test signal phase jitter are highlighted in particular. These jitters are converted to the ADC conversion error that is equivalent to noise in the output codes. So the jitters influence to the SNR performance that is ENOB. The equation $SNR[\text{dB}] = -20\log(2\pi \cdot F_{signal} \cdot JitterRMS)$ describes the performance limit by the jitter-based SNR. When considering the sampling clock jitter and the phase noise of the signal, you should watch the test signal frequency, not the sampling frequency; particularly paying attention to under-sampling status.

The low phase noise clock in the Verigy V93000 SOC test system is an appropriate source for both the sampling clock and the test signal. The experiment proves that it is capable of providing ENOB > 11 bits performance in a video application ADC testing. ●

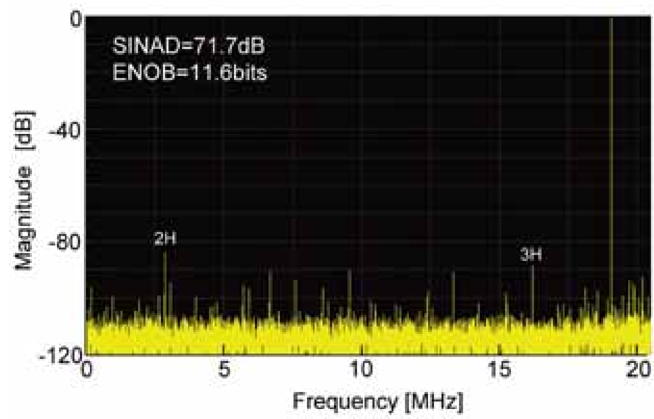


Figure 8: Measurement result: FFT spectrum

BOUNDARY-SCAN TESTING PUSHES INTO THE DESIGN & DEVELOPMENT COMMUNITY

JAMES STANBRIDGE, UK SALES MANAGER AT JTAG TECHNOLOGIES, RETURNS TO OUR PAGES TO RECOUNT A NUMBER OF INTERESTING DEVELOPMENTS WITH BOUNDARY-SCAN TOOLS

Time certainly flies in our fast-paced electronics industry, which makes it almost five years since I offered an overview of boundary scan (a.k.a. IEEE Std. 1149.1 and as JTAG, after the Joint Test Action Group that developed it) for Electronics World's November 2006 issue.

While the basic, so-called 'dot 1' standard has not changed at all during the past five years – although there are some proposals outstanding by the current working party – there have been several exciting developments with regards to tools. Indeed, both the hardware and software solutions that allow engineers to harness the embedded boundary-scan in their existing designs (for board testing and the programming of devices) have developed at a pace.

Also, and perhaps most interestingly, boundary scan has pushed further into the 'development space' as the industry provides lower cost and in some cases free debug tools. This has made the technology available to even the most modest of electronic engineering departments, and even the keen hobbyist.

As mentioned in the earlier article, the boundary-scan test architecture was first devised more than 20 years ago by an ad hoc group, made up chiefly of seasoned test and production engineers. At that time their main aim was to solve perceived problems building and testing PCBs that would (at the time) soon start using Surface Mount Technology (SMT) components.

As the JTAG standard gained acceptance throughout the 1990s, a number of (boundary-scan) tool vendors introduced solutions to make life easier for test engineers who were looking to add JTAG board testing into their regime. With such tools, engineers could extract basic design information from their design team's EDA tools and quickly create structural tests for detecting short and open circuits, plus perform simple logic tests.

Over the years the tools have improved in many aspects, including overall effectiveness, quality of test generation, ease-of-use and integration with other test methods, such as flying probe, bed-of-nails and functional test. However, in nearly all cases, the improvements and enhancements were aimed at test engineers and the tools themselves attracted a price tag that was considered a 'reasonable' expense for optimising (volume) production processes.

> A number of (boundary-scan) tool vendors introduced solutions to make life easier for test engineers who were looking to add JTAG board testing into their regime

Accordingly, the tools remained inaccessible to other interested parties; most notably design engineers who wanted to benefit from the power of boundary-scan, and the 'access to silicon' it affords, but could not justify investment in a 'production tool'.

Low-Cost and Even No-Cost JTAG Tools

Whilst boundary-scan was developed primarily as a structural test technique for production purposes, the JTAG Test Access Port (TAP – described against Figure 1) was soon being used for other functions – specifically by the silicon vendors themselves. It is for this reason that the term JTAG is sometimes confusing, as it means different things to different industry groups.

For example, most designers using programmable logic will be familiar with JTAG as an in-circuit programming port for the devices of Altera, Lattice, Cypress, Xilinx and other PLD vendors. Similarly, designers of embedded systems will no doubt know JTAG as a means of accessing the on-chip debug features within microprocessor, RISC and DSP cores.

Today though, a growing number of designers are realising the true potential of the 'hidden' boundary-scan features, utilising this function as a means of debugging prototype hardware; though often without a large production tools budget.

Late 2009 saw a step-change in the world of boundary scan when a family of no-cost/low-cost boundary-scan debug tools called JTAG Live (www.jtaglive.com) were launched. These were, for the first time, aimed more at design engineers, and are able to make use of existing design interface hardware such as Altera's USB Blaster and Xilinx's programming cables. What's more, the basic ingredients needed to set up these tools are simply the Boundary-Scan Description Language (BSDL) device model files. No other EDA information such as a netlist or BOM is required to start testing.

For any design that features one or more boundary-scan compliant components designers can choose from three debug tools depending on their needs or budget.

The first is a tool called Buzz, so called as it affords practically instant pin-to-pin continuity tests (a la 'buzzing out'). Also, up to 10 nets can be exercised in a Measure mode and a boundary-scan SAMPLE instruction can be used to monitor activity on any given pin (a la logic probe). What's more, Buzz is free (see box).

A second tool, called Clip, allows the user to build more complex vector-based cluster test sequences. Each vector in a sequence can contain a set of drive values for device inputs and the corresponding sensed values on the device outputs. A timing-style waveform display shows the I/O vectors and by storing the sequence for a known-good board it is possible to create a test for boards of the same type.

The vector sets can be expressed in Hex, Binary or Decimal formats for many types of debug applications, such as Flash ID-code testing or testing I2C and SPI bus protocol parts. If you can access the critical signals of your device with boundary-scan enabled pins then you can most likely test it with Clip. Vector sets can be up to unlimited patterns long and with no limit to the number of pins used. Built in vector generation modes include Walk 1, Walk 0 and Binary count.

The third tool, Script, provides a command and control structure to manipulate and sense cluster I/Os. Specifically, it can be used for functional, device-orientated test. For example, it can be used for mixed signal parts, operations that require user intervention or looping test patterns to set up device registers.

Script uses the open-source Python programming language popular throughout the engineering world due to its easy syntax yet powerful data manipulation capabilities.

IMPLEMENTING BOUNDARY SCAN

ESSENTIALLY, THE TEST DATA OUT (TDO) OF ONE DEVICE CONNECTS TO THE TEST DATA IN (TDI) OF THE NEXT, AND SO ON. Test Clock (TCK) and Test Mode Select (TMS) are effectively in parallel. A fifth pin/pad may be present on some boundary-scan devices. Called TRST it offers an asynchronous reset capability. However, device reset can also be achieved using the 'soft method' of holding TMS high for five clock cycles.

The four or five boundary-scan signals will terminate at a Test Access Port (TAP) on the board.

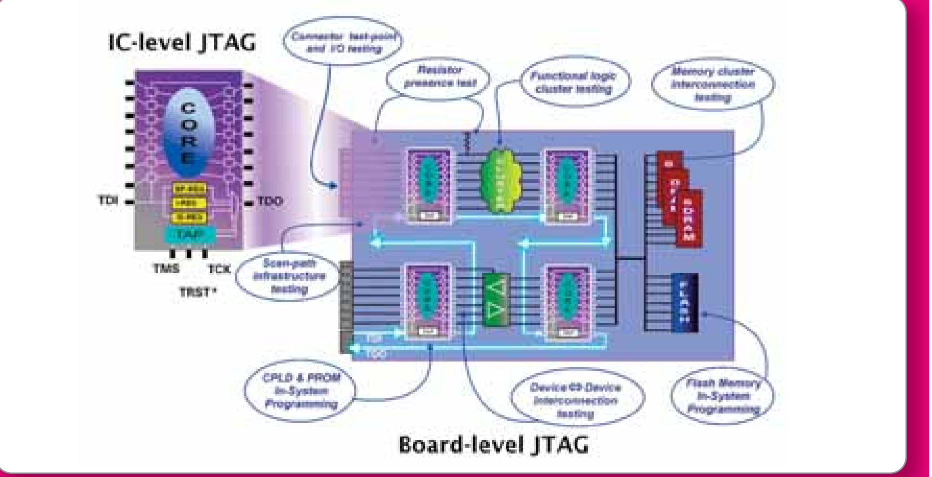


Figure 1: A reminder from JTAG Technologies's 2006 article on how boundary scan is implemented within a device and how boundary-scan components can be daisy-chained together at the board level

Device Types:

	Device Type	Model File	Model Name	Package
1	74LS08	generic_logic\ttl_08.model	TTL08	SO-14
2	74LS132	generic_logic\ttl_132.model	TTL132	SO-14
3	74LS138	generic_logic\ttl_138.model	TTL138	SO-16
4	CAPACITOR	generic_passive\capacitor.model	CAPACITOR	
5	COIL	generic_passive\inductor.model	INDUCTOR	
6	HDR_10	generic_passive\connector.model	CONNECTOR	
7	HDR_40	generic_passive\connector.model	CONNECTOR	
8	ISPLSI2064VE	2064vet1_isc_v_1_0.bsd	ispLSI2064VE_XXLT100	TQFP_100
9	JUMPER	generic_passive\jumper_3pin.model	JUMPER3	
10	K6T1008C2E	generic_memory\sram_async_1mbit_128kx8_2cs.model	SRAM128kx8	TSOP-32
11	M29F010B(N)	st\m29f010b.model	M29F010B	TSOP-32
12	MAX604	maxim\max604.model	MAX604	SO-8

Figure 2: Assigning ProVision and BSDL models to the netlist-defined device types

Figure 3: The Truth Table Reporter (TTR) for visualising faults such as net or pin 'stuck-at' faults or net shorts

Creating test modules in Script promotes device-orientated testing and hence re-use of test code. Using Python open source means that thousands of auxiliary routines can be obtained from a now well-established user community.

Whilst only the Buzz tool is free (see box), Clip and Script remain in the same price bracket as their counterpart bench-top instruments.

The Middle Ground

In addition to the arrival of free tools the industry is also experiencing an influx of attractively-priced software and hardware 'bundles', aimed at the designer-cum-test engineer. ProVision Designer Station (PV_DST) for example, launched in 2010, is pitched as a flexible, low-cost development system for the preparation of all boundary-scan test routines.

It incorporates a highly automated, test program generator for infrastructure and interconnects that take advantage of a library of thousands of non-boundary-scan (a.k.a. 'cluster') device models to create a safe, high-quality core test.

It also includes a number of features for developing cluster tests and device programming applications with standard features such as: Serial Vector Format (SVF) program file executors; Python language module scripting with netlist aware 'bind' feature; and ActiveTest interactive test generator to add more sophisticated test options for logic clusters and device programming.

In the next few paragraphs you can see how the 'fill-in-the blanks' approach of PV_DST allows the user to get control of the boundary-scan capability embedded in their design.

Following start-up, a project wizard prompts the user to add netlist information that is usually gathered from the designer's schematic entry tool. Multiple netlists can be added to an individual project making it simple to support 'stacked' designs comprising main boards and mezzanine cards and/or system cards in a plug-in back-plane.

To complete the picture, device models are then assigned to the netlist-derived device types list (as per Figure 2). Models are of either BSDL-type (with .bsd extensions), in the case of the JTAG devices, or ProVision models (with .model extensions) for the non-JTAG (cluster) devices. A built-in model editor allows the user to construct their own device disable models should the need arise. To aid re-use, the device model assignments can be exported as a model map and kept for use in future projects.

A REAL BUZZ FOR BOUNDARY-SCAN

JTAG LIVE BUZZ'S THREE MAIN TOOLS IN ACTION

'Watch' is a sample mode used to view the activity on the pin of a device. 'Buzz' is effectively a pin-to-pin connectivity check, and 'Measure' is window for setting up 10 drivers (on pins) and sensing logic levels on up to 10 other pins (so is great for verifying combinatorial logic).

Buzz is free and available via download from www.jtaglive.com, which also includes product descriptions, answers to frequently asked questions and highlighted experiences from JTAG Live users.

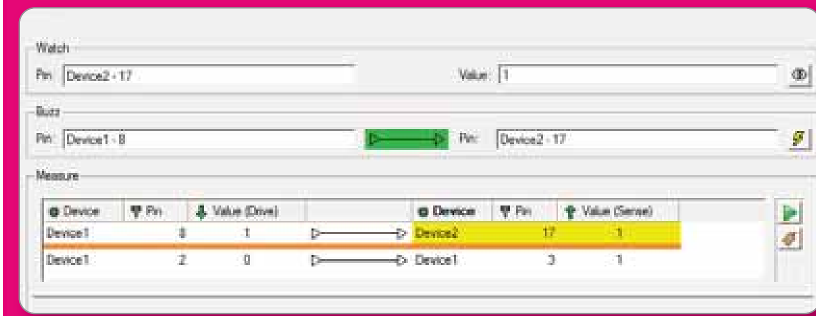


Figure 4: Screenshot of JTAG Live Buzz

With models assigned invoking the automatic program generator for interconnect, testing is a fully guided process. The generator dialogue box also offers a number of test pattern options for the advanced user.

> *Script uses the open-source Python programming language popular throughout the engineering world due to its easy syntax yet powerful data manipulation capabilities*

Following a test execution, results are displayed in a Truth Table Reporter (TTR – see Figure 3). Each net is displayed showing the status of each boundary-scan driver/sensor at each vector level. Any sensor error is highlighted to enable speedy identification of faults such as net or pin 'stuck-at' faults or net shorts. TTR also features advanced modes such as device-by-device vector displaying.

An interconnect test can often contribute over 80% of a digital board's fault coverage if most of the high pin-count parts are JTAG (IEEE Std.1149.1) compliant. Moreover, using the JFT and/or ActiveTest modules users can 'top-up' the fault coverage to get figures of up to 95% of nets and pins tested using boundary-scan by implementing cluster tests (a type of functional test targeted at a specific device or device group).

Cluster tests typically target devices such as memories, flash parts, SPROMs, Ethernet PHYs and other register-based parts and can be used for structural test as well as in-system programming. Of course there will always be a proportion of interconnects such as power connections to regulator parts etc not tested, however it is likely these will have been inspected visually and/or tested functionally.

The Future

As more and more designers see the benefits of improved time-to-market due to a less frustrating debug phase, the use of JTAG for hardware debug is expected to increase rapidly and the cost of tools will fall even further. In the near future you can also expect that on-chip debug features of chips will provide further opportunities to increase test coverage via the now venerable JTAG port. ●

DEPLOYING LTE – HOW TO ENSURE YOU GET IT RIGHT FIRST TIME

MANUEL MATO, REGIONAL VICE PRESIDENT FOR EMEA AT THE JDSU COMMUNICATIONS TEST AND MEASUREMENT BUSINESS SEGMENT, EXPLAINS HOW IMPORTANT IT IS FOR OPERATORS TO HAVE A ROBUST TEST AND MEASUREMENT REGIME IN PLACE WHEN UPGRADING TO LTE

The telecoms world is currently in something of an upheaval as the 3G networks we have been using since the second half of the 'noughties' are being replaced by LTE – the next generation of mobile connectivity. Carriers are moving to LTE to deliver the huge increases in traffic volume that the market is demanding, but this move is by no means a simple process. As with any major technology rollout, the technical challenges involved are huge, not least from a test and measurement perspective.

Carriers face the challenge of implementing LTE while meeting the demands of exacting users that will be quick to migrate to other providers if they perceive any drop in standards or performance. With the right approach to LTE test and measurement, however, operators can maintain high Quality of Service (QoS) while minimising capital expenditures and operating costs.

LTE appeals to operators as it not only offers large improvements in performance, but also has the ability to coexist with earlier network standards. LTE capabilities include:

- Downlink peak data rates up to 326Mbps with 20MHz bandwidth;
- Uplink peak data rates up to 86.4Mbps with 20MHz bandwidth;
- Operation in both time division duplex (TDD) and frequency division duplex (FDD) modes;
- Scalable bandwidth covering 1.4, 3, 5, 10, 15 and 20MHz;
- Increased spectral efficiency of between two and four to one relative to HSPA;
- Latency of no more than 10 milliseconds round-trip times between user equipment and the base station.

But these performance gains cannot be taken for granted. It is only with a rigorous test and measurement regime they can be realised. Below are some of the main factors operators should bear in mind when rolling out their next generation of mobile networks.

Ensuring that LTE Delivers on its Promise

1) Understanding changes to the radio and core networks

In order to achieve these performance gains, LTE introduces major changes to the existing radio access and core networks relative to previous generation CDMA and 3GPP deployments. The previous generation base station is replaced by the new eNodeB and the core network is replaced by a new Evolved Packet Core (EPC). Orthogonal Frequency Division Multiplexing (OFDM) radio access is used on the downlink and Signal-Carrier Frequency-Division Multiple Access (SCFDMA) provides the uplink. Multiple Input Multiple Output (MIMO) antenna technology is used on both the uplink and the downlink.

The combination of time-compressed deployments along with the complexity and novelty of LTE creates greater potential for QoS issues than 3G networks. As service providers strive to be first to market with high quality services, they must troubleshoot and manage issues to meet the exacting demands of the discriminating customers that are the first to adopt LTE. These challenges are complicated by the high number of test points that must be monitored and the huge volumes of data that need to be correlated across the network. LTE's complexity means there are far more interfaces that need to be tapped for the relevant data and that the signalling that goes with service delivery is much more complex.

2) The importance of successful trials

Operators are faced with the challenge of successfully planning and executing LTE trials and then getting to first deployment. Trial logistics are complex. The trial team must set the framework, communicate with all network equipment manufacturers (NEMs), police the NEMs during the trial, run test cases in a uniform way, capture and evaluate huge volumes of data, and adapt when something goes wrong. Solving the problems that occur during these trials will allow service providers to move out of initial deployments in time to beat competitors to market.

Figure 1: JDSU's leading drive test solutions for the optimisation of wireless networks and data services

Figure 2: JDSU Signal Analyser Real Time (SART) is shown here benchmarking LTE performance

Fully integrated test platforms that provide on-the-fly measurements from the radio access network to the network core are needed to provide measurements during LTE trials. These tools enable trial teams to replicate services in as many different scenarios and environments as are practical for all relevant standards and on different frequency bands. Testing can verify all functions critical to future LTE services, including data capacity and throughput, network coverage, end-to-end network latency, seamless handover with legacy networks, interoperability of multi-vendor devices and QoS. The latest testing tools support LSTI Field Trial Test Cases, flexible key performance indicators (KPIs), correlation of user plane and control plane data, interactive measurements with preferred UE devices and the latest permutations of LTE standards. The tools work for all vendors' equipment and enable "apple to apple" comparisons. The result is that operators are enabled to make LTE equipment purchasing decisions on objective criteria.

3) Maintaining high QoS

Because of the complexity of LTE technology and with the introduction of new services, there is greater potential for QoS issues than with 3G networks. Service providers must ensure that they can identify and troubleshoot any user, service or network problem in a very short period of time in order to deliver the highest possible standard of customer care. Network monitoring can help by delivering KPIs that provide real-time information on LTE performance and an end-to-end view that enables fast root cause diagnosis so the problem can be corrected before it affects customer satisfaction.

The new generation of service assurance solutions enables mobile operators to track an extensive set of KPIs, including network performance and data service quality, to manage network infrastructure and deliver an outstanding customer experience. Easily configured KPIs and thresholds pinpoint critical service and network problems. That means complex network-wide service information is automatically interpreted and correlated. This information is then presented in a simplified way with guided analysis to assist in problem resolution. These capabilities empower installation and maintenance teams to effectively and accurately identify and diagnose service problems.

Given LTE's complexity and high traffic volume, operators can maximise the efficiency of network assurance and minimise operating expenses by focusing on the right KPIs and the essential data. Hundreds of KPIs will overwhelm operations teams so carriers should look to monitor just the service-focused KPIs that are important to their business. Composite KPIs can reduce the number of KPIs without losing detail while providing flexibility about what sequence of messages a KPI relates to. Operators will most likely need to capture all of the control plane data but can be more flexible about the user plane. An intuitive interface makes it easy to understand signalling messages and clearly highlights failures. On-line real-time filtering allows users to narrow investigations to focus on events related to a cause and provides a sequence diagram for each failure, enabling faster diagnosis.

Newer assurance tools go one step further by analysing subscribers' networks and service interactions, correlating these transactions into a single context and tracing them from real time to several weeks in the past. For example, successfully setting up a call requires that many different individual transactions be completed across the entire network. Effective troubleshooting demands that this series of inter-related transactions be presented in a single end-to-end view of the complete LTE network. This view enables the operations team to diagnose complex issues quickly and reliably to ensure customer satisfaction and protect revenues.

For example, a call setup requires many separate transactions across an entire network. The latest generation of service assurance solutions correlates all the elements into one complete bundle to provide an end-to-end view of the complete LTE network. As an example, a pictorial sequence diagram of a subscriber's session enables the user to perform detailed analysis of signalling procedures. The application provides a historical analysis of each subscriber's interaction with the LTE network. This approach moves troubleshooting from a niche area occupied by handful of specialists into one in which less skilled users are able to effectively diagnose problems. The result is a substantial improvement in operating efficiency in the fault management lifecycle.

> Fully integrated test platforms that provide on-the-fly measurements from the radio access network to the network core are needed to provide measurements during LTE trials

Testing Times Ahead

LTE offer operators a wealth of opportunity for scaling their networks and ensuring there is enough capacity to support the bandwidth-heavy demands of the modern consumer. The upgrade to LTE networks, however, also involves increasing the complexity of the monitoring and troubleshooting processes for the mobile data services that will run over them. It is clear that operators must ensure they have a robust test and measurement regime and a planned set of trials to effectively solve any problems that may occur prior to launch. The test equipment available today can help operators with their LTE deployments by allowing them to evaluate and deploy equipment that meets specifications and quality standards, verify new services and accelerate problem resolution times. ●

PRECISION MEASUREMENT AND LOGGING OF THE MAINS FREQUENCY

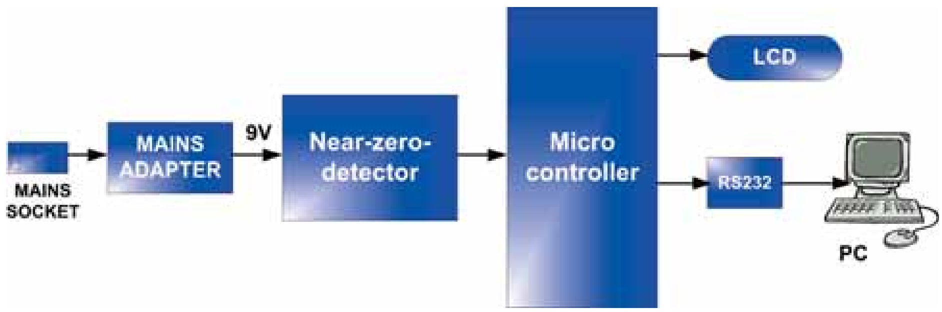
PROFESSOR DR DOGAN IBRAHIM OF THE NEAR EAST UNIVERSITY IN CYPRUS DESCRIBES THE DESIGN OF A PRECISION MICROCONTROLLER-BASED DEVICE FOR MEASURING AND LOGGING THE MAINS FREQUENCY

There are several mains power systems in use around the world. These different systems are characterised by their:

- Voltage;
- Frequency;
- Type of plugs and sockets used.

In general, the type of plugs and sockets used is not a problem, and passive adapters are available to convert between different varieties, as long as the voltage and frequency are correct for the electrical device to be used.

Figure 1: Block diagram of the frequency monitoring device



In general, we can divide the mains voltage and frequency usage in the world into four groups:

- 100-127V, 50Hz
- 100-127V, 60Hz
- 220-240V, 50Hz
- 220-240V, 60Hz

The voltage quoted is the root mean square, and the peak voltage can be calculated by multiplying the voltage with $\sqrt{2}$, or the peak-to-peak voltage is found by multiplying with $2\sqrt{2}$. The frequency used in mains electricity is either 50Hz (20ms period) sinusoidal or 60Hz (16.66ms period) sinusoidal. Table 1 gives a short list of some of the mains voltages and frequencies used around the world.

Incorrect Mains Voltage

Some of the appliances we use at home may be affected if the mains voltage is not correct. For example, the motor speed of some CD players may be affected, even though the motor supply voltage is regulated. The result of this is that the music can play slightly slower or faster. Also, some more sensitive appliances, such as televisions, may not operate correctly if the mains voltage is lowered.

Incorrect Mains Frequency

As the demand on the electricity supply increases the frequency usually drops. The electricity suppliers monitor the mains frequency constantly and aim to keep it within the allowed tolerances. A change in the mains frequency has negative effects in some of the appliances. For example, the speed of AC synchronous motors depend upon the supply frequency, and any appliance such as a turntable using such a motor will run slower or faster depending upon the changes. Also, some home or industrial clocks operate by counting the

Country	Voltage	Frequency
Argentina	220V	50Hz
Australia	230V	50Hz
Belgium	230V	50Hz
Canada	120V	60Hz
Denmark	230V	50Hz
Egypt	220V	50Hz
France	230V	50Hz
Germany	230V	50Hz
India	230V	50Hz
Israel	230V	50Hz
Japan	100V	50Hz, 60Hz
Libya	127V	50Hz
Portugal	220V	50Hz
Turkey	230V	50Hz
UK	240V	50Hz
USA	120V	60Hz
Venezuela	120V	60Hz

Table 1: Mains voltages and frequencies around the world

mains pulses and such clocks will run slower or faster depending upon the changes in the supply frequency.

The UK Mains Supply Tolerance

By law, the Electricity Board is required to supply 230V + 10%, -6%. i.e. between 216.2 volts and 253 volts. In addition, the frequency is required to be maintained at 50Hz ± 1%. i.e. between 49Hz and 51Hz. The European standard supply voltage is 220V and back in 2008 it was decided to change the European standard voltage to 230V and also the UK mains voltage to 230V. Although this sounded easy in theory, in practise it was too costly and uneconomic to change all the supply equipment to give 230V. Instead, the voltage limits were changed in UK, and the UK voltage was kept at 240V which is within the allowed limits of 230V + 10% ,-6%. At the same time, the European standard was left at 220V.

MONITORING THE MAINS FREQUENCY

The expected variation of the mains frequency (in UK) is between 49Hz and 51Hz. The mains frequency can, in practise, be measured using a simple frequency counter. But here the problem is that we need to measure very small changes, in the order of less than 0.01% and the cost of frequency counters to measure such small changes are rather high. In addition, we usually want to log the variations of the mains frequency over long periods of time and then to analyse these changes by for example plotting the results. Most low-cost frequency counters are not capable of logging the frequency changes.

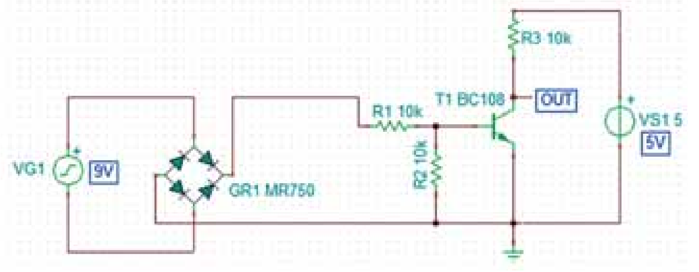
In this article, the design of a microcontroller-based mains frequency measuring and logging device is given. The device has an LCD display that shows the changes in real-time. In addition, the frequency data is sent to a PC over the RS232 serial port and stored in a file on the PC. The stored data can easily be analysed for example by plotting it or by using a statistical analysis package such as Excel.

THE HARDWARE

There are basically two methods used in the literature for frequency measurement. The first method, which is not accurate, involves setting up a time window and calculating the number of cycles within this window. The second method, which is more accurate and is the one used in this article, involves calculating the period of the waveform. Here, basically an accurate timer is used to measure the period and hence calculate the frequency of the waveform.

The block diagram of the designed mains frequency monitoring device is shown in Figure 1. The operation of the device is based on a near-zero-cross-detector circuit. Mains supply is reduced to 9V using a wall mains adapter. As shown in Figure 2, the near-zero-cross-detector circuit is made up of a bridge rectifier and a transistor. Full-wave rectified mains signal is applied to the base of the transistor. The transistor is normally on and its output is low when the signal is high. As the signal drops to 0.7V, the transistor turns off and the collector voltage rises to the supply voltage (+5V), generating a pulse. Figure 3 shows the rectifier output and the transistor output. As shown in the figure, three such pulses are obtained during a full period of the mains frequency. These pulses are then fed to one of the inputs of a PIC microcontroller. The microcontroller starts an accurate timer when a pulse arrives. The timer is stopped at the arrival of the third pulse. Thus, the timer count is proportional to the period and hence to the frequency of the waveform. This timer count is converted into real frequency and is displayed on an LCD display. In addition, the data is sent to a PC using the serial RS232 port.

Figure 2: The near-zero-cross-detector circuit

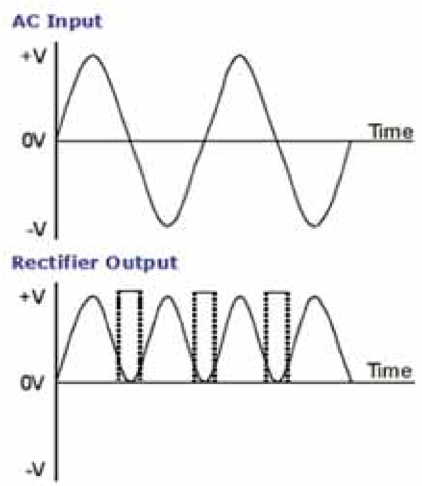


A Visual Basic program on the PC receives the frequency data, time stamps the data and then stores it in a file. The frequency data can be displayed by the Visual Basic program, or for more flexibility and statistical analysis it can easily be imported into Excel and analysed or displayed.

Although the near-zero-cross-detector circuit does not detect the exact zero crossing point of the signal, it generates pulses at the same near zero points of the waveform, thus making it possible to accurately measure the signal period. Figure 4 shows simulation of the near-zero-cross detection circuit. The circuit was simulated using the popular TINA circuit simulation suite, developed by DesignSoft (www.tina.com). Figure 4 shows the rectified full-wave mains waveform together with the output pulses of the near-zero-detector circuit on a virtual oscilloscope of TINA.

Figure 5 shows full circuit diagram of the device. A PIC18F4520

Figure 3: Three pulses are obtained in one cycle of the mains waveform



> *The European standard supply voltage is 220V and back in 2008 it was decided to change the European standard voltage to 230V and also the UK mains voltage to 230V*

Figure 4: Simulation of the near-zero-detector circuit

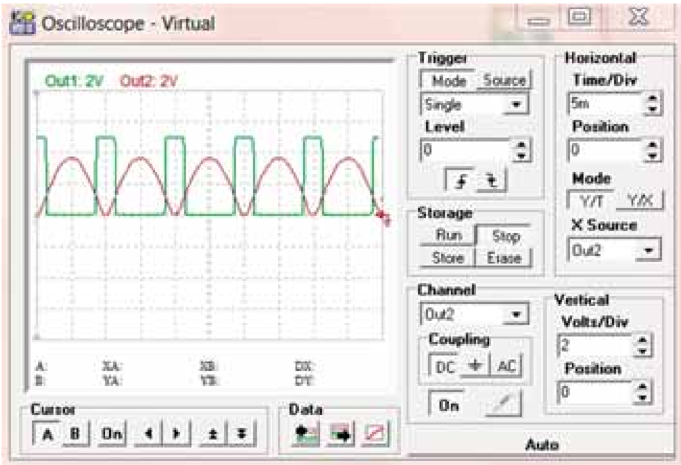
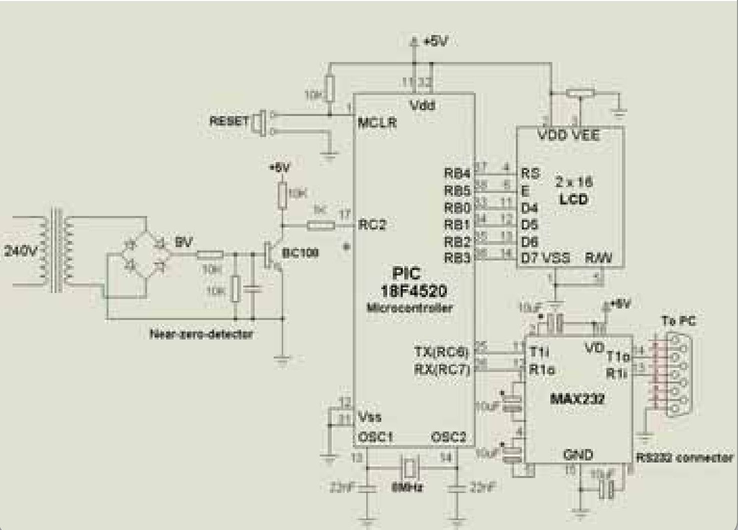


Figure 5: Circuit diagram of the monitoring device



microcontroller (www.microchip.com) is used in the design with the timing provided with an 8MHz crystal. PORT B of the microcontroller is connected to a 2x16 LCD display. UART output pin (RC6) is connected to a MAX232 type (www.maxim-ic.com) RS232-TTL converter chip and then to the PC serial port via a 9-pin D-type connector. Output pulses of the near-zero-detector circuit are fed to port pin RC2 of the microcontroller.

The project was built and tested using the EasyPIC6 microcontroller development board (www.mikroe.com). A small breadboard was used to construct the near-zero-detector circuit.

OPERATION IN DETAIL

The output pulses of the near-zero-detector circuit are counted using 16-bit timer/counter TMR1 of the microcontroller. With an 8MHz crystal, the counting period is 0.5μs and maximum count is 65535. In a perfect 50Hz signal, with 20ms period, the maximum count will be 40,000. Table 2 shows the counter values at different frequencies of the mains supply. The frequency (*f*) of the waveform is then given in Hz by:

$$f = \frac{2x10^6}{count}$$

By considering that a difference of one count can be measured, the accuracy of the frequency measurement is then given by approximately 0.001Hz, or 0.002%.

THE SOFTWARE

The software consists of the microcontroller software (or the measuring software) and the PC software (or the data logging software).

Microcontroller Software

Figure 6 shows operation of the microcontroller software. Counter TMR1 is cleared and internal counting starts on the high-to-low transition of the input pulse on pin RC2. The counting continues until the third pulse is detected, and stops on the high-to-low transition of the third pulse. The frequency is then calculated using the equation given above. Floating point calculations are used in the program for high accuracy.

The calculated frequency is displayed on the LCD as well as it is sent to the PC over the serial link. This process is repeated forever with a 5-second delay between each measurement. Parts of the program are written in Assembly language so that the pulse edges can be captured accurately. Figure 7 shows a typical display of the measured frequency.

```
BEGIN
        Initialise global program variables
        Configure LCD
        Configure UART
        DO FOREVER
                Wait until first low-to-high transition
                of the pulse
                Clear timer/counter TMR1
                Start timer/counter TMR1
                Wait until second low-to-high
                transition of the pulse
                Wait until third low-to-high
                transition of the pulse
                Get timer/counter value
                Calculate the frequency
                Display frequency on LCD
                Send frequency to RS232 port
                Wait 5 seconds
        ENDDO
END
```

Figure 6: Operation of the microcontroller software

Figure 7: Typical display of the measured frequency

The microcontroller software is based on the mikroC (www.mikroe.com) language. The full microcontroller program listing is given in Figure 8.

Frequency (Hz)	Counter value
49.0	40816
49.2	40650
49.4	40485
49.6	40322
49.8	40160
50.0	40000
50.2	39840
50.4	39682
50.6	39525
50.8	39370
51.0	39215

Table 2: Frequency and counter values

```
/********************************************************
Author: Dogan Ibrahim
Date: January 2011
File: Mains frequency.C
********************************************************/
unsigned int TimerValue;
const float num = 2000000.0;
float Frequency;
char Txt[15];

// LCD module connections
sbit LCD_RS at RB4_bit;
sbit LCD_EN at RB5_bit;
sbit LCD_D4 at RB0_bit;
sbit LCD_D5 at RB1_bit;
sbit LCD_D6 at RB2_bit;
sbit LCD_D7 at RB3_bit;

sbit LCD_RS_Direction at TRISB4_bit;
sbit LCD_EN_Direction at TRISB5_bit;
sbit LCD_D4_Direction at TRISB0_bit;
sbit LCD_D5_Direction at TRISB1_bit;
sbit LCD_D6_Direction at TRISB2_bit;
sbit LCD_D7_Direction at TRISB3_bit;
// End LCD module connections

void main()
{
//
// Timer 1 in 16 bit mode with prescaler=1, use internal
clock
//
 T1CON = 0x80;
 TRISC=4;
 ADCON1 = 0x0F;

 Uart1_Init(4800);
 Lcd_Init();

 for(;;)
 {
 Lcd_Out(1,1,"MAINS FREQUENCY");
 asm {
 b1:
 btfss PORTC,2
 goto b1
 b2:
 btfsc PORTC,2
 goto b2

 movlw 0                              // Clear
Timer1
 movwf TMR1H
 movwf TMR1L
 bsf T1CON,0                          // Start
timer1
 b3:
 btfss PORTC,2                   // Wait for 1 period
 goto b3
 b4:
 btfsc PORTC,2
 goto b4
 b5:
 btfss PORTC,2
 goto b5
 b6:
 btfsc PORTC,2
 goto b6

 bcf T1CON,0        // Stop timer
 movff TMR1L, _TimerValue+0 // Read timer value
 movff TMR1H, _TimerValue+1
 }
 //
 // Calculate the frequency and display it
 //
 Frequency = num / TimerValue;
 FloatToStr(Frequency, Txt);
 Lcd_Cmd(_LCD_CLEAR);            // Clear LCD
 Lcd_Out(1,1,"F = ");            // Display heading on
LCD
 Lcd_Out(1,5,Txt);
 Uart1_Write_Text(Txt);
 Uart1_Write(10);
 Uart1_Write(13);
 Delay_ms(5000);                 // Wait for 5 seconds
 }
}
```

Figure 8: Microcontroller program listing

PC Software

The PC software reads measured frequencies from the microcontroller, inserts the current date and time, and then stores the time-stamped data in a file on the PC for offline processing. This program is based on Visual Basic 6 (www.microsoft.com) and the main program form is shown in Figure 9. The user starts and stops data logging by clicking the appropriate buttons. Data is stored with the fields being separated with a comma so that it can easily be imported to other programs. As shown in Figure 9, there is the option of plotting the data after stopping the data collection. However, it is much more flexible to import the collected data to a program such as Excel and perform statistical analysis, or plot the data in greater detail and with more options.

Figure 10 shows a typical plot of the collected data after it is imported into Excel. Here, the data collection time was about 15 minutes.

IMPLEMENTATION OF EMBEDDED ACTIVE RFID

WITH WIRELESS MESH SENSOR NETWORK FOR INDUSTRIAL AUTOMATION

IN THIS ARTICLE, A ZIGBEE TECHNOLOGY PLATFORM IS APPLIED TO A 2.45GHZ ACTIVE RFID SYSTEM TO SUPPORT A WIRELESS MESH NETWORK BY DEVELOPING A FULLY AUTOMATED AND EMBEDDED SYSTEM FOR PRODUCTION MONITORING. BY **CHE ZALINA ZULKIFLI**, **WIDAD ISMAIL** AND **MOHAMMAD GHULAM RAHMAN**

Industrial automation has become very important in the manufacturing industry and as such it is attracting the attention of new technologies to make it more reliable, economic and efficient; technologies such as Wireless Sensor Network (WSN), radio frequency identification (RFID) and web-based monitoring systems.

In this article, a ZigBee technology platform is applied to a 2.45GHz active RFID system to support a wireless mesh network by developing a fully automated and embedded system for production monitoring.

Automated monitoring and control solutions significantly increase manufacturing efficiency by expanding the coverage area and dramatically reducing maintenance costs.

Automated solutions enhance both – data acquisition scope and reliability, and facilitate growth with expansion through the deployment of highly scalable systems.

This article explains the related applications and technology in achieving this goal and then investigates the technical specifications for the hardware and software requirements to develop the proposed automated monitoring system for real-time industrial production using a wireless mesh sensor network.

Widespread Use

Wireless networks are used in many applications, such as the military, education, government service, agriculture, home automation, health and the automotive industry among others. Each of these areas has its own applications, depending on its requirements and specifications. For example, the health and welfare sector needs sensor compactness and wireless connectivity, whereas low cost is imperative for the automotive and home automation sectors.

In this article we are focusing on industrial automation and process control, which have totally different network requirements. In the proposed system, a wireless mesh network is used for industrial monitoring control. Wireless mesh networks combine the reliability of hardwiring with the versatility of wireless networking, even though there's compromise on the speed.

Mesh networks consist of low-cost, battery-powered sensor modules and embedded networking intelligence communication that can hinder an optimal production output. ZigBee is a growing technology that can provide many advantages in industrial automation. Production line activities involve a variety of processes, such as checking the quality of manufactured

> Unlike the ZigBee beacon mode, the ZigBee non-beacon mode is simpler and uses peer-to-peer networks

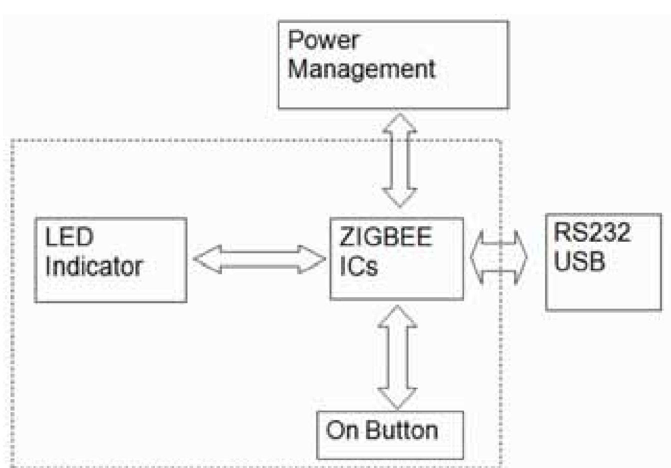


Figure 1: Block diagram of the in-house developed active RFID 2.45GHz reader

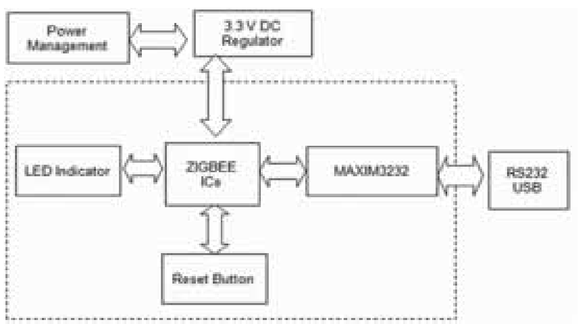


Figure 2: Block diagram of the in-house developed active RFID 2.45GHz tag

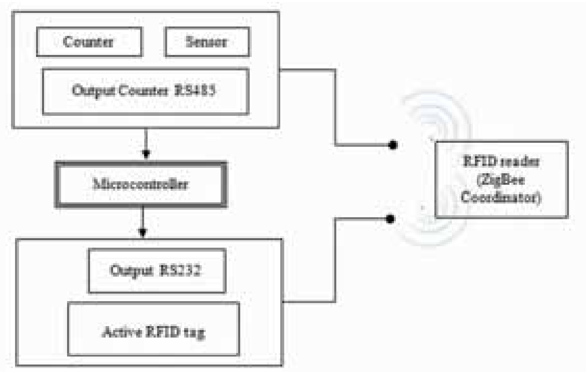


Figure 3: Block diagram of the embedded hardware architecture

ZIGBEE TECHNOLOGY OVERVIEW

THE ZIGBEE SPECIFICATION WAS FINALIZED IN DECEMBER 2004, AND PRODUCTS SUPPORTING THE ZIGBEE STANDARD HAVE ALREADY ENTERED THE MARKET.

ZigBee is designed as a low-cost, power-saving and low-data rate wireless mesh technology. Its features include self-organization, support for multi-hop routed networking topologies, interoperable application profiles and Advanced Encryption Standard (AES) based security. ZigBee is a type of LR-WPAN technology and its lower layers are based on the IEEE 802.15.4 LR-WPAN standard.

ZigBee-compliant products operate in unlicensed bands worldwide, such as 2.4GHz (global), 902-928MHz (America) and 868MHz (Europe). Raw data throughput rates of 250kbps can be achieved at 2.4GHz (16 channels), 40kbps at 915MHz (10 channels) and 20kbps at 868MHz (1 channel).

ZigBee operates in two main modes: non-beacon mode and beacon mode. In beacon mode, the network coordinator will periodically send out a beacon to the devices within its network while controlling the power consumption over wide networks, appearing like a mesh or a cluster tree. In this mode, all the devices will know when to coordinate with one another. Unlike the beacon mode, the non-beacon mode is simpler and uses peer-to-peer networks. Thus, the trait of beacon mode is appropriate in the proposed system, as it is applied as a mesh topology which contains more coordination due to many end devices used in the network.

Compared to Bluetooth technology, the ZigBee data transmission speed is slow, but it can reach speeds up to 250kbps as well as operate in the ISM band. Thus, the trait is appropriate to be used in proposed system for use in an industrial automation environment.

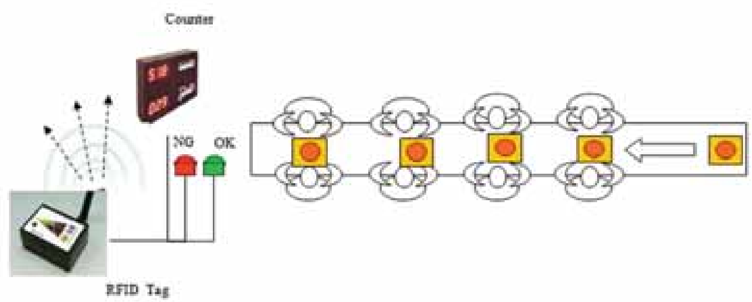


Figure 4: Selected assembly line

products, which has to be manually updated in the production database.

In manufacturing, barcodes are popularly used in most applications. Compared to modern-day RFID technologies, barcodes have several weaknesses including requires human input, plenty of space and restricted data storage, as the barcode is more limited than an RFID tag. Studies show that these technologies are very useful during production monitoring, as they are flexible, offer cost reductions and a minimum use of cables. On top of that they offer sharing of important information among others.

Taking Advantage of Wireless Systems

To take full advantage of the emerging wireless networks, this research focuses on the following difficulties: (1) time constraints, cabling and cost; (2) high-power consumption in the industrial sector; (3) lack of flexibility; (4) multipath reductions; (5) data throughput capacity; (6) configurable operation; (7) network architecture flexibility; (8) node and receiver placement options; (9) operating range; and (10) introducing a smart/intelligent system.

To meet the needs and overcome the difficulties of deploying a fully automated monitoring system of the production output for the industrial sector, we are applying active RFID solutions with the ZigBee technology to support a wireless mesh network in the production area. Moreover, an intelligent web-based monitoring system is introduced in this project.

The implementation of wireless technology in automation systems can reduce the frequency and severity of equipment failures and enable the user to move away from reactive to proactive maintenance. Wireless

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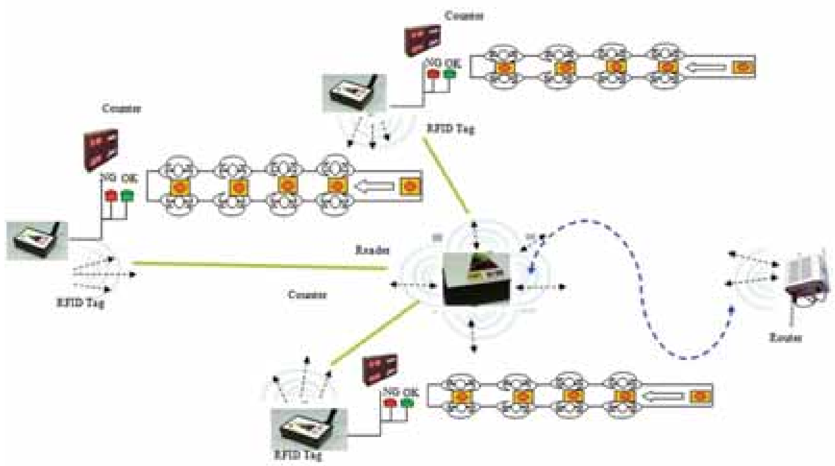


Figure 5: Distribution and integration of several production lines that can communicate via the wireless mesh network

technology enables management to have a proper understanding of the condition of the field and process equipment in real time. This means that the management can only take out unserviceable equipment for repair if and when it is really necessary. As problems are identified early and accurately, interrupting the production process for maintenance would be minimized. Not only does this improve production rates, it also has a very significant impact on the maintenance costs.

More important is the transformation of local plant-floor data into strategic management information. Mesh networks can combine all the relevant data into a database to be accessed by management applications used by plant managers, production managers and, even, executive management.

Wireless Sensor Network (WSN)

Providing full network coverage in large facilities, such as warehouses and factories, typically requires massive lengths of cabling that leads to a questionable return on investment. Wireless Sensor Network (WSN) provides an intelligent platform to gather and collect data from the sensor nodes that can detect and interact with the physical environment.

> We identified interconnection and mapping protocols, handling communication, throughput, diagnostics, preplanning and reliability as the key challenges in implementing a wireless network for industrial automation

Using a wireless mesh as a backbone network simplifies installation and provides an affordable and completely portable solution for both small- and large-scale deployments. In addition to being easy to install, mesh network nodes can be added virtually anywhere an Ethernet is required, including time clocks, scales, surveillance cameras and, even, in moving equipment such as forklifts, cranes and conveyor systems.

Existing manufacturing organizations, so far, have been implementing ordinary monitoring systems. Some organizations use individual LCDs by which only the current operator or worker knows the real-time output, limiting visiblity and transparency. So, based on this Electronic Signage, management needs to go to the production floor to monitor the outputs and to provide workers with different directives. However, to overcome this shortcoming, we propose the Managerial Control and Data Acquisition System (MCDAS) that collects data through the ZigBee technology, where active RFID is embedded to support the wireless mesh network, to develop a fully automated and integrated web-based programming architecture for production monitoring and control systems.

Radio Frequency Identification (RFID)

RFID consists of a transponder, a reader and software. The RFID tag has a microchip with data storage, logical functions and antenna, which receives radio frequency waves produced by the reader or transceiver to permit wireless transmission of data. The RFID reader consists of a radio frequency module, a control unit and a coupling element to question the tags via radio frequency communication.

Readers are usually connected through middleware to a back-end database. The RFID middleware refers to the special software that sits between the reader network and the

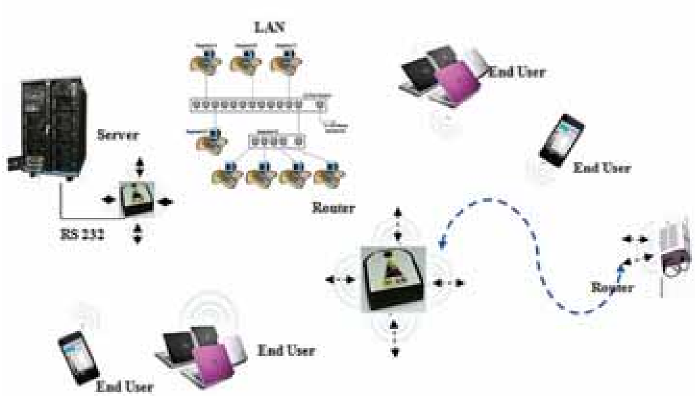


Figure 6: A communication setup linking the reader, server and end user

THALES AGREES SPONSORSHIP TERMS WITH AVIONICS EUROPE 2012

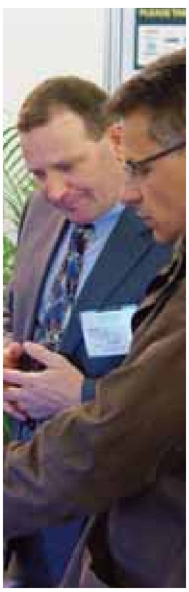
Thales Avionics, a world leader in military and civil avionics, has decided to become a major sponsor and exhibitor at Avionics Europe from 21st–22nd March 2012 in Munich, Germany.

Avionics Europe agreed sponsorship terms with Thales to be the Delegate and Visitor Bag Sponsor, whilst having a significant presence on the exhibition floor, to demonstrate their leading range of systems, products, services and solutions.

Avionics Europe has also gained the support of Association of European Airlines, SESAR and EUROCAE, who will all be hosting 2 hour workshops on a range of topics relating to the Single European Sky initiative and its impact on the avionics industry.

The Avionics Europe conference and exhibition saw a 30% growth in attendance at the 2011 event, highlighting a confident and upbeat return of activity to the aerospace industry following the preceding challenging economic climate.

Avionics Europe, with its industry leading conference programme is unique in delivering high quality presentations and full details of the 2012 conference programme can be viewed at www.avionics-event.com.



AVIONICS EUROPE 2012

AVIONICS EUROPE 2012 celebrates its 10th Anniversary, and once again has the envious title of the premiere conference for avionics. Avionics Europe 2012, for the Commercial and Defence Aerospace Industries, will consist of a trade exhibition, two-day conference programme, workshops, exhibitor presentations and technology demonstrations.

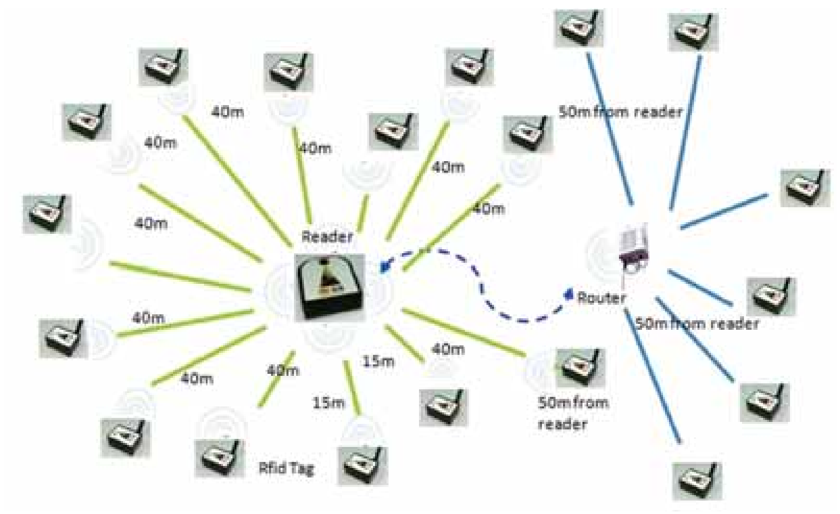


Figure 7: Experimental setup

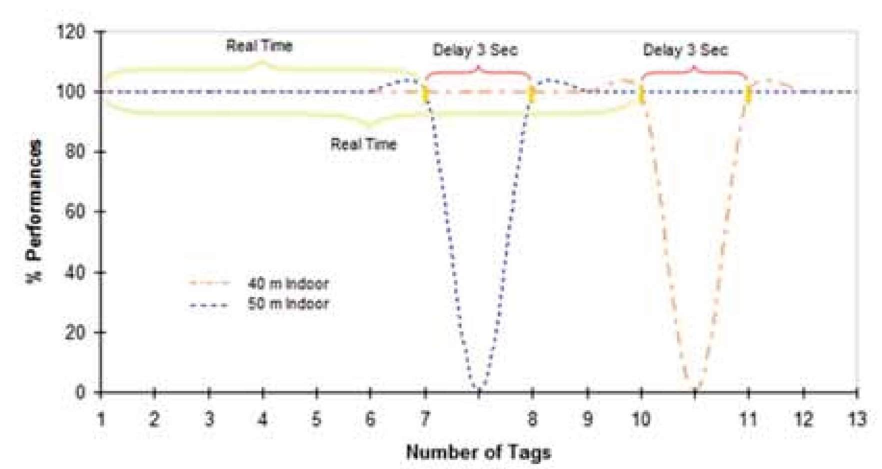


Figure 8: Performance of data acceptance

application software to help with the processing of significant amount of data generated by the reader network. The middleware is responsible for 'cleaning' the data, i.e. eliminating false reads, in addition to performing aggregation and filtering of data. By monitoring multiple readers, the middleware can also detect the movement of RFID tags as they pass between read ranges of different readers.

RFID technology is available in two main types: passive RFID, where the tag is small, low cost and low range, and relies on the reader to provide the energy to power the tag; in active RFID, the tag is larger and offers greater detection range and larger data capacities as it contains its own power source (i.e. battery, or an energy harvesting system).

The application of RFID is used in machine-to-machine communication and as such it is appropriate to be used in our proposed system.

Real-time monitoring system application in industry may require long range tag detection. Since active RFID has the ability to transmit of its own accord on a regular basis over long distances and offers larger memory capacities, we've chosen active RFID for our system.

Here, we are applying an in-house built in, 2.45GHz Contactless Active Integrated RFID (CAIRFID) to support our wireless mesh network. In Figure 1 and Figure 2 are the block diagrams of the proposed CAIRFID reader and tag respectively to be implemented in the proposed system.

Although RFID is a rapidly growing technology that offers many advantages, it also has some challenges that need to be overcome. The most important challenge is managing the RFID data, which is noisy, generated dynamically in very large streams, has limited active lifespan and possesses useful contextual characteristics such as temporality, spatiality and implicit semantics.

The deployment of large-scale RFID applications also introduces unique challenges such as scalability and heterogeneity. In monitoring and data acquisition applications of many items, security is the main issue for RFID applications.

We identified interconnection and mapping protocols, handling communication, throughput, diagnostics, preplanning and reliability as the key challenges in implementing a wireless mesh network for industrial automation. However, in the proposed system, using ZigBee technology may reduce the above mentioned problems as the ZigBee specification provides a standardized set of protocols, services and interface to produce wireless network hardware and software platforms to generate a low-power wireless mesh networking system for monitoring and control.

System Development

Our proposed system is divided into three main parts. The first stage consists developing the data collecting system and its integration. In the second stage, the output of the first part will be transmitted by an active RFID tag to an RFID reader using the ZigBee wireless technology. In this part, it is necessary for the RFID reader to communicate with the database server in real time. The last stage is the web-based monitoring part, where the end user can access the system to view the outputs produced from each line via an Internet access.

Figure 3 provides a block diagram of the embedded hardware between the three main elements for the first stage: the sensor and counter, microcontroller and active RFID tag. There's also a photo sensor integrated with the counter. When the sensor detects the object, it will send the data to the programmable integrated circuit (PIC) to process; the counter then starts to operate. From the PIC, the data is transferred to the active RFID tag. The RFID reader (coordinator) will receive the data from the active RFID tag wirelessly through the ZigBee network.

In Figure 4, the diagram shows an assembly line, and the hardware depicted in Figure 3 will be used at the end of the production line, starting from detecting the output and up until transmitting it wirelessly.

At the end of the line, the photo sensor detects the output produced by the production line. This data is then sent to the PIC for processing. The counter counts the quantity of items produced by each line. The processed data from the PIC is passed to the active RFID tag which communicates with the RFID reader through ZigBee. This active RFID tag updates the data to the reader accordingly when the data from the counter is renewed.

Figure 5 shows the integration of a number of production lines that communicate with the RFID reader through a wireless mesh network. Each line's reader transmits the data wirelessly to the database server, which manages the user requirements. The end user can access the MCDAS system to view the results produced from the production lines accordingly.

In MCDAS, there's a production monitoring software that can be used by a permitted user (for example a plant manager) wishing to view the details and line status of each assembly line. MCDAS allows feedback at any time and from anywhere. With the online production monitoring system, the user can collect data from every station and determine what status have been run, how many units have passed or failed, which station has been utilized, down times, production-line efficiency and so on. The user may see real-time information of all the production lines and models or run station-history reports to evaluate areas where production could be more efficient. It also serves as a schedule utility that can be used by supervisors to set schedules for each line.

Figure 6 shows the communication scenario in the network. As shown here, three types of end users can access the system (for example a plant manager can use a mobile phone).

In our research we conducted several experiments to ascertain capabilities and specifications of the hardware used. Figure 7 shows the experimental setup and Figure 8 shows the performance graph.

Our proposed system also contains a sleep mode function. Sleep modes are supported by the tags only. Router and reader devices participate in routing data packets and are intended to be mains-powered. Tags must be joined to the router or reader before they can operate on the ZigBee network.

The reader or router device does not track when the tag is awake or asleep. Instead, the tag must inform the router or reader when it is able to receive data. The router or reader must be able to buffer incoming data packets destined for the tag until the tag can wake up and receive the data. When the tag is able to receive data, it sends a poll command to the reader or router. When the router or reader receives the poll command, it will transmit any buffered data packets for the tag. Routers and readers are capable of buffering one broadcast transmission for sleeping tags.

From the experiment we've seen that the distance between tags and reader of below or equal to 40m, one reader can receive 100% real-time data from one to ten tags simultaneously. If the tags are placed at random and there

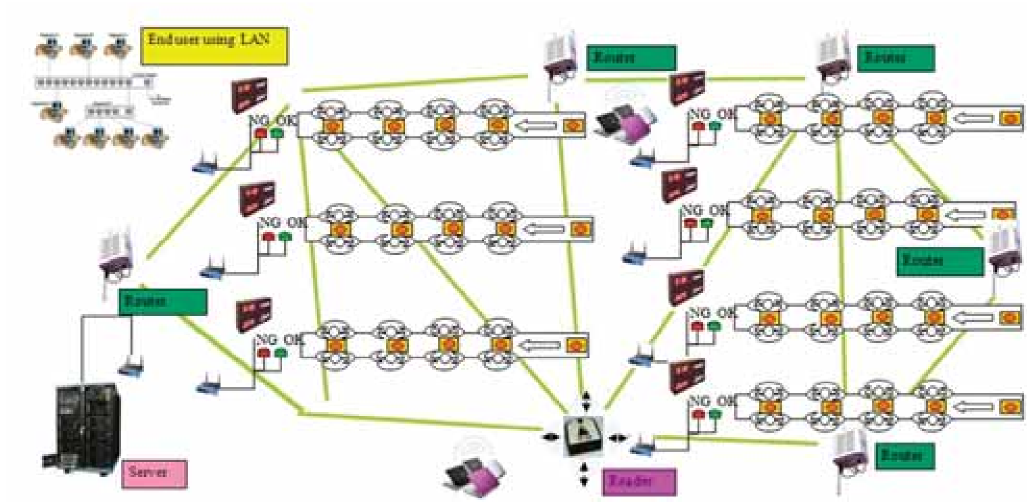


Figure 9: The embedded architecture of the proposed system

are more than 10 of them without an additional router, there is a delay for the reader to receive the data from remaining tags. For distances of 50m between tags and readers without any router, up to even tags' data was accepted by the reader in real time. If there are more than seven tags, a router should be added so that the reader receives the data from remaining tags in real time too.

Potential Impact

By implementing this proposed wireless mesh network and web-based monitoring system, manufacturers can increase their productivity as it is a powerful reporting and archiving tool. With the ability to connect to both MCDAS and emerging hardware technology, production reports can seamlessly integrate the data flow from plant floor to the management office systems.

Typical operations include logging of information from MCDAS to an SQL server; scheduling of pre-configured reports; displaying and filtering of line productions; down-time monitoring, retrieval of archived information; and report generation for preview, emailing and printing. Figure 9 shows the whole scenario of the embedded architecture for the proposed system.

A New Technique

A wireless network adopting a web-based monitoring system is still a new technique. Therefore, new research in this field is greatly welcome, especially on the side of wireless technology, to ensure excellent communication and monitoring capabilities. Hopefully, this development of a fully automated monitoring system using wireless technology can be adopted and used for improvement of systems used in different applications. More importantly, the findings of this research will be of benefit to other areas/disciplines that use time monitoring systems. Also, further research in the areas of the complexities of real industrial environments and applications, high-level programming languages, wireless mesh networks, ZigBee technology and active RFID can be conducted effectively using the findings of our research. ●

WHAT THE READERS SAY

MODES OF CONDUCT

In his letter in the September issue of EW, Ivor Catt flatly rejects the concept that current can flow in two directions along the same conductor. He writes "*I say that the idea that electrons can hop along down a conductor in both directions, waving to each other as they pass, is truly amazing.*" He appears to believe that electrons are the only entities capable of moving electric charge from one location to another.

As far as I am aware, Ivor has never mentioned the existence of photons in any of his articles. The Wikipedia definition of this entity is: "*In physics, a photon is an elementary particle, the quantum of electromagnetic interaction and the base unit of light and all other forms of electromagnetic radiation.*"

Since photons can travel through solid material (glass), I have no problem in accepting the fact that they can also travel along conducting material. Light can be reflected back towards its source. So can current. The relationship between photons and electrons in a conductor can be likened to that between the wind and waves on the sea.

It is also possible for one group of photons to propagate along the facing surfaces of a conductor pair carrying differential-mode current, whilst another group propagates along the outer surfaces carrying antenna-mode current. There is a clear correlation between these two modes and those dubbed "Odd" and "Even" by Ivor.

Conventional transmission line theory is an analysis of the behaviour of differential-mode currents and voltages. It is possible to visualise the propagation of energy either as a movement of charge along a conductor or as an electromagnetic wave in the immediate environment. Since this analysis assumes that the current in the "return" conductor is equal in magnitude but opposite in direction to that in the "send" conductor, it effectively ignores the existence of the antenna-mode current.

An experiment was carried out to investigate the behaviour of a conductor pair as a transmission line (see Circuit Modelling of Interference Coupling, pages 221-230 www.designemc.info), and to compare it with the behaviour of the cable as an "accidental antenna". The cable under test was a 15m length of two-core mains cable. A voltage transformer was used to inject a sinusoidal signal at the mid-point of one conductor. All cable terminations were open-circuit. A current transformer clamped round the other conductor was used to measure the differential-mode current. Figure 1 shows the frequency response of the setup.

The circles represent the measured values of the admittance; the ratio of the amplitude of differential-mode current to the source voltage (amps/volt). The frequency scale (Hz) is linear. The solid line is the response of a circuit model of the assembly-under-test; a model derived from the concepts of electromagnetic theory. The peak at 5.66MHz defines the frequency of quarter-wave resonance of a 7.5m line, corresponding to a propagation velocity of 170Mm/sec.

When the current transformer was removed, then clamped round both conductors, the measured current was that which propagated away from the cable into the environment; the antenna-mode current. Figure 2 shows the response of the transfer admittance (amps per volt) over the same frequency range as previously.

Again, the measured values are shown as circles whilst the solid line shows the response of the circuit model. This shows that the frequency of resonance of a 15m cable, acting as a half-wave dipole, is 7.55MHz. This corresponds to a propagation velocity of 227Mm/sec.

The fact that the propagation velocity for antenna-mode current is higher than that for differential-mode current provides evidence to support Ivor's conclusion that there are two modes of propagation, and that one mode is faster than the other.

The fact that the response of the circuit model matches that of the actual hardware demonstrates that existing electromagnetic theory is perfectly adequate to explain the phenomena. There is no need to bang the drum and insist that we need to devise a new theory of electromagnetics.

A more fruitful approach would be to review the way Circuit Theory is applied.

Ian Darney

DISCUSSING 'THE CATT QUESTION'

I was pleased to see EW looking at femtosecond technology in the October issue, and am looking forward to more in future issues with, hopefully, some reference to underlying physical mechanisms which Ivor Catt, Ian Darney, Stephen Crother, Barry McKeown and others are very interested in.

Recent reports are showing data – and videos – using zeptosecond pulses combined with stroboscopy to better understand QED, Quantum Chaos, String theory and other proposals which are a matter of considerable debate and disagreement at present; and there is the prospect of pushing 'down' to the yoctosecond region which we should be anticipating when we discuss 'The Catt Question'.

Tony Callegari

SUPERCAPACITORS REPLACE BATTERIES IN POWER RIDE-THROUGH APPLICATIONS WITH HELP OF 3MM × 3MM CHARGER

BY **JIM DREW**, SENIOR APPLICATIONS ENGINEER AT LINEAR TECHNOLOGY

Supercapacitors are finding their way into an increasing number of applications for short-term energy storage. One such application is a power ride-through circuit, in which a backup energy source cuts in and powers the load when main power supply fails for a short time. This type of application has been dominated by batteries in the past, but supercapacitors are fast making inroads as their price-per-farad, size and effective series resistance per capacitance (ESR/C) continue to fall.

In a power ride-through application, series-stacked capacitors must be charged and cell-voltage balanced. Supercapacitors are switched into the power path when needed and the power to the load is controlled by a DC/DC converter. Features that make a good choice for power ride-through applications include small package size, programmable charging current, automatic cell voltage balancing, low drain current on the supercapacitors and a, low noise, constant current charger.

Supercapacitor Characteristics

Supercapacitors come in a variety of sizes, for example a 10F/2.7V supercapacitor is available in a 10mm × 30mm 2-terminal radial can with an ESR of 25mΩ, while a 350F/2.5V supercapacitor with an ESR of 1.6mΩ is available in a D-cell battery form-factor.

One advantage supercapacitors offer over batteries is their long life.

> *Two parameters of the super-capacitor that are critical to an application are cell voltage and initial leakage current*

A capacitor's cycle life is quoted as greater than 500,000 cycles; batteries are specified for only a few hundred cycles. This makes the supercapacitor an ideal "set and forget" device, requiring little or no maintenance.

Two parameters of the supercapacitor that are critical to an application are cell voltage and initial leakage current. The manufacturers of supercapacitors rate their leakage current after 100 hours of applied voltage while the initial leakage current in those first 100 hours may be as much as 50 times the specified leakage current.

The voltage across the capacitor has a significant effect on its operating life. When used in series, the supercapacitors must have balanced cell voltages to prevent over-charging of one of the series capacitors. Passive cell balancing is a popular and simple technique. The disadvantage of this technique is that the capacitor discharges through the balancing resistor when the charging circuit is disabled. The rule of thumb for this scheme is to set the balancing resistor to 50 times the

Figure 1: A 5V power ride-through application

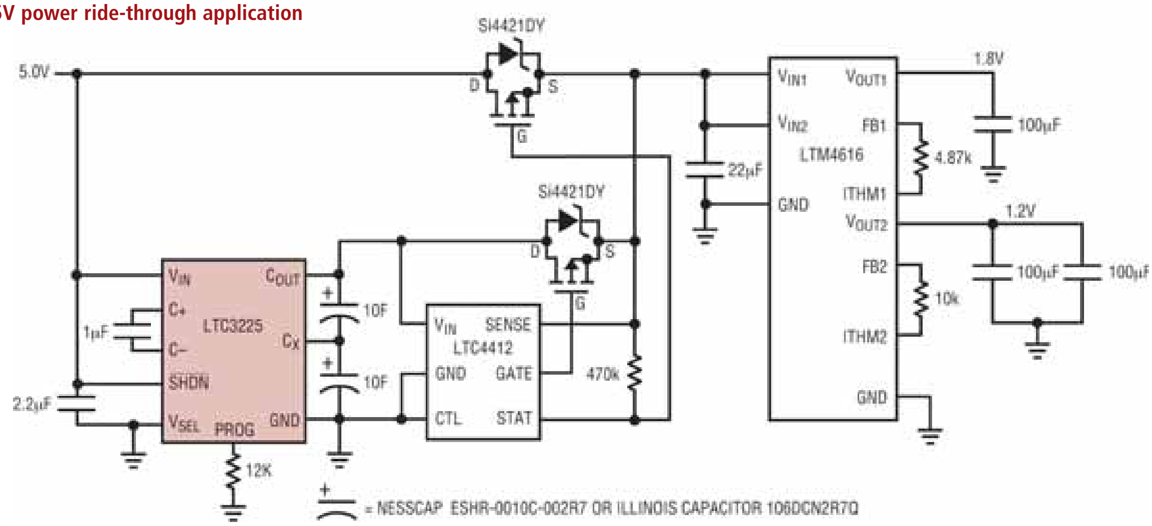
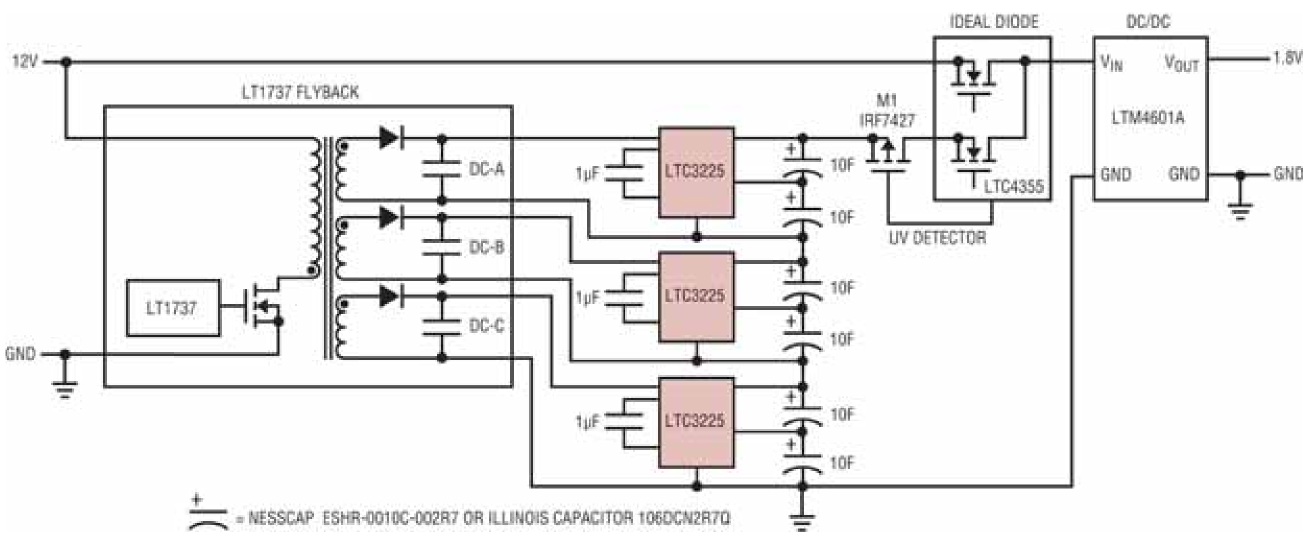


Figure 2: A 12V power ride-through application



worst case leakage current, estimated at 2µA/F.

An alternative is to use a non-dissipative active cell balancing circuit, such as the LTC3225, to maintain cell voltage. The LTC3225 presents less than 4µA of load to the supercapacitor when in shutdown mode and less than 1µA when input power is removed. The LTC3225 features a programmable charging current of up to 150mA, charging two series supercapacitors while balancing the voltage on the capacitors.

Power Ride-Through Applications

To provide a constant voltage to the load, a DC/DC converter is required between the load and the supercapacitor. As the voltage across the supercapacitor decreases, the current drawn by the DC/DC converter increases to maintain constant power to the load. The DC/DC converter drops out of regulation when its input voltage reaches the minimum operating voltage (VUV).

To estimate the requirements for the supercapacitor, the effective circuit resistance (RT) needs to be determined. RT is the sum of the capacitors' ESRs and the circuit distribution resistances:

$$R_T = ESR + R_{DIST}$$

Assuming 10% of the input power is lost in the effective circuit resistance when the DC/DC converter is at VUV, the worst case RT is:

$$R_{T(MAX)} = \frac{0.1 \bullet V_{UV}}{P_{LOAD}}$$

The voltage required across the supercapacitor at VUV threshold of the DC/DC converter is:

$$V_{C(UV)} = \frac{V_{UV}^2 + P_{IN} \bullet R_T}{V_{UV}}$$

The required effective capacitance can then be calculated based on the required ride-through time (TRT), and the initial voltage on the capacitor (VC(0)) and VC(UV):

$$C_{EFF} = \frac{2 \bullet P_{IN} \bullet T_{RT}}{V_{C(0)}^2 - V_{C(UV)}^2}$$

The ESR of a supercapacitor decreases with higher frequency. Manufacturers usually specify the ESR at 1kHz, while some manufactures publish both the value at DC and at 1kHz. The capacitance of supercapacitors also decreases as frequency increases and is usually specified at DC.

When using a supercapacitor in a ride-through application where the power is being sourced for seconds to minutes, use the effective capacitance and ESR measurements at a low frequency, such as 0.3Hz.

Applications

Figure 1 shows two series connected 10F, 2.7V supercapacitors charged to 4.8V that can hold up 20W. The LTC3225 is used to charge the supercapacitors at 150mA and maintain cell balancing, while the LTC4412 provides an automatic switchover function. The LTM4616 dual output switch mode µModule DC/DC converter generates the 1.8V and 1.2V outputs.

Figure 2 shows a 12V power system that uses six 10F, 2.7V supercapacitors in series charged by three LTC3225's set to 4.8V and a charging current of 150mA. The three LTC3225's are powered by three floating 5V outputs generated by the LT1737 flyback controller. The output of the stack of six supercapacitors is set up in a diode OR arrangement via the LTC4355 dual ideal diode controller. The LTM4601A µModule DC/DC regulator produces 1.8V at 11A from the OR'd outputs. The LTC4355's MON1 in this application is set for 10.8V.

Meeting the Needs

Supercapacitors are meeting the needs of power ride-through applications where the time requirements are in the seconds to minutes range. Supercapacitors offer long life, low maintenance, light weight and environmentally friendly solutions when compared to batteries. To this end, the LTC3225 provides a compact, low noise solution to charging and cell balancing series connected supercapacitors. ●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Choosing the Most Appropriate Tools and Techniques for NANO MEASUREMENTS

OVER THE NEXT SEVERAL ISSUES OF ELECTRONICS WORLD MAGAZINE, **JONATHAN TUCKER**, CHAIRMAN, IEEE NANOTECHNOLOGY COUNCIL STANDARDS COMMITTEE, WILL PRESENT THIS TUTORIAL ON THE TEST AND MEASUREMENT ASSOCIATED WITH NANOTECHNOLOGY

Electrical measurements on nanoscopic materials place stringent requirements on the instrumentation. In order to measure conductivity, impedance, or other electrical properties, and relate those measurements to the density of states, a galvanic connection must be made to the nanoscopic DUT. This represents one of the major hurdles to be overcome in the field of nanotechnology testing. There are only a few tools available and few device constructs that facilitate connections of this type.

Electrical measurements on passive devices (any device that is not a source of energy) are made by following a simple procedure: stimulate the sample in some way and measure its response to the stimulus. This method also works for devices that have both passive and active properties with linear or non-linear transfer functions. With appropriate techniques, a source-measure algorithm can be useful for characterizing sources of energy.

For nanoscopic particles, this general method takes the form of source-measure testing to quantify impedance, conductance and resistance, which reveal critical material properties. This test methodology is useful even if the end application is not an electronic circuit.

Several considerations are important in the characterization of nanoscopic particles:

Figure 1: DC SMUs are a good choice for a variety of nano material and device test applications because they can switch rapidly between sourcing voltage/measuring current and sourcing current/measuring voltage

- Nanoscopic particles will not support the magnitude of currents that macroscopic device can carry (unless they are superconducting). This means that when a device is interrogated, the magnitude of a current stimulus must be carefully controlled.
- Nanoscopic particles will not hold off as much voltage from adjacent devices as a conventional electronic component or material (such as a transistor). This is because smaller devices can be and are placed closer together. Smaller devices also have less mass and may be affected by the forces associated with large fields. In addition, internal electric fields associated with nanoscopic particles can be very high, requiring careful attention to applied voltages.
- Given that nanoscopic devices are so small, they typically have lower parasitic (stray) inductance and capacitance. This is especially useful when they are used in an electronic circuit, enabling faster switching speeds and lower power consumption than comparable macroscopic devices. However, this also means that instrumentation for characterizing their IV curves must measure low currents while tracking the short reaction time.

Because nanoscopic test applications often require low current sourcing and measurement, appropriate instrument selection and use is critical for accurate electrical characterization. In addition to being highly sensitive, the instrumentation must have a short response time (sometimes referred to as high bandwidth), which is related to a DUT's low capacitance and ability to change state rapidly at low currents.

The switching speed of a sourcemeasure test circuit may be limited by the instrumentation used to follow the state of the device. This is especially true if a nonoptimal measurement topology is used to observe the device. The two possible topologies are source current/measure voltage or source voltage/measure current.

When measuring high impedance (> 10,000 ohms) devices, the source voltage/measure current technique is best

FURTHER READING

TO LEARN MORE ABOUT SPECIFIC TECHNIQUES FOR IDENTIFYING AND ELIMINATING SOURCES OF ERROR IN NANO MEASUREMENTS, SEE "Techniques for Accurate Nanotech Electrical Measurements" online.

When considering the measurement of low impedance (< 1000 ohms) devices, the source current/measure voltage technique will generally yield the best results. Current sources are stable when applied to lower impedances, and a good signal-to-noise ratio can be achieved without great difficulty. This allows for accurate low voltage response measurements.

When measuring high impedance (> 10,000 ohms) devices, the source voltage/measure current technique is best. Stable voltage sources to drive high impedances are easily constructed. When a well-designed voltage source is placed across a high impedance, it will quickly charge the stray capacitance of the DUT and test cables and rapidly settle to its final output value. The small current response of the DUT can be accurately measured with an appropriate ammeter.

A commercial DC source-measure unit (SMU) is a convenient test tool for many nanoscopic material and device measurements (see Figure 1). SMUs change measurement topology automatically – that is, they can rapidly switch between sourcing voltage/measuring current and sourcing current/measuring voltage. This makes it easier to minimize measurement noise while maximizing measurement speed and accuracy.

Some nanoparticles can change state with the application of an external field. When investigating such materials, an SMU can be configured to source voltage and measure current for a nanoparticle in its high impedance state. When the material is in its low impedance state, more accurate results are achieved by sourcing current and measuring voltage. Furthermore, the SMU has a current compliance function that can automatically limit the DC current level to prevent damage to the material or device under test (DUT). Similarly, there is a voltage compliance function when voltage is being sourced.

When using the compliance function, an SMU will satisfy the source value unless the user's compliance value is exceeded. For example, when an SMU is configured to source voltage with a preset current compliance, if that compliance value is exceeded, the SMU automatically starts acting as a constant current source. Its output level then will be the compliance current value. Alternately, if the SMU is set to source current with a compliance voltage, it will automatically switch to sourcing voltage (the compliance voltage) if the DUT impedance and the current it draws begin to drive the voltage higher than the compliance value.

Although a nanoscopic device, such as a CNT switch, can change states rapidly, the change in instrument state is not instantaneous. Depending on the SMU model, the switching time can range from 100 nanoseconds to 100 microseconds. Although such switching speeds are not fast enough to track a nanoparticle as it changes state, the time is short enough to allow accurate measurements of both states while limiting DUT power dissipation to acceptable levels.

New Digital Differential Pressure Sensors with Low Power Consumption

Sensirion launched new differential pressure sensors in the SDP600 series. The new SDP6x6 sensor line features especially low energy consumption, making it suitable for long-term battery operation.

The SDP606 and SDP616 sensors are designed to enter sleep mode after performing each measurement. They wake up when a "measure" command is received and enter sleep mode again after completing the measurement. The operation currents of a standard SDP600 sensor can be high as 6mA, but the new SDP6x6 sensor is optimized for operating currents no greater than 400μA. There is virtually no current drain (< 1μA) in sleep mode.

This drastic reduction in power consumption allows the new sensors to be used in battery-powered applications. The new differential pressure sensors are excellent solutions for medical and HVAC applications, where high accuracy and reliability with very low energy consumption are required.

The new sensors extend the comprehensive product range of Sensirion's digital differential pressure sensors in the SDP600 series.

www.sensirion.com/sdp6x0

ONE-CHIP POWER SWITCH SERIES MEETS 2013 ERP LOT 6 STANDBY POWER REGULATIONS

The power saving requirements of the 2013 EU eco-design directive ErP (Energy-related Products) Lot 6 requires the maximum power consumption of electronic devices in standby mode to be less than 0.5W. This requirement remains a significant challenge for auxiliary power supply designs in applications such as PCs, game consoles and LED TVs.

Fairchild Semiconductor introduced the FSB series of AC regulators, the next-generation green-mode Fairchild Power Switch (FPS) to help designers meet the challenge of achieving less than 0.5W power consumption in standby mode. By incorporating Fairchild's mWSaver technology, devices in the FSB series dramatically reduce standby and no-load power consumption, enabling conformance to all worldwide standby mode guidelines.

The FSB series integrates advanced current-mode pulse width modulator (PWM) and an avalanche-rugged 700V SenseFET in a single package solution allowing auxiliary power designs with higher standby energy efficiency, reduced size, improved reliability and a lower system cost than previous solutions.

www.fairchildsemi.com

TI'S ENHANCED CODE COMPOSER STUDIO IDE SLASHES DEVELOPMENT TIME

Further simplifying embedded software development, Texas Instruments Incorporated (TI) introduced significant upgrades to its industry-leading Code Composer Studio integrated development environment (IDE) based on the Eclipse open source software framework.

Featuring major user interface improvements that ease development and a 5x smaller installation package that speeds setup, Code Composer Studio IDE v5 now runs on Windows and Linux operating environments and starts at the low cost of $79 – thousands of dollars less than competitive offerings.

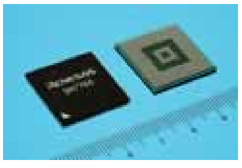
Code Composer Studio IDE provides a single user interface to take developers through each step of the application development flow. It includes a suite of tools that simplifies software design for embedded processing applications by accelerating software code development, analysis and debugging through a common development environment. Code Composer Studio IDE v5 is compatible across many devices in TI's broad embedded processing portfolio, including single and multicore digital signal processors (DSPs), microcontrollers, video processors and microprocessors.

www.ti.com

Single Chip Solution for Top View System with Image Recognition Capabilities

Renesas Electronics and Renesas Mobile Corporation announced the availability of their new image recognition system-on-chip (SoC), the SH7766. This solution integrates on a single chip all the functions required for the implementation of camera-based surround view systems together with the display of crucial information such as lanes, signs and markings, pedestrians, vehicles, etc.

The new SH7766 SoC retains compatibility with Renesas's existing SH77650 image recognition SoC while delivering improved performance. In particular, the display functions such as viewpoint conversion and dynamic range control (brightness compensation, etc.) have been enhanced. These new functions make it possible to develop applications with clear top-view virtual camera visualization. These can use different viewpoints to display the changing surroundings in real time and provide monitoring functionalities such as advanced driver assistance systems (ADAS).



Renesas's next-generation SH7766 image recognition SoC improves on the performance of its predecessor, the SH77650, and delivers enhanced view functions and higher image recognition engine performance.

www.renesas.eu

MSO-FUNCTIONALITY OSCILLOSCOPE ALLOWS QUICK TESTING OF COMPLEX EMBEDDED DESIGNS

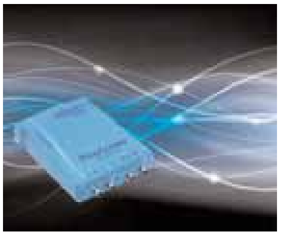
Rohde & Schwarz launched the R&S RTO high-performance oscilloscope, which makes it easy for users to obtain accurate results quickly. A new function has now been added to significantly broaden the application range: a hardware option turns the R&S RTO into a mixed signal oscilloscope (MSO). In addition to the usual two or four analog channels, the oscilloscope now features 16 digital logic channels with 400MHz input frequency. Equipped with the MSO option, the R&S RTO allows time correlation between the instrument's analog and digital sections.

The R&S RTO with MSO functionality offers a very high sampling rate (5 Gsample/s) over the entire 200 Msample memory depth. A maximum time resolution of 200ps makes it possible to accurately analyze signal content and quality. Critical events such as narrow, widely separated signal faults can be reliably detected using the digital channels. The option comes with hardware-based acquisition, trigger and processing units.

www.rohde-schwarz.com

PICOSCOPE OFFERS THE WORLD'S FIRST 1GS/S USB-POWERED OSCILLOSCOPE

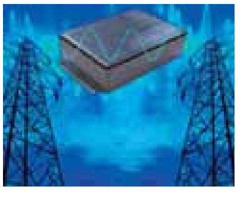
The three new oscilloscopes in the PicoScope 2000 Series are the first USB-powered oscilloscopes to offer a real-time sampling rate of 1GS/s. With two channels, bandwidths ranging from 50MHz to 200MHz, a built-in function generator, arbitrary waveform generator and external trigger input, these compact and economical scopes are perfect for engineers and technicians needing a complete test bench in a single unit.



The scopes are supplied with a full version of the PicoScope oscilloscope software. As well as standard oscilloscope and spectrum analyzer functions, PicoScope includes valuable additional features such as serial decoding, mask limit testing, segmented memory and advanced triggers. It provides a large, clear display that shows waveforms in great detail and allows easy zooming and panning. Other advanced features include intensity- and colour-coded persistence displays, math channels, automatic measurements with statistics, and decoding of I2C, UART/RS232, SPI and CAN bus data. Free updates to the software are released frequently.

www.picotech.com

New Avnet Abacus Aluminium Enclosures Withstand Full Immersion



Avnet Abacus has introduced the IP67 and IP68-rated Deltron 480 and 483 series of aluminium enclosures manufactured by DEM Manufacturing, a division of the UK-based Alpha 3 Manufacturing Limited.

Designed for the most demanding electrical and environmental conditions in marine, industrial, food preparation, transportation, leisure, military and aerospace, the enclosures can optionally feature EMI/RFI protection. All are certified to BS EN 60529: 1992.

The enclosures provide the highest standard of protection against dust and water and will withstand prolonged immersion in water, to depths of up to 1 metre for 30 minutes. The IP68 enclosures can handle depths of up to 5 metres for 1 hour.

Manufactured in aluminium 380 alloy, the Deltron 480 series offers 15 sizes of standard boxes, whilst the Deltron 483 series consists of 9 sizes of flanged boxes. Sizes range from 60mm x 55mm x 31mm to 275 x 175 x 66mm.

www.avnet-abacus.eu

HIGH-ACCURACY INSTRUMENTATION AMPLIFIER OFFERS ON-CHIP CALIBRATION

Microchip announces its first instrumentation amplifier, the MCP6N11. The new instrumentation amp features Microchip's unique mCal technology, which is an on-chip calibration circuit that enables low initial offset voltage and a means of controlling offset drift, resulting in higher accuracy across time and temperature.

The MCP6N11's low-power CMOS process technology enables low power, whilst providing a gain bandwidth product of 500kHz, and a hardware shutdown pin for even greater power savings. The device's low, 1.8V operation allows two 1.5V batteries to be drained beyond typical use, whilst its rail-to-rail input and output operation enables full-range use, even in low-supply conditions.

The device's mCal technology provides a highly accurate way to minimise drift over time and temperature, whilst the low-power operation/shutdown requires less current for the given speed and performance, extending battery life and leading to less self-heating. The MCP6N11's low-voltage operation, with rail-to-rail input and output, enables a greater dynamic range.

www.microchip.com/get/KQ76

NEW RANGE OF MULTIFUNCTIONAL HIGH VOLTAGE DC ELECTRONIC LOADS

Telonic Instruments has introduced a new range of high quality multifunctional electronic and evaluation equipment manufactured by Japan based Kikusui. The PLZ-4WH series is designed primarily for use in the automotive industry, and specifically electric vehicles (EV) and hybrid electric vehicles (HEV).

The range supports input voltages up to 650V and is used to evaluate EV and HEV in vehicle chargers, DC/DC converters, battery cells and power supplies for high voltage DC electric supply systems. It is able to operate PFC tests on European and other three-phase 400V system input power supplies, as well as evaluating and testing high voltage parts relating to such equipment.

This innovative range has six operation modes, constant current, resistance, voltage, power, constant current + constant voltage and constant resistance + constant voltage modes.

The range comprises of four models with an operating voltage of 650V and current of 100A with power of 165/1000W.

www.telonic.co.uk

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AVX'S AEC-Q200 QUALIFIED 0402 CAN BUS VARISTOR DELIVERS LOWEST SPECIFIED LEAKAGE CURRENT

AVX Corporation has expanded its automotive CAN BUS varistor product offering to include a miniature 0402 device that provides sub-1ns response to ESD strikes. The AEC-Q200 qualified CAN0005 varistor delivers the lowest specified leakage current available on the market. The bi-directional CAN0005 also provides excellent current and energy handling capabilities as well as EMI/RFI attenuation.

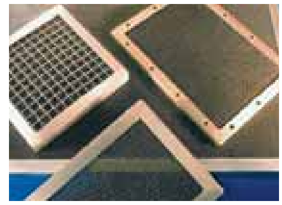
"AVX offers one of the broadest AEC Q200-qualified product offerings of any automotive supplier. The introduction of the CAN0005 varistor provides our customers excellent ESD protection and the lowest specified leakage current in an AEC-Q200 Qualified 0402 varistor on the market today," said Jeremiah Woods, global marketing manager for circuit protection.

The CAN0005 provides an ESD rating of 25kV. The low profile 0402 varistor features a fast response time to ESD and can withstand successive 1k strikes at 8kV (IEC 61000–4-2).

Typical pricing ranges from $0.03 - $0.09 depending on volume and package.

www.avx.com

RoHS-Compliant EMC Ventilation Panels



Kemtron has introduced a RoHS-compliant aluminium passivation process for its aluminium honeycomb EMC ventilation panels. The process has eliminated the hexavalent chromium which is present in some aluminium passivation processes; the new conversion coating meets the requirements of Mil-C-5541E for corrosion and electrical conductivity.

The standard honeycomb vent panel is constructed from two layers of aluminium honeycomb set at 90° to each other and set in an extruded aluminium frame. To achieve optimum RF attenuation the overall cell thickness to cell diameter ratio needs to be 4:1. Each vent is supplied with an EMC gasket to ensure effective EMI shielding and grounding. Fixing points can either be plain thru-holes or inserts.

For harsh environments it is possible to include various styles of kick plate to one face of the honeycomb. In addition 30° and 45° honeycomb is available to provide either directional air flow or prevent ingress of dripping water.

www.kemtron.co.uk

LECROY ANNOUNCES USB 2.0 HSIC DECODE TEST SOLUTIONS FOR OSCILLOSCOPES

LeCroy Corporation announced the availability of USB 2.0 High Speed Inter-chip (HSIC) protocol decode annotation for its WaveSurfer, WaveRunner, WavePro, WaveMaster and LabMaster oscilloscopes.

The HSIC technology communicates between microchips in embedded sub-systems, leveraging the traditional host-device topology of USB and, hence, the large amount of code that already exists. This makes HSIC extremely lucrative in areas demanding fast time-to-market, such as in the mobile industry for example which includes smart phones and tablets.

LeCroy HSIC USB solutions consist of an intuitive HSIC decode annotation overlaid on the physical layer (analog) waveform signal on the oscilloscope display with corresponding tabular display of data and a quick zoom to a specific packet. In addition, WaveRunner, WavePro, WaveMaster and LabMaster support LeCroy's ProtoSync option, which takes the testing to an even higher level by providing a transaction and application level view of the HSIC traffic in the familiar CATC protocol analyzer view.

www.lecroy.com

AVNET EMBEDDED RELEASES UNIQUE PACKAGE SOLUTIONS

Avnet Embedded introduced a unique Advantage Pack solution, complete with a ready-to-use Windows Embedded OS image script and Panel PC hardware.

An Advantage Pack will help engineers save precious time in producing an image. The Advantage Pack is a complete kit, ready to go with all start-up and driver files, example OS image scripts and a deployment 'how-to' guide. Advantage Packs are produced to support Windows Embedded Standard 2009 and Windows Embedded Standard 7 on selected hardware available from Avnet Embedded EMEA.

A Windows Embedded Standard 2009 Advantage Pack is available now for the Flytech K750 Series of Panel PCs and a Windows Embedded Standard 7 Advantage Pack is scheduled for release within the next two weeks. This unique service is offered free of charge when purchasing a Flytech Panel PC from the K750 series Panel PC via Avnet Embedded EMEA.

www.avnet-embedded.eu

KONTRON'S AM4140 ADVANCEDMC MODULE WITH 4/8-CORE FREESCALE QORIQ PROCESSOR

Kontron announced its powerful AdvancedMC processor module AM4140. Equipped with a Freescale QorIQ P4040/80 CPU with up to 8 cores at 1.5GHz and high-speed fabrics, the new Kontron AM4140 offers outstanding performance for parallel, multi-threaded applications on MicroTCA integrated platforms.

The module incorporates the high-performance Freescale QorIQ P4040/80 4/8-core processor with cores based on the e500 power architecture. With high-speed frame handlers and multiple high-speed connections like Serial Rapid IO, 10 Gigabit Ethernet and PCI Express, the Kontron AM4140 meets highest demands in multi-threaded processing. In order to match demands on high throughput and low latency, the Kontron AM4140 provides a fast dual-channel memory of up to 8GB ECC-RAM.

The Kontron AM4140 provides flexible configuration of high-speed fabrics. On AMC ports 4-7, 4x SERDES lines can be configured either as PCI Express (root complex or end point) or Serial Rapid IO ports (host or agent).

www.kontron.com

KEITHLEY PUBLISHES CD ON HIGH PERFORMANCE SOURCE MEASUREMENT SOLUTIONS

Keithley Instruments has published an informative CD entitled "*Configuring Cost-Effective, High Performance Sourcing and Measurement Solutions*". A free copy is available upon request from Keithley at http://www.keithley.com/promo/pr/092.

The CD offers a wide variety of application notes and tutorial information on using Source-Measurement Units (SMUs) in applications such as high power, high brightness LED test, solar cell characterization and high-resistance measurements.

SMUs combine the capabilities of a number of instruments, including DC voltage and current sources and a digital multimeter (DMM). These instruments are equally suitable for standalone benchtop use and as building blocks in highly scalable system solutions, combining wide I-V dynamic range with tightly synchronized operation. A convenient selector guide simplifies identifying the most appropriate SMUs for a particular application. The CD provides detailed overview of the features and advantages of each of Keithley's SMU families, including links to data sheets, application notes, application briefs and online demos.

www.keithley.com

Automotive Low-Side MOSFET Pre-Driver IC

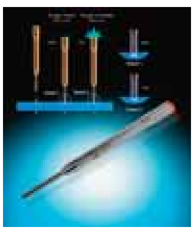
The new A3944 from Allegro MicroSystems Europe is a low-side MOSFET pre-driver IC targeted at the automotive market.

The new device, which complements Allegro's existing automotive pre-driver family, is a programmable 6-channel low-side MOSFET control IC, with a 50V rating on drain feedback inputs which makes it suitable for use in automotive diesel applications.

While its extensive diagnostics and wide operating voltage range make the A3944 ideally suited for the automotive market, it may also be used in consumer and industrial applications.

Each channel of the A3944 is controllable by a combination of parallel and serial inputs and provides sufficient gate drive-current to allow PWM control up to 10kHz, depending on the MOSFET gate charge. Each channel also provides independent fault diagnostics for short-to-ground and open-load conditions when in the "off" state, and short-to-battery when in the "on" state. A short-to-battery condition can disable the output until reset or for a programmable retry time.

www.allegromicro.com



New Tool Detects Blocking in Test Probes

A new tool for the detection of blocked or tight plungers in the test probes used in automatic test systems has been introduced by Peak Test Services.

With the new Peak blocking tester, the correct functioning of the contact probes built into ATE test modules or fixtures can be tested very quickly and simply using minimal spring force.

The tester incorporates a Peak P201/G switch probe integrated with an LED display which illuminates if the plunger is stuck. The test height is adjustable by a threaded sleeve, and the spring force can be adjusted by changing the integrated probe. The maximum spring force is restricted to 6.0N: a value which eliminates any potential damage to the connector elements.

www.thepeakgroup.com

Compact MIL-Spec DC-DC Converter Delivers 20A Output Current

Roband Electronics has added yet another innovative product to its compact military specification DC-DC converter range. The new RO-MIL-2213, which is supplied in 3.3V and 5V output versions, is capable of delivering a 20A output current from a package size measuring just 76.3 x 38.2 x 10.2mm.

The RO-MIL-2213 is a high-efficiency, high power-density, single-rail unit comprising an isolated, high-frequency, pulse width modulated push-pull converter. While it is specified to operate from a nominal 28V supply, this versatile power supply will accept a wide input voltage range from 12-40V (5V output version) and 14.5-40V (3.3Voutput version). Options include an 80V input surge capability and a variant that will operate from an input as low as 9V. External synchronisation is also available as an option.

The RO-MIL-2213 operates over the military temperature range without de-rating. It is unconditionally stable and does not require additional external components for correct operation.

www.roband.co.uk

Livingston Publishes New Catalogue

Test equipment sourcing specialist Livingston has released the latest edition of its Used Equipment Catalogue. Available in English, German, French, Spanish, Italian, Polish and Dutch, the catalogue is divided into six core categories: General Purpose, Electrical & Industrial, Fibre Optics, RF & Microwave, Communications and Broadcast. It includes a broad variety of test hardware, such as power supplies, logic analysers, frequency counters, oscilloscopes, function generators, multimeters, power quality analysers, fibre optic splicing equipment, optical sources, signal analysers, network analysers, signal generators, cable/antenna testers, protocol testers, access testers, radio test sets, video test systems and thermal imaging cameras.

Among the leading equipment manufacturers to find in this publication are Aefos, Aeroflex, Agilent Technologies, Anritsu, Chauvin Arnoux, EXFO, FLIR Systems, Fluke, JDSU, Lecroy, Rohde & Schwarz, Sumitomo, Sunrise Telecom, Tektronix, Trend Communication and XL Wireless. All items are immediately available from stock and come with a seven day money back guarantee.

http://www.livingston.co.uk/n_81/2011-used-equipment-sales-catalogue

MANA SCIENTISTS DISCOVER THAT INORGANIC SYNAPSES MIMIC THE HUMAN BRAIN

Researchers at the International Center for Materials Nanoarchitectonics (MANA) at NIMS, Tsukuba, Japan, have demonstrated for the first time the key features in the neuroscience and psychology of memory by an AgS_2 synapse.

Artificial neural networks have attracted attention as a means to a better understanding of biological neural networks, as well as aiding developments in artificial intelligence. The complex and interconnected nature of thought processes make neural behaviour difficult to reproduce in artificial structures without software programming.

The researchers at MANA have mimicked synaptic activity with the electronic behaviour of a nanoscale AgS_2 electrode. They observed a temporary higher-conductance state in the AgS_2 system following an incident electric pulse. Repetition of the input pulse over 2s intervals led to permanently higher conductance. These two responses mimic the short-term plasticity and long-term potentiation in biological synapses. In neuroscience, long-term potentiation (LTP) is a long-lasting enhancement in signal transmission between two neurons that results from stimulating them synchronously.

In the most widely accepted 'multistore' model of memory in human psychology, new information is stored briefly as a sensory memory. Rehearsal converts short-term memory to long-term. When demonstrating memorization of the numerals '1' and '2' in a 7 × 7 inorganic synapse array, the behaviour of the artificial synapse indicated 'multistore' memory rather than a conventional switch.

BURKHARD VOGEL, Managing Director, Germany: This research result is a major step towards future computing and it's worth diving deeper into the stuff on the MANA website.

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, INFN – Laboratori Nazionali del Gran Sasso, Italy: The human brain is a vast and complicated communications network where more than one hundred billion neurons process information essential for our survival.

Neural networks have seen an explosion of interest over the last few years and are being successfully applied across an extraordinary range of problem domains, in areas as diverse as medicine, engineering, biology and physics.

Neural networks are very sophisticated modeling techniques capable of modeling extremely complex functions. They are also intuitively appealing, even though at present they are only based on a crude low-level model of biological neural systems. In the future, the development of this neurobiological modeling may lead to genuinely intelligent computers.

The focal point for the biological basis of learning is the contact point between nerve cells or 'neurons' i.e. the 'synapse'. New synapses grow and develop to create neural networks with experiences of learning. Creation of neural networks is a function of 'synapse modification' or 'neuroplasticity'.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: The scientists took as a starting point the operation of the human brain to develop tools based on training, called networks of neurons. Thus the research, carried out by the NIMS, Tsukula, group in Japan, is miraculous and interesting because it is based on artificial intelligence. Indeed, this science becomes an important means of recognition to approach the human thought but let us not forget that it is the computer which operates to recognize and adapt to situations as a human would do.

The exploit of NIMS, Tsukuba, is formidable especially that the synapses are crucial to biological computations. They allow the nervous system to connect and to control other systems in the body.

Science advances, and one can only encourage any research which allows facilitating the life of the human being. But I think that one should not confuse the knowledge to advance science and the human intelligence which remains beyond any artificial intelligence.

> In the future, the development of this neurobiological modeling may lead to genuinely intelligent computers

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: The concept of an electrode and its name are due to Faraday. It appears that this inorganic electrode model of the human organic synapse is actually two breakthroughs. The first being related to short-term plasticity (STP) and secondly long-term potentiation (LTP) of human memory processes. This new insight should permit significant advancement in neuromorphic engineering, a concept developed by Carver Mead, which has come along way since the 1980s although technically it is just at the stage investigated by Faraday. But at its heart is, once again, a material science question in the type of material used to mimic nature.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: Emulation of the neural behaviour of brain cells has been a difficult task because of the complex nature of the thought processes. It is interesting that the nanoscale AgS_2 inorganic synapse has analogy to an individual biological synapse and can memorize without the need of programming. This new breakthrough will in no doubt help to improve our understanding of artificial neural systems and help us to create such complex systems that emulate the human memory processes closely.

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector please register your interest with the editor by writing to Svetlana.josifovska@stjohnpatrick.com