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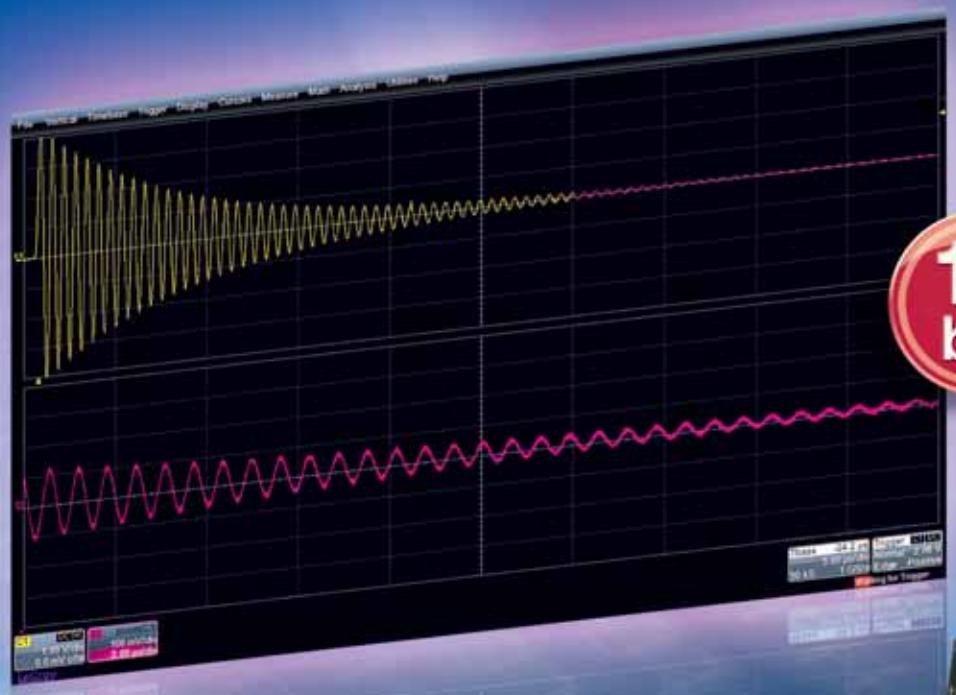

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DISTRIBUTION TRADE BODY AFDEC RELEASES FORECAST FOR 2012

The Manufacturers' Authorised Distributor (afdec) group within the Electronic Components Supply Network (ecsn) late last year released its 2012 forecast for the UK/Eire electronic components market served by distributors.

Following a declining second half of 2011 afdec members predict that the overall UK/Eire Distributor Total Available Market (DTAM) in 2011 will be £1.18bn, a growth of a little over 4% compared to the previous year. At £3.14bn the Total Available Market (TAM) will show just 2% growth compared to the previous year.

"The recovery in the UK/Eire electronic components markets continued slightly beyond our expectations in the first half of 2011 but then faltered into the second half, ending the year much in line with our original forecast," said Aubrey Dunford, ecsn Market Analyst. "However, in 2012 afdec members forecast that both DTAM and TAM will decline back to 2010 levels."

The association forecasts that the UK/Eire electronic components markets will decline further in the first half of 2012. Q1 is likely to be the low point, with a gradual recovery commencing in Q2 and Q3, and positive growth returning in Q4.

The consensus of ecsn's afdec members is that in 2012 the UK/Eire DTAM will decline by 5% to £1.12bn, with the TAM declining by 6%. The book-to-bill ratio, an important industry indicator, started trending down in 2010 and only went below unity in May '11, but has remained negative, confirming that overall demand has been weakening. According to Dunford there are early signs of an improvement in the electromechanical product area but semiconductors and passive components will probably not pick up until the end of Q1 2012.

"We have been witnessing an inventory correction right across all global markets," said Dunford. "The extended lead times for many components in 2010 resulted in customers increasing their inventory and component manufactures scrambling to meet demand and add capacity in an attempt to gain market share, this was exacerbated in 2011 by concerns over supply network disruption following the earthquake and tsunami in Japan."

> *Macro-economic events may yet again have derailed longer term capital investment in the manufacturing capacity for electronic components*

The ongoing problems in the Eurozone and beyond have prompted a marked deterioration in both consumer and business confidence and as a result the global sales of electronic components are likely to decline in 2012, but afdec and ecsn members are confident that the current situation is significantly different to the last recession experienced in November 2009. Today customers are able to provide better visibility and in some markets demand remains strong, particularly in automotive.

Component product groups (and manufacturers) are also seeing their markets react differently, with semiconductors currently having a tougher time than passive or electromechanical components. That said, all parties in the supply network will be adjusting their order backlogs, inventory and production capacity.

According to ecsn/afdec chairman Adam Fletcher, the pendulum of inventory correction is in danger of swinging too far, with the supply network potentially having another problem in keeping up with a small future increase in global demand.

"Unfortunately macro-economic events may yet again have derailed longer term capital investment in the manufacturing capacity for electronic components, particularly semiconductors. Smart organisations will continue to make a sensible investment in inventory to mitigate future supply network problems," he said.

afdec is the Association of Franchised Distributors of Electronic Components, a UK trade association.

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BIOINSPIRED MATERIALS LIGHT UP MODERN TECHNOLOGY

The physical mechanisms and role of refractive index can be considered by looking at some tropical fish, including the South American fish called 'Neon Tetra' which is capable of changing colour from green in the daytime to violet-blue at night

Scientists at the National Institute for Materials Science (NIMS) in Japan are focusing on the challenges of creating photonic crystals inspired by 'structural colour' found in nature. Structural colour refers to the bright colours found on insects, birds, fish and other animals.

Nature's ability to actively control colour has led scientists to integrate structural colour into the design of modern technologies such as low power displays and optical filters.

Hiroshi Fudouzi at NIMS has described the challenges facing materials scientists for the realization of photonic crystals based on the designs of bioinspired structural colour in a review paper, published in Science and Technology of Advanced Materials (STAM).

He includes mathematical models that describe the reflection of light from 1D multilayers and 3D colloidal crystals. Specific examples include layer-by-layer synthesis of polymer-based Bragg reflectors; electrochemical tunable colour of block copolymers between red and green; and stress/strain induced changes in the colour hydrogel membrane from red to blue.

Opal is an example of a 3D photonic crystal with well understood diffraction properties. Synthetic opal structures can be synthesized using 3D nanostructures of monodispersed polystyrene particles on silicon substrates, a highly stable new soft material consisting of a colloidal crystal embedded in a poly (N-isopropylacrylamide) hydrogel whose diffracted wavelength is thermally tunable across the entire visible spectrum.

In a 3D opal photonic crystal-humidity sensor, the colour changes from blue to red at high humidity, based on the nanoporous structure of a Hercules beetle. A high-performance optical gas sensor can be created with a highly selective response based on Morpho butterfly wings and new, more complex materials designs such as gyroid and related phases.

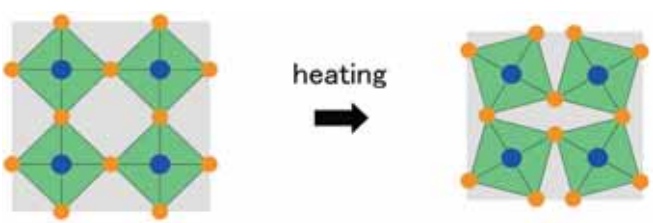
Materials that shrink when heated

New research holds promise for applications ranging from high-precision optical components to tooth fillings.

One common reason that people with fillings experience toothache is that their fillings expand at a different rate to the original tooth when, for example, drinking a hot drink. Contrary to intuition, however, not all materials expand when heated – some actually contract.

Recent research on these so-called negative thermal expansion (NTE) materials has led to the discovery of alloys exhibiting unexpectedly large thermal contraction.

Controlling the thermal expansion of composites is important for producing nanometer-scale electronic circuits, as well as the next-generation fuel cells and thermoelectric devices. An ability to combine NTE materials with 'normal' materials which expand upon heating ensures a reduction in thermal expansion in a composite material – something that people with tooth fillings would appreciate. An example of such a composite is Invar, an iron-nickel alloy with a uniquely low coefficient of thermal expansion. As a result it is used where high dimensional stability is required, such as precision instruments, clocks or seismic creep gauges.



Schematic of negative thermal expansion in a flexible network
[By Dr. K. Takenaka, published in Science and Technology of Advanced Materials Vol. 13 (2012) 013001]

Koshi Takenaka at the Department of Crystalline Materials Science, Nagoya University in Japan works on NTE materials for practical applications. In the latest issue of Science and Technology of Advanced Materials (**http://iopscience.iop.org/1468-6996/13/1/013001**) he summarizes the physical mechanisms governing NTE with emphasis on recent developments.

Takenaka notes that, "NTE materials will expand our capability of thermal-expansion control, opening a new paradigm of materials science and technology thermal-expansion-adjustable composites". One challenge facing the scientist is that the addition of NTE materials to composites leads to undesirable instabilities at interfaces. New methods for producing stable interfaces between the host composite and NTE compensators are of critical importance. Nevertheless, the so-called 'one-component' materials – such as manganese antiperovskites, zirconium vanadates, and hafnium tungstates – exhibiting negligible thermal expansion offer a promising route towards achieving this goal.

European Research Project Aims to Deliver "Energy for a Green Society"

The partners in a publicly-funded European research project announced details of the multinational/multidisciplinary program called 'Energy for a Green Society' (ERG). This three-year ENIAC JU project aims to achieve substantial advances in the solar-energy supply chain, from sustainable harvesting to smart distribution. These advances include pushing solar-cell efficiency towards 25% and reducing power conversion losses by 20%.

The need for exponential growth in solar-energy production, as required by Europe's 2020 climate targets and general energy policies, creates formidable technological challenges. The ERG program aims to address these requirements by improving the efficiency of solar cells, devising innovative harvesting techniques, reducing power-conversion losses and enhancing energy-management strategies.

In the first stage, European researchers will focus on the design and development of innovative solar cells, exploring novel architectures, approaches and materials. One of the program's objectives is to demonstrate commercially viable applications of printable dye-sensitized solar cells that represent a promising low-cost alternative to silicon solutions.

"The ERG initiative will contribute to the establishment of a solid electronics design base for Europe and create a set of technology standards for the solar energy sector," said ERG project coordinator Dr Francesco Gennaro, who is also Staff Engineer for STMicroelectronics. "ERG's goal is to achieve significant efficiency improvements along the whole supply chain from PV panels to grid connection and make them available to all partners."

The 'Energy for a Green Society' project will span 36 months. The total cost of the project is €25.7m, partially funded through a combination of European and national grants, under the rule of ENIAC JU 2010. The participating countries are Italy, Belgium, Germany, Spain, Ireland, The Netherlands, the Slovak Republic and the UK.

ENIAC JU

The ENIAC Joint Undertaking (JU) is a public-private partnership on nanoelectronics, bringing together the ENIAC member States, the European Union and AENEAS (an association representing European R&D participants in this field).

It coordinates research activities through competitive calls for proposals to enhance the further integration and miniaturization of devices, and increase their functionalities. It aims to deliver new materials, equipment and processes, new architectures, innovative manufacturing processes, disruptive design methodologies, new packaging and 'systemising' methods. It will drive and be driven by innovative high-tech applications in communication and computing, transport, health care, energy and environmental management, security and safety, and entertainment.

The ENIAC JU was set up in February 2008 and will allocate grants throughout 2013. The projects selected for funding will run until 31 December 2017. The total value of the R&D activities generated through ENIAC JU is estimated at €3bn.

BATTERY CHARGING IN PORTABLE PRODUCTS – THE WAY FORWARD

By Trevor Barcelo
Product Line Manager – Battery Management Products, Linear Technology Corporation

BACKGROUND

Applications in portable power are extensive and diverse. Products range from wireless sensor nodes that consume average power measured in microwatts to cart-based medical or data acquisition systems with multi-hundred watt-hour battery packs. However, despite this variety, a few trends emerge – designers continue to demand more power in their products to support increased functionality and look to charge the battery from any available power source. The first trend requires increased battery capacities. Unfortunately, users are often impatient and these increased capacities must be charged in a reasonable time, which leads to increased charge currents. The second trend requires tremendous flexibility from the battery charging solution. Each of these issues will be examined in greater detail.

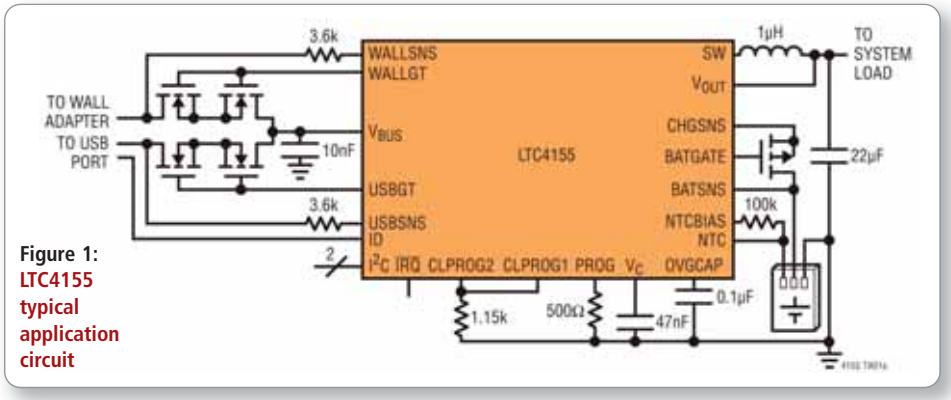


Figure 1: LTC4155 typical application circuit

WANTING MORE POWER

Consider modern handheld devices – both consumer-oriented devices and industrial devices may include a cellular phone modem, a WiFi module, a Bluetooth module, a large, back-lit display … the list continues. The power architecture of many handheld devices mirrors that of a cell phone. Typically, a 3.7V Li-ion battery is used as the primary power source due to its high gravimetric (Wh/kg) and volumetric (Wh/m3) energy density. In the past, many high powered devices used a 7.4V Li-ion battery to reduce current requirements, but the availability of inexpensive 5V power management ICs has pushed more and more handhelds to the lower voltage architecture. The tablet computer illustrates this point well – a typical tablet computer incorporates significant functionality along with a very large (for a portable device) screen. When powered from a 3.7V battery, the capacity must be measured in thousands of milliamp-hours. In order to charge such a battery in hours, thousands of milliamps of charge current are required.

However, this high charge current does not prevent consumers from also wanting to charge their high powered devices from a USB port if a high current wall adapter is not available. To satisfy these requirements, a battery charger must be able to charge at a high current (>2A) when a wall adapter is available, but still efficiently make use of the 2.5W to 4.5W available from USB. Furthermore, the product needs to protect sensitive downstream low voltage components from potentially damage-causing overvoltage events and seamlessly direct high currents to the load from a USB input, a wall adapter or the battery while minimising power loss. At the same time, the IC must safely manage the battery-charging algorithm and monitor critical system parameters.

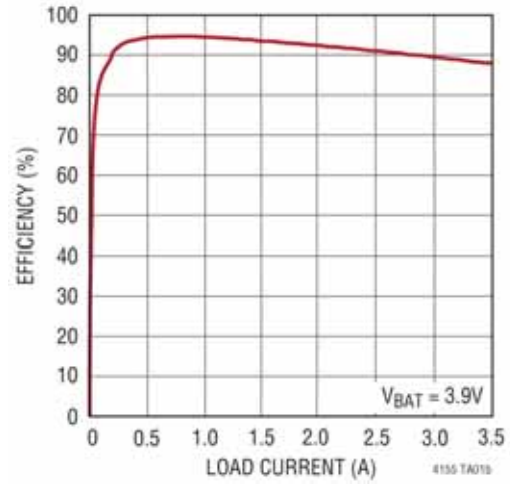


Figure 2: LTC4155 typical efficiency

CHARGING SINGLE-CELL PORTABLES

While the above requirements might seem impossible to find in a single IC, consider the LTC4155, a high power, I²C controlled high efficiency PowerPath manager, ideal diode controller and lithium-ion battery charger. It is designed to efficiently transfer up to 3A from a variety of 5V sources, resulting in over 3.5A available for battery charging and system use (see Figure 1). Even at these high current levels, the LTC4155's 88 – 94% efficiency eases thermal budgeting constraints (see Figure 2). The LTC4155's switching PowerPath topology seamlessly manages power distribution from two input sources such as a wall adapter and USB port to the device's rechargeable lithium-ion battery while preferentially providing power to the system load when input power is limited.

The LTC4155's switching regulator acts like a transformer, allowing the load current on V_{OUT} to exceed the current drawn by the input supply and making greatly improved use of the available power for battery charging, compared to typical linear-mode chargers. The previous example illustrated how the LTC4155 can efficiently charge at up to 3.5A, resulting in faster charge times. Unlike ordinary switching battery chargers, the LTC4155 features instant-on operation to ensure system power is available at plug-in even with a dead or deeply discharged battery.

While charging a battery at a high rate, it is important to monitor battery safety. The LTC4155 will automatically stop charging when the

battery temperature falls below 0°C or rises above 40°C (as measured by an external negative temperature coefficient [NTC] thermistor). In addition to this autonomous feature, the LTC4155 provides a 7-bit expanded scale analogue-to-digital converter (ADC) to monitor the battery temperature with approximately 1°C resolution. Combined with the four available float voltage settings and fifteen battery charge current settings, this ADC can be used to create custom charge algorithms based on battery temperature.

A simple 2-wire I^2C port provides access to the NTC ADC results, enabling adjustment of the charge current and voltage settings. The I^2C port also provides USB compliance by controlling 16 input current limit settings (including USB 2.0 and 3.0 compatible settings). The communication bus allows the LTC4155 to indicate additional status information such as input supply status, charger status and fault status. USB On-The-Go support provides a 5V supply back to the USB port without any additional components.

The LTC4155's dual input, priority multiplexer autonomously selects the most appropriate input, wall adapter or USB, based on a user-defined priority (default priority goes to the adapter input). An overvoltage protection (OVP) circuit simultaneously protects both inputs from damage caused by accidental application of high voltage or reverse voltage. The LTC4155's ideal diode controller guarantees that ample power is always available to V_{OUT} even if input power is insufficient or absent.

Managing two inputs (e.g., USB and wall adapter) is sufficient for many portable applications such as tablet computers or industrial bar code scanners. However, designers of portable devices continue to seek ways to charge the battery from any available power source.

MULTIPLE INPUT SOURCES

There are several reasons for users to charge batteries from multiple input sources. Some applications may need to be untethered from the grid and look to solar panels to provide power. Other applications demand the convenience of being able to charge from a wall adapter or an automotive battery or a high voltage industrial or telecom supply. Whatever the reason, the requirement places a significant burden on the battery charging system. Most battery chargers make use of a step-down (either switching or linear) architecture to charge a battery from a voltage supply higher than the maximum battery voltage. Prior charger products have typically been limited to input voltages of about 30V. These limitations prevent a designer from considering a telecom supply as a viable input supply or a solar panel with a 42V open-circuit voltage. In some cases the voltage range of the desired input supplies varies both above and below the battery voltage. Designing a solution for these challenges typically involves a compilation of high precision current sense amplifiers, ADCs, a microprocessor to control charging, a high performance DC/DC converter and ideal diode or multiplexing circuitry. Linear Technology proposes an alternative and improved solution.

POWERFUL CHARGING SOLUTION

The LTC4000 converts any externally compensated DC/DC power supply into a full-featured battery charger with PowerPath control. Typical DC/DC converter topologies that can be driven by the LTC4000 include, but are not limited to, buck, boost, buck-boost, Sepic and flyback. The device offers precision input and charge current regulation and operates across a wide input and output voltage range of 3V to 60V, allowing compatibility with a variety of different input voltage sources, battery stack sizes and chemistries. Typical applications are widespread due to the device's general purpose configuration and include high power battery charger systems, high performance portable instruments, battery backup systems, industrial battery equipped devices and notebook/subnotebook computers.

The high voltage capability of the LTC4000, in addition to the fact that it can be combined with many different DC/DC topologies, allows it to create a powerful battery charging solution with virtually any input supply (see Figure 3). To ensure that power from these inputs flows to the appropriate load, the LTC4000 features an intelligent PowerPath topology that preferentially provides power to the system load when input power is limited. The LTC4000 controls external PFETs to provide low loss reverse current protection, low loss charging and discharging of the battery and instant-on operation to ensure system power is available at plug-in even with a dead or deeply discharged battery. External sense resistors provide input current and battery charge current information, allowing the LTC4000 to work with converters that span the power range from milliwatts to kilowatts.

The LTC4000's full-featured battery charge controller charges a variety of battery chemistries including lithium-ion/polymer/phosphate, sealed lead acid (SLA), and nickel. The battery charger also includes precision current sensing that allows lower sense voltages for high current applications.

CONCLUSION

The modern portable product designer has an extremely challenging job – particularly when it comes to power. Customers continue to demand features that require more power and consequently, larger batteries. Meanwhile, customers want the convenience of charging these batteries from just about any available power supply. While these trends in portable power are design challenges, the LTC4155 and LTC4000 make the job considerably easier. In low voltage systems, the LTC4155 provides up to 3.5A of charge current efficiently and with a host of high performance features. The LTC4000 creates a powerful charging solution from virtually any input with unparalleled performance and flexibility.

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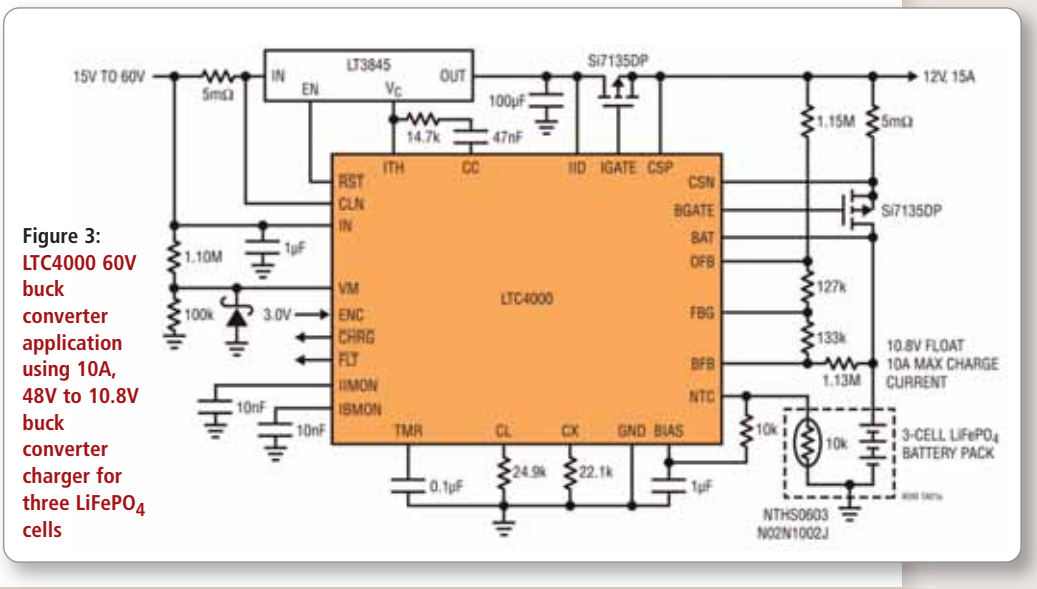

Figure 3: LTC4000 60V buck converter application using 10A, 48V to 10.8V buck converter charger for three $LiFePO_4$ cells

AT Commands Over the Air: A Faster, Less Expensive Way to Administrate Wireless Devices

ONCE WIRELESS DEVICES ARE DEPLOYED IN THE FIELD, THE CHALLENGE IS TO FIND A COST-EFFECTIVE WAY TO MAINTAIN THEM.
BY **CHRISTOPHE CHAMPIGNY**

IN THIS SECTION

WHICH WILL BE PUBLISHED EVERY QUARTER

Sierra Wireless authors will prepare 'how to' articles about the design and development of wireless systems

Earlier this year, one of our metering customers had a field-support problem. A large number of wireless devices, recently deployed, were unable to connect to the network. After a bit of analysis, they tracked the problem back to their production process: a small error had resulted in the main processors being loaded with the wrong version of the configuration code.

Correcting the mistake on the production line was easy enough, but fixing the devices already deployed in the field posed a much bigger challenge.

Sending technicians to every installation to change the configuration settings simply wasn't feasible; it would take far too much time and would be prohibitively expensive. They considered a recall, where every device would be shipped back to the factory, corrected and then redeployed, but that too looked rather costly and time-consuming.

They asked us if we could suggest any other options. As luck would have it, we had recently launched a turnkey service based in the cloud that enables remote device administration on a large scale. The service makes it possible to send AT commands, over the air, to any number of devices. Using this new service, our metering customer was able to correct the configuration settings in all the devices at once. It was a quick, effective fix that minimized down-time and saved cost, as there was no need to issue a recall or send technicians into the field.

Cloud-Based Administration

Figure 1 shows the cloud-based administration service.

The user interacts with a graphic-based web client secured by an RSA key. The web client accesses the management service portal, which in turn communicates, via the Internet and the GSM network, with the AirPrime embedded wireless modules in the field.

To maintain security, the management services portal and the embedded modules communicate using Open Mobile Alliance Device Management (OMA-DM) technology. The OMA-DM connection uses mutual authentication mechanisms to keep the communications private. The communication takes place over the same carrier subscription as other data transmissions. Access to the portal is password-protected, and any data stored on the portal is kept safe in redundant back-ups.

The management service gives administrators the ability to do several things. It lets them monitor key parameters and track communication traffic for a group of devices, and it supports remote upgrade campaigns through a secure delta mechanism. Perhaps most noteworthy, though, is the service's ability to send AT commands over the air.

Sierra Wireless product range in different packages

The OMA-DM connection uses mutual authentication mechanisms to keep the communications private; the communication takes place over the same carrier subscription as other data transmissions

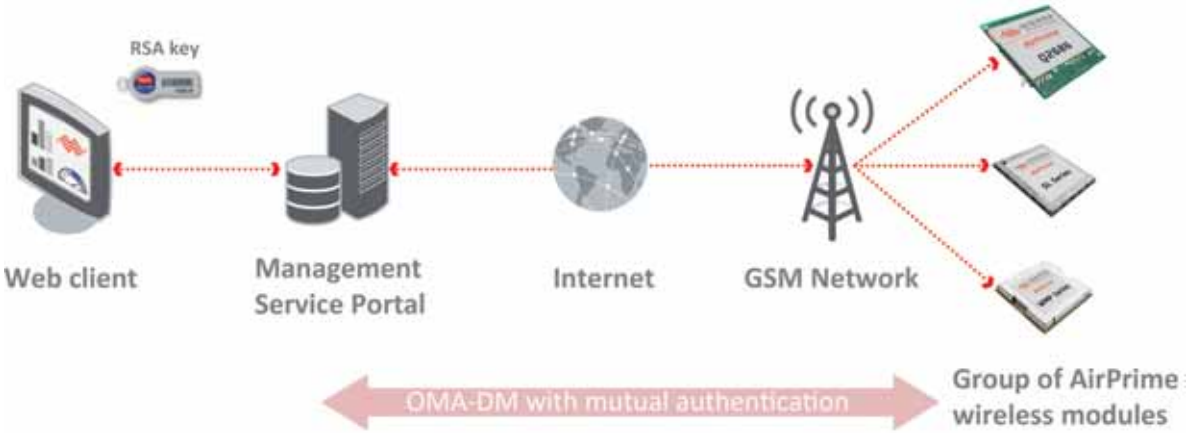

Figure 1: Cloud-based administration for wireless devices

Sierra Wireless AirPrime device

Over-the-Air Transmission

The AT command set has been in widespread use for decades and is the standard language for controlling modems. Just about anyone who's worked with a modem has used AT commands at one time or another. Until recently though, AT commands could only be sent locally, over a wired connection to the device. Now, being able to send the commands wirelessly opens up a number of new possibilities for device administration.

Over-the-air transmission reduces the need to have service technicians in the field, because problems can be identified and corrected remotely. As in the example of our metering customer, being able to transmit AT commands over the air meant they could push a new MCU configuration to every installation from a central location.

As another example, in healthcare, sending AT commands over the air makes it possible to service wireless medical equipment without taking the machinery offline and without having a technician disrupt the patient or interfere with sterile environments, such as intensive care units or operating rooms. In the area of transportation, sending AT commands wirelessly makes it much easier to maintain and service aftermarket products, such as stolen vehicle tracking boxes or the monitoring devices used by insurance companies to track driver behaviour. A whole fleet of devices can be diagnosed and updated while they're operational, without issuing recalls.

Sending AT commands over the air also benefits control and monitoring applications, such as heating and cooling systems or fire and burglar alarms in industrial and residential environments. Systems can be monitored and maintained around the clock, from one or several locations, and with a minimum of service disruptions.

Supported Commands

The AT commands can be used to modify the network or application configurations when usage conditions change, or to change the parameters in the modem itself. The commands can also be used for debugging purposes. If the platform isn't behaving as expected, the administrator can use AT commands to verify parameters, such as which carrier is being used, to help pinpoint the problem and get to a quick resolution.

The initial phase of the service supports those AT commands most relevant to device administration. The service will continue to evolve as new use cases arise. This may mean that the number of AT commands supported will also grow, but, for now, the focus is on device monitoring and device configuration.

Easy-To-Use Interface

The service uses simple dialog boxes and pop-up windows to manage transactions, so it's easy to work with the remote devices. The user just selects the "AT Commands" tab and enters the text of the command to be sent.

There's no need to learn a complex programming language, so there's hardly any learning curve. Users familiar with the simple, straightforward AT command set can begin monitoring and configuring their wireless devices right away.

No Need to Send Technicians Out

Finding an efficient, cost-effective way to monitor, configure and maintain wireless devices once they've left the factory has always presented a challenge. A new kind of turnkey service, based in the cloud, makes it possible to send AT commands over the air, so it's much easier and much less expensive to address problems, issue updates and implement fixes. The service provides a single point of access for tracking, monitoring and configuring even very large numbers of already-deployed devices, so administrative tasks can be executed without recalls and without sending technicians into the field. ●

Brevity

MYK DORMER IS SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
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Bandwidth is a finite resource. With each passing year, new services and applications make greater and greater demands on increasingly crowded frequency allocations. In the wider world, bands can be re-allocated – the withdrawal of analogue television services is an example, or basic infrastructure can be improved, as is the case in the 3G/4G mobile phone networks.

In the low-power wireless sector things are not so "easy". New, usable, bands are not realistically going to be assigned to this relatively small (compared to television or 'phone) industry. Innovative coding or modulation methods have their limits, especially where unit costs are low and investment in R&D is modest, while the inter-related limits of maximum transmitter power and required operating range place an upper bound on link data rate.

This presents the low-power-wireless engineer with only one reasonable course of action: send less data. This seems obvious, until you examine some of the techniques used, or proposed for use, in the telemetry and telecontrol areas. With the rise of third-party network architectures (such as Zigbee and its imitators), and the introduction of methods originating in the wired-network sector (such as TCP/IP), the data overhead needed to execute simple control functions seems to be spiraling out of control.

To illustrate let us consider a simple control task: the remote switching of outdoor decorative festival lighting. Assuming the issues of range, power supply and appropriate frequency band selection have been addressed, what remains is simply the remote control of a switch – or rather a number of switches, all operating simultaneously. This represents one bit of information, and yet I have heard serious suggestions that each light bulb should be assigned its own IPv6 address to be controlled by the transmission of an entire xml page!

Of course I am not actually advocating sending just one bit (i.e. a logic level) over a radio link: it is always necessary to condition the "information" to fit the (noisy, non-DC coupled) characteristics of the radio baseband path, but I am suggesting that the controlling data packet should be more carefully designed to fit the application at hand, rather than trying to use one "generic solution" in each new and very different case.

There is a minimum size to any packet:

- Enough preamble to stabilise the radio link;
- A long enough framing/sync sequence to discriminate data from noise;
- Sufficient payload bits to support the task.

Preamble is a repetitive sequence of bits (usually 010101...) and it is there to enable the transmitter to settle and the receiver data recovery circuits to acquire the data stream. The necessary preamble duration is set entirely by the timing specifications of the radio hardware.

The framing, or synchronisation, sequence is a unique pattern of bits that the receive decoder can recognise, identifying "start of packet" to the decoder process. It needs to be sufficiently long so statistically it cannot be mimicked by noise or interference – the actual number of bits depends on the acceptable "false triggering" probability. In typical control tasks this must be very low, so typically 16 bits of framer, combined with some sort of error checking (parity, CRC or checksum) across the data, is a minimum.

Beyond this, the overall system design will probably require addressing bits, to allow identification of individual units and to eliminate spurious activation in adjacent systems sharing a frequency, possibly network routing information and some form of bit error detection.

The control packet in our imaginary lighting controller could therefore be as simple as:

preamble (defined by radio used)
16 bits of framer
4 bits of address
1 bit of payload (light on/light off)
3 bits error detection

Realistically, allowing for future expansion and flexibility would suggest a slightly longer packet (maybe 8 bits each for address, payload and checksum) but, even then, a five byte (plus preamble) packet could be more than sufficient for a fairly complex real-world task – which is less data than an IPv6 address on its own. ●

I am suggesting that the controlling data packet should be more carefully designed to fit the application at hand, rather than trying to use one "generic solution" in each new and very different case

PLUGGING INTO WHAT'S NEXT WITH MOUSER ELECTRONICS

For European design engineers faced with reducing energy consumption, it is becoming increasingly important to obtain the right product from the right distributor to maintain a speed-to-market advantage. The European Commission (EC) estimates that 80 percent of all product-related environmental impacts are determined during the design stage. Since April 2011, Tier 2 requirements of the Eco-Design Directive 2009/125/EC for Energy-related Products (ErP) are in effect in European Union countries. All external power supplies for consumer electronics and office equipment must meet Level V/ErP2 efficiency standards in order to gain the EC mark of approval, a prerequisite to sales in the European marketplace.

To aid design engineers in the search, Mouser is dedicated to providing an extensive product offering of Level V/ErP2 External Power Supplies from key global suppliers. In addition, the design-fulfillment distributor offers local technical support from its nine support centers across Europe, including a local office in the UK and a flagship office in Munich.

"Our goal is to provide the newest products and most advanced technologies in Level V external power supplies from key suppliers in this area, staying ahead of the tough efficiency standards facing design engineers," says Graham Maggs, Director of Supplier Marketing for Mouser Electronics in Europe. "Engineers know and trust that Mouser will provide energy-efficient design solutions that meet today's standards while providing fast, accurate shipping and local technical support."

Charting the new requirements, the new Level V energy-efficient criteria consist of the following:

- No-load condition power consumption shall not exceed 0.3W (for Po≦51W) or 0.5W (for 51W < Po ≦ 250W)
- Average active efficiency shall not be less than the following limits:

Available through the award-winning www.mouser.com website, Emerson Network Power offers the DA Series medical wall-mount external power supplies, in 12W and 18W versions, with US and EU interchangeable AC plugs. The DCH5 Series wall-mount adapters provide 5W of power and are designed with an AC plug for use in the United States, Europe, United Kingdom, or Australia; and a USB receptacle which accepts an external cable. This unique design eliminates the need for dedicated power cable attachments and connectors. Also available from Emerson Network Power is the DP40 40W Desktop Power Supply Series, featuring both ITE and medical-grade approvals. To learn more, visit **www.mouser.com/emersonpower/.**

Output Power ~ PO	Average Active Efficiency (%) (Output Voltage ≧6V)	Average Active Efficiency (%) (Output Voltage <6V)
PO ≦ 1W	0.48•(PO)+0.14	0.497•(PO)+0.067
1W < PO ≤ 51W	0.063•ln(PO)+0.622	0.075•ln(PO)+0.561
PO > 51W	0.87	0.86

Providing global OEMs with worldwide compliance, Phihong USA offers a comprehensive line of Level V/ErP2-rated standard adapters. Available products consist of 5V-56V desktop versions with outputs of 20W to 120W, 3V-56V wall-mount versions with outputs of 2W-60W, and a Power-over-Ethernet (POE) model. The Phihong Level V/Erp2-compliant lineup includes the industry's first 60W wall-mounted adapter, with interchangeable international AC clips. Visit **www.mouser.com/phihong/.**

Mouser's Power PKC is a value-added resource that helps design engineers speed development.

SL Power's broad offering of Level V/ErP2-compliant external power supplies includes the CENB/MENB series, offering both ITE and medical approved devices. This new single output series covers a range of 12 power levels from 10W to 220W, available in models from 5V to 48V. Desk-top and wall-mount versions are offered, with interchangeable blades to meet country specific inlet requirements. Visit http://www.mouser.com/slpower/.

Finally, Cincon presents an array of Level V/ErP2-compliant external power supplies comprised of wall-mount adapters, as well as desk-top models, available with US, international, and interchangeable plugs. Cincon adapters are available with medical and/or ITE approvals. The newest Level V/ErP2 addition to Cincon is the wall-mount TR15RM Series, with interchangeable AC plugs, delivering up to 15W of power. Learn more at http://www.mouser.com/cincon/.

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The distributor's award-winning website www.mouser.com., features more than 2,500 Product Knowledge Center (PKC) training sites and represents the most up-to-date resource for design engineers to quickly search products, manufacturers or applications. For more information and a complete listing of Level V/ErP2-compliant external power supplies available at Mouser Electronics, visit **www.mouser.com/knowledge/power/levelveps/.**

NOVEL NUMERICAL SMALL SIGNAL MODELLING TECHNIQUE

FOR NON-PWM, DISCONTINUOUS ZVS BUCK-BOOST CONVERTER

MAURIZIO SALATO AND **DAVIDE FRANZONI** FROM V·I CHIP INC PRESENT A SIMPLE NUMERICAL METHODOLOGY TO MODEL SMALL SIGNAL AC CHARACTERISTICS OF PWM SWITCHING CONVERTERS, AND SPECIFICALLY, A DISCONTINUOUS BUCK-BOOST CONVERTER IS ANALYZED

Several techniques have been developed over the years in order to model the small signal AC characteristics of PWM switching converters with various features, e.g. multiphase, variable frequency [1, 5]. If non-conventional modulation techniques are used, they become analytically difficult, because of the nonlinear behaviour introduced by the non-PWM strategy.

Specifically, a discontinuous buck-boost converter is analyzed, where the ZVS transitions are obtained by managing reactive power between converter reactive elements, and modulation timing is based on three real-time variables. The different methods have been compared on one particular model item, the low frequency modulator gain (control node voltage to converter output current).

Power Conversion

State-of-the-art power conversion often relies on non-conventional control techniques [2]. The non-conventional usually refers to the general control architecture, where multiple feedbacks, feed-forward loops or digital state machines are just a few examples. The focus of this article is a particular buck-boost converter topology [3], which requires a modulation technique based on three different inputs: the converter instantaneous input voltage, the instantaneous output voltage and the more traditional control node voltage.

The purpose of this modulation technique is to eliminate the inherent nonlinear characteristics of the topology, such that the effective transfer characteristic, as seen from control node to output, can be assumed linear for general control purposes. This obviously puts the burden on the modulator AC modeling and, at

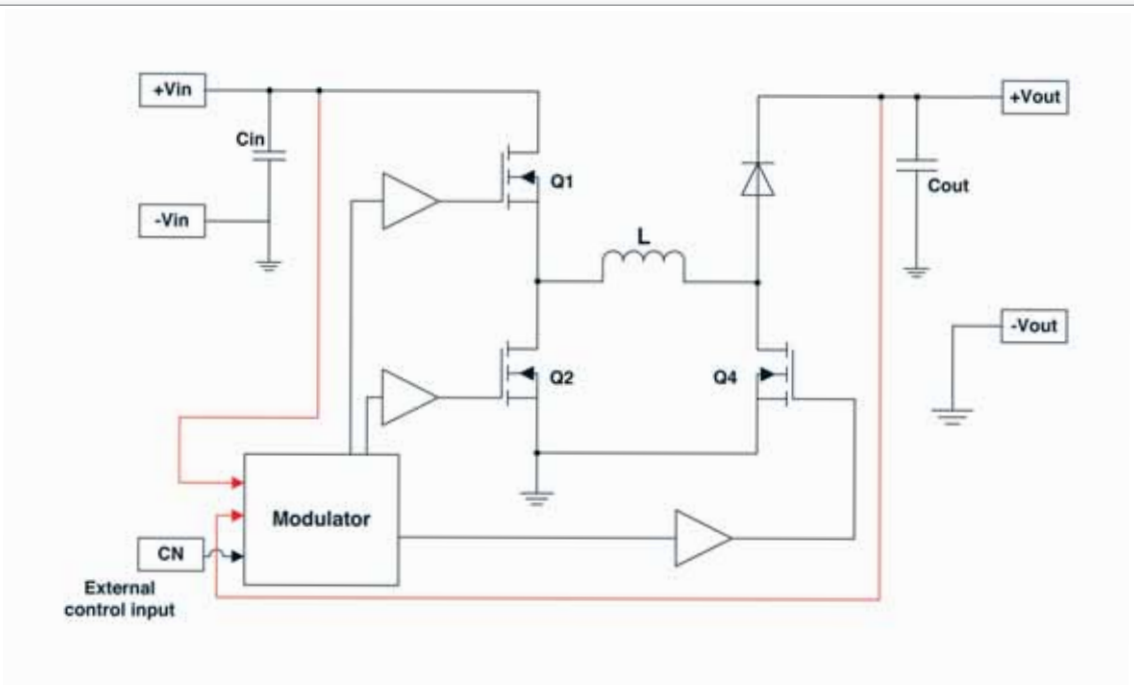

Figure 1: Block diagram of the considered ZVS buck-boost converter

the same time, requires a more complex model in order to account for an input-to-output transfer characteristic that might not be negligible, but usually is.

The System

Figure 1 shows a block diagram of the considered converter structure [3]. The red lines emphasize the non-conventional inputs to the modulator block. Figure 2 shows the topological states in Boost Mode ($V_{IN} < V_{OUT}$) [2].

It is important to notice that the second topological phase (inductor connected between input and output) is uncommon, as is the fourth (inductor clamped to a steady current level). The equation describing the output current of the converter involves multiplications of time-varying variables such as $V_{IN}(t)$, $V_{OUT}(t)$ and $V_{CN}(t)$ that are affected by the nonlinear characteristic of the system. Therefore, in order to design a simple linear feedback, it is necessary to provide a linear equation describing the system around each steady state condition of operation and derive the equivalent AC small signal model.

The Problem

In general, a nonlinear system can be always described as the sum of different order terms; in case of the considered converter state variable (I_{OUT}):

i_{OUT} = (DC terms) + (1st order AC terms) + (2nd and higher order AC terms)

The DC (average) transfer characteristic for the modulator block and the converter power-train can be written as a combination of DC inputs (such as input, output and control node voltages) and system parameters (such as inductance):

$$I_{OUT} = f\,(V_{CN}, V_{IN}, V_{OUT}, L) \qquad (1)$$

It is important to note that L is the only constant, as input and output voltages have a direct impact on the timing (and not just on the energy stored on the inductor). The small signal transfer characteristic will therefore have the two extra inputs and include 1st and all the higher order terms:

$$\hat{i}_{OUT} = f\left(\hat{v}_{CN}, \hat{v}_{IN}, \hat{v}_{OUT}, V_{CN}, V_{IN}, V_{OUT}, L\right) \qquad (2)$$

The resulting model is shown in Figure 3, where G_{CN} and G_{IN} are the small signal, low frequency gains of the transfer functions from control node to output and from input to output respectively. Notice that r_{OUT} models the AC output impedance characteristic.

The general approach requires the use of superposition principle, with regard to the multiple inputs. Equation 2 can only be derived by assuming all the variables ($V_{IN}(t)$, $V_{OUT}(t)$ and $V_{CN}(t)$) but one constant, applying for each one the AC variation sufficiently small in magnitude, calculating the effect on the output current and then moving on to the next variable; finally assembling the entire function.

The three approaches discussed here apply to all the items in the small signal model. For sake of simplicity, the different

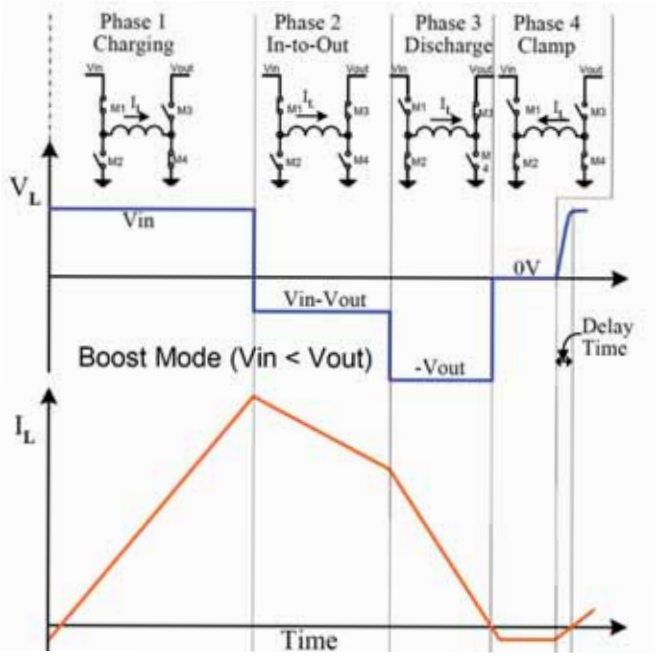

Figure 2: Topological states of the considered ZVS buck-boost converter

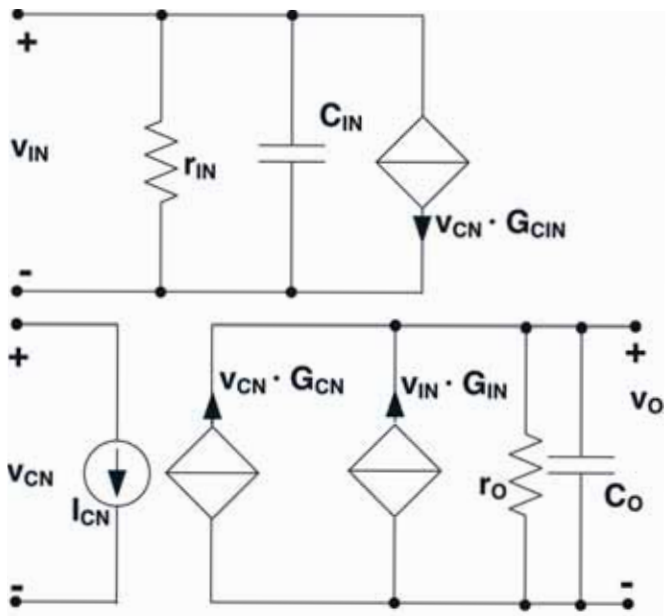

Figure 3: Small signal model of the converter

methods have been compared on one particular model item only, the low frequency modulator gain (control node to output) G_{CN}.

Analytical Approach

One valid approach (common in small signal analysis, [5]) is to identify G_{CN} by partial derivatives of the averaged transfer Equation 1:

$$G_{CN} = \left.\frac{\partial I_O}{\partial V_{CN}}\right|_{V_{IN},\, V_{OUT} = \text{CONST.}} \qquad (3)$$

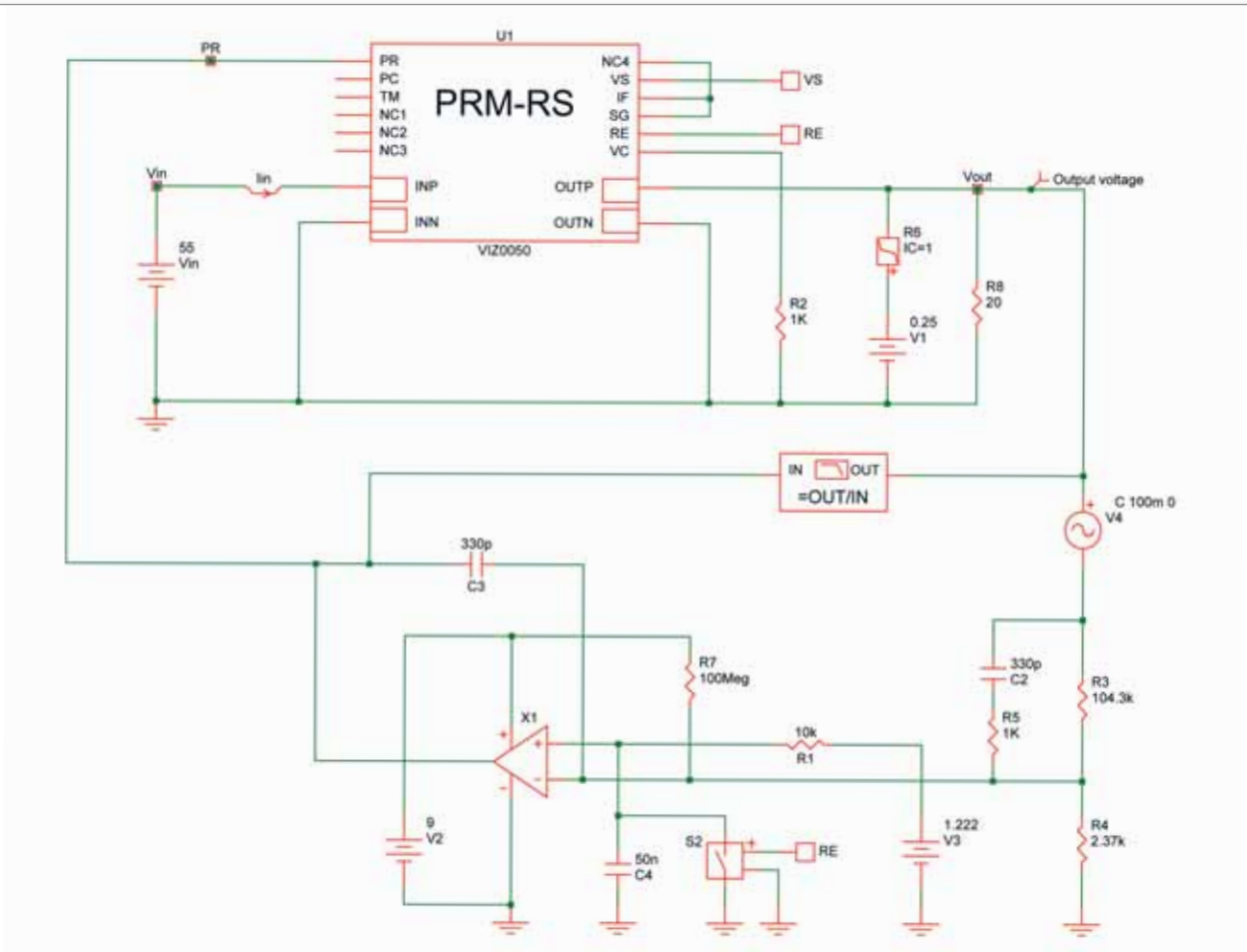

Figure 4: SIMPLIS model of the considered converter

Although this is not the most efficient methodology in mathematical terms, it is necessary because of the nonlinearity of the modulation scheme.

In the case considered, the approach turns mainly into a differential calculus exercise, somewhat complicated by the number of terms within Equation 1. Moreover, because of the system nonlinearity, it is difficult to judge if second order terms can effectively be neglected, as they might actually contribute to the result in some specific conditions. The authors chose not to neglect any; suffice to say that the complete, closed-form

> *The POP analysis in SIMPLIS is a powerful tool, as it can account for any nonlinear device as well as parasitics, if present*

Equation 3 for parameter G_{CN} in the case considered contains more than 25 terms.

Although analytical, this method is prone to propagating errors because of necessary assumptions on control timing parameters. In the analyzed case, a well known and characterized nonlinear behavior could not be considered, as the resulting function would have been extremely difficult to manage in closed form.

Numerical Approach

The objective is to simplify the modeling across the entire operating range. To this point, a purely numerical approach can be used. The approach consists in separating higher order terms in Equation 1, and can be summarized in the following steps:

(a) Model the three-variables timing present in the analog control IC (see Figures 1 and 2):

$$\begin{cases} t_1 = f\left(V_{IN}, V_{OUT}, V_{CN}\right) \\ t_2 = f\left(V_{IN}, V_{OUT}, V_{CN}\right) \\ t_3 = f\left(V_{IN}, V_{OUT}, V_{CN}\right) \\ t_4 = f\left(V_{IN}, V_{OUT}, V_{CN}\right) \end{cases} \quad (4)$$

(b) Model the converter output average current as a function of the timing (the input, output and control node voltages), as well as the inductor value:

$$I_{OUT} = f\left(t_1, t_2, t_3, t_4, V_{IN}, V_{OUT}, V_{CN}, L\right) \quad (5)$$

(c) For a defined DC condition, apply a finite "small" differential to one parameter (with all the others constant), for example the control node V_{CN}:

$$\begin{cases} V_{CN+} = V_{CN} + \varepsilon \\ V_{CN-} = V_{CN} - \varepsilon \end{cases} \Rightarrow \hat{v}_{CN} = V_{CN+} - V_{CN-} \quad (6)$$

and calculate the impact on the output current:

$$\begin{cases} I_{OUT+} = f\left(t_{1+}, t_{2+}, t_{3+}, t_{4+}, V_{IN}, V_{OUT}, V_{CN+}\right) \\ I_{OUT-} = f\left(t_{1-}, t_{2-}, t_{3-}, t_{4-}, V_{IN}, V_{OUT}, V_{CN-}\right) \end{cases} \Rightarrow \hat{i}_{OUT} \cong I_{OUT+} - I_{OUT-} \quad (7)$$

(d) Calculate the parameter of interest, in the considered example G_{CN}:

$$G_{CN} \cong \frac{\hat{i}_{OUT}}{\hat{v}_{CN}} \quad (8)$$

It is obvious that several higher order function terms are included in the modeling, as long as numerical resolution issues do not arise. In fact, step (c) utilizes the entirety of converter transfer function, including higher-order terms, as steps (a) and (b) do not neglect any interaction among the various variables, and capture all of them in each numerical output.

Simulation Approach

The entire converter has been modeled in SIMPLIS environment. The switching model can be analyzed through "Periodic Operating Point" (POP) analysis, which provides AC characteristics of virtually any element within the closed feedback loop. Figure 4 shows the model with the closed voltage loop in AC POP analysis configuration.

The POP analysis in SIMPLIS is a powerful tool, as it can account for any nonlinear device as well as parasitics (if present). The model utilized is considered state of the art and has been extensively validated and confirmed to be within ±5% of V_{CN} statistical characterization data across the operation range.

Comparisons and Conclusion

The simulation model showed good match with both, analytical and numerical modeling methods. The graphs in Figures 5 and 6 summarize the obtained low frequency control node to output voltage gain, which is defined as:

$$\left.\frac{v_O}{v_{CN}}\right|_{f \to 0} = G_{CN} \cdot \frac{r_O \cdot R_{LOAD}}{r_O + R_{LOAD}} \quad (9)$$

In a few cases, the three methods show a mismatch up to 5dB; however, average mismatch is just 1.5dB.

Normally, terms higher than 1st order are not included in parameters of AC small signal modeling; however, the proposed numerical approach shows a reasonably good match when the same higher order terms are instead included, therefore offering a simple approach in complex, multi-variable systems. Moreover, the numerical method requires significantly less time (and resources) compared to the others, and can easily be developed in spreadsheets or numerical tools like MathCad or MatLab. ●

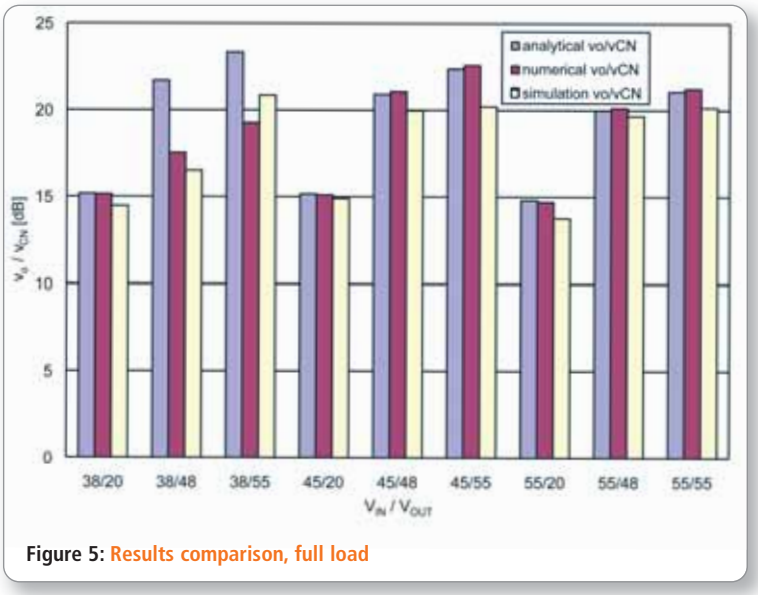

Figure 5: Results comparison, full load

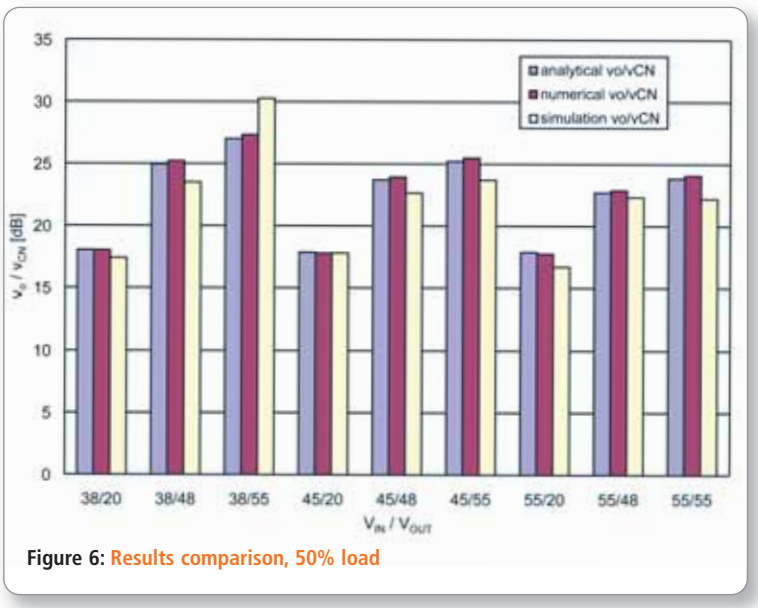

Figure 6: Results comparison, 50% load

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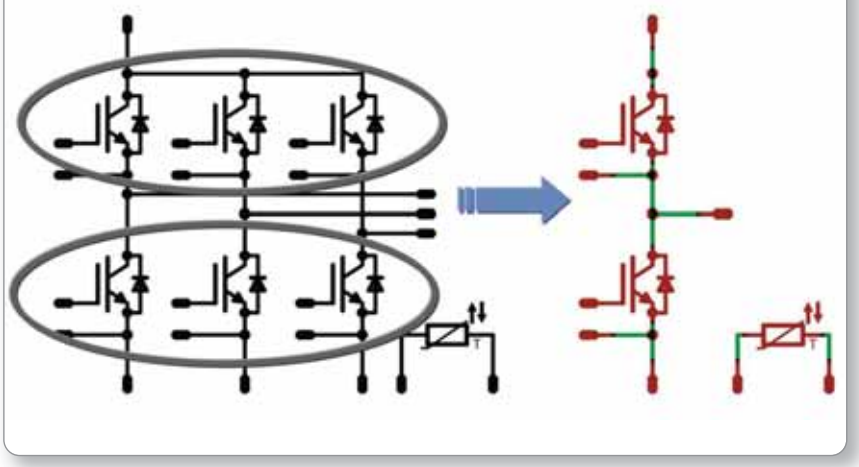
PARALLELING OF IGBTs AND DIODES OF A POWER MODULE – PUSHES POWER CAPABILITY

WERNER OBERMAIER, HEAD OF PRODUCT MARKETING AT VINCOTECH GMBH,

DESCRIBES ONE APPROACH OF PARALLELING IGBTS AND DIODES WITHIN A POWER MODULE TO EXTEND ITS POWER CAPABILITY

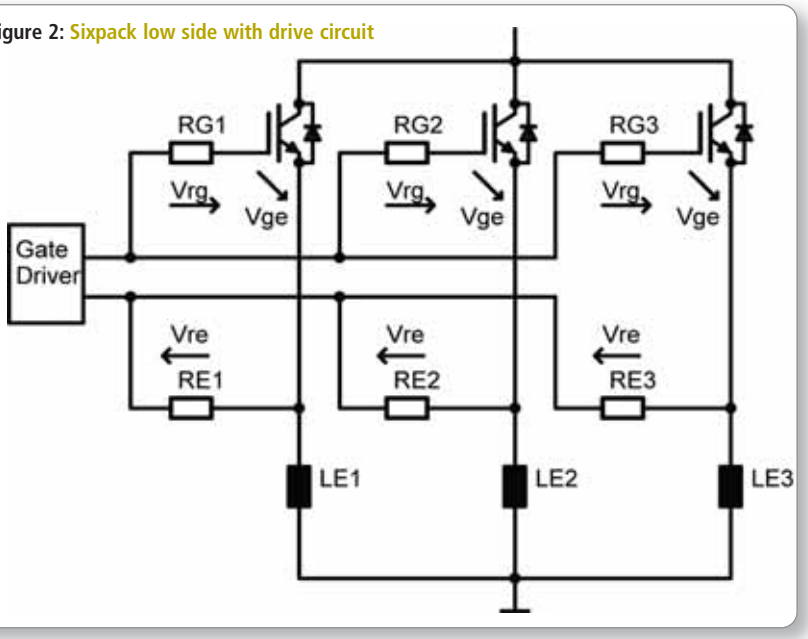
Figure 1: Sixpack used as a half bridge



The increasing request for motor drives with higher power levels is also driving the demand for power modules providing higher currents. The conventional approach to fulfill this requirement is to look for dedicated high current power modules. This article describes the alternative approach of paralleling IGBTs and diodes within one power module to extend its power capability, for example using a 35A sixpack module as a 100A half bridge. This approach provides an advantage due to the improved thermal behavior of several small chips rather than fewer big ones. The breakthrough in performance is seen when the real-life data of parameter variations within one power module are considered, instead of the datasheet values, which suggest a much higher spread. Figure 1 shows how a sixpack can be used as a half bridge.

The calculations are based on the P700-F sixpack module from Vincotech, which uses Infineon IGBT3 Low Loss IGBTs and Emcon HE FREDs. Both components feature a positive temperature coefficient for their voltage drop at high junction temperatures. This is important in avoiding thermal runaway of individual components when paralleled.

Figure 2: Sixpack low side with drive circuit



Switching Behavior

When paralleling IGBTs, special attention has to be given to the drive circuit. Because of variations in the gate threshold voltage of the different chips, simply connecting the gates is not adequate. Instead, each gate has to be driven by its own gate resistor and, therefore, its own current source in order to ensure that the chip with the lowest threshold voltage does not clamp the voltage for the others and carry all the current. Furthermore, the layout of the emitter circuit has to be very symmetrical in order to minimize differences in emitter inductances and resistances. Even minor, unavoidable

differences in emitter inductances and resistances will generate compensation currents between the gate drive emitter connections.

To limit these currents, the introduction of an emitter resistance in the drive circuit is strongly recommended. It is best to use a resistor in the range of at least 0.5 Ohm, but not to exceed approximately 1/3 of the total gate resistance. To ensure real emitter drive sensing, the module needs to provide emitter sense connections with separate bond wires, as do the power modules from Vincotech.

Moreover, any mismatch in the delay, rise and fall times of the driver circuit are to be avoided, as these will also result in a mismatch of switching currents and, therefore, switching losses of the different devices. Recommended is the use of a single gate drive circuit with individual gate and emitter resistors for the different IGBTs, as shown in Figure 2. If higher drive currents are required, a single driver circuit with individual push-pull driver stages is recommended.

Since the switching losses and their mismatch depend on the layout, it is good practice to measure and confirm them in the real application. If the recommendations above are followed, it is fair to assume that the switching losses for the different devices will match to within 10 to 15%.

On-State Behavior

The on-state behavior is more critical. The datasheet for the P700 sixpack suggests a relatively large variation in IGBT collector-emitter and diode forward voltage. For the IGBT, the collector-emitter saturation voltage at 25°C is given as 1.7V typical and 2.25V maximum. No value is provided for the minimum voltage. Considering this information, the paralleling of chips cannot be recommended, since the current sharing among the individual IGBTs cannot be ensured. The situation is even worse for the diodes.

In reality, however, the actual spread of the devices within one power module is much lower. This is due to the fact that they are picked from locations either exactly next or very close to each other on the same wafer, and will therefore feature extremely similar electrical characteristics.

To determine the real voltage variation, Vincotech has collected data from more than 40,000 modules produced in multiple lots distributed over a period of more than one year. This evaluation shows that the saturation voltage variation for 99.99% of the high side or low side IGBTs does not exceed 310mV at 25°C and 450mV at 125°C respectively.

For the FREDs, the value is 400mV at 25°C and 490mV at 125°C. The distribution of the voltage spread within the measured series is shown in Figure 3 for the IGBTs and Figure 4 for the diodes. Table 1 shows the probabilities for different voltage spreads.

When considering current sharing, apart from the low or high side of the voltage variation of the IGBTs and FREDs, it is important to know what value the third device will exhibit. Again, instead of using a worst-case view based on the datasheet voltage spread, the

Figure 3: IGBT saturation voltage spread

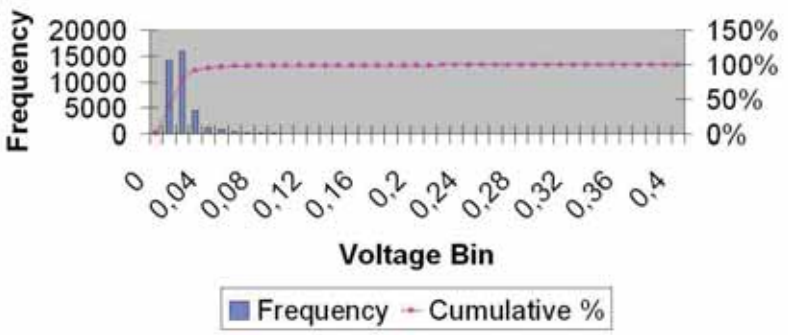


Figure 4: FRED forward voltage spread

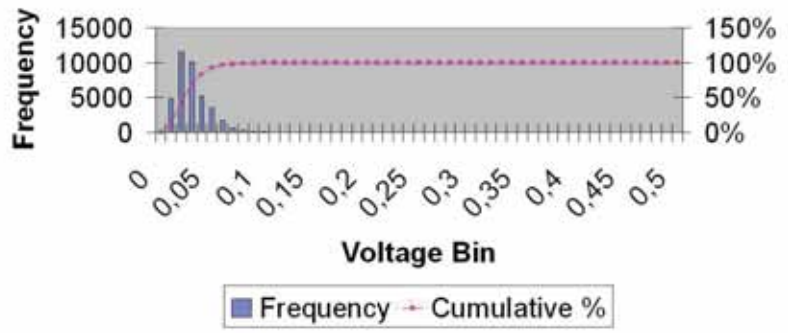


Table 1: Voltage spread for different probabilities

IGBT Voltage

Probability	Voltage Spread (min/max) Tj = 25 °C	Voltage Spread* (min/max) Tj = 125 °C
99.1%	≤ 100 mV	≤ 140 mV
99.9%	≤ 240 mV	≤ 350 mV
99.99%	≤ 310 mV	≤ 450 mV

*) values are extrapolated based on 25 °C data

FRED Voltage

Probability	Voltage Spread (min/max) Tj = 25 °C
99.1%	≤ 90 mV
99.9%	≤ 200 mV
99.99%	≤ 400 mV

*) values are extrapolated based on 25 °

Figure 5: IGBT current de-rating distribution

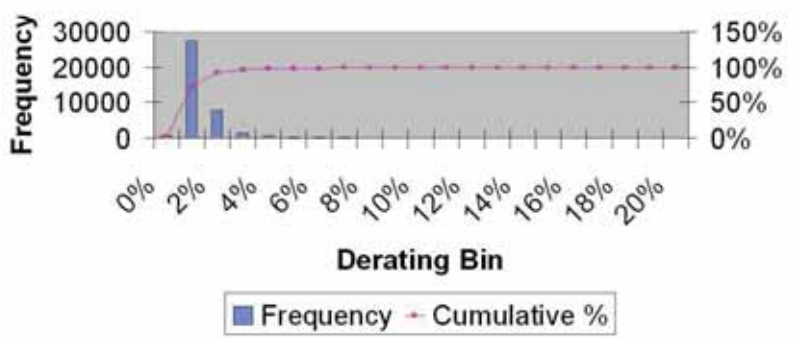


Figure 6: FRED current de-rating distribution

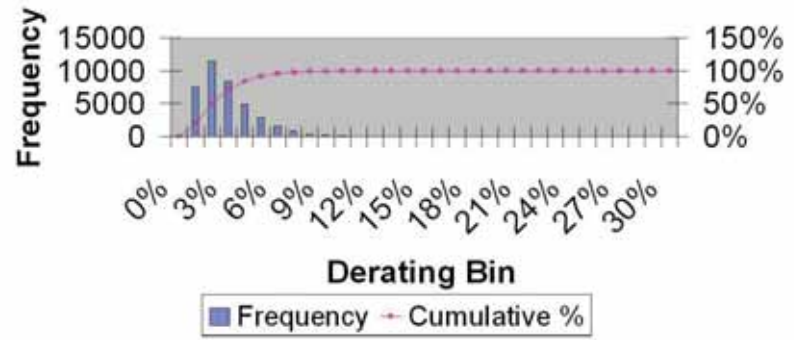
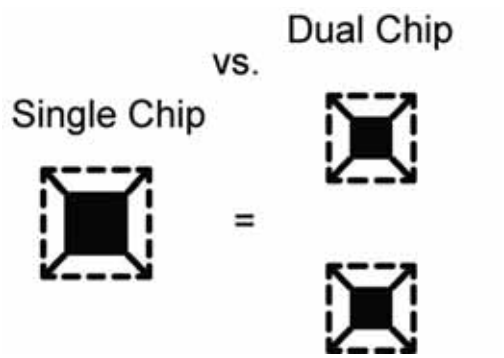


Figure 7: Improved thermal spreading



actual data collected from the 40,000 modules can be used. Based on this information, current sharing can be calculated for each module individually.

The device with the lowest voltage drop is used to determine the voltage for the other two devices. By doing so, it is ensured that the best device will run at the maximum current level it is designed for and that the other devices will run at a lower current level well within their design limits.

The current of the other devices can be calculated using the dynamic voltage slope of the saturation voltage for the IGBT or the voltage slope of the forward current for the diode. The total current of the module can be calculated as:

$$I_{total} = I_{nom}\ (best\ device) + I_2 + I_3$$

and the current de-rating for the module can be calculated as:

$$D = I_{total} / 3 * I_{nom}$$

Figures 5 and 6 show distribution of the de-rating for the paralleled IGBT and FRED section of the module. Table 2 shows the probabilities for current de-rating.

For a design where the 13% de-rating for the IGBT and 25% de-rating for the diode are used, only one device out of 10,000 will exceed the targeted design limit of all devices running less than the originally targeted current. Due to this fact, this single device out of 10,000 devices exhibit a lifetime which is lower than expected.

On the other hand, the distribution curves show that, for the IGBTs, 90% of the modules will share the current within 2% and 99% within 6%. For the FREDs, current sharing for 90% of devices will be within 5% and for 99% within 9% respectively. With a design made using the 13% and 25% de-rating, the majority of the modules will run with a much better current sharing, thus running at a temperature lower than expected. This will not only compensate for the lower lifetime of the few devices, but also improve the overall lifetime and reliability of the design.

Thermal Behavior

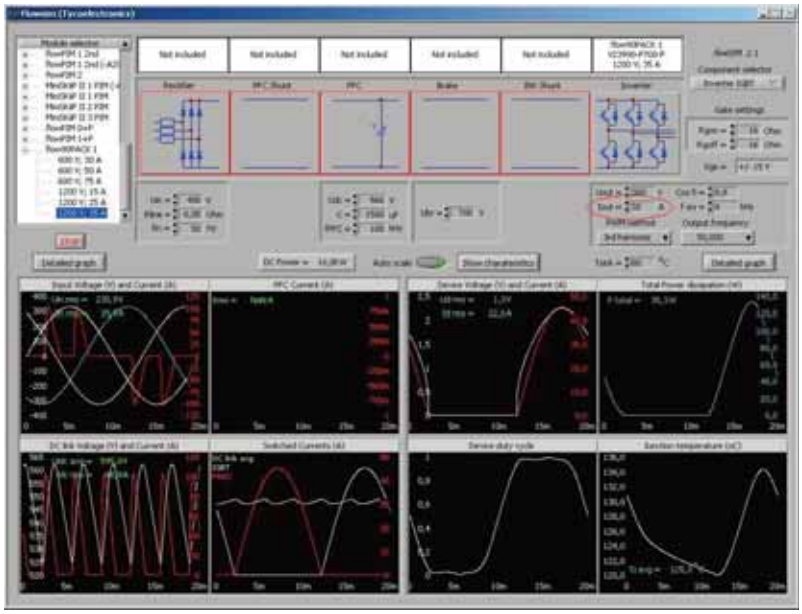
Using multiple smaller chips instead of one larger chip improves the thermal behavior, described by the thermal impedance of a device. This is due to the fact that not only the chip itself, but also a certain area around the chip, will participate in the transfer of heat from the chip to the heatsink. Figure 7 shows the improved thermal spreading when using two small chips instead of one large, with an equal total area in both cases.

This can also be seen when comparing the thermal resistance of the 100A IGBT in the P569-F module with the 35A IGBT in the P700-F module. The thermal resistance junction to heatsink for the 100A device given in the data sheet is 0.57K/W. The resistance for the single 35A IGBT is 1.29K/W, resulting in an overall resistance of 0.43K/W, when three of them are used in parallel. This provides an improvement of about 25% in thermal performance, which compensates for some if not all of the de-rating required due to the non-ideal current sharing.

Example Using 35A Sixpack Power Module

As an example, the performance of a 35A sixpack module used as a half

Figure 8: *flow*SIM P700 IGBT phase current determination



bridge is compared to a 100A single-chip half-bridge module. The conditions and parameters used for the evaluation are shown below:

– **Device:**
  P569: half bridge 100A/1200V
  P700: SixPACK 35A/1200V
– **Motor frequency:** 50Hz
– **Cos phi:** 0.8
– **PWM frequency:** 4kHz
– **Heatsink temperature:** 80°C
– **Tj max:** 125°C

In the first step, the phase current capability of the individual devices, the IGBT and the FRED are determined for the P700 and P569, using the Vincotech flowSIM simulator. This simulator already takes the improved thermal performance of the smaller chips into account, which does not need to be explicitly considered later on. Figure 8 shows the flowSIM result for one 35A IGBT of the P700-F module.

In the next step, the current de-rating is applied and the result is multiplied by 3 for the three paralleled devices. Table 3 shows the result for the IGBT and FRED for both solutions.

The result reveals that the overall performance for the application at hand can be improved by 13% using the P700-F 35A sixpack instead of the P569-F 100A single-chip half-bridge. The actual improvement will vary for different application parameters and as such it needs to be evaluated at the most critical point.

Boosting Performance

The use of sixpacks as half bridges can boost the performance and enable the use of preferred modules and packages at higher power levels. Special care has to be taken regarding the drive circuit, and current de-rating is to be considered when calculating the current of a single chip used in a multi-chip arrangement.

Individual emitter sense down to chip level and symmetrical design are required of the power module, both of which are met by Vincotech modules. With the use of components in parallel, not only can higher current levels be reached, but also the reliability of the design can be improved. ●

Table 2a: IGBT current derating for different probabilities

IGBT Current Sharing Probability

Probability	Required Current Reduction
99.9%	11%
99.99%	13%

Table 2b: FRED current derating for different probabilities

FRED Current Sharing Probability

Probability	Required Current Reduction
99.9%	14%
99.99%	25%

Table 3: Comparison between single chip P569-F and multi-hip P700-F solution

	P700-F		P569-F	
	IGBT	FRED	IGBT	FRED
Simulated phase current	32 A	103 A	74 A	180 A
Required derating	13%	25%	0%	0%
Resulting phase current	**28 A**	**77 A**	**74 A**	**180 A**
Number of devices	3	3	1	1
Total phase current	**84 A**	**232 A**	**74 A**	**180 A**
Limiting value for application	**84 A**		**74 A**	
Improvement	**13%**			

WIBAWA CHOU AND **CESARE BOCCHIOLA** FROM INTERNATIONAL RECTIFIER CORPORATION ANALYSE THE NEUTRAL POINT CLAMP INVERTER TOPOLOGY, WHICH EVOLVED FROM SUCCESSFUL ADVANCES AT HIGHER VOLTAGE LEVELS, AS AN ALTERNATIVE TO THE HALF BRIDGE OR FULL-BRIDGE TOPOLOGIES USED IN SOLAR INVERTER DESIGNS

MAXIMISING INVERTER EFFICIENCY FOR GRID-CONNECTED SOLAR GENERATORS

The rising costs of traditional fossil fuels, combined with the increasing efficiency and accessibility of "green" power sources, such as solar or wind-powered generators, is encouraging householders and commercial property owners to set up their own micro generators. This will not only take care of their individual energy needs but also take advantage of feed-in tariffs that enable individuals to sell their excess generating capacity to utility companies.

There is an anticipated consumer market for small and medium-sized renewable energy generating equipment, which will place pressure on suppliers to deliver continuous and rapid improvements in aspects such as efficiency, power quality, cost and size. All aspects of the generating system, from the solar panels or small wind turbine to the charge control, storage and DC-to-AC inverter electronics, will be required to exhibit exemplary performance in each respect.

Given that the efficiency of today's solar panels is relatively low, in the region of 15-20%, innovative techniques to drive up the efficiency of the inverter stage will be critically important if renewable energy sources are to be harnessed effectively.

Improving Inverter Design

A number of approaches to solar inverter design have already been commercialised. However, each has limitations in terms of efficiency and cost. Inverters built using a multi-level topology will improve the efficiency of the final link between tomorrow's micro-generators and the grid.

Half-bridge and full-bridge topologies are commonly employed in green-energy applications, such as rooftop home systems, designed to power typical domestic loads and feed any unused energy into the grid. The inverter is supplied by positive and negative DC voltage rails of up to ±400V.

The power switches making up the bridge are commonly Insulated Gate Bipolar Transistors (IGBTs), which combine the high current-carrying capability of a bipolar transistor with a MOS gate structure that can be controlled conveniently using a voltage signal. IGBTs are usually supplied with a matched co-packaged diode. Table 1 summarises the advantages of IGBTs, compared to MOSFETs, for use in a grid-connected inverter operating from a DC bus of several hundred volts.

The half-bridge topology, which comprises one high-side and one low-side power switch, as well as bulk capacitors and an output filter, is built using only two IGBTs, as shown in Figure 1. This topology delivers benefits such as low component count, which can help to save bill-of-materials costs. To ensure adequate power quality, necessary to allow feed-in to the grid, an AC output of low harmonic content is achieved by using pulse-width modulation at a high frequency. Applying PWM at 20kHz produces a close approximation to a sine wave at the normal AC line voltage and frequency

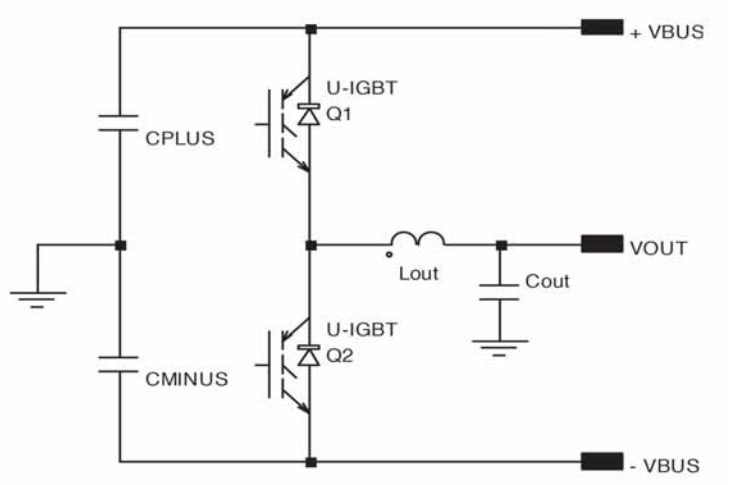


Figure 1: Half-bridge inverter typically employing 1200V IGBTs to operate from ±400V DC supply

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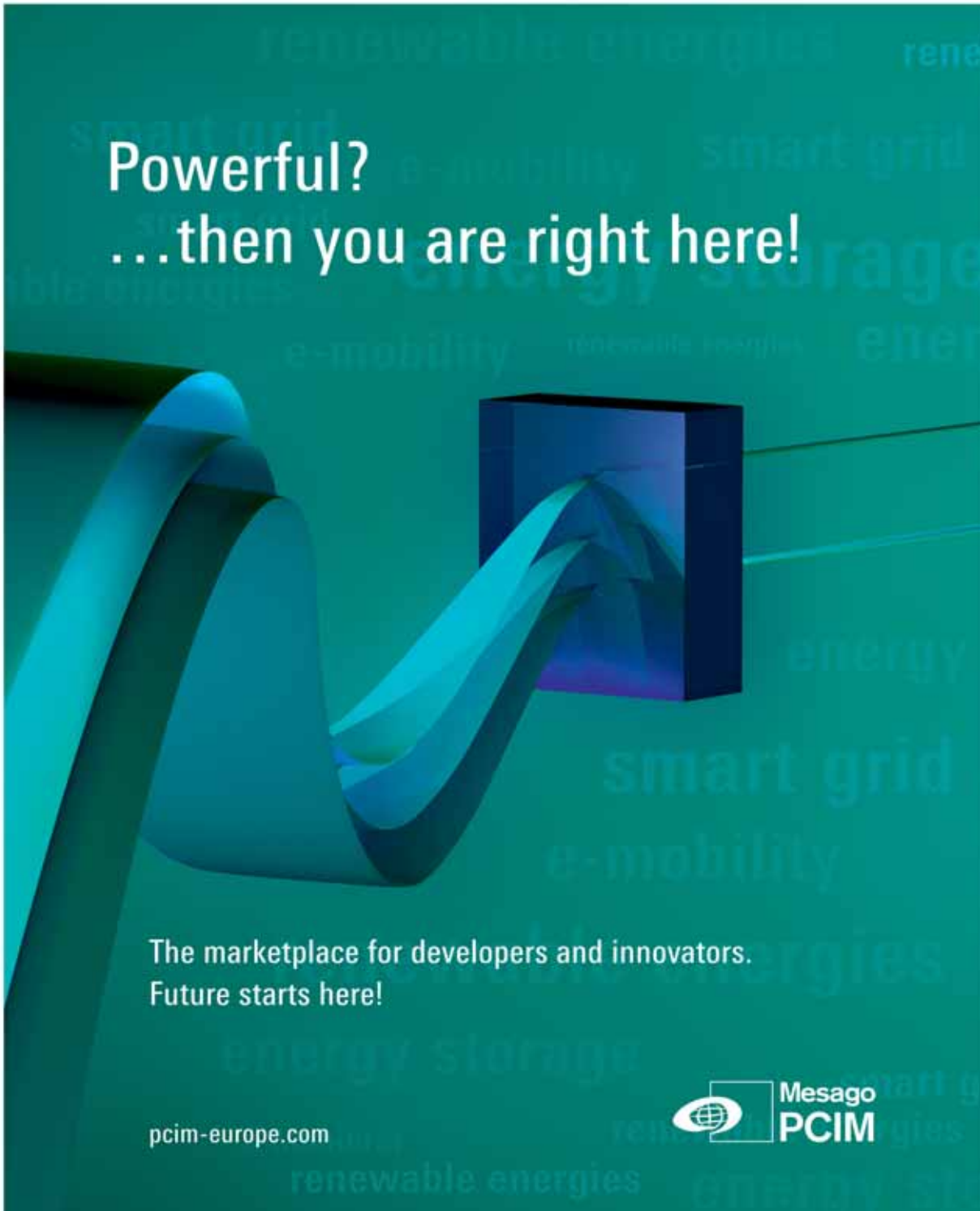

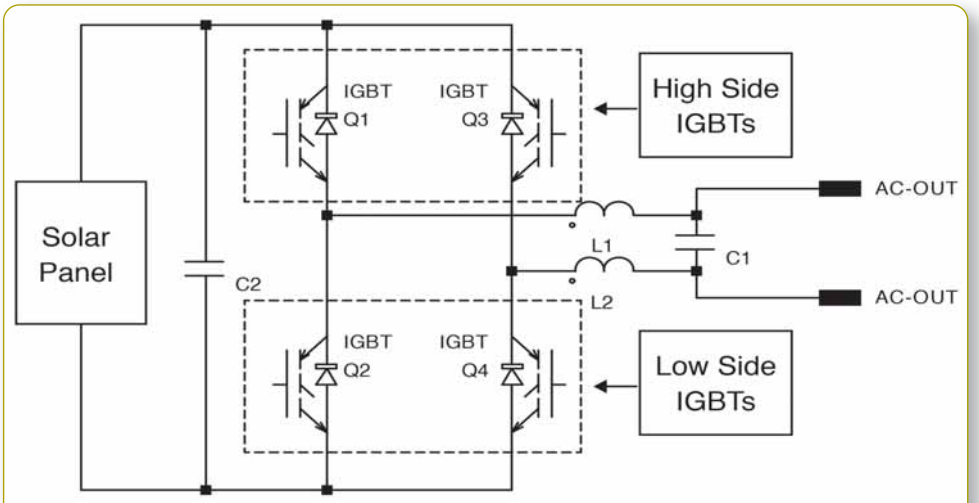

Figure 2: The full-bridge inverter topology allows asymmetrical modulation of high-side and low-side IGBTs for optimum efficiency

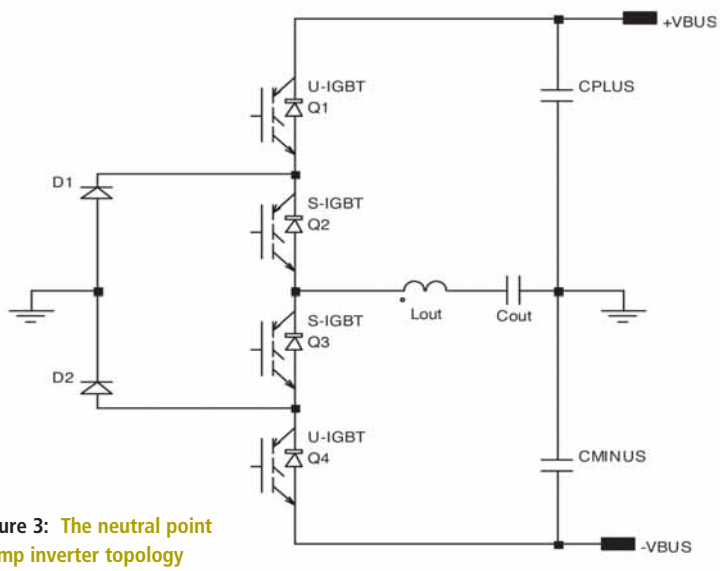

Figure 3: The neutral point clamp inverter topology

(50/60Hz). Since the modulation frequency of 20kHz is outside the normal human hearing range, audible noise is also minimised.

However, standard IGBTs are not well suited to high switching frequencies. Device designers must typically find a compromise between turn-off time and on-state voltage drop (VCEon). Ultrafast planar IGBTs achieve faster turn-off times and lower switching losses, at the expense of a higher voltage drop. Trench-gate IGBTs have been developed for applications requiring improved efficiency at high switching frequencies, such as solar inverters. These devices achieve lower voltage drop and total switching loss than ultrafast planar IGBTs.

Operating the half-bridge inverter at a lower IGBT switching frequency is not desirable, as this will result in increased audible noise and require the use of larger filtering components.

Full-Bridge Topology

Using a full-bridge inverter enables designers to mitigate the switching losses of a half-bridge topology by applying asymmetrical modulation. In a full-bridge inverter as shown in Figure 2, the high-side IGBTs are modulated at 20kHz while the low-side devices are commutated at 50/60Hz. A significant proportion of the switching losses incurred in the low-side circuit are eliminated, effectively increasing the efficiency of the inverter.

Even so, some drawbacks remain. As with the half bridge, the IGBTs must have a high blocking voltage of up to 1200V to provide adequate safety margin in a ±400V DC system. Devices with 1200V blocking voltage tend to have a higher voltage drop and higher switching losses than IGBTs with lower blocking voltage. It is also difficult to satisfy the demand for a smooth sinusoidal output characteristic, containing minimal harmonics, without the use of large output filtering components.

Multi-Level Inverters

Inverters making use of a multi-level topology are now being adopted in grid-

Evaluation criteria	IGBT attribute
Cost	Lower cost per ampere for high-current applications such as renewable energy
Switching performance	Switching performance can be optimised for applications requiring 20kHz to 100kHz switching frequency
Temperature stability	Percentage increase of conduction loss at elevated temperature is much less than MOSFET
Power density	IGBT chip size is smaller, enabling smaller power module with less parasitic inductance
Circuit design	IGBT, as a voltage-controlled device, permits gate drive circuit design similar to that for MOSFET inverter

Table 1: Advantages of IGBTs in grid-connected inverter applications

NEW FUNCTION/ARBITRARY WAVEFORM GENERATORS

Telonic Instruments Ltd launch Rigol's new DG4000 series waveform generators, the latest development in their family of fast, intuitive, modern test and measurement instruments. A function/arbitrary waveform generator, the DG4000 features 2 output channels with up to 160 MHz output, 14 bit voltage resolution, a 500 MSa/s sample rate, a high resolution 7" display and 130 built-in waveforms.

Rigol's DG4000 series helps engineers accomplish a ranging of testing by combining many functions into one easy-to-use instrument. Functions include Arbitrary Waveform Generator, Function Generator, Pulse Generator, Harmonic Generator, and Analogue/Digital Modulator. The DG4000 series also incorporates Rigol's Direct Digital Synthesizer (DDS) technology, ensuring signals are delivered with stability, precision, purity and low distortion.

Designed to target the requirements of R&D engineers, production test engineers' and universities, Rigol's DG4000 series is ideal for applications in the communications, aerospace/defence, research and education, industrial and consumer electronics, computing and instrumentation industries.

DG4000 Series waveform generators are available in 60, 100 or 160 MHz models. Pricing begins at £565.

For more information please contact Doug Lovell at Telonic on 01189786911 **www.rigol-uk.co.uk**

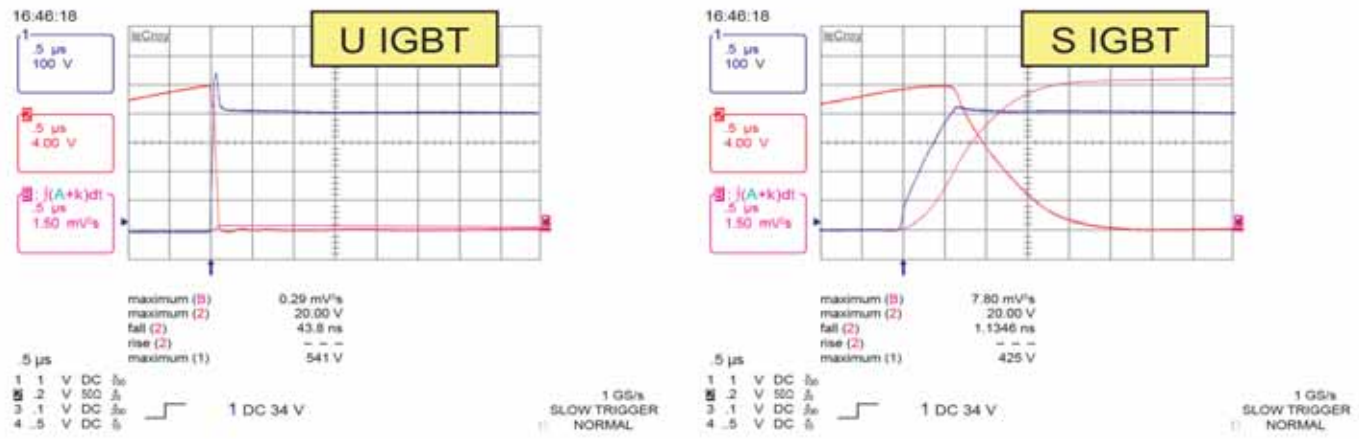

Figure 4: Turn off switching characteristics of U and S IGBTs, showing current (red, 4A/div) and voltage (blue, 100V/div)

Figure 5: Simulated power losses in neutral point clamp inverter, operating Q2/Q3 (S type IGBT) at 60Hz and Q1/Q4 (U type IGBT) at 20kHz

connected solar applications, drawing on innovations originally aimed at high-power equipment operating at high voltages. Because power semiconductors are unable to withstand direct connection to such high voltages, multi-level inverters are used to provide a high voltage at the output with the use of power switches of significantly lower blocking voltage. The multi-level topology includes a number of capacitor voltage sources which, when added together, reach the required output voltage. Several designs have been proposed, including diode-clamped, capacitor-clamped and cascade inverters.

A diode-clamped topology such as that shown in Figure 3 can be used in a grid-connected solar application. This allows the use of lower voltage IGBTs, combined with asymmetrical modulation, to minimise conduction and switching losses and thereby increase the efficiency of the inverter while also minimising harmonic content in the AC output and allowing the use of small filtering components.

Although, as with the full-bridge topology, the diode-clamped inverter has twice as many IGBTs as the half-bridge, each device is required to have only half the DC bus voltage blocking capability of a half-bridge inverter. Hence, for an inverter operating from +400Vdc and -400Vdc, devices with 600V blocking capability are sufficient. 600V devices typically have lower voltage drop and switching energy loss compared to 1200V devices, which is sufficient to deliver a net improvement in inverter efficiency.

This topology has the advantage of allowing asymmetrical modulation, as used with a full-bridge inverter but not suitable for use in a half-bridge arrangement. Hence, the inverter designer can deploy both techniques to help increase the micro-generator's overall power-conversion efficiency.

In the circuit of Figure 3, the DC bus voltage is divided by the two series-connected bulk capacitors CPLUS and CMINUS. The middle point of these capacitors can be defined as the neutral point. In the positive AC-output cycle, the forward current path for a resistive load is through Q1 and Q2. In the negative cycle, the current passes through Q3 and Q4. The freewheeling paths for a resistive load are D1 to Q2 for positive current or Q3 to D2 for negative current, respectively.

The clamping diodes D1 and D2 are the key components that distinguish this topology from a conventional half-bridge

inverter. These freewheeling paths clamp the voltage to the inverter's neutral point, hence the topology is known as the neutral point clamp inverter. D1 and D2 are typically fast-recovery diodes with 600V blocking voltage capability. The anti-parallel diodes connected to IGBTs Q1, Q2, Q3 and Q4 do not have to be fast-recovery types since their purpose is to provide a current path in case the inverter is feeding reactive loads.

IGBT Selection

With an NPC inverter, asymmetrical modulation can be applied whereby the middle two IGBTs (Q2 and Q3 of Figure 3) are operated at the fundamental frequency. For a grid-connected micro generator application this typically means 50Hz or 60Hz. At this frequency the biggest loss of the IGBT is due to conduction. Effectively, the switching loss of the IGBT can be neglected.

Standard speed IGBTs (S-type IGBT) with very low VCEon can be used for these middle position IGBTs to improve the efficiency of the NPC inverter. An S IGBT has very low VCEon but at the expense of higher turn-off energy.

The outer IGBTs are pulse-width modulated at high frequency to achieve an AC output of low harmonic content, enable the use of small output filter components and prevent audible noise. During IGBT turn off, the neutral point clamp diodes D1 or D2 provide a freewheeling path to maintain a continuous current on the output filter inductor. Ultrafast trench field stop IGBTs (U-type IGBT), which have balanced conduction and switching losses, are an ideal choice for the outer IGBTs. The U IGBT has low fall time and turn-off energy but higher VCEon than an S IGBT.

Figure 4 shows the differences in turn-off switching characteristics displayed by U and S IGBTs. This figure clearly shows the turn-off speed difference that can be exploited to achieve the lowest overall system power dissipation based on the switching frequency of the IGBT.

Efficiency Analysis

Simulation results for a 4.6kVA NPC inverter, shown in Figure 5, illustrate the benefits of using IGBTs with two different characteristics. The simulation operates the outer IGBTs at 20kHz while the inner IGBTs operate at 60Hz. A resistive load is assumed. The inverter operates from a ±400V DC power supply. The simulation analyses and calculates energy loss at each switching cycle and integrates the result to give the power dissipation.

To help understand the advantages of using the S IGBTs in the low-frequency 60Hz circuit, simulation results for U type IGBTs operated at 60Hz are also shown. Figure 6 shows the difference in power loss measured at 60Hz, comparing the U and S type IGBTs. The S IGBT, which has lower VCEon, is the most suitable for use in the Q2 and Q3 locations operating at 60Hz, compared to the U type device. This figure illustrates the benefits of using IGBTs with two different characteristics for an NPC inverter.

Although the S IGBT has a finite switching loss, even at 60Hz, the losses are very small in practice, particularly when compared to the benefit of lowering the conduction loss of Q2 and Q3 of an NPC inverter.

A further simulation compares the losses of U and S IGBTs when operated at 20kHz. Although the S IGBT has lower conduction losses compared to the U type device, the switching loss is very high. This makes the S type IGBT unsuitable for use as Q1 and Q4 switches, which are modulated at 20kHz.

Alternative Topology

The neutral point clamp inverter topology offers an alternative to the half bridge or full-bridge topologies currently in the market. This topology, evolved from successful advances at higher voltage levels, yields efficiency improvements by enabling the use of IGBTs with lower blocking voltages that have inherently lower conduction and switching losses. It also permits the use of asymmetrical modulation effectively eliminating switching losses in the low-frequency IGBTs.

Careful selection of the inner and outer IGBTs in the neutral point clamp inverter is essential to maximise the efficiency gains achieved by using this topology. ●

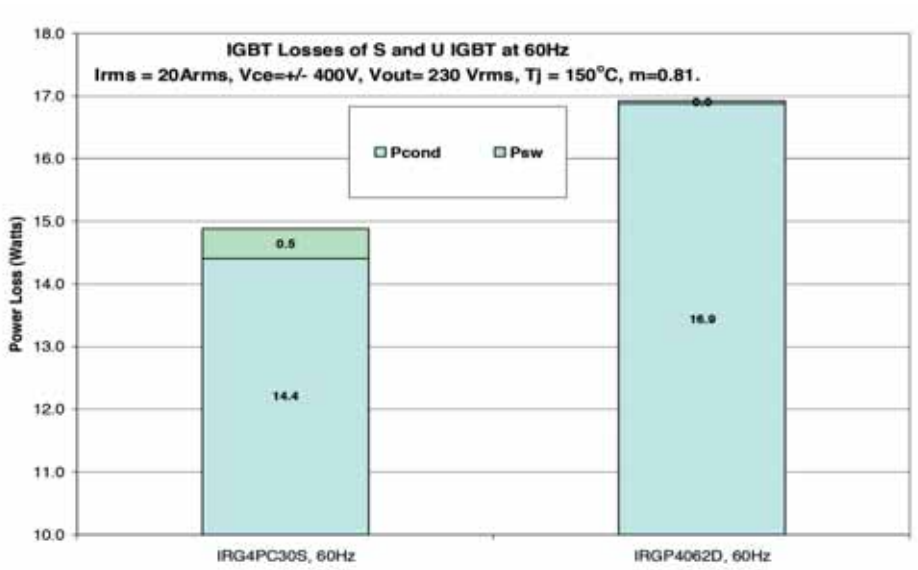

Figure 6: Power loss simulation of S and U IGBTs operating at 60Hz. S IGBT offers the lowest power dissipation at 60Hz

Electronics WORLD

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Advanced USB Battery Charging Detection with X-Chip;

New series of highly sophisticated USB controller ICs from FTDI

Find out more on pages 32 & 33

Bob Frostholm, Director of Marketing at analog ASIC firm JVD Inc based in San Jose, California, explains the needs of a true mixed-signal ASIC

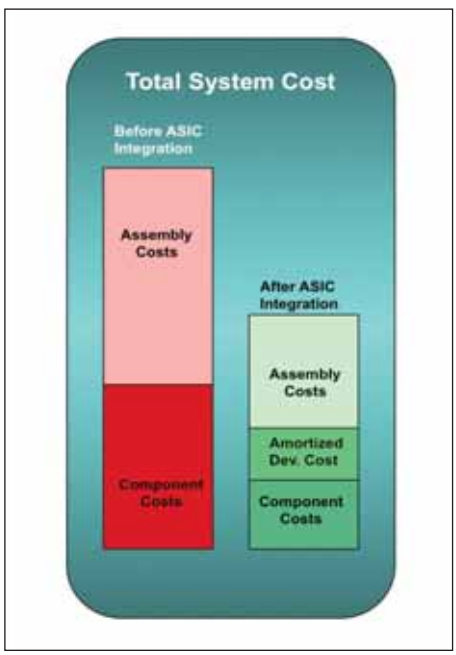
DEMYSTIFYING ANALOG AND MIXED-SIGNAL ASICs

Application Specific Integrated Circuits (ASICs) typically conjure up the notion of massively complex logic chips containing tens or hundreds of thousands (even millions) of transistors, configured to solve a customer's unique set of problems. Unlike multi-function standard product ICs such as a microcontroller that can find its way into a wide variety of applications, ASICs are designed for one specific application and, generally, for one specific product or product family.

ASICS' ORIGINS

To better understand the role and applicability of ASICs, it is important to briefly review their historical origins. The first Integrated Circuits from the early 60s contained just a few transistors and performed simple digital logic functions such as "and", "or", "nor", etc. These were called SSI devices, meaning Small-Scale Integration.

As photolithography techniques improved, more and more transistors could be built on a single sliver of silicon. Soon, chip companies were developing Medium Scale Integration "MSI" devices for logic functions like flip-flops, buffers, latches, etc (10-100 transistors). Large Scale Integration "LSI" devices (100-1,000 transistors) and eventually Very Large Scale Integration "VLSI" ICs (up to 100,000 transistors) followed, providing lower system costs and higher levels of performance. Today, of course, we have digital chips in excess of a billion transistors, thanks to advanced sub-micron lithography and the low voltage, high-speed processes upon which they are built.



"Almost 60% of the $37bn of analog ICs sold in 2010 were ASICs; yet very few mixed-signal ASIC design houses fully understand the implications of custom analog design and its applicability to analog-centric ASICs"

The first digital ASICs were built using a standard cell library consisting of fixed-height, variable-width 'tiles' containing the digital logic functions discussed above. The ability to reuse these blocks repeatedly saved time and money when designing a custom logic IC.

Analog ICs were initially comprised of a pair of matched transistors and soon expanded to include rudimentary op-amps, voltage regulators, comparators, timers and much more. Analog applications typically involve much higher voltages so these ICs needed their own unique set of manufacturing processes. More recently, market demands for smaller sizes, higher speeds and lower power consumption have forced a merging of analog and digital functionality on a single silicon chip. Cells consisting of the basic analog building blocks discussed above were created and added to the digital libraries. These analog cells were restricted to the digital fab processes developed for predominately logic applications.

Today, most ASIC companies offer some degree of analog functionality as part of their services. In many cases, the analog functions are mimicked with digital design techniques. In others, compromises to the analog functionality must be made to facilitate the use of standard library cells that are designed to yield well in the fab processes developed for high speed, high density, low-power digital designs. Often, these chips are referred to as mixed-signal ASICs or as big "D", little "A" ASICs, meaning high digital content and minimal analog content.

ASICS' CRITICAL ROLE

Analog ASICs play a critical role in our lives. Without them, none of the portable electronic devices we use in our daily lives would exist. Imagine a world without cell phones, MP3 players and navigation systems. Building them with standard products would make them prohibitively expensive and physically impossible to carry around in purses and pockets. Every automobile contains dozens of ASIC chips for everything from climate control to airbag deployment; and from suspension control to entertainment systems. ASICs also play important roles in applications for hospital medical equipment, eMeters, home appliances such as washers and dryers, scuba gear, hearing aids, and much more.

The analog ASIC market is huge. In fact,

research firm IC Insights reports that almost 60% of the nearly $37bn of analog ICs sold in 2010 were ASICs. Yet very few mixed-signal ASIC design houses fully understand the implications of custom analog design and its applicability to analog-centric ASICs.

ASICs requiring high analog content should be directed to those design houses that specialize in analog circuit design rather than those who simply select analog IP blocks from a library. Analog ASIC companies have large staffs of competent, well-experienced analog engineers with expertise in a wide range of analog functions. Table 1 offers a range of these required design skills.

Reviewing an ASIC house's patent portfolio as a quick guide to the creativity of its engineering team will serve as a first order measure of its analog expertise. Clearly, the large analog IC houses (like ADI, Linear Tech, Maxim, National, TI) have patent portfolios a mile deep. Those that also engage in analog ASIC development set high bars regarding who can access this capability and impose high minimum order requirements. For example, TI reports that its application-specific analog business focuses on a small number of large customers like Seagate, Sony, Samsung, Hitachi Global Storage Technology, Toshiba and a few others that require custom application-specific products. Minimum annual unit and or dollar volumes force the majority of the smaller customers to seek out independent analog or mixed-signal ASIC design houses.

THE MYTHS SURROUNDING ASICS

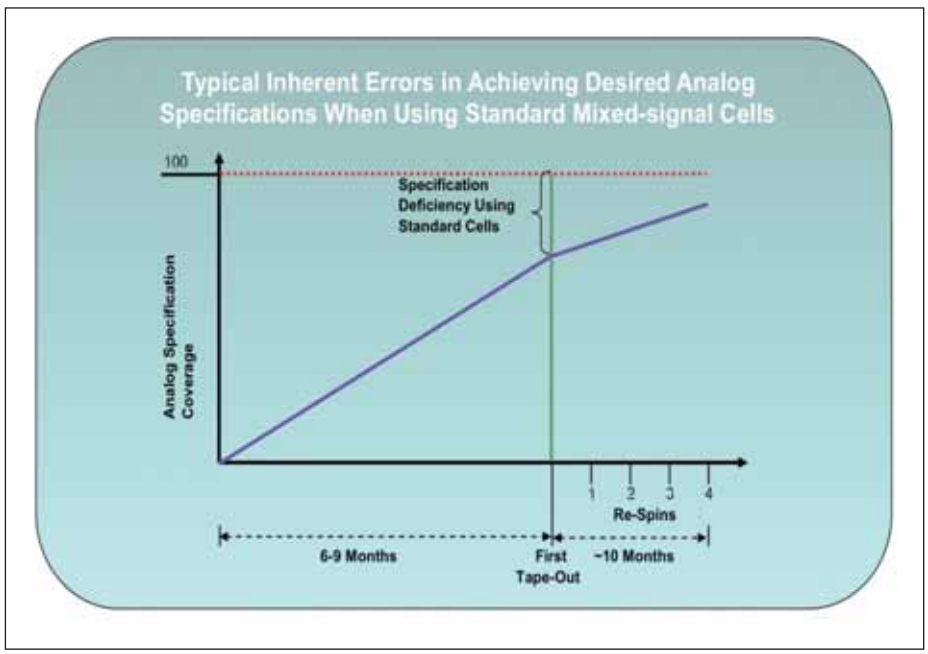
Myth #1: It is only economical to integrate analog functions into an ASIC if the analog content is minimal.

The ASIC concept began as an integration tool to lower the costs of computationally heavy logic circuits. Today, after 30-plus years, ASICs remain heavily digitally-oriented. When we hear terms like SoC (System on Chip) and reuseable IP (Intellectual Property) associated with ASICs, we often think of the massively complicated, digital-centric ASICs that may contain a few important analog functions. Historically, it is these products that have garnered the attention of the media and established a mindset among the user community that a little analog can go a long way.

But what about the applications requiring analog-centric ASICs? These are SoCs as well, even though they may not contain a microprocessor core or even memory. The medical/industrial world is rife with such requirements yet most ASIC companies are quite unprepared for the challenges of hand-crafting the unique analog circuitry required for these important applications.

The actual manufacturing cost of the ASIC chip may imply huge savings when compared to the collective costs of the ICs it replaces. However, there are other costs associated with the ASIC that must be considered and amortized over the life of the product. Non-Recurring Engineering (NRE) costs based on the complexity of the design, as well as hard tooling costs, such as masks and test hardware, can add a few pennies or dollars to the ASIC chip cost, depending on the complexity and lifetime volume of the device.

Incorporating elements into the chip that require more exotic processes for features like high currents, low noise or high frequency will increase the cost of all the elements in that chip. Therefore, it is as important to know what to incorporate into the ASIC as it is to know what should remain a discrete component. Interestingly, the use of multiple



By Graham Brown, Future Technology Devices International (FTDI)

ADVANCED IC SOLUTIONS FOR USB-BASED CHARGING

For years consumers have been forced to rely on a raft of different proprietary adaptors to charge the various portable electronics goods they own – now this is starting to change. Driven by concerns about the rising levels of e-waste, the European Commission (EC) has put legislative measures in place that mean smartphone handsets sold in Europe must forthwith be able to charge up using USB. Though this will have the upshot of greater convenience for their customers, as charging will be done via a single all encompassing interconnect, it does present certain design challenges to OEMs.

USB has always had the capacity to transfer current. Until now this was really only used to power peripherals (such as mice, keyboards, etc), which had very lower level requirements. With the prospect of it now being the primary method for providing the necessary charge to power portable devices, performance levels will need to be boosted in order to maintain the short recharge times that consumers have come to expect. With the advent of the the USB Charging Specification Version 1.2, the level of charging current supported by the interface is raised from 500 mA to 1.8 A, allowing far quicker recharge of the portable device's batteries.

The specification's high power charging option is enabled by use of a Dedicated Charging Port (DCP). Whereas a conventional USB interconnect has four shielded wires, two for data transfer (D-, D+) and two for power transfer (the VBUS connection, the GND ground connection) with a DCP the data wires are shorted together in order to make them inoperative. It is possible for portable electronics devices to identify when they are connected to a DCP, so that they know the port is fully focussed upon charging and does not deliver any Host functionality. Devices can then take advantage of the increased power offered by the DCP (up to 10W).

Figure.1 details a charging circuit compliant with the new specification. There are a large number of discretes involved in this system - leading to design, procurement and bill-of-materials difficulties. Furthermore, the microcontroller unit (MCU) has to handle DCP identification. This means that some of its processing power is being taken away from the core function which it should be concentrating on. As well as reducing system performance, charging circuits of this kind will need the engineers implementing them to deal with creating reams of complex code.

To assist OEMs producing portable devices for industrial, consumer and medical application sectors, FTDI has developed a

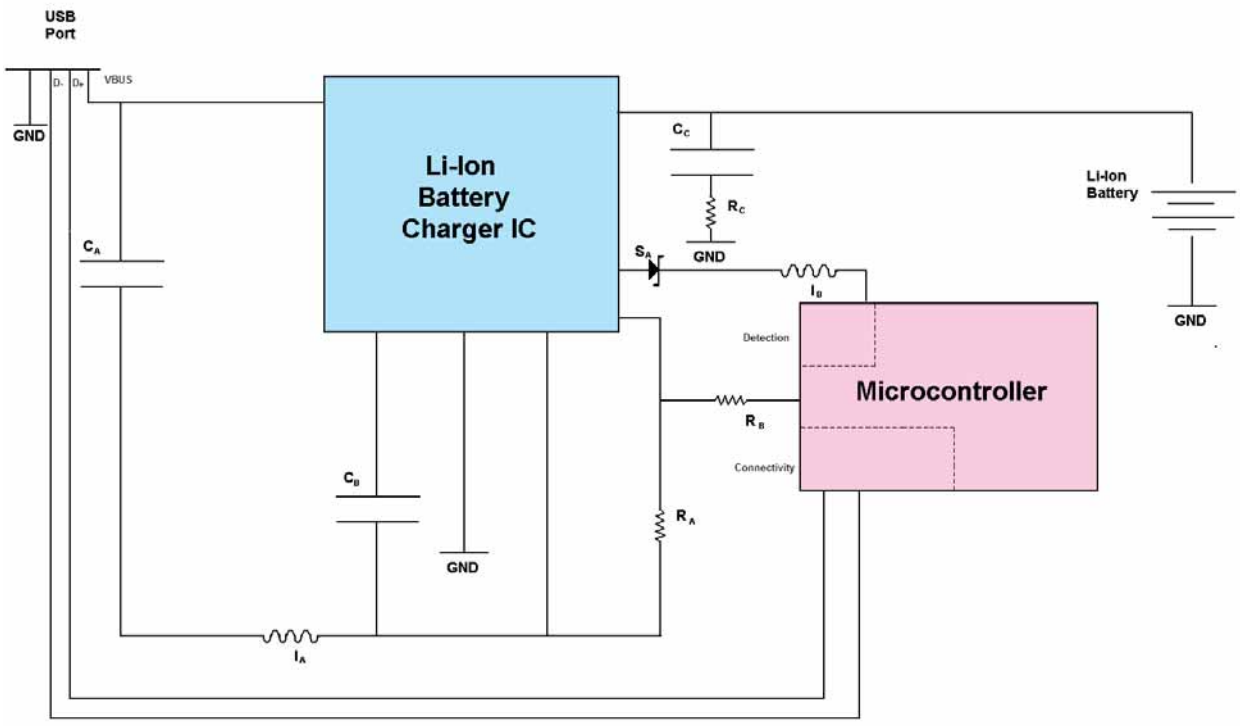


Figure 1: Conventional USB Charging Specification Version 1.2 Compliant Charging Circuit

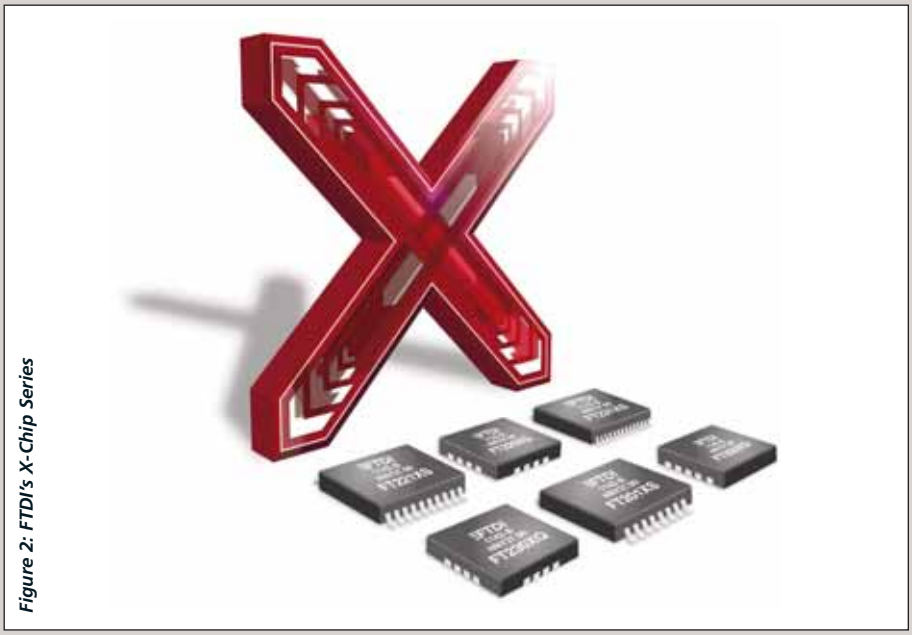


Figure 2: FTDI's X-Chip Series

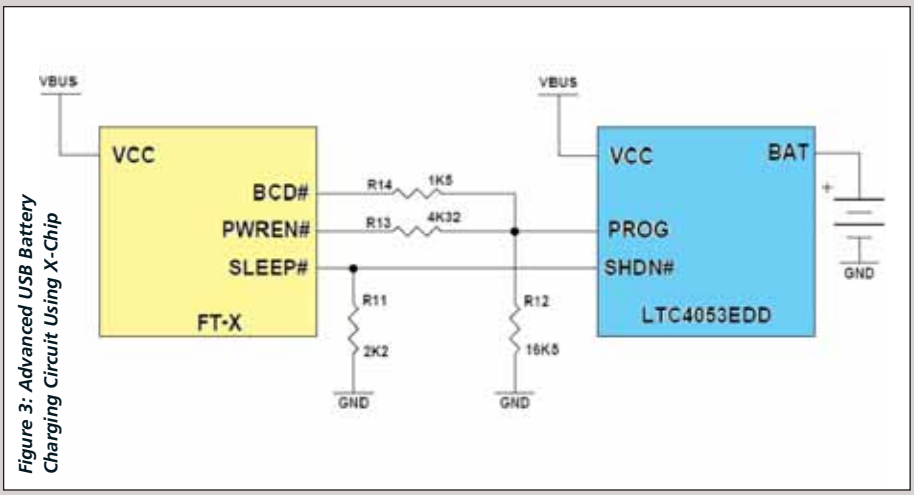


Figure 3: Advanced USB Battery Charging Circuit Using X-Chip

new series of highly sophisticated USB controller ICs. Each member of the X-Chip series integrates functionality that allows automatic detection of a DCP connection. It dispenses with the need for any of the additional software and hardware implementations that the conventional charging circuit already discussed is hampered by.

Figure.3 describes a circuit that is able to charge a battery when connected to either a USB Host port or a DCP. The X-Chip works in combination with a battery charging controller (the LTC4053 from Linear Technology is recommended). The charge rate is set by the resistance connected to the PROG pin of the battery charging controller. The CBUS pins are employed to control the charging rate of the battery depending on whether a normal USB Host port or a DCP is available, based on the current level these two options are capable of supporting. The CBUS pins are as follows:

1. BCD# - This is an open-drain active-low output signal, asserted to indicate that the X-Chip is connected to a DCP.
2. PWREN# - This is an open-drain active-low output signal, indicating that the X-Chip has been enumerated by the USB Host controller.
3. SLEEP# - This is a push-pull active-low output signal, indicating when the X-Chip has been put into USB suspend mode. It can shut down the battery charging controller when the device is powered from a USB Host and the Host has placed the X-Chip into suspend mode.

If the portable device is connected to a USB interface and it is identified as a DCP, the X-Chip asserts a signal on one of its CBUS pins to indicate this to the device.

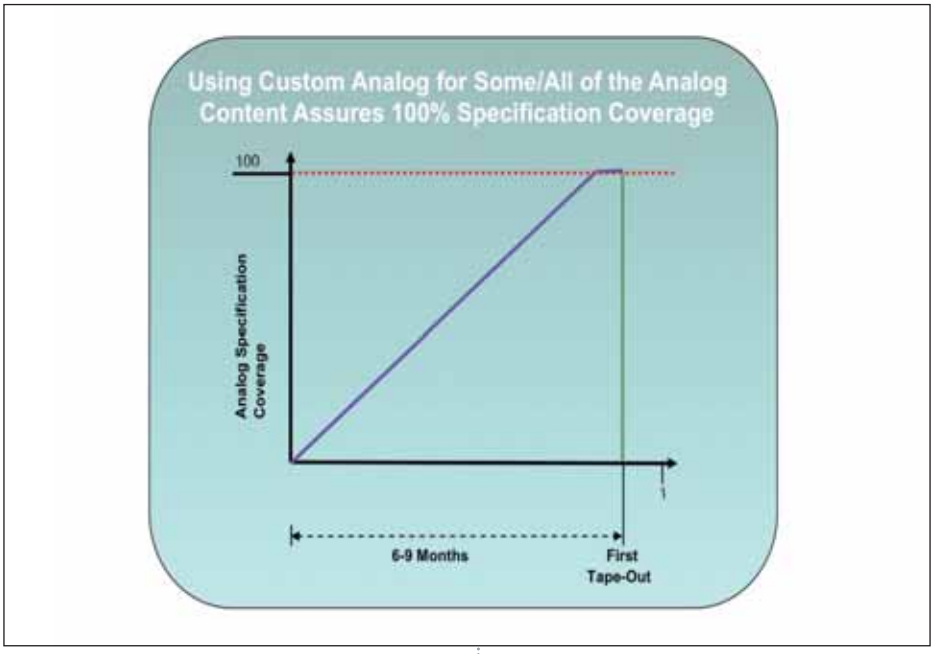
When connected to a DCP, as the D+ and D- are shorted together, there can be no transfer of data, which implies no enumeration capability. The PWREN# will indicate that the device is not connected to a normal USB Host because it is not enumerated. This allows the charging rate of the battery to be altered by the charging circuit to take into account the current level that can be supported. This results in a markedly shortened recharging period if the higher current offered by a DCP is available.

The resistors R12, R13 and R14 shown in Figure 3, set the resistance of the PROG pin on the battery charging controller. The BCD# configures the resistor network on the PROG pin to set a charging current.

The BCD#, PWREN# and SLEEP# outputs have all been designed to minimise the external circuitry required for charging applications. Normally external MOSFET devices would need to be specified to select the range (once again raising costs and system complexity). Since the X-Chip asserts its BCD# signal to indicate the detection of the DCP, resistor R14 is shorted to ground and the PROG pin of the battery charging controller will thus have a resistance of 16.5 kΩ in parallel with 1.5 kΩ to ground. This leads to a 1A charging current being initiated. If the X-Chip is connected to a normal USB Host, BCD# is not asserted and a lower charging current is applied.

The huge popularity of USB connectivity has made it very attractive as a way of charging modern portable devices. Amendments to the specification that covers USB charging will greatly increase the current levels that this interconnect can support. This will accelerate the charging times so that they are comparable with those of traditional power adaptors. Specifying a highly integrated interface IC, like the FTDI X-Chip, will make it possible for OEMs to incorporate advanced USB-based battery charging into their products while fully optimising their engineering resources, as well as curbing bill-of-materials costs and development times.

www.ftdichip.com/FT-X.htm



smaller, less complicated analog ASICs, differentiated by their manufacturing processes, can offer surprising cost-reduction results.

Most analog applications use a collection of passive elements and discrete transistors in addition to the ICs involved. Integrating as many of these components as possible to the ASIC often comes for free and can have a dramatic effect in lowering the end product's total assembly cost. It is this potential total-system cost-saving that bolsters the justification to develop the analog ASIC.

Myth #2: Mixed-signal ASIC means the same thing as analog ASIC.

Even though the term "mixed-signal" implies a combination of analog and digital circuitry on a single chip, there is a distinct difference in the skill levels required to combine library cells (analog and digital) on a silicon chip versus actually creating an analog design that uniquely satisfies all requirements of the specification. For many applications, analog library cells offer sufficient performance to meet the system requirements, However, more and more frequently, the increased sophistication of the analog application necessitates designs that are truly 'application specific' and not a compilation of general purpose analog cell blocks (see Table 2).

Like the big analog IC companies, true analog ASIC companies employ experienced analog designers who are artisans at analog invention. Many of them have spent years at the big analog companies, learning from the industry gurus.

Be careful not to let a mixed-signal design house negotiate you away from your ideal specification. Close isn't good enough – analog must be exact.

Myth #3: Only ultra-high volume applications can benefit from analog ASICs.

As noted earlier, many large semiconductor companies focus their ASIC efforts onto a handful of very large customers. Clearly, these are the privileged few and everyone else must seek out development and manufacturing partners who can and will match their needs. All full service ASIC houses have their own business criteria regarding minimum NRE, tooling and, most importantly, annual volume. Some ASIC houses avoid the issue by just offering design services and leaving the issue of manufacturing to the customer. Either way, it is often the subcontract wafer fabs rather than the ASIC companies themselves that dictate minimum annual volume restrictions.

The semiconductor industry operates in alternating cycles of boom and bust. A brief look back in time reveals that in boom times, capacity at the big Asian foundries fills quickly and all but the most promising, high-volume customers are turned away. Aggregators have somewhat mitigated the problem by combining numerous smaller company requirements under the umbrella of their larger purchasing power. However, the large Asian fabs are built to benefit from economies of scale, offering processes tailored for the mass market: high density, low-power logic.

For many, analog is problematic. Fortunately, there are many alternatives. Throughout the world and, in particular in Silicon Valley, there are numerous 'boutique' wafer fabs that specialize in analog processes and are happy to accept lower volume business. Considered a well-guarded secret by many, these fabs welcome low and moderate volume analog business and offer pricing quite competitive with the billion dollar fabs in Asia. These smaller fabs have come to realize that while analog designs are often focused on lower annual volumes, analog in general has shown to be less susceptible to the violent supply/demand curve swings inherent to the general semiconductor industry. An additional attribute is that often analog chips can sometimes remain in production for as long as ten years or more. For the fabs, accepting reduced annual volumes becomes an annuity that offers payback for years to come. Experienced analog ASIC companies have spent decades nurturing these relationships for their customers.

Myth #4: Using existing IP from analog cell libraries lowers chip cost.

Using predesigned, functional cells such as amplifiers, converters and transceivers can shorten development time and therefore has a ripple-through effect of lowering the chip's total cost. However, even though design time is reduced, there are other tradeoffs that must be considered. Standard analog library cells do not pack as neatly as digital cells. Using analog library cells can result in blocks of unused silicon on the die that will impact the yield of the wafer.

Additionally, since the analog circuitry of a mixed-signal ASIC is likely to be the input or output of the circuit, or both, these cells must be placed closer to the periphery of the chip to facilitate easy access to bonding pads.

Handcrafting some or all of the analog functions allows the designer to accomplish several things. In a mixed-signal design, handcrafted analog circuits are laid out to fill voids created when using standard digital cells, better optimizing overall silicon area utilization. Moreover, handcrafting the analog portion allows the designer to determine

precisely the performance parameters of the circuit rather than be restricted to the fixed performances of a limited number of standard cells available in the library.

The conundrum of using overdesigned cells is another consideration worthy of the designer's attention. As an example, for a given application, some analog parameters may be able to be relaxed, simplifying the handcrafted design compared to a standard cell. Alternatively, handcrafting the analog circuitry affords the designer an ability to improve other performance parameters that can have far reaching implications that make the ASIC less costly in terms of test yield and thus more competitive in the marketplace.

Myth #5: Cell-based ASIC designs ensure product differentiation.

Designing the analog portion of a mixed-signal ASIC using a cell library is tantamount to designing a system using standard, off-the-shelf, analog ICs, with one key exception – selection. At board level, there are tens of thousands of IC amplifiers, voltage references, converters and more from which to choose. In a cell library, the designer is limited to choosing from to a few of dozen amplifiers, voltage references, converters, etc. Performance compromises may be needed to accommodate these limited choices. Analog-centric ASIC development affords a perfect opportunity to rise above the competition.

As noted earlier, nearly 60% of the worldwide analog IC market is ASICs. If you and your competitors are basing your designs around the same mixed-signal cell libraries, both of you will have approximately the same performance specifications, dictated by the specifications of the library cells.

True product differentiation comes from invention. It is derived by creating uniqueness to a product not readily available to the competition. Cell libraries fail to deliver the necessary uniqueness often needed in critical analog applications.

Myth #6: Handcrafted analog is too expensive, compared to standard cells.

There is a time and place where standard analog cells are more than adequate. Experienced analog ASIC design houses recognize this and only offer full custom analog design when the need merits it.

Handcrafted analog can create the differentiation required to break out of the pack with a superior performing chip and thus a superior end-product for your customer. Additionally, stepping back from the cell library approach opens up options for manufacturing, since cell libraries are typically developed for one process at one fab. Broader use libraries are available that specify a process, for example, 0.35um CMOS, but have relaxed specifications such that they can be instantiated in multiple fabs.

Handcrafted analog creates an unlimited set of manufacturing options, especially through the use of boutique foundries. Many of the boutique fabs differentiate themselves by the variety of services they offer and their willingness to make adjustments to their processes to accommodate optimization of the chip's performance. A recent example is a circuit JVD developed for a major automotive component supplier. The chip required a high voltage MOSFET that was not available in the boutique foundry's standard process. Integration was critical to the success of the project, so the foundry and JVD worked together to create the needed device structure. The subsequent design provided the high voltage robustness needed for the application while minimizing parts count and the physical size of the end product.

> **"The medical/ industrial world is rife with requirements for these SoCs, yet most ASIC companies are unprepared for the challenges of hand-crafting the unique analog circuitry required for them"**

Non recurring engineering (NRE) costs are a compilation of several variables. These costs must be amortized over the number of chips produced during the lifetime of the product to determine their effect on the unit cost of the ASIC. When executed properly, NRE costs associated with handcrafting the analog circuitry return a disproportionately lower unit cost of the final chip. The key to success is analog design experience resident at ASIC house doing the integration.

Myth #7: The most cost-effective solution is to pack as much as possible into the mixed-signal ASIC chip.

In a recent posting on LinkedIn's Global Semiconductor Alliance GSA Networking Group discussion page, an IP Market Analyst commented on the difficulty of integrating customer-specific analog into a predominately digital design, citing the need to have three or four pre-production runs. The product, an SoC for a PalPlus TV system, missed its release date by more than a year.

This case shows the problem clearly. Insufficient analog expertise can get a mixed-signal ASIC house and its customers into a real bind. Missing a product launch window by a year or more is the kiss of death. When the analog component of the design is critical (for example, more than a basic A/D or DAC), it's best to seek out analog ASIC experts to perform the integration.

Moreover, splitting the functions into multiple chips should be considered when both the analog and digital contents are excessive. The fact remains, analog circuits perform better in non-digital fab processes. When possible (from a cost/yield/board space perspective) the long-term cost benefits of a dedicated analog ASIC chip can be overwhelming.

DETERMINING THE RIGHT COMBINATION

The application will always determine the appropriate combinations of technologies that are best suited for the ASIC design. As our dependence on cognitive prosthesis devices (smartphones, Wii controllers, tablet PCs, etc.) increases, copper tethers disappear and analog increases its dominance in ASIC designs. MEMS advances have placed Star Trek style sensors in our daily lives. Medical imaging, sensing and monitoring continue to improve our daily lives. All of these and more increasingly rely upon better, faster, denser analog circuit content.

When considering a new ASIC design, carefully consider the role analog will play in its deployment. To minimize risk, choose your ASIC development partner carefully. Most of the time, mixed-signal ASIC design skills will be sufficient. To minimize risk, seek out an analog ASIC partner with the right analog design skills and experience to match the application. ●

This article presents a study of variability-aware design methodology that allows designers to lower the risks of silicon failure and to improve their design margins and flows. Supplied by a group of researchers and engineers at CSR, the University of Southampton and Cadence Design Systems

MANAGING VARIABILITY IN 40NM AND 28NM DESIGNS

IC design houses these days must survive and thrive in very competitive markets. This can only be done through product differentiation. But how to accomplish differentiation, given that silicon and standard cell libraries have become commodities? Increasingly the differentiation is coming from design flows and the way they manage challenges such as variability. Timing and power variability are becoming more significant at each new process node and they impact margins, silicon utilization, silicon failure and the time it takes to close timing.

This article presents a variability-aware design methodology that allows designers to lower the risks of silicon failure and to improve their design margins and flows. Specifically, the article reports a study by Cambridge Silicon Radio and the University of Southampton that investigated the effect of layout context on variability in performance and power in standard 40nm and 28nm libraries. The article evaluates various mitigation strategies that can be applied to predict and minimize the effects of systematic variability.

At 40nm and below, variability cannot be analyzed by simply considering devices in isolation. Both lithographic effects and stress have significant impacts on device behavior. Consequently, the context of a cell – what is located near to it in the chip layout – has to be considered. The study reported here primarily focuses on analyzing the cells used to build the clock tree. In this study we use "context" to mean those cells that lie on all sides of the cell under analysis – not the cell itself. We also looked at the impact of the context on the delay of critical paths.

> **"Compressive stress will improve the performance of PMOS devices, while tensile stress will improve the performance of NMOS devices"**

STRESS EFFECTS

Mechanical stress is a major source of variability at 40nm and below. Stress itself is not the issue – the variability induced by stress is the problem. Stress affects carrier mobility, saturation velocity and threshold voltage (Vth). As a result, stress affects the performance and timing of a circuit.

Stress is often intentionally induced to increase electron or hole mobility and, thus, boost transistor performance. Stress liners are often used to create compressive stress on top of PMOS devices and tensile stress on top of NMOS devices. Compressive stress will improve the performance of PMOS devices, while tensile stress will improve the performance of NMOS devices.

Stress is also unintentionally and non-uniformly induced through various process steps, especially shallow trench isolation (STI). The width and thickness of the STI, which generally becomes compressive after processing, determines how much stress is applied. STI-induced stress can change IC drive current, either improving it or degrading it, by as much as 10%. Since it is compressive, wider STI will increase PMOS performance and degrade NMOS performance, while narrower STI will have the opposite effect.

Another proximity effect that is typically modeled along with stress is well proximity effect (WPE). WPE impacts mobility and threshold voltage, and it has a proximity effect that impacts the stress liner. All these effects are layout dependent and have a combined effect on the device performance.

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VARIABILITY CASE STUDY

We used commercial 40nm and 28nm cell libraries for our study. We first generated a baseline context for each of the clock tree cells, using the same baseline context for each cell under analysis. We then generated a large number of random contexts, allowing any

Table 1: Device variations

Process	Max Vth	Max Idsat	Max Ioff
40nm	3.3%	9%	24.2%
28nm	3.91%	11.5%	2.18%

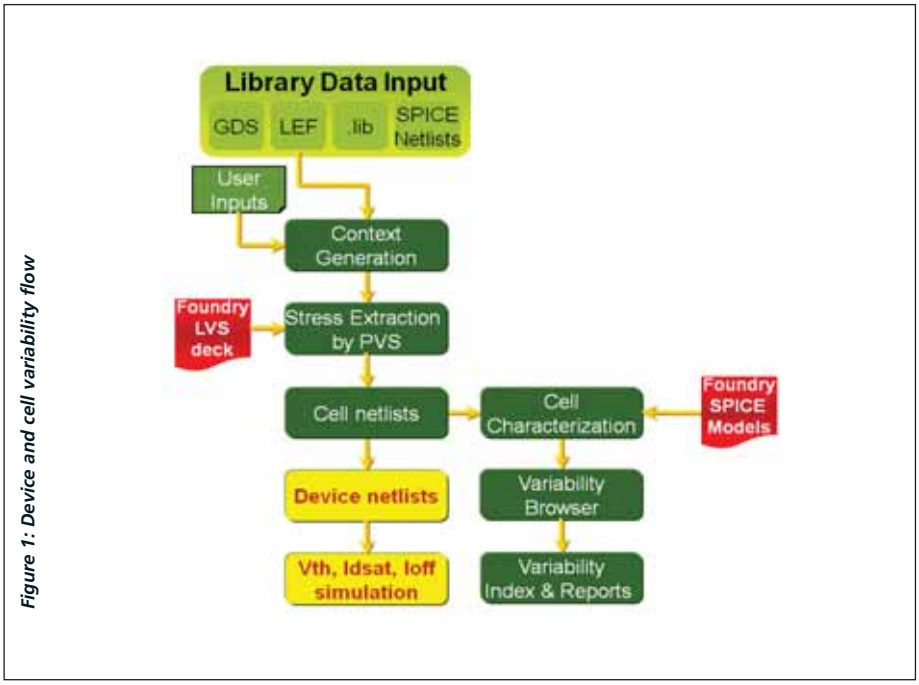


Figure 1: Device and cell variability flow

cells from the library to be placed around the cell under analysis.

We used the Cadence Litho Electrical Analyzer (LEA) to build the variability analysis flow shown in Figure 1. We used this flow in both the baseline and random cases to automatically generate the context, extract the stress effects of each context, quantify the delay and leakage variability, and compile variability reports. We extracted the device netlists from the cell libraries and simulated the electrical characteristics for device-level analysis. Furthermore, in the 40nm library, we included regions of dummy diffusion in the cell library in an attempt to standardize the context effects.

We modified the cell layouts in the library to determine whether these efforts are effective. In addition to library variability analysis, we ran a post-route stress variability analysis with Cadence LEA as shown in Figure 2. With such an analysis, chip designers can analyze critical paths that might be especially sensitive to proximity effects and optimize those critical paths to reduce sensitivity to variations.

ANALYSIS RESULTS

To run the analysis, we used Cadence LEA context generation and stress extraction to create cell netlists for different contexts. We then simulated the discrete device characteristics, looking at primary MOS device electrical characteristics such as voltage threshold (Vth), the saturation driving current (Idsat) and the leakage current (Ioff). By simulating the same device under all the different context cases, we could calculate the device-level variability due to stress. The variability at both device and cell level resulted from the variations of stress-related transistor parameters. We first conducted these experiments for a commercial 40nm standard cell library and repeated the same experiments for 28nm.

Table 1 shows the results of this experiment. It shows that device electrical characteristics including Vth, Idsat and Ioff are affected significantly by layout-dependent effects. The Vth spreads of n-MOSFETs are up to ~16mV and more than 3% for 40nm and 28nm technologies, resulting in more variability of Idsat and Ioff, especially Ioff at the 40nm node. p-MOSFETs show a similar scale of context dependent variability as n-MOSFETs at 40nm, but smaller variability is found at the 28nm technology node.

We focused our cell library study on the timing and leakage variability of clock tree cells due to stress. The cells were placed by Cadence LEA with top and bottom contexts of filler cells, and with left and right contexts of cells randomly selected from the library. The cells were characterized at the worst corner and lowest temperature.

We characterized cell performance at different combinations of input rising/falling slew and loading capacitance. The values were extracted from the input cell library (.lib). We obtained the maximum delay and output slew spreads from this extraction. The leakage was characterized at combinations of low and high inputs at the

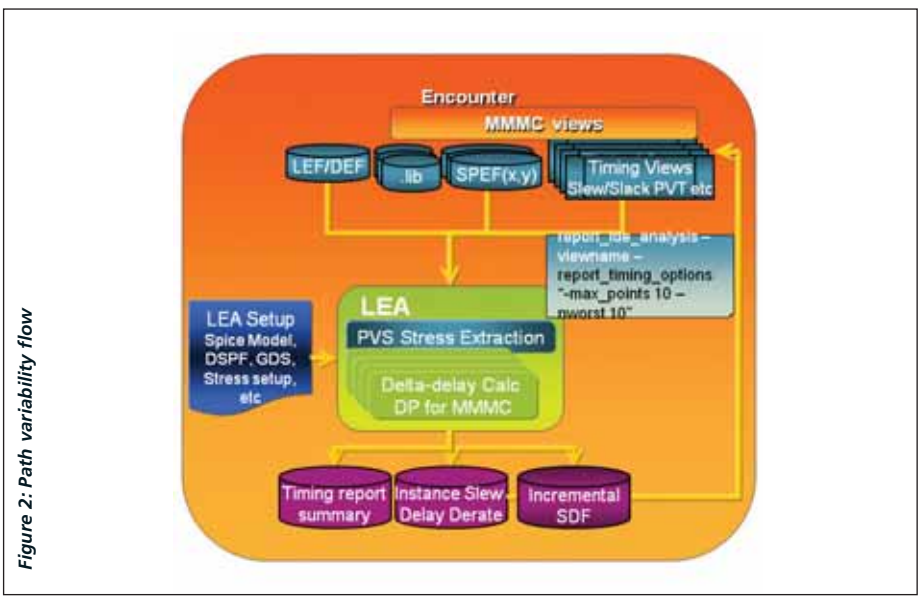


Figure 2: Path variability flow

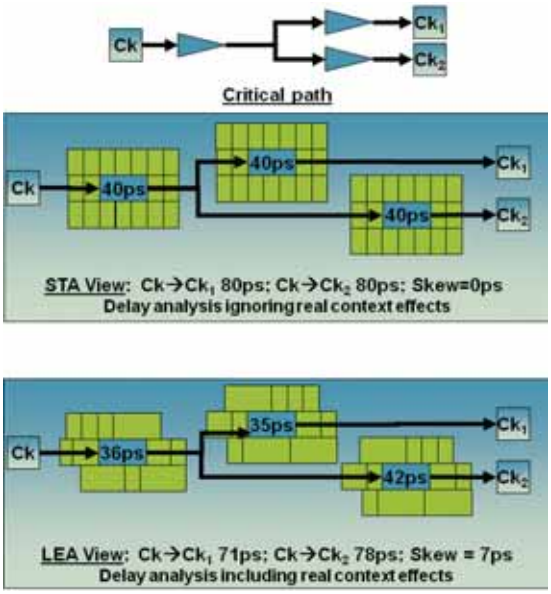


Figure 3: Cadence LEA critical path analysis

"We analyzed the context-induced variability of the critical paths of a 40nm IP block consisting of around one million instances; it had about 100 different types of cells and we analyzed the top 66 critical paths"

input terminals, and the maximum leakage spread was found. Therefore, the variability in Table 1 comes from different conditions of input slew, loading capacitance and input voltage for different cells. At 40nm, the worst delay variation due to the context of the clock buffer is 15.39% and the worst leakage is 30.48%.

To check path variability, we analyzed the context-induced variability of the critical paths of a 40nm IP block consisting of around one million instances. It had about 100 different types of cells and we analyzed the top 66 critical paths. Cadence LEA extracted all 492 instances that belonged to these paths with their contexts, for a total of 3,175 instances. As illustrated by Figure 3, Cadence LEA then calculated the delay variation due to context and updated the timing report accordingly. Initial results showed delay variations of up to 86ps or almost 5%.

MITIGATION STRATEGIES

Layout-dependent stress affects the most devices located near the border of a cell. This means that smaller cells demonstrate higher variability and bigger cells have lower variability. We also found that the top and bottom context cells have a negligible effect on cell variability, confirming that the relative systematic variability of bigger cells should be less.

We also looked at the mitigation strategies for the different stress effects and came up with some observations and suggestions. With diffusion spacing, for instance, we noted that dummy diffusion in the vertical direction may reduce variability but it increases area and power consumption. Our suggestion is to try to remove dummy diffusion if the layout-dependent systematic variability has not become worse.

Another observation is that smaller vertical diffusion spacing enhances NMOS driving current, but reduces PMOS driving current. Our suggestion is to place the top context cells a little further from and the bottom context cells a little nearer to the selected cell. Finally, we observed that smaller horizontal diffusion spacing benefits device performance. Our suggestion is to place right and left context cells as close as possible to the selected cell.

With WPE, we observed that the smaller the distance from gate to well edges, the higher the WPE on the device. Thus the physical parameters should be larger to minimize WPE. Our suggestion is to keep the top context cells far from the cell, and not to let the bottom context cells get too close. Try to use bigger cells as the left and right contexts.

Finally, we observed that variability is not affected by removing dummy poly, so there is no suggestion to do so.

UNDERSTANDING VARIABILITY

To improve our understanding of variability and develop a more effective design methodology, we used the Cadence LEA software to study context-dependent variability for devices, cells and paths at 40nm and 28nm. To quantify the stress effects on device and cell variability, the cells of interest were surrounded by context cells selected randomly from the cell library. Then, the device and cell netlist were extracted for variability analysis.

We analyzed cell performance and leakage variability due to stress. We found that the smaller cells have significant context-dependent variability while bigger cells are more immune to its kind. This is because layout-dependent stress has its greatest effect on devices located near the borders of a cell.

Finally, by analyzing the physical sources and properties of layout-dependent effects, we developed suggested strategies for mitigating layout dependent variability of 40nm and 28nm CMOS cells, as presented in this article. By analyzing and mitigating variability in this fashion, design teams can have better control over margins, fewer silicon re-spins, more predictability, faster turnaround times and more differentiation in the end products they produce. ●

COMBINED SOLAR PANEL AND COIN BATTERY DUAL-POWER SUPPLY SOLUTIONS

DUAL-POWER SUPPLIES CONSISTING OF SOLAR PANELS AND SMALL-SIZED BATTERIES CAN NOW BE EASILY USED IN PORTABLE DEVICES, SAYS **RAIMUND WAGNER**, PRODUCT MANAGER FOR ROHM SEMICONDUCTOR EUROPE

The interest in using solar energy as additional power source is increasing, especially in the area of small-sized electronics that normally rely on small coin cell batteries for power.

Energy generation by solar panels has been already adopted as a power source in some small-device applications, such as wristwatches and pocket calculators, to extend the life of the batteries or substitute them if needed. However, in terms of development costs and number of system components, these solutions have proven to be challenging, as they require specific electronics systems that combine the solar panels and batteries, but also including safety features and voltage control.

New methods for easy implementation of such functionalities are very much needed so that solar energy use can be widely expanded in the market. In order to realize this, some requirements have to be met, such as having high-precision voltage at ultra-low current consumption and effective power supply switching at low impedance.

For further cost reduction, easy integration of dual-power supplies and short time-to-market processes are also desirable. Controlling the dual-power sources (solar panel and battery) independently facilitates reliable functionality, whilst eliminating the need for software or additional components. In response to these demands, LAPIS Semiconductor, a member of the ROHM

Group, has developed a power-controlling IC series that implements a dual-power supply and all the functions necessary to realize reliable solar-energy driven applications.

Required Safety Functions

Driving a microcomputer and peripherals by battery and solar power generation has to be implemented in a highly efficient way. Although this extends the life of the battery, many monitoring functions are needed to ensure proper operation of the system.

It's possible to build a dual solar-based power supply by using standard primary batteries or rechargeable secondary batteries. For both configurations the state of the battery and solar panel needs to be constantly monitored to verify the driving conditions of the system.

When using standard primary battery, there has to be a prevention function to protect it from any current backflow from the solar panel. In addition, the voltage provided to the external components has to be monitored and stabilized by a regulator, to prevent unstable power supply conditions.

If rechargeable batteries are used, there must be continuous monitoring of their status and, in case an overcharge voltage is detected, the charging of the battery has to stop immediately. If low voltage is detected, the power supply has to be stopped to prevent overdriving the microcomputer. For optimum power efficiency, the quiescent consumption current of the control IC needs to be kept low too.

Reliable Dual Power-Supply Control

LAPIS Semiconductor, a subsidiary of the ROHM Group, has developed the ML9077/ML9078 LSI families for small-sized electronics that rely on small capacity batteries. These products drive a microcomputer and its peripherals whilst charging the battery from a solar panel, or they can switch the supply sources between the solar panel and the primary battery, all automatically while saving power and providing the required safety.

The concept is based on the use of two alternating LSIs. ML9077 automatically controls recharging and switching of the power source if a solar panel is used in combination with a rechargeable battery. It monitors the power supply from the secondary battery and controls the voltage to prevent overcharging.

When the voltage of the rechargeable battery becomes lower than the selected limit (1.8V or 1.1V), the power pin for external microcontroller (VDO) will be open (no power is supplied), and when the voltage of the rechargeable battery rises again above those limits, the ML9077 restarts supplying power to the MCU. Thus, reckless driving of the microcomputer at low voltage can be prevented.

The rechargeable control circuit continuously compares the voltage of the rechargeable battery (VBAT) to that of the solar cell (VSC). It continues recharging when VSC is larger than VBAT and stops recharging when the VSC equals VBAT or below. The overcharge prevention circuit switches off the current of the solar cell when it detects that the voltage of the rechargeable battery meets the defined voltage level. The ML9077 supports rechargeable batteries which require a charging voltage in the range of 3.2V to 2.5V. These could be Lithium Manganese Dioxide [ML] batteries (charging voltage 3.1V) or Cobalt Titanium Lithium [CTL] batteries (charging voltage 2.6V). Consequently the ML9077 is designed by using an ultra-low power, low leakage process which reduces the power consumption of the device itself to only 80nA.

A typical discrete solution without ML9077 requires eight components for the recharge control, overcharge prevention and low voltage detection. This includes comparators analysing the reference voltage and switches. Using a set-up with ML9077 as described here requires only one component (see Figure 1); which means that the mounting space on the PCB can be reduced drastically and the power consumption can be reduced from 3µA to 0.08µA for the same function.

ML9078

The second device in the series is ML9078, which continuously compares the voltage of the connected solar panel and the voltage of the primary battery. The device makes an automatic selection and uses the higher voltage as power supply for the microcomputer and the peripheral electronics. A real-time monitoring is available to check if the solar battery or the primary battery are in use.

As the solar panel and primary battery voltages are continuously monitored, the connection from the primary battery can be automatically blocked when the solar panel voltage becomes higher than that of the primary battery, preventing current backflow from the solar panel to the primary battery. With it, the primary battery can be

Figure 1: Comparison of a solution with and without ML9077

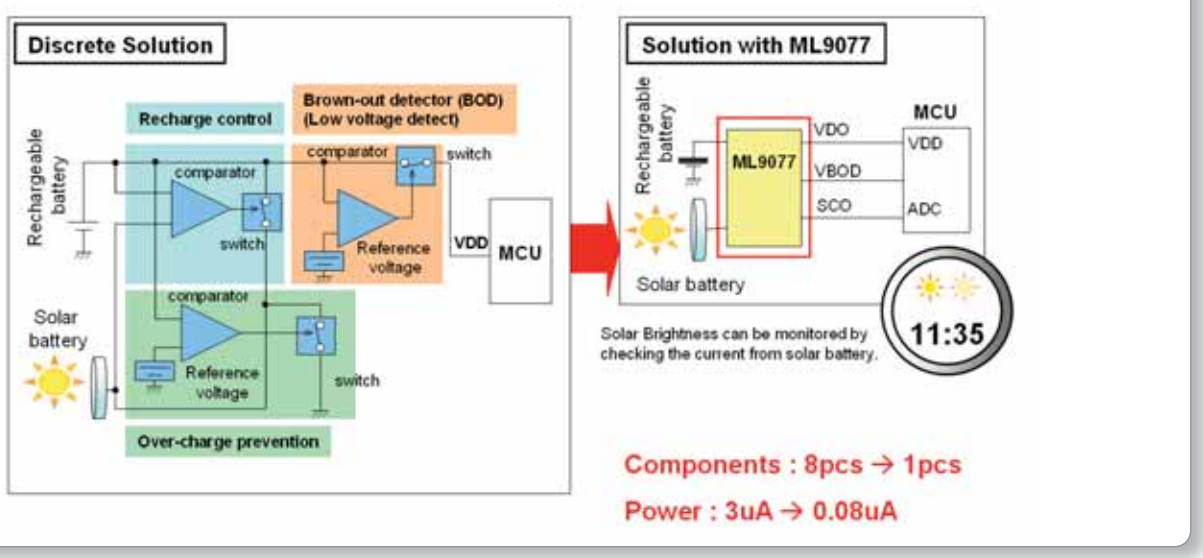
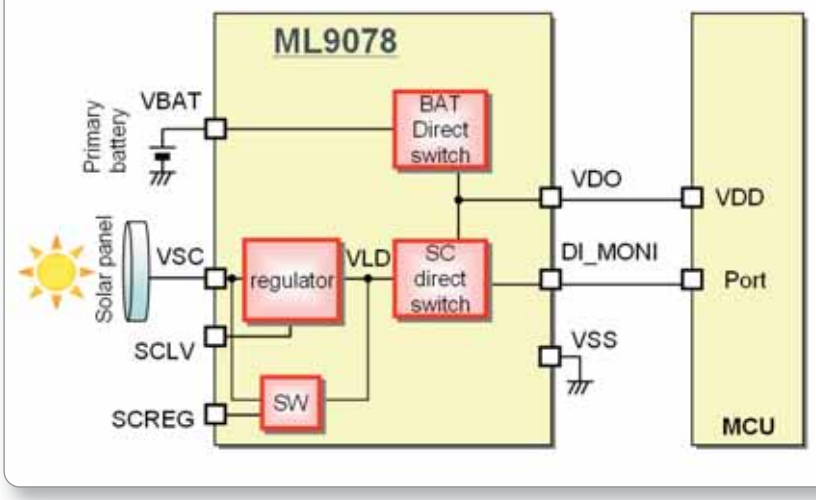


Figure 2: ML9078 – solar power, primary battery control LSI



protected from desctruction. The microcontroller will also be protected as voltage exceeding the limit will not be supplied to it.

Depending on the type of application, an additional internal regulator can be used to adjust the VDO voltage output. Since the voltage range generated by the solar panel is dependent of its components and specification, it has to be determined on a case-by-case basis if a regulator should be used. For instance, four-cell amorphous silicon solar panels typically provide a voltage range of 3.2V to 2.0V, depending on the luminosity of their light source or the size of the panels, and 3V lithium coin batteries also typically provide 3.2V to 2.0V. In such cases the internal regulator can be switched off, as it will not be needed to down-convert the VSC voltage. Solar panel power continues to be supplied to the VDO, as long as the VSC is higher than VBAT.

The voltage regulator can provide voltages in the range of 1.65V to 3.3V in case of ML9078-001 or 1.5V to 3.0V in case of ML9078-002. No internal regulator is available for ML9078-00, which means that VDO is always equal to VBAT or VSC. For efficient operation, the quiescent current of the device operating at 25degC is 80nA or less for ML9078-001/ML9078-002 and 160nA or less for ML9078-003.

When implementing ML9078 the original component count of a discrete solution can be reduced from four to one as no switches, inverter or comparator are required. Power can be reduced from 1µA to 0.08µA while keeping the same function level. The designs become easier, costs go down and development time shortens. Additionally, the device enables the product to display an "eco" icon by monitoring a signal which indicates the power source is in use and consumes very little itself, also using solar power and thus extending the lifetime of the primary battery.

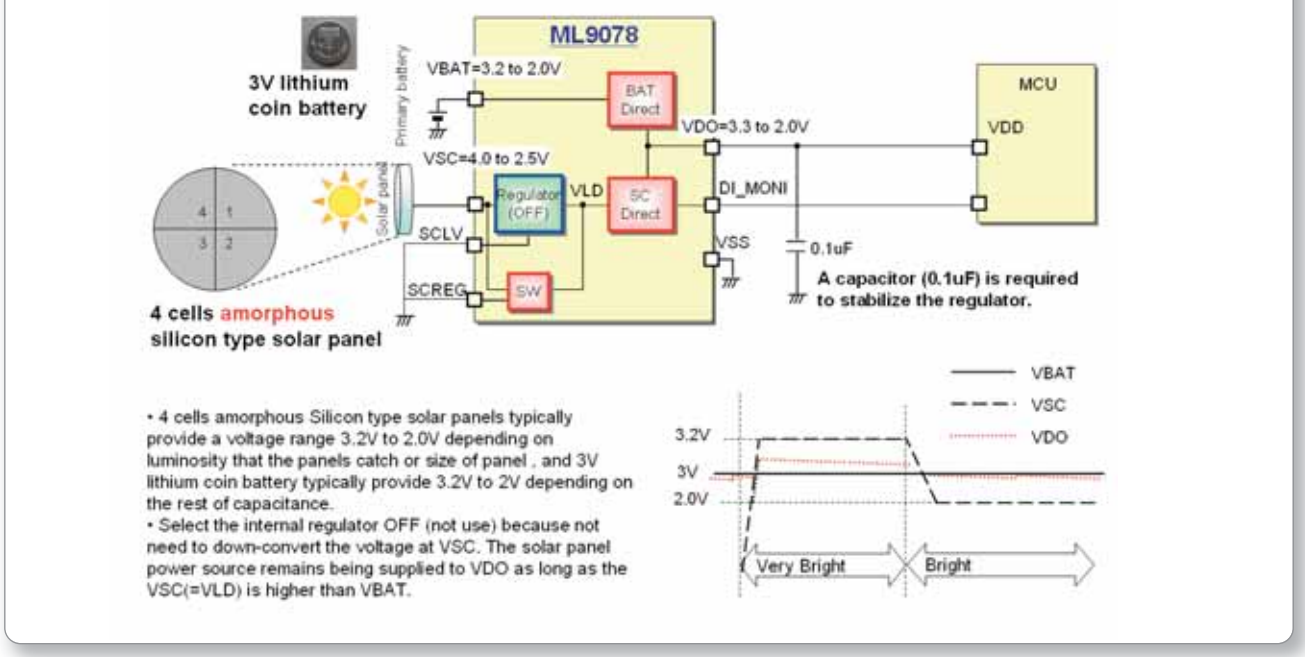
'Eco' Applications

With these new LSIs, ROHM Semiconductor is the first in the industry to introduce ideal solutions for the integration of dual-power supplies combinations of solar panels and batteries. They can be used in any type of low power 'eco' application, like wristwatches, e-book readers, standing clocks, pocket calculators, bicycle meters, remote controllers, lights, radios, portable toys, battery chargers and so on.

Key features are the automated switching, integrated protection functions, as well as the ultra-low current consumption and high reliability. These devices contribute to the miniaturization of end products; since the size of the WQFN package is only 3mm x 3mm.

For fast design-in, evaluation boards are available as well several configurations which allow easy testing of different battery and solar cell options. ●

Figure 3: Application example



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QUALIFICATION AND VERIFICATION CONSIDERATIONS FOR DIGITAL POWER SUPPLIES

PATRICK LE FÈVRE, MARKETING AND COMMUNICATIONS DIRECTOR AT ERICSSON POWER MODULES, CONSIDERS THE QUALITY ASSURANCE AND VERIFICATION ISSUES IN THE MOVE TO DIGITAL POWER TECHNOLOGIES FOR ON-BOARD DC/DC CONVERTER MODULES USED IN INFORMATION AND COMMUNICATIONS TECHNOLOGY (ICT) EQUIPMENT

Digitally-controlled and managed power supplies represent a rapidly growing part of the power conversion industry, especially in telecom and datacom markets. This is an exciting and dynamic part of the market as it offers many advantages over the conventional, analog-based, control methodologies.

The hardware and system impacts of digital power are well discussed, but this highly configurable approach to power supplies has other impacts both to suppliers of power hardware and to their OEM customers. One impact is the quality assurance process, which faces new challenges with the introduction of digital power supplies.

A conventional power converter or regulator with an analog control system is 'hard wired' to perform to a set of specifications, and the normal quality control processes are designed for this environment. With digital power, the converters and regulators are highly configurable via software, resulting in an almost infinite number of possible performance attributes. Some of the quality assurance issues that arise from this change include management of software levels, verification of memory operation internal to power supplies, sourcing of critical digital control components, more complex verification testing, lifetime and reliability implications, software upgrade procedures and failure analysis.

Digital Control

A comparison of the differences between analog and digital control is shown in Figure 1. Much of the content internal to the converter remains essentially unchanged when going from analog to digital control. Examples are input and output filtering, magnetics and power semiconductors.

The primary impact of digital control is in the control/feedback loop of the power supply. The analog control chip is removed and replaced by a microcontroller (MCU), memory support and an interface bus for communication outside the power supply. Control algorithms for the power supply are contained in software, loaded into the internal memory.

This approach provides several benefits including: higher efficiency; higher packaging density; increased configurability; fewer hardware part numbers; field configurability and upgradeability; and faster system time-to-market.

Digital control also raises risks or potential concerns from a quality assurance perspective, including:

- How are the logistics managed, with almost infinite configurability?
- The new software component must be verified and qualified.
- The internal memory must be extremely reliable, so how can it be verified that no data is lost?
- How is the operation configuration of the power supply achieved during manufacturing testing?

Software

From an operational point-of-view, the biggest difference between analog and digital control is the added component of software that provides many benefits for the developers and users of digital power products, but it also adds complications to the qualification, manufacturing and logistical support processes.

MCUs used in digital power products are supported with onboard non-volatile memory, used to store the basic firmware that allows boot-up and operation of the MCU. Clearly the robustness of this data is critical to the operation of the converter or regulator. This basic firmware tends to be relatively stable in regard to change activity for any given hardware implementation of the MCU. This firmware is loaded into the MCU non-volatile memory during the manufacturing process of the MCU.

> MCU and memory are highly complex, small-geometry ICs that are critical to the operation of the power supply, and are located in close proximity to the large currents and fields resident within a switching power supply. Their robustness in such an environment must be carefully verified so that data integrity is not compromised

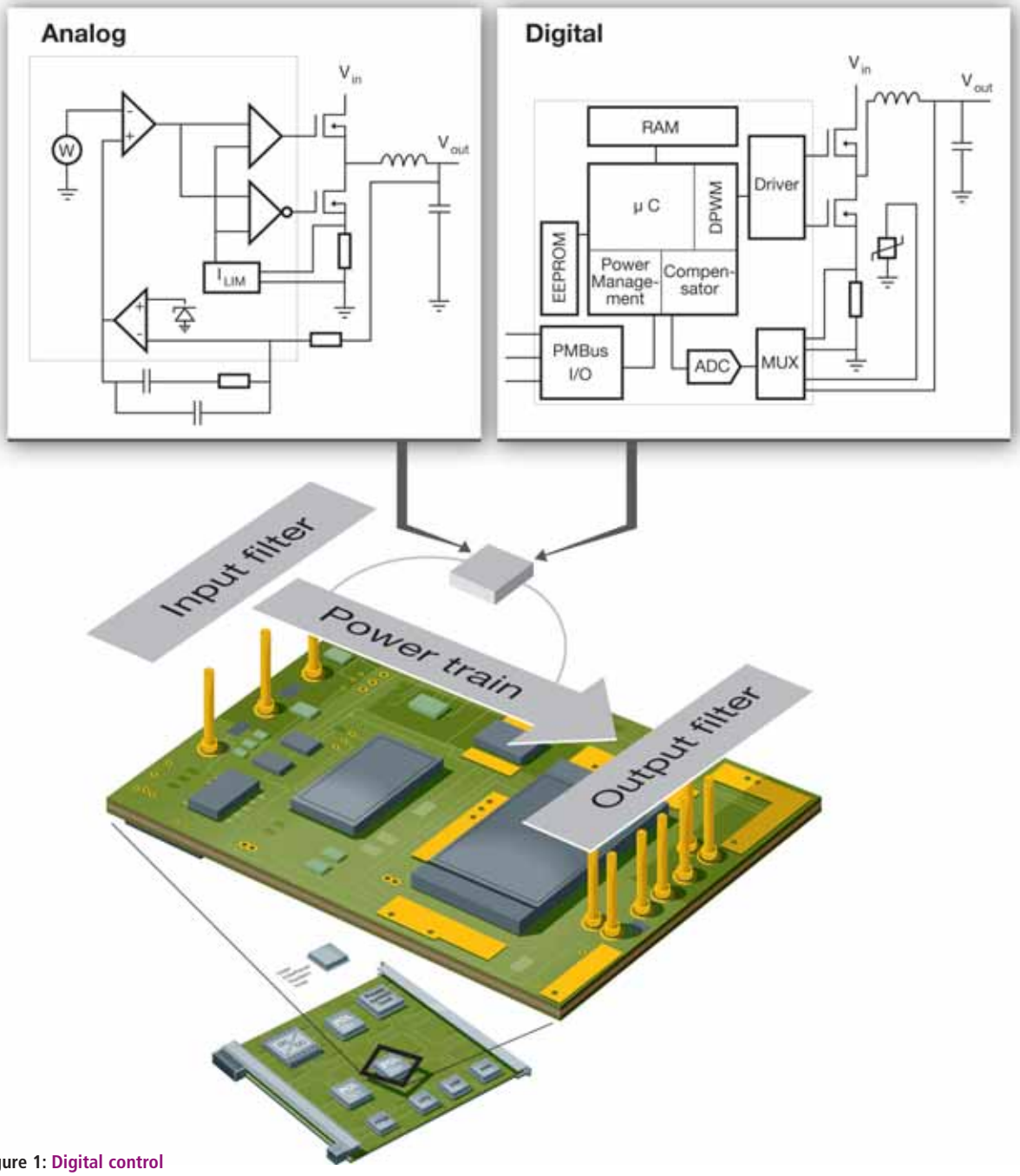


Figure 1: Digital control

The more interesting and flexible software in a digitally-controlled power supply is the application programming. This code contains operating parameters for the power supply's feedback control loop, settings for output voltage, fault detector limits, error-handling routines and sequencing information. Each digital power supply is capable of operation over a broad range of parameters.

During the manufacturing process of a standard digital power supply, default settings are defined, entered and verified before product shipment. In addition, several other representative settings must be tested to ensure that the power supply will operate reliably over its intended range of functionality.

A further complication is that the OEM can do some part of the application programming. Thus the software and the processes for its control and quality assurance must address usage during manufacturing and by the customer during product development and field deployment.

Quality Assurance Implications

The quality assurance implications of digital power must extend through all stages of manufacturing processes from the sourcing of raw materials through field support activities, see Figure 2.

A high degree of emphasis on quality must be placed in all of the material sourcing. In the case of digital power, the biggest new challenge will be the management of the MCU device, both from a sourcing security point-of-view and in terms of managing the included

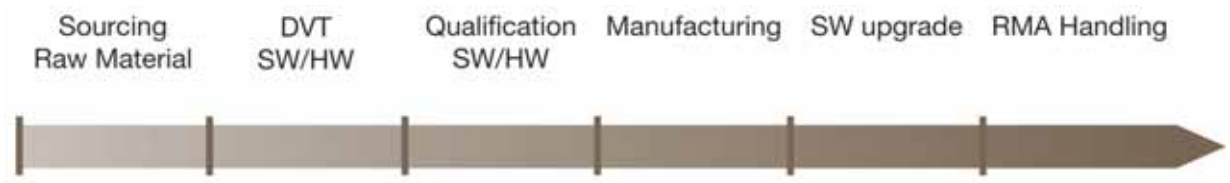


Figure2: Quality assurance process

firmware. Digital MCU chips intended for power supply applications tend to be relatively few in number. They are also highly complex devices and usually with no standardization from supplier to supplier. Consequently, second sourcing is often not an option and therefore serious consideration must be made for 'secure sourcing'. The chip provider should have two or more manufacturing sources, and regularly ship products from them to ensure equivalency and to minimize start-up problems at any manufacturing site.

There should be very close contact and substantial dialog between the manufacturer and the suppliers of the MCU chips used in digitally-controlled power supplies. The following provisions will be necessary:

- Two or more equivalent manufacturing sites for MCU chips;
- Inclusion of a very robust non-volatile memory and communication interface;
- Built-in fault detection and diagnostic capability of the digital functionality;
- Extended quality testing during the IC design and manufacturing processes;
- Insurance of level control for firmware loaded during IC manufacturing;
- Thorough control of logistics flow during IC manufacturing and shipment.

Design Verification Testing (DVT)

Design Verification Testing (DVT) is done near the end of a product's design cycle for the purpose of ensuring that the product, as designed, meets all its requirements and specifications. Both functionality and performance must be verified.

With digital power, DVT will also apply to the software content of the product. An analog product has a few well-defined 'corners' of its specification space. For example, the parameters of output voltage, output current and temperature might be the key elements of the specification for an analog power supply. These three parameters define a three dimensional space such as a cube. By making measurements at each of the eight corners of the cube, operation of the product can be ensured over the entire operational ranges of the three parameters.

The situation is entirely different with digital power. Because the software is highly configurable and can control dozens of individual parameters, the number of possible combinations is essentially infinite, and the number of 'corners' expands exponentially.

In essence, the software makes it possible to define an almost infinite number of 'products', not just one. Ericsson, for example, addresses this problem by using an intelligent DVT process. The concept of an intelligent DVT is to define software for multiple platform implementations spanning the expected applications for the power supply. Each of these implementations will include specification of the external functionality of the product such as output voltage and fault monitoring/handling behavior. Each implementation will also define parameters and functionality within the power supply such as control loop compensation settings. A checksum will be generated for each configuration so that the operation of the memory can be verified.

Another area requiring exceptional focus during DVT is the electromagnetic susceptibility (EMS) performance of the MCU and memory. Clearly these are highly complex, small-geometry ICs that are critical to the operation of the power supply, and are located in close proximity to the large currents and fields resident within a switching power supply. Their robustness in such an environment must be carefully verified so that data integrity is not compromised.

> Ericsson also tests the data retention and integrity of the memory by comparing the memory content via checksum both before and after the standard hardware environmental tests, such as 1000h 85°C/85% RH and life testing

Also important is to ensure that the communications bus interfacing the power supply to the outside world meets all the requirements of the appropriate specification. This is important to guarantee that the power supply will interface seamlessly with host controllers in customer systems and provide compatible communication with all other devices on the bus.

Qualification

Qualification testing ensures that the design and manufacturing processes produce a product that will provide long-term reliability under a variety of environmental conditions. This testing can be done at more than one level in the process flow, both at the component supplier and after final assembly of the power supply, for example. The key qualification challenge for digital power will be the long-term performance of the microcontroller and memory with regard to software data integrity.

The hardware qualification testing of a digital power product is very similar to that of a conventional analog product, but with additional emphasis on those elements that can affect the reliability of the stored data. The IC supplier is of course required to conduct and document extensive qualification testing at the chip level. These tests will include write endurance and data retention. As an example, Ericsson also tests the data retention and integrity of the memory by comparing the memory content via checksum both before and after the standard hardware environmental tests, such as 1000h 85°C/85% RH and life testing. Extended EMS environmental

tests will be defined to insure long-term reliability in a variety of intended application environments.

Manufacturing

The purpose of the quality focus during the manufacturing process is to eliminate all quality risks in every manufacturing step, to ensure that customers receive products on time and within specification. 'Making it right the first time' will save time and money for both the manufacturer and its customers in the long run. The changes to the manufacturing process to enable production of digital power products are actually rather minor. Changes relate to the software control component in terms of dealing with the software and memory verification. Software customization also means that now the same physical hardware can represent multiple part numbers. This customization will be done during the manufacturing electrical test process when the application software is loaded into the power supply memory. To facilitate loading and verifying the software, Automated Test Equipment (ATE) will need to be modified to include a standardized communication interface. An integrated intelligent logistics system will be used during the manufacturing test process to ensure that the correct application software is loaded into the power supply depending upon its intended purpose and functionality. The ATE will, by means of the communications interface, then conduct a memory check to verify that the software loaded into the power supply is the same as the memory content of the power supply. This is done via a bit-by-bit comparison of the input data and stored data read from the power supply memory as shown in Figure 3.

Software Upgrades

The focus on quality should also include the period after the product is shipped. Software performance and functionality enhancements could occur after the product is implemented in an end customer's equipment. These changes could be driven by improvements developed at the manufacturer or they could be the result of specific customer requests due to a change in the system requirements for the particular application. It is important to have a reliable system in place for managing this software change and upgrade activity. Software upgrades are loaded into the customer's host computer, which could be part of a development system or the control computer in the system application, can then provide the update to the affected digital power supply via the standardized communication bus.

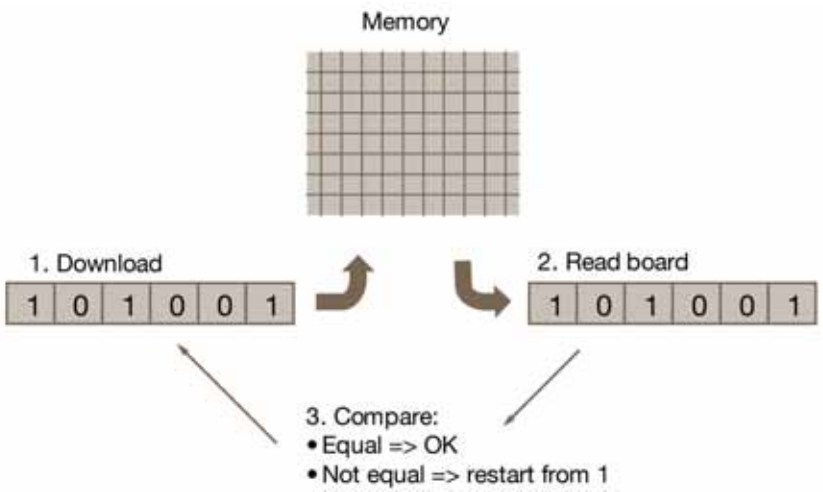
Customer Support

In case of a quality problem in the end-user product it may be related to a failure in the power supply hardware, or it could be created because of some anomaly in the end-user's product or system. In either case, it is important to have processes in place to make the proper determination accurately, quickly and with the minimum amount of disruption to the customer. All customer enquiries and concerns should be handled in a professional manner and resolved with a closed feedback loop so that corrective action is effectively communicated to the customer. The method used by Ericsson for this process, for example, is the Return Material Authorization (RMA). Digital power will actually offer some advantages for this process relative to a conventional analog power supply because of the digital supply's ability to capture operational information within the customer's system and store it in memory. Analysis of the memory content of the power supply should be quite helpful in locating the cause of the problem. This can be accomplished quickly because of the ability to transmit this data electronically in real time rather than waiting for shipment of a power supply back to the manufacturer. Furthermore, root-cause analysis and fixes for corrective action can also often be done while the power supply is still installed in the customer's application system, providing a very rapid response and resolution.

Major Trend

The use of digital power technology is a major trend for telecom and datacom systems and conversion from analog to digital control in a power supply results in new demands on the verification and qualification processes. But being proactive in facing all these new quality assurance challenges is in the best interests of the customers, and maintaining an open dialog is the best way to proceed, so that the benefits of digital power can be maximized in the transition from an analog to a digital environment. ●

Figure 3: Memory verification



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DETERMINING JUNCTION TEMPERATURE AND SWITCHING LOSSES OF POWER MOSFETS

BY **ALEXANDER ASINOVSKI**, PRINCIPAL ENGINEER, MURATA POWER SOLUTIONS INC

Junction temperature of power MOSFETs is one of the major criteria to obtain temperature derating curves for power converters. In order to keep the junction temperature (Tj) within specifications, allowable drain (leads) temperature (T_D) is often calculated by the following equation:

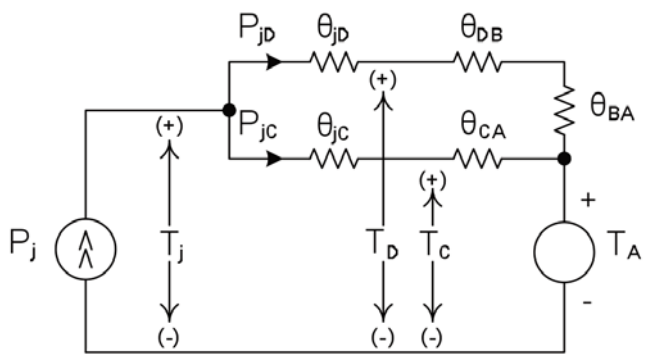
$$T_D = Tj - Pj * \theta_{JD} \quad (1)$$

where Pj is the total heat power generated inside the package (includes conduction losses, switching losses and gate losses), and θ_{JD} is the junction-to-drain (leads) thermal resistance, which is a package-related parameter, defined by the MOSFET manufacturers in their data sheets. Typical values of θ_{JD} for some standard power MOSFET packages are shown in Table 1.

If, for example, a MOSFET in an SO8 package (θ_{JD} = 15°C/W) dissipates Pj = 1W of power, which must maintain a junction temperature below 125°C, then the measured drain temperature must not exceed 110°C according to Equation 1: T_D = 125°C – 1W * 15°C/W = 110°C.

Using Equation 1 implies that Pj can be determined under any operational condition and, also, that the total power generated inside the package is dissipated to ambient through the drain leads. In reality, the accuracy of the Pj calculation is relatively low because the switching losses in the MOSFET cannot be calculated accurately enough. Also, since a portion of the Pj is dissipated to ambient through the MOSFET package, actual heat-flow through the drain leads is smaller than Pj, which presents another source of error while using Equation 1.

Figure 1: Total heat Pj generated in the MOSFET is dissipated to ambient through two parallel branches: junction-drain (leads)-PCB-ambient and junction-case (package)-ambient



A Determining Method

The objective of this article is to present a method for determining a MOSFET junction temperature and switching losses based on the given thermal resistances, and lead and case (package) temperature measurements.

In order to develop such a technique let us consider the MOSFET thermal model in Figure 1 which is a modification of the model used in www.irf.com/technical-info/designtp/dt99-2.pdf.

According to this model, the total heat generated in the package, represented by a current source Pj, flows to ambient through two parallel branches: junction-drain (leads) -PCB-ambient ("drain" or "lead" branch, labeled P_{JD}) with θ_{JD} (junction-to-drain thermal resistance), θ_{DB} (drain-to-PCB thermal resistance) and θ_{BA} (PCB-to-ambient thermal resistance), and junction-case (package)-ambient ("case" or "package" branch, labeled Pjc) with θ_{JC} (junction-to-case thermal resistance) and θ_{CA} (case-to-ambient thermal resistance). Also in Figure 1, Tc is the case temperature and T_A is the ambient temperature represented by a voltage source.

Applying conventional electrical circuit analogy to the diagram in Figure 1 and Ohm's law, we obtain the following equations for the heat portions P_{JD} and Pjc flowing through the respective "drain" and "case" branches:

$$P_{JD} = Pj/(1 + \theta_D/\theta_C) \quad (2)$$

$$Pjc = Pj/(1 + \theta_C/\theta_D) \quad (3)$$

where $\theta_D = \theta_{JD} + \theta_{DB} + \theta_{BA}$ (total "drain" branch thermal resistance) and $\theta_C = \theta_{JC} + \theta_{CA}$ (total "case" branch thermal resistance), so that total heat flow Pj is:

$$Pj = P_{JD} + Pjc \quad (4)$$

Applying Ohm's law to the series combinations of thermal resistances in each branch of the diagram in Figure 1 we get two equations for junction temperature Tj:

$$Tj = T_D + (T_D - T_A) * \theta_{JD}/(\theta_{DB} + \theta_{BA}) = T_D + (T_D - T_A) * \theta_{JD}/\theta_{DA} \quad (5)$$

$$Tj = Tc + (Tc - T_A) * \theta_{JC} / \theta_{CA} \quad (6)$$

Both Equations 5 and 6 do not contain heat power Pj and each of them can be used for calculating the junction temperature Tj, as long as the case, drain, ambient temperatures and thermal resistances of the package are known.

If we apply these equations to a typical SO8 power MOSFET with thermal resistances θ_{CA} = 380°C/W, θ_{JC} = 18°C/W, θ_{JD} = 15°C/W and θ_{DA} = 20°C/W (given in www.irf.com/technical-info/designtp/dt99-2.pdf), substituting these values into Equations 2 and 3 we obtain:

In reality, the accuracy of the Pj calculation is relatively low because the switching losses in the MOSFET cannot be calculated accurately enough

$$P_{JD}/P_j = 1/[1 + (15 + 20)/(18 + 380)] = 0.92 \quad (7)$$

$$P_{JC}/P_j = 0.08 \quad (8)$$

In other words, 92% of total power generated in the silicon is dissipated to ambient through the drain and the remaining 8% through the case.

Another important observation is that θ_{CA} is much greater than any other thermal resistance in the system, which makes the second term in Equation 6 relatively small. Assuming Tc = 125°C and T_A = 85°C for the set of parameters given above, the junction temperature according to Equation 6 is:

$T_j = 125 + (125 - 85) * 18/380 = 126.9°C$. This is only 1.9°C greater than the case temperature. Using Equation 5 to calculate the drain temperature, we obtain:

$T_D = (T_j + T_A * \theta_{JD}/\theta_{DA})/(1 + \theta_{JD}/\theta_{DA}) =$

$= (126.9 + 85*15/20)/(1 + 15/20) = 108.9°C$

This temperature is lower than the case temperature by 16.1°C. This implies that, for an SO8 power MOSFET with θ_{JD} being on the same order as θ_{DA} and with θ_{CA} being much greater than θ_{JC}, the drain temperature tends to be lower than the case temperature, not only that but the plastic case temperature is an accurate representation of the junction temperature.

According to the measurement results in **www.irf.com/technical-info/designtp/dt99-2.pdf** the difference between Tj and Tc for SO8 packages is typically 1-3°C. If we use the same equations for other MOSFET packages like PPAKSO8, D2PAK, DPAK and LFPAK with low junction-to-drain thermal resistances θ_{JD} (see Table 1), both the drain and case temperatures are close to the junction temperature Tj. For DirectFET type MOSFETs with metal case θ_{JD} is even lower and, according to Equation 5, the drain temperature is an accurate representation of the junction temperature.

For a more accurate Tj calculation based on Equation 5, parameter θ_{DA} unavailable from MOSFET data sheets can be determined as follows. According to Figure 1 junction-to-ambient thermal resistance θ_{JA}, provided in the MOSFET data sheets, is a parallel combination of θ_D and θ_C resistances and $\theta_{DA} = \theta_D - \theta_{JD}$. Applying this to the diagram in Figure 1 we can get:

$$\theta_{DA} = \theta_{JA}/(1 - \theta_{JA}/\theta_C) - \theta_{JD} \quad (9)$$

Taking into account that θ_C is approximately one order greater than θ_{JA}, Equation 9 can be rewritten as:

$$\theta_{DA} \approx 1.1 * \theta_{JA} - \theta_{JD} \quad (10)$$

Substituting (10) into (5) we get:

$$T_j \approx T_D + (T_D - T_A) * \theta_{JD}/(1.1 * \theta_{JA} - \theta_{JD}) \quad (11)$$

where all the thermal resistance values are available from the data sheets.

Conventional Technique

The junction temperature was calculated above based on parameters specified on the component data sheet and temperature measurements taken from the device under test conditions. A conventional drain (lead) and case (package) temperature measurement technique is based on the thermocouples placement on the package and on the lead areas. The measured temperatures with the thermocouples are lower than actual temperatures for two reasons: first, the thermocouple itself works as a heat sink cooling the device down and, second, its physical placement is critical when trying to determine the hottest temperature of the device. A more accurate temperature measurement method is the use of an infrared camera which determines the hottest spot temperature in the areas of interest (case and lead) without the heat flow intrusion.

As soon as the junction temperature Tj is determined, total power Pj generated in the silicon can be calculated by the formula:

$$P_j = (T_j - T_A)/\theta_{JA} \quad (12)$$

where θ_{JA} (junction-to-ambient thermal resistance) is available from the MOSFET data sheets. Pj can also be calculated based on Equation 2 and junction-to-drain thermal resistance θ_{JD} which is also available from the MOSFET data sheets:

$$P_j = (1 + \theta_D/\theta_C) * (T_D - T_A)/\theta_{JD} \quad (13)$$

θ_D and θ_C are not available from the data sheets but since θ_C is approximately one order greater than θ_D, Equation 13 can be rewritten as:

$$P_j \approx 1.1 * (T_D - T_A)/\theta_{JD} \quad (14)$$

After Pj is determined, switching losses Psw can be calculated in the conventional way:

$$P_{sw} = P_j - P_{dc} - P_g = P_j - I_{rms}^2 * Rds_{on} - Q * V_g * F_{sw} \quad (15)$$

where Pdc is the conduction DC losses, Pg is the gate drive losses, I_{rms} (RMS value of drain current), Rds_{on} (MOSFET ON resistance), Q (total gate charge), V_g (peak gate voltage), Fsw (switching frequency). For a square wave drain current with peak I_{pk} and duty cycle D, $I_{rms}^2 = I_{pk}^2 * D$.

From the above analysis based on the thermal model in Figure 1 it is quite evident that the hottest spot temperature on the lead and case (package) areas of a power MOSFET is typically a couple of degrees Celsius less than the junction temperature. This hottest spot temperature can be accurately measured by an infrared camera without the heat flow intrusion.

- A more accurate junction temperature value can be calculated by Equations 5, 6 and 11, based on lead and case temperatures measured by an infrared camera and thermal resistance values provided in the MOSFET data sheet.
- Total power generated inside the silicon and switching losses can be determined by Equations 13 to 15.

Thermal Resistance	Package Type					
	DirectFET	PowerPAKSO8	DPAK	D2PAK	LFPAK	SO8
θ_{JD} (°C/W)	1	1.5	1.5	1.5	2	15

Table 1: Typical values of θ_{JD} for some standard power MOSFET packages

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eoSemi Unveils Silicon Oscillator Technology

eoSemi disclosed further details of its innovative silicon oscillator technology and announced that it has commenced shipping pre-commercial versions of its first product. The company is working with a small group of key strategic customers and partners.

eoSemi's ATOC (Accurate Timing Oscillator Circuit) technology allows the company to offer all-CMOS silicon alternatives to the costly, bulky quartz crystal oscillators that are used in almost every consumer electronic product. Because its devices can be made using standard semiconductor manufacturing technology, eoSemi's products are cheaper, smaller, easier to integrate, more robust and consume less power than competing offerings.

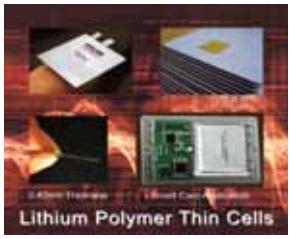
ATOC brings together a number of innovations in oscillator design, including proprietary techniques to sense and compensate for changes in temperature and physical stresses within the device. A unique fundamental circuit design allows the oscillator's output frequency to be tuned instantaneously in real-time, and compensates for drift over the lifetime of the device.

www.eosemi.com

VERY THIN LITHIUM POLYMER PRIMARY CELLS FROM POWERSOLVE

Powersolve continues to bring innovative power products to the marketplace with the introduction of Lithium Polymer thin-cells that can be manufactured down to just 0.4mm thick. The CP Series consists of Lithium Polymer thin cells which are primary laminated aluminium thin foil batteries with a nominal 3VDC output.

Very light in weight, the new CP Series cells are available in a wide range of standard sizes from 16mAh up to 3000mAh.



Powersolve says the technology allows a customer to request a cell built to a size that suits a specific application.

The cells have a very low self-discharge rate of around 1% a year with a shelf life of 10 years. The cells are safe in use, explosion-proof and operate between -40 to +85ºC.

The CP 452345 is a typical example of the CP Series. Measuring just 0.45mm x 23mm x 45mm, it weighs 0.7g and gives 30mAh.

Powersolve will be at this year's National Electronics Week, taking place on the 18th and 19th of April in Birmingham.

www.powersolve.co.uk

1A, 0.5V Ultra-LDO Voltage Regulator with Programmable Soft-Start

The new XC6603/04 series from Torex is a high speed and highly accurate LDO family which can supply up to 1A of output current while consuming only 100µA. With the help of a bias voltage that can be set between 2.5V and 6.0V, the XC6603/04 operates with input voltages from 0.5V to 3.0V and is readily available with fixed output voltages from 0.5V to 1.8V in 0.1V increments.

It is thanks to its integrated N-ch driver transistor that the minimum input and output voltages of the XC6603/04 can be much lower than more traditional LDOs with their integrated P-ch transistors. Another advantage of the XC6603/04 integrated N-ch driver transistor is that it dramatically reduces the on-resistance at low output voltages, leading to dropout voltages as low as 155mV @ 1A with VOUT = 1.2V (VBIAS = 3.6V). This makes the XC6603/04 ideally suited for low input/output voltage applications which require high output current and extended battery life.

www.torex-europe.com

LECROY'S 8- AND 12-PORT SPARQ SIGNAL INTEGRITY NETWORK ANALYSERS

LeCroy Corporation has announced the availability of 8- and 12-port models of the SPARQ series of signal integrity network analyzers. The SPARQ makes S-parameter measurements quickly and is a fraction of the price of Vector Network Analyzers (VNAs). With the SPARQ models, signal integrity engineers have a product for characterizing crosstalk in multi-lane differential structures.

The 8- and 12-port SPARQ units are extensions to the SPARQ series of signal integrity network analyzers launched in September, 2010. SPARQ is designed specifically for signal integrity applications, and uses state-of-the-art TDR/TDT techniques to measure the S-parameters of passive devices.

SPARQ users can connect the SPARQ to their DUT and PC, which runs the SPARQ application. After configuring the measurement by setting the number of ports, points and end frequency, the measurement is started by simply clicking "Go".

The SPARQ automatically calibrates in only about 1 minute using the built-in OSLT calibration kit.

www.lecroy.com

New 16-Channel Temperature Input Module for Yokogawa's Scopecorder

A new 16-channel temperature/voltage plug-in input module for the Yokogawa DL850 ScopeCorder has been added to the range of electrical and physical input modules available for this versatile instrument.

The new module extends the electromechanical testing capabilities of the DL850 ScopeCorder by allowing it to be used for a wide range of applications where parameters such as voltage and current need to be measured simultaneously with physical parameters such as temperature.

The new 16-channel temperature/voltage input module and its external scanner box will find use in many electromechanical processes where temperature change or heating is expected and needs to be monitored along with electrical parameters and physical ones such as pressure and strain. By configuring the ScopeCorder with multiple input modules, a portable measuring device with up to 128 channels can be configured to suit any R&D, service or maintenance task. Typical applications include tests on domestic electrical appliances, inverters and electric drives.

www.yokogawa.com

DUAL LNB SUPPLY AND CONTROL VOLTAGE REGULATOR IC

The new A8299 from Allegro MicroSystems Europe is a robust dual-channel low-noise block (LNB) regulator, designed to provide the power and interface signals via coaxial cable to the LNB down-converters used in analogue and digital satellite receivers.

The A8299 is a monolithic linear and switching voltage regulator which minimises the need for external components by integrating the boost switch and compensation circuitry within the low-profile package. The boost regulator architecture allows the use of smaller external components such as ceramic capacitors, which minimises the solution footprint and height profile as opposed to using electrolytic capacitors.

The A8299 offers an adjustable LNB output current limit from 250mA to 950mA, and features in-built diagnostics and a wide range of protection capabilities.

The A8299SETTR-T is supplied in a small (5mm × 5mm), low-profile (0.9mm) QFN 28-pin package (suffix ET), and its features and functions easily meet or exceed industry requirements for the latest generation of satellite set-top boxes.

www.allegromicro.com

PMBUS-COMPLIANT SYNCHRONOUS BUCK CONTROLLER POWER SAVING MODES

Powervation Ltd, pioneer in adaptive digital power IC solutions that increase system efficiency, improve field reliability and accelerate time to market, announced the PV3101 – a new single phase digital DC/DC controller featuring the company's Auto-Control adaptive loop compensation technology.

The PV3101 uses proprietary DSP/RISC dual-core architecture with a precision data acquisition engine running advanced control and power management algorithms in firmware. With this architecture, Powervation's new controllers provide features, flexibility and performance beyond that seen on other digital power solutions today.

The Auto-Control adaptive loop compensation algorithm provides the industry's first and only real-time autonomous compensation solution and is able to modulate the converter's bandwidth on a cycle-by-cycle basis to optimize the trade-off between dynamic performance and system stability. PV3101 uses full differential voltage, current and temperature measurements and an 11-bit ADC to provide precision measurement, tight control and accurate real-time reporting of telemetry information for key power-supply parameters.

www.powervation.com

Powerlock Box From ITT ICS Offers Fast Emergency Power Supply Connection

The VEAM PowerLock Box from ITT Interconnect Solutions enables emergency power to be quickly and safely re-connected to large facilities such as supermarkets, defence installations, factories, hospitals and offices in the event of failure of the mains supply. Offering a single re-connection point, the PowerLock Box provides a simple and speedy solution, vital to protect valuable frozen and chilled foodstuffs in supermarkets and restore power to essential equipment in hospitals and offices.

The VEAM PowerLock Box provides a single, easy-to-use connection point for any emergency generator and, when fitted in a supermarket's electrical switch room or sub-station, allows cables from a mobile generator to be quickly connected to the store's power system. The PowerLock Box has ground, neutral and 3-phase connectors which are keyway controlled and can only be mated in the correct sequence. Contacts are finger-protected to prevent inadvertent touching of live parts.

www.ittcanon.com

MOLEX PRESENTS GLOBAL DISTRIBUTOR OF THE YEAR AWARD TO AVNET ELECTRONICS MARKETING

Avnet Abacus, one of Europe's leading interconnect, passive, electromechanical and power distributors, today announced that Molex Incorporated has awarded the 2011 Global Distributor of the Year award to Avnet Electronics Marketing, a leading global distributor of electronic parts and embedded subsystems. The award recognizes valued partners demonstrating financial, operational and executive management excellence. Molex is represented by Avnet's European interconnect, passive, electromechanical and power specialist distributor, Avnet Abacus, in the EMEA region.

"We are proud to recognize Avnet's significant contribution to our global distribution results in 2011," said Graham Brock, president, sales and marketing division, Molex. "This award represents the commitment demonstrated by the Avnet teams in Asia, Europe and the Americas and the contribution that it made to significant revenue growth for both our companies. We have worked very hard to be a major supplier of interconnection products to Avnet for 29 years."

www.avnet-abacus.eu

Murata Introduces 4:1 Input 204W Quarter-Brick DC/DC Converter

Murata Power Solutions announced the UWQ series of isolated open-frame 204 Watt DC/DC converters packaged in a through-hole mount industry standard quarter-brick format.

Measuring just 58.4 x 36.8 x 11.7mm and boasting an efficiency of 92%, the UWQ series has an ultra-wide 4:1 input voltage range of 18–75VDC around a nominal 48VDC input. Providing a single output voltage of 12VDC up to 17A of current with a line regulation of ±1% and load regulation of ±1.5%, the UWQ series is ideal for applications that require a regulated bus converter. The input to output isolation is certified to 2,250VDC in accordance with the internationally recognized safety standard EN/UL60950.

Features include remote On/Off control for negative or positive polarity, and protection against over current, over temperature, input under voltage and output short circuit. Designed for Regulated Intermediate Bus Architectures, typical applications include optical networking, wireless base-stations and microwave radio communications equipment.

www.murata-ps.com

The World's First COM Express Mini Computer-on-Module with Dual Core Processors

Kontron announced the world's first COM Express mini Computer-on-Module with Dual-Core processing power.

The Kontron COMe-mCT10 – the latest addition to the family of formerly named nanoETXexpress modules – is based on the next-generation Intel Atom processors N2600, N2800 and D2700. Optimized for low-power small form-factor designs, the PICMG COM Express Type 10 pin-out Computer-on-Module provides up to twice the graphics power, up to 28% higher processor performance and processor thermal design power (TDP) which is cut in half, compared to the second generation Intel Atom processors.

The credit-card-sized COM Express mini form-factor is ideal for developers of small devices who want to take full advantage of the high level of standardization and scalability of the COM Express standard. Applications based on the new Kontron COM Express mini Computer-on-Module COMe-mCT10 with Intel Dual core processor performance are well-suited for handheld mobile embedded systems, as well as small portable, in-vehicle or stationary devices such as POS/POI, infotainment, digital signage, gaming and medical.

www.kontron.com

NEW FLAME RETARDANT EMC SHIELDING GASKET FROM KEMTRON

Kemtron, the British manufacturer of RFI/EMI shielding gaskets, materials and components has launched a flame retardant, low smoke, low toxicity EMC shielding gasket.

It's tested and approved to the international standard UL94V-0 by Underwriters Laboratories for flame retardancy, file number E344902. Also tested for smoke density to BS 6853:1999: Annex D.8.3and oxygen index to BS EN ISO 4589-2:1999, confirming the material meets the requirements for minor internal use on vehicles category 1a such as gaskets for electronic enclosures, is making it highly suitable for applications in underground transportation, trains and other safety critical applications.

The material is nickel-coated graphite loaded into silicone elastomers, product code SNG-FR. This allows the gasket to provide a highly electrically-conductive path between mating flanges of an electronics equipment enclosure giving a high level of RFI/EMI shielding. The material can be supplied as an extruded strip in various profiles, "O" rings or flat die cut gaskets.

www.kemtron.co.uk

Hybrid Connector Module Combines Power-Supply and Signal Contacts

Power supply and signal contacts are combined in the new Han 70 A Hybrid Module, the latest model in Harting's Han-Modular highly flexible open connector system.

The Han 70 A Hybrid Module has a power contact with a current capacity of 70A at a rated voltage of 1000V and four additional signal contacts designed for up to 400V, based on standard Han E crimp contacts rated at up to 16A.

The power contact has axial screw terminals. Cables measuring from 6 to 22mm² (8-4 AWG) can be connected without using an expensive special tool. A secure and durable connection can be made with a standard 2.5mm hexagon screwdriver.

Harting's Han-Modular series enables users to create their own customised connector to the desired configuration. Various modules are available for electrical, optical and gaseous signals, and the range is constantly updated.

www.harting.com

TELONIC ANNOUNCES PROMOTIONAL £260+VAT PRICE ON RIGOL DS1052E OSCILLOSCOPE

The Rigol DS1052E is now available from Telonic Instruments at a promotional price of just £260 for a limited time. The DS1052E is Rigol's 50MHz, 2-channel flagship digital oscilloscope. With features including FFTs, signal record and replay, roll mode display, alternate trigger mode, adjustable trigger sensitivity, PictBridge printing and deep memory (up to 1 Million points), the DS1052E is a complete oscilloscope for the bench at a great new price.

The DS1052E also makes it easy to save and recall test setups, waveforms and data with full USB integration and control. The features and intuitive design of the DS1052E make it a great value from the consultant's bench to the development lab.

www.rigol-uk.co.uk

ANSMANN ENERGY RELEASES NEW LI-ION PACKS WITH UN CERTIFICATION

In addition to complex customized battery packs with individual safety board and communication software, ANSMANN is launching a new range of standard Li-ion packs. These new Li-ion packs will offer seven different configurations (2250mAh at 3.7V, 7.4V, 11.1V & 14.8V, 4500mAh at 3.7V & 14.8V and 6750mAh at 3.7V).

With ultrasonic welding technology and in-house 3D plotter/cutter, ANSMANN is able to fulfil special battery pack requirements and to produce physical samples without expensive tooling set-up charges. ANSMANN also uses state-of-the-art equipment to provide certification and approval for every battery pack.

The combination of off-the-shelf Li-ion batteries and 3D plotter technology significantly reduces lead-time and eliminates the prohibitive upfront costs usually associated with Li-ion projects.

ANSMANN has a dedicated laboratory for testing Lithium batteries in conformance with UN transport regulations. The UN testing procedure is designed for batteries using Lithium technology.

www.ansmann.co.uk

UNIVERSITY MAKES A 3D OBJECT INVISIBLE

Austin, Texas-based university scientists have managed to make a three-dimensional object invisible. They cloaked an 18cm cylindrical tube in an experiment that used the so-called plasmonic metamaterials, and then bombarded it with 3.1GHz microwaves.

In the experiment, the university researchers hit the tube with microwaves. The microwaves that bounced off the tube cancelled out with those of the metamaterial's refracting negatively, rendering the tube invisible.

"When the scattered fields from the cloak and the object interfere, they cancel each other out, and the overall effect is transparency and invisibility at all angles of observations," said the University of Austin Assistant Professor Andrea Alu.

So far the cloaking worked best at the microwave frequency of 3.1GHz. In theory it can work with visible light too, however the objects will be only micrometers small.

For now, the plasmonic metamaterials approach has the potential to camouflage military objects.

HARRY JOSEPH, audio-visual consultant, New York City, US: Oh, good! The slippery slope will now be invisible.

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, Italy: Potential applications of metamaterials are diverse and include remote aerospace applications, sensor detection and infrastructure monitoring, smart solar-power management, public safety, high-frequency battlefield communication and lenses for high-gain antennas, improving ultrasonic sensors and, even, shielding structures from earthquakes.

By fabricating such metamaterials fundamental limits tied to the wavelength of light cab be overcome. Light hitting a metamaterial is transformed into electromagnetic waves of a different variety – surface plasmon polaritons, which are shorter in wavelength than the incident light. This transformation leads to unusual and counterintuitive properties that might be harnessed for practical use. Moreover, new approaches that simplify the fabrication process of metamaterials are in development. This work also includes making new structures specifically designed to enable measurements of the materials' novel properties. Furthermore, nanotechnology applications for these nanostructures are currently being researched, including microscopy beyond the diffraction limit.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: It is interesting that 3D invisibility can be achieved at microwave frequencies. I am sure this will have potential applications where microwave frequencies are used, such as in microwave communications, radar, etc. But the real challenge will be to do 3D cloaking at visible light. Then the number of potential applications will be countless!

> Light hitting a metamaterial is transformed into electromagnetic waves of a different variety – surface plasmon polaritons, which are shorter in wavelength than the incident light

IVOR CATT, Engineer and Scientist, UK: I was employed in the weapons industry, and found out about military weapon projects with ludicrous objectives. This is the military-industrial-scientific complex at its extreme.

I always wonder who would rather be attacked by one (invisible?) plane costing one billion dollars or one thousand planes costing one million dollars each. A dictator cannot really buy ten million rifles costing a pound each. Where would he put them? Easier to buy an aeroplane costing the same, and park it somewhere. Then use the 20% commission to build palaces.

While in GEC, the technical director called us together to announce the good news: "We've tripled our spend capability!" That meant we had tripled our 14% profit (taxpayers' money) on the cost, plus 14% weapon design project.

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: The key phrase being: "...our results pave the way to realistic, practical applications of 3D standalone cloaks for radar evasion and non-invasive radio frequency probing". The latter issue has been neglected, whereas the former still has arbitrary geometries to contend. Metamaterials enable the control of negative refractive indices, the other breakthrough aspects relating to diffraction and dispersion where announced, also in January, in Nature Vol481 article '*Demonstration of temporal cloaking*'. Temporal cloaking has greater potential for communication systems but it is when this time-space duality is integrated that a fuller appreciation of what light is may emerge.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Since long ago man has tried to become invisible, mostly through fantasy. Hermes, the Greek God of commerce, triumphed thanks to his helmet which made him invisible. The young Harry Potter ran away from Voldemort thanks to his invisible cape. Although up to now the scientists have not fabricated such cloaks, the idea already comes from Texas-based University in the US. What was science fiction in the past becomes a reality today.

By combining various materials and by using electromagnetic waves, the physicists hope to manipulate light to shield objects. This technology is applied to materials behaving under particular conditions, but still, scientists are getting closer to the concept. For now it's plasmonic metamaterials that are the key to invisibility, even though it can only work at certain frequencies. Apart from its use in the military field, the technology could come in handy for security systems too.

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector please register your interest with the editor by writing to Svetlana.josifovska@stjohnpatrick.com

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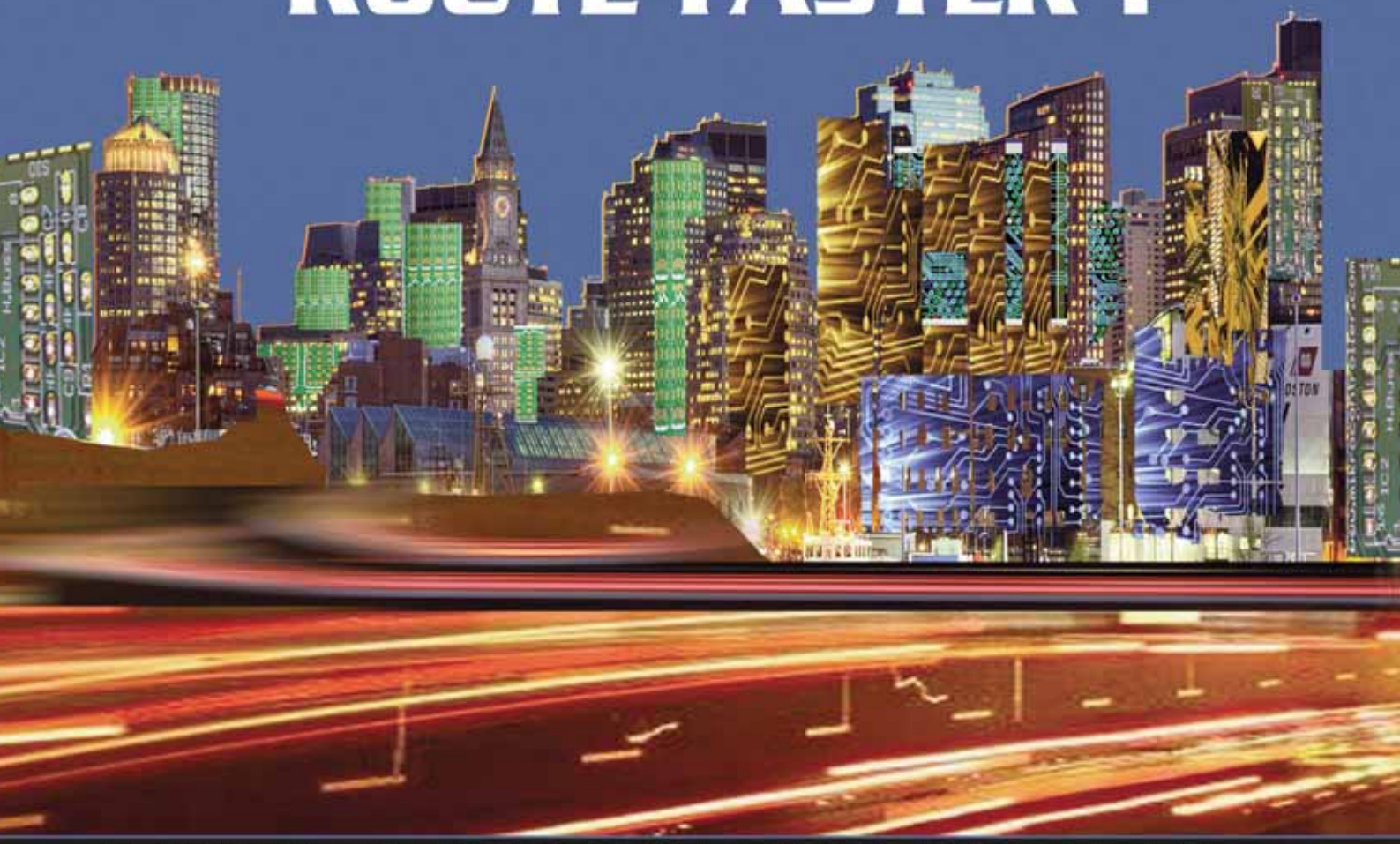

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