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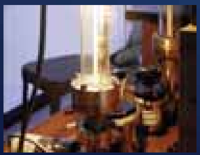

Technology
New growing technique for graphene

NEW series
DAQ system design

Special report
Audio

Cover supplied by MOUSER ELECTRONICS More on pages 8-9

REGULARS

05 **TREND**
HOW SOFTWARE GAVE NEW LIFE TO DEVICE MANUFACTURERS

06 **TECHNOLOGY**

10 **THE TROUBLE WITH RF...**
LOOK BACK!
by **Myk Dormer**

12 **FOCUS**
LEGACY OF CONSUMER MEMORY TRANSLATES TO A GENERATION OF PROBLEMS
by **Victoria Barrett**

39 **LETTERS**

40 **NEW DAQ SYSTEM DESIGN COLUMN**
by **Maurizio di Paolo Emilio**

44 **TIPS 'N' TRICKS**

46 **PRODUCTS**

50 **LAST NOTE**

06 Technology

12 Focus

FEATURES

14 **MEASURING LOUDSPEAKER IMPEDANCE**
Loudspeakers present their manufacturers with a number of challenges when it comes to test and measurement, both at the design and manufacturing stage. **Joe Begin** considers how to test loudspeaker impedance accurately using the constant voltage method

18 **MOBILE HANDSET AUDIO PERFORMANCE**
Greg Davis addresses the mobile phone's audio playback facility and, specifically, the MP3 player audio output to headphones

20 **THE SAFE OPERATING AREA (SOA) PROTECTION OF LINEAR AUDIO POWER AMPLIFIERS**
Michael Kiwanuka gives a detailed account of over-voltage and over-current protection for power semiconductors in audio power amplifiers

36 **WORLD'S FIRST 40NM MONOS FLASH TECHNOLOGY**
Jürgen Axmacher outlines the benefits for the automotive sector of Renesas's latest MONOS embedded flash technology fabricated in the 40nm process node

COMPETITION WINNER

Gary Sims from Buckinghamshire in the UK and RF Engineer at Cable Free Vision Ltd won our recent competition.
He wins a copy of "Baxandall and Self on Audio Power" book.
Congratulations from the EW team!

HOW SOFTWARE GAVE NEW LIFE TO DEVICE MANUFACTURERS

For many years the physical device was the livelihood of the device manufacturing industry. Every year, manufacturers could structure their business models and sales goals around the very predictable sales of physical devices. But with the globalised economy, increased competition and business demands moving towards differentiated, on-demand and cloud capabilities, the realities of the physical device marketplace have rapidly changed.

On one level, the device itself was the problem. As devices became commoditised, the number of suppliers dwindled and manufacturers could not differentiate themselves with the device itself. The device became expensive to manufacture and to stock – money that could be better spent on innovation and development. Once the device was sold, the relationship between the vendor and purchaser was generally at an end, especially if the device was built well. If the device was built poorly, then that's an entirely different problem.

At another level, technology was evolving, people were not using devices the same way they had in the past and many manufacturers were so steeped in the traditional way of doing businesses they hadn't evolved to meet users' needs. These differing demands, coupled with the commoditisation of hardware devices, forced many device manufacturers to rethink their business models.

Monetising Devices with Software

Many device manufacturers simply could not remain profitable selling only devices. They needed to figure out a way to add value, monetise the embedded software the device was running and extend its life. The software business was, and still is, very profitable, generating healthy margins, recurring revenues and global market reach. Many manufacturers already had software embedded in their devices, they just needed to figure out a way to use the embedded software to differentiate the device and monetise the capabilities and capacity of the device. Wisely, manufacturers chose to embrace a software-centric approach to selling hardware, to ensure differentiation and optimisation of revenue.

Monetising software allowed manufacturers to deliver more value to customers in the form of capacity and capability provisioning and upgrades, protection of intellectual property, competitive differentiation, additional revenue streams and targeting of multiple geographies, without the increase in manufacturing stock keeping units (SKUs). The result was improved customer satisfaction and, ultimately, increased profit margins and, therefore, significantly improved business performance.

> *While a shift in business strategy to a software-centric value proposition offers numerous advantages, it is not easily or quickly accomplished*

Managing the Transformation

While a shift in business strategy to a software-centric value proposition offers numerous advantages, it is not easily or quickly accomplished. To effectively transition business strategies and optimise the results achieved from such a shift, it is important that manufacturers follow a proven, practical process for adaptation.

There are several initial steps that are imperative for a smooth transition to a software-centric business model, including securing organisational buy-in, comprehending software licensing, training sales staff on how to sell software, creating go-to-market strategies and a thorough understanding of the software value lifecycle. Beyond the practical steps, there are also the organisational impacts. Organisations need the right people – the right knowledge, the right experience and the right champion – to move the mission forward.

In addition, device manufacturers need to think like a software company by adopting and deploying the right methodologies and technology for embedding software licensing and entitlement management while adapting their operational and business processes to support a software business model. Adopting application usage management solutions that leverage embedded software licensing, entitlement and device lifecycle management can enable manufacturers to unlock new revenue streams, protect and monetise intellectual property and implement configure-to-order manufacturing processes that dramatically reduce inventory while facilitating greater responsiveness to changing market conditions.

With all of this considered, the transition can be challenging, but there are substantial benefits to be gained for those manufacturers willing to make the transition.

Today, the shift is happening everywhere. Everyday devices, from a satellite box to the office ventilation system, to more sophisticated devices like medical and military equipment, are running on embedded software. Much of the software on these devices is sold by brands we might think of as traditional device manufacturers – brands that have made the profitable decision to become software-centric.

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HIGH QUALITY GRAPHENE GROWN IN LAB

Georgia Tech graduate students Yike Hu and John Hankinson observe a furnace used to produce graphene on a silicon carbide wafer *[Photo: Gary Meek]*

Scientists from the Georgia Institute of Technology have for the first time provided details of their "confinement controlled sublimation" technique for growing high-quality layers of epitaxial graphene on silicon carbide wafers. The technique relies on controlling the vapor pressure of gas-phase silicon in the high-temperature furnace used for fabricating the material.

The basic principle for growing thin layers of graphene on silicon carbide requires heating the material to about 1,500 degrees Celsius under high vacuum. The heat drives off the silicon, leaving behind one or more layers of graphene. But uncontrolled evaporation of silicon can produce poor quality material useless to designers of electronic devices.

"For growing high-quality graphene on silicon carbide, controlling the evaporation of silicon at just the right temperature is essential," said Walt de Heer, a professor who pioneered the technique in the Georgia Tech School of Physics. "By precisely controlling the rate at which silicon comes off the wafer, we can control the rate at which graphene is produced. That allows us to produce very nice layers of epitaxial graphene."

De Heer and his team begin by placing a silicon carbide wafer into an enclosure made of graphite. A small hole in the container controls the escape of silicon atoms as the one-square-centimeter wafer is heated, maintaining the rate of silicon evaporation and condensation near its thermal equilibrium. The growth of epitaxial graphene can be done in a vacuum or in the presence of an inert gas such as argon, and can be used to produce both single layers and multiple layers of the material.

"This technique seems to be completely in line with what people might one day do in fabrication facilities," said de Heer. "We believe this is quite significant in allowing us to rationally and reproducibly grow graphene on silicon carbide. We feel we now understand the process, and believe it could be scaled up for electronics manufacturing.

Graphene Mixer Can Speed Up Future Electronics

Researchers at Chalmers University of Technology in Sweden have for the first time demonstrated a novel subharmonic graphene FET mixer at microwave frequencies. The mixer provides new opportunities in future electronics, as it enables compact circuit technology and operation at extremely high frequencies.

A mixer is a key building block in all electronic systems; it combines two or more electronic signals into one or two composite output signals. Future applications at THz frequencies – such as radar systems for security and safety, radio astronomy, process monitoring and environmental monitoring – will require large arrays of mixers for high-resolution imaging and high-speed data acquisition. Such mixer arrays or multi-pixel receivers need new types of devices that are not only sensitive but also power-efficient and compact.

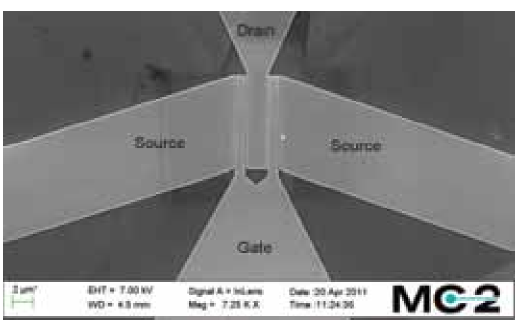
The ability of graphene to switch between hole or electron carrier transport via the field effect enables a unique niche for graphene for RF IC applications. Thanks to this symmetrical electrical characteristic, the researchers at Chalmers have managed to build the G-FET subharmonic resistive mixer using only one transistor. As such no extra feeding circuits are required, which makes the mixer circuit more compact than conventional ones. As a consequence, the new type of mixer requires less wafer area when constructed and can make possible advanced sensor arrays, for example for imaging at millimetre and sub-millimetre waves as G-FET technology progresses.

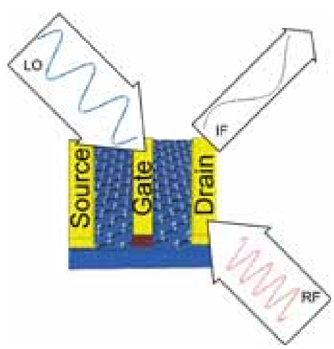
"The performance of the mixer can be improved by further optimising the circuit, as well as fabricating a G-FET device with a higher on-off current ratio," said Jan Stake, a professor and part of the research team. "Using a G-FET in this new topology enables us to extend its operation to higher frequencies, thereby exploiting the exceptional properties of graphene. This paves the way for future technologies operating at extremely high frequencies."

In addition to enabling even more compact circuits, the G-FET provides potential to reach high frequencies in circuits, and enables a subharmonic mixer to require only half the local oscillator (LO) frequency compared to a fundamental mixer. This property is attractive especially at high frequencies (THz) where there is a lack of sources providing sufficient LO-power.

Moreover, the G-FET can be integrated with silicon technology. It is CMOS (Complementary Metal Oxide Semiconductor) compatible and it can be used in CMOS electronics for back-end processing on a single chip.

Graphene was first produced in 2004, but it has rapidly gone from curiosity-driven to applied research. You can find out more about the active research into graphene at Chalmers: **www.chalmers.se/en/news/Pages/Millions-in-research-to-take-graphene-out-of-the-lab.aspx**





Schematic picture of a subharmonic graphene-FET mixer. The LO and RF signals are fed to the gate and drain terminals, respectively, and the IF signal is extracted from the drain terminal. *[Image: Chalmers]*

MOUSER ELECTRONICS: ANSWERING THE CALL OF DESIGN ENGINEERS WITH ADVANCED PRODUCTS FOR NEW DESIGN

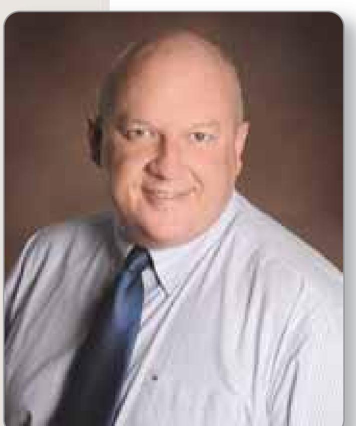
Most of the recent innovations in audio can be attributed to modern digital audio. With digital electronics, sound generation does not have to originate as mechanical energy transformed into a propagating sound wave. An audio experience can be created entirely via digital electronics of unnatural origin.

"Digital advancements in audio have taken sound possibilities to new levels that we never thought were possible 10 years ago," says Graham Maggs, Mouser Electronics Director of EMEA Marketing and Business Development." Mouser is a top global distributor of electronic components and semiconductors, providing the newest products and advanced technologies from more than 450 suppliers.

In addition to the newest products available on the European market today, Mouser provides design engineers in Europe with local technical support from its European headquarters in Munich, Germany, local office in the United Kingdom, and seven other offices throughout Europe. The global design-fulfillment distributor provides the full package of the newest products and comprehensive resources, helping engineers get their designs to market faster.

"We deliver a speed-to-market advantage for the engineers," Maggs continues. "Up against the clock, their time is extremely valuable. Engineers appreciate our fast product delivery and unmatched local support in local language, currency and time zone."

Maggs says that today's innovative products are leading to amazing design possibilities in sound. For example, a recently patented invention can focus sound so that it can be aimed at a specific location with no effect on individuals nearby. It separates sound within small spaces, allowing diners to experience different music at each table of a restaurant. Clearly, a mixture of powerful electronics and software can enable innovation in audio that expands applications beyond the entertainment industry.



Graham Maggs, Mouser Electronics, Director of EMEA Marketing and Business Development.

Audio innovation is within reach thanks to today's creative and well-tuned devices. Some excellent examples of this technology can be found in Mouser Electronics' comprehensive Audio Applications Product Knowledge Center (PKC) training site. The easy-to-navigate site focuses on solutions from noise cancellation, wireless headphones, and guitar wiring, to the latest in consumer audio for entertainment in sound bar technology. To learn more, visit **http://www.mouser.com/audio_applications/**.

Audio innovation also encompasses vibration and silence, as well as audible sound. Active noise-cancellation in a car cabin is one new application here. What's Next? Microphones embedded in the headliner pick up ambient road noise that is quickly processed and locally broadcasted as anti-sound waves of equal amplitude but opposite phase to cancel local interior noise.

Digital advancements in audio have taken sound possibilities to new levels

The electronics to implement active noise cancellation typically include a powerful DSP and surrounding devices, such as Texas Instruments' highly integrated stereo audio CODEC, with features required for such an application: Fast, flexible, powerful, and ideally suited for the task with extensive signal processing options in an integrated mini-DSP, Maggs explains.

Mouser's audio site features applications with system block diagrams to navigate for easy reference. Functional blocks link to lists of relevant and recommended parts from major component manufacturers such as Texas Instruments, Fairchild Semiconductor, Maxim Integrated Products, Bourns, and NXP Semiconductors.

The Audio Applications site on mouser.com includes related articles and resources from innovating manufacturers. The educational site for audio applications is a training repository for information, technical documents, application notes, and videos.

"Our goal is to provide design engineers across Europe with the newest products and product knowledge to help them get their designs to market faster," Maggs concludes.

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Look back!

MYK DORMER IS SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
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As engineers it is in our nature to always look to the future and to seek the next breakthrough – or even barrier. During design – low power RF included – each passing month reveals new devices, new techniques and, sometimes, if we're lucky even new band allocations. The fundamental motivation of the designer/engineer is in itself to invent and produce new things.

Engineering is a very wide discipline, not only in the breadth of the subject (mechanical, electronic, chemical etc) but also in time. It is as old as human society itself and has been practiced in some form or other throughout history. A fine definition of engineering I recently heard was "absolutely everything that doesn't involve starving in a cave". It is useful to remember that this gives us thousands of years of development and prototyping to examine, be inspired by and to draw from.

It is far too easy to become fixated only on the cutting edge of our technological endeavour. In electronics this shows as greater levels of integration and more extreme levels of abstraction from the fundamental circuitry. While this has facilitated amazing leaps forward in technological capability over the past decades, a resourceful engineer can achieve better results by casting an eye back over the methods used by previous generations now and again, and using some of these concepts and ideas to complement our more usual, modern methods.

All very worthy sounding, but where does this actually have any practical applications in current day design? Some examples should clarify the matter:

1. Especially applicable to low power wireless, study of the text books and circuit manuals of the nineteen fifties, sixties and seventies (such as the RSGB and ARRL handbooks) can unearth some absolute circuitry gems: this was a time when it was simply not possible to solve a design problem by throwing silicon at it. Techniques like neutralisation, and many of the less "standard" LC filter topologies, are still highly useful now.

> *A resourceful engineer can achieve better results by casting an eye back over the methods used by previous generations, now and again*

2. When designing logic or switching circuitry, remember the DTL and RTL techniques that preceded today's integrated CMOS logic. At low speeds a couple of transistors or diodes can do the work of a much more expensive 74 series (or similar) package.
3. Look at the various functions we tend to implement in digital ASICs or in firmware (such as time delays and filters) and look back at the methods used to implement them in the past: when accuracy isn't of utmost importance, a simple RC network is still often the best method.
4. Always consider (at least briefly) the discrete circuit method of fulfilling a task before reaching for an integrated circuit. In low power RF design it is surprising how often an "old fashioned" circuit is either cheaper, offers better performance, or draws much less current.
5. Underlying fundamentals do not change. Good engineering practice (in terms of screening, grounding, EMC filtering, even mechanical assembly methods) is timeless, and historical study can remind us of good ways of doing these things, or occasionally bring a forgotten innovation back into use.

I am not intending to preach a Luddite agenda, nor am I nostalgically harking back to some imaginary bygone era when things were "better", but I am strongly of the opinion that the history of our technological advance still contains some useful tools for those of us working in the present.

I will let Isaac Newton have the last words: "If I have seen further it is by standing on the shoulders of giants."

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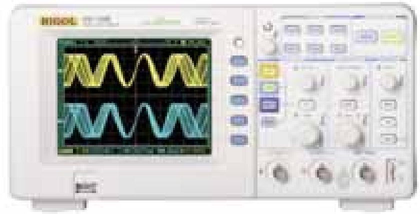

Telonic Instruments Limited are specialists for test and measurement equipment, laboratory power supplies, safety test instruments, RF filters and attenuators and custom test systems. Telonic have recently been awarded UK distribution of Rigol test and measurement equipment. To celebrate this new partnership Telonic are offering one lucky Electronics World reader a chance to win their flagship digital oscilloscope the Rigol DS1052E oscilloscope, worth £245+VAT.

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Legacy of consumer memory translates to a generation of problems

VICTORIA BARRETT, MARKETING DIRECTOR FROM NEXUS GB, POINTS OUT THE PROBLEMS RELATED TO THE USE OF CONSUMER MEMORY IN SPECIALIST AND INDUSTRIAL APPLICATIONS

A survey of design engineers conducted by portable memory specialist Nexus GB has shown that industry is overwhelmed by problems resulting from the use of consumer memory in specialist and industrial applications. Furthermore, Nexus believes that, if practices don't improve, these problems will only get worse as time passes.

Nexus surveyed just under a hundred design engineers, all of whom were working in a senior role in UK organisations. The participants were asked a series of non-leading multiple choice questions and the possible answers were displayed in random order with hundreds of potential combinations on each page.

A staggering 70% of respondents to the survey claim to have experienced problems due to one or more of three leading factors identified: obsolescence, lack of compatibility between products from different manufacturers and loss of data due to unreliable connectors.

> *A staggering 70% of respondents to the survey claim to have experienced problems due to one or more of three leading factors identified: obsolescence, lack of compatibility between products from different manufacturers and loss of data due to unreliable connectors*

SITA application

Independently, each of these leading factors affected 20-30% of those who took part in the study. Furthermore, these complications are all more likely to take effect the longer a product has been in circulation. As a result, Nexus believes that persistent inappropriate use of consumer style memory products in industry could create a legacy of technical challenges for forthcoming generations of design engineers to face.

Bad News

It's very bad news if one of these affects your company's product when it's launched, or within a couple of years of it being in production. However, things can get much worse if it kicks in further down the line, when you might find that a complete re-design is required. This could be due to a combination of obsolescence with another factor, such as changes in memory standards for example.

Rectifying the issue can become really expensive at that stage. It's far cheaper to start with a memory product in the first instance. Choosing a product which is fit for purpose could spare the cost of re-design at a later stage of the project.

The first thing to look for is memory that is guaranteed to work in your bespoke device. Although consumer memory may physically fit your application, it may not work for any one of a number of technical reasons. This takes away the most compelling reason to use consumer memory – its widespread availability.

Unsurprisingly, when asked whether they have experienced problems with the low mated lifecycle of consumer memory products and their associated connectors, a sizeable portion of respondents indicated 'cost and down time' were the most frequent issues. The second most common answer illustrates the price of human error; there

Klixkey application

have been cases when CF cards were inserted the wrong way up, which resulted in bent pins in the connector. Replacements can add up to a hefty bill for the end user.

Over 28% of the participants agreed that using consumer memory had resulted in problems with obsolescence, while 23% said they had experienced issues with loss of data due to unreliable connectors.

Choosing a controlled connector so that only approved products fit is perhaps the best way to resolving the issue. If you design in USBs or camera cards, users can plug in untested and unqualified consumer memory. This isn't the case with a specialist memory key or token.

Incompatibility between products from different manufacturers created difficulties for 22% of respondents, while theft of the memory product itself has been a problem for 10% of the designers surveyed. This point highlights the fact that there are cases where secure and rugged industrial memory can find a home in an application where one might usually use a high-street USB stick. Just think about the cases of government departments who have lost crucial client data over the last couple of years by moving it around the country on a CD, memory card or USB!

Memory Standards

Changing memory standards have surprisingly created few crises, perhaps because of the number of machines that are now built on a 'fit and forget' basis; only 8.5% of participants claimed this had affected them. History shows that USB and SD 'standards' are driven by the consumer market and changes can adversely affect embedded OEMs who adopt the products. For instance SDHC cards use a different addressing method to SD cards, meaning embedded devices using SD can't also use its successor, even though they fit in the connector.

Using the right form-factor can give additional benefits. It can discourage theft, because USB drives and SD cards can be taken by employees, but a stock design from a specialist portable memory supplier cannot. If there is the possibility of product or data theft in your application, this should be an important consideration.

Although our survey has turned up some shocking figures, they wouldn't be surprising for anyone in the industrial memory sector. Accounts from Nexus GB's customers over the years have illustrated quite a few of the problems highlighted by the survey. For example, we were once contacted by a client the day they launched their own product because, on that very same day, they had received a letter from the consumer memory manufacturer requesting a 'last time buy' order before production ceased. Sadly, in the consumer memory world, Moore's Law makes this situation inevitable.

According to the idea outlined by Gordon Moore in 1965, computer chips double their output every eighteen months. This is true of consumer memory, where the need to store and play increasingly large files such as high-resolution photographs, films and games means that we demand a huge capacity from the USB on our key ring. It's not surprising that consumer applications quickly outstrip industrial ones – it can often take an OEM eighteen months to get a project from drawing board to production line.

When one summarises the issues our survey highlighted, it's easy to see why electronics is an industry beset with memory problems. After all, the reason we are designing memory into the application in the first instance is the data or functionality that the memory device contains. The device itself is secondary to the ultimate function, which makes it ironic that the use of consumer memory can create so many issues, while the stress-free alternative of industrial memory often remains in the shadows. ●


Datakey and receptacle

Nexus GB is the UK and Ireland exclusive distributor for US manufacturer Datakey Electronics's range of portable, rugged keys and tokens containing non-volatile memory. These reliable and re-programmable items provide data transport, security and access control solutions even in extreme environments where other methods, such as USB memory, would not survive. Furthermore, distinct from consumer-like memory solutions, they are a well-established product that will not become obsolete as technology progresses. As a result, they are commonly used by design engineers working on long-term projects, with more than three million units currently in UK service

MEASURING LOUDSPEAKER IMPEDANCE

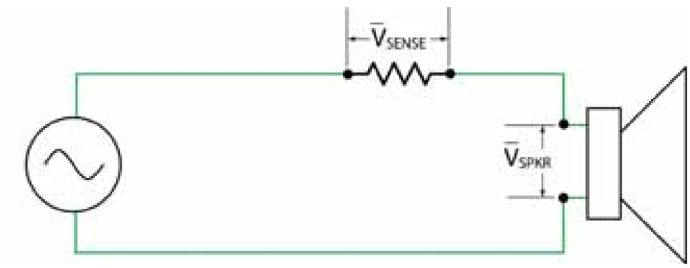

Figure 1: Schematic of loudspeaker impedance test

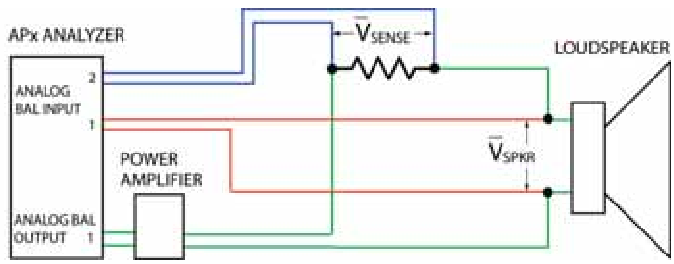

Figure 2: Connections

AUDIO PRECISION'S DIRECTOR OF TECHNICAL SUPPORT **JOE BEGIN** CONSIDERS HOW TO ACCURATELY TEST LOUDSPEAKER IMPEDANCE USING THE CONSTANT VOLTAGE METHOD

As anyone who's tried to measure the impedance of a loudspeaker knows, it's not a simple matter of getting out a multimeter – that just gives the DC resistance of the speaker coil. Impedance must be measured across the entire audio frequency band and, with a typical loudspeaker driver or multi-driver system, it can vary widely with frequency due to the various electrical and mechanical properties of the drivers, crossovers and cabinet.

> Measuring loudspeaker impedance by the constant voltage method means that the voltage across the loudspeaker terminals will stay relatively constant across the frequency range, regardless of speaker impedance fluctuations

A plot of loudspeaker impedance can reveal valuable information to a designer, such as the resonant frequency of a driver and the type of load a loudspeaker will present to an amplifier. On the production line, deviation from the impedance curve of a "golden unit" can indicate a defective or out-of-spec driver.

Speaker impedance can be measured using the constant voltage or constant current methods. The constant voltage method, which we'll describe in this article, best represents actual operating conditions, although it requires use of an external power amplifier and sense resistor. The constant current method doesn't require this extra hardware, making it an attractive alternative for use on a production line.

The Constant Voltage Method

Measuring loudspeaker impedance by the constant voltage method means that the voltage across the loudspeaker terminals will stay relatively constant across the frequency range, regardless of speaker impedance fluctuations. This allows testing to be done at a specific speaker voltage level, and by running the test multiple times at different levels, it can be determined if the impedance curve is level-dependent.

Figure 1 shows a basic schematic of the constant voltage method, while Figure 2 shows the actual connections. Two analyzer inputs (analog balanced) are used to make the measurements: One channel measures voltage across the sensing resistor (Vsense) and the other measures voltage across the speaker (Vspkr). The power amplifier provides the ultra-low output impedance and high current necessary to drive low-impedance speaker loads. While the analyzer can be used to drive the speaker directly, some combinations of output voltage and speaker impedance may exceed its maximum output current. In addition, the

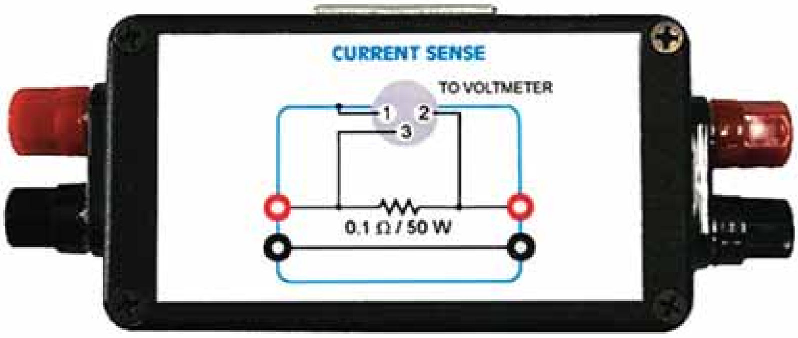

Figure 3: Current sense test jig

minimum 50Ω output impedance of the analyzer feeding a speaker creates a current source, defeating the main advantage of the constant voltage method.

Testing, Testing

To make the connections easier, I constructed a measurement test jig that contains a 0.1Ω 50W current sense resistor (see Figure 3). This jig has dual banana binding posts on each end and an XLR connector on the side, which makes for easy connections to the audio analyzer, the speaker and the amplifier. The jig shown is one of a kind, but you can easily construct one yourself.

The value of the sense resistor is not critical, but it should have reasonable precision (say 1%) and a sufficient power rating. A value of 0.1Ω is a good choice, because it does not significantly compromise the low output impedance of the constant-voltage source, and a division by 0.1 (or multiplication by 10) is convenient.

Four-terminal current sense resistors are available for use in a Kelvin configuration, in which the current is supplied through two opposing terminals and the sensing voltage is measured across the other two terminals. In addition to offering more convenient connections, the 4-wire Kelvin configuration provides more accurate sensing measurements. Examples include the Ohmite 10 series and the Riedon UAL series.

Deriving the Result

Based on the circuit in Figure 1, the current (i) is derived from the equation:

$$\bar{i} = \frac{\bar{V}_{sense}}{R_{sense}}$$

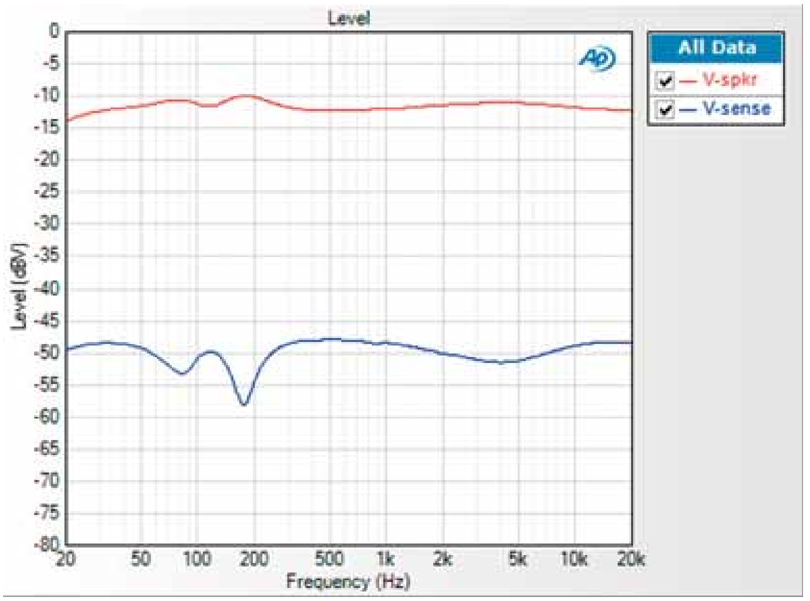

Figure 4: The level measurement (primary) result

Figure 5: Intermediate result for impedance magnitude

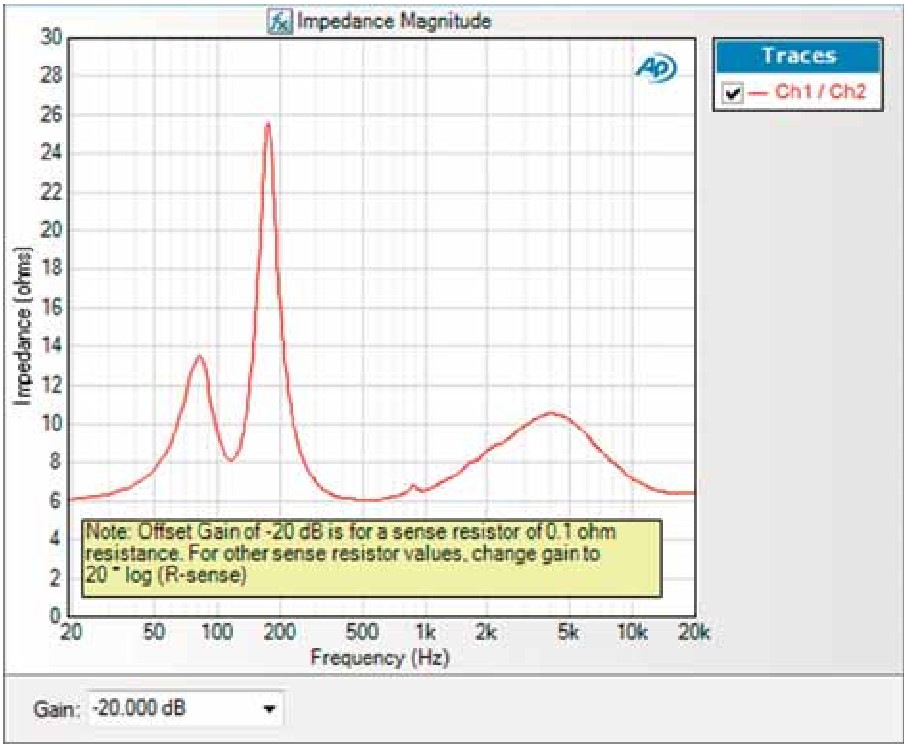

Figure 6: Impedance magnitude (derived)

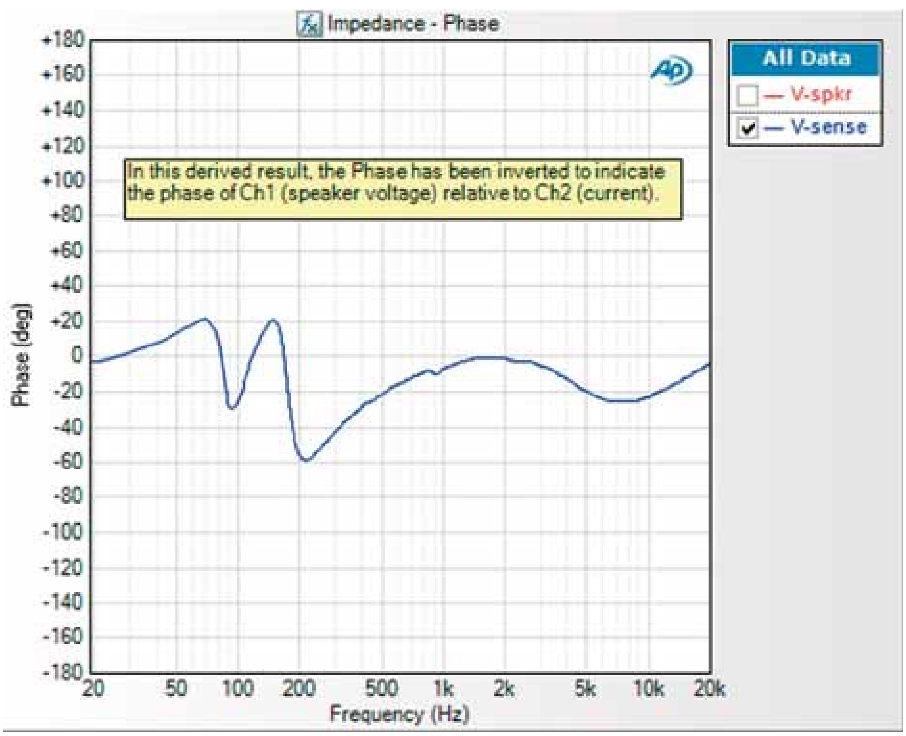

Figure 7: The relationship between impedance, phase and frequency

and the impedance can be derived from:

$$\bar{Z} = \frac{\bar{V}_{spkr}}{\bar{i}}$$

Combining the above two equations yields:

$$\bar{Z} = \left(\frac{\bar{V}_{spkr}}{\bar{V}_{sense}}\right) R_{sense}$$

In the equations above, the bar above i, V and Z denotes that they are phasor quantities (i.e. they have both a magnitude and phase).

In Figure 4, the impedance is derived from the level result in the acoustic response measurement. In practice, any frequency response measurements could be used; acoustic response was chosen because it is fast on the AP analyser used for this project, and allows multiple averages to be taken. As shown, the input channels have been re-labeled in signal path set-up to Vspkr and Vsense, for convenience.

To get the impedance magnitude (Figure 6), we first use an intermediate derived result named Z Mag – intermediate (Ch1/Ch2), see Figure 5. This is a compare-derived result, and simply divides Ch1 by Ch2 (Vspkr/Vsense). Next, we use an offset derived result to multiply the intermediate derived result by Rsense. In this case, we need to multiply the result by 0.1Ω. A multiplication by 0.1 is equivalent to an offset of -20dB. Hence a gain of -20dB was applied to the offset operation as shown in Figure 6. If other values of Rsense are used, the gain for this offset operation should be set according to the equation:

$$Gain\ (dB) = 20\log(R_{sense})$$

Finally, to get the impedance phase (Figure 7), we used an invert derived result on the primary phase result. This is to correct for the fact that the primary phase result is the phase of channel 2 relative to channel 1, and in this case we want the phase of the speaker voltage (channel 1) relative to the current (channel 2). Alternatively, we could have just swapped the two measurement channels and this invert operation would not have been required. ●

MOBILE HANDSET AUDIO PERFORMANCE

IN THIS ARTICLE, GREG DAVIS, SENIOR MARKETING MANAGER FOR SIGNAL CONDITIONING PRODUCTS AT FAIRCHILD SEMICONDUCTOR, ADDRESSES THE MOBILE PHONE'S AUDIO PLAYBACK FACILITY AND, SPECIFICALLY, THE MP3 PLAYER AUDIO OUTPUT TO HEADPHONES

The mobile phone market continues to evolve from mainly voice communications devices to sophisticated organizational and entertainment appliances. With the arrival of smartphones users enjoy feature-rich portability, such as integrated MP3 players, video playback, cameras, Bluetooth connectivity and GPS among others – all with a touchscreen interface. Additionally, multitasking operating systems have arrived with seemingly limitless applications, resulting in powerful portable devices with the smartphone being one such great example.

Hi-Fi Wanted

Along with all of the smartphones' functionalities, users expect high performance and, especially, an excellent audio performance. Whilst listening to music or movies in high fidelity is welcomed, there can be some undesirable elements spoiling the experience, such as power supply noise, harmonic distortion, crosstalk and data compression; if not designed carefully, the audio IC headphone amplifier and the system surrounding it can also be a major noise contributor.

The key parametric in amplifier noise is the signal to noise ratio (SNR). Higher SNR results in higher audio quality, while low SNR results in a noisier output.

Every audio output has a 'noise floor', the inherent noise of the system and audio ICs. Best board-layout practices can help reduce the noise floor, as can optimized IC designs. The goal is to maintain as much difference between the amplitude of the noise floor (undesirable content) and the music (desired content). Noise is most obvious during quiet passages between songs, or when playing content with high dynamic range, where the difference between louder and quieter passages is higher, as in classical music for example. SNR is a ratio of desired content to undesired content. From an analytical standpoint, the equation is a ratio expressed on a logarithmic scale due to the vastly different amplitudes of the noise floor and desired signal:

$$SNR_{dB} = 10\log_{10}\left(\frac{P_{signal}}{P_{noise}}\right)$$

where P_{signal} is the average power of the desired signal (music) and P_{noise} is the average power of the noise floor.

Expressed as voltage:

$$SNR_{dB} = 10\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)^2 = 20\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)$$

where A is the root mean square (RMS) voltage of the signals.

In audio IC design, there is often a reference used for A_{signal}, which is the maximum output level the amplifier can deliver a 1kHz sine wave into a 32Ω load at 1% total harmonic distortion + noise (THD+N). Note: some manufactures spec A_{signal} under a no-load condition or at a higher THD+N to artificially elevate the SNR spec.

Associated SNR

All IC amplifiers have an associated SNR depending on their design and layout. These amplifiers power external headphones when listening to music on a mobile handset. Considering that that data that makes up the media is already highly compressed (usually MP3, AVI, or MOV formats), then why is there a requirement for SNR of 100dB and above for headphone amplifiers; this is even higher than a CD which has a theoretical SNR of 96dB?

First, data compression and noise are two distinctly different components of audio degradation. Data compression is based on lossy algorithms that reduce file size by eliminating or masking portions of content that are not easily heard by the human ear. Lost content as a result of data compression cannot be recovered. Further, noise that is inherent in the original recording cannot be reduced either. However, the noise that is added by the handset design, including the headphone amplifier IC, can be reduced.

The specified SNR of an amplifier is measured in the lab with a fixed numerator (A_{signal}) value. It is important to note it is not a typical listening level. For example, many IC headphone amplifiers are capable of churning out over 30mW into 32Ω. If turned up that loud, you can hear the earbud from across a room!

In reality, due to the close coupling of the eardrum to the earbud inserted in the ear canal, a reasonable listening level is in the range of 0.1mW – 0.5mW into 32Ω, depending on the efficiency of the earbuds. This is only a fraction of the full output power. Because SNR is the ratio of the signal to noise, and since the noise floor does not change, using these realistic listening levels lowers the apparent SNR to the listener.

> The specified SNR of an amplifier is measured in the lab with a fixed numerator value; it is important to note it is not a typical listening level

As an example, an amplifier is specified at 105dB SNR using an A_{signal} 1kHz tone at

$30mW_{RMS}$ into 32Ω with 1% THD+N. First convert $30mW_{RMS}$ to V_{RMS}:
$P_{RMS} = (V_{RMS})^2/R$
or $V_{RMS} = \text{sqrt}(P_{RMS} \times R) = \text{sqrt}(0.03W_{RMS} \times 32\Omega) = 0.979\ V_{RMS}$
We now calculate A_{noise} using the equation:

$$SNR_{dB} = 10\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)^2 = 20\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)$$

So $105dB = 20\log_{10}(0.979V_{RMS}/A_{noiseRMS})$
Or inv-$\log_{10}(105dB/20) = 0.979V_{RMS}/A_{noiseRMS}$
so $A_{noise} = 5.5\mu V_{RMS}$
Or this can be calculated as:
$105dB/20 = \log_{10}(0.979V_{RMS}/A_{noise})$
Or $10^{105dB/20} = 0.979V_{RMS}/A_{noiseRMS}$
Or $A_{noise} = 0.979\ V_{RMS}/10^{105dB/20} = 5.5\mu V_{RMS}$

Now that we know the noise floor A_{noise}, let's determine the SNR using the same amplifier, under the same conditions, at a typical listening level of $0.1mW_{RMS}$. Again, using the equation:

$$SNR_{dB} = 10\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)^2 = 20\log_{10}\left(\frac{A_{signal}}{A_{noise}}\right)$$

first convert $0.1W_{RMS}$ to V_{RMS}:
$P_{RMS} = (V_{RMS})^2/R$
or $V_{RMS} = \text{sqrt}(P_{RMS} \times R) = \text{sqrt}(0.001W_{RMS} \times 32\Omega) = 0.179V_{RMS}$
Now calculate the new SNR:
$SNRdB = 20\log_{10}(0.179V_{RMS}/5.5\mu V_{RMS}) = 90.24dB$. Note this is about 15dB less at typical listening level.

SNR measurements are a key indicator of the quality of an audio amplifier. Given that users now expect the same audio quality as found on MP3 players, special attention must given to this important specification. ●

THE SAFE OPERATING AREA (SOA) PROTECTION OF LINEAR AUDIO POWER AMPLIFIERS

MICHAEL KIWANUKA GIVES A DETAILED ACCOUNT OF OVER-VOLTAGE AND OVER-CURRENT PROTECTION FOR POWER SEMICONDUCTORS IN AUDIO POWER AMPLIFIERS

The desirability, or lack thereof, of over-voltage and over-current protection for power semiconductors in audio power amplifiers remains a point of contention in the field [1]. For example, some designers [2] appear to recommend multiple-transistor complementary output stages, as often mandated by high-power class-A operation, to circumvent the need for SOA protection of bipolar devices. Others [3] suggest that such voltage-current (alias V-I) limiters may be dispensed with altogether by merely adopting enhancement-mode power MOSFETs (hereinafter e-MOSFET).

These views appear to be rather more widely accepted than they should and constitute a charter for near heroic unreliability in amplifiers so designed, as even a momentary short to ground can destroy an expensive output stage.

The zener diode-clamping of the gate-source voltage of e-MOSFETs is thought by some [4,5] to be all that is required in regard to protection. While the zener diodes are mandatory (ideally with $10V < V_{zener} < 20V$ to prevent premature clamping), they only serve to protect the e-MOSFET's gate oxide insulation from over-voltage destruction [6] and do nothing to protect the device from accidental short circuits and forbidden voltage-current combinations that may occur when the amplifier is called upon to drive reactive loads.

The positive temperature coefficient of on-resistance [7] and, therefore, negative temperature coefficient of drain current, enjoyed by e-MOSFETs eliminates the secondary breakdown phenomenon which is the bane of bipolar transistors, but does not constitute licence for wilful violation of power dissipation limits in linear audio-frequency applications.

This is in contrast to ultrasonic switching usage, where e-MOSFET dissipation bounds may be blissfully ignored and adherence to drain current and drain-source voltage limits will suffice.

All output stage semiconductors used in complementary or quasi-complementary (full or half bridge) linear audio power amplifiers – without exception – require SOA protection for reliable operation. However, such circuitry must be carefully designed to prevent premature activation during normal amplifier operation.

Single Slope Linear Foldback Limiting

Many low to medium-power (sub-200W into 8Ω) commercial audio amplifiers incorporate a single slope linear foldback voltage-current protection circuit (Figure 1) attributed to S.G.S. Fairchild Ltd by Dr A.R. Bailey [8]. In practice, the complimentary output transistors T_{01} and T_{02} may each consist of a compound arrangement of at least two transistors in series.

The instantaneous collector-emitter voltage v_{ce}

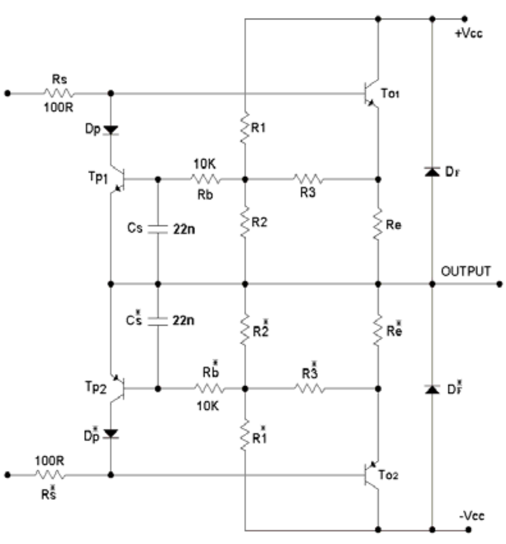

Figure 1: Improved version of Fairchild's single slope linear foldback protection circuit applied to a complementary output stage

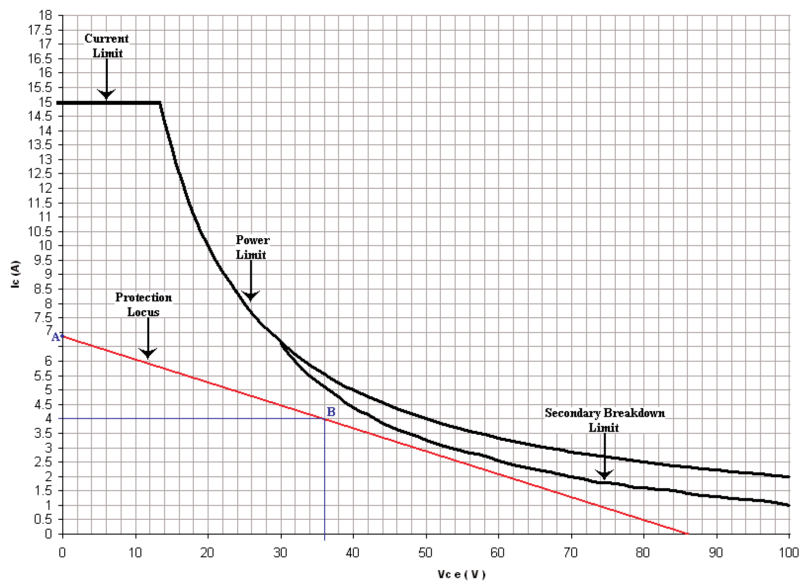

Figure 2: Safe operating area of On Semiconductor's MJL3281A; the single slope linear foldback protection locus is drawn to intersect the Vce-axis at a value greater than 2 | V_{cc} | to prevent premature limiting

across T_{O1} is sensed by R1, R2 and R3, while the output current, expressed as a voltage across emitter resistor R_E, is simultaneously monitored by R2 and R3. Thus, these voltages are summed algebraically at the base of protection transistor T_{P1} which is driven into conduction shunting voltage drive to T_{O1} in the event of an over-voltage, over-current or simultaneous occurrence of both conditions in the output device.

The series resistor R_S (typically $100R \le R_S \le 2K2$) expedites this process by limiting the current required by T_{P1} to shunt voltage drive to T_{O1}. The freewheeling diode D_F protects the output device from excessive base-emitter reverse bias, due to beyond-rail voltage spikes generated when SOA protection is invoked with inductive loads, while D_P performs the same function for the small-signal protection transistor T_{P1} by preventing its base-collector junction from being forward biased [5].

If the amplifier's output approaches the negative supply rail while driving a sufficiently low impedance, the current sunk by T_{O2} generates an appreciable voltage drop across its emitter resistor R_E^*; the output is then at an appreciably higher potential than the common input to the complementary output stage. Consequently, transistor T_{O1} is reverse biased and T_{P1}'s base-collector junction, in the absence of its collector diode D_P, would be forward biased, causing current to flow from emitter to collector.

Diode D_P prevents this form of spurious inverse-active mode limiter activation by decoupling T_{P1}'s collector as T_{O1}'s base-emitter junction is reverse biased. The potential at T_{O1}'s emitter is then equal to the output voltage since T_{O1} is non-conducting and, contrary to Duncan[10], only negligible leakage current flows through its emitter resistor R_E. By symmetry the explanation above also applies to the negative half of the circuit.

A small-value capacitor is sometimes connected across the base-collector junction of each protection transistor [1] with a view to eliminating oscillation that occurs in the network during the limiting process. These capacitors appear in parallel at AC and are entirely unsatisfactory, as they create an ill-defined and, therefore, undesirable feedfoward path around the output stage, shunting it out of the global feedback loop at high audio frequencies, precisely where the amplifier is most vulnerable with respect to non-linearity.

Such vulnerability is due to a necessarily diminished feedback factor at high audio frequencies in the interest of Nyquist stability. Connecting the capacitor across the base-emitter junction of each protection transistor is the preferred solution.

Series base resistors R_b and R_b^* (of the order of 10K) are also recommended for each protection transistor. These base ballast resistors make for better controlled activation of the protection transistors by damping anomalous voltage spikes otherwise provoked by these transistors being overdriven.

Additionally, the single pole low-pass filters, comprising ballast resistors R_b, R_b^* and shunt capacitors C_S and C_S^*, prevent activation of the protection transistors at ultrasonic frequencies where such protection is unnecessary. For typical values, the source impedance of the protection circuit (referred to the base of each protection BJT) may be deemed negligible, compared to the value of the ballast resistor. For brevity, diodes D_F, D_F^*, D_P, D_P^*, base-emitter shunt capacitors C_S, C_S^* and ballast resistors R_b, R_b^* are omitted in all subsequent figures.

The values of R_b and C_S shown in Figure 1 provide 6dB of attenuation at approximately 1kHz. This is roughly equivalent to doubling the permissible power dissipation per output device at this frequency.

The filter's nominal time constant may not exceed 500µs with bipolar output transistors, as the filter is required to partially damp the oscillation that occurs during limiting and not completely eliminate it. This is because this oscillation is intrinsic to the circuit's operation. For instance, if the amplifier's output swings are positive during persistent SOA overload (such as a continuous short-circuit to ground or negative supply rail), protection transistor T_{P1} is driven forward-active, cutting off output transistor T_{O1}. The fault is therefore removed with respect to T_{O1} and protection transistor T_{P1} is promptly disabled. This in turn causes the instantaneous recurrence of the overload condition and attendant reactivation of T_{P1}. The on-off action of the protection transistor in these circumstances appears as persistent local high frequency oscillation which, contrary to popular opinion, has nothing to do with the stability of the protection circuit or, indeed, the amplifier's major feedback loop.

The resistor values for the arrangement of Figure 1 are obtained by drawing the desired protection locus on a linear-linear scale graph of the output transistor's DC safe operating area (Figure 2). One of the three resistors (usually R3) is assigned an arbitrary value (typically $100R \le R3 \le 1K$), and the two remaining resistors evaluated from simultaneous equations developed from two convenient points on the protection locus.

With this arrangement, it is essential that the linear protection locus intersect the SOA's Vce axis at a value greater than the sum of the moduli of the amplifier's voltage supplies; otherwise T_{P1} turns on under normal loading when the output swings negative, even with the output open-circuit. Similarly, T_{P2} would be activated under normal output loading when the output swings positive. This effectively short-circuits the "small signal" circuit preceding the output stage directly to the output, causing gross distortion.

Failure to adhere to the above condition appears to have caused some designers to erroneously abandon electronic SOA protection

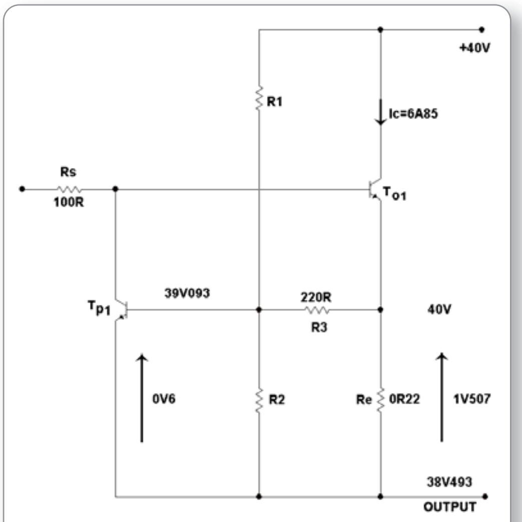

Figure 3: Output conditions at point A on the protection locus of figure 2

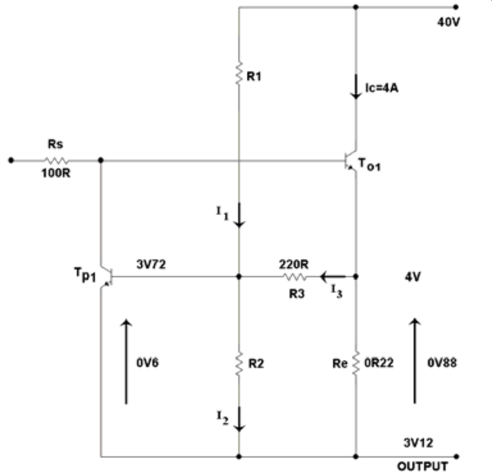

Figure 4: Output conditions at point B on the protection locus of figure 2. The contribution of I_3 to the current in Re is negligible

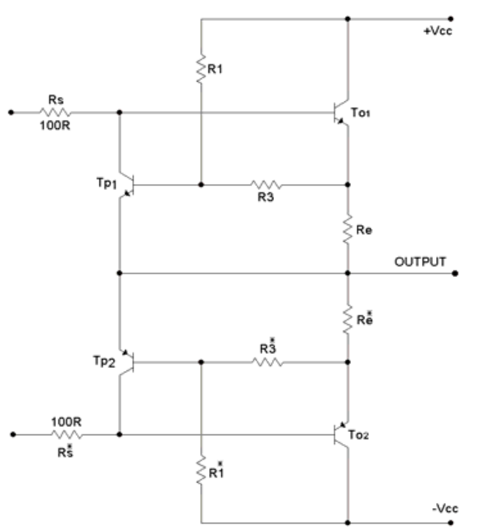

Figure 5: Compromised single slope linear foldback scheme gives grossly inefficient SOA utilisation

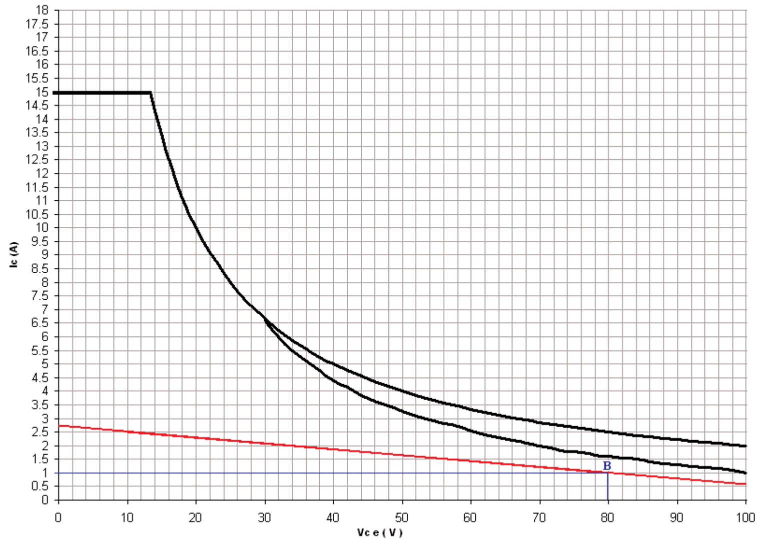

Figure 6: Linear protection locus clearly shows the inflexibility of the scheme of figure 5

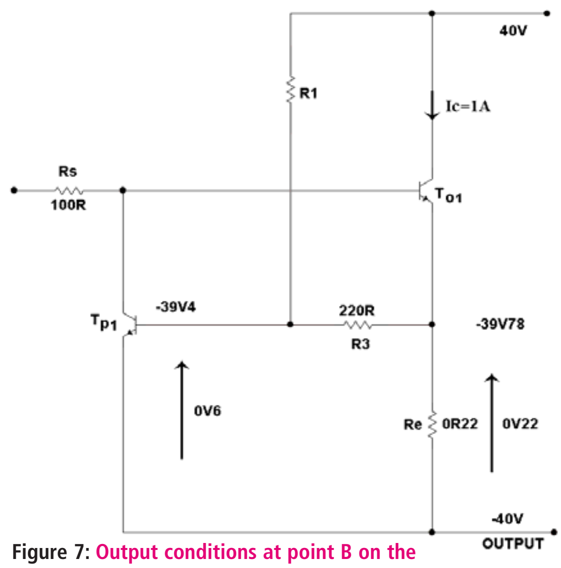

Figure 7: Output conditions at point B on the protection locus of figure 6

of any form altogether[1,12]. However, this requirement presents a significant impediment to the efficient utilisation of the comparatively large SOA in the low-Vce region of the graph. This is especially true of amplifiers with relatively high supply-rail voltages where in the case of bipolar transistors secondary-breakdown severely curtails flexibility in optimal placement of the protection locus.

This is graphically illustrated in Figure 2 for an amplifier with nominal ±40V supply rails, and using On Semiconductor's excellent[13] 200W MJL3281A-MJL1302A complementary power transistors. Note that although the datasheet SOA of 200W for these devices is used here for brevity, this is specified at a device case temperature $T_C = 25^\circ C$. The later is only achievable with an improbable heat sink of infinite dimensions. In practice, the datasheet SOA should be adjusted (viz. "derated") to accommodate the transistor's steady-state case temperature with the designer's selected heat sink.

Only the positive half of the circuit of Figure 1 need be used to calculate the required passive component values (Figure 3). Ideal active devices are assumed, with infinite input impedance, zero saturation voltage and zero ohmic resistance. The error thus accrued is negligible, provided small-signal transistors of high current-gain $(\beta \approx 100)$ are used. Let V_{be} = 0V6, R_3 = 220R and Re = 0R22.

Taking two arbitrary points A and B on the locus where at point A Ic = 6.85A, Vce = 0V, and at point B Ic = 4A, Vce = 36V, it follows from Figure 3:

$$0.6 = \frac{1.507\mathbf{R}_2}{\mathbf{R}_2 + \mathbf{R}_1 220/(\mathbf{R}_1 + 220)} \qquad (1)$$

With reference to Figure 4 and noting that the contribution of I_3 to the current in $\mathbf{R}_e$ is negligible:

$$\mathbf{I}_2 = \mathbf{I}_1 + \mathbf{I}_3 \qquad (2)$$

$$\Rightarrow$$

$$0.6/\mathbf{R}_2 = (40 - 3.72)/\mathbf{R}_1 + (4 - 3.72)/\mathbf{R}_3$$

$$\Rightarrow$$

$$0.6 = \mathbf{R}_2(36.28/\mathbf{R}_1 + 0.28/220) \qquad (3)$$

Solving (1) and (3) simultaneously gives $R_1 \approx$ 12K4 and $R_2 \approx$ 143R0. For enhanced accuracy it is recommended that these values be made up from series or parallel combinations of 1% resistors where necessary. When the output swings to -40V, then 80V appears across R_1 in series with $\mathbf{R}_2 // \mathbf{R}_3$ to a good first approximation. Thus, the voltage present at the base of the protection transistor T_{P1} is given by:

$$\mathbf{V}_{be} \approx \frac{80(\mathbf{R}_2 // \mathbf{R}_3)}{(\mathbf{R}_2 // \mathbf{R}_3) + \mathbf{R}_1} \approx 0V55$$

Therefore, it follows that spurious activation of T_{P1} cannot occur if instantaneous collector current i_c is less than the maximum permissible collector current $I_{C(MAX)}$ at $v_{ce} \approx 2|V_{cc}|$. A general expression that facilitates the rapid verification of the compliance of any amplifier using single slope linear foldback limiting may be developed:

$$\left|\frac{2\mathbf{V}_{cc}(\mathbf{R}_2 // \mathbf{R}_3)}{\{(\mathbf{R}_2 // \mathbf{R}_3) + \mathbf{R}_1\}}\right| < \mathbf{V}_{be}$$

$$\Rightarrow$$

$$\left|\frac{2\mathbf{V}_{cc}\mathbf{R}_2\mathbf{R}_3}{(\mathbf{R}_2\mathbf{R}_3 + \mathbf{R}_1\mathbf{R}_2 + \mathbf{R}_1\mathbf{R}_3)}\right|_{T_A = 25^\circ C} < 0V6 \qquad (4)$$

Equation 4 is true only at an ambient temperature T_A of $25^\circ C$ as the threshold voltage of the protection transistors may be expected to drop roughly 2mV per degree Celsius increase in temperature. Further, Equation 4 is valid subject to the following condition:

$$i_C < I_{C(MAX)}\Big|_{v_{ce} \approx 2|V_{cc}|} \qquad (5)$$

This condition is invariably fulfilled during normal operation as no practical loudspeaker system would demand that the output transistor sustain $v_{ce} \approx 2|V_{cc}|$ while providing any appreciable current.

Figure 5 shows a common variation[10,11,13,14] on the single slope linear foldback limiter of Figure 1, with resistor R_2 excised so that from Equation 4:

$$\left|\frac{2\mathbf{V}_{cc}\mathbf{R}_3}{\{\mathbf{R}_3 + \mathbf{R}_1 + (\mathbf{R}_1\mathbf{R}_3/\mathbf{R}_2)\}}\right| < 0V6$$

Since $\mathbf{R}_2 \to \infty$ then:

$$\left|\frac{2\mathbf{V}_{cc}\mathbf{R}_3}{(\mathbf{R}_3 + \mathbf{R}_1)}\right|_{T_A = 25^\circ C} < 0V6$$

The optimal protection locus for this network (Figure 6) must be plotted so that calculated resistor values comply with the above condition. This scheme is atrociously inefficient, as for a nominal $V_{ce} \approx 0V$ and Re = 0R22, resistors R_1 and $\mathbf{R}_3$ are in parallel and, of necessity, the collector current i_c is prematurely limited to:

$$\left\{\mathbf{I}_c\big|_{V_{ce} \approx 0V} < (\mathbf{V}_{be}/\mathbf{R}_e \approx 2A7)\right\}$$

A value of Re = 0R1 gives a modest improvement, with $\left\{\mathbf{I}_c\big|_{V_{ce} \approx 0V} < (\mathbf{V}_{be}/\mathbf{R}_e \approx 6A0)\right\}$. Clearly claims[13] of "load-invariant" drive capability made for power amplifiers using this scheme are rather premature.

The protection locus is realised by deriving output stage conditions (Figure 7) at a single arbitrary point B on the locus subject to:

$\{0 < \mathbf{V}_{ce} < 2|\mathbf{V}_{cc}|\}$. With $\mathbf{V}_{cc} = 40V$, Re = 0R22, R_3 = 220R and noting that R_1 and R_3 constitute a simple voltage divider, then:

$$R_1 \approx \frac{(40+39.4)}{(-39.4+39.78)/220R} \approx 46K$$

This unwarranted dependence on the value of Re is unacceptable as in some applications, such as output stages comprising paralleled complementary e-MOSFET pairs, $(0R1 < R_e \le 1R0)$ may be required to guarantee equable current sharing.

Driving Reactive Loads

A clear appreciation of the nature of the amplifier's load is required to establish the bounds within which the SOA limiter must remain inactive. Figure 8 shows an ideal complementary emitter follower (in Electronics Workbench's Multisim Professional SPICE simulator[15]) used to drive the de facto standard $(8\Omega\angle 0^0)$ test load to ±40V supply rails.

The plots obtained in Figure 9 show that the voltage v_{ce} across T_{01} is precisely 180^0 out of phase with the current i_c it is required to source; the voltage across the device is a minimum when its collector current is at a maximum and conversely. Instantaneous power dissipation is merely the product of instantaneous device voltage and current; peak transistor dissipation $P_{d(max)} \approx 50W$ occurs twice in T_{01}'s conducting half-cycle, at half the peak load voltage $(v_{out}/2 \approx V_{cc}/2)$ and half the peak load current $i_{c(peak)}/2$.

Since the $(8\Omega\angle 0^0)$ load line resides well below the linear protection locus of Figure 10 (reproduced from Figure 2), it is clear that a single pair of MJL3281A-MJL1302A power transistors operating from ±40V rails will comfortably drive an 8Ω dummy load to clipping without invoking protection; however, this will certainly not be the case with loudspeaker loads, which are invariably reactive[16,17].

An amplifier with "high-fidelity" aspirations, intended to drive full-range multiple-transducer loudspeaker systems, including electrostatics, should at least be capable of driving a $(4\Omega\angle\pm 60^0)$ impedance without invoking SOA-protection.

A $(4\Omega\angle -60^0)$ impedance was devised in SPICE by driving a 2Ω0 resistor in series with a 45µ9441 capacitor at 1kHz with the ideal complementary emitter follower of Figure 8. The traces thus obtained (Figure 11) were used to plot the $(4\Omega\angle\pm 60^0)$ load line in Figure 10. Peak transistor dissipation $P_{d(max)} \approx 362W$ (with $\sim 39V_{(Peak)}$ across the load) occurs at $v_{ce} \approx 46.9V$ and $i_c \approx 7.7A$.

In other words (Figure 12), because current leads voltage in a capacitive impedance, transistor T_{01} (Figure 8) is required to source $i_c \approx 7.7A$ when the output swings away from the negative supply rail to $V_{out} \approx -6V$. Similarly, transistor T_{02} must sink $i_c \approx 7.7A$ when the output swings from +Vcc to $V_{out} \approx +6V$. Note that the crossover discontinuity in the output voltage characteristic (at $|v_{out}| \approx 35V$) now precedes zero voltage crossing by 60^0 (Figure 12); this is contrary to the popular view that the crossover

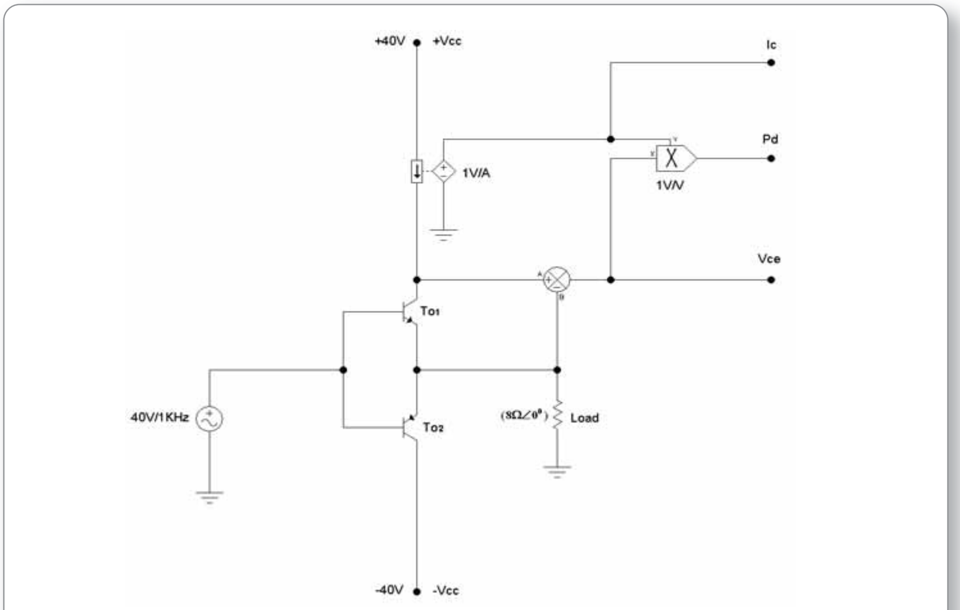

Figure 8: Ideal emitter follower used to determine instantaneous collector current i_C, collector-emitter voltage v_{ce} and device dissipation P_d

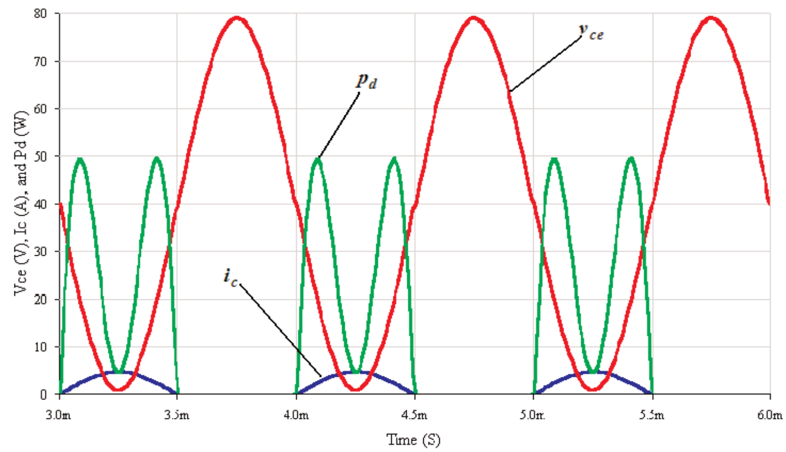

Figure 9: Instantaneous v_{ce}, i_C and P_d in sourcing output transistor while driving roughly 39V across an (8Ω<0º) load

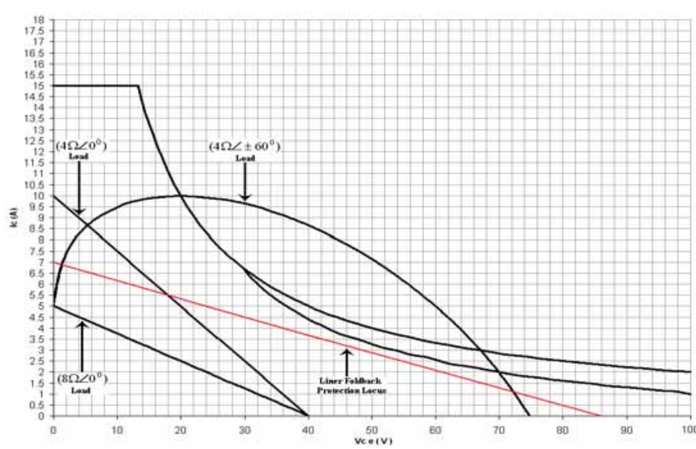

Figure 10: The reactive load gives an elliptical characteristic which causes more than seven times greater peak device dissipation than for the (8Ω<0º) case

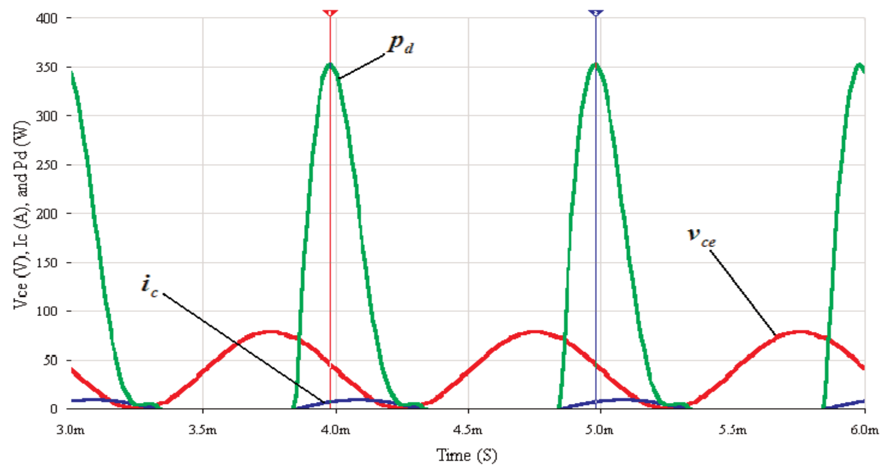

Figure 11: Instantaneous v_{ce}, i_C and P_d in sourcing output transistor T_{01} obtained by driving a (4Ω < –60º) load to a little under 40V $_{(Peak)}$

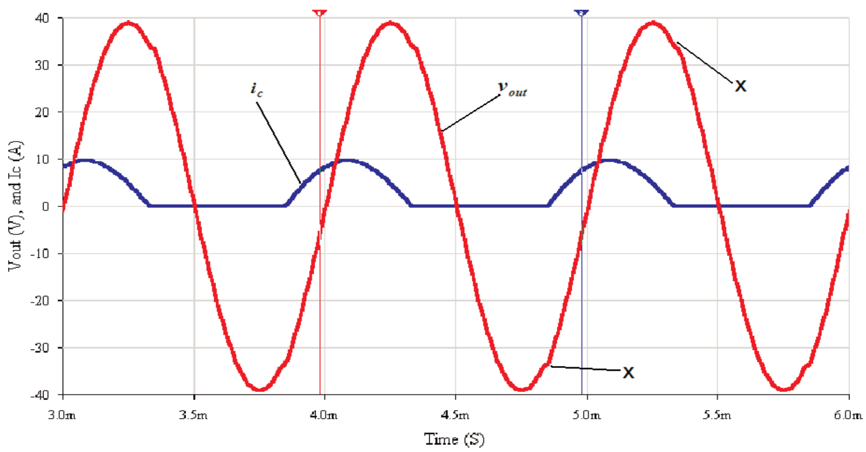

Figure 12: Transistor T_{01} delivers 7.7A to the (4Ω < –60º) load when the output voltage swings away from -Vcc to -6V. The crossover discontinuity marked X now precedes zero voltage crossing by 60º

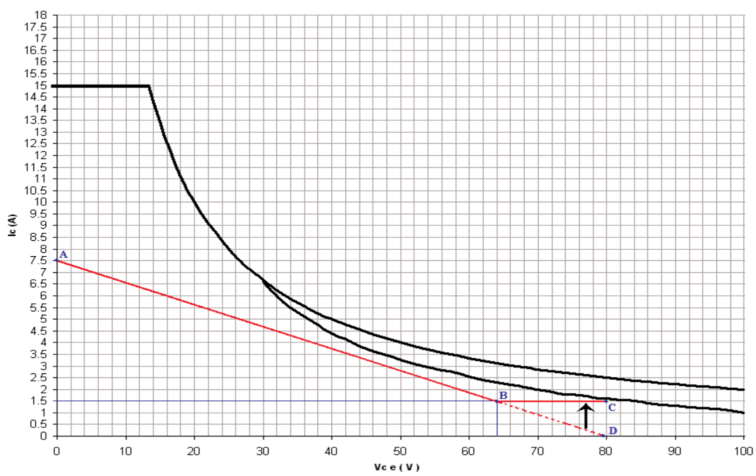

Figure 13: Single slope single breakpoint non-linear foldback protection locus

discontinuity is coincident with zero voltage crossing regardless of the nature of the load. With a $(4\Omega\angle+60^0)$ inductive impedance, in which current lags voltage, the output conditions are reversed, with the load demanding $i_c = 7.7A$ from T_{01} when the output swings from the positive supply to $v_{out} = -6V$. Regardless of the nature of the load, however, device voltage v_{ce} and load voltage v_{out} are always 180^0 out of phase and of course, being a voltage follower, the input voltage is always in phase with v_{out} at the frequencies of interest.

The linear foldback protection locus (Figure 10) only permits 3A at Vce = 46.9V; therefore, a minimum of three output pairs are required to drive a notional $(4\Omega\angle\pm60^0)$ loudspeaker system from ±40V supply rails without intrusive limiter activation. Note that this may need to be "derated" to four transistor pairs to accommodate realistic device case temperatures. On this basis, and using other established techniques[11,18] including mandatory DC offset and thermal overload protection systems, a reliable and versatile low distortion amplifier may be constructed.

As the cost of power transistors is significant, there is a compelling financial incentive to minimise the number of devices used by utilising the SOA as efficiently as possible. To this end, it has been suggested[10] that, ideally, the protection locus should closely match the bounds of the SOA. This is unnecessary as reactive load drive primarily requires that current delivery in the $|V_{cc}| \le v_{ce} < 2|V_{cc}|$ region be maximized without violating suitably derated DC safe operating limits. In general, as shall be demonstrated, an optimally located non-linear protection locus with at least one breakpoint should suffice.

Single Slope Single Breakpoint Non-Linear Foldback Limiting

Introducing a zero-gradient segment at some optimal point in the protection locus permits an increase in current delivery at the low-Vce end of the SOA without significantly compromising available current at higher device voltages (Figure 13). The single slope linear foldback protocol (Equation 4) is made redundant as the protection locus does not cross the Vce-axis at any point.

The zero-slope segment BC is realised by splitting R_1 in Figure 1 into R_{1A}, R_{1B} and clamping the voltage across R_{1B} and R_2 with zener diode D_1 (Figure 14) when $\{64V \le v_{ce} < (2|V_{cc}| - 80V)\}$. When $(0V \le v_{ce} < 64V)$, segment AB, the diode is off (virtually open-circuit) and the circuit reverts to a single slope linear foldback regime. This scheme was apparently introduced by Ruehs[20], but the algebra used to establish component values was incorrect.

The zener diode is disconnected and resistors R_{1A} and R_{1B} amalgamated into one resistor R_1 (Figure 15). As was the case with the circuit of Figure 1, component values are then established for the single-slope locus ABD at arbitrarily


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	Output Power	Output Voltage	Output Current (Max.)	Input Voltage Nom.	Input Voltage Range	Efficiency (Typ.)
Root Part No.	W	Vdc	A	Vdc	Vdc	%
ULT-3.3/7.5-D48	25	3.3	7.5A	48	36-75	85.5
ULT-5/5-D48	25	5	5A	48	36-75	89
ULT-12/2.5-D48	30	12	2.5A	48	36-75	91

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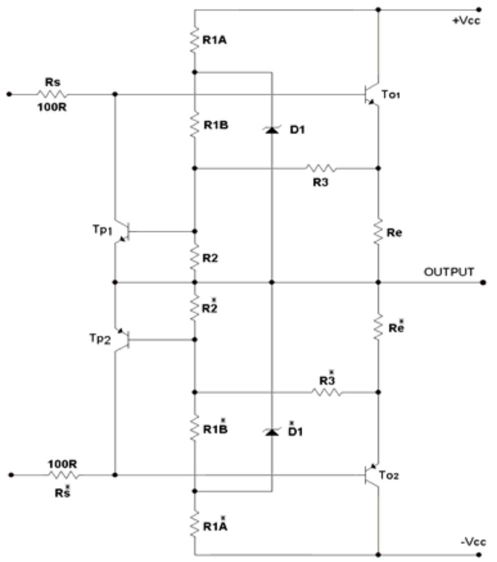

Figure 14: Single slope single breakpoint non-linear foldback protection cell applied to a complementary emitter follower

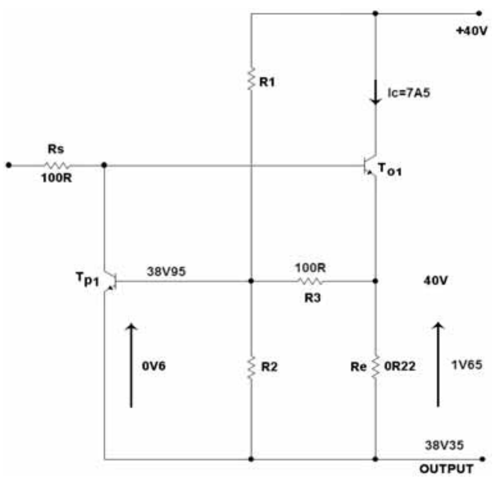

Figure 15: Output conditions at point A on the protection locus of figure 13

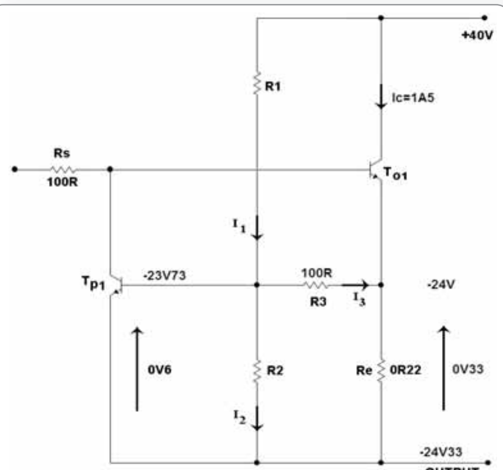

Figure 16: Output conditions at point B on the protection locus of figure 13. The contribution of I_3 to the current in Re is negligible

selected points A and B where at point A, Ic = 7.5A, Vce = 0V, and at point B Ic = 1.5A, Vce = 64V. With reference to Figure 15 and selecting $\mathbf{R}_1$ = 100R:

$$0.6 = \frac{1.65\mathbf{R}_2}{\mathbf{R}_2 + \mathbf{R}_1 100/(\mathbf{R}_1 + 100)} \qquad (6)$$

From Figure 16 and noting that the contribution of $\mathbf{I}_3$ to the current in $\mathbf{R}_e$ is negligible:

$$\mathbf{I}_2 = \mathbf{I}_1 - \mathbf{I}_3$$

$$\Rightarrow$$

$$0.6/\mathbf{R}_2 = (40 + 23.73)/\mathbf{R}_1 - (-23.73 + 24)/\mathbf{R}_3$$

$$\Rightarrow$$

$$0.6 = \mathbf{R}_2(63.73/\mathbf{R}_1 - 0.27/100) \qquad (7)$$

Solving (6) and (7) simultaneously gives $\mathbf{R}_1 = 4\mathrm{K}8$ and $\mathbf{R}_2 = 56\mathrm{R}$.

The zener diode, with an arbitrarily selected zener voltage $V_Z = 10V$ is now introduced and resistor $\mathbf{R}_1$ split into resistors $\mathbf{R}_{1A}$ and $\mathbf{R}_{1B}$ (Figure 17). At point B in the protection locus of Figure 13 the diode is at the threshold of conduction and the voltage across it is its zener voltage V_Z. However the current through the diode at this point is still negligible compared to the current through $\mathbf{R}_{1A}$ and $\mathbf{R}_{1B}$. Thus, from Figure 17:

$$\mathbf{I}_1 = \mathbf{I}_2 + \mathbf{I}_3$$

$$\Rightarrow$$

$$\mathbf{I}_1 = \frac{0.6}{56} + \frac{(-23.73 + 24)}{100} = 13.42\mathbf{mA}$$

$$\Rightarrow$$

$$\mathbf{R}_{1B} = \frac{(-14.33 + 23.73)}{13.42\mathbf{mA}} = 700\mathbf{R}4$$

$$\Rightarrow$$

$$\mathbf{R}_{1A} = \mathbf{R}_1 - \mathbf{R}_{1B} = 4\mathbf{K}8 - 700\mathbf{R}4 = 4\mathbf{K}1$$

As is the case with the linear foldback locus of Figure 2, a minimum of three output pairs is required to drive a $(4\Omega\angle \pm 60^{0})$ load, since available current at $v_{ce} = 45\mathrm{V}97$ remains unchanged at $i_C = 3\mathrm{A}1$.

However, with the protection locus of Figure 13, available current per output pair at Vce=4V increases from 6A4 to 7A1 and the current at $v_{ce} = 2|V_{cc}|$ increases from 0A5 to just under 1A5 per output pair.

Since the locus is non-linear, caution must be exercised to ensure that while pursuing the secondary objective of enhancing current delivery in the low-Vce region of the SOA, available current in the critical higher device voltage region ($|V_{cc}| \le v_{ce} < 2|V_{cc}|$) is not simultaneously compromised by the location of the breakpoint.

The circuits of Figures 18 and 19 are frequently used [5,19,21] to realise single slope single breakpoint non-linear foldback protection. The small signal diode in Figure 18 is used to establish the flat portion of the locus. Unfortunately simulation reveals that this arrangement gives a soft and grossly ill-defined breakpoint.

Alternatively the small signal diode (Figure 19) is used to create a single slope single breakpoint regime by means of a simple voltage polarity-dependent divider [23]. However, this scheme (beloved of North American manufacturers) is unsatisfactory with respect to flexibility in breakpoint placement. This is because diode commutation can only occur at $v_{out} = 0V$ (i.e. $v_{ce} = |V_{cc}|$) so that the nominally zero-slope portion of the locus is solely defined by the voltage drop across Re being equal to the protection transistor's base-emitter voltage. The locus of Figure 21 requires a nominal Re = 0R47; this more than doubles gain-step distortion [11, pg 256] generated by a class-AB output stage compared to the circuit of Figure 14, for which Re = 0R22.

A smaller value of Re cannot be employed as this would result in a commensurate and necessarily unsafe vertical displacement of segment BC. Thus, segment BC is fixed for $|V_{cc}| = 40V$ and gives even more inefficient SOA usage in the crucial $|V_{cc}| \le v_{ce} < 2|V_{cc}|$ region than the compromised single slope linear foldback arrangement of Figure 5.

Further, using a fixed reference voltage (zero volts in this case), independent of the floating collector-emitter voltage v_{ce}, as the basis for SOA protection is rather optimistic as it presumes equally invariant supply rails that do not sag under load. For example, a nominal 40V supply rail that sags by 5V under load would effect a 5V horizontal displacement of segment AB to DE (Figure 21). Conversely, a primary supply surge could cause a potentially disastrous horizontal translocation along BC of segment AB into and perhaps well beyond the transistor's SOA limits.

Since the diodes in Figure 19 are, in theory, never forward biased simultaneously, the modification in Figure 20 is often adopted [18] in what may at first appear to be an elegant simplification. The excision of one of the resistors in this fashion is, alas, a false economy at best, as the performance of the circuit is now significantly compromised by the finite reverse recovery time of the diodes, with minority carrier storage causing the diodes to conduct briefly when reverse biased. This causes minute intermittent zero-crossing oscillation at the output, which may easily be misdiagnosed as a class-B crossover anomaly.

Since segment BC is established by merely selecting Re = 0R47, only point A on locus ABC (Figure 21) is required to obtain a solution. Let $\mathbf{R}_1 = 220\mathbf{R}$ and $V_{cc} = 40V$ (Figure 22):

$$\mathbf{I}_2 = \mathbf{I}_1$$

where:

$$\mathbf{I}_1 = (40 - 34.02)/220\mathbf{R} = 27.18\mathbf{mA}$$

With $V_f = 0V7$ at 27mA:

$$\mathbf{R}_2 = \mathbf{V}_{R2}/\mathbf{I}_2 = (34.02 - 0.7)/27.18\mathbf{mA} = 1\mathbf{K}2$$

The circuit in Figure 19 is capable of modest improvement however, and therefore merits closer scrutiny.

This scheme can be made more efficient (Figure 23) by changing the voltage divider's fixed reference voltage from zero to two arbitrary voltages V_{Ref1} and V_{Ref2} of equal magnitude but opposite polarity, such that $\{0V < (|V_{Ref1}| = |V_{Ref2}|) < |V_{cc}|\}$; nominal 40V rails are assumed. This enhances the flexibility of the circuit, as the breakpoint can now be freely located along CF (Figure 24) giving rise to a more efficient locus BEF.

The reference voltage is equal in magnitude to the output voltage V_{out} at the breakpoint in locus BEF (Figure 25); i.e. $|V_{Ref1}| = |V_{Ref2}| = |V_{out}|_{V_{ce}=60V} = 20V6$, with $V_{Ref1} = -20V6$ and $V_{Ref2} = +20V6$. This calls for a nominal 60V6 zener diode.

It is recommended that the required voltage drop be realized with multiple low-voltage devices $(6V \le V_Z \le 12V)$ as these possess a significantly lower series impedance than may be obtained with single device[22]. In practice, therefore, each of Z_1 and Z_2 may, for example, consist of six On Semiconductor 1N5240B 10V zeners in series with a forward biased 1N4448 diode, all biased at a nominal 25mA by R_Z and R_Z^*.

Crucially, in Figure 23, the cathode of diode Z_1 is connected directly to $+V_{cc}$, effectively bootstraping V_{Ref1} to the supply rail, so that any anomalies on the supply are directly impressed on the reference voltage. This effectively eliminates the potentially fatal tendency of segment BE to migrate back and forth along CF with non-ideal supply rail fluctuations. Similarly, V_{Ref2} is bootstrapped to the supply rail by connecting the anode of Z_2 to $-V_{cc}$.

Let $R_1 = 220R$ and $|\pm V_{cc}| = 40V$ (Figure 26):

$I_2 \approx I_1$

where:

$I_1 = (40 - 35.9)/220R \approx 18.64mA$

With $V_F \approx 0V7$ at 20mA:

$R_2 = V_{R2}/I_2 \approx (35.9 - 0.7 + 20.6)/18.64mA \approx 3K0$

The dependence of segment EF (Figure 24) on the value of Re for the circuit in Figure 23 remains its Achilles' heel. The singular advantage of the network of Figure 14 is that it permits the arbitrary location of a breakpoint in the protection locus without undue reference to the value of Re.

Moreover, because the entire network of Figure 14 floats between the output and supply rails the position of the locus in the SOA remains resolutely invariant in the face of deviant power supply behaviour, without recourse to a bootstrapped voltage reference.

Dual Slope Single Breakpoint Non-Linear Foldback Limiting

Introducing a resistor R_d in series with diode D_1 (Figure 28) causes the voltage drop across the series combination to increase linearly above the diode's conduction threshold. This effectively induces a net linear increase in potential across resistors R_{1B} and R_2 for i_c and v_{ce} combinations in the $v_{ce} \ge 36V$ region of the SOA (Figure 27). The gradient of segment BD in the protection locus can now be varied linearly[11] with R_d about point B which gives vastly greater flexibility with regard to optimal placement of the breakpoint.

As is the case with single slope linear foldback SOA limiting, segment BD must intersect the SOA's Vce axis at a value greater than the sum of the moduli of the supply rails if spurious limiter activation is to be prevented. Available current per output pair at Vce≈4V is further increased to 12A8 compared to 7A1 for the locus of Figure 13.

Initially, as previously established, resistor values are calculated for the single slope segment ABE (Figure 27) in the absence of the zener diode and resistor R_d. Additionally, resistors R_{1A} and R_{1B} are combined into a single resistor R_1.

Arbitrarily selecting $R_3 = 100R$ and points A and B where at point A $I_c = 14A$, $V_{ce} = 0V$, and at point B $I_c = 4A$, $V_{ce} = 36V$, it follows from Figure 29:

$$0.6 = \frac{3.08R_2}{R_2 + R_1 100/(R_1 + 100)} \qquad (8)$$

From Figure 30:

$$I_2 = I_1 + I_3$$

$$\Rightarrow$$

$$0.6/R_2 = (40 - 3.72)/R_1 + (4 - 3.72)/100$$

$$\Rightarrow$$

$$0.6 = R_2(36.28/R_1 - 0.28/100) \qquad (9)$$

Solving (8) and (9) simultaneously gives $R_1 \approx 1K5$ and $R_2 \approx 22R7$. The zener diode (arbitrary $V_Z = 10V$) is now introduced and resistor R_1 split into R_{1A} and R_{1B} (Figure 31):

$$I_1 = I_2 - I_3$$

$$\Rightarrow$$

$$I_1 = \frac{0.6}{22.7} - \frac{(4 - 3.72)}{100} = 23.6mA$$

$$\Rightarrow$$

$$R_{1B} = \frac{(13.12 - 3.72)}{23.6mA} = 398R$$

$$\Rightarrow$$

$$R_{1A} = R_1 - R_{1B} = 1K5 - 398R \approx 1K1$$

Resistor Rd is now introduced and its value established by consideration of the circuit conditions at point D ($I_c = 0.5A$, $V_{ce} = 79.89V$) on the locus of Figure 27. Thus from Figure 32:

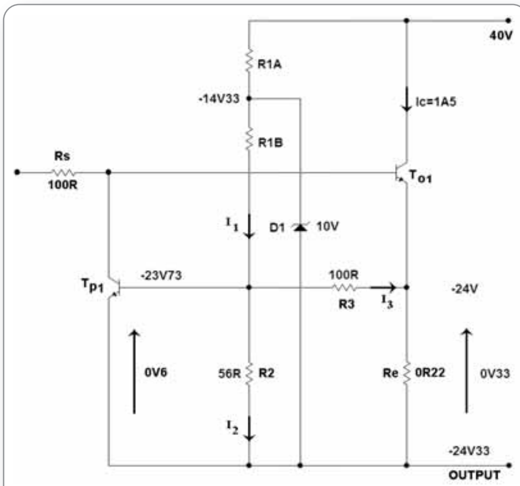

Figure 17: Output conditions at point B on the protection locus of figure 13 with D1 in situ and R1 split into two. The contribution of I_3 to the current in Re is deemed negligible

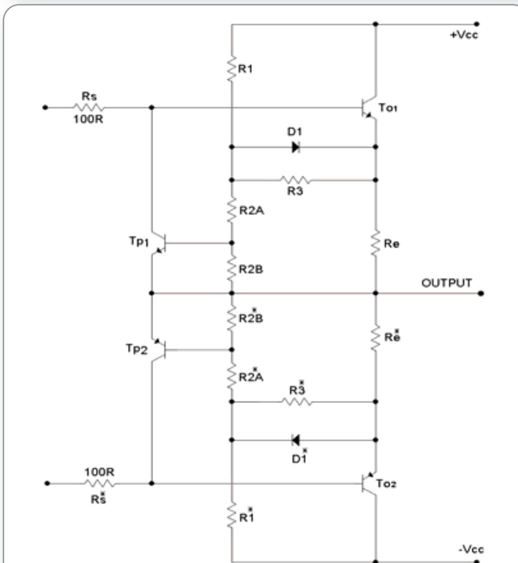

Figure 18: Small signal diode-based single slope single breakpoint non-linear foldback limiter

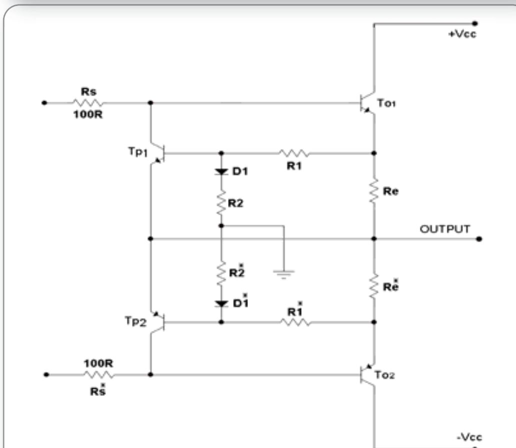

Figure 19: Polarity-dependent voltage divider used to introduce a single breakpoint in an otherwise linear-slope locus

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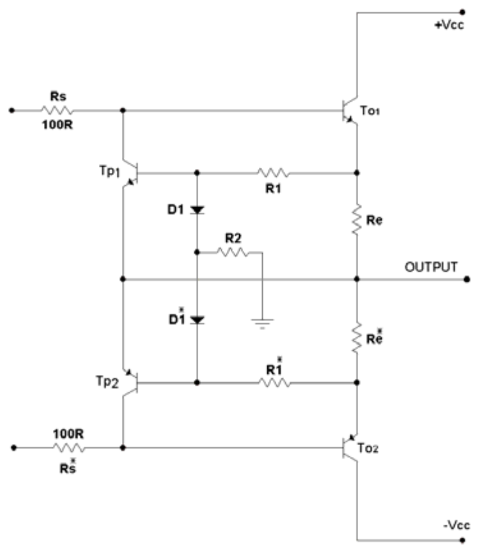

Figure 20: A common variation in figure 18 which gives inferior performance due to the finite reverse recovery time of the diodes

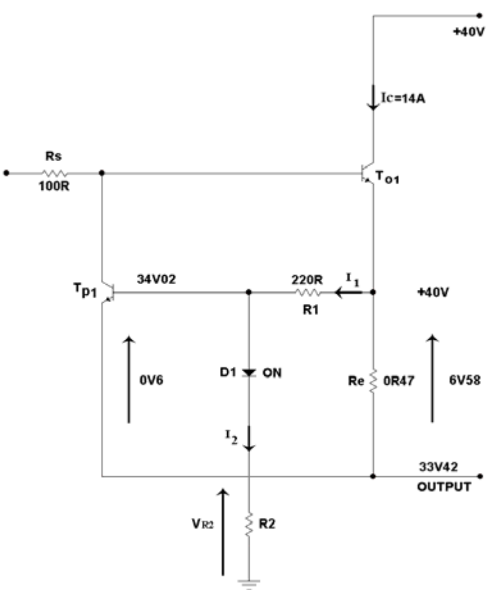

Figure 22: Output conditions at point A on the protection locus of figure 21

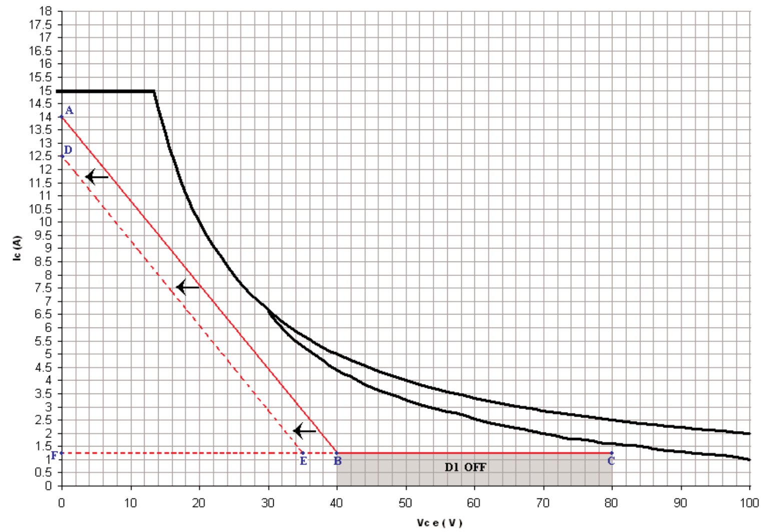

Figure 21: Single slope single breakpoint non-linear protection locus described by network of figure 19. A notional 5V drop in the supply rail causes an equivalent horizontal translation of segment AB to DE

$$I_{1B} = I_2 + I_3$$

$$\Rightarrow$$

$$I_{1B} = \frac{0.6}{22.7} + \frac{(-39.4 + 39.89)}{100} = 31.3\text{mA}$$

$$\Rightarrow$$

$$V_x = -39.4 + I_{1B}R_{1B} \approx -26.9\text{V}$$

$$\Rightarrow$$

$$I_d = I_{1A} - I_{1B} = \frac{(40 + 26.9)}{1\text{K}1} - 31.3\text{mA} \approx 27.5\text{mA}$$

$$\Rightarrow$$

$$R_d = \frac{(V_x + 30)}{I_d} \approx 111\text{R}5$$

The dual slope single breakpoint scheme of Figure 33, sometimes erroneously[10] described as "treble slope", is an amalgam of the circuits of Figures 5 and 19. As in Figure 19, the breakpoint occurs at $v_{out} = 0V$ (i.e. $v_{ce} = |V_{cc}|$) giving locus ADEF (Figure 34). However, segment DEF, being part of CDEF, is established by R_1 and R_3, and its efficacy is therefore as dependent on the value of Re as the network of Figure 5.

Resistor R_1 merely pulls the base of the protection transistor low as required for $\{0V \le v_{ce} < 40V\}$; this gives segment AD whose position in the SOA is ill-defined for non-ideal supply rails due to the use of an invariant voltage reference. Since the breakpoint for this arrangement is fixed at $v_{ce} = |V_{cc}|$, only points A and F on locus ADEF are required to obtain a solution. With reference to Figure 35, let $R_3 = 220\text{R}$ and $|\pm V_{cc}| = 40\text{V}$:

$$I_1 = I_3$$

where:

$$I_3 = (-39.4 + 39.78)/220\text{R} \approx 1.73\text{mA}$$

$$\Rightarrow$$

$$R_1 = (40 + 39.4)/1.73\text{mA} \approx 46\text{K}$$

With reference to Figure 36:

$$I_2 = (40 - 37.52)/(R_1 // R_3) = 2.48/219\text{R} \approx 11.33\text{mA}$$

With $V_f = 0\text{V}7$ at 11mA:

$$R_2 = V_{R2}/I_2 = (37.52 - 0.7)/11.33\text{mA} \approx 3\text{K}3$$

Clearly, this scheme's indecent dependence on the value of Re makes it inferior to the standard linear foldback arrangement of Figure 1. Consequently, given Re = 0R22, the protection locus of Figure 34 permits the delivery of only 1A5 at Vce≈45V97, requiring a minimum of six output pairs for unimpeded drive into a $(4\Omega\angle \pm 60^{\circ})$ load from ±40V supply rails.

As with Figure 23, the network of Figure 33 may be usefully improved (Figure 37) by changing the diode's reference from zero to an arbitrary voltage V_{Ref1} such that $(0V < |V_{Ref1}| < |V_{cc}|)$. This enhances the flexibility of the circuit as the breakpoint can now be moved freely along segment CF, giving rise to a more efficient locus BEF whose position in the SOA is unaffected by non-ideal fluctuation of the supply rails (Figure 34).

The reference voltage is established by determining the output conditions at the breakpoint (Figure 38). Therefore, for locus BEF in Figure 34, $V_{Ref1} = -16\text{V}33$ and $V_{Ref2} = +16\text{V}33$, which calls for a nominal 56V33 zener diode. With reference to Figure 39:

$$I_1 = I_3$$

where:

$$I_3 = (-39.4 + 39.78)/220\text{R} \approx 1.73\text{mA}$$

$$\Rightarrow$$

$$R_1 = (40 + 39.4)/1.73\text{mA} \approx 46\text{K}$$

With reference to Figure 40:

$$I_2 = (40 - 38.4)/(R_1 // R_3) = 1.6/219\text{R}0 \approx 7.3\text{mA}$$

With $V_f = 0\text{V}65$ at 7mA:

$$R_2 = V_{R2}/I_2 = (38.4 - 0.65 + 16.33)/7.3\text{mA} \approx 7\text{K}4$$

Note that there is no change in the value of

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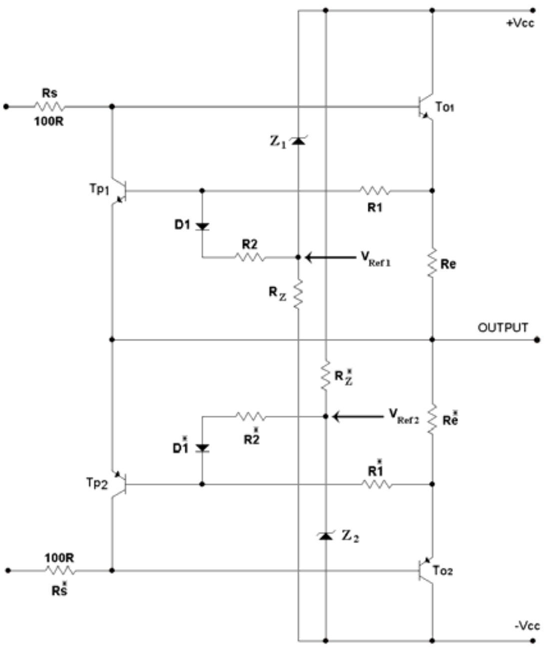


Figure 23: The use of arbitrary voltage references of equal magnitude makes for a worthwhile mprovement in efficiency compared to the arrangement of figure 19

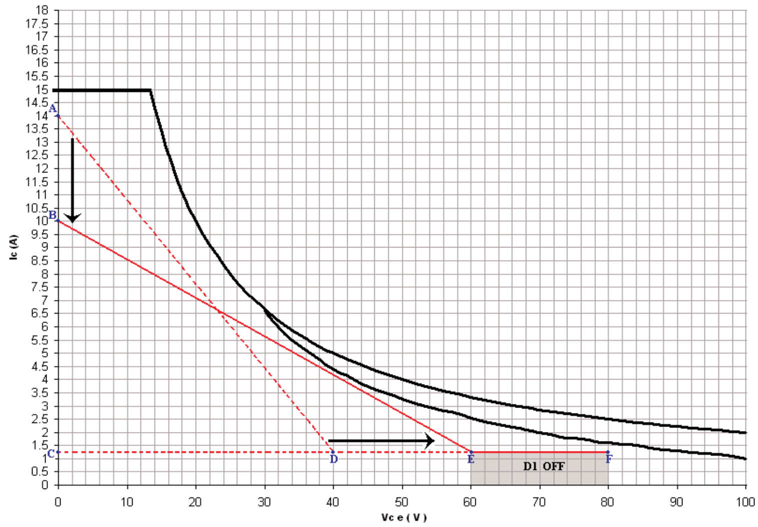


Figure 24: Improved single slope single breakpoint locus BEF realised by using an arbitrary voltage reference

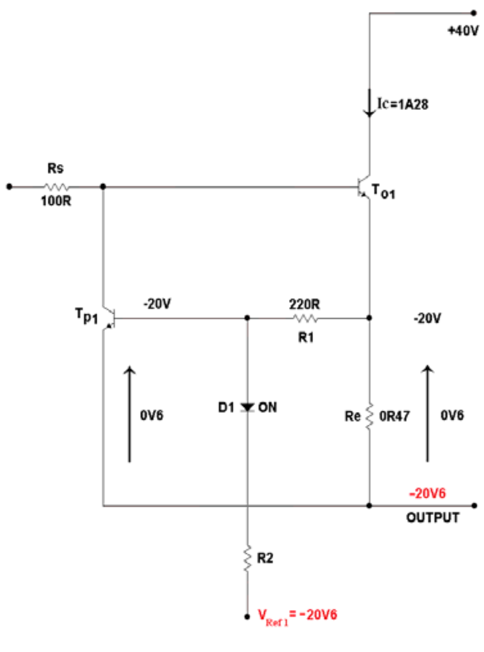


Figure 25: The reference voltage is made equal in magnitude to the output voltage at the breakpoint (i.e. when Vce=60V); the diode is then at the threshold of conduction

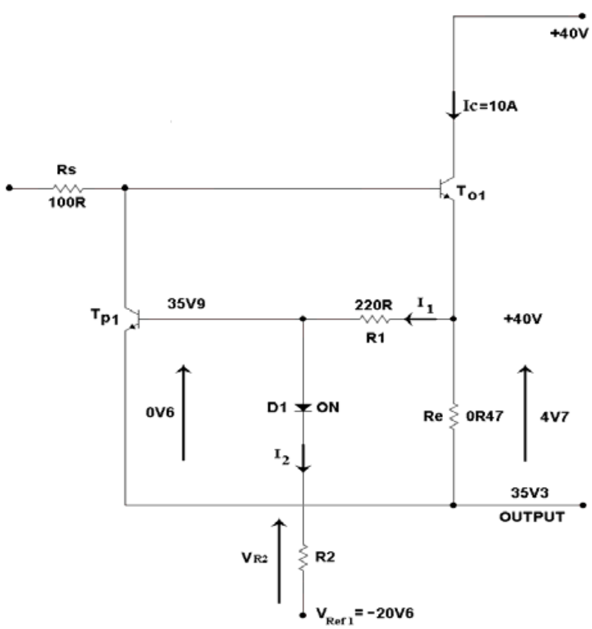


Figure 26: Output conditions at point B on the protection locus in figure 24

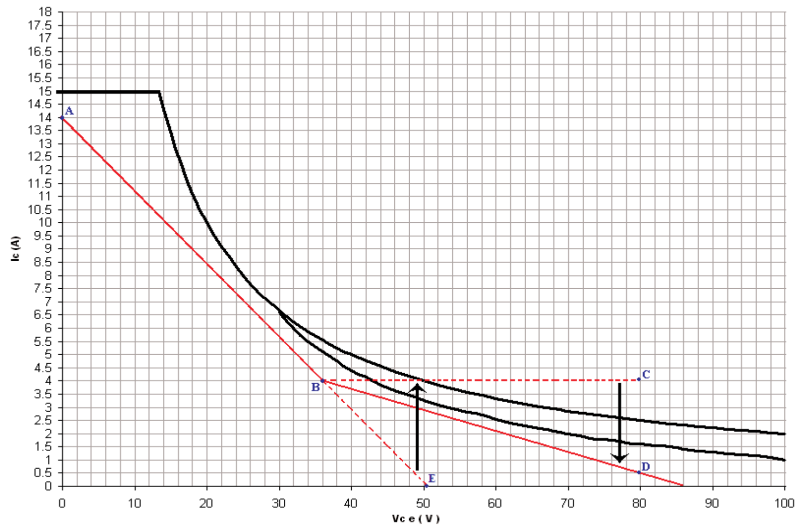


Figure 27: Dual slope single breakpoint non-linear foldback protection locus

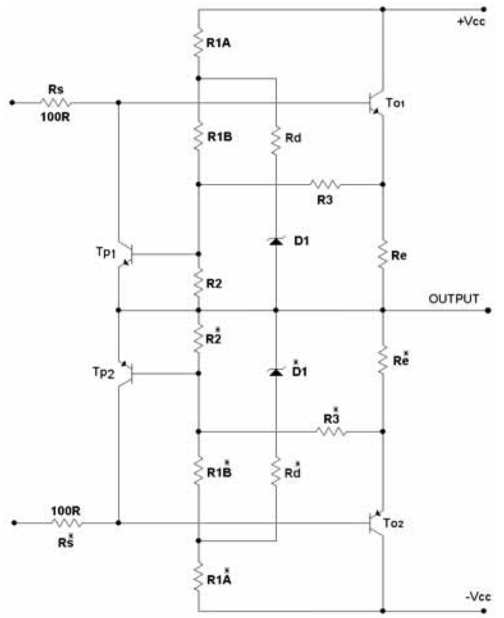


Figure 28: Dual slope single breakpoint non-linear foldback limiter

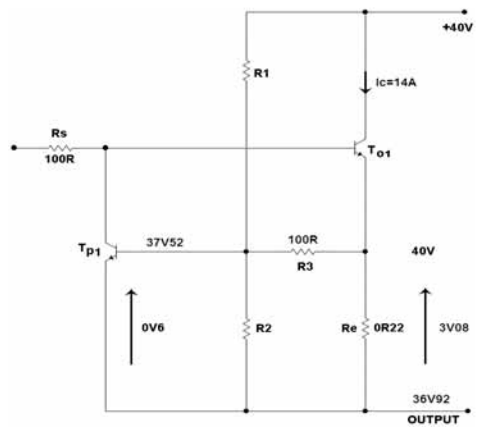


Figure 29: Output conditions at point A on the protection locus of figure 27 in the absence of the zener diode and resistor Rd

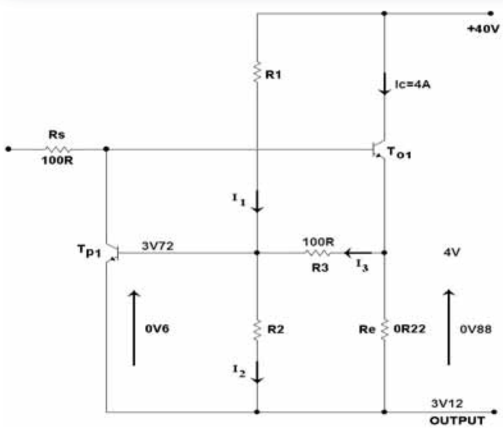


Figure 30: Output conditions at point B on the locus of figure 27 in the absence of the zener diode and resistor Rd

$\mathbf{R}_1$ and $\mathbf{R}_3$ in the circuits of Figures 5, 33 and 37, with different values of $\mathbf{R}_2$ required to merely pull the base of the protection transistor low as required when the diode is forward biased.

Although the efficacy of the protection locus is in part ameliorated by the means described above, the gradient of segment EF, being part of CDEF, is determined by resistors $\mathbf{R}_1$, $\mathbf{R}_3$ and limited by practical values of Re-an affliction absent from the circuit of Figure 28.

Complete independence from Re of both segments of the dual slope protection locus described by the circuit of Figure 37, may be realised by introducing base-emitter resistors $\mathbf{R}_2$ and $\mathbf{R}_2^*$, respectively for each protection transistor $\mathbf{T}_{P1}$ and $\mathbf{T}_{P2}$ (Figure 41). The result is merely a combination of the linear single slope scheme of Figure 1 and the non-linear single slope circuit of Figure 23.

The linear single slope locus of Figure 2 is reproduced in Figure 42 as segment BCD for which Equations 1 and 3 are valid. Therefore, since, as previously resolved (Equations 1 and 3) $\mathbf{R}_3 = 220\mathbf{R}$ then $\mathbf{R}_1 = 12\mathbf{K}4$ and $\mathbf{R}_2 = 143\mathbf{R}$ (Figure 41). Resistor $\mathbf{R}_4$ pulls the base of the protection transistor low as required for $\{0V \le v_{ce} \le 42V\}$ giving segment AC.

The reference voltage is equal to the output voltage when $v_{ce} = 42V$, so that $\mathbf{V}_{\mathbf{Ref1}} = 40\mathbf{V} - \{42\mathbf{V} + (3\mathbf{A}5 * 0\mathbf{R}22)\} = -2\mathbf{V}77$ and $\mathbf{V}_{\mathbf{Ref2}} = +2\mathbf{V}77$. With reference to Figure 43:

$$(\mathbf{I}_2 + \mathbf{I}_4) = (\mathbf{I}_1 + \mathbf{I}_3)$$

$$\Rightarrow$$

$$\mathbf{I}_4 = (\mathbf{I}_1 + \mathbf{I}_3 - \mathbf{I}_2)$$

$$\Rightarrow$$

$$\mathbf{I}_4 = (40 - 37.96)/12\mathbf{K}4 + (40 - 37.96)/220\mathbf{R} - 0.6/143\mathbf{R}$$

$$\Rightarrow$$

$$\mathbf{I}_4 = 5.24\mathbf{mA}$$

With $\mathbf{V}_f = 0\mathbf{V}6$:

$$\mathbf{R}_4 = \mathbf{V}_{\mathbf{R4}}/\mathbf{I}_4 = (37.96 - 0.6 + 2.77)/5.24\mathbf{mA}$$

$$\Rightarrow$$

$$\mathbf{R}_4 = 7\mathbf{K}7$$

The flexibility of the scheme of Figure 41 is significantly improved compared to that of Figure 37. However, the network of Figure 28 achieves the same versatility with a significantly reduced component count.

Triple Slope Dual Breakpoint Non-Linear Foldback Limiting

With modern power transistors and practical loudspeaker systems, an optimally located dual slope protection locus realised by the limiter of Figure 28 can hardly be improved upon with respect to efficiency in the critical $\{|V_{cc}| \le v_{ce} < 2|V_{cc}|\}$ region. However, with nominally resistive laboratory loads, with which a power amplifier's published specifications are obtained, the $\{0V \le v_{ce} \le |V_{cc}|\}$ region of the SOA is of primary interest (Figure 10).

Thus, in a competitive market place, even when the truth of the matter is known, an amplifier designed to maintain its rated voltage swing across resistive loads of decreasing magnitude (typically to a minimum of 1 ohm) without limiter intrusion may be commercially rewarding. A suitably robust power supply and conservative thermal management are assumed. To this end, the triple slope design of Figure 44 is presented. This circuit is a straightforward amalgam of the dual slope scheme of Figure 28 and the single slope single breakpoint network of Figure 23. Thus, the circuit of Figure 28 is required to produce the dual slope characteristic BDF (Figure 45), while resistor $\mathbf{R}_4$ pulls the base of protection transistor $\mathbf{T}_{P1}$ low as appropriate for $\{0V \le v_{ce} \le 42V\}$, giving segment AC.

Fifty-volt supply rails are assumed; a

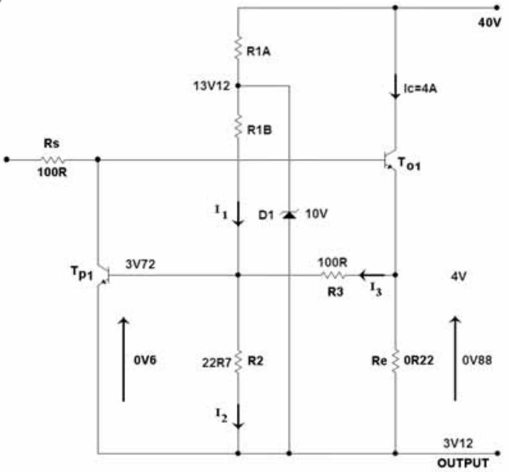


Figure 31: Output conditions at point B on the locus of figure 27 with the zener diode included and R1 split in two

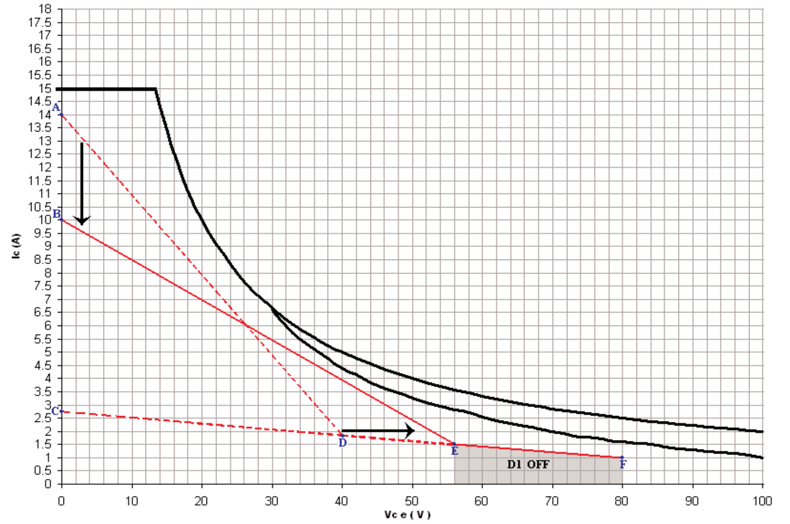


Figure 34: Dual slope single breakpoint loci described by the circuits of figure 33 and 37

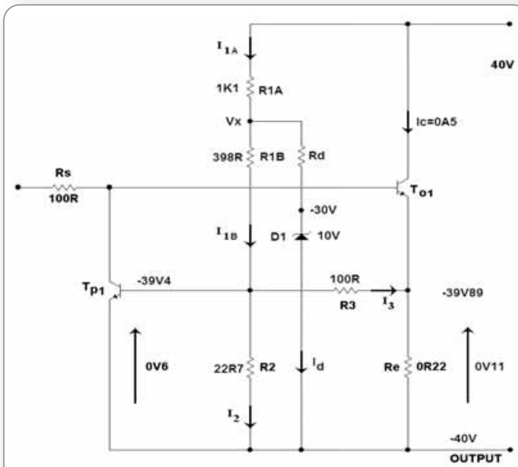


Figure 32: Output conditions at point D on the locus of figure 27 with the resistor Rd introduced

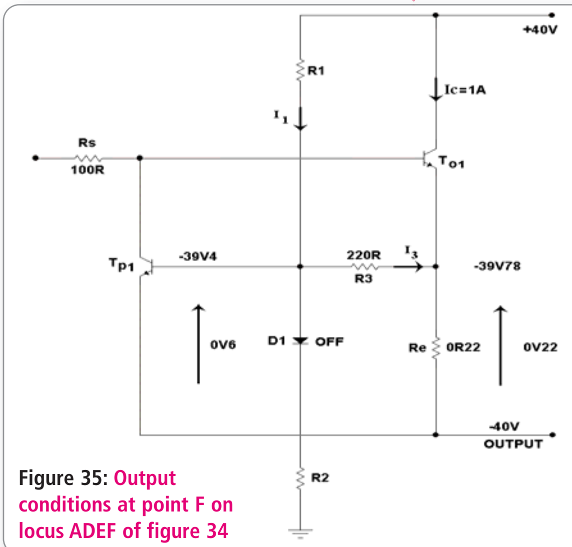


Figure 35: Output conditions at point F on locus ADEF of figure 34

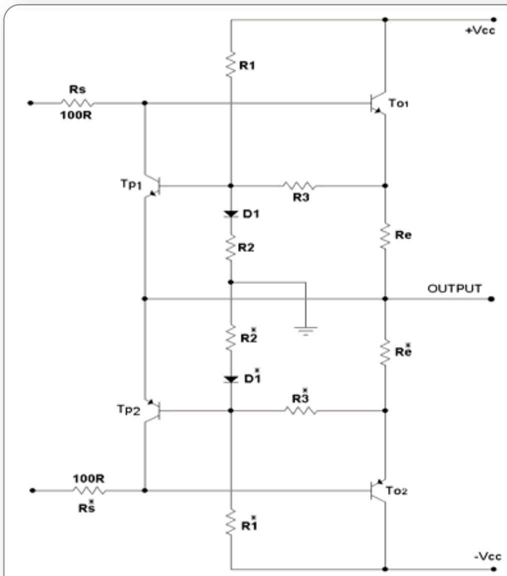


Figure 33: This dual slope single breakpoint scheme is a logical development of the circuits of figures 5 and 19

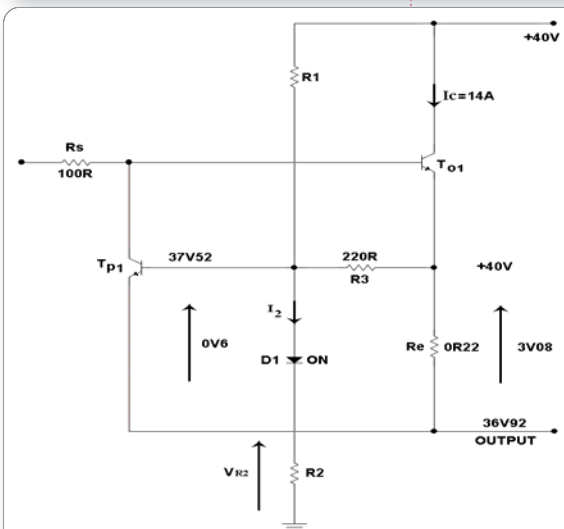


Figure 36: Output conditions at point A on locus ADEF of figure 34

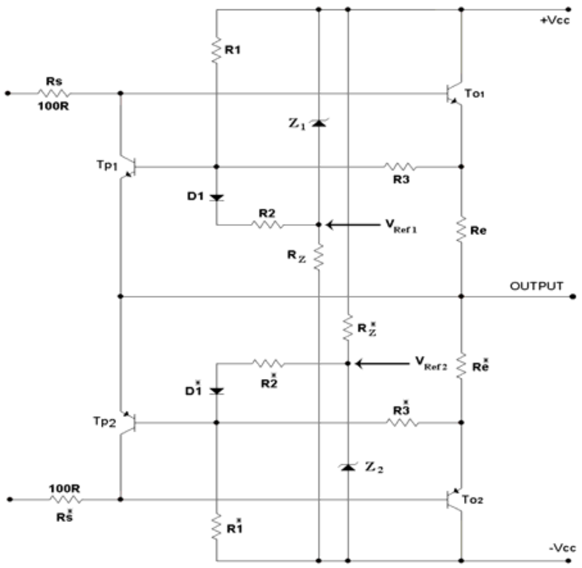


Figure 37: The efficacy of the compromised dual slope scheme of figure 33 is improved by using arbitrary bootstrapped voltage references of equal magnitude

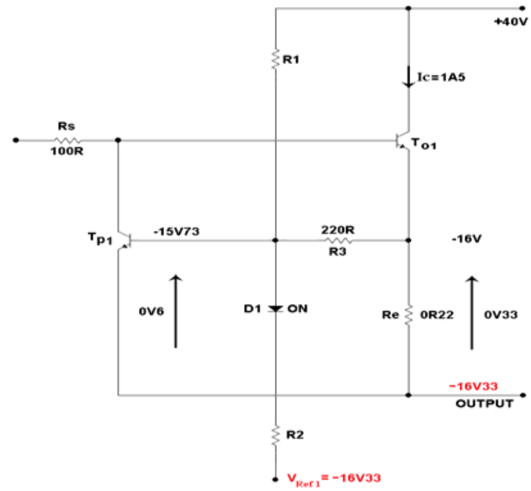


Figure 38: The reference voltage is made equal in magnitude to the output voltage at the breakpoint (i.e. when Vce=56V); the diode is then at the threshold of conduction

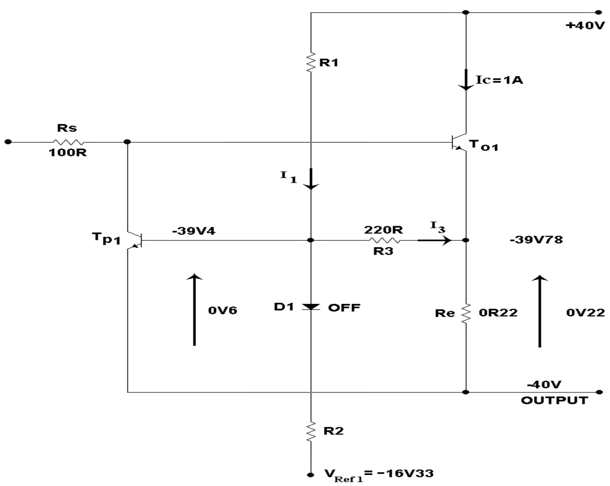


Figure 39: Output conditions at point F on the protection locus of figure 34

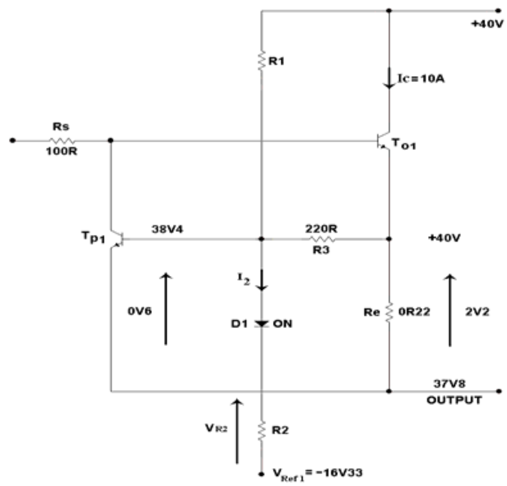


Figure 40: Output conditions at point B on the protection locus of figure 34

triple slope locus with ±40V rails is vastly unnecessary. A $(4\Omega\angle\pm60^0)$ load driven to ±50V rails requires $i_c \approx$ 9A5 when $v_{ce} \approx$ 59V, giving peak transistor dissipation $P_{d(max)} \approx 561W$. The triple slope protection locus of Figure 45 allows 2A at $v_{ce} \approx$ 59V for a single complementary transistor pair. Therefore, at least five complementary pairs are required to drive a notional $(4\Omega\angle\pm60^0)$ loudspeaker system from ±50V supply rails without intrusive limiter activation. The algebra for this arrangement is straightforward if a little tedious and is left to interested readers.

Protecting Paralleled Complementary Output Transistors

Emitter resistor Re performes current-voltage conversion for the SOA limiter and promotes thermal stability by maintaining equable current distribution in an output stage consisting of multiple paralleled pairs of complementary transistors. For this reason, some designers suggest it is only neccesary to monitor the current of a single complementary pair in such an output stage [1,pg.257].

Alternatively, the calculated value of the current sensing resistor R_3 for a single complementary transistor pair is multiplied by the number N of paralleled output pairs with each resistor of value $N*R_3$ used to monitor the current in each transistor as shown in Figure 46.

An obvious disadvantage inherent in both schemes is that the open-circuit failure of a rogue transistor in one half of the output stage could result in the disastrous alteration of the protectection locus for the remaining devices in that section. However, with modern power transistors, this condition is unlikely to materialise; the use of an independent SOA limiter for each complementary pair would eliminate this potential flaw, but is financially indefensible in most commercial designs.

Simulating SOA Protection

SPICE allows the designer to check the results of calculation, to establish whether the deviation from the desired protection locus obtained by using preferred values is significant and to determine the effect of changes in ambient temperature on the position of the protection locus.

The arrangement of Figure 47 is a slightly modified version of the simulation circuit used by Douglas Self[11]. Voltage source V1 models

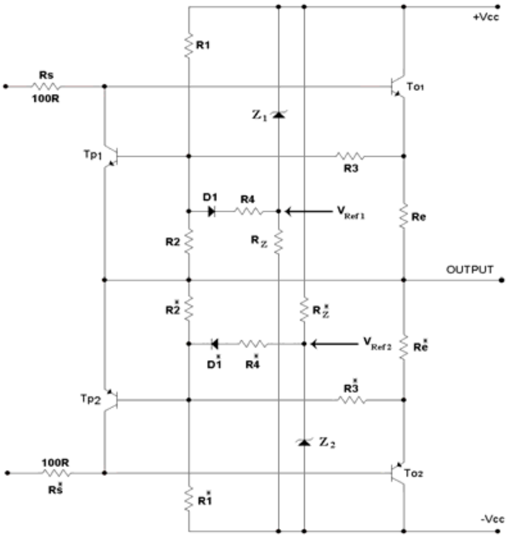


Figure 41: Introducing resistor R_2 into the circuit of figure 37 facilitates placement of an arbitrary locus in the SOA without undue dependence on the value of R_e

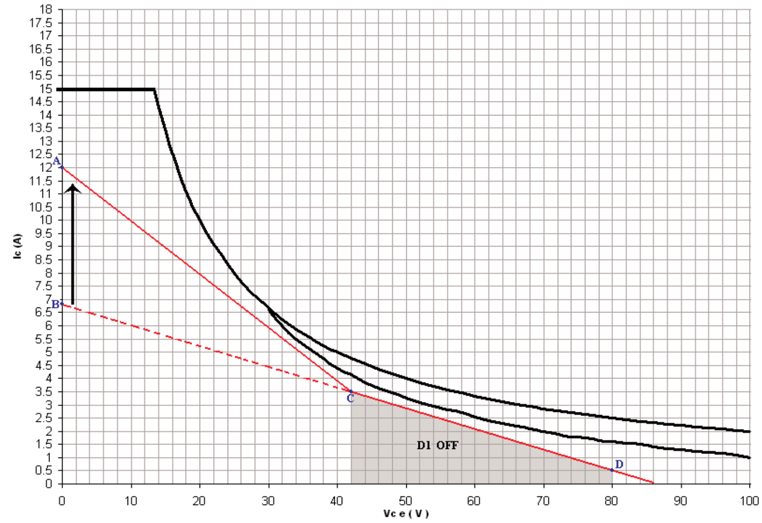


Figure 42: Dual slope single breakpoint protection locus described by the circuit of figure 41. Resistor R_4 modifies the linear single slope segment BCD of figure 2 by effecting a vertical translation of segment BC about point C

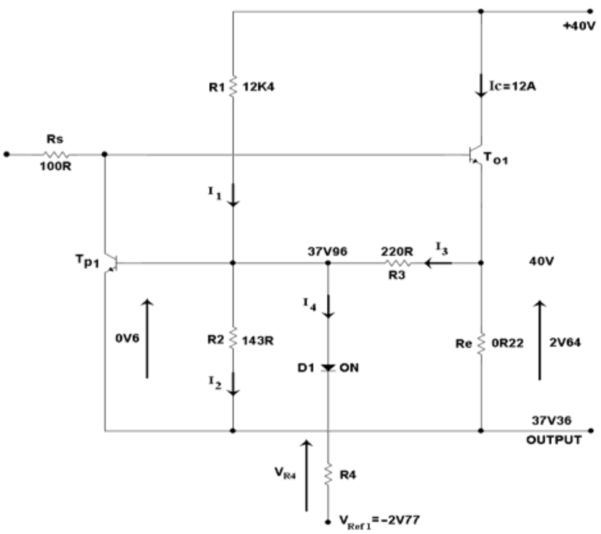


Figure 43: Output conditions at point A on protection locus ACD of figure 42

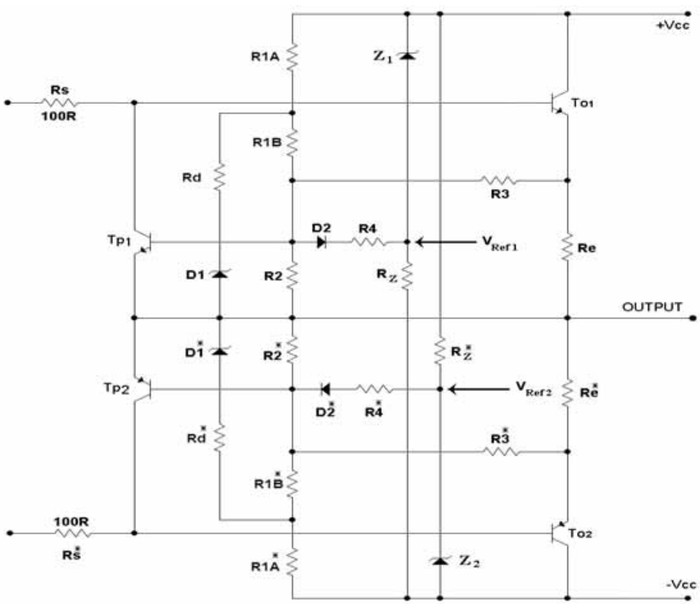


Figure 44: Triple slope dual breakpoint non-linear foldback limiter

the output transistors collector-emitter voltage Vce, while the unity gain voltage controlled current source G1 generates the current in the notional output transistor's emitter resistor R6. The current produced by G1 is the quantity that is plotted as V1 is DC swept. This current is a function of the voltage at the collector of the constant current source loaded protection transistor Q1.

Unfortunately, results obtained from this circuit can be grossly misleading unless it is correctly calibrated. This is because an increase in the value of the protection transistor's constant current source I1 causes the plotted locus to move upwards, while an increase in Q1's current gain causes the locus to move downwards.

To calibrate the circuit, the single slope linear foldback circuit of Figure 1 is used because it gives inherently more accurate results than the non-linear foldback arrangements whose accuracy is compromised by zener diodes with tolerances no better than 5%. Thus, having obtained the calculated values for a given single slope locus, I1 must be adjusted (for a given transistor model for Q1) until the plotted locus conforms to that predicted by the calculated component values.

Figure 48 shows the effect on the protection locus of increasing the simulation temperature from 27°C to 45°C. This magnitude increase in temperature may occur in the vicinity of the SOA protection circuitry in, for example, a powerful class-A amplifier.

The drop in threshold voltage (approximately 2mV/°C) of the protection transistor combined with the increase (approximately 6mV/°C for a 10V zener diode) in the zener diode's breakdown voltage with increasing temperature cause that part of the locus controlled by the zener diode to move downwards by a significant amount. The 45°C locus can no longer accommodate ±40V supply rails without protection being invoked, even with an open circuit load, when the output swings more than about ±35V. Clearly this effect may be lessened by using a temperature compensated zener diode. Alternatively a zener diode with negative temperature coefficient may be used

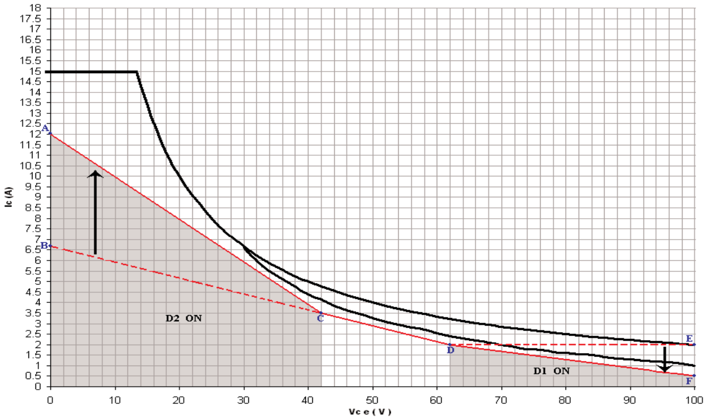


Figure 45: Triple slope dual breakpoint protection locus described by the circuit of figure 44; resistor R_4 modifies the dual slope characteristic BDF by effecting a vertical translation of segment BC about point C

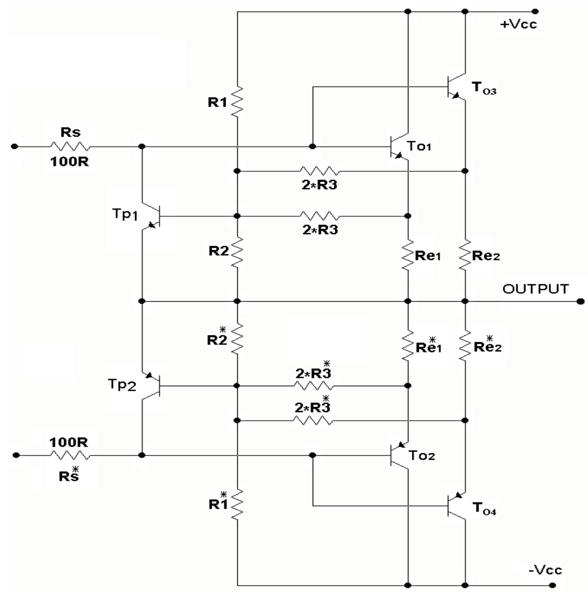


Figure 46: In this single-slope linear foldback scheme, voltage signals from multiple current sensing resistors are summed algebraically at the base of the protection transistor

to compensate for the protection transistor's positive temperature coefficient. This calls for a zener diode with Vz < 5V, which typically has a negative temperature coefficient in the range $0\text{mV} - 4\text{mV}/^{\circ}\text{C}$. The potential for over-compensation is insignificant, but may be accommodated by the judicious placement of that part of the locus controlled by the zener diode.

Conclusion

On grounds of safety and reliability, it is firmly recommended that all nominally linear complementary semiconductor audio frequency power amplifiers incorporate suitable SOA protection. The aversion cultivated by some designers to such is here shown to be wholly illusory. A competently designed SOA limiter should remain demonstrably inert and therefore completely unobtrusive with virtually all commercial loudspeaker systems provided the output stage consists of sufficient complementary transistors to safely drive a $(4\Omega\angle\pm60^{\circ})$ load to the supply rails.

The dual slope circuit of Figure 28 represents a significant improvement in efficient SOA utilisation compared to the single slope topology of Figure 1, with no significant penalty with regard to algebraic or physical complexity. Its characteristic locus (Figure 27) may be readily optimised to accommodate nominal ±50V supply rails with MJL3281A/MJL1302A transistors; however, higher supply rails are not recommended for worst-case reactive loads, as available collector current for these devices rapidly falls below 0A5 for $V_{CE} > 100\text{V}$.

Although e-MOSFETs are at least an order of magnitude less linear than bipolar transistors [11, pg.273], they provide significantly greater scope for reliable design at high device voltages $(|V_{Supply}| >> 50\text{V})$, with the promise of even greater efficiency in SOA utilisation due to the absence of secondary breakdown. Nevertheless there is no need to endure the indignity of e-MOSFET non-linearity and on-resistance voltage inefficiency in sub-200W into 8Ω designs.

More elaborate protection schemes are possible, with the use of as many diodes as the number of required breakpoints. However, the increase in available current in the high voltage region $\{|V_{cc}| \le v_{ce} < 2|V_{cc}|\}$, where it counts with respect to reactive load drive, is negligible relative to the circuit complexity thus engendered. ●

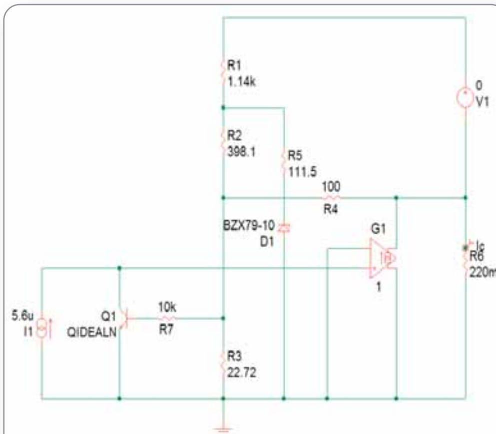


Figure 47: SPICE circuit for simulating dual slope SOA protection

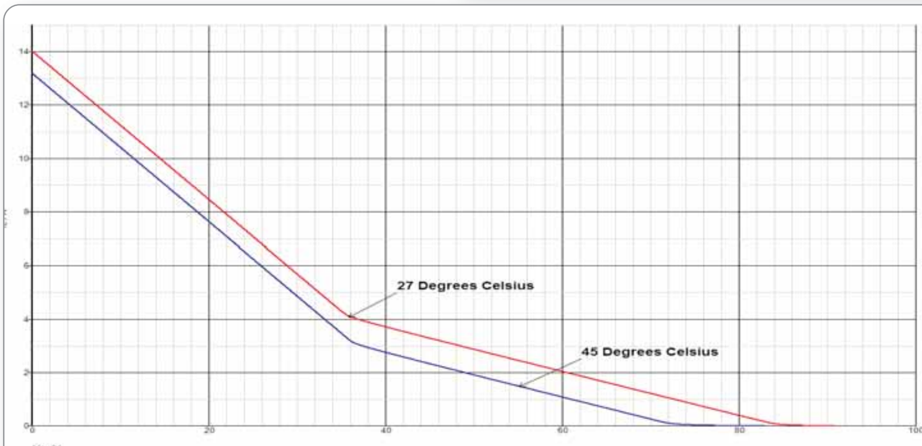


Figure 48: Simulated loci for the circuit of figure 47 at 27 and 45 degrees Celsius

WORLD'S FIRST 40NM MONOS FLASH TECHNOLOGY

JÜRGEN AXMACHER, SENIOR MARKETING MANAGER FOR AUTO CONTROL SYSTEMS IN THE AUTOMOTIVE BUSINESS UNIT AT RENESAS ELECTRONICS EUROPE, OUTLINES THE BENEFITS FOR THE AUTOMOTIVE SECTOR OF RENESAS'S LATEST MONOS EMBEDDED FLASH TECHNOLOGY FABRICATED IN THE 40NM PROCESS NODE

Renesas Electronics has introduced the latest MONOS (Metal Oxide Nitride Oxide Silicon) flash technology. This process will be the basis for the next 32-bit microcomputer architecture for automotive MCU applications and it is hailed 'first in the world' 40nm embedded flash technology for such MCUs.

It is expected the technology will set new standards in the MCU market in terms of reliability, current consumption and efficient programming, as well as read properties. In addition, the new process supports integration of special functions for functional safety and high temperature applications up to 170°C.

Embedded MONOS Flash

To create this embedded flash process, Renesas has drawn upon its own, vast, long-term expertise, as well as that of NEC Electronics with which it merged in 2010. Shortly after the merger, Renesas Electronics introduced a new 32-bit MCU (V850-Fx4-L) product line that combined the V850 core technology with the 90nm MONOS flash process. This product family was specially designed for control applications in the automotive area. It is characterized by efficient programming capabilities, lower power-consumption and higher reliability.

> The major advantage of the MONOS flash cells is that in case of a cell defect in the oxide layer, the charge at the floating gate is not completely drained, resulting in data loss

The major advantage of the MONOS flash cells is that in case of a cell defect in the oxide layer, the charge at the floating gate is not completely drained resulting in data loss, but only a small amount of charge is lost at the defective location. In contrast to the conventional flash technologies where the floating gate is made of a conductive material, the (MONOS) programmed flash-cell contents can still be read thanks to the use of an isolator (Si_3N_4) as floating gate.

The fast read-cycles of the MONOS flash cells are achieved when the same voltage level required to read a flash cell can also be used for the processor core, thus the read logic can be realized with the same CMOS technology. Complex charge pumps for higher voltages are not required. This, in addition to the higher speed, also leads to lower power consumption.

40nm vs Other Process Nodes

Renesas promoted the development of its MONOS flash technology based on a 40nm process at a time when the other semiconductor manufacturers opted for 65nm and 55nm technologies as intermediate steps; Renesas could then easily integrate higher flash memory densities on smaller chip sizes.

Using the 40nm flash cells the total chip size of the new MCU families can be reduced to about 25% compared in 90nm technology or about 50% in a 65nm technology for a comparable device.

The new process is especially characterised by its reliability and long data-retention time; this is one of the most important requirements of automotive applications. The new technology guarantees 20-year data retention for EEPROM emulation and a minimum of 125,000 write/read cycles.

Furthermore the MONOS process is scalable: the knowledge, experience and practical measures implemented in 90nm technology can be also applied to the 40nm technology. The memory structures can be shrunk without reducing the floating gate layer thickness too much, which in the flash process would lead to significant limitations towards data retention time or write/read cycles.

Another important development criterion of the new process is the current consumption of memory cells and that of complete memory blocks. In order to optimize fuel consumption and reduce emissions in vehicles, minimizing current consumption is an important aspect of automotive electronics. This is especially true for battery-powered applications, as in electric cars or vehicle applications with the engine switched off; lower current consumption is an important differentiating factor.

All these aspects are underpinned by the 40nm flash technology.

Additionally, the new technology also meets the temperature requirements of modern automotive developments, where full functionality is guaranteed at ambient temperatures up to 170°C. This is a significant advantage, particularly in the engine and gearbox fields.

Finally, the individual flash cells are integrated into so-called memory blocks with corresponding programming and read logic, which allows optimal connection of these blocks to MCUs with different memory size requirements. Thus, it is possible to realize microcontrollers with embedded flash memory sizes ranging from 128kByte up to 10Mbyte.

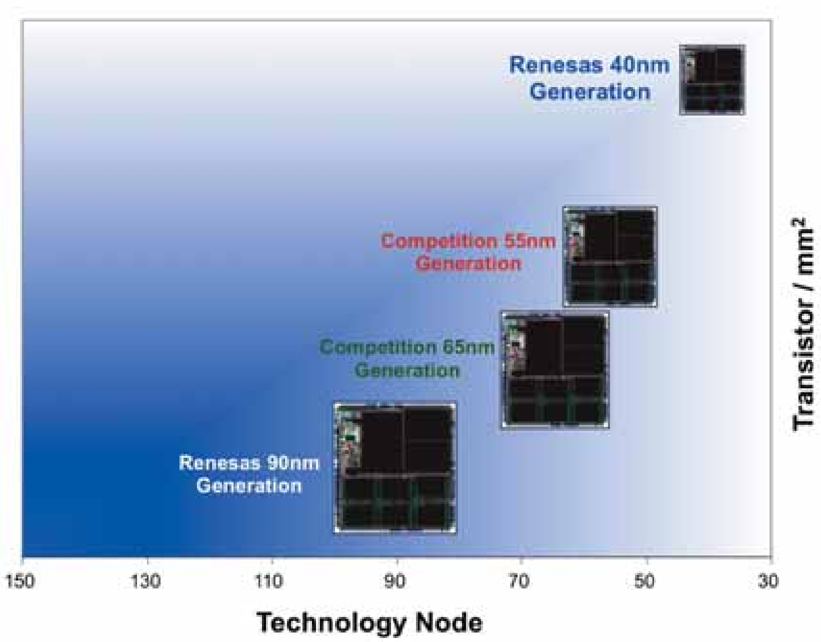


Figure 1: Chip size comparison

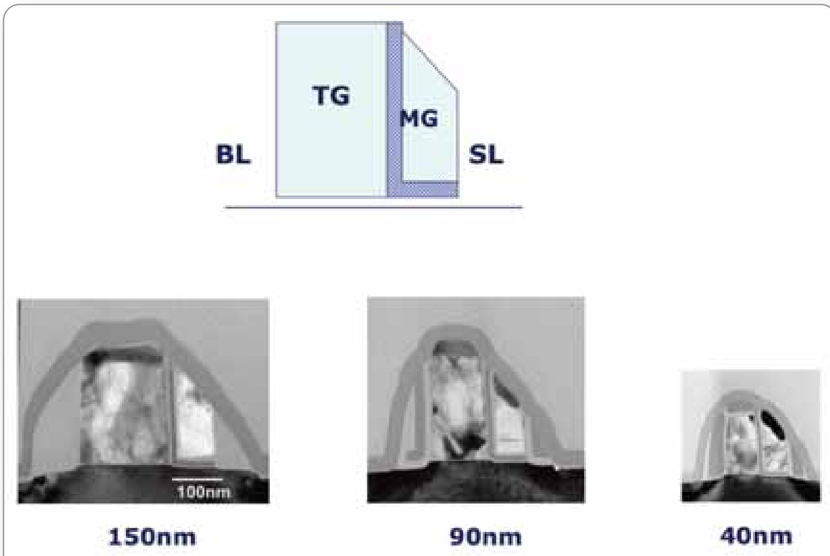


Figure 2: Scalability

Access speed is yet another important parameter of a flash cell. Like the existing 150nm and 90nm MONOS technologies, the 40nm technology will allow an extremely fast memory access time of less than 10ns (random single cycle access up to 120MHz). This will necessitate a cache memory only at frequencies above 100MHz. The costs for this are significantly lower than for flash memories with slower access time.

The Chip Design

The current chip designs with Renesas 90nm technology utilize six to seven metal layers for wiring and shielding within the MCU, whereas the 40nm MONOS process supports up to 11 metal layers. These metal layers essentially consist of a copper-aluminum alloy, guaranteeing much better read cycle time than pure copper layer technologies.

The automotive microcomputers currently being developed using the new 40nm MONOS process fulfill the ISO 26262 standard's requirements for functional safety. In this context the microprocessors

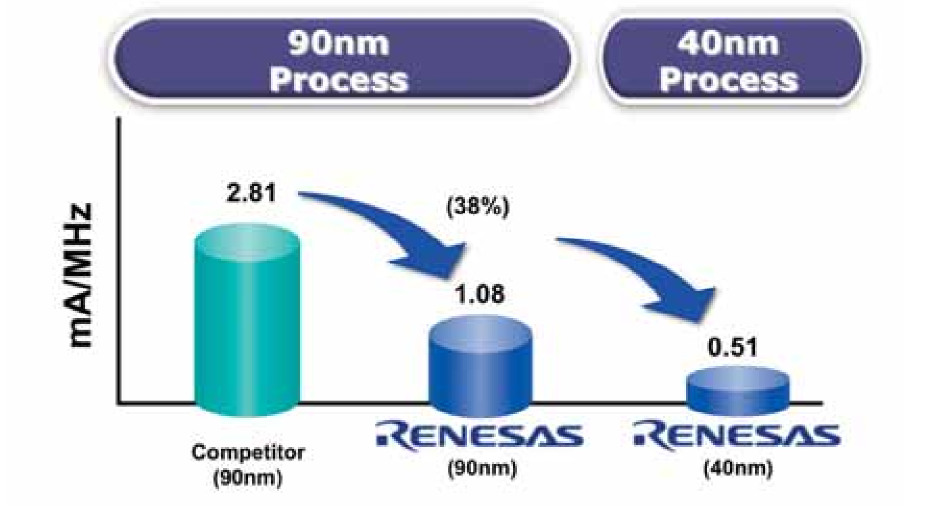


Figure 3: Current consumption comparison

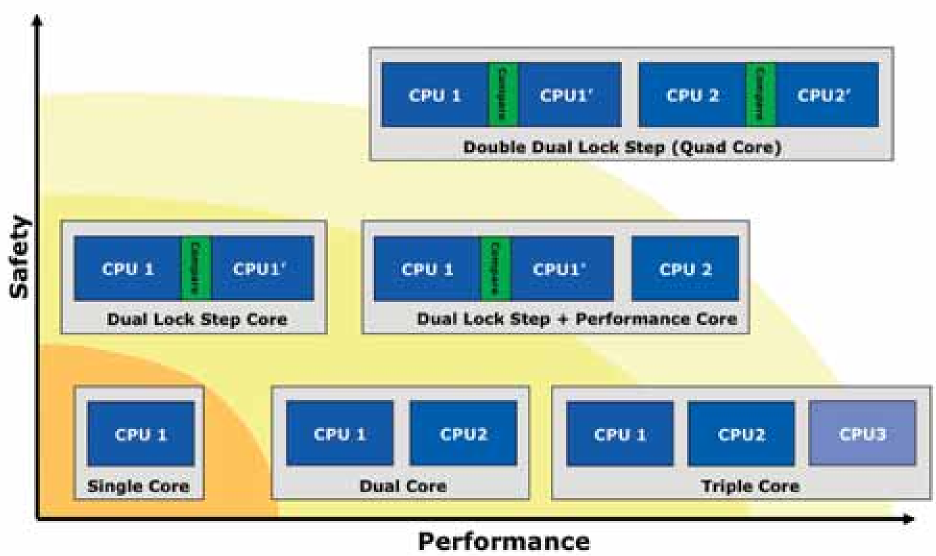


Figure 4: Single-/multi-core systems and applications

contain varied hardware measures which significantly ease achieving the ASIL-A up to ASIL-D safety level goals.

The device integrates functions supporting both, the user (e.g. memory protection mechanisms, runtime monitoring etc.), as well as dedicated safety measures (e.g. RAM/flash error correction techniques, redundant processors, clock monitoring, voltage monitoring, self-test etc). The overall goal of the new product line is to effectively support even the most stringent requirements, i.e. certifications up to ASIL-D level.

The new 32-bit MCU generation with RH850 processor core and 40nm flash will cover a variety of applications with different chip configurations. As such, different core sub-systems will be developed to support automotive requirements ranging from simple single core applications right up to complex multi-core systems, including the so-called Dual Lockstep processors efficiently and in a user-friendly manner.

The "Family" Concept

An important development policy of Renesas is the "family" concept. This ensures that the same processor core and the core sub-systems, defined bus systems and optimized peripheral IPs are used in all MCU families and the corresponding application segments to allow programming of scalable and reusable application software over different developments. As a consequence this concept leads to a qualified and robust AUTOSAR support for all 32-bit MCU families.

This 40nm MONOS technology is an optimal further development of the existing 90nm process and will be used for Renesas's new 32-bit automotive MCU line. Samples of the new microcomputer family will be available in the second half of 2012 and qualified to automotive standards by 2013. High volume production is scheduled for 2014.

Renesas's test laboratories are currently evaluated when the MONOS process will also be used for the following generation. This is due to evaluating other memory technologies (like MRAM for example) as potential candidates, besides the 32/28nm technology step.

RENESAS ELECTRONICS

UNVEILS NEW GENERATION RH850/X1 MICROCONTROLLER FOR AUTOMOTIVE APPLICATIONS

As Electronics World went to press Renesas Electronics announced the new RH850 family of 32-bit microcontrollers (MCUs) for automotive applications.

The RH850 is based on the 40nm MONOS (metal oxide nitride oxide silicon) embedded flash technology described on these pages. This makes Renesas the first semiconductor supplier to provide this technology to the automotive sector.

The RH850 family covers performance classes from 64 megahertz (MHz) up to 320MHz as single core performance. Multi-core systems will achieve even higher overall performance. The embedded flash memory will range from 256kB to 8MB, while additional blocks for data flash, emulating EEPROM functionality, are also included and deliver write/erase endurance values of more than 125,000 write/erase cycles at data retention times of minimum 20 years.

The rollout will involve multiple, application-tailored product series, each equipped with the RH850 32-bit core architecture. The series will span single core, dual-performance cores, dual lock-step cores and multiple core architectures, addressing virtually all 32-bit MCU performance and safety requirements in the various automotive segments.

www.renesas.eu

WHAT THE READERS SAY

WHERE ARE THEY?

I began to specialise in electromagnetic theory in 1962, fifty years ago. I researched the interconnection of high speed (1ns) logic at Motorola in Phoenix. They were making the fastest logic. No lecturer or textbook writer has been addressing the subject anything like as long. Further, textbook writers are trapped in the theory appropriate for steady state, sinusoidal radio, which includes radar. The established theory takes no account of any of the insights gained from high-speed digital electronics.

In 1967 I successfully published a major 20-page article in one of the top refereed journals, since ignored. My two later, minor, papers in ProcIEEE have also been ignored. Today, none of the content of my six books on the web, including the one published by Macmillan, has gained entry into any university course or textbook in the world. This led me to jettison the results of my work, and in 1982 I asked an elementary question in classical electrodynamics, now called "The Catt Question". Although all accredited experts avoided making any comment, two such were selected by their superiors and instructed to comment. They totally contradicted each other, and during the next 30 years refused to discuss their contradiction with each other or with us.

For eight years now, a £500 prize is offered to the first student who gets his accredited expert lecturer or textbook writer to comment in writing on "The Catt Question". Recently, the flaws I have found in classical theory have multiplied, some being published in Electronics World. It has taken me incredibly long to see what in hindsight are obvious further flaws, which explains and might somewhat justify the myopia of all accredited experts. No "expert" comments on what I have found.

When, after trying for ten years, I was finally invited to lecture on "The Catt Question" to the Cambridge University Engineering Society, my talk was boycotted by the students as well as by the lecturers. Students do not tolerate doubt being cast on what they are learning.

A politician who once spoke from the same platform as Ken Livingstone told me: "It is important for a politician to not understand something which it is in his interest to not understand." I paraphrase this as "It is important for an established expert to not understand something which it is in his interest to not understand". Certainly, relevant professors protest to third parties (but not to me) that they cannot understand what I am getting at, when I think my communication is very clear, for instance in "The Catt Question".

"Crimestop means the faculty of stopping short, as though by instinct, at the threshold of any dangerous thought. It includes the power of not grasping analogies, of failing to perceive logical errors, of misunderstanding the simplest arguments if they are inimical to Ingsoc, and of being bored or repelled by any train of thought which is capable of leading in a heretical direction. *Crimestop, in short, means protective stupidity."* – G. Orwell, 1984, pub. Chancellor, 1984 edn., p225

However, this letter points to a much more basic problem. Lecturers and textbook writers today have very little grasp of their theory, the classical theory. In particular, they do not grasp the Transverse Electromagnetic Wave, particularly the step, travelling at the speed of light guided by two conductors. This is the basic building block of 95% of all electronic equipment – the way a logic gate signals to another logic gate. For more than a decade, my website, no. 2 Google hit for TEM, has the title "The TEM Wave; a lost concept" or "Transverse Electromagnetic Wave".

In the last century, no textbook mentioned the relative phase of E and H in a TEM sine wave. The lecturer is not helped when the third hit in Wikipedia gives the wrong relative phase of E and H.

Books on electromagnetic theory "allude" to less and less of the key factors in electromagnetics, for instance even ignoring displacement current, while at the same time advancing from 200pp to 500pp and £20 to £50.

Today's no. 1 hit for TEM, the MIT entry, ahead of my own no. 2 hit, says: "We shall be interested primarily in the sinusoidal steady state. Between the plates, the fields are governed by differential equations having constant coefficients. We therefore assume that the field response takes the form:
$H_z = \text{Re}\ H_z(y)e^{j\omega t}$; $Ex = \text{Re}\ E_x(y)e^{j\omega t}$."
End of MIT quote.

All TEM animations on the web are sinusoidal. This is what traps the lecturer or textbook writer. Knowing the Fourier series, he assumes he can ignore any waveform other than the sine wave, and so he does not think about (or grasp) the very simple voltage step, which is the basis of "The Catt Question", which he therefore cannot cope with. He sees it as an array of sine waves, and so cannot see where the electric charge comes from. Instead, he gets entangled in obscure and irrelevant mathematics, which he dumps on his awed student or textbook reader.

Today's problem is not only that accredited experts around the world do not cope with my advances, including the fatal flaws I point out, or even address them. They do not even have a proper grasp of their own classical theory, having buried it in a mass of sine waves and obscure mathematics, and having ignored the logic step, which is fundamental to today's electronics.

This is very serious, since, as Einstein asserted, electromagnetic theory is a core subject in science.

Ivor Catt

IF YOU WOULD LIKE TO COMMENT
on this subject on any other that you have read on in Electronics World magazine, please write to the Editor at Svetlana.josifovska@stjohnpatrick.com

PLEASE EMAIL YOUR LETTERS TO: SVETLANA.JOSIFOVSKA@STJOHNPATRICK.COM

The publisher reserves the right to edit and shorten letters due to space constraints

Sampling ANALOG SIGNALS

IN A SERIES OF SEVERAL ISSUES, MAURIZIO DI PAOLO EMILIO, TELECOMMUNICATION ENGINEER, SOFTWARE DEVELOPER AND DESIGNER OF ELECTRONIC SYSTEMS, WILL PRESENT A TUTORIAL ON DATA ACQUISITION SYSTEM DESIGN AND, SPECIFICALLY, SAMPLING ANALOG SIGNALS

The aim of this new section is to provide knowledge of the most practical techniques used to resolve problems associated with data acquisition systems.

The definition of proper sampling is quite simple. Suppose you sample a continuous signal in some manner. If you can exactly reconstruct the analog signal from the samples, you must have done the sampling properly (Sample & Hold). Even if the sampled data appears confusing or incomplete, the key information has been captured if you can reverse the process.

The signals we use in the real world, such as our voices, are analog signals. To process these signals in computers, they need to be converted into digital form. To convert an analog signal to a digital form it must be band-limited and then sampled. Signals must be filtered prior to sampling.

Theoretically the maximum frequency that can be represented is half the sampling frequency. In practice a higher sample rate is used for non-ideal filters. The signal is represented as multiples of the sampling period, T, as s(nT), where n is an integer (Figure 1). Typically, an Analog-to-Digital Converter (ADC) would be used to convert voltages to a digital number corresponding to a certain voltage level. The process may be reversed through a Digital-to-Analog Converter (DAC). The sampling theorem (Figure 2) indicates that a continuous signal can be properly sampled, only if it does not contain frequency components above one-half of the sampling rate. For instance, a sampling rate of 2,000 samples/second requires the analog signal to be composed of frequencies below 1000 cycles/second. If frequencies above this limit are present in the signal, they will be aliased to frequencies between zero and 1000 cycles/second, combining with whatever information was legitimately there.

> *A bipolar input stage is used to achieve low offset voltage and wide bandwidth*

To understand this, consider an analog signal composed of frequencies between DC and 3kHz. To properly digitize this signal it must be sampled at 6,000 samples/sec (6kHz) or higher. Suppose we choose to sample at 8,000 samples/sec (8kHz), allowing frequencies between DC and 4kHz to be properly represented. In this situation there are four

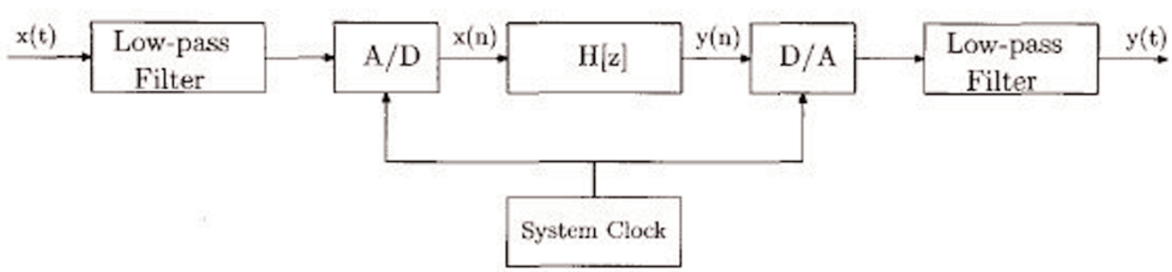


Figure 1: Typical signal processing system

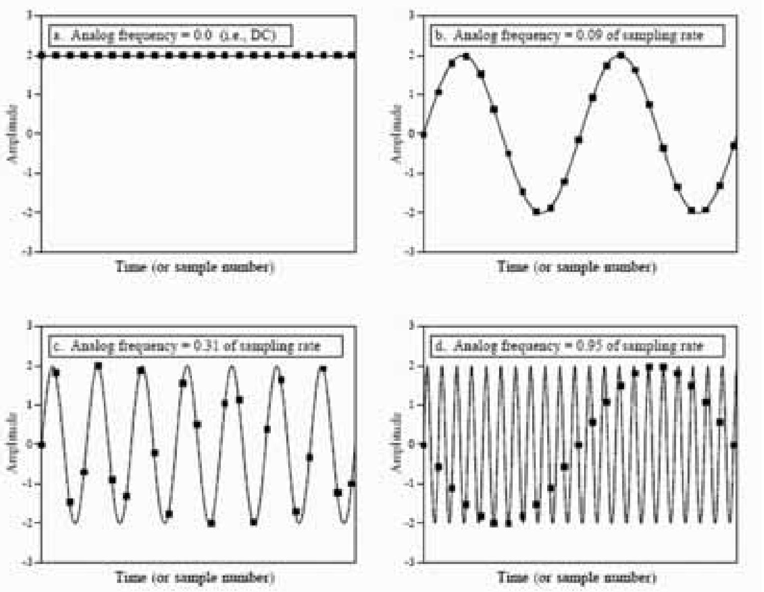


Figure 2: Sampling theorem

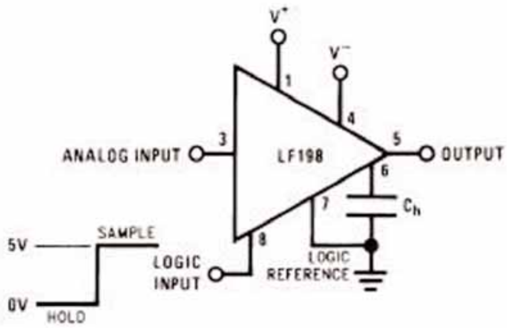


Figure 3: LF198

important frequencies: (1) the highest frequency in the signal, 3kHz; (2) twice this frequency, 6kHz; (3) the sampling rate, 8kHz; and (4) one-half the sampling rate, 4kHz.

The LF198/LF298/LF398 (Figure 3) are monolithic sample-and-hold circuits which use BI-FET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift.

In mathematical terms, the sampling theorem (Nyquist) states that if an analog signal s(t) has a band-limited Fourier transform $S_{a(i\omega)}$ given by:

$$S_{a(i\omega)} = \int_{-\infty}^{+\infty} s(t)\exp(-i\omega t)\,dt$$

such that:

$$S_{a(i\omega)} = 0$$

for:

$$\omega \geq 2\pi W$$

Then the analog signal can be reconstructed from its sampled version if:

$$T \leq 1/2W$$

The quantity W is called the Nyquist frequency.

Various types of distortion can occur, including:

- **Aliasing**. A precondition of the sampling theorem is that the signal be band limited. However, in practice, no time-limited signal can be band limited. Since signals of interest are almost always time-limited (e.g. at most spanning the lifetime of the sampling device in question), it follows that they are not band limited. However, by designing a sampler with an appropriate guard-band, it is possible to obtain output that is as accurate as necessary.
- **Jitter** or **deviation** from the precise sample timing intervals.

An anti-aliasing filter is a filter used before a signal sampler, to restrict the bandwidth of a signal to approximately satisfy the sampling theorem. Anti-aliasing filters are commonly used at the input of digital signal processing systems, for example in sound digitization systems; similar filters are used as reconstruction filters at the output of such systems, for example in music players.

The LTC1564 (Figure 4) is a continuous time filter for anti-aliasing, reconstruction and other band limiting applications. No other analog components or filter expertise are needed to use it. There is one analog input pin and one analog output pin. The cutoff frequency (f_c) and gain are programmable while the shape of the lowpass response is fixed. ●

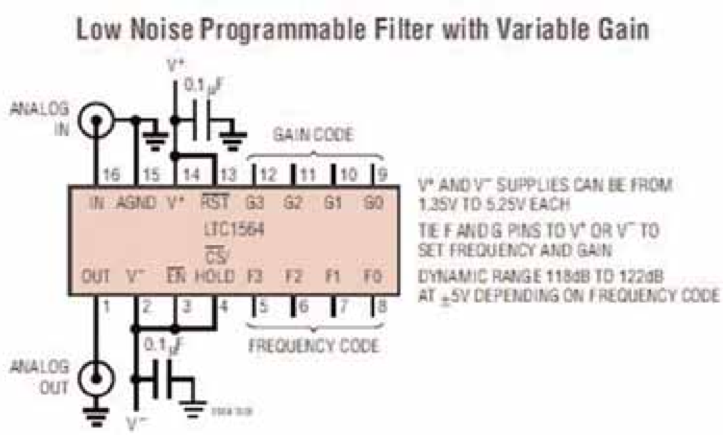


Figure 4: LTC1564

DUAL µMODULE DC/DC REGULATOR PRODUCES HIGH EFFICIENCY 4A OUTPUTS FROM A 4.5V TO 26.5V INPUT

BY **ALAN CHERN**, ASSOCIATE DESIGN ENGINEER AT LINEAR TECHNOLOGY

Systems and PC boards that use FPGAs and ASICs are often very densely populated with components and ICs. This dense real-estate (especially the supporting circuitry for FPGAs, such as DC/DC regulators) puts a burden on system designers who aim to simplify layout, improve performance and reduce component count.

New families of DC/DC µModule regulator systems with multiple outputs are being designed to dramatically reduce the number of components and their associated costs. These regulators are designed to eliminate layout errors and to offer a ready-made complete solution. That way only a few external components are needed since the switching controllers, power MOSFETs, inductors, compensation and other support components are all integrated within the compact surface mount 15mm × 15mm × 2.82mm LGA package. Such easy layout saves board space and design time by implementing high density point-of-load regulators.

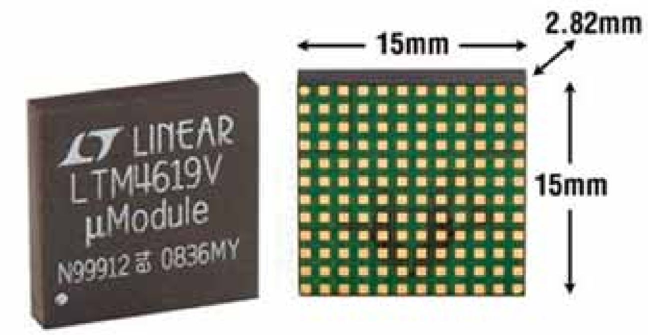
> *The common mode output voltage can be anywhere and still result in a "zero" differential input voltage because the feed-back is symmetric*

One such DC/DC µModule regulator system is the LTM4619 switching DC/DC µModule converter which regulates two 4A outputs from a single, wide, 4.5V to 26.5V input voltage range. Each output can be set between 0.8V and 5V with a single resistor. In fact, only a few components are needed to build a complete circuit (see Figure 2).

Figure 2 shows the LTM4619 µModule regulator in an application with 3.3V and 1.2V outputs. The output voltages can be adjusted with a value change in RSET1 and RSET2. Thus, the final design requires nothing more than a few resistors and capacitors. Flexibility is achieved by pairing outputs, allowing the regulator to form different combinations such as single input/dual independent outputs or single input/parallel single output for higher maximum current output.

The efficiency of the system design for Figure 2 is shown in Figure 3 and power loss is shown in Figure 4, both at various input voltages. Efficiency at light load operation can be improved with selective pulse-skipping mode or Burst Mode operation by tying the mode pin high or leaving it floating.

Figure 1: The LTM4619 LGA package is only 15mm × 15mm × 2.82mm and houses dual DC/DC switching circuitry, inductors, Mosfets and support components

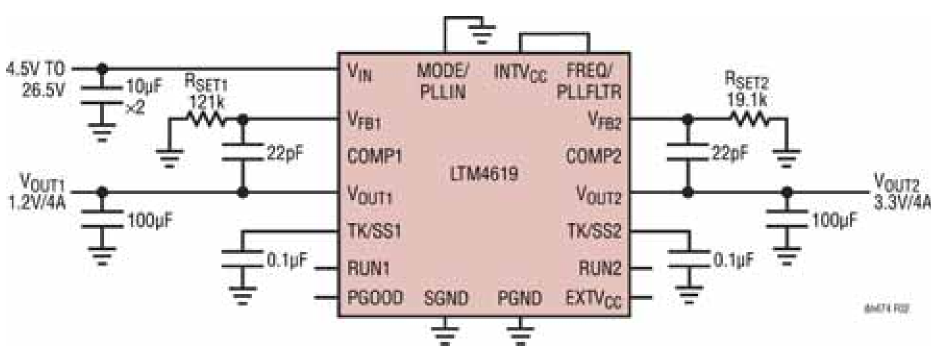


Multiphase Operation for Four or More Outputs

For a 4-phase, 4-rail output voltage system, use two LTM4619s and drive their MODE_PLLIN pins with a LTC6908-2 oscillator, such that the two µModule devices are synchronized 90° out of phase.

Synchronization also lowers voltage ripple, reducing the need for high voltage capacitors whose bulk size consumes board space. The design delivers four different output voltage rails (5V, 3.3V, 2.5V and 1.8V) all with 4A maximum load.

Figure 2: 4.5V to 26.5V input to dual 3.3V and 1.2V outputs with 4A maximum output current each



Thermal Performance

The thermal performance is shown in Figure 5, where the unit is operating in parallel output mode; single 12VIN to a single 1.5VOUT at

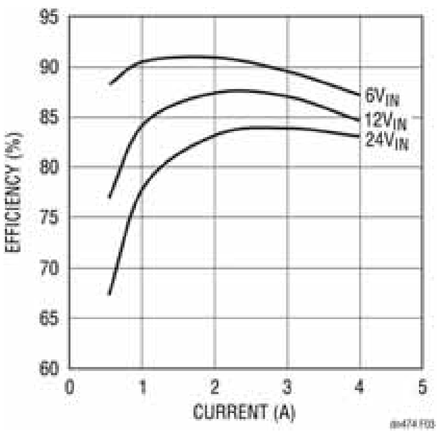


Figure 3:
Efficiency of the circuit in Figure 2 at different input voltage ranges for 3.3V and 1.2V outputs

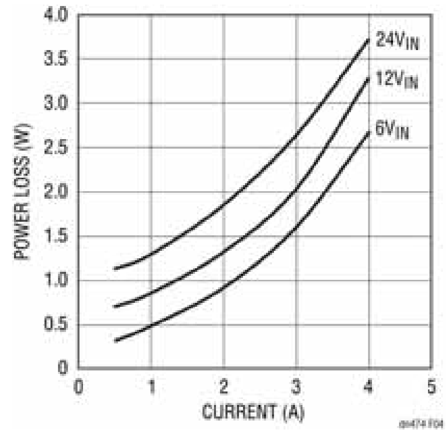


Figure 4:
Power loss of the circuit in Figure 2 at different input voltages for 3.3V and 1.2V outputs

8A. Both outputs tied together create a combined output current of 8A with both channels running at full load (4A each). Heat dissipation is even and minimal, yielding good thermal results. If additional cooling is needed, add a heat sink on top of the part or use a metal chassis to draw heat away.

Easy Conversion

The LTM4619 dual-output μModule regulator makes it easy to convert a wide input voltage range (4.5V to 26.5V) to two or more 4A output voltage rails (0.8V to 5V) with high efficiency and good thermal dissipation. Simplicity and performance are achieved through dual-output voltage regulation from a single package, making the LTM4619 an easy choice for system designs needing multiple voltage rails. ●

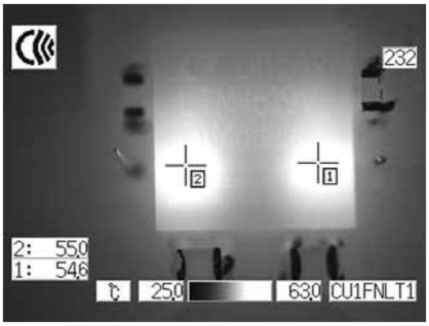
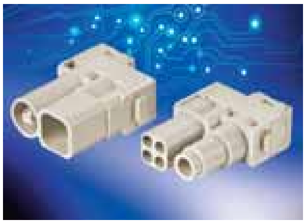


Figure 5:
The thermal performance of a paralleled output μModule regulator LTM4619 (12VIN to paralleled 1.5VOUT at 8A load)



Hybrid Connector Module Combines Power-Supply and Signal Contacts

Power supply and signal contacts are combined in the new Han 70 A Hybrid Module: the latest model in Harting's Han-Modular highly flexible open connector system.

The Han 70 A Hybrid Module has a power contact with a current capacity of 70A at a rated voltage of 1000V, and four additional signal contacts designed for up to 400V based on standard Han E crimp contacts rated at up to 16A.

The power contact has axial screw terminals. Cables measuring from 6 to 22mm^2 (8-4 AWG) can be connected without using an expensive special tool. A secure and durable connection can be made with a standard 2.5mm hexagon screwdriver.

Harting's Han-Modular series enables users to create their own customised connector to the desired configuration. Various modules are available for electrical, optical and gaseous signals, and the range is constantly updated.

www.harting.com

D-Subminiature Connectors with Mixed Contact Sizes To Suit Many Applications

Lane Electronics has made available the Positronic Combo D-Subminiature Series designed for professional, industrial and military applications. The D-Subminiature connectors feature mixed contact sizes for signal, power, coax, thermocouple and high voltage applications and are ideal for use as an input/output connector interface. Positronic's PosiBand closed entry contact is available as an option.

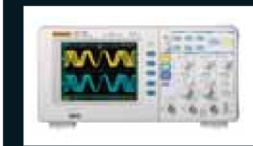
There are 22 contact variants and six shell sizes in the Combo D-Subminiature series; users can mix contact types in a single package. These are size 20 contacts for signal, power and thermocouple, and size 8 for all other applications. Current per contact is a maximum of 100A. A key feature is Positronic's large surface area (LSA) contact system as well as a wide variety of options and accessories.

These include solder PCB mount, crimp, solder, busbar and press-fit terminations, co-planar mounting and sequential mating options, and a contact stabilization option for those applications where reducing "float" in size 8 contacts is necessary or desirable.

www.fclane.com

Closing date for the competition is 31st May 2012.

WIN A RIGOL DS1052E OSCILLOSCOPE WITH RIGOL/TELONIC AND ELECTRONICS WORLD!



Telonic has recently been awarded UK distribution of Rigol test and measurement equipment. To celebrate this new partnership Telonic is offering one lucky Electronics World reader a chance to win its flagship digital oscilloscope – the Rigol DS1052E oscilloscope – worth £245 + VAT.

All you have to do is answer the question below.

What is the bandwidth of the DS1052E?

A. 20MHz

B. 40MHz

C. 50MHz

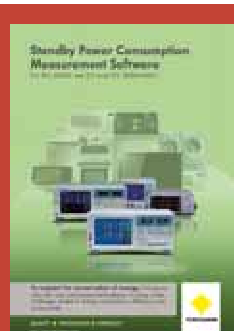
Email your answer A, B or C to rigol@electronicsworld.co.uk providing your name, address, company name, job title and email address.

We will announce the winner in a future issue. The winner will be contacted by email and the kit will be dispatched by post free of charge.

To find out more about the oscilloscope, visit

http://www.rigol-uk.co.uk/ds1000e-series-digital-oscilloscope/

POWER MEASUREMENT SOFTWARE PROVIDES COMPLETE SOLUTION FOR THE LATEST TESTING STANDARDS



A new power measurement software package for the Yokogawa range of precision power analysers provides a complete solution for the testing of standby power in accordance with the latest IEC62301 Ed.2.0 (international) and EN50564:2011 (European) standards.

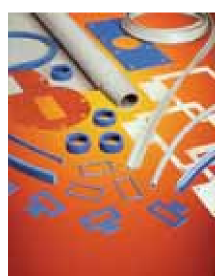
The software is designed for use with the Yokogawa WT210, WT500, WT1800 and WT3000 power analysers, and is targeted at manufacturers of domestic electrical appliances and related equipment, who need accurate measurements to ensure their products operate at optimum energy efficiency with minimum standby power consumption.

"A recent estimate that by 2020 appliances using standby mode will contribute as much as 50 terawatt-hours of electricity consumption per year – similar to the annual electricity consumption of a country such as Portugal or Greece – emphasises the importance of this issue. Ensuring that manufacturers improve the efficiency of equipment in the standby mode can lead to significant reduction in electricity consumption," said Terry Marrinan, Yokogawa's Vice President, Test & Measurement, for Europe & Africa.

www.tmi.yokogawa.com

Conductive Elastomer Selector Guide Matches CHO-SEAL Materials to the Application

The new Conductive Elastomers Selector Guide from Chomerics Europe provides comprehensive details of the company's range of CHO-SEAL moulded and extruded EMI gaskets. The guide helps designers choose the appropriate format – moulded or extruded, and the best combination of physical properties and shielding performance for their product designs. By using a range of elastomers combined with conductive filler materials, Chomerics is able to meet the wide ranging shielding and gasket requirements for applications ranging from aerospace to consumer electronics.



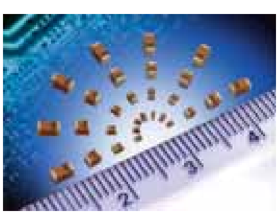
CHO-SEAL conductive elastomers are reliable over the life of the equipment in which they are installed. The same gasket provides both an EMI shield and an environmental seal. CHO-SEAL elastomer gaskets have a range of attributes including resistance to compression set, suitability for use with low closure forces, and high tensile strength. They can also offer corrosion, chemical and fluid resistance plus flame retardancy.

www.parker.com/chomerics

AVX Tantalum Chip Capacitors Deliver Higher CV Than X5R Dielectric Ceramic Devices

AVX Corporation has more than doubled the volumetric efficiency of its tantalum technology, enabling latest versions of its TACmicrochip capacitor to deliver 15µF/4V and 10µF/6V from a 0402 chip. The CV performance of these TLC series devices is even greater than ceramic MLCC devices using the X5R dielectric.

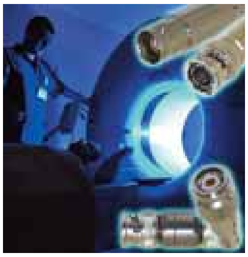
The design of the TACmicrochip capacitor series eliminates the need for moulded plastic from the packaging that is required in traditional designs, allowing much greater capacitance to be squeezed into a given package. This has increased the volumetric efficiency from less than 15% to approaching 50%, making them applicable for a much wider range of uses.



Several series of TACmicrochip are available. High CV 15µF/4V, 10µF/6V TLC parts suit miniature application such as hearing aids, ultra-thin smart phones and tablet PCs. These devices are very stable; for example capacitance does not drop with applied DC voltage or AC ripple voltage.

www.avx.com

INTELLICONNECT EXTENDS RANGE OF WEATHERPROOF TRIAXIAL CONNECTORS



Intelliconnect (Europe) Ltd has extended its market leading range of high-reliability triaxial connectors to include various adaptors and bulkhead mount jacks for several different cable types. These are available in the two existing families of Triax connectors; the TRB series of bayonet couple connectors and the TRT series which features a threaded coupling sleeve.

The high quality connectors are manufactured in the UK, are suitable for high or low volume applications, feature a high integrity clamp construction and are weatherproof.

Key features of Intelliconnect's Triax connectors include low noise, isolated ground, non-constant impedance and suitability to be used with both Twinax or Triax cable types.

Triaxial connectors are commonly used in industrial, broadcast and medical applications, including nuclear medicine, camera cables where reduced 'noise' or interference levels are required, and to ensure accuracy of measurements in medical dosiometry systems. Their standard double screening makes them useful in military and aerospace applications.

www.intelliconnect.co.uk

Mouser Launches Intelligent Bill of Materials Management Tool

Mouser Electronics announced a new Bill of Materials (BOM) Tool on its award-winning website Mouser.com. The innovative tool promises to transform customers' imported bill of materials into an industry-leading part search and purchasing platform.

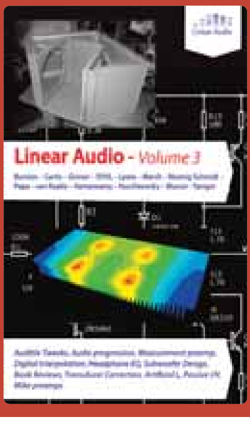
Mouser's new BOM Management Tool is available to anyone with a 'My Mouser' account, enabling users to import a new BOM or view BOMs saved in their account.

With its broad product line and unsurpassed customer service, Mouser caters to design engineers and buyers by delivering What's Next in advanced technologies.

http://uk.mouser.com/bomtool/

VOLUME 3 ISSUE OF LINEAR AUDIO IS OUT NOW

In the latest issue of Linear Audio – Linear Audio Volume 3 – a team of recognised authors has created interesting, entertaining and project-ready articles.



Richard Burwen starts off by explaining how audio tweaks that 'cannot work' may still cause audible differences. Then there are a couple of tutorials: How signal interpolation can improve DAC performance, and how to design that great class-A enclosure from a thermal and dissipation point of view.

Several circuit design articles follow: a headphone buffer/amp with in-ear equalization; the long-awaited Part II of Scott Wurcer's mic preamp article; how to correct for cartridge resonance; and a pair of passive, discrete DAC I/V converters.

On the speaker front there is an article on how to design a subwoofer for THX performance, while labs get a boost from a floating simulated inductor from 10mH to 10H for filter and xover experiments, and a low noise, lab-grade measurement preamp.

Stan Curtis reviews the state of audio and concludes that lots of work still has to be done, especially in digital.

www.linearaudio.net

HARWIN INSTALLS NEW WATER TREATMENT PLANT

Harwin has invested in a new water treatment plant at its UK headquarters and manufacturing facility in Portsmouth, improving the quality of finish of its plated parts and reducing the environmental impact.

Unlike many connector makers, Harwin is a vertically-integrated manufacturing company which keeps not only plating, but all other essential manufacturing operations under one roof. This enables the company to be very innovative and responsive. Utilising previous technology and due to the company's strong growth, the company was using to 7,000 litres of water per hour; the new facility means that the company will use that same amount of water in two weeks.

The new plant which uses resin filter technology, supplied by PureTech, cleans all the rinse water and recycles it back into the plating area. In an industry first for tin, the heavy metals – gold and tin – cleansed from the water can be reclaimed.

www.harwin.co.uk

Mateleco Named 'Best Distributor in France' By RF Connector Maker Radiall

TTI Inc announced that Mateleco, the French connector distributor acquired by TTI over three years ago, has recently been named 'Best Distributor in France' by connector maker Radiall.

Radiall is a global firm designing, developing and manufacturing RF coaxial connectors, antennas, microwave components, fibre optic and multipin connectors, offering an extensive range of interconnect solutions for demanding applications in telecommunications, aerospace, space, defense, automotive, industrial, medical and instrumentation.

"Recently, for the first time Radiall hosted a conference with our distributor partners to assess the market and discuss our strategy. Following the meeting it was our pleasure to present Mateleco with the 'Best French Distributor in 2011' award, recognising their performance," said Pascale Letteron, Distribution Manager for France at Radiall.

Michel Piana, General Director for Mateleco replied: "We have great pleasure in receiving this honour that demonstrates the close co-operation between our two companies. We are enthusiastic and very motivated to try to repeat our success in the coming year."

www.ttieurope.com

LNBR VOLTAGE REGULATOR IC FOR SATELLITE TV RECEIVERS

The A8303 from Allegro MicroSystems Europe is a new addition to the company's family of LNBR (low-noise block regulator) ICs for use in satellite receivers and LCD TV "combo" receivers. The new device uses small ceramic capacitors rather than electrolytic devices to provide a lower profile solution, as well as incorporating a key output voltage setting (15.6V) to accommodate design requirements specific to the Japanese market.

The A8303 is a single-channel LNBR IC that offers industry-leading internal protection and robustness, an integrated boost MOSFET, current sensing and compensation which simplifies the design and minimises component count and PCB size. The A8303 has a low supply current to save energy, incorporates a high level of diagnostics and features a resistor-programmed output current limit to minimise the boost inductor/diode size and hence costs.

The A8303SESTR-T is available in a 4 × 4 TQFN/MLP-20 package.

www.allegromicro.com

36V NANO CURRENT VOLTAGE MONITOR TARGETS MULTICELL APPLICATIONS

Linear Technology Corporation introduces the LTC2960, a 2.5V to 36V, two input voltage monitor that draws only 850nA of quiescent current, offering extended battery life in battery-powered applications.

The LTC2960 provides two adjustable monitoring inputs that can be configured to provide undervoltage (UV) or overvoltage (OV) monitoring, low battery indication, undervoltage lockout (UVLO), power supply sequencing signals or a high voltage window comparator for microprocessor, DC/DC switcher or LDO based systems. The LTC2960 fulfills a broad range of battery-powered, portable application requirements with its wide voltage operation and low current consumption in a tiny 2mm x 2mm DFN or ThinSOT package.

This unique feature set differentiates the LTC2960 for low power voltage monitor applications and makes it ideal for multiple Li+ coin cells, AAs, AAAs and other compact battery-powered or "green" applications. The ±1.5% accurate reset, undervoltage and overvoltage monitoring thresholds are easy to configure with external resistors.

www.linear.com

POWERSOLVE ANNOUNCES PP3 EQUIVALENT PRIMARY AND RECHARGEABLE LITHIUM BATTERIES

Power supply specialist Powersolve announces two new series of Lithium batteries designed to replace 9V PP3 batteries in applications that require long life, a stable operating voltage and a very low self-discharge rate. The G600 Series consist of rechargeable Lithium Polymer batteries while the CP9V Series comprises Lithium Manganese Dioxide primary batteries.

G600 Series batteries are reusable alternatives to standard PP3 format alkaline batteries. They have a rated capacity of 600mAh and feature a standard charge cycle of four hours. These G600 batteries do not suffer from memory effects and come with a protective circuit module (PCM) which protects against over-charging, over-discharging and over-current.

With a nominal capacity of 1200mAh, CP9V batteries feature a maximum continuous current of 400mA, a maximum pulse current of 800mA and a self-discharge rate of less than 2% per annum @ 30°C. Housed in an ABS case weighing just 33 grams, these batteries operate at temperatures up to +60°C.

www.powersolve.co.uk

AMD EMBEDDED G-SERIES BASED COMS FOR PCI-BASED DESIGNS

Kontron announced the availability of two new variants to enhance its COMe-cOH# range of COM Express compact Computer-on-Modules. The new modules are dedicated to PCI-based designs and are based on the energy-efficient AMD Embedded G-Series accelerated processing units (APUs).

The compact Kontron COMe-cOH2 provides increased graphics performance to SFF COM Express applications with pin-out type 2, as well as parallel processing capability and low power consumption. OEMs and system developers can also use the new modules as a drop-in replacement to upgrade their existing applications, thereby improving their return on investment.

With support for Direct X 11 and OpenGL 4.0, the Kontron COM Express compact Computer-on-Modules COMe-cOH2 provide the latest graphics features and bring a new user experience to SFF gaming and Kiosk POI/POS systems. Even with high graphics performance, their optimized energy efficiency simplifies the design of appliances with tight power and thermal restrictions.

www.kontron.com

PCB MOUNTING DISC THERMOSTATS

Asahi's US-802 series of miniature disc thermostats has been designed to solve over-temperature problems in tight spaces in electronic and electrical equipment.

Manufactured in a neat TO-220 size case, the US-802 can be supplied with calibrations from 40°C to 120°C and with either normally-closed or normally-open contacts. Tolerances are as low as ±5K and with a 15K temperature differential, the US-802 provides close temperature monitoring of heat sinks and power components. Fitted with gold-plated contacts, they offer reliable logic level switching but can also switch

up to 1A at 48VDC or 125VAC.

The US-802 also carries UL, C-UL and VDE approvals.

Call today for samples and application advice.

www.atcsemitec.co.uk

UNIVERSITY OF OXFORD

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The University of Oxford offers one of the finest programmes of short courses for professionals in the European electronics and telecoms industries.

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www.conted.ox.ac.uk/electronics

CREE AND THE NOUN PROJECT COLLABORATE TO CREATE THE NEXT "BRIGHT IDEA"

Cree and The Noun Project are working together to help create universally recognizable symbols for LED lighting and other energy-efficient technologies.

"We're continuing to raise people's awareness of the LED lighting revolution, bringing together leading creative minds to help us establish a symbol to represent LED lighting," said Ginny Skalski, Social Media Specialist at Cree. "[By creating standard symbols] the world will no longer be forced to use the inefficient, old-school incandescent light bulb to represent bright ideas or the toxic, mercury-filled CFL to represent efficient lighting."

Earlier in the year, the two organizations sponsored an event called Iconathon at the Cree campus in Durham to create the universally recognizable symbols for LED lighting. The event included presentations from Edward Boatman, co-founder and creative director of The Noun Project, and Paul Pickard, a lighting revolutionary and systems architect at Cree. During the half-day design workshop, attendees helped craft the basis of a new symbol for LED lighting and other important energy-saving technologies, including solar panels, weatherized homes and wind turbines. The final symbols will later be added to the public domain and available for anyone to download from TheNounProject.com, a growing open sourced visual library of symbols and icons that form the world's visual language.

IVOR CATT, Engineer and Scientist, UK: Symbols for components can have drastic implications. The symbol for a capacitor has been extremely damaging, convincing everyone subliminally that the leads enter a capacitor at the middle. This blocks the realisation published in Wireless World in December 1978 that a capacitor is a transmission line. Both are entered at one end. In case of a capacitor, the displacement current creates magnetic field. In the case of the transmission line, it must not create magnetic field because that would undermine the TEM step as it progresses to the other end of the capacitor.

Classical electromagnetic theory survives because of this wrong symbol.

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, Italy: LEDs are more than twice as efficient as compact fluorescent bulbs, currently the standard for greener lighting. They represent the most significant development in lighting since the invention of the electric light more than a century ago.

The key strength of LED lighting is reduced power consumption. When designed properly, an LED circuit will approach 80% efficiency, which means 80% of the electrical energy is converted into light energy.

It will be interesting to see what developments are coming for residential applications of LED lights. LED lighting technology has been researched and developed for the past two decades and we are beginning to see practical applications from these efforts.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: I think it's about time that we stop using energy-wasting traditional light bulbs and increase public awareness of the use of energy-efficient LED lighting. The introduction of new symbols will no doubt raise people's awareness of the LEDs and encourage their use even further, thanks to Cree and the Noun Project who are leading the way in this new LED lighting revolution.

I like the approach that "bright ideas" hopefully will no longer be represented by the old light bulbs!

I like the approach that "bright ideas" hopefully will no longer be represented by the old light bulbs!

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Nowadays the technological evolution does not cease presenting innovations to us. Thus if one decides to develop the LED for public use it is necessary to standardise the symbols and international references.

The workshop, organized by Cree and Noun Project, is an intelligent and useful idea because it makes it possible to better understand the strength of LED technology. Let us not forget that we seek a better world which preserves the environment from pollution. Indeed, the characterization and the standardization of this lighting system will play a significant role in the development of LED technology.

The exploitation of green energies at this stage is very encouraging. All this effort will bear fruit with a control of new concepts having high energy-efficiency. I believe that the world can advance towards a much better future by developing technological science in this way and by reasonable human thought.

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: This is a clever exercise in marketing. But to be able to design universally recognisable symbols is probably not achievable. Consider the case of road traffic management signs: every country has its own set, even though they are all designed to convey the same, or similar, message. There is also only a limited set which all drivers can assimilate and this is a deep subject which has been long studied and argued over.

So, in relation to iconography for devices, there is far more scope and freedom to experiment, but who shall hold the IP rights for successful designs here?

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector please register your interest with the editor by writing to Svetlana.josifovska@stjohnpatrick.com