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Power Supplies: Make or Buy? Mouser Helps You Decide.

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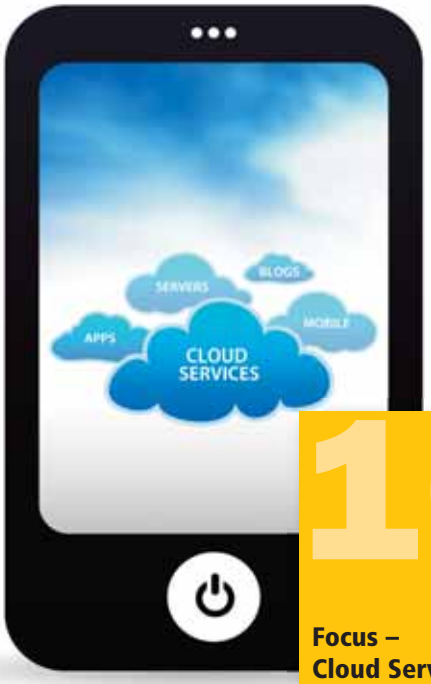

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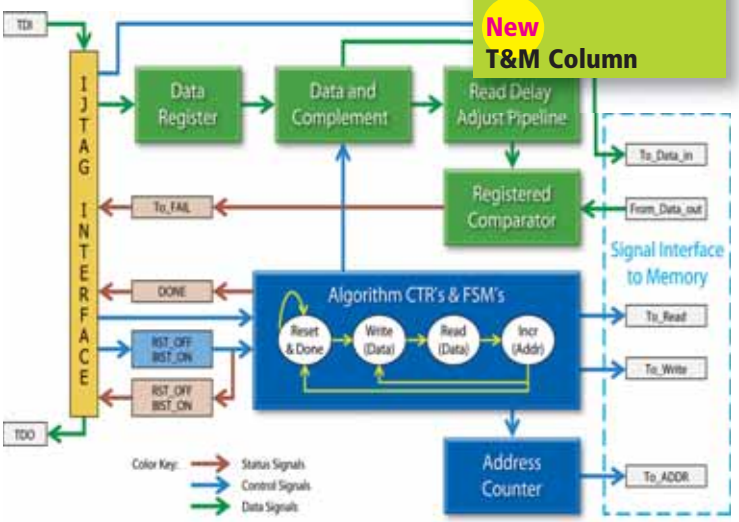

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THE 'INTERNET OF THINGS' OPPORTUNITY FOR INTELLIGENT DEVICE MANUFACTURERS

The trend of pervasive Internet is already gaining hold, and today is described in a number of ways in different industries: intelligent device management, telematics, telehealth, smart road, M2M communications etc

Market analysis firm Gartner says the 'Internet of Things' is on the horizon. The 'Internet of Things' is a phrase used to describe how the Internet will link smart devices, conventional goods and physical assets to allow them to generate and share data. Nearly every product will have a URL – not just smart devices, but even industrial equipment such as buildings, medical devices, telecommunications equipment, test and measurement equipment, oil and gas machinery and so on – that will link to content and services via the web.

This isn't blue sky thinking. Gartner recommends that CIOs and IT leaders set aside a couple of days to develop a strategy for this scenario. The trend of pervasive Internet is already gaining hold, and today is described in a number of ways in different industries: intelligent device management, telematics, telehealth, smart road, M2M communications – to give some examples. Market analysts at Analysis Mason forecast that there will be 2.1 billion M2M connected devices by 2020. According to research consultancy Berg Insights, in December 2011 there were 29.5 million M2M subscriptions in Europe alone.

Opportunity beckons intelligent device manufacturers. They must evolve their products from fixed function and disconnected systems to flexible and seamlessly connected devices. Making products smarter will extend their life, enable the creation of new revenue streams, automate support, reduce manufacturing costs and grow the customer base. In doing so, manufacturers will transform their devices into platforms, and therefore greatly expand their market reach, increase profitability and achieve business goals.

Embedded licensing and entitlement management software is the enabling technology that can help intelligent device manufacturers make their products suitable for a pervasive Internet environment. It offers capabilities that allow manufacturers to personalise offerings without having to manufacture multiple models. Simple changes to the embedded software in the device enable manufacturers to customise the product based on customer needs by managing how it behaves – i.e. by activating or deactivating features, setting device capacity and controlling its behaviour. This greatly simplifies product lifecycle management and facilitates supply chain management. The usage data provided by the embedded software can offer insight into how customers are using hardware, what software they use most often and new services that could potentially be created.

Further, product usage information can enable manufacturers to make conscious choices pertaining to trade-offs between cost and value of service when packaging products and services for customers and markets. Already there are sophisticated embedded licensing and entitlement management solutions available that are enabling intelligent device manufacturers to tailor their approach to product development and business to meet the demands of a highly competitive and connected marketplace.

In a world where the number of devices outnumber people, a pervasive Internet landscape is a certainty. Intelligent device manufacturers must transition to the concept of the 'Internet of Things' by thinking and acting like software companies, not simply product manufacturers. Key to their success will be their ability to understand and adopt a software-centric approach to manufacturing and selling hardware. By leveraging embedded software for licensing and entitlement management, they will create connected devices that unlock new revenue streams, protect intellectual property and implement configure-to-order manufacturing, dramatically reducing inventory while facilitating greater responsiveness to changing market conditions.

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ALTERA JOINS THE 'BIG GUNS' LEAGUE WITH ITS LATEST TECHNOLOGY INNOVATIONS

Programmable logic supplier Altera is entering the ranks of serious silicon technology innovators, traditionally reserved for the likes of Intel, Samsung or ST. Last month it unveiled several key innovations planned for its next generation 20nm products, as well as its vision for future devices such as 3D ICs.

Its new 20nm mixed-system fabric uses a raft of architectural, software and process innovations to deliver a platform that combines hardware programmability of FPGAs, software flexibility of DPSs and microprocessors, and with efficiencies of application-specific hard IP, including 40Gbps transceiver technology.

"Silicon convergence is a big part of our strategy," said Brad Howe, senior VP of R&D at Altera. "We are looking at heterogeneous 3D ICs, with our partner TSMC, which already has its '20SoC' technology, and we'll be basing our products on that."

Among Altera's 3D IC plans are to have a chip that will combine memory and FPGA blocks on one die, then stack other dies on top of it, including an optical module, third party Asic as well as its own IP Asic.

"There will be at least a 10 times increase in system integration [with 3D ICs]," added Howe, "along with an increase in performance but a reduction in system power, board space and system cost."

Although this vision promises a lot, it may not come to fruition any time soon, since the EDA industry has yet to deliver the tools that will support such complex devices.

"3D ICs are a nice vision, but the [EDA] industry is not ready. [The] EDA [industry] has nothing for multi-die environments tool-wise," said Howe. However, as EW went to press, EDA products supplier Synopsys announced it has released enhanced versions of its Galaxy Implementation Platform to deliver a comprehensive 3D IC design solution. It is included in TSMC's new CoWoS Reference Flow to allow a "seamless" move from traditional 2D IC design to multi-die devices.

Among the other innovations Altera unveiled last month are the 40Gbps chip-to-chip transceivers and 28Gbps backplane, and a variable precision DSP block that delivers over 5 TFLOPs of IEEE 754 floating-point performance, all based on the new 20nm mixed-system fabric. The fabric has been optimized through power management techniques, including adaptive voltage scaling, proprietary programmable power technology and optimized process technology to offer reduced device power consumption (dynamic and static power) of up to 60% compared with its previous generation of devices.

The first 20nm products are expected next year.

Altera's vision of a heterogeneous 3D IC

Teledyne LeCroy Debuts Two High Definition Oscilloscope Series with 12-Bit ADC, Providing 16 Times More Resolution

Teledyne LeCroy's new HD4096 High Definition technology is the platform for two new series of oscilloscopes launched this month - the HDO4000 and HDO6000.

The technology is based on Teledyne LeCroy's own high sample-rate 12-bit ADCs, amplifiers with high signal-to-noise ratios and low-noise system architecture. The technology enables these oscilloscopes to capture and display signals of up to 1GHz with 2.5GS/s sample rate and offer 16 times more resolution than other oscilloscopes.

"The number of bits in the ADC determines the resolution of the oscilloscope," said Dan Monopoli, marketing director at Teledyne LeCroy. "The higher resolution in an oscilloscope means it can show finer details and make more accurate measurements."

In the new HDO scopes, for a 12-bit ADC the number of quantization levels is 4096 (based on 2^N), giving a dynamic range of ~ 72dB. With 16 times more vertical resolution than traditional 8-bit instruments, it renders much cleaner and sharper waveform displays. The waveform details which were previously difficult to see can now be easily distinguished and measured.

In addition, Teledyne LeCroy used its own low noise system architecture. "This is a new approach to system architecture," said Monopoli. "You have to work on the redundancy noise so you don't analyse noise. The power supply is the biggest source of noise. It finds itself on the input signals."

The HDO4000 and HDO6000 are available in bandwidths from 200MHz to 1GHz. All HDO models have a large 12.1" touch-screen display and intuitive interface to enhance operation. In addition, they provide powerful debug tools and a comprehensive set of automatic measurements and waveform maths capabilities.

The tools include WaveScan search and find, history mode waveform playback, sequence acquisition mode and LabNotebook report generation. Spectrum-analysis and power-measurement software packages extend the oscilloscopes' capabilities.

The HDO4000 series is aimed at applications that require easy measure and fast debug, whereas the HDO6000 targets applications that also need advanced analysis.

Teledyne LeCroy's new HDO6000 series offers easy measure, fast debug and advanced analysis

POWER SUPPLIES – MAKE OR BUY?
MOUSER ELECTRONICS HELPS YOU DECIDE

Individually, the component cost of a power supply is high compared to an off-the-shelf standard power supply without considering labor. An off-the-shelf power supply may come with a five-year warranty, as well. Thus, it makes sense to design only what you cannot buy.

But sometimes you might need a power supply that is very unique and specialized. Many companies attempt their own design. Some are successful but many incur large expenses, wasting precious time-to-market because they simply do not know how to design power supply systems that are stable, reliable, manufactured in high volume, and operate over long periods of time. Mostly, they don't know when to design it themselves and when to buy what they need. Whether you buy or make, Mouser Electronics is there to help.

WHEN TO BUY

Many times, one is told to "get that $40 dollar part out of the networking system to cut the cost." After all, it's just a power supply and any fresh young engineer can do that. No? "Often, organizations with core competencies other than power electronics do not have the proper background, people, or test equipment and are unaware of associated issues," says Mark Burr-Lonnon, Mouser Electronics' Vice President of EMEA Business. "They dive head first into an area they are ill-prepared to navigate. The mistake is assuming that power supplies can be designed by anyone." Why are companies outsourcing manufacturing to EMSI providers? Simply put, it costs them less and they can do a better job than in-house assembly. Consider also that your customers may have more demanding customers than you. The quality, reliability and cost have been beaten out of the process with a bigger stick than just your organization does by itself. Don't assume that in-house design and production of power supplies will save on total cost.

WHEN TO MAKE

Sometimes you cannot avoid it; you must make your own power supply. When does it make sense to build your own?

1. You can't buy what meets your needs commercially.
2. The requirement for designing your own supply can be handled with off-the-shelf semiconductors or power-supply-on-chip parts that are well supported by applications engineering staff and design tools.
3. You have access to proper test equipment and have the expertise to do the job properly.
4. There is time to do it right. Assume that nothing will be well-behaved.
5. Buying is really too much cost to justify, you will build enough to make a difference, and you feel you can do the job right.

If you consider these conditions and decide to design, the good news is that there is more support than ever before. "New developments in technology available from Mouser include products for many levels of power converter powers," Burr-Lonnon adds. "Recent technology includes digital control for power, which allows, via a GUI, the ability to design and modify margining and sequencing, and designing, configuring, and modification of the control loop."

Although excellent resources are available, the best advice on using reference designs is that you should not put responsibility for the design on component suppliers without some self-effort. The designer and the company with the final product are ultimately responsible for it. Don't proceed without doing four corner testing and evaluation of the design. Make sure it will work over time and temperature. Do some evaluation and/or simulation. Never rely on only on a reference design and go straight to full volume production.

Regardless of the topology or control technology used, definitely invest in training, design tools, test equipment and software to validate the design so it will exceed expectations in the intended application. There are very good resources available in many cases at no cost or minimal investment. Suppliers can provide reference designs, evaluation boards and design software – often at no charge. Also, Mouser Electronics' website uk.mouser.com is updated daily and houses an industry-first interactive catalog, data sheets, supplier-specific reference designs, application notes, technical design information, and engineering tools.

Mouser stocks the newest products for any power level from over 450 suppliers.

Mark Burr-Lonnon, Mouser vice president of EMEA, addresses the issue of making your own power supply solution.

DESIGN CONSIDERATIONS IF YOU "MAKE"

There are some questions you should ask before you make your own power supply or system. First, it's important to consider what type of power converter system you need. This dictates the level of complexity of the overall design effort, risks, and regulatory requirements. Do you have the proper test equipment? Frequency response analyzers, electronic loads, electrical safety testers and other specialized equipment are needed. Do you have these items on hand? Do you have people with the proper skills? Consider the magnetics, PCB layout, grounding, and shielding techniques needed. The autorouter will need to be turned off and manual layout skills will be needed. Safety spacing techniques in layout must meet leakage guidelines.

Is the design off-line or DC-DC; isolated or non-isolated? Is something available off-the-shelf with proven performance? Parts with integrated supplies may be available. "At lower power levels, semiconductor components have become highly integrated with many containing the inductor inside the package forming what is commonly called PSIP, or power supply in a package," Burr-Lonnon explains.

Do you have the expertise and equipment to perform electrical safety testing on the designs to worldwide safety regulations? Do you know how to design magnetics for required clearances? Consider hours of operation; is this going to be a 24x7 high reliability application? It may make sense to buy if it is high power, off-line, isolated, and demonstrated reliability is needed out-of-the-box.

It takes time to obtain safety agency approvals, often at great expense. If your product will ship internationally it will require large input ranges of 85-265VAC/50-60 HZ. It will require agency approvals for worldwide acceptance; are you prepared for the expense and delays? Do you have safety experts who know the regulatory requirements and how to test for them? Switching supplies can generate lots of noise and worse if they are not properly designed. Regulatory agencies have no sense of humor or sympathy for poor-switching power supply design.

MORE RESOURCES THAN EVER BEFORE

If, after considering the issues you still decide to make your own, it is strongly recommended that you involve suppliers early and often in the definition, selection, and design process. "Mouser carries products from over 450 suppliers with resources available for any power level. We know that the earlier you seek support and assistance, the more time you will have to do things in an orderly fashion and the greater flexibility you will have with more options – this funnel gets tighter as you get to the prototype and production phase," Burr-Lonnon adds.

Finally, with regulations, energy efficiency, and so forth becoming a system-level consideration, considering power electronics up-front is critical. Don't choose the wrong part, topology, or circuit only to have units in stock with failures mounting. You are not alone; there are plenty of resources available to help you implement a successful in-house design under the appropriate situations. Whether you buy or make, Mouser is there to help.

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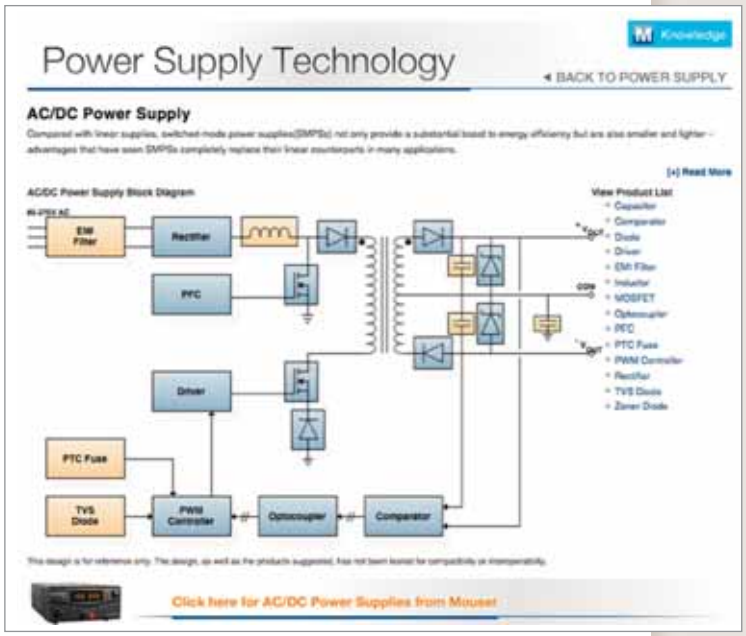

Block diagrams help engineers zero in on the right power supply solutions for their needs.

Variable Definitions Of Processor Units Are Confusing End Users Of Cloud Services

ANTONIO MIGUEL FERREIRA, CEO OF LUNACLOUD SAYS THAT LACK OF STANDARDISATION FOR CLOUD PROVIDERS CREATES CONFUSION FOR SYSTEM DEVELOPERS AND END USERS ALIKE

The need for common standards and transparency in the cloud has been a continuous hot topic ever since this new model of computing became mainstream.

Most of these calls for transparency and standards have so far applied to the data – how secure it is, where it is stored, how to make sure it stays private and what happens in the event the supplier fails to meet its promises. However, the debate on transparency needs to go further.

Currently, there is no common standard for cloud providers to express what CPU (Central Processing Unit) performance they deliver to their customers.

Everyone is aware of what a GB (Gibabyte) is, which is the standard measure for RAM and disk capacity; although other parameters would also need to be taken into account, such as IOPS (Input/Output Operations per Second) for the disk and access speed for the RAM. But the main unit is pretty clear and comparable across providers.

However, the CPU lacks this standardisation. For example, one provider may offer 1 x a certain CPU unit, whereas another might offer 4 x another CPU unit. A customer might think the latter delivers 4 x the processing performance, but that might not be true – they might offer the same kind of performance, if the second provider's CPU unit is 4 x smaller than the first one.

As an example, Amazon AWS uses Elastic Compute Units (ECU), which have equivalent CPU capacity of a 1.0 to 1.2GHz 2007 Opteron or 2007 Xeon processor. Rackspace does not mention CPU allocations in its server configurations at all. At Lunacloud, we use vCPU, which delivers CPU capacity equivalent to a 1.5GHz 2010 Xeon processor.

This lack of commonality in describing CPU values to customers is typical of the cloud industry as a whole, and confuses end users. Worse than that, many providers do not even disclose what kind of processing power they sell to their customers.

The importance of this issue is underlined by research conducted by the Cloud Industry Forum, which asked IT decision makers of their most significant concerns about the adoption of the cloud in their business. Some 19% stated confidence in the clarity of charges, 23% stated confidence in knowing who to choose to supply the service and 35% stated confidence in vendor reliability.

This problem has grown because of the exponential increase in the demand for cloud services. Unfortunately, the industry has not been able to catch up by developing common standards where customers need them most. Fortunately, there are some providers paving the way for others in terms of breaking it down for the customer as clearly as possible.

Until these standards become commonplace, cloud infrastructure providers need to make sure they are transparent in communicating what they deliver for CPU capacity, as well as for all other features they provide. Also, customers should benchmark providers against each other, ideally through independent third parties, besides making simple price comparisons.

Benchmarking and testing are the ways to truly understand and compare various providers. Some manufacturers do benchmarking against their competitors to confirm they are delivering better value for the same price, or same value for a lower price, but this kind of analysis is currently not done by most end customers and, ideally, it should be done by independent third parties.

There are a number of worthwhile tests the customers themselves can run to establish the CPU measurement, such as the Timed Linux Kernel Compilation (LKC) and the Parallel BZIP2 Compression (PBC) tests. The LKC tests how long it takes to build the Linux 3.1 kernel. PBC tests the time needed to compress a 256MB file with parallel BZIP2 compression using POSIX threads. These tests calculate the amount of time a processor can take to perform certain operations; the less time it takes, the better.

Lack of Standards is Hampering Adoption

This lack of standardisation creates confusion, in that customers do not know what they are getting. With such a variety of cloud infrastructure providers in the marketplace, it is essential that each provider is as explicit as possible, to enable the customer to make informed decisions on which provider is best for them.

However, there are ramifications for the providers as well – the lack of standardisation means that comparing oneself to competitors can be difficult, making it hard to understand where your service sits in the marketplace.

Timed Linux Kernel Compilation: **http://openbenchmarking.org/test/pts/build-linux-kernel**
Parallel BZIP2 Compression: **http://compression.ca/pbzip2/**

> *Currently, there is no common standard for cloud providers to express what CPU performance they deliver to their customers*

I believe it will be at least two to three years before we see an industry standard measurement of CPU performance introduced, possibly by an independent organisation such as SPEC (Standard Performance Evaluation Corporation). Unfortunately, all that customers can do until then is to test the CPU themselves and push for standardisation – something that will benefit everybody.

Although some providers may disagree with this and believe the current situation enables them to sell what they want without being transparent, we should all be pushing for industry standards. Users need to trust their cloud providers. ●

Standards are needed for wide cloud adoption

Can't beat the clock

MYK DORMER IS SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
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Interference from locally generated sources of unwanted RF energy is the absolute bane of low power wireless implementations, limiting operating range and causing a whole host of awkward customer issues.

Usually the interferer originates from the customer's own digital equipment (the dreaded "fog" – see the October issue of EW). This is easy to diagnose (if not necessarily to fix), but it is not the whole subject: sometimes the interferer is generated by the radio module itself.

This may seem surprising: one might expect a competently designed radio module to be pretty much without any potentially problem-causing emissions, but this is not necessarily so: in a typical radio design there will usually be several oscillators integral to the architecture. If we take a dual conversion superheterodyne as an example, there will be first and second local oscillators at least. In a multichannel example we will then add the PLL reference oscillator and, probably, the clock belonging to a local microcontroller. There may be others.

These oscillators have the potential to emit RF energy, no matter how carefully designed and/or screened they might be. Interferers will be present on the fundamental frequency, and there will (probably) be significant amounts of signal present at the low lower-order harmonics (up to F x 5 at least, sometimes further).

Even on a legally tested and type-approved module, some of these interferers can be quite large. EN300-220 (and many other) approval specifications set a limit of -57dBm for spurious outputs from receiver apparatus. Assuming (worst case) a narrowband radio with a usable sensitivity of -117dBm, an interferer on channel at this level would result in a de-sensitisation of 60dB!

Obviously no wireless design will be encountered that generates a complete picket fence of -57dBm spurs on every harmonic and product of all its internal frequency sources, as such an imaginary device, while theoretically legal, would barely work at all. It is, however, worth examining some of the problems that are sometimes encountered:

First local oscillator. Leakage of this signal is not a problem in terms of receiver performance per se, in fact, duplex links have been implemented in the past where a unit's receiver local oscillator and its transmitted carrier are one and the same signal, but in situations where multiple receivers are co-located then the LO leakage of one unit can be seen as an interferer by another.

Digital clocks. The internal microcontrollers used in most radio modules are, fortunately, low speed, low power devices, so are very unlikely to put a fundamental or low order harmonic spur in band. Unfortunately, emissions by this clock – and other low frequency sources in the design – can cause problems if they are insufficiently isolated from the LO or front end circuits, as a (relatively) high level, low frequency interferer can mix with the local oscillator to produce a comb of low level products, at Flo ±(n x Fclk). Each of which introduces a potentially serious spurious response at the radio input.

PLL reference oscillator. This is usually a high stability crystal or TCXO, somewhere between ten and thirty MHz. Unless great care is taken, its electrical and physical proximity to the radio's VCO circuits makes the generation of a comb of spurious responses (as detailed in the preceding paragraph) all too likely. Fortunately, the radio's front-end filtering will suppress at least some of these. VHF designs may also suffer from direct interference, as harmonics may fall in-band.

Second local oscillator. Only an issue for multiple conversion designs (most narrowband VHF and UHF types, alas) this oscillator is typically somewhere around 20.945MHz (for 21.4MHz intermediate frequencies) or 44.545MHz (for 45MHz IF radios). The higher order harmonics of this oscillator frequently result in "lost channels" in the VHF bands, although the UHF band harmonics rarely have enough energy to cause issues (see Table on the next page).

Identifying the problem is one thing: a cure is quite another. If you are designing a radio from scratch, then careful screening, decoupling and extensive testing is the way to minimise self-generated interferers and spuri. Minimise the power generated in digital clocks and keep associated tracks

> *Even on a legally tested and type-approved module, some of these interferers can be quite large*

short. Single chip, low-power CMOS microprocessors are a great benefit here: external high speed address and data busses can present insurmountable interference issues. Where possible, shut down processor clocks when their circuits are not in use. Where oscillator frequencies can be chosen, attempt to avoid harmonics falling in-band; a design covering 433-435MHz would be better fitted with a 13MHz reference oscillator (with relevant harmonics at 429 and 442MHz) than with a 14MHz part, which would put a harmonic on 434.0MHz.

As a low power wireless module user, you are in the hands of your supplier. They should have designed to minimise internal clock interference, but you cannot guarantee that the module you have committed to use is entirely free of it. At this point, a coping strategy is needed: "Accept that there will be some "lost" channels".

As the strictures of a real world design make the complete absence of interferers unlikely, it becomes necessary to choose a band-plan that works around them. Basic ISM band radios are actually quite unlikely to have lost channels; the bands are quite small and do not have second LO harmonics falling inside them, but it is still good practice to avoid using frequencies which are integer multiples of 1MHz (434.0MHz for example), which are very often compromised by clock oscillator noise.

21.4MHz and 455KHz IFs	125.670MHz, 146.615MHz, 167.560MHz, 188.505MHz
45MHz and 455KHz IFs	133.635MHz, 178.818MHz, 222.725MHz
10.0MHz reference	130MHz, 140MHz, 150MHz, 160MHz, 170MHz, 180MHz
12.8MHz reference	128MHz, 140.8MHz, 153.6MHz, 166.4MHz, 179.2MHz
13.0MHz reference	130MHz, 143MHz, 156MHz, 169MHz, 182MHz
19.2MHz reference	134.4MHz, 153.6MHz, 172.8MHz

Table 1: VHF Band Lost Channels

Radios with wider tuning ranges, especially examples operating on the wider licensed VHF and HF bands, are almost bound to have at least a few blocked channels. Work with your supplier and customer to identify them (this may require disclosure of intermediate and clock frequencies by the module supplier) and then write them out of your band plan.

Where an operational requirement forces the use of a blocked channel there is still an avenue to explore: it may be possible to change the operating frequency of the offending source to move the blocked channel to a different (and irrelevant) frequency. Digital clocks can be moved in frequency (if timing-critical firmware routines can be re-written). There is usually a range of TCXO frequencies available (10MHz, 12.8MHz, 13MHz, 19.2MHz and 26MHz are all very common, and there are others), if the PLL reference divider programming can be tweaked. If the second local oscillator is the issue then it may even be possible to move it (and the first IF frequency) a few hundred KHz up or down band (in addition to 21.4MHz, many quartz suppliers offer 21.7MHz versions of the same parts. Similar substitutions are possible at 45MHz).

This sort of modification will involve the radio supplier, but if they have parts in stock and programming effort available, then it's quite possible to convince them to do a "special" if it clinches a worthwhile order.

Good RF design will minimise internally-generated interference, but no radio can ever be absolutely immune. If a blocked channel can be identified early enough, it will be possible to design around it.

So plan carefully, talk to the supplier and, as ever, test everything!

BUS SYSTEMS WITHIN A 48V BOARD NET AND THE CHALLENGES THEY MIGHT PRESENT

MATTHIAS MUTH FROM NXP SEMICONDUCTORS DISCUSSES THE BUS SYSTEM CONFIGURATIONS FOR IN-VEHICLE NETWORKS AND THE POTENTIAL PROBLEMS COMMUNICATING ECUS COULD CAUSE WHEN THEY ARE PART OF BOTH THE 48V AND 12V POWER DOMAINS

Last year, several German car manufacturers announced their intention to upgrade their future car platforms to 48-volt supplies in addition to the familiar 12-volt board networks. The driving force behind this new power domain is the need for more powerful electrical actuators for applications such as active vehicle stabilisation and electrical power steering. Even though the 12-volt and the 48-volt supply domains share one electrically connected ground, there are quite a few basic questions concerning the consequences for on-board network topologies based on CAN and FlexRay when applications cross these supply domains.

In this article, the potential effects and bus system constellations for in-vehicle networks are discussed in detail in the case when the communicating ECUs are part of both power domains. Special attention is paid to signal integrity and robustness in the case of possible failures, such as 'loss of ground' for example. Since the initial vehicle platforms will introduce the 48-volt board networks in conjunction with FlexRay and CAN interfaces, these bus systems are used as examples, explaining the challenges encountered in mixed supply domain vehicles with direct-coupled ground.

Overview Of 48-Volt Requirements

For the development of 48-volt on-board networks (Figure 1) special attention was paid not to exceed the maximum permitted DC voltage of 60 volts during normal operation. Based on this specification, in principle it is possible to operate the new 48-volt systems without galvanic isolation, as this critical contact voltage of above 60 volts is avoided. In contrast to this, systems with even higher operating voltages, such as those in hybrid-electric vehicles with voltages of several hundred volts, must always be built with a complete galvanic insulation, which results in much higher system costs.

In a mixed 48-volt/12-volt in-vehicle network, it is possible that the ground for both systems is combined and galvanically coupled so there's no need for special measures to isolate the contacts. However, in a system with CAN or FlexRay buses, there are issues relating to the communications between the two voltage domains.

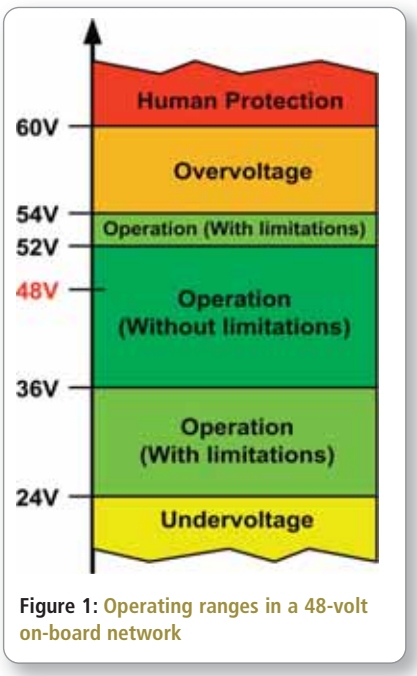


Figure 1: Operating ranges in a 48-volt on-board network

Even if the bus system, such as CAN or FlexRay, uses a differential interface, the bus transceivers always require a common

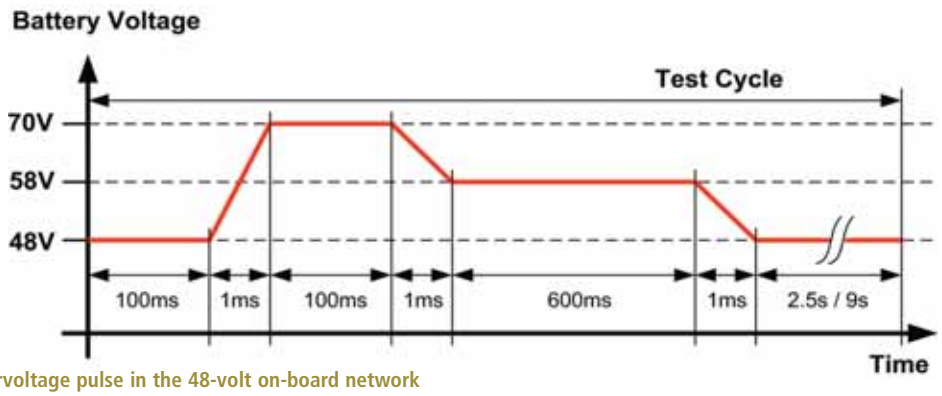


Figure 2: Overvoltage pulse in the 48-volt on-board network

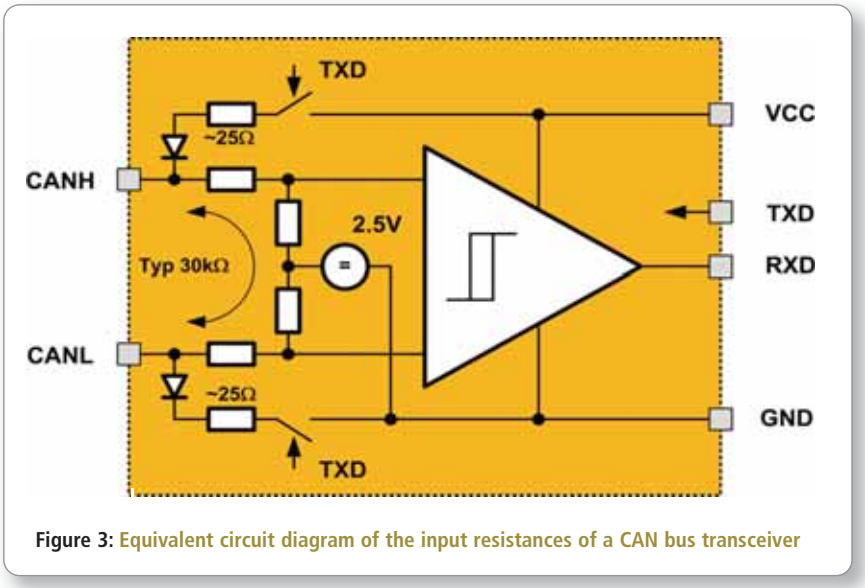


Figure 3: Equivalent circuit diagram of the input resistances of a CAN bus transceiver

ground. In a mixed on-board voltage network this common ground is not always available during normal operation or in the event of a fault. So then the questions is: which one of the two ground references should remain as the main one for the bus system – the 12-volt ground (terminal 31) or the 48-volt ground (terminal 41)? While both terminals are galvanically coupled at a central location in the vehicle, it cannot be ruled out that there may be a major deviation or even an elevated noise level in the ground potential.

In addition, there are already leanings toward temporary overvoltages in the 48-volt in-vehicle network, especially when it comes to re-using energy from the braking system. Another scenario, for example, could be during towing a car, when an electrical actuator within an active dynamic chassis control system may operate as a generator, producing a major overvoltage at each pothole, which then feeds back into the 48-volt network. In such a case voltages of approximately 70 volts are to be expected with a pulse length of up to 100ms (Figure 2).

In general, in mixed on-board networks with two batteries, contact between the 12-volt and the 48-volt supplies must be prevented. It may be necessary to equip control units that need both voltages with separated connectors that reliably prevent a wrong a connection between the different supply voltages. The 48-volt supply does not require reverse polarity protection hardware

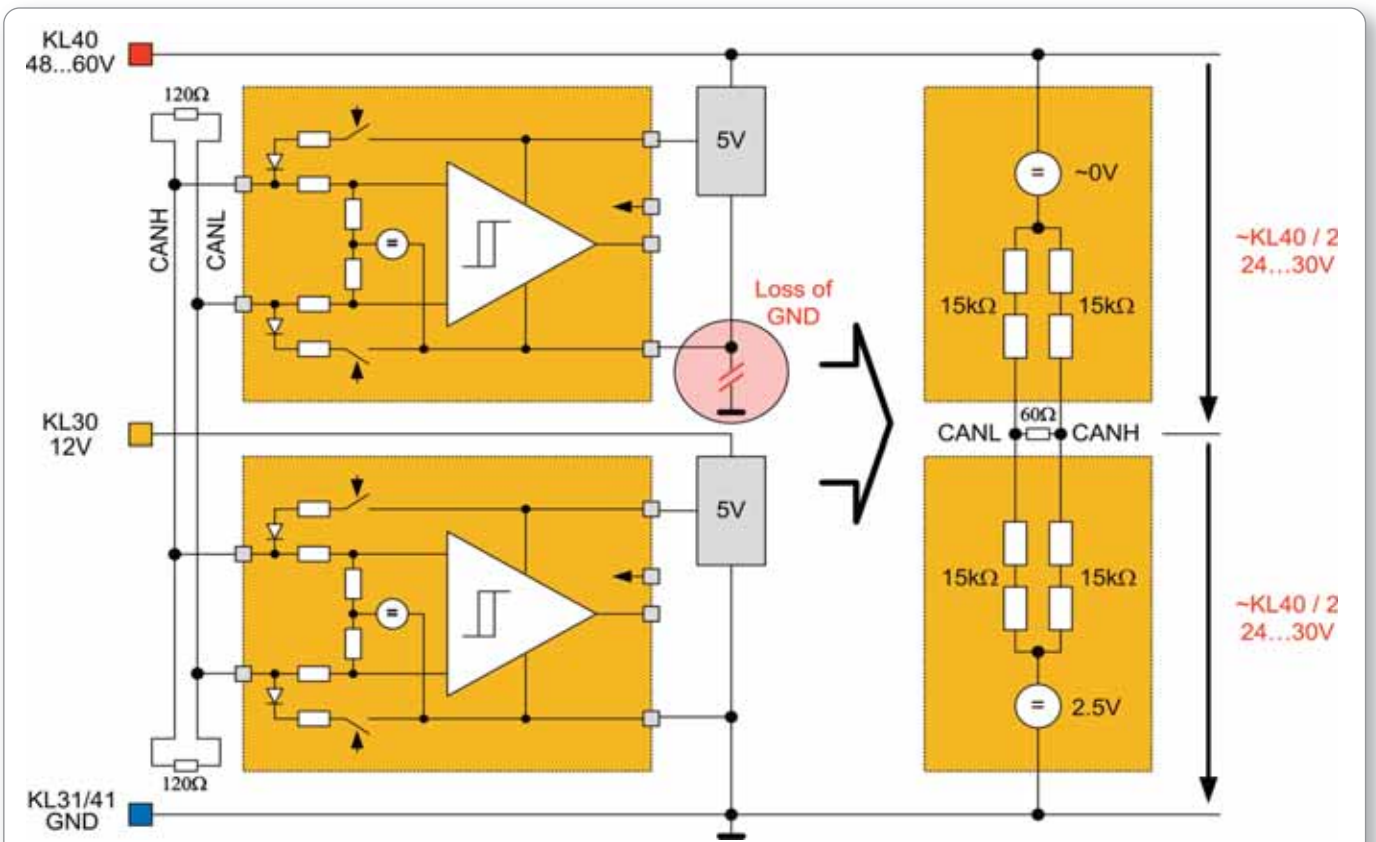


Figure 4: Structure of the voltage divider when ground is lost, equivalent circuit diagram of the CAN bus transceiver

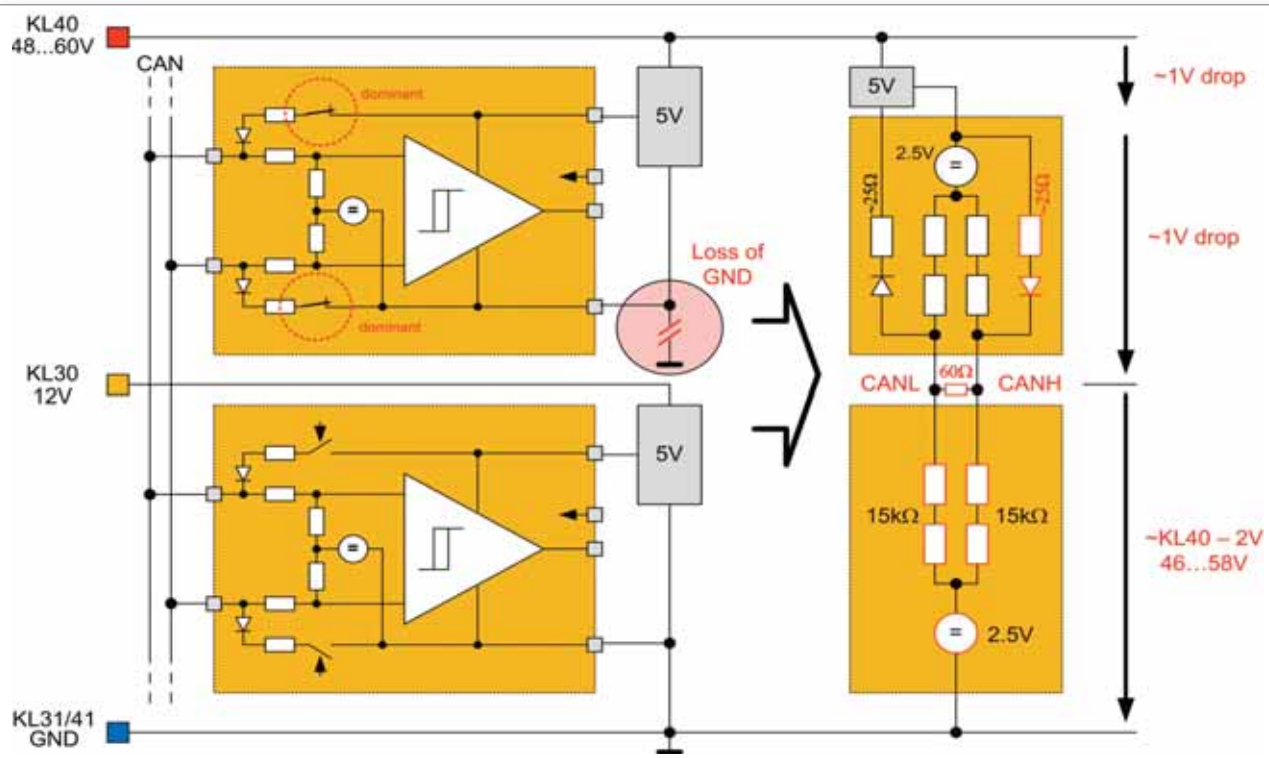


Figure 5: Structure of the voltage divider during 'hot plugging', equivalent circuit of the CAN bus transceiver

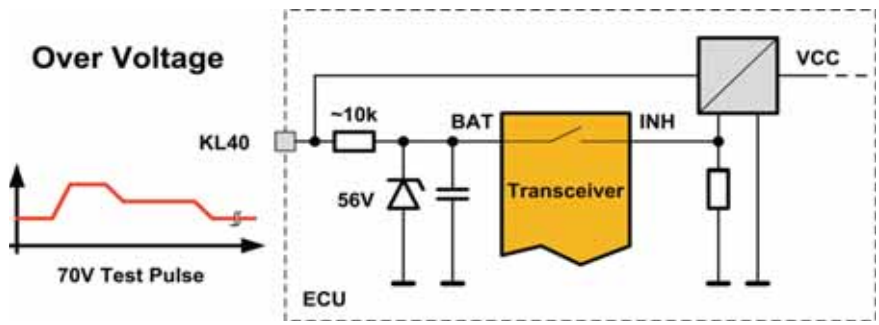


Figure 6: Clamping circuit for the protection of the 70-volt pulse, no increased standby current

because wrong connection of the 48-volt battery is prevented by restrictive measures, such as so-called "jump starting", which is used in the 12-volt systems but is not allowed here. This must be prevented here, because the uncontrolled series connection of the batteries would exceed the 60V.

One might assume that these new applications require the control units to be equipped with galvanic isolation in order to reliably prevent undesired cross-currents between voltage domains. However, it is possible to develop mixed 48-volt/12-volt systems without any isolation. The risk of component damage or faulty communication can be avoided without the need for isolation by using appropriate bus components.

In any case it has to be ensured that there's no "hard" short-circuit between 48 volts and one of the bus lines. In such an event, the worst case 70-volt pulse voltages (and in some circumstances even higher) would be connected to the bus lines without a current limitation, which would destroy all of the connected transceivers. Galvanic isolation within the electronic control unit (ECU) doesn't help since it will not protect the bus lines, only the ECU-internal low voltage interfaces. Consequently, a bus short-circuit, combined with an overvoltage in the 48-volt on-board network would lead to the destruction of all connected ECUs.

As both on-board voltages are connected via ground, fundamentally there won't be any new effects added to what is already seen in today's 12-volt on-board networks. Only the maximum battery voltage is now considerably higher and will have a harder impact on the communication interfaces.

Case A: Loss Of Ground At A Control Unit

As it is already known from the 12-volt world, the entire electronics within the control unit will drift more or less swiftly in the direction of the battery voltage, with a speed dependening on the buffer capacitors available. For the bus transceiver in the control unit without ground, the bus lines appear to have a 'negative' potential difference up to the full battery voltage, as all other control units maintain these bus lines within their normal voltage range. However, if the ungrounded control unit is supplied with 48 volts, the voltage potential compared to the bus potential will be correspondingly bigger than in the case of 12 volts.

On account of the typical implementation of a bus transceiver, the connection to the bus lines is always associated with an internal series resistance (receiver input resistor network, typically > 15kohm per bus line resulting in 30kohm differential), which prevents a major compensating current (Figure 3). Basically, the ungrounded transceiver forms a voltage divider that can be calculated from the remaining network of

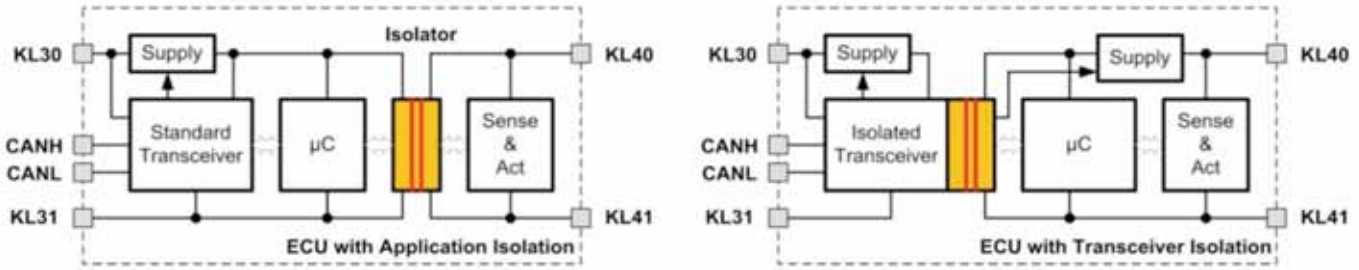


Figure 7: Variants for the galvanic isolation on the control unit level

all bus transceivers with ground connection and the internal resistance of the transceiver without ground connection (Figure 4).

If loss of ground has to be assumed for a control unit, the largest bus potential arises in the following cases:

- **Two-node network:** The bus potential will settle to approximately Vbat/2 as two bus transceivers of the same type with almost identical internal resistances will form a voltage divider. In the case of 60 volts, this would mean a bus potential of approximately +30 volts for the grounded bus transceiver and -30 volts for the ungrounded bus transceiver. Here, the fact that the grounded bus is not at 0 volts but at around 2.5 volts (CAN and FlexRay) is neglected.
- **Large network:** Here, many bus transceivers are active in parallel and correspondingly maintain the bus at a low potential, so the ungrounded bus transceiver has less influence on the bus voltage. The consequence is that the remaining grounded in-vehicle network is exposed to a much lower overvoltage than in the two-node case, while at the ungrounded bus transceiver a major negative potential is present – in extreme cases even the full negative battery potential.

In case of 'loss of ground', the first requirement for a bus transceiver can be formulated, which can be applied in a 48-volt on-board network without restrictions. Control units that are operated with 48 volts should be fitted with transceivers of an adequate electrical robustness at the bus pins against negative voltage potentials. In the case of a 60-volt battery potential, 58 volts would be sufficient for this because the potential divider for the remaining vehicle continues to be present and the bus voltage in the remaining network is not zero volts but is closer to 2.5 volts. Control units operated with 12 volts could, in this situation, cope with a much lower electrical robustness, as in the worst-case scenario where with two control units half the battery potential occurs (see Figure 4). Thus, in case of a 'loss of ground' fault, bus transceivers with a positive electrical robustness of at least +30 volts should be deployed. This particularly affects carry-over components originally coming from existing 12-volt vehicles.

Case B: Connecting And Disconnecting Components While Powered (Hot Plugging)

It is interesting to consider scenarios in which control units are connected or disconnected during running bus communication. Here, a number of different voltage potential configurations exist with temporary ground connection and active bus communication with low resistance bus drivers in the process of transmitting dominant bits. Both sides of the communication have to be considered; the on-board vehicle network side with many active nodes and ground connection as well as the control unit being connected or removed. A critical new aspect is that the calculation of the voltage divider used in the previous case is no longer correct. If an active transmission (driven by a 12-volt ECU) is present on the bus system while the 48-volt device is losing its ground connection, the lower part of the potential divider offers a considerably lower resistance than the internal resistance of the control unit without ground connection. For this reason the full battery voltage is present at the node without ground connection much sooner and this happens even in small networks.

Another critical situation comes up when the 48-volt control unit is in the middle of a transmission when it is separated from the ground potential. In this case it has to be assumed that this control unit continues transmitting for a while, even without the ground connection, as the local supply buffers continue supplying the control unit, keeping it active (Figure 5). As the supply capacitances are increasingly depleted, the potential at the control unit moves towards the 48-volt battery potential. However, it continues sending with the active driver stages until the local voltage, just before the battery voltage is reached, becomes too small to keep the control unit active. Therefore, the remaining vehicle network is actively pulled in the direction of the 48-volt voltage supply. This means that the high-resistance voltage divider ratio is no longer valid and the bus voltage becomes much larger, until it has almost reached the full 48-volt battery voltage minus the voltage drop caused by the bus driver and some internal impedances of the local voltage regulator.

From the hot plugging case, further requirements for transceivers can be derived – specifically for the transceivers in the remaining in-vehicle network (i.e. for all 12-volt control units, too). In order to safely withstand the case 'connecting or disconnecting while powered', all the bus transceivers in the network with a 48-volt control unit must have a positive electrical robustness of +58 volts, so that an actively sending 48-volt control unit does not destroy any bus transceivers in the event of loss of ground and high battery voltage.

The effects depicted in Figures 4 and 5 and the consequences for the CAN system can be equally projected to the FlexRay bus system. FlexRay bus transceivers require a corresponding electrical robustness at the bus connections, as control units without direct 48-volt supply can also be affected by an overvoltage as described before.

When using an active star connection (assuming a 12-volt on-board network), the different parts of the network are separated from each other, and for this reason the high electrical robustness is only required for the control units in the corresponding branch of the network. The active star, however, must be equally robust.

Case C: Battery Connections Of Battery-Supplied Bus Transceivers

This is another issue that may arise for control units that support the so-called

'sleep mode' and controlling the entire electric power supply via the bus transceiver. These bus transceivers usually have a direct battery connection, as well as an INH output for control of the power supply ('inhibit' or alternatively 'enable function'). As mentioned at the beginning of this article, in a 48-volt on-board network, voltages can briefly exceed 60 volts (see 70 volt test pulse in Figure 2).

Preventing destruction of the bus transceivers by such voltage peaks at the BAT input requires a clamping circuit. Its purpose is to prevent voltage peaks affecting the bus transceiver. As the power consumption of bus transceivers is quite low (in the area of a few mA), simple clamping circuits consisting of a series resistance and a Zener diode are suitable for this (Figure 6). However, care has to be taken that the Zener clamping voltage is chosen considerably above the nominal operating range of a 48-volt control unit, because otherwise one has to expect increased standby currents in the system.

This results in a further requirement for the bus transceivers in a 48-volt on-board network. The electrical robustness of the transceivers BAT and INH pins should be considerably above the nominal 48 volts, ideally at least 58 volts, to prevent elevated standby currents. If the electrical robustness of these pins is lower, an additional standby current has to be accepted.

Case D: Control Units With Several Ground Connections (KL31 And KL41)

A special case is presented by control units that combine both voltage domains on a single board. Typically only one of the two ground connections detaches while the other continues to be connected. As both ground potentials are already connected in the vehicle, both should not be connected galvanically at a second location, in order to prevent ground loops. If the ground connection is lost on one side, uncontrolled cross-currents can occur in the control unit, which then causes the load current to pass across all of the components along unplanned paths, leading to damage. For such applications, galvanic isolation is the ideal means to prevent such eventualities. Isolation can be provided both on the transceiver side and on the actuator side. Depending on the system configuration, one or the other variant can be the more advantageous. This has to be checked in each individual case (Figure 7).

As a rule, it is desirable to supply control units only from one voltage domain in order to avoid the need for galvanic isolation and the associated costs.

Signal Integrity On The Bus In The Event Of A Fault

So far we have concentrated on the issues of potential damage to bus transceivers and have shown how this can be prevented by appropriate selection of components. Another important aspect is the signal integrity of the bus systems when, for example, a control unit experiences a loss of supply voltage. Does this have consequences for the remaining communications within the vehicle?

Signal integrity in the FlexRay bus

As explained above, to cope with loss of ground it is worth building a voltage divider consisting of the remaining network and the control unit without a ground connection. The result is an average bus voltage between ground and the 48-volt supply when the bus has reached its 'idle' state. As soon as a node in the remaining network starts sending, in the case of FlexRay the transmitter initially actively drives both bus lines to transmit the TSS (transmission start sequence). In this phase, the bus is pulled down to the nominal level, which takes a short time (Figure 8).

This can be compared with discharging a capacitance. During the TSS phase the FlexRay cable will be 'discharged' reliably, the TSS reaches the nominal value and is correctly identified by all nodes. As in the TSS, an adequate time reserve is provided; this small additional delay at the beginning of the frame is harmless. In laboratory measurements the time delays in the TSS recognition were approximately 10ns, which is uncritical on account of the nominal length of the TSS is normally 1µs (for 10Mbit/s).

All other bits are now sent by the push-pull bus drivers, so that the high resistance path of the bus transceiver without ground connection no longer is completely overwritten by the active bus transceiver, while the bus transceiver with the loss of ground appears only as a high pull-up resistance. If this bus transceiver without ground connection has any ESD clamp at less than the 58 volts mentioned above, "side effects" are to be expected.

When deploying appropriate bus

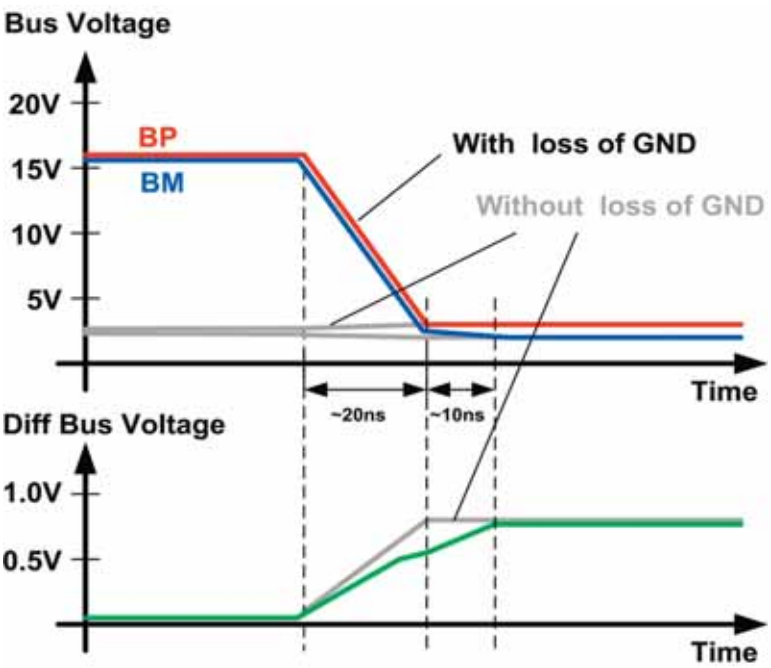


Figure 8: TSS at the start of the communication, 3-node network, one node without ground (simplified illustration based on laboratory measurements)

transceivers, the bus communication does not experience any side effects from a GND loss event. Also the 'asymmetric delay', which is critical for the FlexRay, remains in a range without negative effects. It can therefore be stated in relation to the FlexRay bus system that, even in the event of a loss of ground within a 48-volt control unit, no negative effects can be expected for the remaining communications within the vehicle. Nevertheless, a hard bus short-circuit of the battery to the bus lines should be prevented by structural means, as mentioned earlier.

Signal integrity in the CAN bus

In the CAN bus system, the situation is somewhat different when the influence of a control unit without ground connection is considered. The effects described below are fundamentally identical to those of a 12-volt vehicle and not new, but have different characteristics in the 48-volt system, i.e. stronger impact.

In the CAN system, the already described voltage divider also settles in any recessive bus state. Here however, two effects become relevant that do not exist in the FlexRay system: In the CAN system the first active bus edge (start of frame) is a synchronizing edge. This is described as 'hard synchronisation' in the CAN standard. If the first edge is delayed, this results in a major synchronisation deviation between the nodes. In the least favourable case, this can be so severe that the communication no longer works (Figure 9).

The second important difference from FlexRay is the fact that a CAN bus transceiver has no push-pull driver stage. Instead, the so-called recessive bits in the protocol are not actively driven. This results in every recessive bit being once again exposed to the voltage divider with the non-supplied node, which in turn influences the the timing of the subsequent dominant bus edge. As already mentioned, this same case also exists in the 12-volt on-board network; however, there the potential shift in the recessive case is reduced. In practice, it is unlikely that a CAN network stops communicating if an ungrounded 48-volt control unit is connected to it.

The background for this is the following assumption: CAN networks that have a critical 'bit timing' are usually very large networks with many involved nodes. In this case, the contribution of the unsupplied participant to the voltage divider is negligible, but only as long as the unsupplied bus transceiver has been selected in accordance with the criteria described above.

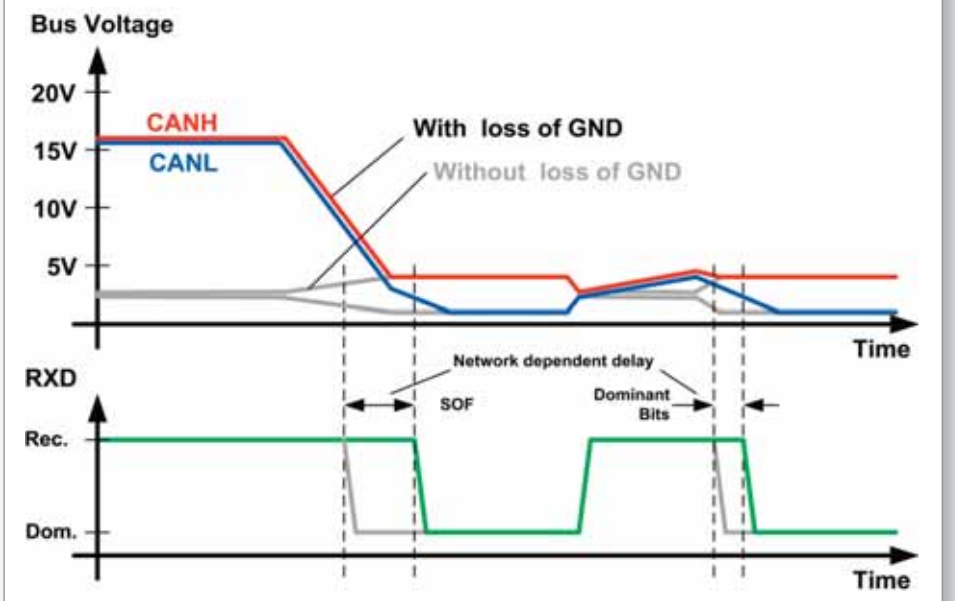


Figure 9: CAN network with 3 nodes, delay of the dominant edges

Figure 10: NXP TJA1081 FlexRay transceiver

Small CAN networks are not likely to be operating close to the limit of the CAN 'bit timing' and thus should not have timing problems because, in addition their capacitive load becomes smaller and, therefore the additional delay for the first dominant bit is rather short. In each case, it is advisable that individual networks be investigated in detail with this in mind and to evaluate whether a loss of ground could have relevant consequences for the bit timing or not. In this respect, familiar simulation methods based on simple bus transceiver models are suitable.

Recommendations For The Bus Interfaces In The 48V Environment

It is always advisable to feed the power supply of a control unit from a single source, simply in order to avoid possible cross currents and avoid the need for expensive galvanic isolation.

In systems with control units connected to the 48-volt supply and no isolation measures, the following criteria are to be applied for the selection of transceivers:

- Electrical robustness of the bus pins of at least ±58 volts for all transceivers in the entire network or branch.
- Electrical robustness of the BAT and the INH pins of ideally +58 volts (if the values are smaller, standby current in the control unit increases).

NXP Semiconductors already provides suitable products for CAN and FlexRay with the required electrical robustness. For example, for the CAN bus, the transceivers TJA1051/TJA1042/TJA1043/TJA1048 and TJA1049 are available, and for FlexRay, all products (e.g. transceivers TJA1081B – see Figure 10 – and TJA1083, as well the 'active star' TJA1085) fulfil the requirements for electric robustness in a 48-volt environment. In particular for FlexRay it should be pointed out that the 'active star' TJA1085 also offers this electrical performance. Furthermore, there are already samples of the galvanically-isolated CAN transceiver TJA1052i available, which is particularly suitable for handling the potential CAN 'bit timing' phenomenon during a loss-of-ground situation, if required.

Based on the components mentioned here, there are no obstacles to the mass introduction of 48-volt board nets using CAN and FlexRay for communication between the two voltage domains. ●

STANDARDIZATION IN THE AUTOMOTIVE INDUSTRY

THILO SCHUMANN FROM CAN IN AUTOMATION (CIA) EXPLAINS THE DIFFERENCES BETWEEN AUTOSAR AND CIA 447 FOR AUTOMOTIVE APPLICATIONS

More than 25 years ago, Robert Bosch laid out the Controller Area Network (CAN) concept for the needs and requirements of the automotive industry. CAN is now extensively used in the automotive industry and every major international carmaker has adopted it for most of their product lines – almost every new car uses CAN. However, there is no standardized higher layer protocol in use so far. There are several attempts in standardization like OSEK (Offene Systeme und deren Schnittstellen für die Elektronik in Kraftfahrzeugen; or in English: Open Systems and their Interfaces for the Electronics in Motor Vehicles), but they are not very widely adopted. Now, together with different carmakers, CAN in Automation (CiA) has developed one defined interface based on the international standardized higher layer protocol CANopen. It is intended for use in special-purpose cars such as taxis, police vehicles, emergency response vehicles and cars for disabled people.

Past Efforts

Historically, there have been different standardization efforts in the automotive industry. One of the first was OSEK/VDX (Open Systems and the Corresponding Interfaces for Automotive Electronics/ Vehicle Distributed eXecutive). Then, there's Autosar, the well-known standardization effort in terms of the development process. Then there was the standardization effort regarding the diagnostic interfaces as requested by law in the European Union (EU) and mandated by the US.

Contrary to these standardization efforts, during the last few years the automotive industry started to take a different approach with the help of CiA, even though initially this standardization effort focuses on special purpose-cars.

OSEK/VDX

OSEK was founded as a joint project by key representatives of the German automotive industry. The purpose was to develop an open-ended architecture for distributed control units, and it was mainly aimed at the following areas:

- Communication (data exchange within and between control units);
- Operating system (real-time execution of ECU software and base for other OSEK/VDX modules); and
- Network management (configuration determination and monitoring).

The goal was to support the portability and reusability of the application software by:

- Specification of abstract interfaces to be as application-independent as possible;
- Specification of a user interface independent of the hardware and the network;
- Efficient design of architecture: making the functionalities configurable and scalable to enable optimal adjustment of the architecture to any application;
- Verification of functionality and implementation of prototypes in selected pilot projects.

Several specifications were developed as part of this effort. The specifications that cover these requirements are named accordingly as OSEK COM, OSEK OS and OSEK NM. Other specifications are developed in addition to supporting the architecture design process and portability, and these are OSEK OIL and OSEK RTI. Most of the specifications are now internationally standardized at ISO and are available since 2005 as a set of specifications within the ISO 17356: Road Vehicles – Open Interface For Embedded Automotive Applications.

Even though the idea was to standardize the design process of automotive applications, real use has so far been limited. Of the three, OSEK OS is most widely used, with several proprietary real-time operating systems already existing, providing OSEK OS conforming APIs.

OSEK NM is partly used, whereas OSEK COM is not used at all and is being sidelined with OEM proprietary solutions.

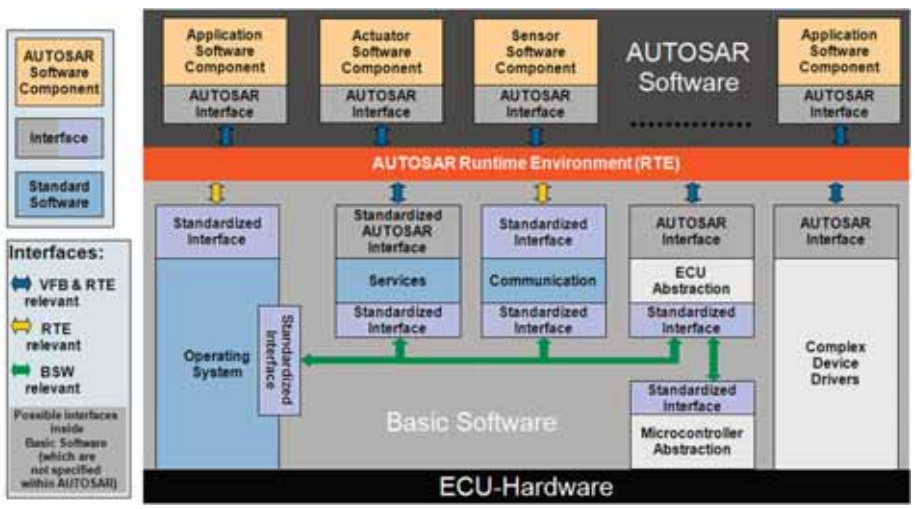
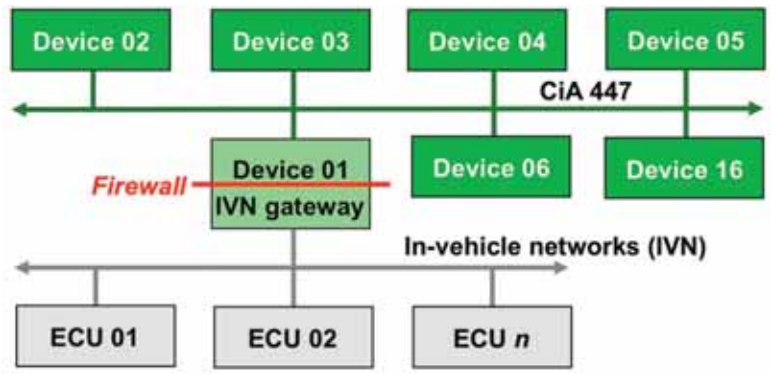


Figure 1: Autosar has the approach of middleware in a framework

Figure 2: CiA 447 is different to Autosar as it is specific purpose, covering devices



But even OSEK COM's specification is very loosely defined, especially in terms of existing byte orders being allowed to exist within one message. The reason behind this is that OSEK COM focuses on the specification of the services, but does not include any protocol definitions. There are no protocol definitions of OSEK COM on CAN, Flexray and LIN. Currently, the protocol definition has to be manufacturer-specific.

Autosar

Following OSEK/VDX, Autosar (Automotive Open System Architecture) entered the scene. Its objectives and goals are different from those of OSEK/VDX, but it was set up by almost the same market players.

Autosar is described as open and standardized automotive software architecture, jointly developed by automobile manufacturers, suppliers and tool developers. As shown in Figure 1, Autosar's approach is that of middleware in a framework, defining a degree of abstraction that allows independent hardware and software development.

Under the interface definition of the Autosar Runtime Environment, the input, output and control functions are considered an Autosar software component that can run on any hardware without having to know anything about it. However, Autosar does define the interfaces for different services within the basic software.

There is a big advantage to this approach as it allows 'ring-fence' isolation of the runtime environment from the hardware itself. This means the supplier of the runtime environment has clearly defined interfaces they can rely on. Also, the basic software itself is designed with modularity in mind. The advantage is well-defined separation between modules.

Autosar as middleware allows developers to use and swap of software components between different vendors'

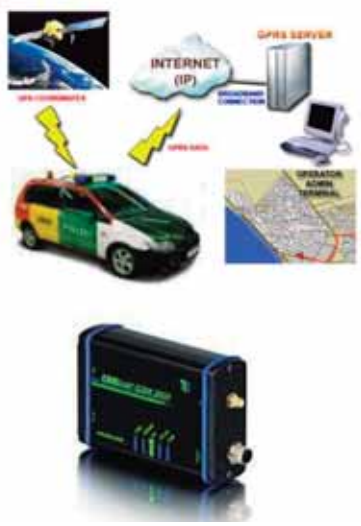
Figure 3: CiA 447 covers data signals

The most basic function in all fleet management systems, is vehicle tracking. It is usually GPS-based.

The CiA 447 provides several GPS-related and navigation system parameters:

- 60B0$_h$: GPS current position
- 60B1$_h$: GPS satellites
- 60B2$_h$: GPS status
- 60B3$_h$: GPS date
- 60B4$_h$: GPS UTC time
- 60B5$_h$: GPS velocity and heading
- 60B6$_h$: GPS altitude

- 60C0$_h$: Distance to selected destination
- 60C1$_h$: Position description request
- 60C2$_h$: Position description
- 60C3$_h$: Start route guidance
- 60C4$_h$: Current position request
- 60C5$_h$: Current position



offerings within this ecosystem, so a car maker does not have to stick to any particular supplier.

The general approach of this concept is not new to information technology; it is known as POSIX. POSIX has the same ideas in the computer world and is realized in many operating systems these days, including but not limited to GNU/Linux, Windows and the different BSD (Berkeley Software Distribution) variants, including Mac OS X. The idea behind the concept is clearly to have reusable software components that reduce software development in future product generations.

But it is worth mentioning that Autosar does not standardize the car itself or any of the functions and signals within it. This is still completely manufacturer specific.

Diagnostics

The standardization of the diagnostics interface of a car has a completely different approach. It was mandated by the EU and the US for two different reasons: first, as cars become more complex, third party service became almost impossible. Second, as cars use more sensors, such as for measuring exhaust gases and for control purposes, and they have to adhere to ever-more demanding environmental requirements, there should be easy access to the data. With these requirements in mind, the diagnostic interface was defined.

There are standardized services and protocols to collect and read diagnostic data from the different devices within the car. The basic diagnostic data is also standardized to enable basic servicing and to read out environmental data collected by the car itself. But, the standardized diagnostic data is still very limited, even though manufacturers have extended the data sets significantly. The extension is made due to the same diagnostic interface being used by the car makers' specific contractors to allow servicing.

Standardizing the diagnostic data is the first time automotive-specific datasets have been defined. It is available as ISO 15765: Road vehicles – Diagnostic Communication over Controller Area Net work (DoCAN).

CiA 447

The standardization of CiA 447 follows in some ways in the same footsteps of ISO 15765. For now, it defines the automotive application of certain cases that apply to special purpose cars. It started in 2006 when the BZP (German nonprofit organization for Taxi and Cars for Hire) organized an event on CAN-networked taxi-specific devices. As a result, the Car Add-on Devices Special Interest Group (SIG) within CiA was born. Its aim is to specify the CAN-networked devices within special purpose cars. It started with the taxi, evolved to police cars and the next step is emergency response vehicles and cars for disabled people.

CiA 447 is the specification defined by the group, currently available in version 2.0. It has already been partly implemented by some car makers with more implementations in the pipeline.

CiA 447 is different from Autosar in that it is specific purpose, covering devices and data signals (see Figures 2 and 3). The expert group identified the relevant devices for the specific purpose and defined their data signals and behavior. The idea behind this approach is to allow an easy plug-and-play connection of those devices.

However, the application behavior has been left undefined and open to be manufacturer-specific, as the behavior of a taxi or police application depends largely on the requirements defined by a country, governmental organization, the state or sometimes even by a district.

Within the CiA 447 definition, even the car can be treated as a device; it has inputs and outputs, but no application behavior as such. For example, it does not matter which device will provide the GPS information from the car, it could be the car itself or the navigation system, or it could be a completely separate GPS device that relates to the car or the fleet. The advantage of this approach is that the input and output devices are very well defined. However, the application behavior can be adjusted to the current requirements very easily, if needed.

Growing Support

Car makers are interested in standards, since they have to build cars with partly configured devices but may have to add the specifics afterwards, after they've been built.

Autosar and CiA 447 are two non-conflicting standardization approaches that may complement each other.

Device functionality, data signals and interfaces are well defined in terms of an application, which allows portability and reusability within a development environment.

Other applications and, specifically OEM independent applications like the eCall initiative, for example, may be able to profit from the knowledge gained from Autosar and CiA 447. ●

REFERENCES

OSEK/VDX: www.osek vdx.org
Autosar: www.autosar.org
CiA: www.can cia.org

RS COMPONENTS OFFERS ENGINEERS SUPPORT FROM CONCEPT TO CREATION

Visit RS at Electronica – Hall A4, Stand 117

In a dynamic industry that is evolving evermore swiftly, finding alternative methods to reduce design cycle times is a priority uppermost in the minds of electronics engineers. In this tough competitive environment, a company's success is increasingly dependent on the ability of its engineers to develop highly differentiated products that deliver enhanced performance and functionality in a fast time-to-market. As a result, engineers are on the lookout for increasing levels of support to help them achieve their design and development goals. This is a unique opportunity for distributors like RS to get involved and offer easily accessible and powerful cost-effective tools and added value service to enable significantly faster product development.

Over the past two years RS has taken considerable steps towards helping engineers meet time-to-market demands through the introduction of various eCommerce initiatives, including advanced parametric search tools to deliver fast product selection and highly efficient purchasing. The company has also developed a unique online design ecosystem that provides support to engineers from a product's conception right through to its production.

At the core of this effort is the DesignSpark.com online support community and the award-winning DesignSpark PCB schematic capture and PCB layout software, which is downloadable and completely free. With no restrictions or limitations, the fully-featured DesignSpark PCB has created a new benchmark for PCB design tools, and has been embraced by engineers worldwide, with almost 160,000 downloads from the RS website since its launch in July 2010.

With the recent introduction of Version 4.0 of the tool, engineers now have access to an industry-leading component library, PCB quote service and BOM quote functionality. On top of this, the newly developed ModelSource, downloadable from the DesignSpark site, provides the industry's largest open-source component library.

DESIGNSPARK PCB VERSION 4.0

DesignSpark PCB Version 4.0 is a substantial extension of the software's capabilities and makes the flow from design to purchase considerably quicker and easier. The simplicity of the DesignSpark PCB user interface with its built-in wizards has now been combined with substantial time saving benefits for engineers. New functionality includes an enhanced library manager, featuring an easy-to-use attribute and part number driven interface to an extended library of over 80,000 components. Additionally there are new tools to obtain quotes for the Bill-of-Materials (BOM) and production quotes from PCB manufacturing and assembly subcontractors.

BOM QUOTE TOOL

The BOM Quote tool is a new feature within the DesignSpark PCB software and links with the RS website to provide an instant quotation for the components in the design. The tool takes advantage of RS part numbers embedded within the new component library and automatically generates a BOM that has been 'scrubbed' to match the components gathered from the design – with options to either save a copy of the BOM, request a quote, or to automatically populate the shopping basket on the RS website.

PCB MANUFACTURING QUOTE TOOL

Also available within the DesignSpark PCB software is the new PCB Quote tool, which is based on attributes taken directly from the PCB design software, such as board size, copper layer count, manufacturing limits such as track width, copper gap and drill size. Engineers can obtain a direct quote from various PCB subcontractors.

MODELSOURCE

ModelSource is a unique new component library that contains more than 80,000 component schematics and footprints of semiconductors, passives and electromechanical components from leading manufacturers. It is available via the DesignSpark website for any engineer to freely access, with components available in more than 20 different formats for use with other popular PCB design software packages.

ModelSource is also integrated into DesignSpark PCB Version 4.0, greatly enhancing the software tool's existing library. Additionally, ModelSource contains more than 30,000 3D models in 24 formats for widely used mechanical 3D software tools. Engineers can use ModelSource to search by manufacturer or RS part number where a specific part has been chosen for a design. When the choice of device is open, an attribute-driven search can be used to quickly identify components before downloading the model for use in the design tool.

Fundamentally, these kinds of tools and design resources are fast becoming a lifeline for engineers, who are increasingly relying on them to help cut development costs and reduce time-to-market.

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USING THE LIN BUS IN AUTOMOTIVE APPLICATIONS

PROFESSOR DOGAN IBRAHIM OF THE NEAR EAST UNIVERSITY IN CYPRUS DESCRIBES THE FEATURES OF VARIOUS AUTOMOTIVE BUS SYSTEMS AND PRESENTS THE DESIGN OF A MICROCONTROLLER-BASED TWO-NODE LIN BUS PROJECT

The number of electronic components used in vehicles has increased rapidly in recent years. With the increasing demand for safety, comfort and additional performance, we see many more electronic components being added to modern vehicles. As a result, there's a need to connect all these electronic components and modules so they can communicate reliably, safely and in real time.

Today's cars have more electronics and sophisticated devices than ever before: different types of sensors, actuators, monitoring units, navigation systems, entertainment systems, stabilization and traction control aids and so on, which are distributed and embedded in different parts of the vehicle. All of them require to be connected to each other to exchange information related to their functionality and to allow the monitoring of their states at any time. It is estimated that in a typical modern passenger car over 70 electronic control units are used, exchanging over 3000 signals, with this number increasing rapidly with the increased complexity.

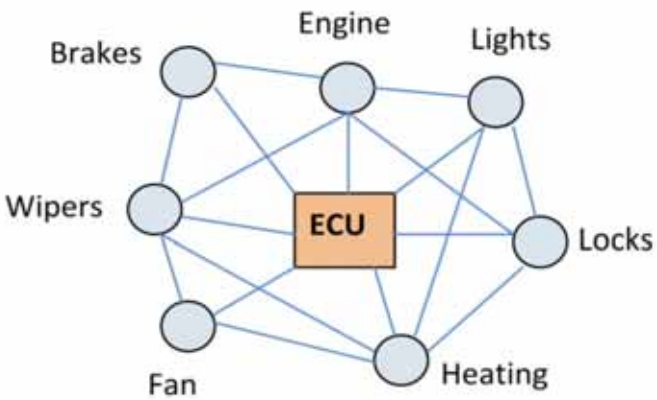

Figure 1: Old-style vehicle electronic wiring

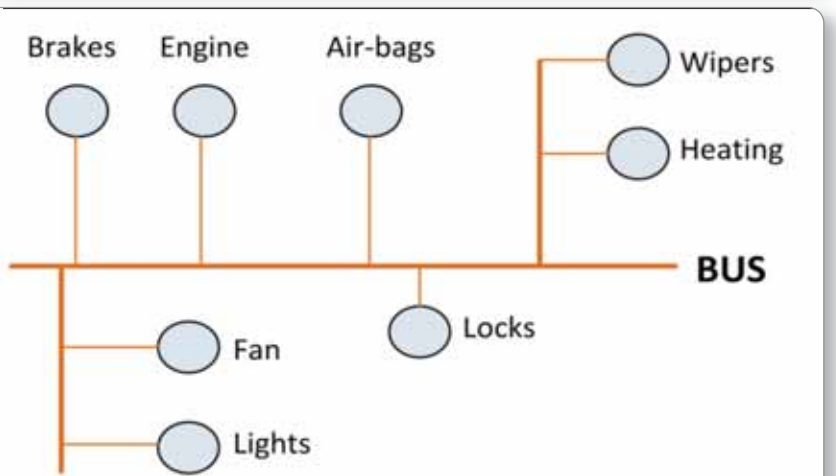

Figure 2: Modern vehicle electronic wiring

In the past, automotive manufacturers connected various electronic components and modules using point-to-point wiring systems. In a typical vehicle hundreds of wires were running between different parts of it. This resulted in bulky, heavy and expensive wiring, and made it very difficult to trace electronic faults. There was no central co-ordination between different parts of the electronics as most modules were controlled locally and unaware of the existence of other modules around. Maintenance and repair of the vehicle's electronics were difficult, since locating a faulty electronic component or a loose wire required complex circuit diagrams where each wire had to be traced individually. Figure 1 shows a traditional old-style vehicle electronic wiring system.

With the growing complexity of vehicle electronics, it became almost impossible for the manufacturers to design safe and reliable electronic systems based on the old, traditional methods. What was needed was some kind of protocol-based electrical connection with less wiring. The solution was to network the various electronic modules in a vehicle, thus eliminating the messy wiring, cutting down the amount of wire used, increasing reliability, and most importantly increasing safety and reducing maintenance and repair costs (see Figure 2). This approach resulted in an "intelligent" car where the various electronic modules can communicate with each other to perform intelligent operations. One example is

automatically turning on the wipers when rain starts, or automatically turning on the lights when it becomes dark or the vehicle enters a tunnel.

Modern Approach to In-Vehicle Connectivity

Groups of manufacturers jointly developed many automotive bus systems. Although each has its own characteristics and performance levels, the most important parameters in an automotive bus system are:

- Safety level;
- Robustness;
- Data rate;
- Cost and complexity;
- Immunity to external electrical noise;
- Reliability.

The advantages of a network-based automotive system can be summarised as:

- Simple and reduced wiring;
- No complex circuit diagrams;
- Lower cost;
- Very easy to trace and detect a faulty module;
- Centralised control;
- Easy to check the health of the overall vehicle.

For example, an engineer can easily communicate with the central controller of the vehicle by plugging-in a dedicated visual monitor unit (or a PC) to check the status of nearly all of the vehicle's electronic modules. Faulty modules can be identified in a matter of seconds and replaced. This approach reduces the maintenance time and cost of repair considerably.

Vehicle Bus Systems

There are many automotive bus systems, some developed by vehicle manufacturers on their own and some developed jointly with other vehicle manufacturers and/or semiconductor manufacturing companies. Some of the most common types of automotive buses and their properties are given briefly here. Table 1 summarises the basic features of the different automotive bus systems:

- CAN;
- LIN;
- FlexRay;
- MOST;
- ByteFlight.

- The CAN (Controller Area Network) bus was originally developed in Germany by Robert Bosch in 1980s for in-vehicle networking. This is a serial two-wire multi-master bus that is one of the most reliable and most commonly used automotive buses today. The physical layer of CAN consists of a pair of twisted wires. The communication speed over the bus is up to 1Mbps (at 40m bus length and it drops to 50kbps at 1000m). CAN bus offers medium speed and reliability, even in noisy environments. In general there are several CAN bus implementations in a vehicle. For example, low speed CAN is generally used to control seat and window operations, whereas brake control and engine management are controlled with high speed CAN. It is important to note that the CAN bus is so reliable and robust that it is also used in other fields, such as industrial automation, aerospace systems, hospitals and building automation systems.
- The LIN (Local Interconnect Network) bus was developed by the LIN consortium consisting of BMW, Audi, Volvo, VW, Motorola, Volcano and DaimlerChrysler. This is a low-speed serial bus designed for in-vehicle communication between intelligent sensors and actuators. LIN bus requires only single 12V wire for its physical implementation (the vehicle chassis is used as the signal return path). The bus can be operated at up to 20kbps and is a single master, multiple slave architecture. In a typical application the master broadcasts a message asking for data and the slave with the correct message header sends back the requested data. LIN bus is used in applications where low speed is acceptable and where the implementation of CAN would be too expensive. Typical application areas of LIN bus are in air conditioning systems, sun-roof control, wiper motors, key-lock mechanism, climate control, small motors and temperature sensors. The maximum communication speed on the bus is 19200 baud over a maximum cable length of 40m. LIN is a low cost bus based on an 8-bit UART interface where the master node is able to synchronise all the slave nodes so the slaves can operate without external timing sources.
- FlexRay was initially developed by BMW

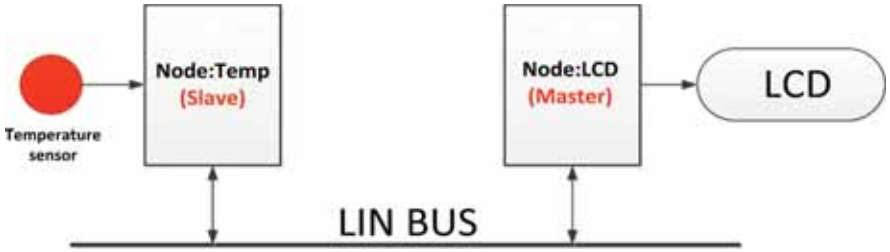

Figure 3: Block diagram of the project

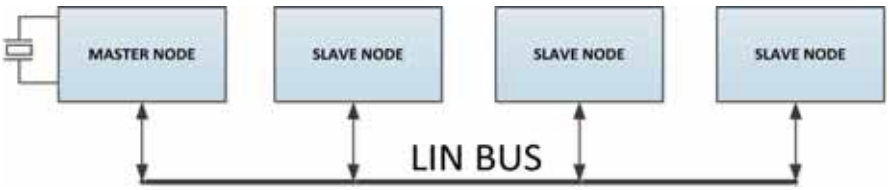

Figure 4: LIN bus structure

Bus	Bus access	Max Data Rate	Physical	Application
CAN	CSMA/CA	1Mbps (at 40m)	Twisted pair	Body, engine
LIN	Polling	10kbps	Single wire	Body, comfort
FlexRay	TDMA/FTDMA	10Mbps	Electrical/optical	Engine, safety
MOST	TDM/CSMA	25Mbps	Optical	Multimedia, navigation
ByteFlight	FTDMA	10Mbps	Optical	Safety

Table 1: Some commonly used automotive bus systems

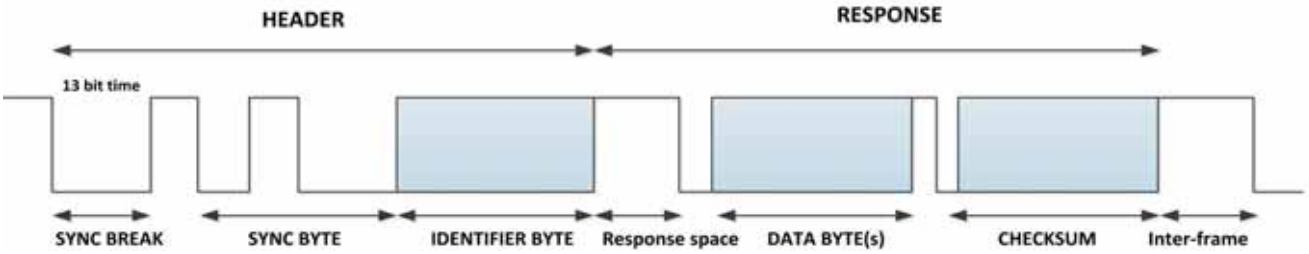

Figure 5: LIN bus frame format

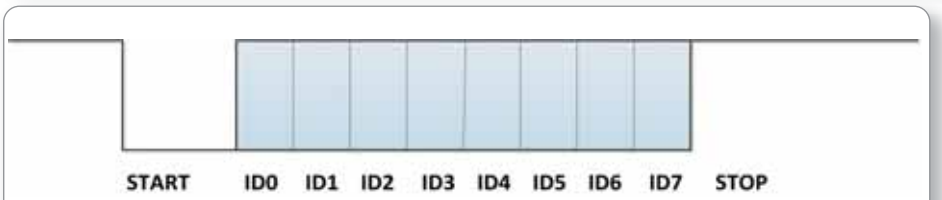

Figure 6: Identifier byte

and DaimlerChrysler as a fast, efficient and error-free serial bus for automotive systems. The bus supports up to 10Mbps and as such is suited to real-time, high-speed, safety-critical and fault-tolerant applications, such as engine, brake and steering wheel control. The physical medium can be either electrical or optical. The bus is based on a TDMA (Time Division Multiple Access) protocol where each device on the bus has a fixed slot allocated to it. TDMA is deterministic and thus is extremely reliable, since the respond times of devices on the bus are known. FlexRay has been chosen as the most suitable protocol for steer-by-wire and brake-by-wire applications on modern vehicles.

- The MOST (Media Oriented Systems Transport) bus is used in telemetric and multimedia applications in modern vehicles, such as video, audio, navigation (GPS), communication and so on. To ensure safe and reliable operation that is not susceptible to electromagnetic noise, MOST uses optical media with very high bit-rate (maximum 24.8Mbps in synchronous and 14.4Mbps in asynchronous mode) and the protocol is based on TDM/CSMA (Time Division Multiplex/Carrier Sense Multiple Access). MOST supports up to 64 nodes that can be arranged in ring, star, or chain topology.
- ByteFlight has been developed by BMW together with Motorola, Elmos and Infeneon for use in high-safety related applications, such as automotive and avionic systems. The bus is based on FTDMA (Flexible Time Division Multiple Access) protocol and combines both event-controlled and time-controlled protocols to guarantee deterministic latencies for high-priority messages. ByteFlight offers 10Mbps bandwidth with optical physical connection. ByteFlight supports several bus systems in a mixed bus environment. For example, CAN bus and ByteFlight can co-exist and can communicate and interchange data in the same vehicle environment. Special controllers are available to create a mixed bus system with ByteFlight, CAN and others.

ID4	ID5	Data length
0	0	1 byte
0	1	2 bytes
1	0	4 bytes
1	1	8 bytes

Table 2: The length of the data bytes and their codes

MCU-Based LIN Bus Project

This section covers a simple project that will demonstrate the theory and operation of the LIN bus by showing how two nodes can communicate over it. As shown in the block diagram in Figure 3, the project uses two PIC microcontrollers as LIN nodes. Node TEMP has an analog temperature sensor IC connected to one of its analog ports and node LCD has a 2x16 text based LCD connected to its output port.

In this simple application, node TEMP is selected as the slave and node LCD is the master. The master requests the current temperature every second from the slave and then displays it on the LCD.

LIN bus has been developed for low-speed and low-cost applications. Main features of this bus are (further details can be obtained from http://www.lin-subbus.org):

- Master-slave with one master and up to 15 slaves;
- 1-wire bus (vehicle chassis is the signal return path);
- Data rates from 1 to 20kbps (19.2kbps is usually used in automotive applications);
- Only master needs an accurate crystal clock since the slaves self-synchronise to the master;
- Multicast data transmission over the bus;
- 2, 4, or 8 byte data messages;
- Sleep/wake capability to reduce power consumption;
- Checksum (8 bits) and parity (2 bits) error detection;
- Compatible with UART serial communication protocol.

Figure 4 shows a typical LIN bus structure. The bus supports up to 16 nodes, where bus length is limited to 40m while operating at 19.2kbps. Since the bus is based on an 8-bit UART interface, the protocol can easily be implemented by almost all microcontrollers, either in software or hardware.

The LIN Bus's Characteristics

The LIN bus protocol is based on frames (see Figure 5). A frame consists of a Header and a Response with the following fields:

- Synchronisation break;
- Synchronisation byte;
- Identifier byte;
- Response space;
- Data byte(s);
- Checksum byte;
- Inter-frame space.

Synchronisation break is a low signal on the bus which lasts for at least 13 bit times and is terminated with a high signal lasting at least one bit time on the bus.

Synchronisation byte is sent only by the master and is used for slave self-synchronisation. This byte is sent in accordance with UART asynchronous serial

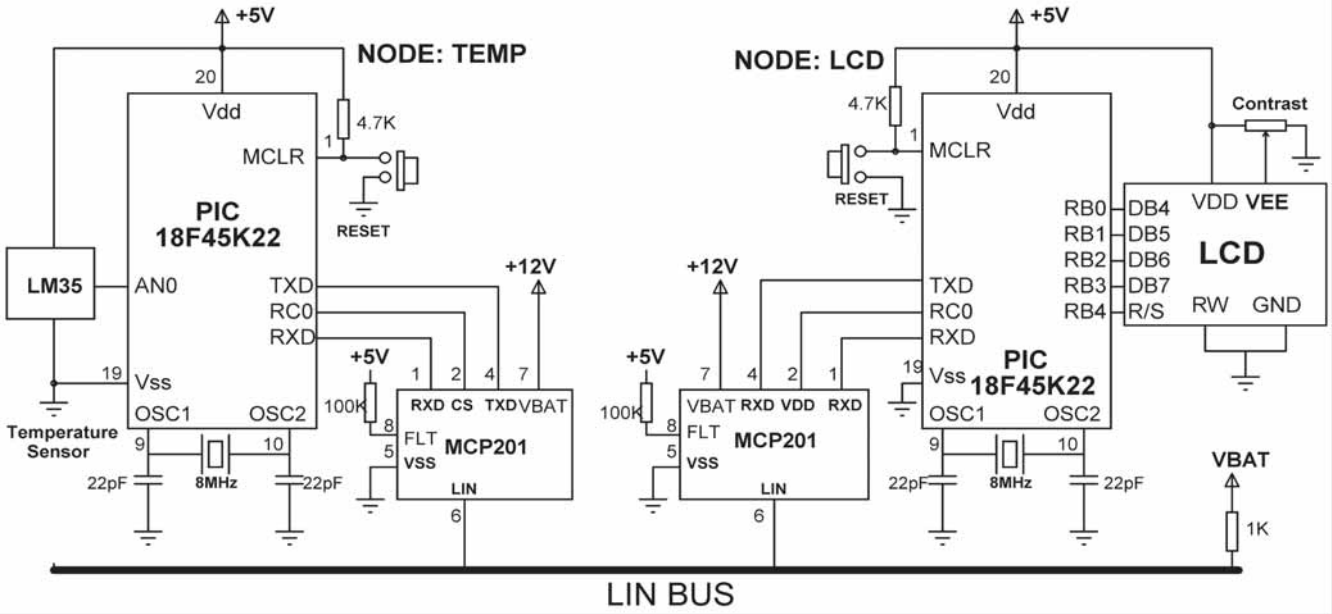

Figure 7: Circuit diagram of the project

communication standards, i.e. the data starts with a start-bit and is terminated with a stop-bit. The byte sent is consecutive ones and zeros, i.e. bit pattern "01010101" (hexadecimal 0x55). A slave can extract the data bit-rate by measuring the overall 10-bit synchronisation byte length (including start and stop bits) and then dividing it by 10.

The identifier byte defines the destination identity and the length of the data bytes that follow. There can be up to 64 identifiers, organised in 4 groups of 16 messages. Figure 6 shows the identifier byte in detail. The first four bits (ID0 to ID3) define the message identifier, bits ID4 and ID5 define the length of the data bytes that follow, and are coded as in Table 2.

Bits ID6 and ID7 are used for parity, where parity is used for the identifier bits only. ID6 is the even parity and ID7 is the odd parity, both calculated as follows:

ID6 = NOT(ID1 Ø ID3 Ø ID4 Ø ID5)
ID7 = (ID0 Ø ID1 Ø ID2 Ø ID4)

where Ø is the logical "Exclusive-OR" operation.

After the identifier and the response space, a slave can begin to send the requested response over the bus, or alternatively it can get any data sent for itself.

Data bytes can be 1, 2, 4, or 8 bytes long and they can be transmitted either by the master or the slaves. The data is transmitted in UART asynchronous serial communication standards with one start bit and one stop bit.

Checksum byte is computed only on the data bytes. The calculation is based on a simple inverted modulo 256 sum where the inverted eight bit sum along with the carry bit from all data bytes are used in the calculation. New release LIN2.0 specification uses a new checksum called enhanced checksum where the identifier byte is also added to the checksum calculation (the new release still supports the old LIN1.3 checksum calculation).

Inter-frame space simply consists of a high signal on the bus to denote the end of a frame.

The LIN bus supports sleep and wake-up modes in order to save power when the vehicle is not used. The sleep command is sent from the master as three identifier bytes 0x3C, followed by data byte 0x00. After receiving this command the slaves enter the sleep mode.

Figure 8: EasyPIC V7 microcontroller development board

A slave can awaken the master if an event occurs and this re-starts communication on the bus. The wake-up identifier is 0x80. In addition, a master can also wake up slaves by sending the identifier 0x80 on the bus. Once the request has been sent, normal communication resumes on the bus.

The LIN bus supports a primitive error detection mechanism by using checksum and parity bits. There are no error correction mechanisms and normally the master is expected to manage the error detection and recovery procedures.

The Project Hardware

The circuit diagram of the project is shown in Figure 7. Each node consists of a PIC18F45K22 microcontroller and a MCP201 type LIN transceiver chip, providing half-duplex, bidirectional communications

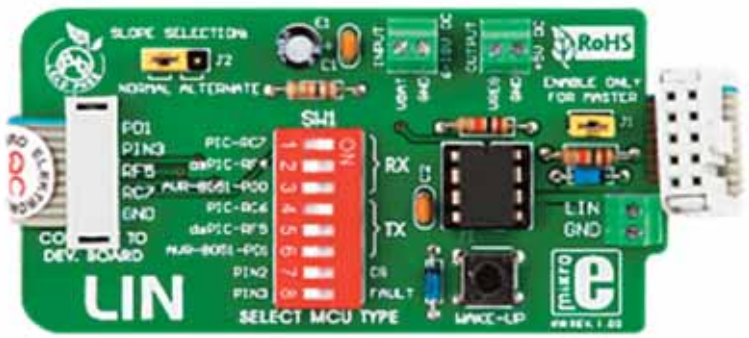

Figure 9: LIN bus board

interface between a microcontroller and the serial network bus. Pins RXD and TXD of the chip are connected to microcontroller UART ports RC7 (RXD) and RC6 (TXD) respectively. The output pin (LIN) of the chip is connected to the LIN bus. An external 12V power supply is used to power the chip. In addition to a bus interface, the MCP201 incorporates wake-up logic and fault-detect output. Since the LIN bus is open-collector it is pulled-up with a 1K resistor. The MCLR pin of the microcontroller is connected to an external reset button.

An LM35 type analog temperature sensor is connected to analog input AN0 of the slave node TEMP. Similarly, a text LCD is connected to PORT B of the master node LCD. The master node is assigned identifier 3 and it requests the temperature every second from the slave node, which is given identifier number 5. The received temperature is displayed on the LCD connected to the master node, in integer format for simplicity.

Construction Of The Project

The project was built using a pair of mikroElektronika EasyPIC V7 (see Figure 8) microcontroller development boards and a pair of LIN bus boards (see Figure 9), incorporating the MCP201 transceiver chip. The LIN bus board is simply connected to PORT C, to the IDC10 I/O port connector at the edge of the microcontroller board. Connections to the LIN bus board can be configured using an 8-way DIL switch located on the LIN bus board. In addition, the board contains a pushbutton switch for manual wake-up of the MCP201 chip but this feature is not used in this simple, example, project. EasyPIC V7 includes all the hardware, microcontroller programmer and in-circuit debugging tools necessary for easy and quick microcontroller-based system development.

The Project Software

The project code was developed using the mikroC PRO for PIC language, which includes a rich set of library functions supporting peripherals such as USB, CAN, RS232, RS485, LCD, GLCD, SD card, I2C and so on. The operation of the project is described as a PDL in Figure 10. Nodes TEMP and LCD are given identifier numbers 5 and 3 respectively.

Master (Node: LCD)

```
BEGIN
  Configure I/O ports and UART
  Configure LCD
DO FOREVER
    Send Synchronisation break
    Send Synchronisation byte
    Send identifier 5 to request data
    Wait and read temperature from the bus
    Display the temperature
    Wait 1 second
  ENDDO
END
```

Slave (Node: TEMP)

```
BEGIN
  Configure I/O ports and UART
  Configure A/D converter
  DO FOREVER
Wait for Synchronisation break
Wait for Synchronisation byte
Read identifier
IF data is requested from this slave THEN
    Read temperature from the sensor
    Send temperature over the bus
                    ENDIF
            ENDDO
END
```

Figure 10: Operation of the software

The UART module inside the PIC microcontroller is programmed to operate at 19.2kbps and is set to generate the synchronisation break and the synchronisation byte at the beginning of a frame. The master node then requests data from the slave by sending the slave identifier. The received data is displayed on the LCD by the master. The slave task waits until it receives a request for data and then reads the temperature from the sensor via the A/D converter, sending this data over the bus. The temperature is sent as only one-integer data for demonstration purposes. The above process is repeated forever. Note that for simplicity the error conditions (parity and checksum) are not checked here. In normal operations the error conditions must be checked and corrective actions must be taken for error-free communications on the bus.

The operation of a LIN bus can easily be analysed using protocol analyser hardware/software systems. The Lin Bus Serial Analyzer from Microchip is a dedicated hardware analyser box (Figure 11) that is connected between a PC and the LIN bus under investigation; the data on the bus is captured and displayed on a PC screen. The LAP-C (www.zeroplus.com.tw) is a PC-based logic analyser incorporating protocol analysis software for various bus systems, such as CAN, LIN, I2C, USB, RS232, RS485 and many more. Any activity on the bus can be captured and displayed on its associated PC screen for analysis. ●

Figure 11: LIN bus board

SDR Demonstrator for Wireless Data Systems

The DE9941 is a credit card sized demonstration platform for a complete Software Defined Radio (SDR) for wireless data applications. It is designed to be small and low-cost with minimal components/values.

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- CMX994 Direct Conversion Receiver
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ESCAN – AN OPEN SOURCE, HIGH BANDWIDTH, EVENT-SCHEDULED CONTROLLER AREA NETWORK

A. WILLIAMS, C. QUIGLEY AND **R. MCLAUGHLIN** FROM WARWICK CONTROL TECHNOLOGIES

INTRODUCE THE ESCAN PROTOCOL, INCLUDING A BRIEF COMPARISON WITH OTHER SCHEDULING PROTOCOLS USED IN AUTOMOTIVE APPLICATIONS

Event Scheduled CAN (ESCAN) is an open source scheduling protocol for CAN (Controller Area Network). The aims of the protocol are discussed here, including the ability to optimise the available bandwidth over CAN and enable maximum bus loading, as well as providing a worst case determinism for message reception. These advantages include a simple-to-implement basic protocol stack; no special hardware requirements are needed to support the protocol other than a TTCAN compliant CAN controller (this is so the retransmission of CAN frames can be disabled).

The protocol also uses a small amount of CPU and memory overhead to transmit its schedule control data, resulting in high potential bus loading at all CAN bit rates.

In this article, the protocol itself will be introduced along with a brief comparison with other scheduling protocols in the literature. Preliminary experimental performance data for ESCAN is collected and compared with a TTCAN Level 1 implementation showing benefits. Finally the effect of using ESCAN as a scheduling layer for the CANopen protocol will be analysed.

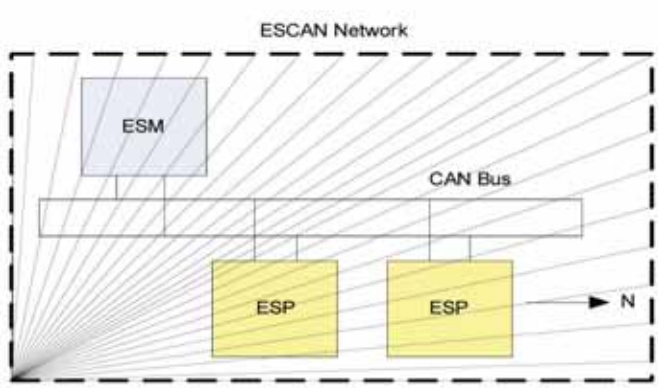

Figure 1: Basic ESCAN network

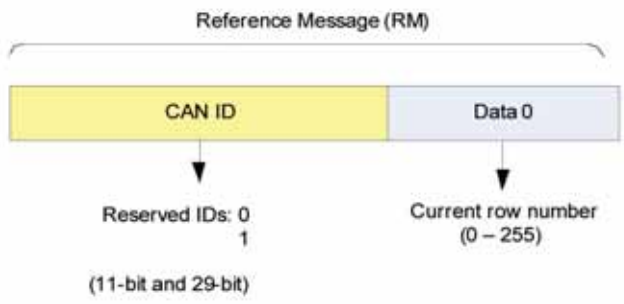

Figure 2: Reference Message (RM) format

Determinism and CAN

CAN was developed by Robert Bosch GmbH in the 1990s [6] and has become the most prominent open standard network protocol used by the automotive industry. One problem of CAN is its inherently non-deterministic nature, and designers tended to rely on the protocol itself to schedule message transmission effectively. This approach, in turn, created a number of problems during systems integration, such as non-deterministic message delays and bus loading.

It is a well-known feature of CSMA-CD (Carrier Sense, Multiple Access, Collision Detection) type networks such as CAN that they can operate with reasonably predictable message latency up to about 40% bus loading. An excursion beyond this leads to great variability in the latency for lower priority messages.

A solution to the bus loading problem of the non-deterministic approach was developed at Volvo [5] that could determine the worst-case message latency by assigning higher priority (or periodicity) signals to higher priority CAN messages. Lower priority signals (or periodicity signals such as those that are event triggered) are assigned to lower priority CAN messages. The result was that the CAN bus was able to run at a higher loading, with the worst case latency known at the design time of CAN messages; therefore, design trade-offs could be made to ensure acceptable latency. This is a Pseudo-Deterministic approach, since the determinism is defined as worst-case latency; this is the process implemented in the Volcano tools [4].

The key principles of this CAN design process are based on a Publisher-Subscriber model [3]. This methodology improves the procedure of traditional CAN bus development using a non-deterministic methodology, since it allows

the OEM to deal much better with multiple system suppliers.

Pseudo-deterministic approaches for CAN and work by Kopetz on the Time Triggered Protocol (TTP) [2] have led the way to an improved deterministic approach to design for time-triggered protocols. Time-triggered protocols are deterministic in nature and their associated design process deals much better with the systems' integration issues, since they allow the designer to easily conceptualise the communications timing and map signals and messages across different buses. They are also good for dealing with the problem of multiple suppliers in the same way, as pseudo-deterministic approaches.

The CAN protocol was extended under ISO-11898 part 4 to Time Triggered CAN (TTCAN) to address the determinism problems of CAN and therefore provide a deterministic approach for CAN systems. The main characteristic of TTCAN is that bus access is controlled via a Time Division Multiplexed Access (TDMA) type method, using a regularly repeating cycle of time called the Basic Cycle. The Basic Cycle is divided into a fixed number of time windows (fixed at design time), which can be a mixture of four types: Reference Message, Exclusive Window, Arbitration Window and Free Window. This is sent by the time master control unit (global time master) and controls the timing of the Basic Cycle [7].

This is a technology currently available for commercial automotive applications such as private networks, and effectively doubles the usable bandwidth of CAN [1].

ESCAN

ESCAN is an abbreviation for Event Scheduled Controller Area Network, a scheduling protocol for CAN messages. The protocol is inherently simple, allowing a reliable schedule to be developed in the minimum amount of time, achieving high efficiency and reliable operation.

The network is formed by a higher-layer protocol that sits on top of the CAN network specified in the ISO 11898 standard [6].

It is a way of controlling messages on the CAN network through scheduling, in order to achieve maximum efficiency and determinism. As the protocol sits on top of the CAN network, the physical connections, interfaces, messages, etc, remain as specified in the above-mentioned ISO standard.

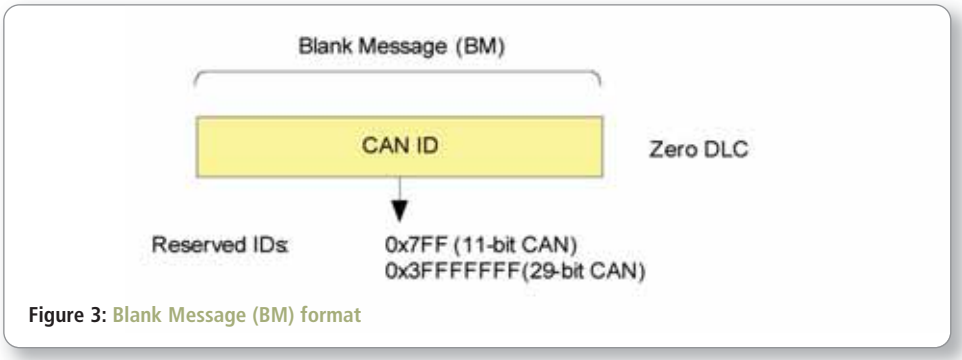

Figure 3: Blank Message (BM) format

Figure 4: The basic ESCAN global schedule matrix

The ESCAN protocol was introduced and described in detail in 2011. It has many advantages for embedded system developers over existing protocols such as TTCAN, including:

- Simple and easy to implement protocol with a basic software stack;
- No dedicated hardware required; i.e. scheduling is implemented in software;
- Reliable, with added redundancy when the option-redundant master is used;
- Plug-and-play of extra nodes;
- Excellent expandability of the network, without the need for any rework to the current nodes. Schedule size can be altered during operation, and other parameters can be tuned to improve efficiency;
- Low bus overhead for schedule control data;
- High bus loads possible at all CAN bit-rates.

> ESCAN is an abbreviation for Event Scheduled Controller Area Network, a scheduling protocol for CAN messages

ESCAN Network and Nodes

An ESCAN network consists of two types of nodes: the Event Schedule Master (ESM) and an Event Schedule Participant (ESP) (shown in Figure 1). There must be at least one ESM and one ESP on a network.

The protocol does not place any limitations on the number of ESPs on the network – this is governed by the physical properties of the CAN bus and node interfaces, per the ISO 11898 CAN network [6].

The ESM is a dedicated node on the network for controlling and monitoring the schedule and has no other function. It transmits two types of messages onto the network: a Reference Message (RM) and a Blank Message (BM). The ESP is a regular node on the network, performing its designed tasks and communicating information to other ESPs over the network. ESPs transmit their messages within allocated schedule slots and use received messages from other ESPs on the network, if required.

ESPs only transmit one type of message – Data Messages (DM).

There are three types of messages on an ESCAN network: Reference Messages (RM), Blank Messages (BM) and Data Messages (DM). All three types of messages are the traditional CAN frames specified in the ISO 11898 specification, but have special meaning within the context of the higher layer protocol. All

Bit-rate (kbit/s)	Master CPU Loading (%)	Slave CPU Loading (%)	Max. Bus loading (%)
50	3.6	1.4	96.5
100	4.9	2.7	95.5
125	5.9	3.3	94.5
250	8.9	6.4	90.9
500	14.4	11.9	84.9
1000	23.2	20.8	74.3

Table 1: ESCAN controllers @ 20MHz

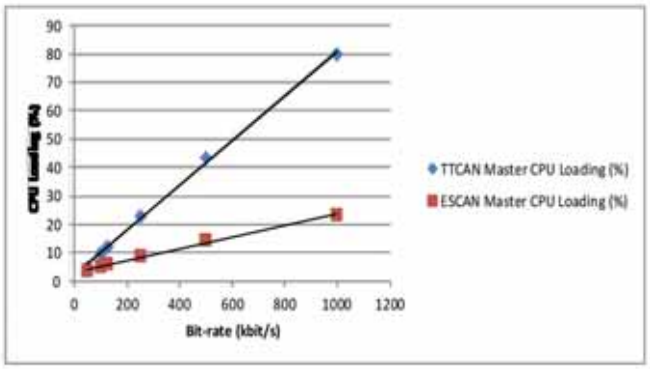

Figure 5: ESCAN controllers @ 20MHz

types of messages can use either 11-bit or 29-bit CAN identifiers, depending on the application, however it is recommended that 11-bit IDs are used where possible to increase efficiency.

Both ESM and ESP nodes receive all types of messages on the network in order to process and communicate using the schedule.

Reference Message (RM)

The RM is transmitted by the ESM and marks the beginning of a Row Cycle (see the ESCAN Schedule section). The CAN ID of an RM is reserved by the protocol and can be either 0x0 or 0x1, depending on whether a redundant ESM is implemented or not (see the Redundant ESM for Critical Applications section).

The RM has a fixed DLC of 1 byte containing the current row number within the schedule. The row numbering system in ESCAN begins with 0 and goes up to 255, i.e. 256 rows. This row number data byte enables ESPs to synchronise with the schedule. A diagram of the RM is shown in Figure 2.

Blank Message (BM)

The BM is transmitted by the ESM and to ensure continuation of the ESCAN network either when free slots are implemented or in the event of an ESP failure. The CAN ID of the BM is reserved in the ESCAN protocol and is either 0x7FE for 11-bit CAN or 0x3FFFFFFE for 29-bit CAN, i.e. one higher than the lowest priority ID available.

A BM contains no information for the other nodes and, therefore, has a DLC of 0 at all times.

Data Messages (DM)

Data messages are transmitted by ESPs only, and are used to communicate data from one ESP node to another. These are the normal frames transmitted on non-scheduled CAN networks.

The only limitations on these messages are they do not use the reserved CAN IDs of the RM and BM, and they are not remote frames (remote frames are forbidden on an ESCAN network). Apart from these, they can be of any length (DLC) and any ID format (11-or 29-bit).

ESCAN Schedule

All ESPs communicate to other ESPs by transmitting messages at particular times set out by the Global Schedule Matrix (GSM), a basic example of which is shown in Figure 4.

The GSM can be viewed as an X by Y matrix, where X is the number of columns and Y is the number of rows in the matrix. There can be any number of columns between 2 and 256 inclusive, and any number of rows between 1 and 256 inclusive.

The numbering system within ESCAN always begins at 0 for both rows and columns. Each cell within the GSM represents a transmission slot for one of the three types of CAN messages. Each row of transmission slots is called a Row Cycle. The transmissions in the first column of the GSM are always filled by reference messages from the ESM. The rest of the slots in the GSM are either filled with Blank Messages from the ESM or DMs from the ESPs.

Each DM slot is dedicated to a single message i.e. multiple messages do not share a slot. A message can transmit in any of the non-RM slots. Slots that are not occupied by an RM or a DM are filled in with BMs from the ESM. The purpose of filling unused slots with BMs is so that there is always some form of message event in each slot. A slot without a message event would cause the bus to stop, and for this reason BMs are mandatory.

The ESM

The ESM is a dedicated node on the network. Its sole task is to transmit the RMs at the beginning of each Row Cycle, and to transmit BMs in slots which are not occupied by DMs from ESPs. Its responsibilities are to ensure that every slot within the GSM is filled by a message at all times.

The ESM is the first node to transmit on the network. All ESPs wait for the ESM to transmit its first RM before they begin in order to synchronise to the schedule transmitted by the ESM. As mentioned before, the ESM must fill all empty slots within the GSM with BMs. The ESM does not need to know where the empty slots are in order to transmit its BMs. Instead, the ESM waits for a period of time after the previous message in the schedule, known as the ESP-Response Gap (ESP-RG) – see box on the next page, for any ESP to transmit a DM into the current slot. If after this period a DM has not been transmitted, the ESM transmits a BM onto the network to fill the slot.

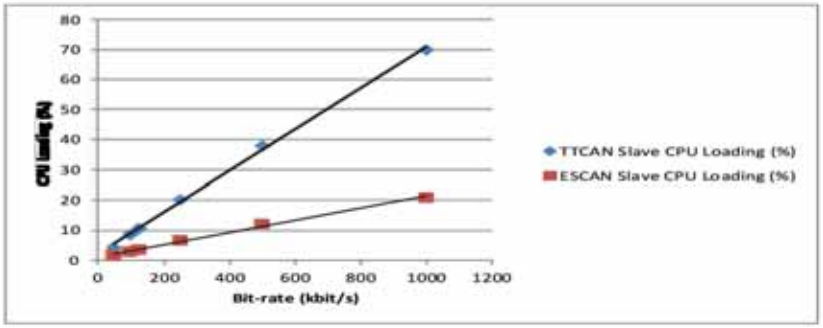

Figure 6: Comparison of TTCAN and ESCAN slave CPU performance

The ESP

The ESP transmits its DMs in specific slots within the schedule. The ESP's primary responsibility when it comes to the schedule is to keep track of the current slot within the schedule and to transmit its messages in assigned slots when the time arises.

In order for the ESPs to work with the ESCAN schedule they must receive every message on the bus. The ESP has two variables in order to use the schedule: a Current Row variable and a Current Column variable.

When an ESP starts up it is required to synchronise itself to the network schedule. Synchronisation is done through the reception of an RM from the ESM. The ESP waits until it receives an RM on the CAN bus. When the first RM is received, the ESP sets the current row variable (according to the RMs data byte) and the current column to 1. Then, the ESP is in a position to communicate using the schedule.

Should an ESP be disconnected from the network and reconnected again, it is important that the synchronisation procedure be performed again, otherwise it will attempt to communicate with incorrect schedule information. This means an ESP can be connected to the network at any time, and is able to start communicating at the soonest possible moment.

Dynamic Schedule Negotiation

Higher layer protocols such as CANopen generally consist of a mixture of periodic frames (in the case of CANopen, Process Data Objects are generally transmitted periodically) and infrequent unscheduled bursts of data, for example configuring a CANopen node using Service Data Objects.

A scheduled approach to transmitting data works well for period data but it is wasteful to allocate slots in a schedule for frames that will only be used occasionally. The ESCAN protocol extends the concept of schedule tables and allows the participants in a network to dynamically expand and shrink the schedule table.

In normal operation the ESM will wait for the ESP-RG timeout to expire and then transmit a BM in order to maintain the schedule matrix. A BM is transmitted with a low-priority CAN frame (defined by the network designer) with a DLC of 0. The ESM keeps track of how many times a BM has had to be transmitted into a particular slot and after a configurable number of consecutive BMs have been transmitted (default is 5), the ESM will begin to transmit Empty Messages in that cell of the matrix.

An Empty Message has the same format as a Blank Message, however a lower priority CAN identifier is used. Once a slot has been marked as Empty it is now available for another ESP to use for transmitting messages. The communica-tions stack on the ESP will keep track of the empty slots, and when an immediate frame transmission is requested the next available empty slot will be allocated to the ESP. The ESP can then use this slot to transmit any message it chooses with any identifier, depending on what the application on the ESP is currently doing. In the case of a CANopen node, the new slot can be used for SDO transfer between a master and a slave.

Once an ESP no longer needs additional slots in the schedule it can stop transmitting a CAN frame in that position. Once again the ESM will begin transmitting BMs in that slot to ensure that the network remains synchronised and the ESPs can still count the column index.

After the configured number of consecutive frames has been transmitted, the ESM will flag the slot as blank and available for other ESPs to use.

Extending the Schedule

Since the schedule can be built up dynamically with ESPs requesting and releasing slots as they need them, the schedule could quickly fill up from its initial size. The ESM therefore always transmits an RM at the end of the schedule table and immediately transmits a single Empty Message.

If no ESP is waiting for a slot then the ESM will transmit the RM with a row index of 0 and restart the schedule. If an ESP is waiting for a vacant slot for transmission then it can use this Empty Message. The ESM will then flag this as a

ESP-RESPONSE GAP (ESP-RP)

ESPS MONITOR THE CURRENT POSITION WITHIN THE SCHEDULE BY KEEPING TRACK OF THE ROW NUMBER WITHIN THE REFERENCE MESSAGE AND THE NUMBER OF MESSAGE EVENTS RECEIVED IN THAT ROW SINCE THE REFERENCE MESSAGE.

In order for the schedule to work, a time gap is introduced by the ESM to allow an ESP to respond with a message before a Blank Message is transmitted.
This time gap is called the ESP-Response Gap (ESP-RG). The length of this gap is dependant solely on the slowest processor on the network. There is no recommended ESP-RG value – it must be determined by the developer.
There are two ways to calculate the optimum ESP-RG value: by calculating the response time for each ESP on the network using a simulator or other hardware setup; or by configuring the network using a large value for the ESPRG and using a bus analyser to determine the actual ESP-RG of the ESPs on the bus. The ESP-RG can then be lowered to the optimum value during network operation through the ESM, in order to achieve the best performance (see the Dynamic aspects of the Schedule section for more information on the dynamic aspects of ESCAN).

Rows (Cycles)	User Columns (Windows)			
	1	2	4	8
1	25 *(58)*	26 *(63)*	28 *(73)*	32 *(93)*
2	26 *(64)*	28 *(72)*	32 *(88)*	40 *(120)*
4	28 *(76)*	32 *(90)*	40 *(118)*	56 *(174)*
8	32 *(100)*	40 *(126)*	56 *(178)*	88 *(282)*

Table 2: ESP memory usage in bytes – TTCAN values provided for comparison in brackets and taken from a previous study [1]

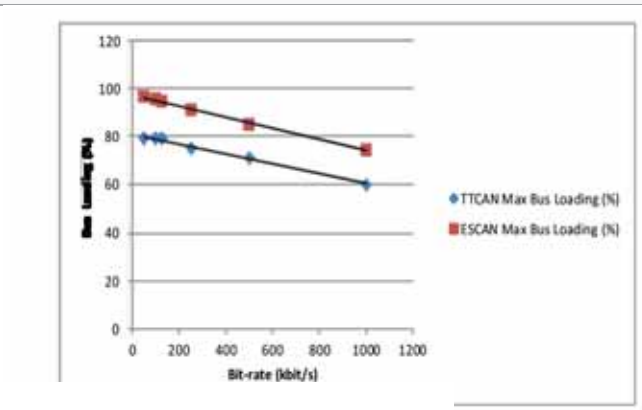

Figure 7: Comparison of TTCAN and ESCAN max bus loading

valid row and continue to transmit an RM for it. It will also fill the remaining slots of the row with Empty Messages.

To reduce the schedule the ESM monitors the last row of the current schedule table. Once a row consists of Empty Messages in its entirety, it is deleted from the schedule and is no longer transmitted. The row count is reduced by one and the placeholder RMis transmitted at the start to indicate a blank row.

Comparison of ESCAN and TTCAN Implementations

In order to compare the performance characteristics of the ESCAN protocol with the nearest equivalent higher layer protocol – TTCAN Level 1 (software implementation), an Atmel CC01 processor was configured with the protocol stack for ESCAN and a basic 10 column x 10 row schedule table created to allow the CPU performance characteristics to be compared against results obtained from analysis conducted with TTCAN by Quigley et al [1]. The experimental setup consisted of a single ESM node and an ESP configured to transmit a data frame in every slot of the schedule matrix. The frames transmitted are static and there is no application-specific processing being done in addition to the ESP and ESM protocol stacks.

Performance Comparison of Master Nodes

The current implementation of the ESM protocol stack compares exceptionally well with a TTCAN Time Master node, with a significant reduction in the CPU requirements necessary to run the master task.

The CPU requirements for the ESM compares favourably in the way that it scales with an increased bit rate. At 1Mbit a TTCAN Master is at 80% CPU utilisa-tion, leaving only 20% available for the user application; an ESM node running
at 1Mbit requires just under 25% of the available CPU cycles, leaving 75% available for the application that is running alongside the protocol stack.

The memory requirements for the protocol master (ESP) implementation used in this comparison are fixed for all schedule sizes as the usage is not dependant on the size (ROM 1284 bytes, RAM 31 bytes).

Performance Comparison of Slave Nodes

The memory requirements for the slave protocol implementation used is detailed in Table 2. This highlights the difference in memory requirements for a basic implementation with a single 8-byte data frame.

As the schedule matrix is increased in size, the only additional memory required is for an internal message index. There would be additional memory requirements introduced by adding more distinct CAN messages, however this is at the application layer and is not a consequence of the scheduling protocol.

Comparison of Bus Loading

The maximum bus loading achieved with the current implementation of the protocol stack is detailed in Figure 7. The synchronisation mechanisms used by the protocol mean that there is no CAN identifier arbitration needed on the bus, as all frames are transmitted on the schedule rather than contesting for access to the bus. This results in a 14-18% improvement in the achievable bus loading across all bit rates. The reduction in bus loading found at the higher bit rates is due to the fixed processing time and fixed response gap periods becoming proportionally more significant.

Further ESCAN Work

The ESCAN scheduling protocol provides a marked improvement in memory utilisation, CPU loading and higher bus loading over the TTCAN level 1 implementation in [1]. Existing higher layer protocols, such as J1939 and CANopen, could be implemented on top of an ESCAN implementation to take advantage of the higher bus loading capabilities available. These protocols would particularly benefit from the scheduling since the timing parameters for protocol features such as PDOs in CANopen are generally fixed and can be positioned in to the schedule matrix at fixed intervals, where they are guaranteed bus access.

The reduction in memory and CPU requirements results in additional resources being freed up for more complex application or, alternatively, would allow the selection of a lower cost microcontroller part with fewer available resources, or permitting the microcontroller to run at a lower clock frequency, reducing the power requirements and temperature of the system.

The current design for dynamic scheduling does not take the timing requirements on the existing messages into account. For example, when the schedule table is extended, a message currently transmitted every 100ms could end up being transmitted every 150ms, as the schedule is expanded and takes longer to cycle around back to the same point.

A mechanism needs to be defined that can maintain these timing constraints and ensure that critical messages are sent at their expected interval.

Analysis of the potential for schedule fragmentation needs to be conducted, as well as researching the effect these additional scheduling techniques could have on the stack size and performance of the network, given that the primary motivation for ESCAN is a high performance network.

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WHAT THE READERS SAY

ACADEMIA AND INDUSTRY DISCONNECT

In September letters, Ivor Catt pedantically refers the reader to his "Question", which has to do with an ideal step function on an ideal lossless transmission line, and asks where the charge comes from.

The real world is what needs modelling, in order to make sense of what is happening, and Raymond Boute does just that (June issue, p38), which is a much simplified explanation similar to the response Dr Pepper gave to Catt many years ago.

I don't expect anyone will ever satisfy Catt as his dispute appears to be with what is taught by academia and lack of consensus on which view to adopt.

My bigger concern with academia is the disconnect between course content and industry practice. Many of today's students have a poor concept of even basic electronics, while at the same time trying to use complex ICs or digital devices.

My own brief experience with further education teaching convinced me that the actual teaching came a poor second to securing ongoing funding for the next academic year, and revising courses to take account of new ideas was even lower. The primary aim seemed to be to teach enough of the curriculum (often well out of date) to get students through the exam/assessment process, without worrying to much about what actually happens in the real world.

I can safely say that most of my learning about electronics was during my working life as a broadcast engineer, dealing with real-world problems. But whereas my enthusiasm and interest was maintained by several electronics magazines, with detailed projects to build and IP freely shared, these days there is little, as more and more people guard IP, fearful that someone else will profit from their ideas. In today's world the series of articles about current dumping amplifiers, as pioneered in the Quad, would probably never appear, as the fear would be that some Chinese company would mass produce them at much lower cost.

Sadly, a more connected world seems to have stifled the sharing and collaboration that allowed the blossoming of electronics during the '70s and '80s. Also, the complexity of much of today's electronics is such that "hobbyist" construction is out of the question. (Anyone want to do a Smart Phone project?!)

There is still a place for projects to enthuse the youth of today, and maybe initiatives like the Raspberry Pi will help. It is to be hoped so!

Ray Lee

electronica

13 – 16 November 2012, Messe München

Opening hours: Tue – Thur: 9am – 6pm
Fri: 9am – 5pm

electronica is the world's leading trade fair for electronic components, systems and applications. It has been held every two years in Munich since 1964 and presents innovations from the entire range of products and services in the electronics industry.

electronica is the most important international meeting-point for the electronics industry and in addition to the exhibition areas, it features a supporting program containing conferences, such as the electronica Automotive Conference, and various indsutry-related discussions.

In 2010 electronica was attended by 72,000 visitors, and some 2.578 exhibitors showcased their products and services. The total amount of exhibition space was 142,500 square meters. As in the past, the 2012 fair will feature well-known major manufacturers, as well as interesting specialists and newcomers.

The program consists of many related events, which include three international conferences, four forums, CEO roundtable and over 300 lectures. In addition, and for the first time ever, there will be an embedded platforms conference on the 14th and 15th of November. Together with the exhibition and the forum, it is part of the show's three-pronged approach to embedded electronics.

Embedded technologies are very significant throughout the entire electronics industry. At electronica 2010 that fact was underlined by 230 German and international companies in this sector and by the embedded forum. This year, the embedded platforms conference not only gives exhibitors an additional platform where they can present their developments and solutions, but it gives system architects and developers an opportunity to gather information about pioneering technologies and their potential applications.

When developing a successful product, selecting the right embedded module – i.e. the processor platform, operating system, drivers and networking technology – is not the only thing that plays an important role. It is also essential that the individual components interact correctly and that they are adapted to suit the specific application.

"The conference is our way of addressing this challenge for embedded system engineers, who can come here to gather specific information about selecting a platform that is right for them," said Nicole Schmitt, electronica Exhibition Director.

"Processor and controller manufacturers and their software partners can also attend seminars and lectures to find out what solutions they can use to support developers in the areas of component selection and system design. Sponsors that have already indicated interest include Infineon and TQ Components," she added.

More information about electronica 2012 is available online at www.electronica.ds

Sensirion Launches The World's Smallest Humidity And Temperature Sensor

At Electronica 2012 Sensirion presents the world's smallest humidity and temperature sensor, setting new standards for size, power consumption, production volume and price.

The tiny SHTC1 humidity and temperature sensor is specifically designed for mobile devices where size is a critical factor. Sensirion has rigorously followed the maxim "smaller is better" and developed the world's smallest sensor in its class, measuring a mere 2 x 2 x 0.8mm. The sensor is based on the proven CMOSens Technology, which allows the sensor and the signal processing electronics to be combined on a single silicon chip to achieve small device size. Production is targeted at high volume to allow low unit prices to be achieved by economy of scale. The supply voltage of 1.8V is also fully in line with the needs of the target industry.

www.sensiron.com/shtc1
Hall A2, Stand 206

Impressively Fast and Reliable: Swissbit X-500 Series Industrial SATA II SSD

With the industrial SATA II SSD (solid state drive) of the X 500 Series, Swissbit AG is extending its successful industrial 2.5" SSD product line. This 2.5-inch storage solution achieves a data rate on SATA II of up to 260MB/sec and an impressive 15,000 IOPS with 4k random accesses. Added to this are features such as NCQ, TRIM, the ATA security set and in-field update.

To ensure the absolute reliability of the power fail protected X 500 Series, Swissbit combines sophisticated mechanisms and augments these with the S.M.A.R.T. (self-monitoring, analysis and reporting technology) protocol, the lifetime monitoring tool or SDK and an efficient BCH-ECC (error correction code) unit.

The X-500 Series is available in storage densities from 16GB to 512 GB as SLC (single level cell) and in MLC (multi level cell) versions.

www.swissbit.com
Hall A6, Stand 121

Panasonic Releases World's 1st SMT Thermopile Array Sensor

Panasonic Electric Works Europe AG released the first ever Surface Mount Technology (SMT) thermopile array sensor, the Grid-EYE. Years of continuous research in infrared sensing technology led to the development of a state-of-the-art thermopile sensor that features 64 thermopile elements in an 8 x 8 grid format.

Contrary to conventional thermal sensors that only measure temperature of a certain point-of-contact, Grid-EYE, based on Panasonic's MEMS technology, can measure temperature of the entire specified area without any contact; in other words, it is a "contact-less thermopile array sensor". The 64 pixels yield accurate temperature measurement over a viewing angle of 60° provided by a silicon lens. Grid-EYE uses an I²C communication interface, enabling temperature measurements at speeds of 1 or 10 frames/sec. An interrupt function is also available.

www.panasonic-electric-works.co.uk
Hall B6, Stand 105

IQD Launches New Series Of Fast Programmable Oscillators With Class Leading Phase Jitter Performance

The short lead-times offered by programmable oscillators are typically offset by relatively poor performance in comparison to standard crystal oscillators, especially as regards phase noise and jitter. IQD's two new ranges of programmable oscillators offer the best of both worlds with phase jitter performance comparable to traditional crystal oscillators combined with lead-times as short as three days.

Both models, the IQXP-20 clock oscillator and the IQXP-30 voltage controlled oscillator, offer RMS phase jitter down to 0.4ps across all output types. A very wide frequency range from 10.0MHz up to 1.5GHz is available from along with HCMOS output capable of driving 15pF; LVPECL and LVDS outputs are also available at the higher frequencies.

Frequency stabilities down to ±10ppm and operating temperature ranges out to -40 to +85 degrees C are available.

www.iqdfrequencyproducts.com
Hall B5, Stand 314

Inductive Components For Industrial Applications

SMP Sintermetalle Prometheus GmbH & Co KG (SMP) introduces at this year's Electronica in Munich inductive components for industrial applications, such as frequency converters. The components are low-loss, have good EMC characteristics and allow a space-efficient design.

The inductive components are installed both at the frequency converter's input, where they provide power recovery, and at the converter's output, where they act as filter chokes. Because of their space-saving design and low-noise operation, SMP's chokes are also used in frequency converters' internal DC links, as both single and common-mode chokes.

The components' cores consist of powder composites with low magnetostriction, which SMP specifically engineers for each application. With their low eddy current and hysteresis losses, the materials contribute to the components' exceptional efficiency. Their encapsulated design ensures that the components emit only low-intensity stray fields.

www.smp.de
Hall B6, Stand 153

Amphenol's Latest EMI Filtered Terrapin Connector Launched At Electronica 2012

Amphenol will be launching its latest enhancements to the field proven Terrapin connector series at Electronica this year. This ruggedised series is now available with embedded EMI filter circuits and can be supplied with either standard or customised Pi, C or LC filters.

By embedding its latest planar filtering technology into the Terrapin connector, Amphenol enables systems engineers to reduce the overall size and weight of equipment whilst improving overall signal integrity. All of the high performance electrical and environmental features of the standard Terrapin connector have been retained, including a high level of IP68 sealing and EMC with only a minimal increase in the overall length of the product to accommodate the filtering components.

Filtered Terrapin connectors will be available with specific pre-determined filtering values at a reduced leadtime.

www.amphenol.co.uk
Hall B4, Stand 636

Seica SpA at Electronica

Once again Seica has great news this year for visitors at Electronica with a first ever showing of its complete COMPACT line of in-circuit and functional testers, including six different models. Like all of Seica's solutions, this line is based on the core software/hardware VIP platform, but is specialized for multiple applications, with specific reference to the automotive industry, and includes systems dedicated to in-circuit test, on-board programming of digital devices, functional and end-of-line board testing (EOL), with manual or fully automated UUT loading/downloading.

In addition, visitors will be able to view a wide range of application solutions on the different systems, including test fixtures and programs implemented in VIVA software and NI Labview/TestStand, which is 100% compatible with the COMPACT systems' hardware architecture. This is a unique opportunity for a closer look and a hands-on experience of Seica's capabilities.

www.seica.com
Hall A1, Booth 459

Binder Shows Wide Range Of Circular Connectors On Its Stand At Electronica

Binder UK will be joining forces with its parent company Franz Binder GmbH and will show a wide range of circular connectors on Stand 261 in Hall B3 at Electronica 2012 on 13th to 16th November.

Among the extensive display will be high-power versions of M12 connectors that can carry up to 8A on each contact. Until recently M12 connectors have been limited to 4A with a maximum cable diameter of 8mm and individual wire sizes of 0.75mm². This meant that designers had to specify larger circular or more cumbersome connectors such as mixed layout D types. The new high power Binder M12 connectors can carry 8A at 250V on the 4-pole versions while the 5-pole can carry 4 x 8A and 1 x 2A at 125V.

Also on show for the first time are new versions of the popular Binder 620 series of sub-miniature, snap-in IP67 connectors.

www.binderconnectors.com
Hall B3, Stand 261

Beta LAYOUT At Electronica 2012 In Munich, Germany

Beta LAYOUT is exhibiting at this year's Electronica event, where the firm will also unveil its newest innovation 'Magic PCB'.

Beta LAYOUT has developed a groundbreaking application machine to embed RFID chips into a printed circuit board. The chips are embedded during the initial production steps, allowing for identification and traceability from the onset. RFID chips have a high reading accuracy with the added advantage of an invisible copy protection. The RFID chips function within the UHF frequency bands (860MHz to 960MHz) and can be operated globally.

The second highlight at the Beta LAYOUT booth is the new online IDF-to-3D tool (IDF = Intermediate Data Format). Using any printed circuit board software that outputs IDF data this tool allows design engineers to create a 3D data model of their assembled printed circuit board.

www.beta-layout.com
Hall C1, Stand 305

Pickering Interfaces at Electronica 2012, Hall A1.530

Pickering Interfaces has continued in 2012 to regularly release a steady flow of new products in both the LXI and PXI platforms. At electronica 2012 it will showcase the following new products: 40-727/728/729 expandable RF matrices, 40-884 4x4 6GHz RF matrix, 40-611 multiplexer, 40-738 USB hub and 40-567 BRIC matrix.

Building on the success of Pickering's unique 40-726A RF matrix, the 40-727/728/729 new modules now allow Pickering to provide a family of expandable RF matrices for a broad range of RF applications.

40-884 4x4 6GHz RF is the first 4x4 RF solid state matrix available in PXI. This product is an addition to its continually expanding family of 40-88X solid state switching solutions.

The 40-611 multiplexer is an enhancement of the PXI multiplexer offerings with the highest density 2A multiplexers in PXI, featuring very low channel cost.

www.pickeringtest.com
Hall B6, Stand 105

Mercury Electronics Europe To Show New Low EMI Clock Oscillators At Electronica 2012

Mercury Electronics Europe is exhibiting at Electronica 2012 and is launching new low EMI clock oscillators in a small footprint 5 x 3mm package.

Exhibiting on booth 528 in hall B5, Mercury Europe offers a very broad range of crystal products manufactured in the company's state-of-the-art facility in Taiwan. The range includes clocks, VCXOs, TCXOs and OCXOs. The TCXO range includes low current versions and LVDS/PECL output formats.

The latest addition to the Mercury Electronics low EMI range of clock oscillators pioneered in Taiwan is the smaller footprint 5 x 3mm 3HM53R version. These oscillators are used extensively in aircraft seatback audio systems and medical equipment where EMI approval testing is an essential part of the qualification requirements.

An improvement of more than 12dBc EMI emission is possible with these oscillators.

www.mecxtal-europe.com
Hall B5, Stand 528

New Enclosures and Interconnection Products At Electronica

CamdenBoss is launching a number of new products across its enclosure, interconnection and industrial control ranges at the forthcoming Electronica 2012 exhibition, November 13 to 16, Messe Munich, Germany.

Among the new enclosures to be launched are the 71 and 72 series flanged IP66 cases, which offer large, robust enclosures with IP66 sealing gasket ideal for outdoor applications (71 series) and wall-mounted IP66-rated cases (72 series).

There is also a new range of UL94-V0 small potting enclosures – the 200 series. Manufactured in black or white ABS for high rigidity and impact strength, these new enclosures are ideal for encapsulating and protecting electronic components and feature a lid secured with four fixing screws.

CamdenBoss is also launching a new versatile modular DIN rail mounting enclosure that is designed to match instrument cases.

www.camdenboss.com
Hall A2, Stand 149

THIS IS A NEW MONTHLY COLUMN COVERING ISSUES RELATED TO TEST AND MEASUREMENT (T&M)

High-Speed DDR Memory Raises The Stakes On Memory Validation And Test

BY **REG WALLER**, EUROPEAN DIRECTOR, ASSET INTERTECH INC

In the not so distant past engineers didn't lose sleep over characterizing, validating and testing on-board memory. Today the stakes are much higher, as the speeds of memory technologies like DDR3 (Double Data Rate) and DDR4 have increased dramatically.

In a connected world, system throughput is almost everything. Moving large amounts of data in and out of systems requires more than raw processor speeds. As it happens, excessive memory errors can bring the fastest processor to its knees. Engineers are having problems with memory soldered onto circuit boards. Several recent surveys by the International Electronics Manufacturing Initiative (iNEMI) showed that memory test tops the list for engineers, as one of the most pressing problems they face.

Memory validation and test are a problem as they're becoming harder to do and, more importantly, memory errors can have a devastating effect on system performance, reliability, robustness and credibility. Google and the University of Toronto published the results of an extensive study about the incidence of memory errors, with data for the study being gathered from a portion of Google's vast installed base of high-performance servers. The study found that errors in memory were much higher than commonly expected. As a result, Google adopted a policy which states that one uncorrectable error in a DIMM (Dual In-line Memory Module) is sufficient to replace that DIMM. The challenge for system designers and manufacturers is to eliminate those memory errors before the system is installed.

> *The study found that errors in memory were much higher than commonly expected*

Sources of Memory Errors

Memory is vulnerable to many error-causing factors. For example, clock, data and address signals can be disrupted by jitter, noise, voltage aberrations, temperature and other environmental conditions. During manufacturing, variations in resistance, capacitance, inductance and others parameters can cause the corruption of data stored in memory devices. In some cases these factors corrupt the signaling on buses connecting memory to the rest of the system.

Another contributing factor to memory errors is the very intolerant nature of high-speed memory technologies like DDR. Among the reasons DDR3 and DDR4 are so fast is that DDR signals carry clock and data on both the rising and falling edges. As a result, the DDR bus must be finely tuned by adjusting the parameters of the DDR data window to ensure data throughput is optimized. A window that is not perfectly aligned will slow performance and may introduce memory errors.

What Makes Memory So Difficult To Characterize And Test?

Hard and soft memory errors are not new, but dealing with them is, especially as engineers use old legacy external instruments, or test systems that rely on placing a probe on the circuit board or on a chip pin soldered to the board. The test pads that were formerly designed into boards for probe access are quickly disappearing, the victim of increased board densities and complex multilayer construction, high-speed buses that will not tolerate the capacitive coupling effects introduced by pads and probes, and other factors. And then there are the advanced chip-scale packages like ball grid arrays, which hide pins underneath the die.

Into The Breach With Non-Intrusive Embedded Instruments

Fortunately for designers, manufacturing test engineers and field service technicians, non-intrusive instruments and test tools are able to overcome the diminishing effectiveness of external, probe-based instruments like those oscilloscopes that designers have always used, as well as manufacturing testers such as in-circuit test (ICT) systems.

The non-intrusive software-based tools use instrumentation embedded in circuit boards and inside chips to apply patterns that verify the performance, test the electrical integrity and characterize the functionality of memory buses and cells. Figure 1 shows a block diagram of a generic memory built-in

self test (MBIST) instrument.

Some of the technologies employed in non-intrusive board test (NBT) applications include boundary scan, processor-controlled test (PCT), FPGA-controlled test (FCT), functional test and others.

Having several non-intrusive tools for memory test adds to the effectiveness of the toolset since each phase in a product's life cycle has different objectives and requirements for its memory test. For example, designers during board bring-up have a particular set of concerns when they're validating and characterizing the memory architecture on a prototype board. Manufacturing test engineers deal with different constraints like the 'beat rate' of a production line. And when a system is installed in the field, the service organization probably will require a different set of capabilities to support troubleshooting and repair operations.

Ultimately, a memory test toolset must be multifaceted so the right tool can be deployed at the right time. Certainly these new non-intrusive software-based tools for memory validation and test will help engineers sleep the night through once again. ●

In the next issue, we will cover processor-controlled test (PCT), which accelerates prototype board bring-up by performing non-intrusive functional test on memory before the operating firmware is available.

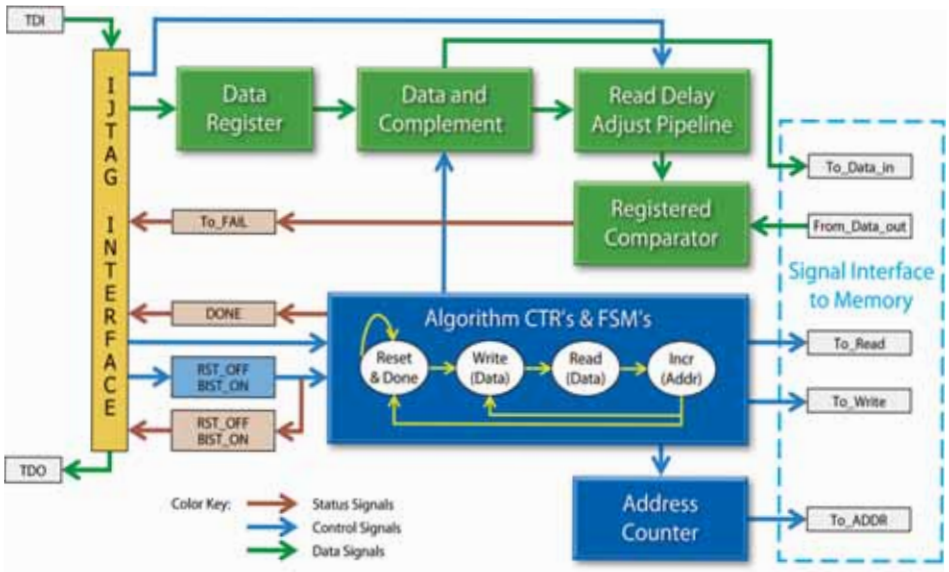


Figure 1: Block diagram of a generic memory built-in self test (MBIST) instrument

Data Acquisition System Design: Power Management and Timing System

IN THIS SERIES, **MAURIZIO DI PAOLO EMILIO**, TELECOMMUNICATIONS ENGINEER, SOFTWARE DEVELOPER AND DESIGNER OF ELECTRONIC SYSTEMS, PRESENTS A TUTORIAL ON DATA ACQUISITION SYSTEM DESIGN

PC power management for computer systems and data acquisition systems is desirable for many reasons, in particular to:

- Reduce overall energy consumption;
- Prolong battery life for portable and embedded systems;
- Reduce cooling requirements;
- Reduce noise;
- Reduce operating costs for energy and cooling.

Portable systems require long battery life while still delivering high performance. Dynamic power management (DPM) policies trade off performance for power consumption at the system level in portable devices. It is a design methodology aimed at controlling performance and power levels of digital circuits and systems, with the goal of extending the autonomous operation time of battery-powered systems, providing graceful performance degradation when power supply is limited, and adapting power dissipation to satisfy environmental constraints.

> *Since the dynamic energy consumed by an application is the product of the CPU power and time spent running an application, running a program with reduced voltage and frequency leads to significant energy savings*

Recent advances in processor design techniques have led to the development of systems that support very dynamic power management strategies based on dynamic voltage and frequency scaling. Since CPU power consumption typically decreases with the cube of voltage, while frequencies scale linearly with voltage, significant opportunities exist for tuning the power-performance tradeoff for the needs of the application.

Lower power consumption also means lower heat dissipation, which increases system stability, and it also means lower energy use, which saves money and reduces the impact on the environment.

Microprocessors' power management can be done over the whole processor, or in specific areas. With dynamic voltage and dynamic frequency scaling, the CPU core voltage, clock rate, or both, can be altered to decrease power consumption at the price of potentially lower performance. This is sometimes done in real time to optimize the power-performance tradeoff.

Low-power design is a critical consideration, even in high-end computer systems, where expensive cooling and packaging costs and lower reliability often associated with high levels of on-chip power dissipation are important concerns.

Dynamic voltage and frequency scaling techniques have proven to be highly effective in achieving low power consumption while meeting the performance requirements. Dynamic frequency scaling (also known as CPU throttling) is a technique in computer architecture whereby the frequency of a microprocessor can be automatically adjusted "on the fly", either to conserve power or to reduce the amount of heat generated by the chip. Dynamic voltage scaling is a power management technique where the voltage used in a component is increased or decreased, depending on the circumstances. Dynamic voltage scaling to increase the voltage is known as overvolting.

Power Management Using Dynamic Voltage Scaling

An efficient power saving technique for processors dynamically changes the CPU supply voltage depending on the workload of the current. This technique is called dynamic voltage scaling (DVS). Reducing the voltage in CMOS circuits reduces the processor's power consumption quadratically. Since processor clock frequency is dependent on supply voltage, reducing the voltage makes a program run slower.

However, this slowdown is linear with the supply voltage. Since the dynamic energy consumed by an application is the product of the CPU power and time spent running an application, running a program with reduced voltage and frequency leads to significant energy savings. DVS techniques can be classified into schemes that use information about tasks'

deadlines and schemes that maintain an acceptable performance degradation to achieve significant energy savings.

Timing and Synchronization For Designing DAQ Systems

Timing and synchronization are required when designing a data acquisition system. The timing system may need to coordinate tasks between instruments, or instruments may need to communicate directly with each other in a way that requires hardware synchronization. Examples of common timing and synchronization tasks include handshaking between a DMM and switch, phase-lock-looping a waveform generator with a digitizer, or synchronizing an RF down-converter with an IF digitizer.

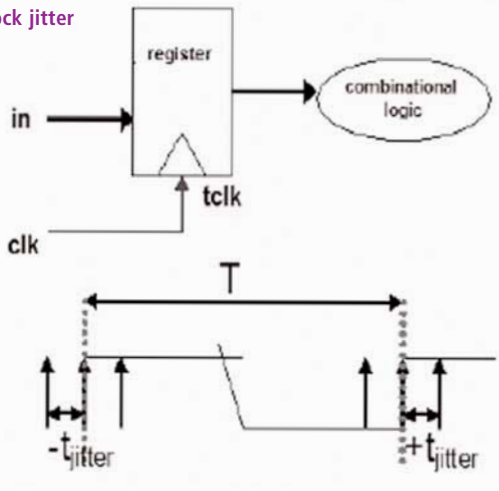
Most digital circuits designed and fabricated today are synchronous. In essence, they are based on two fundamental assumptions that greatly simplify their design: all signals are binary, and all components share a common and discrete notion of time, as defined by a clock signal distributed throughout the circuit. The advantages of asynchronous circuits are:

- Low power consumption;
- High operating speed;
- Better modularity;
- Robustness to variations in supply voltage, temperature and fabrication process parameters.

CLOCK SKEW

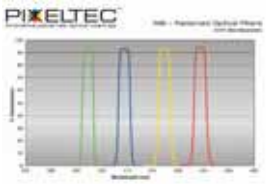
THE SPATIAL VARIATION IN ARRIVAL TIME OF A CLOCK TRANSITION IS KNOWN AS CLOCK SKEW. The clock skew between two points t_j and t_k is given by $t_j t_k$, where t_j and t_k are the rising edge of the clock with respect to the reference. Clock skew is constant from cycle to cycle and does not cause clock period variation, but only phase shift (see below). Clock jitter refers to the temporal variation of the clock period, that is: the clock period can expand or shrink on a cycle-by-cycle basis.

Clock jitter



Patterned Optics Available with High-Precision Bandpass Filters

Ocean Thin Films now provides its patented PixelTec patterned optical coating process for high-precision bandpass filters, opening up new possibilities for application-specific cameras. The extended capability enables optical devices to be micro-patterned with multiple narrow-band filters, creating even greater contrast and resolution for multispectral applications from cellular microscopy to factory vision systems.



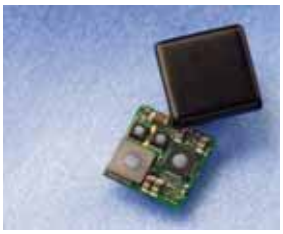
By combining state-of-the art sputtered coating expertise with exclusive microlithography technology, PixelTec delivers highly accurate geometric and spectral performance across the ultraviolet (UV), visible and near – short wave infrared ranges (NIR – SWIR). The pioneer in lithographic patterning of optical coatings, Ocean Thin Films continues to advance this technology – with more than 2 million precision patterned optics delivered. PixelTec optical coatings are increasingly used for purpose-fit performance in a multitude of medical, defence and industrial applications, enabling more compact, robust and cost-effective devices.

www.oceanthinfilms.com

LIQUI-FORM 2000 OFFERS HIGH THERMAL CONDUCTIVITY

Bergquist introduced the Liqui-Form 2000, its first product in a new 'Liqui-Form' product line. Liqui-Form 2000 is a highly conformable shear-thinning material which requires no curing, mixing or refrigeration; the product's formulation delivers excellent thermal performance, low applied stress and a reliable long-term performance for the most demanding applications.

Liqui-Form 2000 is thixotropic and has a natural tack to ensure it forms around the components and stays in place in the application. Unlike traditional pre-cured gap filling materials, a liquid approach offers infinite thickness options. It also eliminates the need for specific pad thicknesses or die-cut shapes for individual applications. Precise amounts of Liqui-Form 2000 can be applied directly to the target surface, resulting in less waste and a more effective use of the material.



During extensive laboratory testing, Liqui-Form 2000 provided consistent and reliable thermal performance. This gap filling material is ideal for fragile assemblies or for filling intricate air gaps between electrical components.

www.bergquistcompany.com

NEW, EXTENDED VERSATILITY VARIANTS OF CONNECTORS

Harting has introduced a number of new variants in its har-flex robust circuit-board connector family which extend its versatility in a wide range of board-to-board and board-to-cable applications with a contact pitch of 1.27mm.

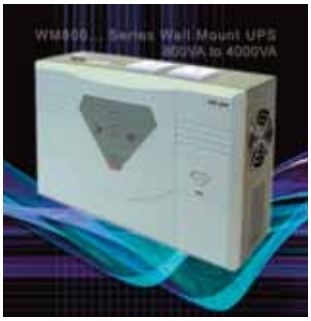
Featuring a compact but robust design, har-flex ensures reliable operation at all times – even under adverse conditions – through two large holders that ensure that the connectors are firmly held in place using surface-mount joints.

A low-wear insertion and withdrawal procedure is ensured by a very smooth contact point between the male and female contacts. This is the result of a special follow-up treatment in the punching process which Harting has developed from its extensive experience with punching technology. This characteristic also has a positive impact on vibration resistance, which has been verified according to recognised test standards.
The har-flex IDC connector for flat ribbon cable also meets the most exacting requirements in terms of robustness.

www.harting.co.uk

WALL-MOUNT UPS UNITS FROM POWERSOLVE

The WM Series of uninterruptible power supplies announced by Powersolve are wall-mount units designed to provide back-up power for long periods. Rated from 800VA/600W to 4000VA/3000W, the WM Series accepts a very wide AC input range while providing a pure sine wave output for up to several hours or more.



These are line interactive UPS systems with a 3ms transfer time. They are both generator compatible and cold start capable and feature adjustable voltage transfer points and charging voltage.

WM Series units combine high power chargers with smart battery management enabling them to charge high capacity external lead acid batteries (up to 500AH) for longer hold-up times. The units provide adjustable charging currents for different batteries as well as intelligent, two-stage charge control. Powersolve can also provide units with an optional solar charger input.

The WM Series accepts a wide AC input voltage range of 140 to 310VAC for 230V models and 70 to 155VAC for the 115V version.

www.powersolve.com

New Product from Peak Electronic Design Limited

Peak Electronic Design Limited is launching its latest product in December 2012 – the DCA Pro. This is an advanced new design that features a graphics display, USB communications, PC software and an enhanced component identification library.

The DCA Pro supports all the components that the popular Peak Atlas DCA55 supports, but with additional ones added to the list, such as transistors (including Darlingtons); silicon and germanium types; MOSFETs, enhancement mode and depletion mode types; JFETs, including normally off SiC types; IGBTs (insulated gate bipolar transistors); diodes and diode networks; LEDs and bicolour LEDs (2 lead and 3 lead types); zener diodes with measurement of zener voltage up to 12V; and voltage regulators (measures regulation voltage, drop-out voltage, quiescent current).

The instrument can be used standalone or connected to a PC; the DCA Pro automatically identifies the component type and pinout, and it measures a range of component parameters.

www.peakelec.co.uk

CML MICROCIRCUITS RELEASES CREDIT CARD SIZE SDR DEMONSTRATOR

CML Microcircuits has released a small demonstration platform for a complete Software Defined Radio (SDR) for wireless data applications.

The DE9941 is a credit card sized demonstration board for a complete linear modulation-based Software Defined Radio (SDR) for wireless data. It is designed to be small and low cost with minimal components/values. The small form-factor is made possible by the high integration of key functions provided by CML's market-leading devices.

There is a growing market requirement for small, flexible Software Defined Radio (SDR) data modems. The technology to accomplish this is now available with the releases of CML's highly integrated RF and Baseband product offerings: the CMX998, CMX994 and CMX7164.

The CMX998 is a market-leading Cartesian Loop Transmitter IC providing optimum PA linearisation for non-constant envelope/linear systems. The CMX994 is the ultimate Direct Conversion Receiver, providing direct conversion from RF down to I/Q baseband.

www.cmlmicro.com

NEW 8-CHANNEL MIXED-SIGNAL OSCILLOSCOPE FROM YOKOGAWA

The new Yokogawa DLM4000 mixed-signal oscilloscope features eight channels. Combining the large screen and 8-channel capability of Yokogawa's earlier 8-channel DL7480 oscilloscope with the mixed-signal technology of the company's pioneering DLM2000 Series, the new instrument is ideally suited to test and debugging applications in the embedded systems, power electronics, mechatronics and automotive sectors.

The DLM4000 Series comprises two models, with bandwidths of 350MHz and 500MHz and a sampling rate of 1.25GS/s, expandable to 2.5GS/s with interleaving. The channels can be allocated as eight analogue channels or seven analogue channels plus one 8-bit digital input. A future option will add 16 more channels of logic to allow seven channels of analogue plus a 24-bit digital input.

The new instruments feature exceptionally long memory (up to 62.5M points per channel and 125M points in interleave mode), allowing both long recordings and multiple waveforms to be acquired.

www.tmi.yokogawa.com

New Quad N And P Channel MOSFETS

Advanced Power Electronics Corp announced new quad complementary N- and P-channel enhanced-mode MOSFETs that target full bridge applications such as servo and DC motors. Simple to drive and with a low on-resistance, the AP9930GM-HF-3 devices are available in a standard SO-8 package commonly used in surface mount industrial designs.

N-channel performance ratings include: Drain Source Voltage (VDS) of 30V; RDS(ON) of 33mΩ; and Continuous Drain Current (ID) of 5.5A. For the P-channel, VDS is -30V, RDS(ON) is 55mΩ and ID is -4.1A. The package is halogen-free and compliant with both current RoHS and REACH environmental requirements for hazardous materials.

"These new quad MOSFETs provide designers with the best possible combination of fast switching, low on-resistance and cost effectiveness," said Ralph Waggitt, President/CEO, Advanced Power Electronics Corp.

www.a-powerusa.com

NEW FLAME RETARDANT EMC SHIELDING GASKET FROM KEMTRON

Kemtron, the British manufacturer of RFI/EMI shielding gaskets, materials and components has launched a flame retardant, low smoke, low toxicity EMC shielding gasket which is tested and approved to the international standard UL94V-0 by Underwriters Laboratories for flame retardancy, file number E344902. Also tested for smoke density to BS 6853:1999: Annex D.8.3 and oxygen index to BS EN ISO 4589-2:1999, confirming the material meets the requirements for minor internal use on vehicles category 1a, such as gaskets for electronic enclosures, is making it highly suitable for applications in underground transportation, trains and other safety critical applications.

The material is nickel-coated graphite loaded into silicone elastomers, product code SNG-FR. This allows the gasket to provide a highly electrically-conductive path between mating flanges of an electronics equipment enclosure giving a high level of RFI/EMI shielding. The material can be supplied as an extruded strip in various profiles, "O" rings or flat die cut gaskets.

www.kemtron.co.uk

MAXIM ANNOUNCES FIVE NEW PRODUCTS

Maxim Integrated Products introduced five high-integration products for factory automation and automotive markets that dramatically improve operating efficiencies and reduce costs. Maxim also announced it has collaborated with two firms to produce a reference design for a highly integrated telehealth fitness ("Fit") shirt that monitors vital signs, lowers the cost of medical diagnosis, and represents a new era in preventive medical care that could reduce health care costs manifold.

The two products targeted at factory automation are the MAX78638 turnkey solution for 3-phase motor energy measurement and diagnostics and the MAX31865, the industry's first fully integrated RTD-to-digital converter in a single-chip package.

Among the Maxim three automotive products are MAX17823 – fourth-generation high-voltage battery sensor; MAX17823, for battery longevity and fuel cell reliability; and the MAX17830, a second-generation, high-voltage battery-management solution.

All these products will be on display at Maxim's booth at electronica 2012 hall A6 at booth 163.

www.maximintegrated.com

Full-Bridge Low-Voltage DC Motor Driver IC

The A3918 from Allegro MicroSystems Europe is a new full-bridge DC motor driver IC capable of a continuous output current of 1A and operating voltages from 2.5 to 9V. An internal PWM current reference allows the user to select the peak chop current using only a resistor.

The new device is the latest addition to Allegro's low-voltage family of motor drivers, providing a single full-bridge option to complement the dual full-bridge capability found in the company's existing family of devices. The single supply and simple logic interface makes this an ideal product for applications involving single-cell lithium-ion batteries.

The A3918 has a unique design which incorporates a two-stage charge pump that ensures that the driver has a low output resistance over the entire supply range from 9V down to 2.5V. This feature dramatically improves battery life when battery voltages are low because the switches do not become highly resistive due to reduced gate drive.

www.allegromicro.com

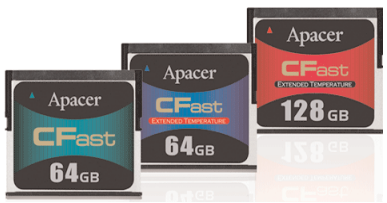
ULTRA-HIGH SPEED INDUSTRIAL CFAST CARDS

When it comes to the ever-evolving core technologies of embedded systems, data transmission efficiency and speed are the main targets for improvement. Apacer has introduced a new CFast memory card to support the SATA II 3Gb/s high-speed transmission mode. Apacer has now upgraded the capacity and speed of its industrial CFast memory cards. Additionally, these cards come in MLC solutions and support extended operating temperatures.

Apacer's latest industrial CFast card features a peak reading speed of 160MB/s, breaking the speed limits of the CF cards currently used by industrial enterprises. This speed is three times faster than typical industrial CF cards, dramatically promoting file transmission efficiency, making it one of the best storage solutions for high performance computing systems.

When it comes to the ever-evolving core technologies of embedded systems, data transmission efficiency and speed are the main targets for improvement.

www.apacer.com



HARWIN ADDS IDC TO POPULAR ARCHER CONNECTOR FAMILY

Harwin is expanding its popular high density 1.27mm pitch Archer M50 connector portfolio with the addition of four new product series and for the first time including IDC cable connectors plus associated cable assemblies.

Two ejector headers in both through-hole solder tail and surface mount options are available; surface mount devices are tape-and-reel packaged for fast, reliable, automated placement.

Additional IDC DIP transition-style connectors and IDC socket connectors complete the enhanced connector line-up. Designed to provide fast, reliable and cost-effective connection using fine pitch 0.635mm ribbon cable without the use of special dedicated tooling, IDC connectors are ideal for medium to high volume cable-to-board connection.

Complementing the range extensions, Harwin is also offering a number of different 150 and 300mm long off-the-shelf cable assemblies.

All connectors are available in 2x5, 2x10, 2x13, 2x17, 2x20 and 2x25 positions.

www.harwin.co.uk

AVX Capacitors Deliver Power To Laser Source On Mars

The ChemCam (chemistry and camera instrument) laser module on board of Mars rover 'Curiosity' – which successfully landed on Mars on 6th August 2012 – contains 630 tantalum multianode capacitors from AVX Corporation, a leading manufacturer of advanced passive components and interconnect solutions. The laser module is used to analyse chemical elements of rocks on Mars.

The design of the laser power source for the ChemCam had to meet extreme requirements and yet deliver high power performance in a small size and very light-weight package. So, AVX's designed a large bank of 630 tantalum multianode capacitors (470µF 10V), providing very low ESR, to be used in this application. The capacitors were produced in the ESA (European Space Agency)-approved manufacturing facility from AVX in Lanskroun, Czech Republic and then re-tested to MIL standards by AVX in Biddeford, Maine, the US.

www.avx.com

SEMTA ATTRACTS GRADUATES TO INDUSTRY

A five-day workshop to advance the business skills of the country's top electronic engineering students has been hailed a big success with the news that electronics degree uptake by British students has increased.

As leaders from the electronics industry's top companies came together for the second annual UK Electronic Skills Foundation (UKESF) event in Edinburgh, it was revealed that, since the inception of the Foundation, electronics degree uptake by British students has increased to 3300, up 23% on 2008.

This year's workshop included seminars on project management, business ethics and negotiation from several UK universities.

"We are delighted to be working alongside so many universities, leading industrialists and the students themselves to help prepare electronic engineering graduates for the workplace and encourage more young people to study in an area where demand for skills will remain high for many years to come," said Darren Race, Semta's UK sector manager for electronics.

UKESF was founded in 2010 by Semta, NMI, the Department for Business, Innovation and Skills (BIS) and industry partners to increase the number of talented electronics engineering graduates entering the industry. Its creation was in response to industry concerns, following a significant decline of some 47% between 2002 and 2008 in UK applicants for electrical and electronic engineering degrees, which threatens the performance and long-term prospects of the industry.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: UK used to be number one in electronic engineering in '70s when electrical and electronic engineering were the most sought-after courses after medicine. Unfortunately, there has been sharp a decline in student numbers selecting engineering subjects since the early 2000s. Thanks to UKESF and Semta we have seen an increase the student interest in electronic engineering and related fields. The investment seems to be in the right direction, with 160 new industry-funded undergraduate scholarships each year. With the current decline in industrial output and manufacturing, UK now needs electronic engineers more than ever.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Electronics is fundamental to many of the things we take for granted today. Everything from mobile phones to aircraft and medical equipment relies on electronics, and it is difficult to think of any area of life that has not been affected by developments in electronics.

Electronics engineers are involved in the design and development of technology that has become essential to all areas of the modern world. This makes the job of the electronics engineer both exciting and challenging, but it also means that there are great rewards for engineers, both in terms of remuneration and job satisfaction.

The workshop, organised by Semta, allows top electronic engineering graduates to meet and learn from industry bosses and so be better prepared for the workplace with the ability to enter the jobs market with more than academic skills. By organising different workshops UKESF will help the students overcome their lack of workplace experience and gain job skills with new knowledge such as team working, customer awareness and communication. A successful career depends on what you know as well as who you know. That's why I find this initiative very promising; by adding business and communication skills, the top electronic engineering students who are classmates today will be industrial leaders tomorrow.

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, INFN – Laboratori Nazionali del Gran Sasso, Italy: Investing in skills and training is a serious business, one that can directly impact on the success of a company. But to find a way through the multitude of courses and training available, finding out which one is best for you and ensuring that the investment pays off is a tough task.

Skills Investment Programs provide individuals with financial assistance to attend apprenticeship programs, attain basic skills and/or access skills training at approved public or private training providers.

Investing in people improves staff morale and retention, attracts the best people to an organization, and boosts productivity and performance.

> The workshop organised by SEMTA allows electronics engineering graduates to meet and learn from industry bosses and so be better prepared for the workplace with the ability to enter the jobs market with more than academic skills

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, Director of Datod Ltd, UK: The implication that the inception of the UKESF correlated with the uptake in electronics degrees is far fetched. However, any effort which encourages careers in engineering is worth supporting and, especially this programme with its leading UK business partners such as ARM, CSR, Dialog and Imagination, and UK engineering universities such as Edinburgh, Bristol, Cardiff, Imperial, Surrey, Southampton, York and Manchester.

However, it is unclear to me how they selected the 47 undergraduate candidates for this additional business skills initiative. In the US this is simply done on a mass scale through their major (engineering) and minor (business) degree structure.

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector register your interest with the Editor by writing to Svetlana.josifovska@stjohnpatrick.com

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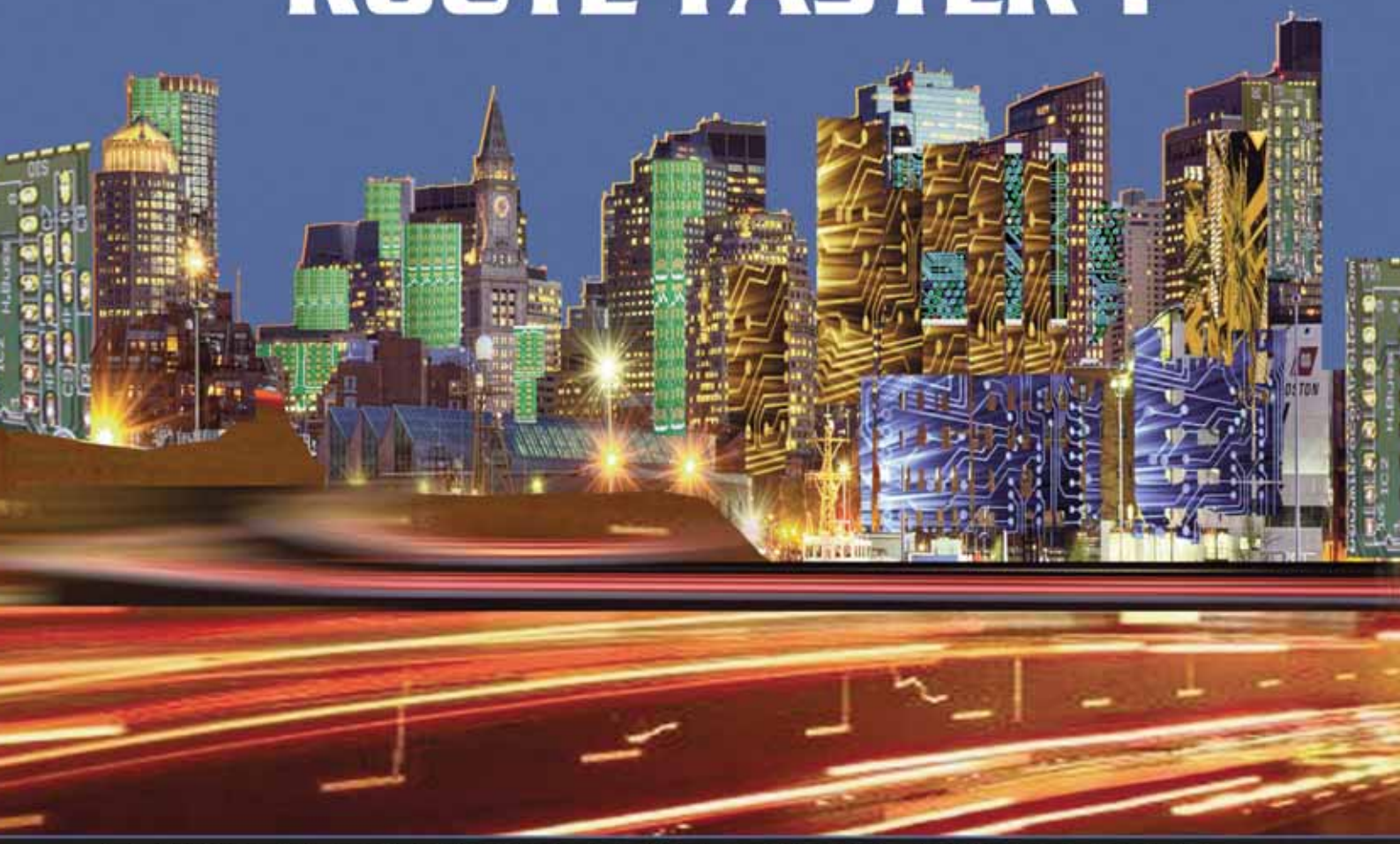

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