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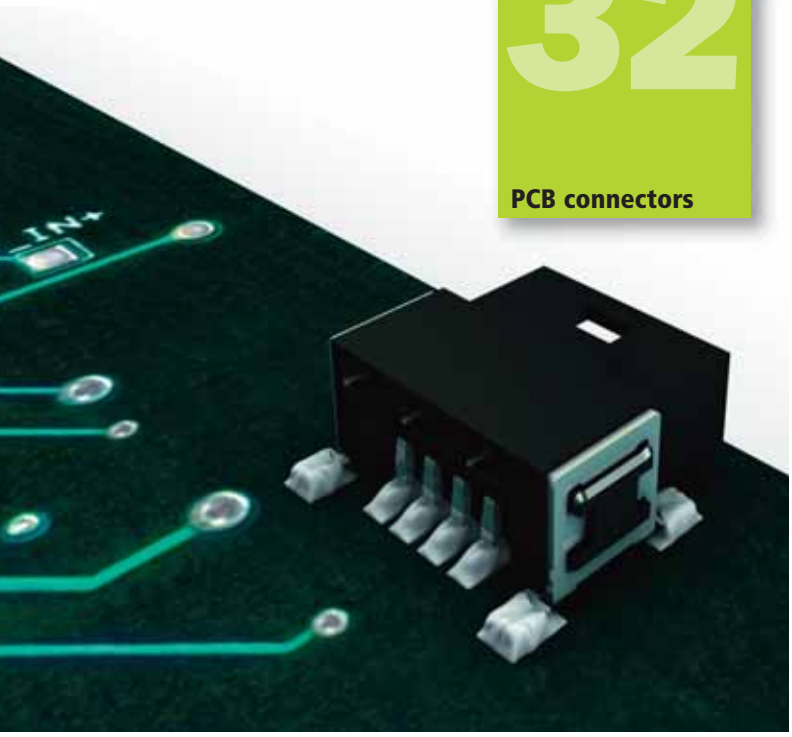

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TRENDS IN THE FPGA MARKET

The Programmable Logic Devices (PLD) market was worth $3.77bn in 2008 and shrank 12% in 2009 to $3.31bn. A recovery saw 2010 revenues grow to $4.72bn and then on to a record annual level of $4.97bn in 2011. The second quarter of 2011 was a record at $1.33bn. Since then the sector has been in decline, with the last quarter of 2012 expected to it make six straight quarters of lacklustre performance.

Taking the mid-point of the quarterly earnings projections from the PLD vendors yields a figure of $1.12bn for the quarter and an annual total of $4.58bn. This would result in a 7.8% decline in 2012.

The industry is suffering from the same effects of recession and global uncertainty seen in the wider economy. However, since FPGAs are taking a larger percentage of the total semiconductor market each year, and are primed to benefit disproportionately once a recovery gets under way.

Altera and Xilinx, the two leading FPGA vendors – and the only consistently profitable companies – have maintained a dominance of the industry for well over a decade. Together they account for over 80% of the market. Altera currently has the momentum, and has gained an average of two points of market share from Xilinx over each of the last three years. The remaining FPGA vendors have made no impact on the status quo.

The product portfolios of the two companies closely track the latest technology, with both currently rolling out multiple devices built on 28nm process technology. These products will increase the capacity and speed available, while also providing price reductions to end customers.

The established players were all founded over 20 years ago, including Lattice Semiconductor and QuickLogic. An early pioneer, Actel Corporation, was the first FPGA company to be acquired by Microsemi Corporation in late 2010.

The history of new entrants in the FPGA sector is chastening, with large and small companies failing or being acquired. In recent years, Tier Logic emerged from stealth with exciting technology in spring 2010, but closed in July having failed to secure adequate financing. SiliconBlue was well funded, but was acquired by Lattice in 2011.

There are two new market entrants with products: Achronix and Tabula. They are both attempting to penetrate the lucrative high-performance market, and each has a foundry arrangement with Intel to access its leading-edge 22nm process.

> ***The FPGA market has many barriers for new entrants; the main competitors are already shipping 28nm devices***

However, the market has many barriers for new entrants. The main competitors are already shipping 28nm devices and have broad support structures and Intellectual Property (IP) portfolios, as well as extensive suites of design software.

Xilinx is rolling out four product families on 28nm that are the design-win vehicles to supplant all its existing high-performance and low-cost products. The Xilinx positioning favours low power, with more modest performance increases. Both positions resonate within sectors of the market.

Xilinx has released a significantly larger device than anything previously available, with a logic capacity approaching the equivalent of 2 million 4-input logic elements. This device will be very attractive to customers for ASIC emulation, and is assembled from four dies using a silicon interposer to connect them together. It has used a similar technology to build a 28Gbps transceiver product.

The Zynq family is positioned as a 32-bit ARM processor chip with a programmable fabric that can be accessed by the ARM. Xilinx has introduced a mid-range family called Kintex that supplements the low-cost Artix and high performance Virtex devices. Kintex fills a gap that has been serviced for several years by the Altera Arria products.

The three 28nm families from Altera are faster and denser extensions of its previous devices, with more logic and memory. The company has introduced sub-families of its low-cost Cyclone devices that feature ARM processors, along with updated families of the Arria and high performance Stratix devices.

Altera and Xilinx have started to release early details of forthcoming 20nm products. The proposed Altera products, for example, have a strong emphasis on blistering performance, and will feature industry-leading 40 Gbps transceivers. It plans to sample 20nm products next year, with volume production in 2014. The target market for these products is clearly the emerging 100G and 400G networking.

Paul Dillien, Consultant at High Tech Marketing, prepared this piece based on the "The FPGA Market" report. Within the report, the pricing philosophies of the leading FPGA companies are analysed and illustrative examples of price structures are presented. www.high-tech-marketing.co.uk/FPGA

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THAI FIRM OFFERS PT10 HISTOGRAM EQUALIZATION IP CORE

Thailand-based engineering firm, SingMai Electronics, has developed a histogram equalization intellectual property core for standard definition (SD) and high definition (HD) video sources. Called PT10, the IP is suitable for implementation in both FPGAs and ASICs.

Histogram equalization is a useful technique for expanding the contrast range of low contrast images allowing previously invisible details to be seen. It is particularly helpful in the extreme lighting conditions encountered in security imaging, in scientific and industrial imaging and in any environment where lighting cannot be controlled. It may also be used to pre-condition images for further processing such as feature extraction.

PT10 calculates the histogram of the image intensities in real time and applies the correction to the next video frame, calculating the correction during the vertical blanking interval.

The PT10 is available now and SingMai offers a full design-in support. The company offers a range of FPGA development boards are targeted specifically at SD and HD video development, and include integrated IP cores to speed time to market. Altera and Xilinx FPGA platforms are provided plus a range of add-on boards including analogue inputs and outputs, CMOS camera sensor interfaces, QVGA LCD display and HDMI and SDI/HD-SDI interfaces.

***Top:** Camera image shows an interior with a brightly lit window which reduces the contrast range. On the left side is the original image; on the right is the image after it's been processed by the PT10 IP core*

***Bottom:** This image shows the histogram equalisation in operation. The view through the tunnel, which has a bright central exit forces the camera to reduce the contrast of the walls (left side of image). The PT10 adjusts the contrast range of the image in real time so the details of the walls are again visible (right side of image).This is particularly useful, for example, in pipe inspection or other remote inspection applications.*

New era for AUTOSAR as it moves to being a global standard

The AUTOSAR (AUTomotive Open System ARchitecture) development partnership has defined its goals for post-Phase III organization beginning in 2013. To guarantee a smooth transition from Phase III at the end of 2012, the partnership is continuing on a permanent basis with the focus on ensuring the stabilization of current releases as well as backward compatibility, the continuous incorporation of functional enhancements and the establishment of a flexible work package structure.

AUTOSAR maintains a maximum of two releases in parallel with a strong focus on stability, backward compatibility and long-term suitability to meet the future market requirements. A well defined life cycle for releases enhances existing AUTOSAR processes and ensures the stabilization of current releases.

"With releases 3.2 and 4.x, AUTOSAR provides stable releases for exploitation in current series developments. The further development of AUTOSAR will be driven by market needs," said Dr Stefan Schmerler, AUTOSAR spokesperson. "As the key software technology in the automotive industries worldwide, AUTOSAR will continue to sustainably meet the demands posed by OEMs' series application at any time. Also, the impact of AUTOSAR in Asia is increasing constantly."

By closing gaps in the existing functionality and encouraging the variety and potential consolidation of functionalities, AUTOSAR will ensure the stabilization of current releases and further improve the quality of specifications. The technical content for 2013 onwards will focus on ensuring interchangability of implementation via acceptance tests, establishing the possibility to generate configuration profiles and further enhancing the management of backward compatibility. The development partnership has published Release 3.2 Revision 2 at the end of June 2012 with the focus on maintenance and improved ease of use. This incorporates feedback from series development. With Release 4.1 Revision 1, planned for publication in March 2013, AUTOSAR will introduce 31 new concepts for enhanced functionality and maintainability, usability and compliance. All these concepts will be thoroughly validated before the release date. In addition, AUTOSAR will enhance support for new technologies like multi-core processors, Ethernet with TCP/IP communication mechanisms and others.

AUTOSAR – AUTomotive Open System ARchitecture

AUTOSAR is a worldwide development partnership of car manufacturers, suppliers and other companies from the electronics, semiconductor and software industry. Since 2003 they have been working on the development and introduction of open, standardized software architecture for the automotive industry. By simplifying the exchange and update options for software and hardware with the AUTOSAR approach, it forms the basis for reliably controlling the growing complexity of the electrical and electronic systems in motor vehicles. AUTOSAR also improves cost efficiency without compromising quality. The "core partners" of AUTOSAR are the BMW Group, Bosch, Continental, Daimler AG, Ford, General Motors, PSA Peugeot Citroën, Toyota and the Volkswagen Group. In addition to these companies, more than 160 members play an important role in the success of the partnership. Companies which join the AUTOSAR Development Partnership can use the specifications free of charge.

Electronica

MYK DORMER IS A SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
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One of the minor perks of my job as an RF engineer is the occasional visit to a big industry show. Officially this is to talk to suppliers and find new parts (RF components being perceived as "too mysterious" for ordinary purchasing staff to source), although in truth it is more useful as a litmus test of the electronics industry in general, and a chance to get an overview of where things are going.

I have, therefore, been lucky enough to attend Electronica, the massive components and systems show held in Munich every other year. Beyond once again being awestruck by the sheer size of the event (using all but two of the airship-hangar-sized halls in Munich's huge exhibition centre), I observed a few interesting details this year:

Overall confidence in the industry feels like it is improving. The previous event (2010) had disappointingly few new products and an overall feeling of uncertainty. This year saw none of that. There were many suppliers offering new products, many companies were exhibiting for the first time and sales budgets were visibly up (see Box right).

Asian suppliers, especially small to middle sized concerns, were far more in evidence, in a wide range of product areas. Large numbers of small booths were grouped in national pavilions – blocks of stands, assigned to Chinese, Korean or Taiwanese companies – which may have been partly funded by umbrella organisations or governmental agencies. One such pavilion was also provided by Russia.

Growth areas in evidence were definitely LED lighting (sunglasses would have been useful in one hall), connectors and power supplies. There seemed to be more middle-sized distributors – rather than the previous dominance by two or three big names, and even a handful of new non-specialist semiconductor suppliers. The show organisers were touting an emphasis on (green) energy storage, but this was little in evidence.

> *Overall confidence in the industry feels like it is improving. The previous event (2010) had disappointingly few new products and an overall feeling of uncertainty*

The representation of low power wireless remains modest: there was a small "wireless pavilion" in the centre of one hall and a few scattered "orphan" stands elsewhere. Not all the major players in the ISM sector were exhibiting, but there were some useful products on show. Noticeably more dedicated antenna suppliers were exhibiting, while the previous events' over-emphasis on "buzzword" protocols (such as Zigbee) seemed absent, with most suppliers offering a range of both proprietary and defined protocol products with little apparent preference. In RF component terms a widening range of single-chip radio products were evident, from both large and – more surprisingly – smaller vendors, while quartz suppliers were numerous, including a number of newer Asian names, previously only seen in Europe through distributors.

The next Electronica is not until 2014, but if you intend to visit, may I make a few suggestions: Swallow the cost and time taken and go for three or four days. It is too big to absorb in just a day or two. Wear good shoes, as the distance you will walk is considerable. Book early, as the hotel room prices climb to astronomical levels closer to the dates. And finally, plan to enjoy Munich. It is a major European cultural centre and well worth taking a few days holiday just to see it and its many attractions – both cultural and gastronomic. ●

INTERPRETING THE PEN GIVEAWAYS

YOU COULD EASILY CALL THIS 'MEASUREMENTS ON THE BIRO SCALE'. Andrea Bowes (my partner) has long maintained that there is a direct predictive correlation between the abundance of give-away pens (and similar small promotional gifts) and the future health of the sector. Comparing this year's healthy crop of such gifts from Electronica with that of the preceding three events suggests that she is almost certainly right.

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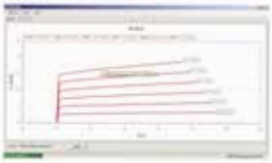
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RESISTIVE AND CAPACITIVE TOUCHSCREEN TECHNOLOGY: HOW DOES IT WORK?

DISCUSSED HERE ARE TWO OF THE MOST COMMON TOUCH TECHNOLOGIES: RESISTIVE TOUCH SENSING AND CAPACITIVE TOUCH SENSING. BY **DAVID ASKEW** OF MOUSER ELECTRONICS

The booming touch sensing market is fuelled in part by continued innovation, and has created a diverse range of touch technologies, including resistive touchscreens implemented in many cost-effective designs, projected mutual capacitive methods used in smartphones, and optical and piezoelectric based devices used in creating very large scale touch displays. But how do they work and why are they used?

Although the capacitive touchscreen market can claim the highest growth rates, resistive touchscreens are widely available and remain in common use. Resistive touch technology is relatively simple and can enable higher resolution at a lower cost when compared with capacitive touchscreens.

Resistive touch sensing is different from other touch methods in that the sensor is mechanically actuated: there are two conductive layers separated by an air gap (see Figure 1), and a pressing force is required to bend the top layer into contact with the bottom. This can be a problem or a benefit, depending on the application. The touch sensor is easy to interface and can be activated with a broad range of objects such as a stylus, pencil eraser, fingernail, or even a gloved finger.

However, the need for a flexible top layer means that the screen is subject to mechanical wear and, although not affected by dust or water, it is more susceptible to scratches and damage from sharp objects. Typical resistive touchscreens also rate the poorest in optical quality, transmitting only about 80% of light. Yet the affordability, simplicity and versatility of resistive touchscreens often make the technology an attractive option for many designs.

How Do Resistive Touchscreens Work?

The two conductive layers of a resistive touchscreen must be transparent, and so they are usually composed of indium tin oxide (ITO). The bottom layer is deposited on glass substrate and is separated from the top ITO layer by transparent spacer dots. The surface of the screen is coated with a flexible layer of protective insulation which will often feature scratch resistance and anti-glare properties.

There are several methods for determining touch location from a resistive screen. The simplest uses only four wires: two connected to the left and right sides of the bottom conductor, and two connected to the top and bottom of the other conductor. A voltage gradient is applied across one of the uniformly resistive ITO layers (e.g. the bottom layer) and when contact is made with the top layer the resulting circuit resembles a voltage divider. The voltage is probed at the top layer to determine the x coordinate of the touch location. This process is repeated for the y axis by applying a potential across the top conductor and measuring the bottom layer voltage.

Resistive 4-wire touchscreens and corresponding controllers are ubiquitous and low cost. However, because this technology uses the flexible layer for measurement, wear and tear on the top ITO sheet can change the resistance characteristics of the conductor, resulting in a potentially significant decline in accuracy. For larger screens, this drawback as well as sensor drift become more apparent. The 4-wire method is therefore most preferable for smaller touchscreens.

The 5-wire resistive touchscreen is an attempt to resolve the issue of using a flexible upper layer for measurements. This technology implements both the "left-right" and "top-bottom" wires of the 4-wire scheme as electrodes attached instead to the four corners of the stable bottom layer, with the fifth wire functioning only

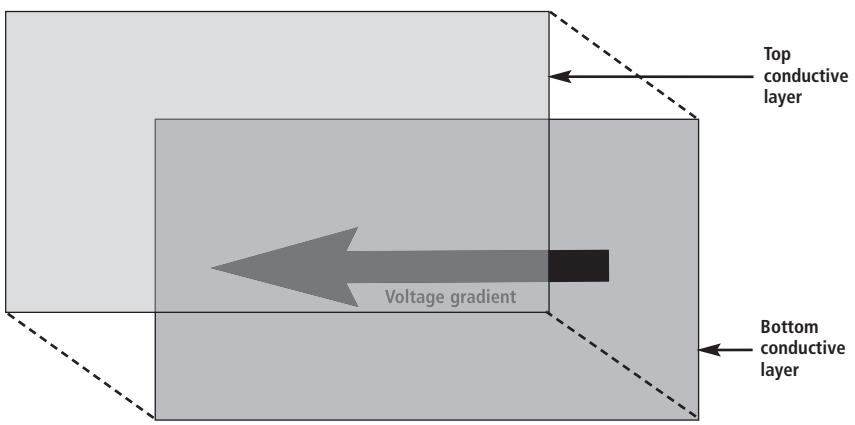


Figure 1: Resistive touch sensing has two conductive layers separated by an air gap

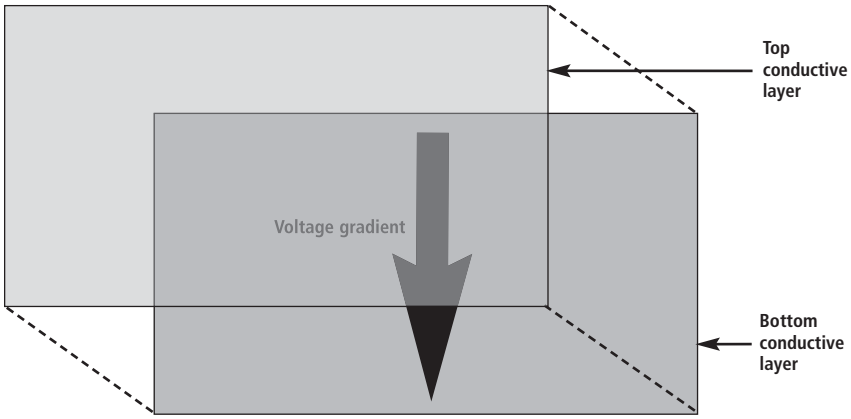


Figure 2: In surface capacitive touch technology the substrate is coated with only a single, uniform conductive layer

as a top layer voltage probe. The bottom layer is therefore used for both X and Y-axis measurements, increasing the overall durability and accuracy of the touchscreen.

Surface Capacitive Touch Sensing

In comparison, capacitive touch technology can offer superior optical qualities. Also, a flexible layer is not required, so capacitive screens can be made highly durable and environmentally resistant. Surface capacitive touch technology differs from projected capacitive technology in that the substrate is coated with only a single, uniform conductive layer, see Figure 2. The conductor is protected by additional layers of insulative material, but thickness is limited due to trade-off with touch sensitivity. There are many different sensing methods used in the industry but all are based on the principle of measuring the resulting increase in capacitance when a finger or conductive stylus is brought near the conductive layer.

Capacitive sensing buttons and sliders may not need to be transparent, so a potentially broad selection of materials can be used for the conductive layer (e.g. typical PCB copper). Also, a wide variety of sensing techniques are possible. For example, changes in capacitance can be detected by applying a time-varying voltage to the conductive layer and measuring the change in RC behaviour of the circuit.

Charge transfer methods are another option; the increased sensor capacitance from a finger touch results in a greater transfer of electrical charge to a reference capacitor, which is measured as the potential across it. While touch buttons are made from a single conductive pad, sliders are usually implemented as a series arrangement of multiple pads.

Surface capacitive designs for a touchscreen are a bit more constrained. ITO or similar transparent conducting oxides are chosen for the conductive layer because sensor transparency is a common requirement. Electrodes are precisely arranged around the conductive layer to generate a uniform AC voltage throughout the sheet. When a finger or conductive stylus is placed at a point on the screen, the user becomes a capacitively-coupled path to ground. The resulting current draw is then measured, typically, from each corner of the conductive sheet and the values are used to calculate the XY coordinates of the touch location.

> In the smartphone industry, projected capacitive touchscreens are becoming increasingly more common due to a variety of advantages over other touch technologies

While surface capacitive designs offer better optical transmission than resistive screens and are not burdened by the greater complexity of projected capacitive screens, they can suffer from parasitic capacitive coupling and have, in general, the poorest resolution of the three. Surface capacitive touchscreens are well suited for applications such as kiosks and basic industrial controls.

Projected Capacitive Touch Sensing

Most projected capacitance touchscreen sensors consist of two transparent conductive layers, typically of ITO, separated by a thin insulator to form a grid pattern. Some of the newest and thinnest designs implement this in a single layer by sputtering the ITO grid on a single substrate.

In the smartphone industry, projected capacitive touchscreens are becoming increasingly more common due to a variety of advantages over other touch technologies such as long product life, high durability, superior optical qualities and true multi-touch sensing. The projected capacitive screen of a typical smartphone may have a couple hundred electrode intersections; however a much higher resolution can be achieved with special algorithms that interpolate the values of adjacent electrodes.

Projected capacitive touch technology can be further classified into either self-capacitive or mutual capacitive screens.

Self-Capacitive Screens

Self-capacitive screens sense touch by measuring the sum of parasitic capacitance (self-capacitance) and the capacitance added by a finger or conductive stylus. In terms of sophistication, this method is somewhere between resistive touchscreens and the more complex mutual capacitive type screens.

Electrodes are laid out in a 2-layer grid and measurements are taken not from an electrode intersection, but from a row and column electrode pair. This presents a problem for multi-touch functionality.

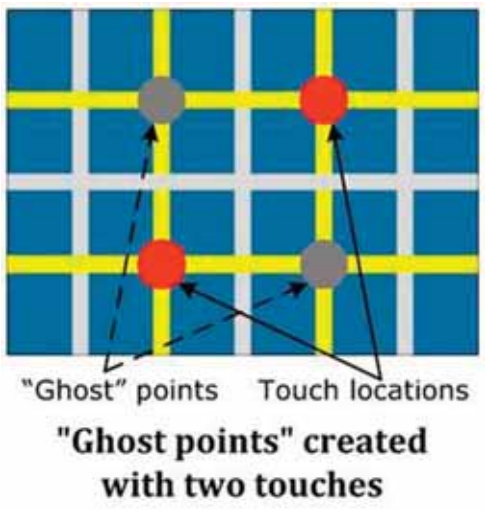


Figure 3: Potential false locations when the screen is touched at two diffferent places

When the screen is touched at two different locations, there are two sets of possible points that can be interpreted by the touch device (this forms a rectangle, with each pair on a diagonal), with no way for software to resolve which pair corresponds to the actual locations touched. The two false locations are called "ghost points", see Figure 3. Fortunately, many multi-touch gestures (such as a "pinch") are insensitive to this effect.

Although many newer designs, especially for smartphones, have moved toward mutual capacitive touchscreens, self-capacitive technology is still in use and continues to improve.

Mutual Capacitive Screens

Mutual projected capacitive sensors are a newer technology and measure the capacitance between electrodes (instead of electrode-to-ground). So, unlike self-capacitive touchscreens, measurements can be taken at each electrode intersection. The intersections are "scanned" individually, typically by driving a column-electrode and then quickly scanning every row-electrode that intersects it. This is advantageous because it means that the hardware structure supports unambiguous sensing of virtually unlimited simultaneous touches.

Mutual capacitance also allows for a greater range of sensor pattern designs, which can help maximize the signal-to-noise ratio (SNR). This is fortunate because measured capacitances can be in the femtofarad range, making LCD noise especially problematic. Still, mutual capacitive technology is gradually replacing its self-capacitance counterpart in many applications, being generally more robust and less optically obstructive.

Looking Forward

These are certainly not the only touch technologies in use today. Many others exist, each with their specific advantages. However, technology and innovation continue marching onward; capacitive touchscreens are being developed that work even while wearing gloves and the world may soon see projected capacitive displays with hover sensing functionality. Meanwhile, Mouser Electronics continues to be a leader in offering the latest products and tools for pressing ahead in this growing industry. ●

HAUL OR NOTHING FOR MOBILE OPERATORS

JIM SYME, PRODUCT LINE MANAGER AT COMMSCOPE, EXPLAINS WHY HIGH-QUALITY MICROWAVE BACKHAUL ANTENNAS CAN IMPROVE NETWORK CAPACITY AND SAVE MONEY IN THE LONG TERM

Rapidly increasing growth in data traffic across mobile infrastructure is stretching networks to their limit. One area of the network that is feeling the pinch is backhaul, which is taking the traffic from the cell site back to the network core.

Typically, three technologies can be used for backhaul: copper cabling, fibre cabling or microwave links. To date, microwave has been the technology of choice – providing an excellent combination of reliability, cost and rollout speed for network operators.

As operators look to expand and enhance their networks during the coming years, backhaul capacity will increasingly become a linchpin for performance. But choosing the right backhaul strategy is trickier than it first appears, and one that forces operators to tread a thin line between expenditure, technical performance and the needs of subscribers.

Front view of the CommScope Sentinel, the world's first commercially-viable ETSI Class 4 microwave antenna with improved radiation pattern

Back view of CommScope's Sentinel microwave antenna

Despite microwave's dominant position in the backhaul sector, it still faces many of the same technical challenges as the normal mobile network access, such as spectrum availability. Spectrum for backhaul is a finite resource that will be increasingly stressed as LTE and 4G networks are deployed.

The potential challenges for microwave backhaul include conflicts between increasingly congested networks, the limited availability of spectrum in the 6.0GHz to 42.0GHz frequency bands, the need for higher modulation schemes in radios to provide greater capacity and the ability of antennas to protect those radios from interference.

In the midst of all this, operators are also under mounting financial pressure to enhance and expand their networks, as the demand for LTE takes hold. Unfortunately, mobile operators are not seeing an increase in revenues from this additional data traffic – quite the opposite; these services are slicing into traditional revenues. A recent study from Ovum estimated that operators lost US$13.9bn in 2011 due to IP-based social messaging services on smartphones replacing traditional SMS use.

It is into this landscape of technical challenges and financial constraints that operators must step in search of the most effective backhaul solutions.

Technical Hurdles

While microwave backhaul is not the only solution operators can choose (both fibre and Ethernet provide valid alternatives), it can often be installed more quickly and at a lower cost, especially in environments with rugged terrain where laying miles of cable would be prohibitively expensive. For this reason, microwave backhaul is seeing increased popularity amongst operators worldwide.

Thanks to rising data traffic, operators are deploying an increasing number of both conventional macro and newer small-cell base station links. This in turn puts greater pressure on microwave backhaul throughput – that is the speed at which data from the wireless network can be fed back to the core network. As a result, more microwave backhaul links are being deployed in networks, resulting in a higher risk of signal interference in congested areas.

It is critical for operators to deploy high quality backhaul antennas that make the best use of the available spectrum and avoid interference as much as possible in order to obtain the best capacity and data throughput. For microwave to remain the best solution for backhaul the antennas should produce highly directional, point-to-point beams for minimal interference – an issue that designers and engineers have been keen to address.

Operators should also undertake careful network planning to ensure they are using the RF spectrum as efficiently as possible. Careful network design and planning is essential to ensuring the long-term, optimal performance of networks – especially since they will

need to be expanded in the future. Software, such as iQlink (a microwave link planning tool) currently exists that can model the expected performance of a backhaul network, providing analysis of interference threats. Over 300,000 network links have been planned and developed with iQlink since 1990.

> A recent study from Ovum estimated that operators lost US$13.9bn in 2011 due to IP-based social messaging services on smartphones replacing traditional SMS use

Financial Challenges

Given the challenges facing them, it's unfortunate – but not entirely surprising – that some operators have chosen to pursue the false economy of reducing capital expenditure (CapEx) on new infrastructure by purchasing lower quality microwave antennas.

These substandard products, often from emerging vendors abroad, have the knock-on effect of reducing network service quality in the long term. The worldwide manufacturing quality of antennas is currently under-regulated, which has led to 20-30% of antenna links not meeting specifications in some networks (Comsearch Research, "*A Study of the Impact of Antenna Selection on Real Microwave Networks, 2010*").

Due to this poor quality infrastructure, many operators also unwittingly fall below CE standards, which require that equipment legally meets EU health and safety regulations.

After five years of using these antennas, a backhaul network's performance will fall well below the efficiency levels it could have maintained with higher quality components. In the longer term, these components must be painstakingly identified and replaced, at a far higher cost to the operator.

Initial CapEx savings of this type are undoubtedly a false economy. Quite apart from the additional operating expenditure (OpEx) that substandard components cause in the long term, poor network performance is commonly cited as one of the greatest factors behind subscriber churn, which directly impacts operator revenue. In an increasingly competitive and crowded marketplace, maintaining an excellent service level is essential to retain customers.

Additionally, if operators pursue the lowest possible CapEx by patching their backhaul networks together through multiple manufacturers, it can become expensive or sometimes impossible to expand or upgrade the network.

Many low cost, low-quality manufacturers do not offer after-sales support and there are no guarantees that their systems will be compatible with those of other vendors. Operators must also take into consideration that lower quality backhaul antennas can become obsolete in the near future.

The Importance Of Network Investment

While operators should not compromise on quality in backhaul networks in a bid to reduce expenditure, long term savings can still be made by deploying robust, future-proofed technologies. Indeed, 70% of the total cost of ownership (TCO) of a microwave link comes after its initial purchase.

Higher quality antennas improve service quality and reduce the risk of subscriber churn. Additionally, they are less likely to fail, meaning that they require fewer maintenance site visits (a primary cause of OpEx in networks) to hunt down problems.

Throughout Europe, the planning of microwave networks has been driven by the various European Telecommunications Standards Institute (ETSI) radiation pattern masks. Antenna manufacturers' compliance to these masks ensures that when the network is properly designed, microwave links do not cause interference with nearby links operating on the same frequency band. Current standards specify Class 2, 3, and 4 with the latter providing the tightest performance.

Currently, most backhaul networks are planned with Class 3 antennas. Historically, this is because there is relatively small cost uplift between ETSI Class 2 and 3 antennas, providing a meaningful advantage in spectrum utilisation without driving up network roll-out expenses.

Class 4 antennas have been manufactured in the past, but usually at a high price versus performance ratio that rendered them uneconomical in all but a few exceptional circumstances. However, with increasing network congestion, the time has come to re-examine the potential performance trade-offs between Class 3 and Class 4

SPECIFIC SOLUTION FOR ADDRESSING CHALLENGES

COMMSCOPE'S OFFERS A MICROWAVE ANTENNA CALLED SENTINEL, WHICH IS DESIGNED TO ADDRESS THREE OF THE GREATEST CHALLENGES FACING WIRELESS NETWORK OPERATORS: RAPIDLY INCREASING DATA TRAFFIC, SPECTRUM SCARCITY AND RETURN ON NETWORK INVESTMENT. IT IS THE WORLD'S FIRST COMMERCIALLY VIABLE ETSI CLASS 4 MICROWAVE ANTENNA.

Sentinel is engineered to maximise the use of wireless spectrum, while withstanding heavy demands in data growth. An innovative improvement in radiation pattern helps squeeze more out of available spectrum and typically yields 40% higher link density. The result is more traffic moving between cell sites and the core network, helping reduce strain on the network and prevent impacts on performance. Sentinel can also minimise interference in the network.

The Sentinel microwave antennas have the most stringent Radiation Pattern Envelopes (RPEs) making them suited to achieving minimal signal degradation in the crowded airspace environments most operators face today. Their small size and light-weight profile makes installation easy and keeps maintenance costs low.

antennas. For a typical 23GHz, 0.6m (2ft) antenna nodal site, the ETSI Class 3 pattern masks would allow for around eight antennas to be deployed. Using Class 4 masks, this jumps to around 22 antennas. Therefore, it is clear that choosing the highest quality components is critical to reducing the cost of networks long term.

Class 4 antennas are robust enough to maintain optimal performance well into the future. For example, they can survive winds of up to 250km/h, something low-cost antennas cannot achieve. Due to their smaller profile they can be deployed more cheaply and require less expensive tower infrastructure. Bulkier antennas drive up operating expenses due to larger tower space leasing and zoning considerations, while each smaller profile antenna can provide an estimated annual savings of $2,500 on leasing costs. Installations or larger antennas are typically more complex and with greater maintenance requirements, which can increase the likelihood of longer network downtime.

Alongside this, effective network planning prior to construction, as well as optimisation during the network build stage can significantly reduce both network CapEx and OpEx, without compromising network performance or service quality.

At the network build stage, costs can also be greatly reduced by choosing one vendor. This is especially true over the long term, when the cost of resolving future network problems is factored in. Choosing single vendor, pre-integrated solutions also means that the operator can be "de-skilled", i.e. the solutions can be installed by less specialised personnel. This is a benefit, since qualified RF engineers are in high demand in the industry, making their time very costly.

> Class 4 antennas have been manufactured in the past, but usually at a high price versus performance ratio that rendered them uneconomical in all but a few exceptional circumstances

The Long Haul

The skyward trend of data traffic shows no signs of slowing, with the UMTS Forum recently predicting that voice and data traffic on mobile networks will grow more than 30-fold during the coming decade.

Clearly, many operators face tough choices in the years ahead. The decision to invest in higher quality infrastructure cannot be taken lightly in the current climate. However, it's also clear that operators should avoid a knee-jerk reaction by lowering CapEx at any cost, or they may find that the choices of today become the problems of tomorrow. ●

USB POWER INTERFACE PROTECTION SOLUTIONS FOR MOBILE DEVICES

THE MOBILE INDUSTRY NEEDS TO CONSIDER HOW TO BETTER PROTECT USB POWER INTERFACES IN VARIOUS MOBILE DEVICES. **ROGER LUO** OF FAIRCHILD SEMICONDUCTOR DISCUSSES EXISTING PROTECTION SOLUTIONS AND PROPOSES NEW ONES

With the vigorous development of 3G mobile communication technology and the rapid adoption of personal mobile devices, USB interfaces have become the major data and power interfaces of smart phones and 3G wireless data cards. This has been a great help for device compatibility and resource conservation. Over the years, in addition to promoting the standardization of interfaces, the mobile industry has needed to consider how to provide better protection to the interoperability between mobile products of different manufacturers, USB cables and power adapters with USB interfaces.

Commonly Used USB Power Interface Protection Circuits

Due to cost considerations and existing chip portfolios being incomplete, most wireless data cards are currently equipped with only simple soft-start circuits (Figure 1) to reduce the risk caused by inrush current and to protect the system.

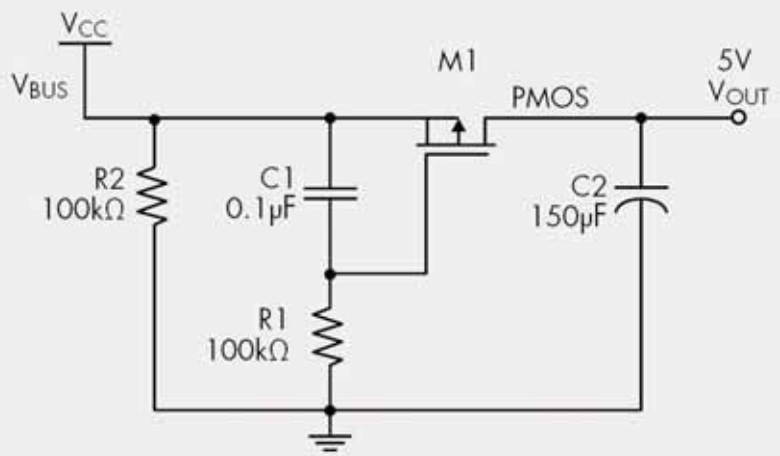
Inrush current is generated when the input load capacitance of the card is charged quickly when the USB interface's 5V voltage source is connected. Usually the resistance between the 5V voltage source and the load capacitance includes that of the printed circuit boards, cables and the power resistance and is less than 200mΩ. As a result, instantaneous initial current levels can be as high as 25A.

Such a large current change may combine with circuit inductance to cause an overshoot of system input voltage and thus damage the system. On the other extreme however, it may lead to system downtime caused by power supply overload. If using the soft-start circuit, as shown in Figure 1, once the wireless data card is inserted into the computer or external 5V power source, the PMOS tube M1 will be disconnected. Then the 5V power source utilizes R1 current-limiting to charge the C1 capacitor, which gradually reduces the gate voltage of PMOS to ground, minimizing the PMOS conduction resistance. In this process, the voltage of C2 will be raised to 5V in a safe manner. When the 5V power source is removed, C1 will be disconnected by discharge of the loop R1 and R2, thus closing M1 until the next system power-up. According to the time constant $\tau = RC$ and charging $U(t) = VBUS*(1-\exp(-t/\tau)$. Discharging $U(t) = VBUS*\exp(-t/\tau)$ shows the soft-start circuit consisting of C1 and R1 needs approximately 10ms to raise the voltage at the two ends of C1 from 0 to VBUS (to 63.2% of VBUS). Alternatively, the power-down recovery circuit consisting of C1, R1 and R2 needs approximately 20ms to reduce the voltage at the two ends of C1 to the original VBUS (36.8% of the original VBUS). Consequently, after 10-20ms charging, the system can basically achieve a smooth soft-start. After 20-40ms of discharging, the system can achieve smooth system recovery to offer protection against the quick plugging or unplugging of power supplies or poor contacts.

Of course, the soft-start circuit also has its inadequacies. For example, it has no over-voltage protection function, so many of the available 3G + WiFi wireless data card routing products often directly use a 5V wall adapter to supply power. Sometimes this is due to the electrical grid quality problems, adapter quality, or interference.

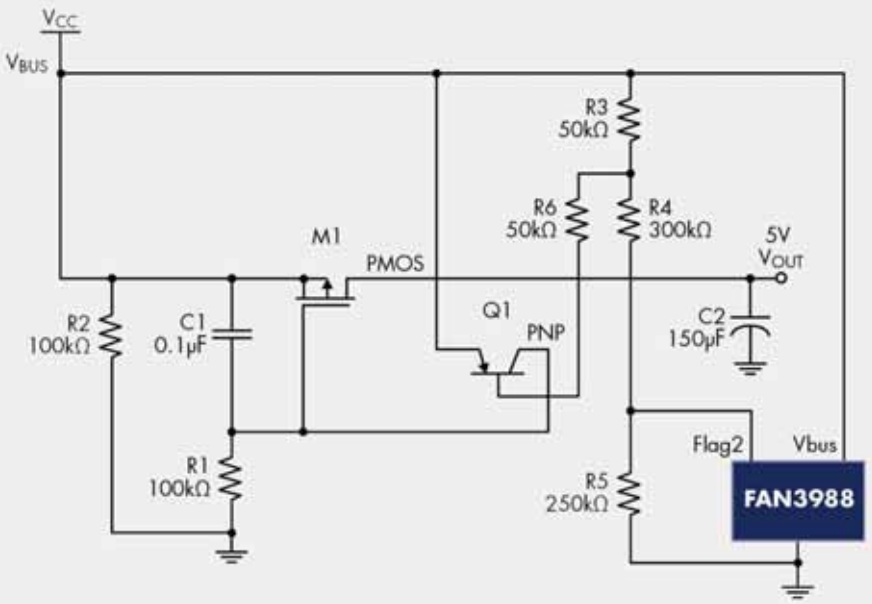
VBUS voltage may greatly exceed 5V, and following the soft-start of the power source such a high voltage will travel directly through M1 and enter the system, damaging the internal chip. For cost reasons, customers may select C2, which is usually a capacitor with a 6.3V rated voltage capacity, often leading to bursting or even burning of the capacitor.

Figure 1: USB power interface soft-start circuit



> If cost is not important, designers of wireless data cards would also consider using an over-voltage protection chip with a built-in power supply channel PMOS

Figure 2: Circuit solution with both soft-start and over-voltage protection functions



USB Circuit Of Power Interface

In view of the potential risks of the above soft-start solution, a circuit with both soft-start and over-voltage protection is recommended to respond to the need to protect the USB power interface. As shown in Figure 2, a PNP transistor Q1, over-voltage condition monitoring chip FAN3988 and four resistors, R3, R4, R5, R6, have been added. An advantage of this design is that soft-start and over-voltage protection can share the same PMOS tube M1.

The FAN3988 device's VBUS pin serves as the power input pin, supplying power to the chip and monitoring the voltage of VBUS in real time. When VBUS exceeds the typical 6V, or falls below 3.3V, the FAN3988's pin Flag2 goes low. Otherwise, Flag2 will give a high level electrical output. At this stage, appropriate transistor parameters and precision resistors are selected to control the turn-on or turn-off of the PMOS tube M1.

For example, when VBUS is greater than 6V, Flag2 of the FAN3988 device has a maximum voltage of 0.3V. In this state, the forward voltage difference at both ends of R3 will be greater than the emitter/base bias positive voltage of the transistor Q1, causing the base current flowing through R6 to be enough to cause saturated conduction of the Q1 emitter collector, reducing the difference between gate voltage of PMOS tube M1 and the VBUS voltage. At this point, M1 is shut down to realize the VBUS over-voltage protection function. Conversely, when the VBUS voltage is within the typical range of 3.3V-6.0V, FAN3988's Flag2 will maintain a high level electrical output of at least 2.4V, so that the voltage difference between both ends of R3 is not enough to turn on the transistor. In this state, the transistor Q1 will not not affect the normal operation of C1 and R1 over M1.

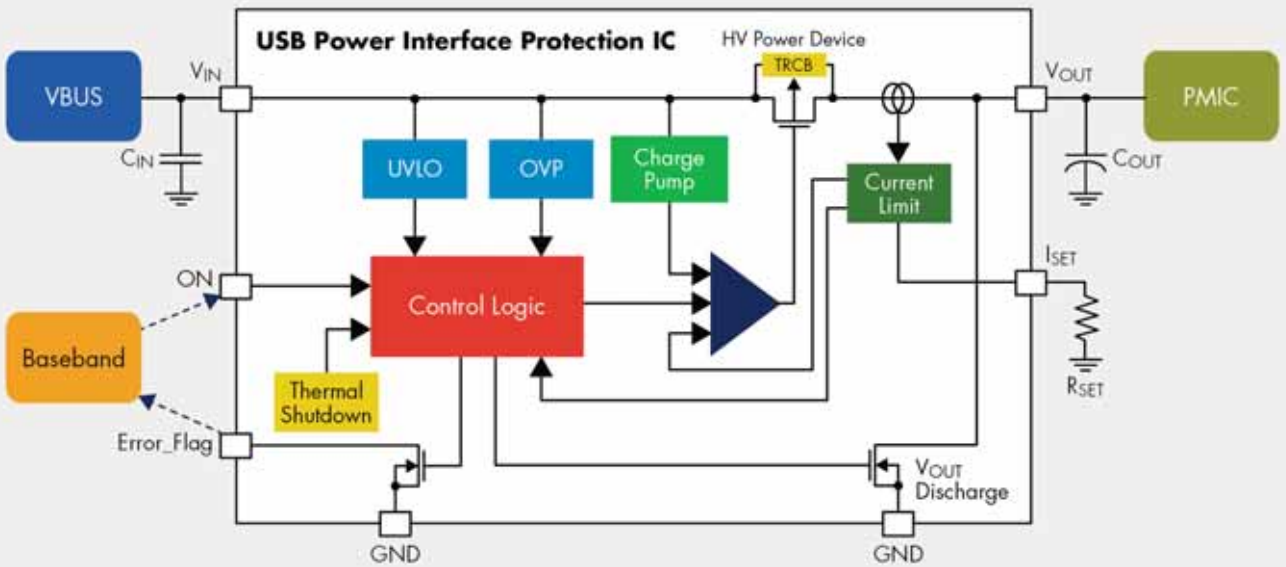
Of course, if not sensitive to cost, R&D engineers of wireless data cards would also consider using an over-voltage protection chip that have a built-in power supply channel PMOS, such as the FAN3989 device, positioned close to VBUS for over-voltage protection, and then serially linking a PMOS along with a relevant resistor-capacitor circuit for the soft-start function.

It is also interesting that, due to cost implications, many engineers attempt using only one PMOS tube alongside several cheap resistors, capacitors and simple over-voltage detection circuits to simultaneously achieve over-voltage circuit protection and soft-start functions. However, this is difficult to achieve, mainly as a result of conflicts in controlling the power supply channel PMOS tube's gate.

Consider that the gate circuit has to be controlled by the RC charge and discharge circuit. Following the VBUS over-voltage, its input voltage must be tracked. Sometimes VBUS voltage may be as high as 28V, to cause the PMOS voltage VGS to approach 0 and thus turn off PMOS. Therefore, possible conflict arises because soft-start requires the connection of capacitance across VBUS and the PMOS tube's gate, while over-voltage protection requires the connection of resistance between VBUS and the PMOS tube's gate. This cannot be realized simultaneously in a single circuit.

In short, the new discrete circuit solutions can work adequately, but are not perfect. For example, some mobile product systems may have requirements for over-current protection (OCP), thermal shutdown, short circuit protection, as well as under-voltage lockout and true reverse current blocking (UVLO & TRCB) protection. The proportionate area of the PCB, occupied by the discrete circuit, may not be satisfactory. In view of this, a number of industry-leading mobile IC vendors

Figure 3: USB power interface protection chip architecture and application solution



are actively developing chips with comprehensive protection functions in order to meet such mobile product market demands.

Single-Chip Solution

As problems with power supply compatibility and thermal damage of smart phones, 3G-WiFi wireless data cards, portable printers/scanners/projectors, portable hard drives and other mobile products appear, engineers will face stronger demands for the protection of USB power supply interfaces. Desingers will be need to give more consideration to material cost, circuit space, power consumption, as well as the timeliness and easy operation of circuit protection. Therefore, miniaturized, intelligent and integrated USB interface power protection chips will become increasingly important.

In Figure 3, a new type of USB power interface protection chip architecture and application solution is shown. The 5V wall-mounting USB interface power adapter directly provides power to the 3G-WiFi wireless data cards and routers, or to other small portable equipment. Chip architecture enables smooth system soft-start, withstands voltages up to 28V, has 5.8V over-voltage protection and over-current protection functions for variable currents ranging from 0.1A to 1.5A. Of course, the chip and system application architecture also addresses other common application problems.

> As more problems with various devices appear, engineers will face stronger demands for protecting USB power supply interfaces

For example, at the end of VIN, an approximate 4.7uF capacitor CIN can be placed, which can help prevent ill effects from the insertion of long power adapter cables to USB, namely a rapid rise of VIN to over 28V. At the end of VOUT, placing a capacitor COUT of approximately 300uF can help with any large current intake under system burst mode. The ULVO function enables the power supply channel to shut off when the VIN voltage is less than 3.5V, thus preventing system failures.

If the voltage at VOUT is greater than the voltage at VIN, the TRCB function can help ensure that, whether being turned off or turned on at the time, the power supply channel will be shut off and the polarity of the PMOS body diode will be adjusted to prevent reverse current. In the event of the unplugging of the power supply or poor contact, the new VBUS output discharge channel, VOUT, can quickly reinitialize, leaving VOUT ready for the next system power-up. In addition, the protection chip also has short circuit and overheating protection functions, and the baseband can obtain error status information, as well as enable/disable the protection chip. The system can set the desired current-limiting value in the power protection chip channel through an external RSET resistor.

Avoiding Interface Failure

For the safety and long term use of mobile products, engineers try to avoid all types of interface failure. Particular attention is paid to the protection of USB power interfaces. Currently, there are many protection circuits in the industry, each with certain advantages and disadvantages. Looking ahead, integrated protection chips with cost advantages will become mainstream in many market applications. For example, Fairchild Semiconductor will soon launch a USB power interface protection chip.

FOURIER ANALYSIS: THE STATE OF THE ART OF US SPECTRUM SENSING CAPABILITY?

BARRY MCKEOWN, OF DATOD LTD, BUILDING ON PREVIOUS ARTICLES, CONTINUES TO EXPOSE THE RELATIONSHIPS BETWEEN FRACTIONAL FREQUENCY INFORMATION IN COMMUNICATION SYSTEMS AND MAGNETIC RESONANCE SPECTROSCOPY

Roger Dalkie is a leading world authority on signal processing at the US National Telecommunications and Information Administration (NTIA). As with William Cameron of Boeing, he understands the limitations of Fourier Analysis and especially the limitations of the DFT and FFT, in particular, when applied for spectral component estimation.

I drew the reader's attention to Cameron's work in the September 2011 edition of Electronics World in the article entitled *"Spectrum Analysis: Opening Another Can of Worms"*, in which I posed a series of open questions.

In this article I will draw attention to further, related aspects of Dalkie's work from NTIA Technical Report *"TR-10-470: Radio Spectrum Estimates Using windowed Data and the Discrete Fourier Transform"*, published September 2010. This report, as with Dalkie's other published body of work, is primarily aimed at establishing a firm appreciation of the state of the art associated with the technical measurement requirements for future Dynamic Spectrum Access (DSA) technology and, especially, the crucial initial-acquision spectrum sensing element stage required when a wireless communication device is activated. Dalkie's work is particularly addressed at the emerging technologies for the NTIA's ongoing test-bed program. It should be noted that DSA technology should not be confused with whitespace technology.

Dalkie's Work

Dalkie states in his introduction: *"Digital signal processing algorithms are commonly used to obtain radio spectrum estimates based on measurements. Such algorithms allow the user to apply a variety of time-domain windows and the discrete Fourier transform to RF signals and noise. The purpose of this report is to provide a description of how signal processing options such as window type, duration and sampling rate affect power spectrum estimates. Power spectrum estimates for periodic RF signals and random processes (stationary and cyclostationary) are analyzed. The results presented can be used to select signal processing parameters and window types that minimize errors and uncertainties."*

Dalkie also states his conclusions as follows: *"In this report, we have described how the application of a window in conjunction with the DFT to periodic radio signals and radio noise affect power spectrum estimates. The results are used to describe how window characteristics and related signal processing parameters affect measurement errors and uncertainties.*

In the case of periodic radio signals, we show that there are errors due to spectral leakage and window scalloping. These errors depend on the window type and related signal processing parameters. In particular, error bounds for various windows are presented. In all cases, the leakage error can be reduced by increasing the number of signal periods in the window (i.e. the window duration). By far, the leakage error decreases most rapidly (as a function of the window duration) for the Gaussian window. The scalloping error is independent of window duration and is smallest for the flat top window."

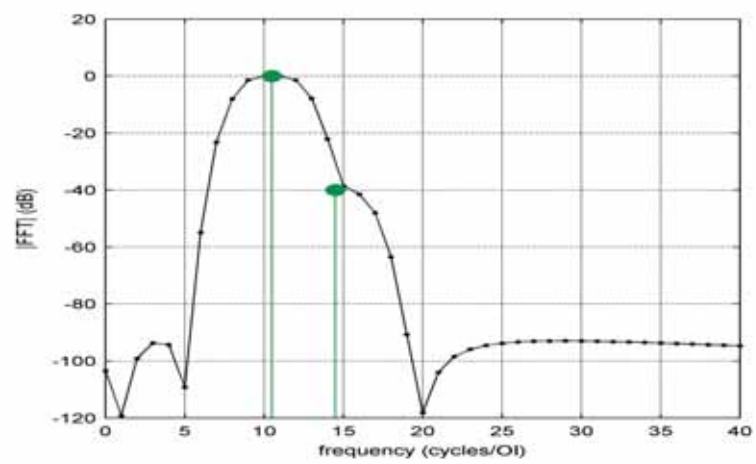


Figure 1: Cameron's signal with flat top window
N = 512 half-samples of Cameron's signal. Plotted on log scale.
Green is the underlying signal frequencies

Response	Frequency
-20 dB	3.3404
-40 dB	4.1297
-60 dB	4.5976
-80 dB	4.8651
-100 dB	4.9750

Table 1: Response and frequency

"In the case of stationary noise, we describe how the window and related signal processing parameters affect both the estimated power spectral density and the total power in the measurement bandwidth. It is shown that the window should be selected so that the noise power spectral density is essentially constant over the bandwidth of the window. Also, the window duration should be long enough so that the noise power spectrum is adequately sampled.

Cyclostationary random processes were also considered. In this case, we examined estimates of the time average of the power spectrum. It was found that in addition to the considerations described for stationary processes, the window bandwidth should be less than (one-half) the repetition rate of the covariance function." Oh Dear!

Of course, if all transmitted signals were truly cyclic and periodic over the observation interval required for signal recovery – by any communication system – then an actual window technique would not be required. Such is the fallacy of Dalkie's report which was exposed first by Cameron and latterly, and more fully, by Datod.

In real engineered systems, at this initial signal acquisition stage, especially as we journey towards deploying DSA spectrum sensing technology for sharing spectrum, the technical problem posed by Dalkie's solution kicks in. Note: any (implied) assumption about clock recovery and synchronisation made at this signal identification stage is irrelevant.

Fundamentally, Dalkie neglects the fractional signal aspect as described by Cameron, and the solution Cameron proposes, but Dalkie correctly concludes that for the application he is seeking to address for DSA spectrum sensing the flat top window is currently the state of the art for spectrum estimation open to the NTIA.

However, Dalkie misses an important aspect here related to spectral efficiency and something Shannon pointed out. Accordingly, I will first take the reader through some of the problems associated with applying Dalkie's flat top window citing the test signals introduced in the September EW article. We shall leave consideration of the Gaussian window case and other issues (sampling noise – what is that about?) that Dalkie raised for another time.

Applying Dalkie's Flat Top Window to Cameron and Datod Test Signals

In Figure 1 we have applied Dalkie's flat top window with the FFT to both of the Cameron fractional signals. Observe that Cameron's -40dB spectral component is barely identifiable by visual inspection, far less by an automated operation required for efficient real-time spectrum sensing estimation in wireless devices.

It is acceptable in this case for a trained human observer to presume that at least two signals are present and that their actual amplitude separation is of the order of 40dB but not much more.

In Figure 2 we have applied Dalkie's flat top window with the FFT to the Datod test signal composed of eleven fractional frequency spectral components. Notice also the effect of additional spectral broadening introduced by applying the window, particularly around the -60dB level. How much spectrum is being wasted here?!

Observe that only the eighth spectral component at 116.35 cycles per OI is clearly individually discernable. The application of Dalkie's flat top window has in fact broadened this spectral component at the attenuated response levels by the frequency margins detailed in Table 1. These are estimated (to 4 d.p. response-calculations) to be the values below the peak component value attained. However, these values are actually single-sided response estimates and are thus required to be doubled in practice. But – and it's a big "but", in a multi spectral component signal the so-called mathematical concept of superposition kicks in and individual responses run into each other across the complete spectral domain. Recall now Marie Farge's very important

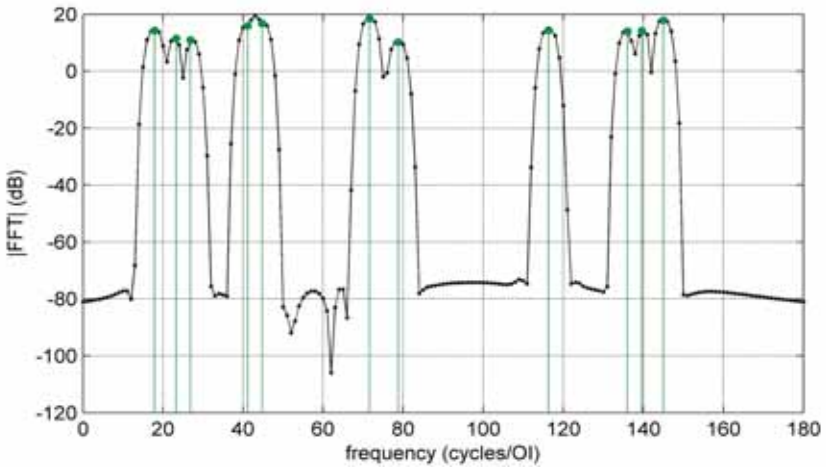


Figure 2: Datod test signal with flat top window
N = 1000 half-interval samples of test signal. Plotted on log scale.
Green is the underlying signal frequencies

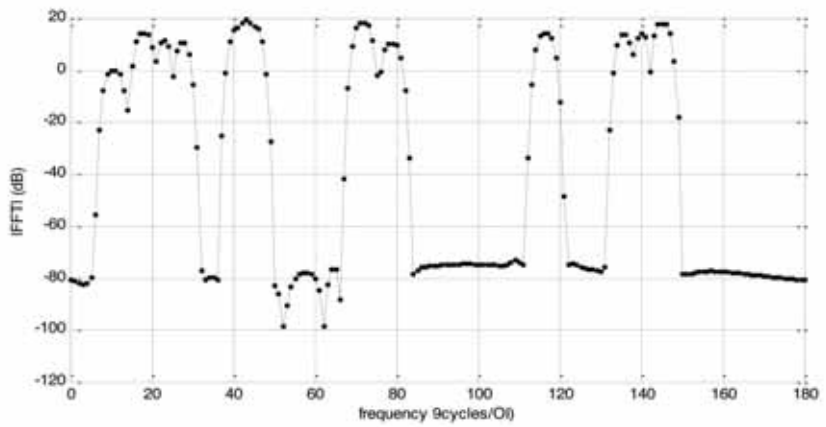


Figure 3: Composite Cameron and Datod test signals with flat top window

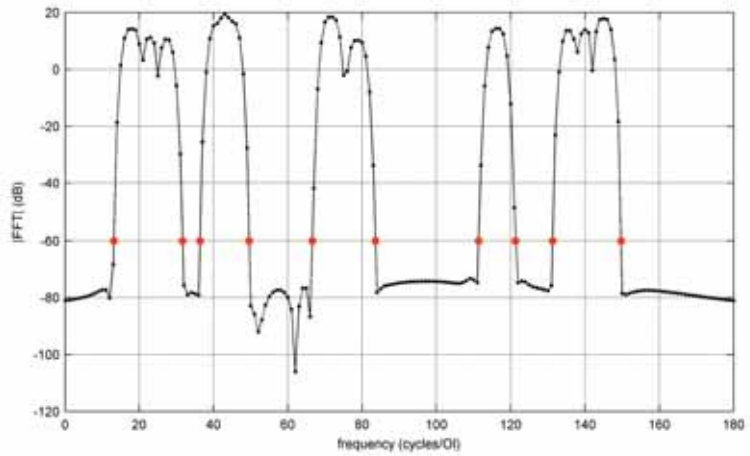


Figure 4: Datod test signal with flat top window and the -60dB spectral component locations

observation from the September article; then observe also in Figure 2 that when the fourth and fifth spectral component run into each other they give a central positioned spectral peak, which is above the actual amplitudes of these spectral components. Oh, dear; so much for a scalloping loss! Consider now also this Farge effect on the other spectral components cited.

What happens when we create a composite signal combining both the Cameron and Datod test signals and apply Dalkie's flat top window? The result is shown in Figure 3.

A big "Oh, Dear"! In all parameter respects, in terms of frequency, amplitude and phase, none of the spectral components can be accurately estimated. More worrying still, even Cameron's second spectral component at -40dB is incapable of being recognised by Dalkie's flat top window applied with the FFT in this case. So could the FFT locate this "lost" -40dB spectral signal without the window or even with another window type applied? Those readers who attempted the -60dB spectral component identification exercise posed in the previous article will know the answer already. Note: The Datod algorithm applied in the September article accurately identifies the -40dB component.

The really serious point to address here is the waste of a precious asset called Spectrum and recognising and accepting that windowing is a work-around procedure developed by engineers to overcome a specific problem with the applied mathematics that has still to be fundamentally addressed in the art of signal processing.

Now give serious consideration to what happens when interfering signals are present and how you identify wanted from unwanted spectral components, dominant, sub-dominant or otherwise at this initial spectrum sensing stage. It's a big question but do you know the answer?

Well, for sure the US NTIA doesn't and neither do the participants of the NTIA test bed either, otherwise Dalkie would be addressing another measurement technique altogether! As for current 3G and 4G technologies: how have they been engineered to address spectral efficiency and operation in this type of spectrum environment? So, the question arises: Exactly how much spectrum do they actually waste?

Accordingly we pose the following exercise concerning the identification of a spectral efficiency measurement technique for readers and the NTIA. In Figure 4 and Table 2 we have identified the location of each of the ten -60dB spectral crossovers in the (eleven spectral component) Datod test signal. What would the reader and the NTIA consider to be an efficient technique for estimating the commercial value of this wasted finite resource, known as spectrum, when this baseband analysis is translated up in order to be engineered into actual real estate for transmission? (Note: We have set the -60dB level for reasons that we shall return to at a later time.)

Location No.	1	2	3	4	5	6
Frequency	13.1668	31.6591	36.3562	49.5869	66.5942	83.5919
Location No.	7	8	9	10		
Frequency	111.3598	121.4349	131.2987	149.6920		

Table 2: Datod test signal -60dB spectral component locations

Questions Arising From Dalkie's And Cameron's Conclusions

In the conclusion of Cameron's paper previously cited, he explains how the application of the sampled signal has been *"contrived such that its Fourier Transform displays the sampling artefacts observed in the FFT"*.

He also states that: *"in Section IV equations were given which precisely predict the transform artefacts due to a signal composed of a single, fractional frequency component. Employing the superposition principle the equations of Section IV the FFT of a sampled signal of arbitrary spectral composition can be predicted."*

"Employing the superposition principle"? Indeed! The trouble with Cameron's approach is that based on the analysis of a single component, his maths (assuming it is correct) cannot fully be extended to precisely predict cases such as the Datod test signal. Also, if you study his diagrams you will see that there are introduced into the spectrum *"small spurious responses distributed near the larger and or smaller spectral components, depending on which case is considered"* by his PSE method. I wonder what Marie Farge would have to say. Superposition in the time domain is linear? Superposition in the frequency/function domain is not?

I will get to Shannon shortly, but am I stating that both Dalkie and Cameron are wrong? Absolutely not! They are both engineers adopting the rules of applied mathematics as they have been instructed in and in which both are extremely well-versed. So where does it all go wrong and who messed up? I won't name the people just yet but they are mathematicians; long, long dead.

Mathematical Adventures

The physicist Einstein (1879-1955) said that *"The trouble with chemistry is that it is too difficult for chemists"*. The mathematician David Hilbert (1862-1943) retorted that *"Physics is far too difficult for physicists"*. So where does that leave us humble engineers who have to bridge the continuous versus discrete mathematical divide handed down in signal processing in order to be able to work in this gap?

I would suggest that we don't. Why should we? It's the mathematicians' mess, so surely it

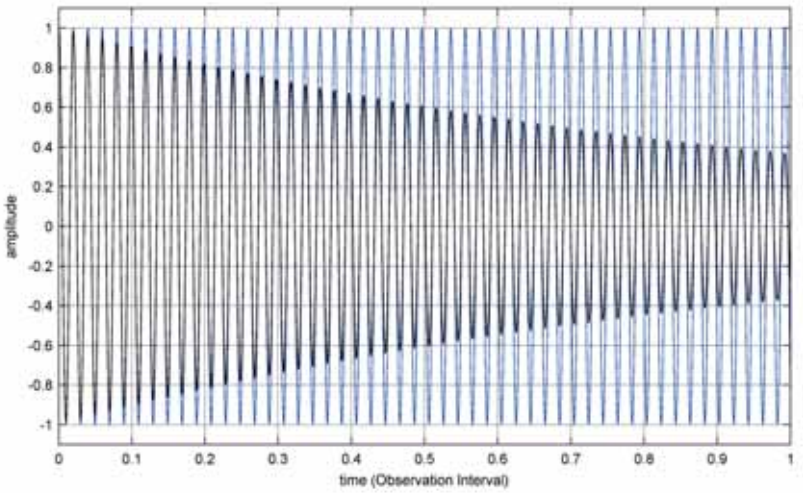


Figure 5: Free inductive decay response overlaid on sinusoid 50.4 cycles/OI

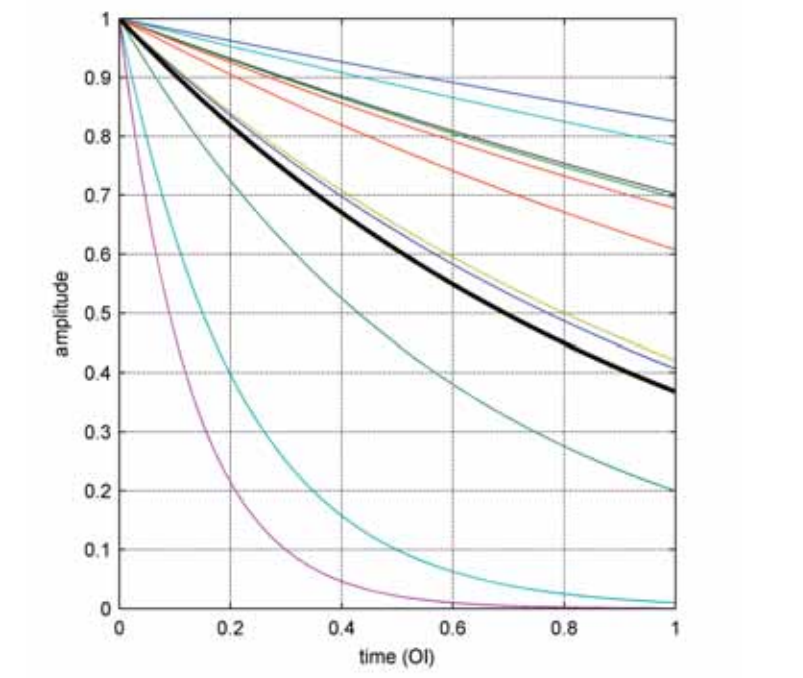


Figure 6: Exponential amplitude decay responses applied to Datod test signal

should be up to them to clear it up, right? But I suppose the concept of the rhetorical question would be lost on a mathematician. Nevertheless, I would also suggest that engineers have to devise a better work-around than Dalkie's windows and Cameron's PSE algorithm in order to construct physically engineered systems that are more spectrally-efficient communication systems, especially for deployed spectrum sensing communications.

So, as engineers, where do we look to what's missing? First we have to revisit the arguments surrounding the "calculus" (I never believed what my secondary school teacher taught me; probably because she did not believe in what she was teaching either) and not get suckered into the priority disputes, so beloved of the mathematicians' vanity.

Newton's form of the calculus arose from geometrical methods and his Method of Fluxions was deemed cumbersome, whereas the Leibniz algebraic form was deemed much more powerful and versatile. Both approaches have historically had their supporters and detractors, but how much consideration has been given to realising that Newton's form applies to a discrete system, as Newton deals with events and processes occurring at a point, whereas the Leibniz form relates to what occurs over the interval, between points, and thus relates to a continuous system?

In the physical reality of a discrete, engineered system operating over an observation interval in time, the concept of a limit and infinity is anathema. That statement might seem obvious to us engineers but to some mathematicians it is heresy. However, neither Newton nor Leibniz messed up here; it was their followers who undertook the study of Limit Theory and introduced their concept of infinity and functions. So, who was it who attempted to stitch them together to create this corruption of ideas?

It was one of my colleagues, an Oxford trained mathematician, who put it another way: *"Their mistake is to try to work back"*. With this illuminating insight, both Dalkie and Cameron should care to revisit their work and eliminate all limits and infinity arguments and see where they get. In this respect Cameron's Figure 1 should be compared with Newton's diagrams and methods.

Einstein at one time stated that the universe is "finite but unbounded". Given the recent palaver at CERN over the speed of light, which at heart has the theoretical mathematical basis of the concept of infinite energy, there is still hope that sanity might prevail and mathematicians look afresh at this gap issue and engage in some critical self-analysis.

In the preface to his book written in 1917 *"The Continuum"*, Hermann Weyl (1885-1955) states that *"it is not the purpose of this work to cover the 'firm rock' on which the house of analysis is founded with a fake wooden structure of formalism – a structure which can fool the reader. Rather, I shall show that this house is to a large degree built on sand. I believe that I can replace this shifting foundation with pillars of enduring strength. They will not, however, support everything which today is generally considered to be securely grounded. I give up the rest, since I see no other possibility"*.

The tragedy is that Weyl never finished this work; other events intervened. I would recommend that this short book be required reading for every discrete "digital" designer; especially the modern foreward by the physicist J.A. Wheeler and his comment on irrationals. Then try to understand why Weyl never got there and just what the "firm rock" actually is.

The deeper tragedy for Western (and especially US) technical dominance in signal processing and mathematical analysis is that since the sixties it has been built on this "pillar of sand". Furthermore, in the case of matched filtering and detection theory: a

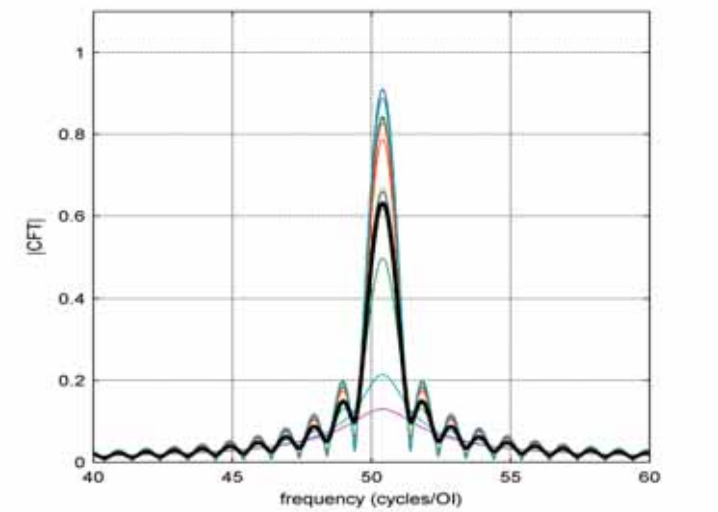


Figure 7: Computed continuous Fourier transform frequency domain FID responses

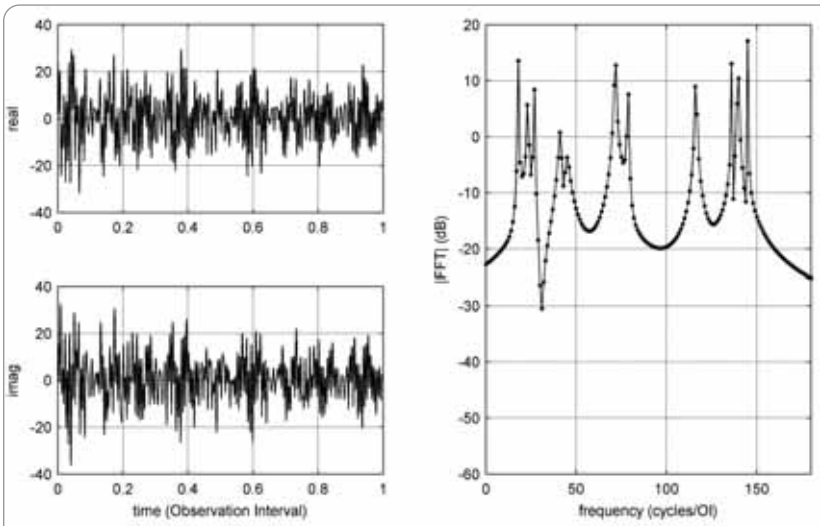


Figure 8: The Datod FID test signal with FFT

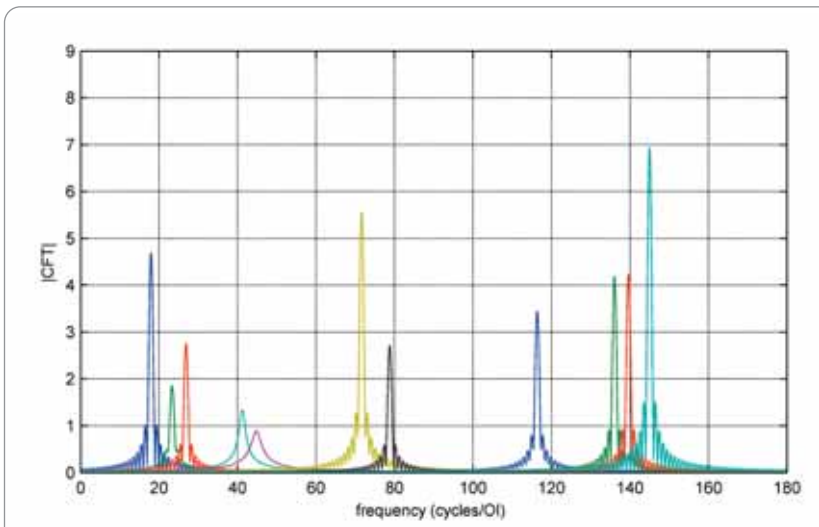


Figure 9: The CFT of the individual Datod FID test signals components overlaid

pillar of salt. Which will lead us eventually to David Middleton and his work, also for the US NTIA, but that is another far more contentious story.

How do we proceed in order to understand how to unstitch all this mathematical mess? Actually, we need to push ahead with these "processes" and understand how they unravel with the additional work-around that has been further introduced before placing it in the context of the work of Maxwell (1831-1979) and Felix Bloch (1905-1983) and both their famous sets of equations.

Maxwell needs no introduction; Bloch was a Nobel Laureate and Weyl's student, who became the first Director-General of CERN in 1954 and also the first Professor of Theoretical Physics at Stanford. In 1928 his work lead to the Quantum Theory of Solids in which he applied his Bloch Waves to describe electrons. It is the phenomenological Bloch equations he devised which are foundational to the truly marvellous engineering achievements of magnetic resonance imaging and magnetic resonance spectroscopy.

Adventures in Magnetic Resonance Spectroscopy

When Fourier analysis (augmenting a second-order differential equation model) is adopted by MRSpectroscopy, the resulting observable time-domain response exhibits a damped sinusoid due to an applied forced vibration. This response characteristic is known as a Free Inductive Decay (FID) in the literature. The where-with-all of the theoretical analysis should not concern us; instead, it is the usual induced spectral artefacts that arise in the DFT/FFT and the work-around introduced that I wish to bring to the reader's attention.

In Figure 5 we present a time domain signal comprised of a fractional 50.4 cycles per OI signal which is overlaid with a damped exponential response thanks to the forced vibration model familiar to engineers.

In Figure 6 we introduce a range of exponential roll-off time-domain envelope responses that we will apply to the individual eleven spectral components of the Datod test signal. In addition we introduce for reference a black line which represents the response for the unitary e-1 roll-off factor. Note that three of the roll-off decays are below this unitary value, whereas the other eight are above it.

Instead of rushing to the FFT we will now compute the individual Continuous Fourier Transform (CFT) of the theoretical response and overlay these individual frequency responses in the normalised magnitude scale.

For a deeper insight into the resulting frequency response profiles we will apply all

these amplitude decays individually to a signal at 50.4 cycles per OI in Figure 7 for reference. Note that with no decay applied, the theoretical response attains unity. Observe now the shape of the frequency response of the three decayed components that are below the unitary e-1 roll-off factor.

One issue that will be familiar to engineers is the establishment of Q-factor analysis and how this relates to resonance. But what familiarity, especially among communication engineers, is there with a decayed resonance being damped out over time and the importance of this aspect to physicists and chemists?

We now apply these eleven exponentially decayed responses to the original Datod test signal components. In Figure 8 we plot both the time domain and the normalised FFT magnitude response of the composite FID signal. These diagrams should be compared with the diagrams in the previous article in order to gain a full appreciation of the further difficulties introduced by the decay parameters and the Datod algorithm that was introduced to overcome the inadequacies of the FFT. Now, if you were unaware that this FFT in Figure 8 incorporated a decay element, could you tell by visual inspection?

In Figure 9 we plot overlaid the eleven theoretical individual normalised magnitude CFT spectral components and in Figure 10 we plot the composite normalised magnitude FFT frequency response. Comparing these figures we observe the difficulty of superposition when viewed in the frequency domain and what the MRS community are up against.

For good measure we now apply Dalkie's flat top window to the Datod FID test signal in Figure 11. Observe the effect of line broadening introduced here by the window. Recall that Dalkie states this to be the window reputed to give the most accurate amplitude peak information. Unfortunately Dalkie does not consider the effect introduced by exponential decay due to forced vibration. How do these amplitudes compare with the individually plotted theoretical responses from Figure 9?

Now we delve into the work-around introduced by the MRSpectroscopy community. In the recent survey paper *"H MR Spectroscopy of the Brain: Absolute Quantification of Metabolites"*, Jansen, Backes, Nicolay & Kooi, Radiology, Vol 240, No 2, Aug 2006, outline the state of the art of the FFT applied to essentially "count molecules". With the FFT this task is a big ask.

What the MRSpectroscopy community does is essentially "peak" the FFT spectrum, component by component, applying first a

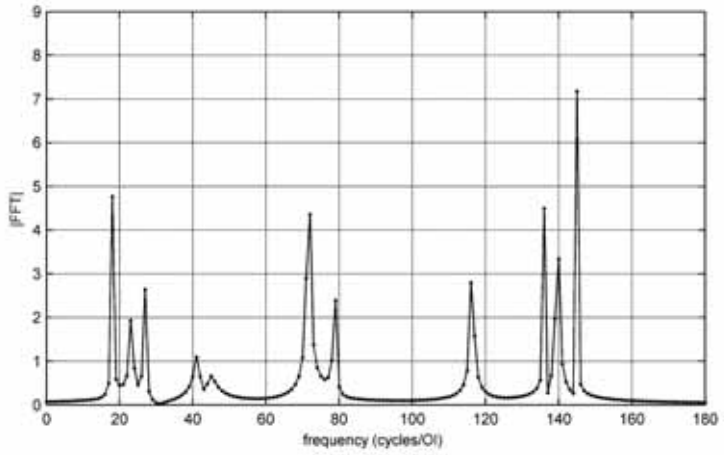


Figure 10: The FFT of the composite Datod FID test signal

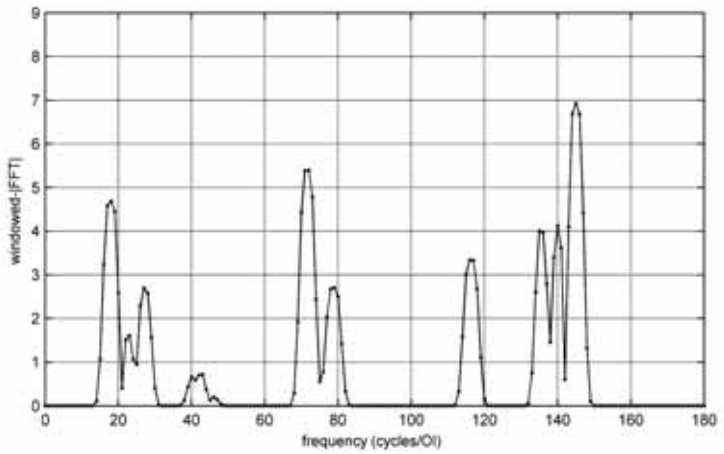


Figure 11: The FFT of the Datod FTD test signal with the Dalkie flat top window

Quadrature Phase Cycling rotation operation and then applying a line fitting algorithm such as the Lorentzian, Gaussian or Voigt model response profile between the "peak" and the "half-height" of the FID frequency response. Compare the signal response at 116.35 cycles per OI in Figures 9, 10 and 11. What do the readers consider to be an acceptable margin for error in this line fitting approach? Again those with access to an FFT package should undertake this as an exercise: it will prove worthwhile and enlightening. Note: without the decay parameter, a quadratic would suffice for line fitting although this step is unnecessary in communication systems.

Being alert now to the pitfalls with fractional frequency determination, we should quote from the paper itself in order to gain an insight into how this community appreciates the problems they confront. We begin by ascertaining what MRSpectroscopy is currently applied for. They authors state: *"Hydrogen (1H) magnetic resonance (MR) spectroscopy enables non-invasive quantification of in vivo metabolite concentrations in the brain. It has proved to be a powerful addition to the clinical assessment tools for numerous pathologic conditions, including epilepsy, multiple sclerosis, stroke, cancer, and metabolic diseases. In nuclear MR, the total area under a metabolite resonance in a 1H MR spectrum is directly proportional to the concentration of the metabolite."*

So, what this MRSpectroscopy community are applying Fourier Analysis to is determining, by measuring an area under a "localised" resonant section of the FFT, the number of molecules present and their concentrations. They characterise the spectral peaks thus: *"Characteristics of MR Spectra: A water-suppressed brain 1H MR spectrum typically displays a number of signals that correspond to several brain metabolites. These signals are characterized by one or more peaks with a certain resonance frequency, line width (full width at half maximum of the peak's height), line shape (e.g., Lorentzian or Gaussian), phase, and*

area. The peaks are separated owing to differences in resonance frequency, which are caused by the difference in the chemical environment of the different nuclei. The molecular structure of a particular metabolite is reflected by a typical peak pattern. The area of a peak is directly proportional to the number of nuclei that contribute to it and to the concentration of the metabolite to which the nuclei belong. However, the peak areas are also influenced by other factors, including T1 and T2 relaxation times".

Now, according to mathematical theory, the technique for estimating areas under a curve is integration. This community views the merits of this technique as follows: *"**Integration**: The traditional procedure to determine the area of a certain peak in the frequency domain is integration. The operator selects a frequency range, which preferably contains only one peak, and then performs numeric integration. Because only the total area under a resonance corresponds to the real peak intensity and the contribution beyond the lower and upper integration boundaries is neglected, the peak area will be underestimated (possibly by up to 40%). Therefore, integration is an adequate method only if the resonances are well separated without any baseline fluctuations. Unfortunately, this is rarely the case, since most in vivo spectra suffer markedly from spectral overlap and baseline fluctuations. Therefore, the area can hardly be attributed to a single resonance, and, in addition, the baseline will lead to an unknown contribution."*

Spectral overlap? Baseline fluctuations? Note the error margin cited and what is deliberately neglected!

Accordingly they appear to know what they want from the FFT and recognise some of the pitfalls present with identifying areas under a curve. Unfortunately, now they introduce the work-around for peak fitting: *"**Peak Fitting**: In this approach, all important peaks are initially selected and coarse estimations of the resonance frequency, line width, and peak intensity are performed, either by the operator or by an algorithm. Subsequently, a fit is performed by using a least-squares optimization algorithm, which iteratively fits all peaks to a line-shape model function, so that the fitted spectrum resembles the experimental spectrum as closely as possible. In general, this method proves to be fairly robust with respect to spectral overlap. However, if the actual line shapes deviate substantially from Gaussian or Lorentzian model functions, the algorithm will not be able to fit the peaks accurately. To prevent this problem, other line shapes have occasionally been used, of which the Voigt profile is the most common. However the use of a Voigt profile introduces more degrees of freedom in the fitting procedure, which can lead to ambiguous results."* There you have it.

Evidently this community recognises that they have a problem and are extremely circumspect in how they interpret their results. Fundamentally though, they do not question the efficacy of the FFT and with it windowing, zero padding and filtering techniques of signal processing.

How do they characterise the accuracy of their response measurements? By the usual method of building models on top of models, in this instance a statistical model: *"Important Considerations for Data Analysis: Quantification accuracy. It is important to study and report the error estimates of the quantification method. Most of the fitting routines present the so-called Cramer-Rao minimum variance bounds, which reflect the theoretical standard of precision for the model parameter estimates obtained from the data."* If this was not such a serious issue, that statement would be hilarious.

The Physics Community Treatment?

For those readers interested in the wider aspects of the line-width and superposition measurement uncertainty, I would further refer you to a recent paper *"Transport through modes in random media" Wang & Genzck: Nature Vol 471 March 2011*. This paper outlines measurements carried out when a microwave field is transmitted through samples of randomly positioned alumina spheres embedded in Styrofoam within a copper tube. Essentially, they are still trying to "count molecules" or in this case alumina spheres. This community have developed other mathematical techniques which are still, nevertheless, just applying models on top of models.

In this case they utilise a Vector Network Analyser (a coherent frequency measurement instrument – worthy of a separate lesson for another day) to produce a measurement of the frequency variation of the resultant speckle pattern. Then they apply another model. They fit a line through the sampled speckle resonance pattern and from this resultant fit they apply another modelling technique to decompose this fit into the required modes they are seeking.

In their example cited they show how one of the measured and "fitted" resonance peaks is composed of three modes, to demonstrate that the resultant measurement is actually a destructive interference pattern. Unfortunately, they have failed to ascertain the adequacy of their initial Fourier model and what they are seeking from frequency domain measurements transformed back into time domain information and to just appreciate what mathematical transforms are actually intended for mathematically.

Datod FID Algorithm: One Solution

As with the case of the previous Datod algorithm, discussed in the September article, it is to accept that the best solution is not just to abandon windows altogether but also to abandon the FFT (a leap which Cameron does not take) and resort to standard geometry, trigonometry, algebra and the raw processing power of modern computing as we have done. After all, the limiting technical hardware issues relating to computer memory and mainframe processing power, which resulted in this ubiquitous uptake of the FFT, are no longer with us.

Accordingly, we have gone further and developed another alternative algorithm based on this approach, which when applied to the Datod FID test signal gives the results outlined in Table 3 from the following equation:

$$s(t) = \sum_{k=1}^{11} A_k \, e^{-M_k t} \, e^{2\pi i (f_k t - \theta_k)}$$

One traditional example of the application of this Datod Algorithm is that it is still possible not only to accurately identify the time domain parameters but by a careful synthesis of each spectral component they can be subtracted from an "actual Frequency Spectrum" (not the FFT spectrum) measurement for analysis of the residual signals. Thus resolving the superposition issue that line fitting ignores and hence once dominant components are removed by subtracting across the whole spectrum the sub-dominant components can be identified, all without recourse to filtering.

Shannon

Finally we arrive at Claude Shannon (1916-2001), genius and enigma: when he is right he is wrong and when he is wrong he is right! Shannon's work underpins virtually all of modern communication theory, derived from Bell Labs, but it is one aspect of his *"Part III: Mathematical Preliminaries"* section that I wish to point out Dalkie's Theorem 15 and to put this down as a further marker:

It appears to me that the vast majority of the 'digital' community who apply the

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	Frequency fk (cycles/OI)		Decay parameter Mk		Amplitude Ak		Phase θk (cycles)	
	Actual	Estimated	Actual	Estimated	Actual	Estimated	Actual	Estimated
Sig 1	17.90	17.9000	0.1915	0.1915	5.16	5.1605	0.87	0.8700
Sig 2	23.27	23.2698	1.6120	1.6117	3.75	3.7506	0.93	0.9299
Sig 3	26.85	26.8500	0.4987	0.4998	3.51	3.5119	0.26	0.2600
Sig 4	41.17	41.1702	4.6210	4.6202	6.24	6.2423	0.16	0.1601
Sig 5	44.75	44.7501	7.7016	7.7093	6.85	6.8559	0.87	0.8701
Sig 6	71.60	71.6000	0.8664	0.8664	8.32	8.3199	0.24	0.2400
Sig 7	78.76	78.7600	0.3536	0.3536	3.23	3.2300	0.65	0.6500
Sig 8	116.35	116.3500	0.9002	0.9002	5.24	5.2399	0.97	0.9700
Sig 9	136.04	136.0400	0.3629	0.3629	5.00	4.9999	0.66	0.6600
Sig 10	139.62	139.6200	0.3894	0.3895	5.10	5.1001	0.87	0.8700
Sig 11	144.99	144.9900	0.2407	0.2408	7.81	7.8105	0.01	0.0100

Table 3: Datod exponentially damped frequency response and estimation algorithm results

The following result is derived in Appendix 6.

Theorem 15: Let the average power of two ensembles be N_1 and N_2 and let their entropy powers be $\bar{N}_1$ and $\bar{N}_2$. Then the entropy power of the sum, $\bar{N}_3$, is bounded by

$$\bar{N}_1 + \bar{N}_2 \leq \bar{N}_3 \leq N_1 + N_2 .$$

White Gaussian noise has the peculiar property that it can absorb any other noise or signal ensemble which may be added to it with a resultant entropy power approximately equal to the sum of the white noise power and the signal power (measured from the average signal value, which is normally zero), provided the signal power is small, in a certain sense, compared to the noise.

DFT/FFT are either unaware of this particular aspect or have given it little thought from his famous *"A Mathematical Theory of Communication"* in the Bell System Technical Journal paper from 1948. However, fundamentally, if you review Shannon's paper what aspect of Fourier Analysis and Weyl's "firm rock" is it built on? For it is on the basis of Shannon's Information Theory that techniques such as that of his colleague Bob Gallagher, now at MIT, in 1960 developed the Low Density Parity Check Codes which play a prominent role in today's communication technology for achieving close to the Shannon Limit for transmission over noisy channels; made practicable now only due to raw processing power then unavailable.

I would also call attention to the following statement from Gilbert Strang's standard text book "*Wavelets and Filter Banks," (page 452): "In closing we recall the original problem – to localise in time and frequency. Geophysics needs to represent short high frequency pulses. Physics needs to divide phase space. The coherent states* g_{pq} - $e^{ipx}g(x - q)$ *give a "Weyl-Heisenberg" frame, with some redundancy – but still f can be reconstructed from* $ff(f,g_{pq})g_{pq}dpdq$. *Mathematics needs (or wants) an orthogonal decomposition, better than* g_{pq} *at high frequencies and with no redundancy. The answer for now is wavelets."*

Wavelets are not the answer, though Gilbert is a wise man, and a leading world expert on linear algebra at MIT, who very well understands the boundary condition aspects of this mathematical technology and that we do meet redundancy in nature. But this redundancy is of a wholly different character and thus the mathematical concept of orthogonality has had its day in engineering and with it goes the FFT, especially as we journey towards quantum computing within the Cloud.

So Where And When Did It All Go Wrong?

For those of you tempted to place the blame with Fourier, don't! Fourier (1768-1830) was a brilliant military scientist seeking the mathematical tools to determine heat flow through a cylinder in order to design better cannons. It was the mathematicians who argued and squabbled over his work.

Instead, I would direct you to the remarks of his fellow countrywoman, philosopher and polymath Simone Weil (1909-1943) on the subject of algebra.

"Money, mechanisation, algebra. Three monsters of contemporary civilization. Complete analogy.

Algebra and money are essentially levellers, the first intellectually, the second effectively.

About fifty years ago life of the Provencal peasants ceased to be like that of the Greek peasants described by Hesiod. The destruction of science as conceived by the Greeks took place at about the same period. Money and algebra triumphed simultaneously.

The relation of the sign to the thing signified is being destroyed; the game of exchanges between signs is being multiplied of itself and for itself. And the increasing complication demands that there should be signs for signs...

Among the characteristics of the modern world we must not forget the impossibility of thinking in concrete terms of the relationship between effort and the result of effort. There are too many intermediaries. As in the other cases, this relationship which does not lie in any thought lies in a thing: money.

As collective thought cannot exist as thought, it passes into things (signs, machines...). Hence the paradox: it is the thing which thinks and the man who is reduced to a state of a thing.

There is no collective thought. On the other hand our science is collective like our technics. Specialisation. We inherit not only results but methods which we do not understand. For the matter of that the two are inseparable, for the results of algebra provide methods for the other sciences."

Simone's brother was the leading mathematician Andre Weil (1906-1998) whose work primarily related to Number Theory and Algebraic Geometry! Coincidence? ●

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Figure 1: The 6000 series Ethernet connectors are ideal for solar energy applications

ENSURING UNINTERRUPTED CONNECTIVITY UNDER OFTEN CHALLENGING CONDITIONS REQUIRES DURABLE, ENVIRONMENTALLY SEALED CONNECTORS, SAYS **STUART HUTCHINGS**, CONNECTIVITY MARKETING MANAGER FOR BULGIN

In today's fast-paced world, where an ever-increasing number of devices are in constant contact – collecting information and responding to external inputs under almost every type of environmental stress – maintaining uninterrupted connectivity is quite a challenge. To ensure equipment can operate consistently and reliably under demanding conditions, OEM manufacturers and suppliers require durable, environmentally sealed connectors and the support of knowledgeable and experienced interconnectivity partners.

Connectors are ubiquitous and, despite their unassuming appearance and sometimes hidden nature, they play a key role in an enormous variety of applications where outstanding performance and reliability are essential. The solar energy industry – which is currently seeing strong international growth – is one potential application for easy to assemble, 'fit and forget' connectors. Although there have recently been moves in Europe to reduce subsidies for solar technologies, there is still a great deal of interest in this green industry, with large solar energy farms being built throughout the world, particularly in the Middle East. Many individual solar inverters must be networked to maintain power distribution across the grid, and advanced electronic control is vital to the creation of a stable energy supply. This requires numerous signal and data connections, each of which must be compact and resistant to penetration by dust or moisture, as well as being UV resistant and able to withstand long-term outdoor exposure.

The food processing industry is another area with a huge number of potential applications for easy-to-use waterproof connectors. As a 24-hours-

a-day, 'always on' industry, food production requires a vast array of electronically-controlled equipment: from conveyors, dispensing machines and ovens with remote monitoring and control requirements, to printers, weighing systems and product inspection equipment with advanced data capture, transfer and storage needs. Strict food safety and hygiene standards are enforced and, as a result, equipment in the food production environment is subjected to regular cleaning and washdown procedures, creating the need for robust, dustproof and waterproof connectors to ensure reliable power, signal and data transfer. In this industry, the use of IP69K rated connectors gives engineers the assurance of a product that meets their stringent requirements.

Fit and Forget Connectivity

Water is an obvious hazard where electrical equipment is concerned, but dust-proofing is equally important, since dust – and particularly cement dust – can erode contacts fairly rapidly, rendering an unprotected connector useless within weeks.

Screw-coupling waterproof connectors have been available for many years. Although very effective, these traditional locking systems take time to couple, and some operators find themselves uncertain of just how tight the connectors need to be to ensure they seal effectively. Clearly, there is a demand for 'quick fit' couplings that are both waterproof and dustproof, and require minimal operator expertise to connect to equipment.

Types of Connector Materials

To accommodate as many applications as possible, both plastic and metal connectors are available. Plastic couplings are manufactured from a blend of PBT (polybutylene terephthalate) and polycarbonate, which significantly reduces the risk of moisture accumulating within the connector and is UV stable, making them ideal for outdoor applications. In addition, these UL94 V-0 rated self-extinguishing connectors are halogen-free, ensuring that in the event of fire no toxic gases are emitted.

While plastic connectors can offer a cost-effective solution, there are applications that require a more robust and rugged material, or where electromagnetic compatibility (EMC) is a potential issue. For these applications, metal connectors are preferable, providing continuation of the cable screen through to the mating connector – and therefore the equipment – and completing the Faraday cage. Perhaps uniquely, metal and plastic can be interchanged, offering increased flexibility for a variety of applications.

BULGIN'S BUCCANEER 6000 SERIES

THE NEW BUCCANEER 6000 SERIES OF EASY-TO-USE PUSHPULL CONNECTORS COMBINES COMPACT SIZE AND DURABILITY TO OFFER AN INNOVATIVE ALTERNATIVE TO SCREW COUPLING CONNECTORS THROUGH A UNIQUE LOCKING MECHANISM THAT REQUIRES JUST A 300 TWIST OF THE COUPLING RING TO COMPLETELY SECURE THE CONNECTOR.

Designed to withstand the harshest environments, these 'fit and forget' connectors have a single piece body and can be connected much more rapidly than connectors with a traditional screw thread mechanism.

The range includes data (USB Ver.2 or RJ45 Ethernet), signal and power versions up to 16A and 277V, and all options meet IP66, IP68 and IP69K standards. Body mouldings and pin carriers are designed to create a robust interface and avoid damage during coupling – guaranteeing a correctly sealed connection, even where access is restricted – and provide engineers and product design professionals with even greater flexibility for a broad range of applications.

The Buccaneer 6000 Series also simplifies casing and panel design by providing a common fitting for both data and power connections.

Figure 2: Robust, waterproof connectors play a key role in an enormous variety of applications

Figure 3: Potential electromagnetic compatibility issues may be resolved by the use of metal connectors

For example, an EMC problem may be resolved by the use of a metal connector within the equipment, while using a corresponding plastic mating connector will reduce the cost as much as possible for the customer. Similarly, for some equipment a plastic connector may be the ideal solution, yet the cable mounting half of this interface may need the additional strength of a robust metal connector to ensure it is not damaged in use.

Crucial Considerations

Any chain is only as strong as its weakest link, and reliability is a crucial consideration in an industry where failure of a single connection can halt an entire production line, potentially causing a lengthy period of downtime and significant revenue losses while the fault is diagnosed. So selecting the right connectors for the right applications is of utmost importance. ●

NEW DEVELOPMENTS IN PCB CONNECTORS

BOARD-TO-BOARD OR CABLE-TO-BOARD APPLICATIONS REQUIRE COMPATIBLE AND CONSISTENT CONNECTORS. IN THIS ARTICLE **KEVIN CANHAM** OF HARTING LTD EXPLAINS HOW TO MEET THESE CHALLENGES WITH NEW TYPES OF HIGHLY VERSATILE PCB CONNECTORS

Connectors need to provide compatible and consistent solutions, irrespective of where they are meant to be used: board-to-board or cable-to-board applications. The challenges presented by trends in miniaturisation, flexibility and increased data-transfer performance are significantly affecting the design of printed circuit board (PCB) connectors.

Today's devices and machines need to be extremely effective and powerful. Major systems and networks are increasingly equipped with back-up structures and controls. Machine status has to be analysed on site and controls need to be directly accessible. On-site response times are speeding up and not just in terms of human users; automated control techniques such as camera inspection are increasingly accessing processes independently on a continuous basis – in real time, if possible.

In view of this situation, components and machines need to be equipped with increasingly intelligent and rapid control elements. Data-transfer rates within the device need to be as fast as those for the external receiver, especially for the demands of image processing. Central control systems must be supplied with sufficient levels of data and information.

New Design Concepts

Technology trends in the industrial and consumer sectors are extremely diverse. Miniaturisation is a central factor: smaller and smaller chips with higher levels of performance make it possible to produce increasingly compact device designs, which has resulted in traditional design configurations being dispensed with; circuit boards are not only getting smaller, but the rigid layout is also disappearing.

In spite of the different ways and the different sectors in which they are used, modern industrial devices are often designed into the same housings to save costs. Functional differentiation is achieved through the structure and composition of the devices themselves. Built-in components, and mainly connectors, therefore need to be even more flexible, so they can be inserted without changing the interfaces in any fundamental way. Modularisation and user-friendly components mean that a great number of variants of the same device are now possible.

When industrial controllers were just being introduced, the focus was on freely available, non-specific connectors. Consequently, connectors based on the DIN 41 612 standard formed the foundation of the rack systems standardised in IEC 60297. Product designers departed from these very open architectures in the second generation, which were based on proprietary control units with backplanes used for the I/O plug-in units.

In a further evolutionary step, the classic rack was replaced, and the manufacturers created individual modules without plug-in frames. These individual interconnected modules were plugged directly into a controller without a rack and backplane. The connectors were created in connection with specific solutions that were optimally adapted to the interconnection method and were implemented as an integral part of the automation modules.

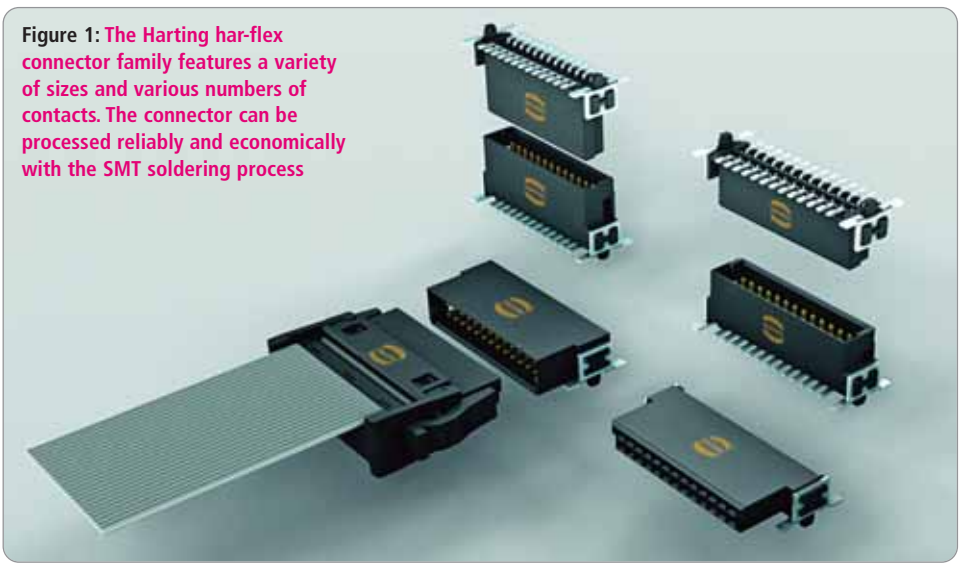

Figure 1: The Harting har-flex connector family features a variety of sizes and various numbers of contacts. The connector can be processed reliably and economically with the SMT soldering process

New Generation

Now a new generation has arrived in interconnection technology for industrial controllers, because the existing proprietary connectivity solutions are neither profitable nor technologically suitable to meet more stringent requirements. This trend is typified in the range of connectors illustrated in Figure 1. This product range uses surface-mount termination technology, and is based on a 1.27mm grid. With its

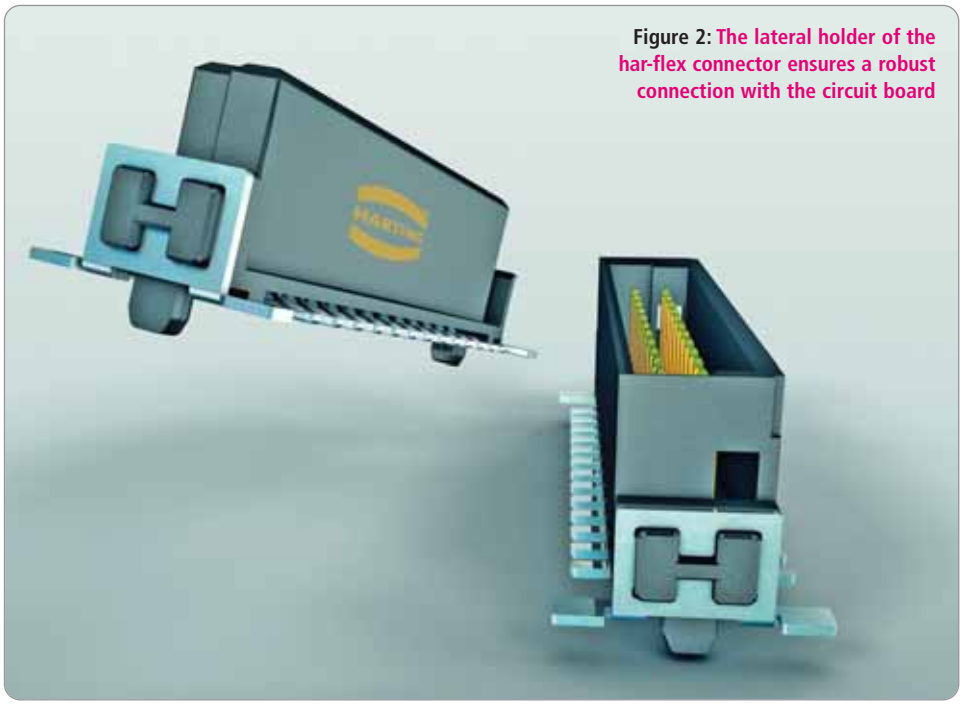

Figure 2: The lateral holder of the har-flex connector ensures a robust connection with the circuit board

diverse selection of straight and angled variants, it provides connectivity solutions for many different board-to-board and cable-to-board applications. For example, two straight connectors are used for a mezzanine application, two angled connectors are used for PCBs on one level, and a combination allows the well-known pairing of mother and daughter cards. By using an insulation-displacement cable connector, two PCBs separated by a large space can be connected with a flat ribbon cable.

The use of ribbon cables makes it possible to create a wide range of board layouts in the device. Developers even have the freedom to produce new housing designs, as the previous layout and its rigid right angles no longer apply. All these connectors can be freely combined and adapted to the housing. This approach is particularly suited to devices fitted with a man-machine interface where, depending on the configuration, displays and pushbuttons must be flexibly combined with the board.

Flexibility is further enhanced by a modular tooling concept which offers a broad choice of configurations between six and 100 poles in even-numbered positions. This flexibility in the choice of number of contacts, combined with high-density contact spacing, allows the designer to maximise the use of PCB real-estate, thereby achieving overall space savings and cost efficiencies.

The result is a general-purpose PCB connector series for both internal and external device connectivity. The continuous scalability forms an ideal basis for customised applications, since the connector can always be optimised to suit specific applications on the device PCB, while also covering the medium- and small-scale volume range that is typical for the production of industrial devices. This flexibility results in an individual design being turned into a standard component. No special tooling changes are needed for customer-specific solutions, resulting in much shorter delivery times.

Mezzanine applications are catered for with a range of straight versions for four different stacking heights that can be used to interconnect PCBs arranged in parallel stacks with spacings of between 8.0mm and 13.8mm. Additional stacking heights are in development. For applications requiring larger spacing between boards, compatible cable-to-board connectors are available using insulation displacement technology.

> Contact quality, which is crucial for a connector, is tested in mating cycle tests; first the male and female connectors are inserted and withdrawn 250 times; then after ten days another 250 mating cycles are conducted

Data and information consistency plays a central role in an increasingly automated and Ethernet-dependent world, and these connectors meet the requirements for the latest transfer protocols such as Gigabit Ethernet and PCI Express, and can be fitted in both switch cabinets and mobile devices. Data transfer rates of up to 3.125Gbit/s are easily achievable.

Process Compatibility

The SMT fixing on these connectors ensures a robust and enduring connection to the PCB and helps to absorb mechanical stress on the solder contacts resulting from insertion and removal forces. The connectors meet the highest demands in terms of their processing capabilities. Special blister packaging provides protection during shipping and handling, while the “pick and place” pads enable automated assembly of the PCBs. The temperature resistant materials of the insulating body, in combination with consistent testing of the co-planarity of contacts, ensure reliable soldering in the reflow process.

The connectors also pass the vibration and shock tests that provide information about connector reliability for applications in the direct vicinity of heavy machines. In these tests, connectors are exposed to sinusoidal oscillation up to 20g acceleration and to individual shocks up to 50g. No contact interruption lasting more than 1µs occurs. The connector owes its high level of mechanical stability to the lateral hold-downs that guarantee a secure hold to the board.

Contact quality, which is crucial for a connector, is tested in mating cycle tests. First the male and female connectors are inserted and withdrawn 250 times. After ten days of storage in a highly concentrated and corrosive gas mixture, another 250 mating cycles are conducted. No significant rise in resistance is

permitted at any time during the test phase.

A very smooth surface in the contact area ensures that wear during mating cycles is minimised, so that the contact coating is preserved. The smooth surface results from the use of a special stamping method that simultaneously rounds and smoothes the contact surface.

Despite the fact that connectors are rarely mated so many times in actual use, these tests shows what these products can stand up to in industrial applications. Some examples of other tests are the endurance load with current and heat (1000h at 70°C), as well as moisture and temperature change tests. This functionality is also maintained in use with plug-compatible products from other manufacturers.

Wire Connection

Connecting industrial equipment with printed circuit boards through a single, flexible wire connection is a primary requirement in modern equipment technology. The application area of PCB connection technology must continue to be universal for the on-site connection of sensor and actuator assemblies. Flexibility in connecting I/O signals with single wires without using tools, thus allowing field customisation, is a key requirement.

There is currently a trend towards standardising the handling of components on printed circuit boards that function as the central component of industrial equipment. While components such as capacitors and integrated circuits (IC) are mounted on the PCB with surface mount technology, the connection technology on the PCB is often the part wired last.

There is a need for PCB terminals that can be handled in one operation, i.e. in the same process and with the same equipment as other SMD components, and that can withstand the high loads on the surface mounted pins at the same time.

SMD PCB terminals not only permit the use of the same fully automated pick-and-place machines and re-flow soldering systems as conventional SMD components; they also guarantee the highest packing densities with dual-sided population of the PCB.

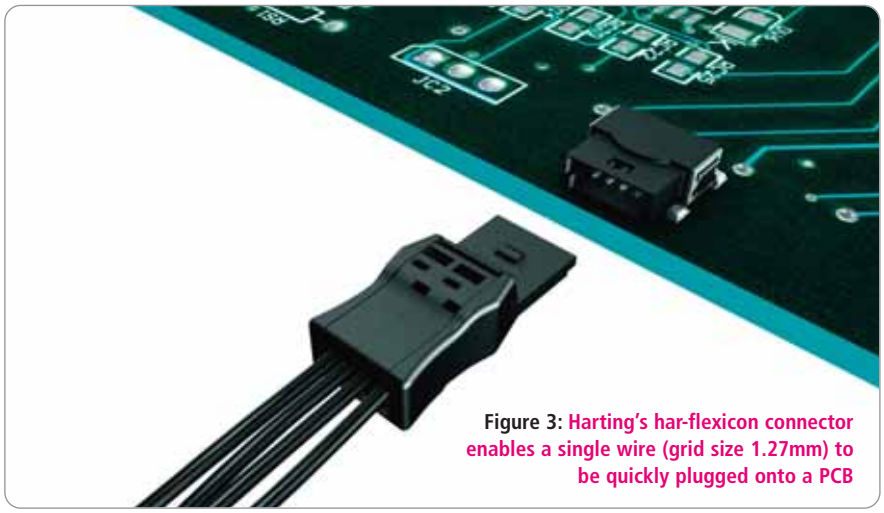

Figure 3: Harting's har-flexicon connector enables a single wire (grid size 1.27mm) to be quickly plugged onto a PCB

Figure 3 shows an innovative PCB connector technology for the connection of I/O signals in industrial equipment that satisfies all the major requirements outlined above: quick single wire connection without the use of tools for flexible working in the field; efficient surface-mount technology; miniaturised grid dimensions; and a high degree of mechanical robustness.

This 1.27mm grid device is the smallest field-installable PCB plug connector for single wires. In a miniature package, the 4-pin connector, comprising a PCB connector and a plug connector, brings all kinds of low voltages, digital/analogue I/O signals, serial sensor signals and communication signals to the PCB reliably and conveniently.

Contacts for flexible wires (AWG 28-26 or 0.05-0.14mm²) can be established without stripping the insulation, using IDC technology. The plug connector is very simple and quick to use despite its small size, and exhibits all the attributes expected of state-of-the-art PCB connectors.

The connection of single wires on-site requires no tools and is therefore very flexible. The PCB connector is designed for the SMT soldering process, and offers cost benefits in the manufacturing process through the use of standardised and automated mounting and soldering processes.

The PCB connector has a height of only 5mm measured from the upper surface of the PCB. It boasts a high level of flexibility when used in industrial equipment – the ability for field assembly means that cable lengths no longer need planning up-front in conjunction with the end-user because individual cable lengths can be tailored on-site. ●

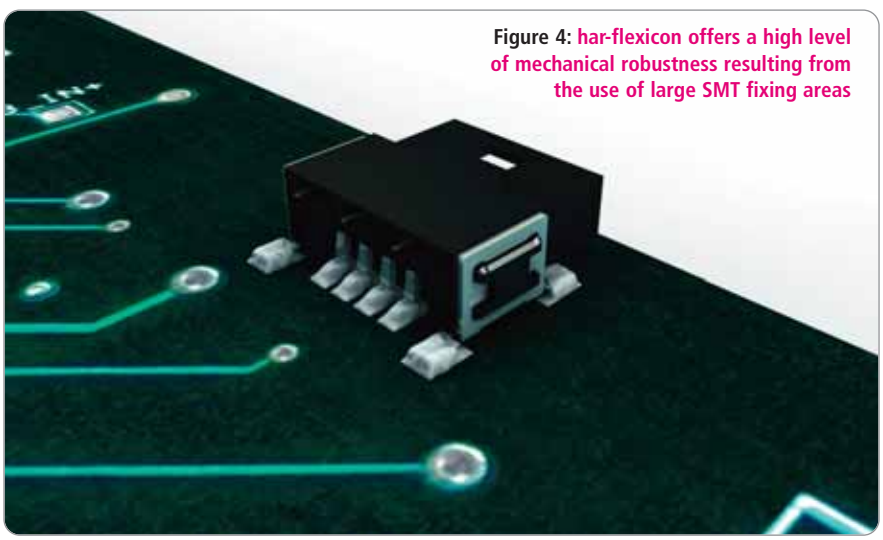

Figure 4: har-flexicon offers a high level of mechanical robustness resulting from the use of large SMT fixing areas

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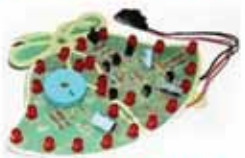

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HANNING CHEN AND **YUNLONG ZHU** FROM THE LABORATORY OF SHENYANG INSTITUTE OF AUTOMATION IN CHINA PRESENT A USED AS AN INSPIRATION FOR AN ALGORITHM THAT SOLVES RFID

Bio-inspired Algorithm for Optimal Dynamic Deployment of RFID Reader Networks

Radio frequency identification (RFID) technology is a type of automatic identification system. The purpose of an RFID system is to enable data to be transmitted by a portable device, called a tag, which is read by an RFID reader and processed according to the needs of a particular application. In recent years, an enormous amount of technical and commercial development of RFID systems has been demonstrated in many industrial applications, such as production, logistics, supply chain management and asset tracking. However, remote ad hoc deployment of wireless RFID readers poses two challenges:

- **Optimal tag coverage:** Some applications, such as RFID-based warehouse management (see Figure 1), need complete coverage only ocasionally. For such applications, using mobile readers to cover the area would be more cost-effective. But, before deploying the readers, it is necessary to answer many important questions, including: (i) how many readers are needed for providing complete coverage, (ii) where readers should be placed. This is the typical tag coverage issue.
- **Reader collision (interference) avoidance:** Reader collision occurs when co-located readers are simultaneously active. Specifically, reader collisions occur at tags situated in the vicinity of two or more readers that simultaneously interrogate tags. Such tags may be unable to correctly decode reader queries, leading to faulty reads or misreads. Figure 2 illustrates the corresponding interference location of the RFID reader networks, shown in Figure 1, which also reports the received power levels according to the path loss.

Thus, given an area to be covered completely within a period, determining the optimal placement and movement pattern of mobile readers and accurately detecting RFID tags in the presence of reader interference, is a difficult dynamic

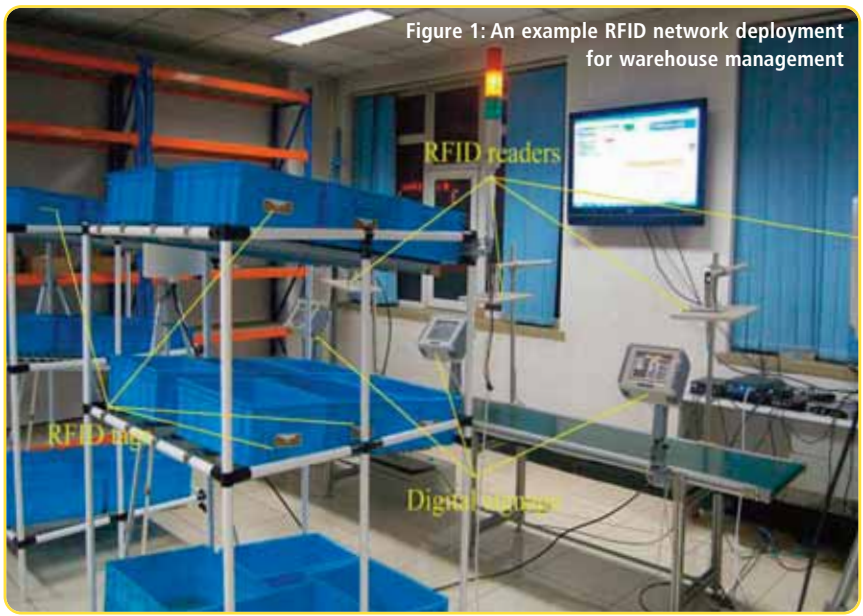
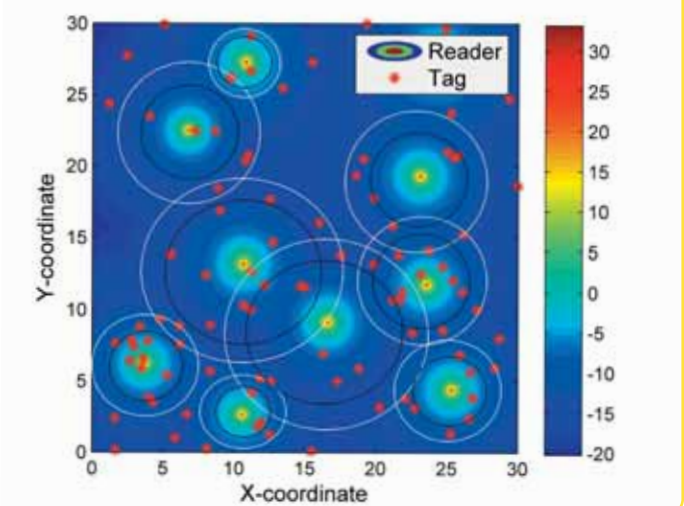


Figure 1: An example RFID network deployment for warehouse management

Figure 2: RFID reader network interference with radiated power (dBm). Black circles represent the read range, white circles the intereference range



INFORMATION SERVICE AND INTELLIGENT CONTROL AT THE RESEARCH PROJECT WHERE THE BEHAVIOUR OF BACTERIA IS NETWORK CHALLENGES

THIS NEW REGULAR FEATURE COVERS ISSUES RELATED TO CHINESE RESEARCH AND DEVELOPMENT (R&D)

optimization problem that can be formulated as:

$$f = wf_c(t) + (1-w)f_i(t), \quad w \in [0,1]$$

where f_c is the optimal tag coverage function; f_i is the interference avoidance function; t is the time step; and w is the weighting parameter.

Artificial Bacterial Foraging Optimizer

The motile bacteria such as E. coli and Salmonella propel themselves by rotating their flagella (see Figure 3). To move forward, the flagella rotate counterclockwise and the organism "swims" (or "runs"). A clockwise rotation of the flagellum causes the bacterium to "tumble" and redirect itself in a new direction. Alternating between "swim" and "tumble" enables the bacterium to search for nutrients in random directions. Swimming is more energetic as the bacterium approaches a nutrient. Tumbling, or a directional change, is more frequent as the bacterium moves away from food to search for more.

Bacterial chemotaxis (the phenomenon whereby some organisms direct their movements according to certain chemicals in their environment) is a complex combination of swimming and tumbling that helps bacteria move in their environment towards the greatest concentration of nutrients. It can also be considered as an optimization process for the exploitation of known resources, and costly exploration for new, potentially more valuable resources.

In this work, we use a recently-developed swarm intelligence search technique that mimics bacterial chemotactic behaviour, namely Self-Adaptive Bacterial Foraging Optimizer (SABFO), to solve the problems of reader collision avoidance and optimal tag coverage in RFID systems. Along with the simple description of chemotactic behaviour in the original Bacterial Foraging Optimization (BFO) algorithm, SABFO also incorporates an adaptive search strategy, which allows each bacterium to strike a balance between exploration and exploitation during algorithmic execution by tuning its run-length unit self-adaptively.

An example of a global optimization case using SABFO is shown in Figure 4, in which a bacterium can switch between exploitation and exploration states by self-adapting its run-length unit, and finally find the global optimal point (0, 0) of the multimodal Rastrigrin function. The Rastrigrin function is a mathematical function often used as a test problem for numerical optimization algorithms.

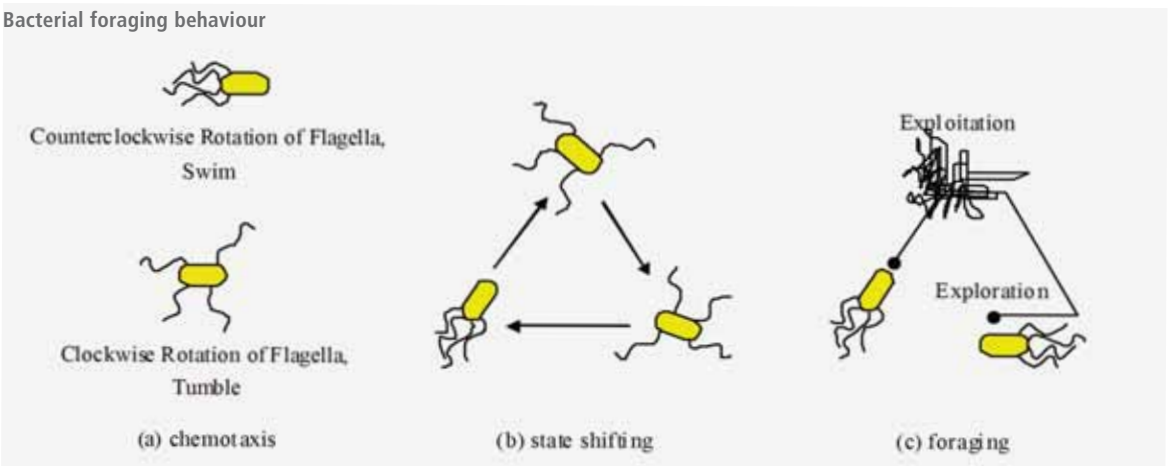
The Algorithm

The overall operating process of dynamic RFID network optimization based on SABFO can be described as follows:

(1) Initialization Phase

- **Reader specification**
  This details the number of mobile RFID readers used; their adjustable radiated power range; the respective interrogation range – the distance up to which a tag can be read by the reader; and the interference range – the distance at which the signals of two transmitting tags might interfere.
- **Topology specification**
  This gives the details of the working area to be covered by the RFID network according to the application setup.

Figure 3: Bacterial foraging behaviour



It includes the shape and dimension of the region; the number of RFID tags to be used; the tag distribution (i.e. tag positioning) in the working area; and the tag power threshold – the minimum power level needed to establish communication between reader and tag.

- **Population generation**
  Individuals forming the SABFO population should be randomly generated. Each bacterium is characterized by real number representation and has a dimension equal to 3M (M is the number of RFID readers used), 2M dimensionalities for the coordinates of reader positions (i.e. a possible network layout), and 1M dimensionalities for radiated powers of each reader (i.e. a possible network parameter setting).

(2) Optimization Phase

At the end of the initialization phase, all the information needed for the optimization phase is now available for generating the optimal RFID network topologies. The basic building blocks of this phase are:

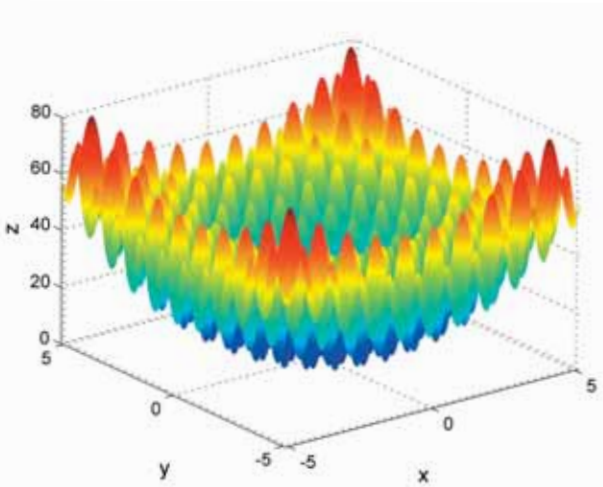
- **Fitness evaluation**
  For each bacterium, evaluate its fitness on a suitable, optimizing, objective function.
- **Population evolution**
  Compare the evaluated fitness values and perform the chemotaxis, self-adaptation, reproduction and elimination dispersal for each bacterium to update its position.
- **Termination condition**
  The computation is repeated until the maximum number of iterations is reached or desired system requirements are obtained.

Experiment Results

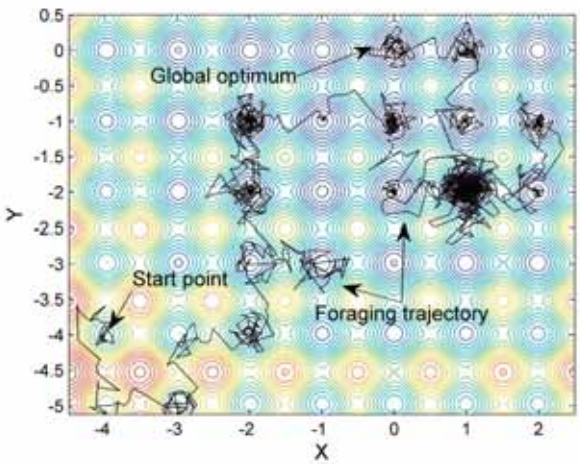
Here's a case study using SABFO, the standard BFO and a hybrid algorithm (combing BFO and particle swarm optimization) for the optimal RFID network deployment in the warehouse (see Figure 1). In Figure 5, the best fitness in a single run is plotted to demonstrate the typical optimization behaviour. As it can be seen, the SABFO is able to track the time-variant global optima of each objective functions much more smoothly and effectively.

To clearly illustrate the simulation results, Figure 6 shows several RFID network optimization solutions obtained in different time steps by SABFO for the combined objective function. In each time step, the tag distribution and the corresponding locations of ten RFID readers optimized by SABFO are shown in Figures 6a-d, which also report received power levels according to the path loss. As shown in the figure, the algorithm increases the power and concentrates the position of the readers in the regions of the working area where higher tag coverage is required; at the same time, it tries to provide sufficient limited distances between RFID readers to avoid interference.

Figure 4: Global optimization by SABFO



(a): 3D landscape of Rastrigrin function – a complicated mathematical function often used as a test problem for numerical optimization algorithms



(b): Bacterial foraging trajectories on 2D contour display

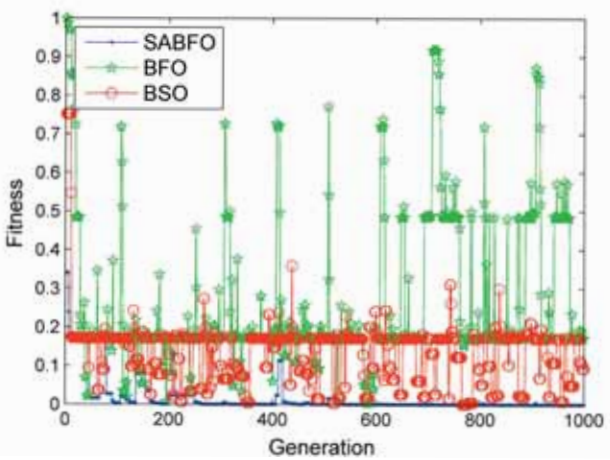
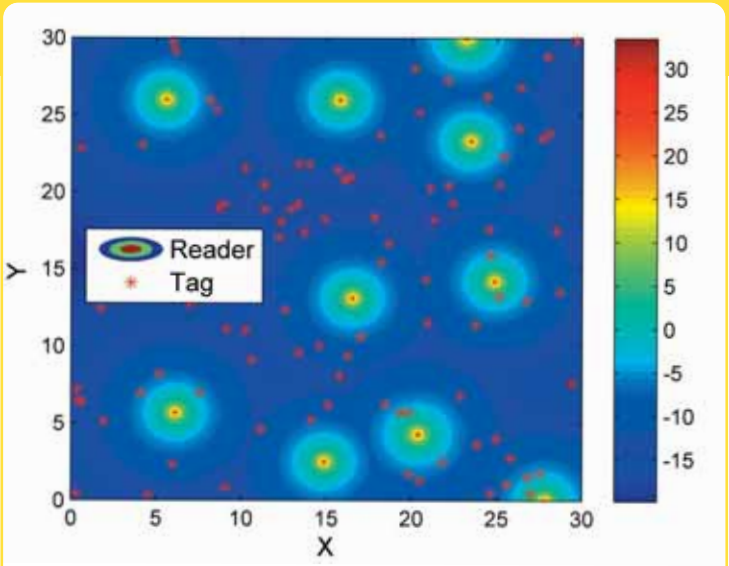
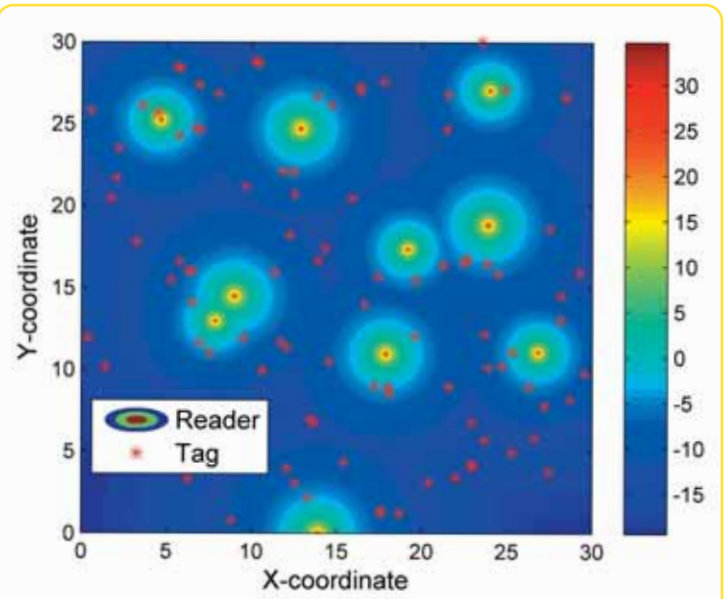


Figure 5: Best fitness in the dynamic tag environment

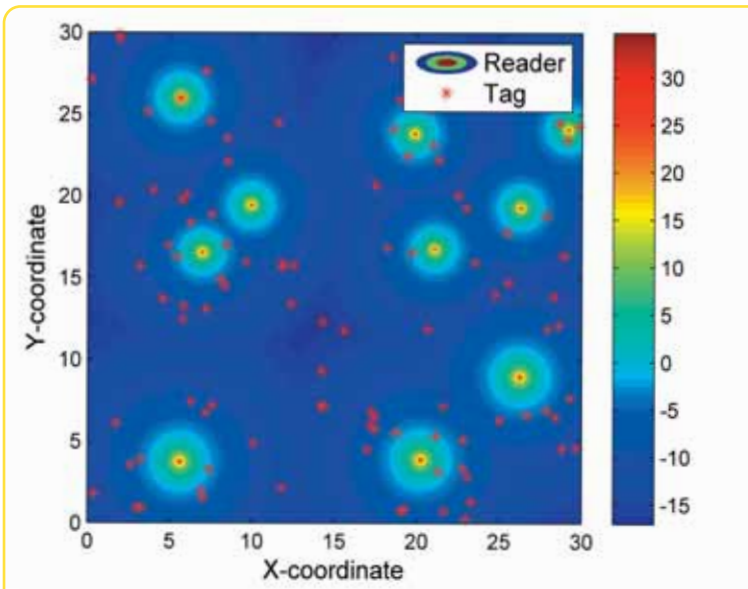


(a): t = 200

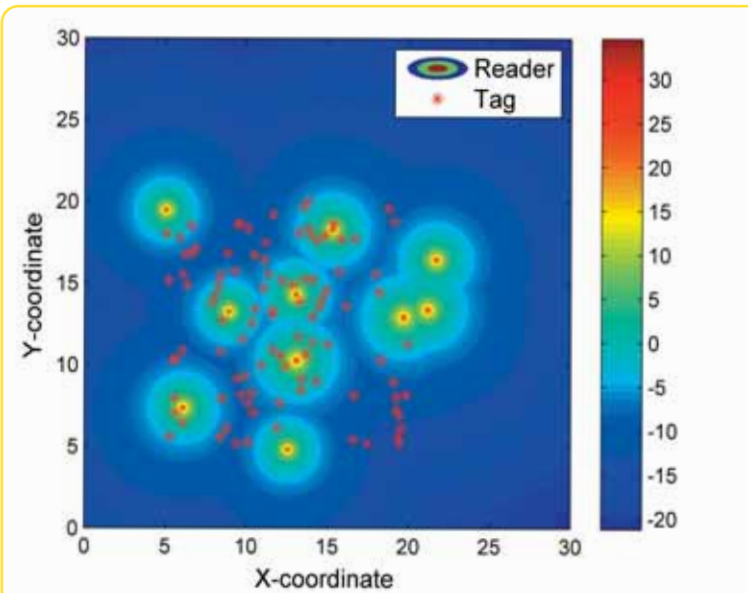


(c): t = 600

Figure 6: Dynamic RFID network deployment results in different time steps



(b): t = 400



(d): t = 800

INFO

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Got bottlenecks? Look to your memory buses!

BY **REG WALLER**, EUROPEAN DIRECTOR, ASSET INTERTECH INC

It's understandable that testing memories and memory buses have become a top-of-mind topic for circuit board test engineers. When system performance takes a nosedive, one of the first places we look for a bottleneck is the memory bus. It doesn't matter how fast the processor is; if it is bandwidth-limited due to a problem and can't get data and instructions out of memory fast enough, the system isn't going to perform the way it should.

Then, the complexity of these very fast memory buses, like DDR3 and DDR4, doesn't help matters much either. The DDR bus achieves its fast data transfer rates because a bit is communicated on both the rising and falling edges of a signal. DDR can do this because the clock signal that synchronizes the DDR signals is communicated over the DDR bus, along with data and addresses. At this level of complexity structural shorts and opens on the board are not the only causes of failed memory transfers. The integrity of the clock, data and address signals may be susceptible to temperature, jitter, noise, voltage aberrations, and other environmental conditions that tend to cause many headaches for test engineers. In addition, the DDR bus must be tuned by adjusting the parameters of the data window. But if there are defects in the manufacturing process or these limiting environmental conditions, tuning the DDR window could be impossible.

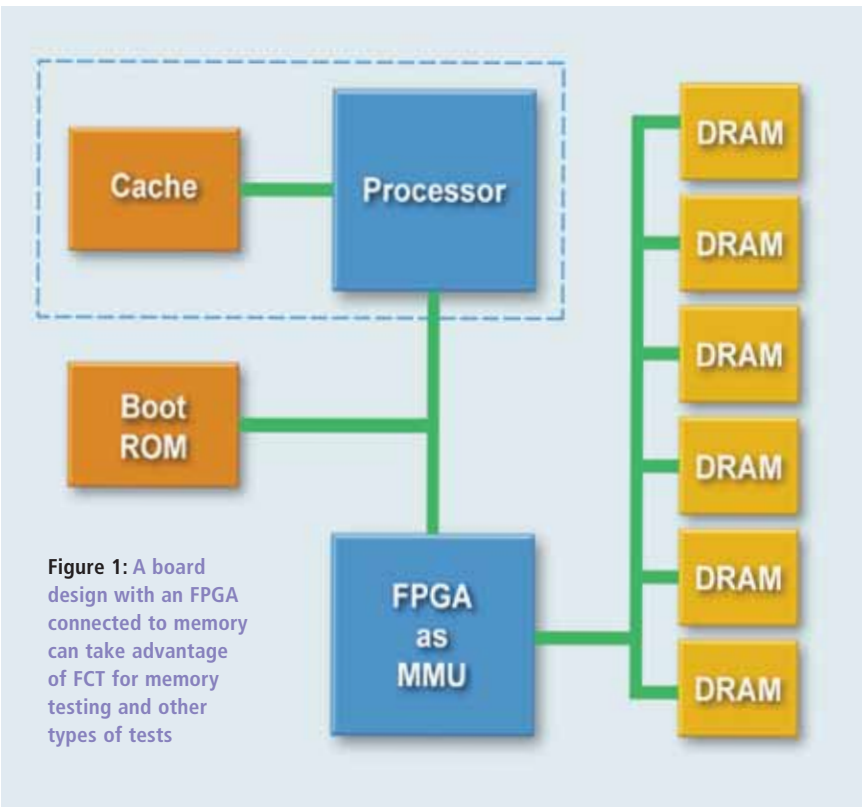

Figure 1: A board design with an FPGA connected to memory can take advantage of FCT for memory testing and other types of tests

Last month I talked about processor-controlled test, a non-intrusive processor-based method for testing memories. Another up-and-coming probeless method makes use of embedded test instruments and executes out of a functional FPGA. Once you're finished with the tests, you just remove the test instrument from the FPGA. This is known as FPGA-controlled test or FCT.

FCT involves embedding in the FPGA a number of test instruments for memory test and/or other types of test as well, such as environmental monitors. So you end up with a temporary board-tester-on-a-chip that could include memory test instruments, a flash programming instrument, pattern generators, SerDes bit error rate (BERT) instruments, monitors for bandwidth-limiting environmental conditions

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and so on. But, the sky's not really the limit, even though the capacities of FPGA have become so large.

Figure 1 shows how FCT may work on a circuit board. It works well for memory test since many circuit boards have an FPGA acting as the memory management unit (MMU) or the communications bus controller. In this architecture, the FCT tester in the FPGA/MMU has access to the memory buses and memory chips so the embedded memory test instruments in the FCT tester can assert tests onto the buses and chips.

One of the very powerful aspects of FCT is the portability of the embedded instruments, i.e. they can be re-used from one design to the next. Portability means no more re-inventing the wheel to implement another test strategy. You just change the parameters on an embedded memory test instrument to fit the architecture of the next board design.

FCT is also portable across the entire life cycle of a circuit board. Since it doesn't depend on the board having functional firmware, an FCT tester can be inserted into prototypes during early board bring-up. This helps ensure the hardware is solid before firmware and software are verified on the board. (Anything to avoid the finger pointing between the hardware and software groups when there's a problem.)

Then, later in the life cycle, the FCT tester could be used during volume manufacturing and then in the debug shop to manage manufacturing yield or to recover boards from the bone pile of non-functional boards, and even in the field to perform troubleshooting. The days of spending all that time and money to reinvent a test suite for each phase of the life cycle could truly be over! ●

DAQ System Design: Sensors And Transducer

IN THIS SERIES **MAURIZIO DI PAOLO EMILIO**, TELECOMMUNICATIONS ENGINEER, SOFTWARE DEVELOPER AND DESIGNER OF ELECTRONIC SYSTEMS, PRESENTS A TUTORIAL ON DATA ACQUISITION SYSTEM DESIGN

Data acquisition (DAQ) systems are the main instruments used in laboratory research by scientists and engineers, in particular for test and measurement, automation and so on. DAQ systems are typically general-purpose instruments suited for measuring voltage or current signals.

Transducers can be used to detect a wide range of different physical phenomena such as movement, electrical signals, radiant energy, thermal, magnetic or mechanical energy etc. They are used to convert one kind of energy into another. However, many of their output signals have to be conditioned prior to entering a board and being transformed into digital signals.

Devices with an input function are sensors, since they detect a physical event that changes in accordance to some event, such as heat or force. In turn, devices with output functions are actuators and are used in control systems to monitor and compare the value of external readings. Sensors belong to the category of transducers.

There are many different types of transducers – each with its input and output characteristics, and the choice depends on the goal of your system; for example what type of signal must be detected and the control system used to manage it (see Figure 1).

Sensors output a voltage or current signal proportional to the variation of physical phenomena being measured. There are two types of sensors: active and passive. Active sensors require external power supply to work; whereas passive sensors generate output signal without external power supply.

In various control system applications generally there is a sensing stage (for example a sensor), a conditioning stage and a processing stage. The conditioning stage manages the input analog signal so it meets the requirements of the electronics system at the processing stage. The conditioning stage can be built, for example by using an operational amplifier to amplify the signal and it can also include filtering, converting, range matching, isolation and any other processes required to make the sensor output suitable for the processing stage. The processing stage will be the analog-to-digital converter (ADC), or microcontroller (MCU) among others.

Different Sensing Devices

There are several ways of detecting temperature in use today, the most common of which are RTDs, thermocouples, thermistors and sensor ICs. The choice of which one to use depends on the application and factors such as required temperature range, linearity, accuracy, cost and features.

Resistance temperature detectors or RTDs are built using several different materials for the sensing element, such as platinum for example. Platinum is used for its high temperature rating, high stability and repeatability. However, nickel and copper can also be found in RTDs.

Thermocouples are composed of two different metals with a common contact point where a voltage is produced (mV) proportional to temperature variations. Thermistors are generally composed of semiconductor materials, and they can have positive or negative temperature coefficient. Thermistors with negative temperature coefficient are used to monitor low temperatures, of the order of 10 deg K.

Magnetic sensors are designed to respond to a wide range of

Quantity being measured	Input Device (Sensor)	Output Device (Actuator)
Light Level	Photodiode Photo-transistor Solar Cell	Lamps- LED- Fibre Optics
Temperature	Thermistor - Thermocouple	Heater - Fan
Force/Pressure	Pressure Switch	Electromagnetic Vibration
Position	Potentiometer - Encoder	Motor
Speed	Tacho-Generator	AC/DC Motors
Sound	Carbon Microphone	Buzzer - Loudspeaker

Figure 1: Sensors and transducers

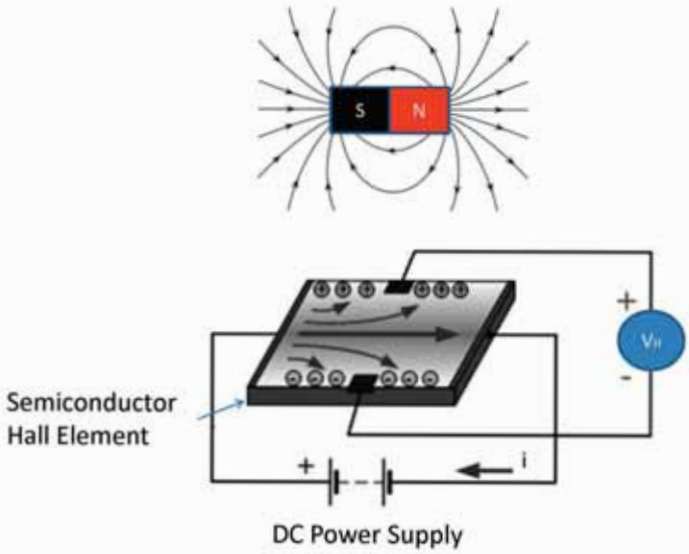
magnetic fields and are widely found in automotive applications for sensing position, distance and speed, such as the position of the car seats and seat belts, airbag control, or wheel speed detection for the anti-lock braking systems (ABS).

Magnetic sensors are based on the Hall Effect (see Figure 2), where a potential difference (Hall voltage) across a conductor is produced in accordance with the applied perpendicular magnetic field.

Most commercial Hall Effect devices are manufactured with built-in DC amplifiers and voltage regulators to improve their sensitivity, since their output voltage is rather small – only a few microvolts.

A potentiometer is an electromechanical device that contains a moving wiper arm so to maintain electrical contact with a resistive surface. The wiper is coupled mechanically to a movable linkage. The wiper and resistive surface create a voltage divider circuit when voltage is applied across the entire resistance within the potentiometer. ●

Figure 2: Magnetic field



The Southern Electronics Show

13 – 14 February 2013,
FIVE, next to Farnborough Airport in Hampshire

The Southern Electronics Show, which will be held on February 13th and 14th at FIVE (next to Farnborough Airport in Hampshire) has reached all-time high exhibitor registrations which currently stand at 750 exhibitors.

To accommodate the growing number of exhibitors, the show's purpose-built venue has been enlarged once more to an impressive 15,000 square metres – larger than three football pitches, or five halls of the NEC combined. Within the venue, visitors can expect to meet world-class companies representing every branch of industry, from electronic components, production equipment, design and sub-contract manufacturing to the latest machinery and automation solutions from firms such as Fanuc and Kawasaki Robotics UK.

The enlarged Electronics Pavilion features an extensive array of components and production equipment, from companies such as Anglia, Finder, Anixter Component Solutions, RS Components, Blundell Production Equipment and Component Force. New names for 2013 include Active Sensors, Amphenol, Blakell Europlacer, Mouser Electronics and Coax Connectors.

The show is also the pre-eminent marketplace for subcontracting and specialist engineering services of all descriptions. The European PCB industry is represented by firms such as Eurocircuits and Spirit Circuits, while companies such as Heber and Briton EMS showcase a wide variety of design and build services. New exhibitors in the Electronics Pavilion include the RJS Electronics, Paragon Electronics Group, Daniel Josefsson and May & Scofield.

In the Manufacturing area, visitors will meet many new companies alongside a comprehensive cross-section of the UK's top precision engineering firms including, Fife Fabrications, Brighton Sheet Metal, Cove Industries, Orbital Fabrications, Farsound Engineering, Muller England and hundreds of others. The show's Auto Aero zone provides a focus for firms specialising in precision engineering for the aerospace and autosport sector, represented by firms such as Aerotech Precision Manufacturing, PGT Ceewrite and TML Precision Engineering.

Free Technical Seminars

Along with the cream of UK manufacturing, the show's free technical seminar programme attracts hundreds of delegates every year. Running in two theatres over both days of the event, the seminar sessions cover a wide range of subjects, from technical issues, to business management, marketing and the latest regulatory developments. Presentations are given by leading experts, which for 2013 include companies such as the UK Atomic Energy Authority, TUV Rheinland, Bang Creations, ATOL Business Services, BobWillis.co.uk and many others.

Participation in the technical seminars, as well as entry to the show itself, is free. However pre-registration for the seminars is strongly advised as spaces are limited.

The Electronics sessions begin with a look at '*Exporting, Distributing and Selling Electrical Products*', with Sergey Putintsev and Jon Jones from international consultants TÜV Rheinland. The legendary Bob Willis will present '*Eliminating Counterfeit Components*'. Bob returns for a later session to look at '*Package on Package Design and Assembly*' – an increasingly important technique being employed in mobile, medical and military applications.

Sylvain Brand of Surface Technology International presents two sessions. In '*Continuously Improving Quality on an SMT Line*', the Lean and 6-sigma Black Belt practitioner looks at how a simple 6-Sigma approach can be effective in reducing waste. His second session, '*Increasing Output of Electronic Box Assembly*', looks at how lean principles can be applied to a production cell to achieve positive transformation in output.

Nick Wainwright, CEO of York EMC Services, examines the implications of the latest EU EMC Directive with particular reference to obligations under the '*Declaration of Conformity*'. Richard Poate of TÜV SÜD Product Service guides delegates through the requirements for '*CE Marking for Consumer Products and Professional Electronics*'. Peter Grundy of the Altus Group takes a look at the pros and cons of automation in '*To Automate or Not To Automate*'. Closing the Electronics sessions is a fascinating look at '*Fusion Means Business*' – how UK companies can win business on new fusion energy projects, delivered by Dan Mistry from the Culham Centre for Fusion Energy.

In the Engineering theatre, Tim Scurlock from Automotive Lean Consulting will look at '*Lean Concepts*' and what they mean for the practicalities of waste elimination. Bang Creations's Stefan Knox returns with an update to one of the biggest hits of 2012; '*Designing for Commercial Success and New Product Development*'. *Sergey Putintsev from TUV Rheinland presents an invaluable insight into 'Selling to Emerging Markets'*, in particular the BRIC countries and the Middle East.

David Kilroy from Manufacturing Insights will examine Best Practice and World Class Manufacturing. Mike Harrison from ATOL Business Services will look at Supply Chain and SC21, while Ian McKay, former quality executive with BAE Military Aircraft will discuss Improving the Manufacturing Process. Paul Laidler of TÜV SÜD Product Service will deliver an Introduction to Machine Safety.

Visitors can keep up with all the latest news on the show blog site, http://blog.industrysouth.co.uk or by joining the Southern Manufacturing

3-in-1 Connectivity Solutions From Weidmüller

On Stand No K46 at SME 2013, Weidmüller will be displaying three functions in one with its Omnimate Power SV/BV 7.62HP Hybrid for power, signals and EMC.

OMNIMATE Signal - Universal device feed-through connector: For extra convenience and cost savings during installation, this lockable device feed-through connector is not dependent on the pole count of the connector and can be quickly installed without any tools.

OMNIMATE Signal - 3.81: With 17.5A instead of 8A, the connectors feature more than twice the current-carrying capacity possible with previous standards, giving 100% more energy without de-rating at ambient temperatures up to 65°C.

OMNIMATE Signal – LSF-SMD 3.5/180: The 3.5mm pitch and the wire outlet direction of 180° allow a high packing density with a maximum wire cross section of 1.5mm².

http://tinyurl.com/d6gn75r
Stand K46

Video of Kikusui PCR-M Range Available at Telonic

New demo videos of Kikusui's PCR-M-series flexible AC power supplies with advanced variable frequency capabilities is now available from Telonic Instruments Ltd. PCR500M, PCR1000M and the PCR2000M deliver greater flexibility – 40Hz through 500Hz 0-270VAC – with DC offset capabilities. Aimed at engineers building system/component reliability for development, production and test applications up to 2000W where reliability, precision-setting and measuring of variable AC power/frequency is critical to success.

Kikusui's advanced feature-set extends the simulation/testing of mains, EMC, margin test, aviation and automotive testing applications, all with settable protection limits, high accuracy plus frequency to 0.1Hz resolution. PCR-M frequency converters all come complete with RS-232C interface plus control and logging software.

www.telonic.co.uk
Stand C25

UK Launch An Innovative Continuous Motion System

The new HepcoMotion PRT2 "1-Trak" continuous motion system gives designers complete freedom in 2D bearing track design. It allows every conceivable configuration to be realised, far exceeding the scope of traditional technology that is limited to simple combinations of straight lines and curves.

The HepcoMotion "1-Trak" system is manufactured from a single piece of material, and provides exceptional strength and accuracy. Resultant systems are seamless and free running with no possibility of misalignment during installation or in service. Smoother, quieter motion is also achieved.

In addition to facilitating a high degree of flexibility in track configuration, the unique three-bearing geometry, combined with the track shape, ensures that the carriages exhibit zero play.

www.hepcomotion.com
Stand T36

40W DC/DC Converters For Railway Applications

Powersolve announces the TEN-40WIR Series of high performance DC/DC converters that provide 40W from a 2 x 1 x 0.4in metal package. Approval to EN50155 allows the new converters to be used in railway applications, while an ultra-wide 4:1 input voltage range (up to 160VDC), coupled with typical efficiency levels to 90% and adjustable output voltages make the new converters suitable for a wide range of applications.

There are 21 models in the range with output voltages ranging from 3.3 to ±15VDC adjustable by external resistor. All models are housed in a
6-sided shielded metal case with an insulated baseplate.

Manufactured by Traco, TEN-40WIR converters meet the EMI requirements of EN 55022 Class A and feature short circuit protection, thermal shutdown and remote on/off. I/O isolation is 1500VDC and operating temperature range is
-40°C to +85°C.

www.powersolve.co.uk

NXP LPC800 LPCXPRESSO BOARD AVAILABLE FROM MOUSER

Mouser Electronics is stocking and shipping the NXP Semiconductors's LPC800 LPCXpresso board, based on the new 32-bit LPC800 microcontroller family designed for the 8-bit microcontroller market. The full-featured IDE-based software development tool, NXP LPCXpresso, supports the complete product design cycle for the LPC800, easing the transition to 32-bit architectures. Based on an ultra-low-power 30MHz ARM Cortex-M0+ processor, LPC800 MCUs are designed specifically for the 8-bit world and offer deterministic, real-time performance.

Featuring easy-to-use, innovative peripherals such as a flexible switch matrix and a state configurable timer, the LPC800 introduces a new level of flexibility without adding complexity. To learn more about NXP LPC800 MCUs and the LPCXpresso Board, visit:

http://uk.mouser.com/nxp-lpc800

HIGH TEMPERATURE THERMAL FUSES

Above 200°C conventional thermal fuses are relatively unreliable, especially if the working temperature is close to the fuse operating temperature. Above 240°C they are not even available, so the intelligent solution is to use the PEPI H-8 high temperature thermal fuse.

Using unique bimetal technology, the PEPI H-8 one-shot thermal cut-off can be supplied with calibrations from 250°C to 280°C and happily works up to 20K below its opening temperature without detrimentally affecting the fuse life. Once the PEPI H-8 has tripped it will not reset again even in ambients as low as
-35°C.

The H-8 has a switching capacity of 10A/250VAC (or 15A/125VAC) and provides the ultimate in over-temperature protection for home appliances and industrial products. It is approved by C-UL and TüV and is available with a variety of terminal options to suit specific applications.

www.atcsemitec.co.uk

NEW ANGLED DUO M12 CABLES IMPROVE DESIGN FLEXIBILITY

The extensive range of Binder moulded connecting cables has been enhanced with the introduction of new angled, duo-connecting cables that have a four-pole, right angle, male M12 duo connector moulded to two PUR cables each terminated with a moulded, straight three-pole M8 or M12 female moulded connector.

This allows users to transfer two signals via one M12 connector and is ideal for machine applications with limited space. IP67 when mated these cables will be particularly useful in application areas such as drives, controls, sensors and automation equipment.

With a current rating of 4A and a voltage capacity of 60V for M12 to M8 and 250V for M12 to M12, these new connectors have a PUR connector body and cable jacket and have gold plated contacts that provide over 100 mating cycles. Standard cable length is 1m but other lengths are available on request.

www.binder-connector.co.uk

AEL Crystal Oscillators Can Be Used With Infineon RKE Chipsets

AEL Crystals has announced that its devices have been approved for use with a wide range of Remote Keyless Entry (RKE) chipsets supplied by Infineon from its wireless control product portfolio.

The AEL Crystals devices recommended for use with Infineon RKE chipsets include 15 transmitter and 15 receiver crystal oscillators covering the 315, 434.2, 868, 868.4 and 915MHz frequency bands, together with five variants for transceivers covering the 315, 434.15, 868.3 and 915MHz frequency bands.

These devices offer an adjustment tolerance of ±10ppm and a frequency stability of ±20ppm across the temperature range of -40 to +85°C. Ageing effects are between 10 and 15ppm over a ten-year span.

RKE is widely used in modern cars. A variety of key fob designs are possible based on Infineon's highly integrated SmartLEWIS MCU family, which combines the transmitter and the micro-controller on one single chip.

www.aelcrystals.co.uk

HAL FOR ADDED FLASH TO PCB TESTING

PCB manufacturers can take advantage of a fast, reliable and safe solution to meet the growing demand for flash/HIPOT tested (2kV) unpopulated boards.

Electrical safety testing specialists Clare has developed a bespoke system utilising its HAL104 instrument connected to a test enclosure, which enables the easy flash testing of PCBs during the initial production stages.

The enclosure has a conductive foam base with modular sections to accommodate different sizes of PCBs. It can have either a spring mounted probe system or a further section of conductive foam can be added to allow it to work with different types of PCBs.

The move follows the increasing US-led trend that all base PCBs must now be flash tested during the manufacturing process to ensure that they have no defects and are compliant with safety standards. This comes from growing demand among global component assemblers that all electronic components should be able to pass a flash test before final build.

www.seaward.co.uk

FUNCTION IMAGES FOR CML'S FAMILY OF DIGITAL PMR PROCESSORS

CML Microcircuits has released new function images for its successful CMX7131/7141 family of digital PMR processors.

The new function images add to the already flexible device allowing it to be used in the design of small, low-cost, low-power digital and analogue PMR radios. Thanks

to CML's innovative chipset designing a small, low-cost, low-power analogue or digital PMR (dPMR) radio has now never been easier.

When the new function image for the CMX7131/7141 is combined with a suitable host and a direct conversion (I/Q) receiver, such as CML's popular CMX994, a low-cost digital PMR radio can be realised. Through the embedded functionality of the CMX7131/7141 managing the CMX994 downconverter autonomously, host microcontroller interactions are minimised enabling the lowest operating power and longest battery life for a digital PMR radio.

The chipset presents a comprehensive dPMR solution, providing RF direct conversion with minimal external

www.cmlmicro.com

Kontron Releases Flex-ATX Motherboard

Kontron launched the feature-packed, yet highly cost-efficient embedded Flex-ATX motherboard KTA75/Flex based on the new AMD Embedded R-Series Accelerated Processing Unit (APU) and the AMD A75 controller hub. It is designed for graphics-intensive and parallel embedded computing applications and provides outstanding long-term stability and reliability.

With its integrated discrete-class AMD Radeon HD 7000 Series graphics it delivers leading edge 3D/HD graphics and accelerated processing capabilities together with the ability to drive up to four displays simultaneously, either as independent displays, or as a single large surface. This makes the long-term available Kontron KTA75M/Flex an ideal solution for applications requiring high graphics and/or parallel computing performance in markets such as industrial automation, medical, and POS/POI, digital signage as well as gaming.

Developers can furthermore utilize the up to 563GFLOPs provided by the integrated GPU to accelerate both graphics- and compute-intensive applications while using industry-standard libraries such as OpenCL, DirectX 11 and DirectCompute.

www.kontron.com

AUTOMOTIVE MULTIPLE-OUTPUT REGULATOR ICS FEATURE 2.2MHZ SWITCHING

Three new automotive power management ICs from Allegro MicroSystems Europe use an internal 2.2MHz constant on-time buck pre-regulator to supply regulated outputs commonly used in automotive CAN bus and microprocessor-controlled applications. The devices are targeted at the automotive market for bias supplies within control units for functions such as electronic power steering, transmission control, antilock braking and emissions control.

The A4407 supports four regulated outputs: a 5V linear regulator, a 5V tracking/protected linear regulator, a 3.3V linear FET controller/driver and an adjustable linear regulated output. The A4405 supports three regulated outputs: a 5V linear regulator, a 5V tracking/protected linear regulator, and a 3.3V linear FET controller/driver. The A4406 is a scaled-down version of the A4405 and can supply a 5V tracking/protected linear regulator and a 3.2V linear FET controller/driver.

www.allegromicro.com

WORLD'S FIRST RF VECTOR SIGNAL TRANSCEIVER REDEFINES INSTRUMENTATION

National Instruments introduced the world's first RF vector signal transceiver (VST), the NI PXIe-5644R, and with it a new class of software-designed instrumentation. This software-centric architecture represents a new era in which engineers and scientists can use LabVIEW to tailor open, field-programmable gate array (FPGA)-based hardware for their specific needs.

The transceiver offers up to 6.0GHz frequency coverage and 80MHz instantaneous RF bandwidth; industry-leading performance for testing the latest wireless standards such as 802.11ac and LTE; more than 10 times faster measurements than comparable solutions; and it can replace multiple traditional instruments at a fraction of the cost and size. It is built on FPGA technology programmable with LabVIEW and it easily expands to support multiple input, multiple output (MIMO) configurations or parallel testing in a single PXI chassis.

www.ni.com

IAR Systems Extends Development Tools

IAR Systems announced the availability of a new edition of the development tool suite IAR Embedded Workbench, tailored for the small ARM Cortex-M0 and ARM Cortex-M0+ cores. The ARM Cortex-M0 edition of IAR Embedded Workbench targets developers working with MCUs based on these very small and energy-efficient cores, and is offered at a considerably reduced price from that of the full version which supports all ARM cores.

Based on the full edition of the recently announced version 6.50 of IAR Embedded Workbench for ARM, support for this special edition is limited to the development of MCUs based on ARM Cortex-M0, Cortex-M0+ and Cortex-M1 cores.

During the last year, IAR Systems has added a comprehensive list of new features to its development tool suite, including a new source browser, an enhanced text editor and stack usage analysis functionality. In addition, enhancements to the optimization technology in the powerful IAR C/C++ compiler result in outstanding code execution speed.

www.iar.com/ewarm

HIGH-CURRENT OUTPUT CHIPSET FOR WIRELESS CHARGING

Toshiba Electronics Europe has announced a free positioning wireless charging chipset consisting of a high-efficiency power transmitter and receiver for charging smartphones and other mobile products anywhere on the battery charging pad.

The Toshiba chipset is fully compliant with the Wireless Power Consortium (WPC) Qi interface specification, A4, A8, A12 and A14. It includes the TB6865FG power transmitter and TB6860WBG receiver and features a two-coil control architecture for cost-effective battery charging. The position of a mobile device is detected by the TB6865FG and only one of the coils is energized for charging, thereby preserving efficiency and allowing product freedom of placement. As a result, end users can place a Qi-capable mobile product on a Qi compliant charging surface and achieve up to 74 percent better efficiency across a majority of the charging area. In addition, the design flexibility of the TB6865FG allows the control of two coils, so two mobile products can be charged simultaneously.

www.toshiba-components.com

SPARK Pro

ADACORE AND ALTRAN PRAXIS RELEASE SPARK PRO 11

AdaCore and Altran Praxis today announced the release of the SPARK Pro 11 software development and verification environment, providing a major step forward for the developers of high-assurance systems. SPARK Pro 11 offers many enhancements particularly in the area of program proof.

A number of significant enhancements have been made to the way that functions and proof functions are handled in SPARK Pro 11. These changes will improve project efficiency by eliminating the vast majority of rules that were previously manually encoded. The main changes include a more powerful language for specifying proof functions and the ability to use the functions in any proof context. This greatly simplifies the task of writing and maintaining functional contracts for critical software, providing high-assurance at lower cost.

Proof is a very powerful technique for achieving high levels of assurance in safety or security-critical software.

www.adacore.com
www.altran-praxis.com

Altera Quartus II Software Version 12.1 Now with Enhanced Design Flow

Altera announced the release of its Quartus II software version 12.1, a design suite for CPLD, FPGA, SoC FPGA and HardCopy ASICs.

The latest version strengthens the Quartus II software's high-level design environment by continuing to ease traditional hardware development tasks so users can maximize productivity while benefiting from the broad range of leading-edge capabilities of Altera devices.

Quartus II software version 12.1 bolsters its support for high-level design flows with the inclusion of an SDK for OpenCL, and enhancements to both its Qsys system integration tool and DSP Builder model based design environment.

Also included in the latest software release are several enhancements, such as a partial reconfiguration design flow, new intellectual property (IP) cores and expanded support for 28nm FPGAs and SoC FPGAs. These enhancements further enable customers' to rapidly design, implement and get to market using Altera devices.

www.altera.com

BVM ANNOUNCES STRATEGIC PARTNERSHIP WITH ASROCK

UK-based electronics hardware manufacturer and distributor BVM has secured a strategic distribution deal with global motherboard company ASRock. The landmark agreement represents an exciting opportunity for BVM to build on already impressive business performance and meet the company's ambitious growth targets.

The partnership affords exciting opportunities for both companies, as they look to enter new markets. For Taiwanese-based ASRock, the world's third largest motherboard supplier, the partnership enables it to expand its market share in the industrial PC sector. For expanding IPC distributor and development partner BVM, the relationship opens up new market opportunities, most notably in the point-of-sale (POS) and gaming sectors.

BVM Group Managing Director, Rod Clarke, said: "We are delighted to be working with a market leader like ASRock, renowned for being an innovative and forward-thinking company. We felt the synergy between the two companies was a perfect fit."

www.bvmltd.co.uk

NEW LABORATORY EQUIPPED WITH AGILENT INSTRUMENTS SUPPORTS UNDERGRADUATES

Agilent Technologies supplied its instruments to Bangor University in a £2m sponsorship programme. The Agilent-branded laboratory, located in the School of Electronic Engineering at Bangor University, will support undergraduate and postgraduate courses in electronic engineering.

"Bangor University has a world-class reputation in optoelectronics and organic electronics and it is a real privilege to be able to support this new teaching lab and the young engineers who will be learning in it," said Graham Newton, Agilent's education and research manager in Europe. "Agilent has always been committed to working with and supporting academic institutions to help develop the next generation of engineers. One of the ways we do this is by helping to equip teaching laboratories with cutting-edge instrumentation."

Agilent equipment in the lab includes 27 oscilloscopes, 25 DC power supplies, 25 digital multimeters and two precision source/measure units. The new laboratory can accommodate up to 48 students at a time.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: Laboratories are an integral part of engineering education. Good laboratories are the key requirements for advanced research and development in both, undergraduate and postgraduate courses. The new £2m cutting-edge laboratory equipment by Agilent Technologies at Bangor University will no doubt increase the teaching and research potential of this university at a time when most institutions are having financial difficulties.
Well done, Agilent Technologies!

MAURIZIO DI PAOLO EMILIO, Telecommunications Engineer, INFN – Laboratori Nazionali del Gran Sasso, Italy: Investment in undergraduate teaching laboratories means that students can learn in excellent facilities. Not much can be learned from just sitting in classes, listening to lecturers, memorizing pre-packaged assignments and providing well-rehearsed answers. Students must grasp what they are learning and in particular apply it to practice, which is helped by using an efficient laboratory.

Good learning – like good work – is collaborative and social, not competitive and isolated. Moreover, an efficient laboratory means good research at a university can be applied to industrial applications.

> Good learning – like good work – is collaborative and social, not competitive and isolated

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Agilent is one of the best known engineering companies in the world. It specializes in the development and manufacture of test and measurement equipment.
It is encouraging to learn that such a well-known international company takes part in financing high-level research laboratories and that it collaborates with universities.

The solidarity and existing bond between Agilent and the universities has a direct impact on the international influence of this company, so subsidising their engineering laboratories – by providing instruments or any other kind of aid – is an extension of that bond. In general, it is necessary to create a multiple and diversified industrial partnership and to carry out active collaborations with universities.

I also believe the effort provided by Agilent to furnish Bangor University's laboratory with equipment, and its commitment towards undergraduate and postgraduate training of engineers will reinforce the power of this company in the field of design and manufacturing of high performance test and measurement instruments. Indeed, the laboratory equipment will help train future engineers who will be tomorrow's innovators, and they will take that knowledge of Agilent's instruments into industry.

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: Companies such as Agilent are not altruistic but know how to make good marketing investments in developing future engineers and scientists, who then grow up with their instruments as benchmark standards. Accordingly, its £2m investment in undergraduate facilities at the new Poirot Laboratory will in due time produce a payback.

However, their donation of a 1.1THz PNA network analyzer (the first in Europe) to the new Roger Pollard terahertz research facility at Leeds University should in the long run be more beneficial, particularly in the new field of graphene technology, where the network analyser will allow researchers to perform on-wafer terahertz (THz) measurements of transistors, THz biosensors, magnetic storage elements, THz spin-switches and novel acoustoelectric devices. Pollard was one of the gurus in S-parameter network analysis measurement techniques. Can Bangor in the future match Leeds? I don't believe so, but I would be happy to be proved wrong, particularly if they can produce engineers of Pollard's calibre.

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector please register your interest with the Editor by writing to Svetlana.josifovska@stjohnpatrick.com

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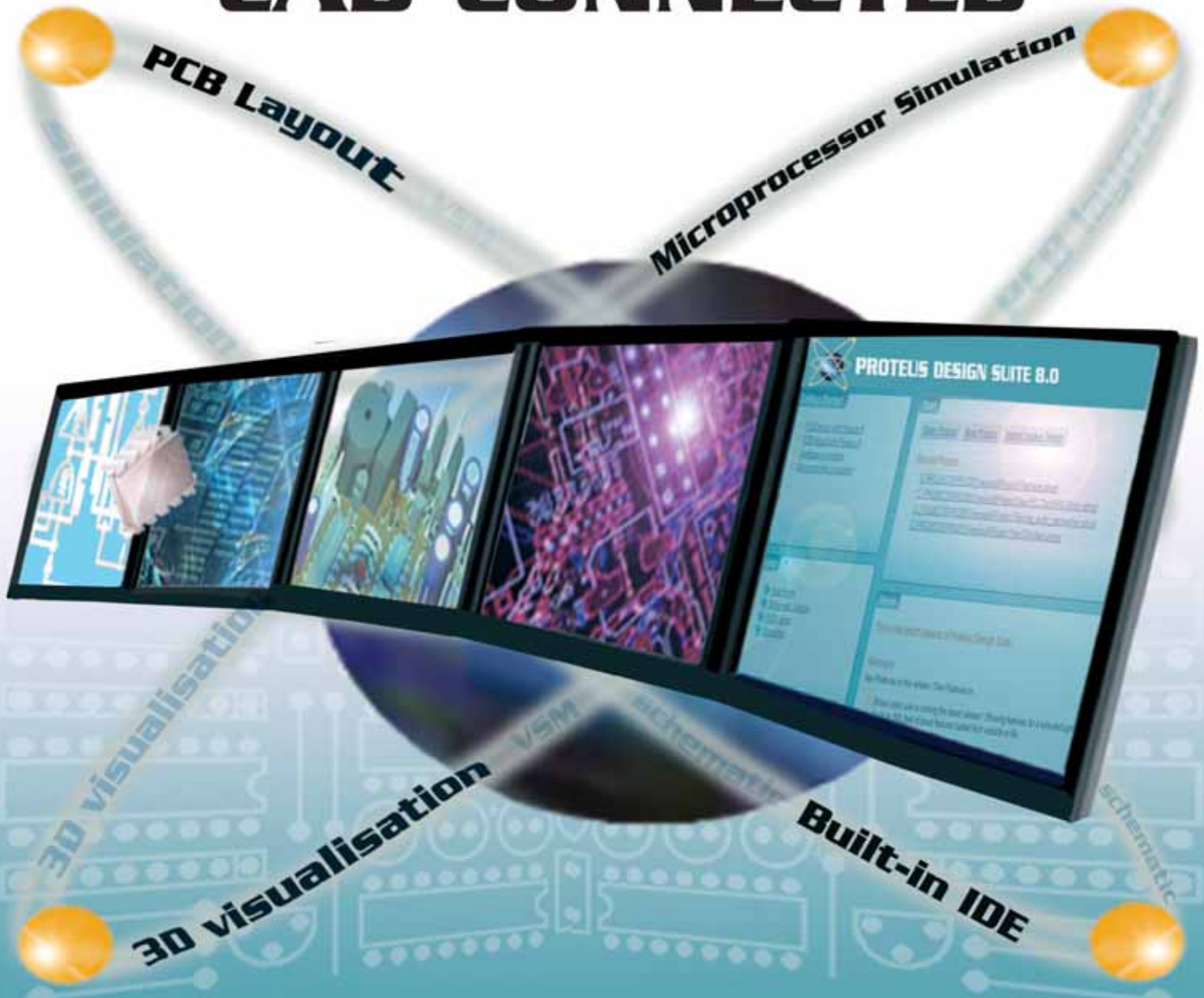

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