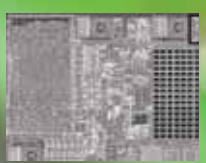
March 2013
Volume 119
Issue 1923
£5.10

Electronics WORLD

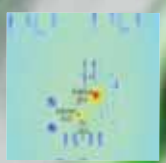
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

THE ZERO-TRANSISTOR IC, A NEW PEAK IN IC DESIGN

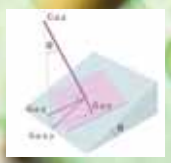
www.electronicsworld.co.uk



Special Report 1:
Filters



Special Report 2:
Power



R&D
From China

Performance Leadership in Every Possible Way

65 GHz
160 GS/s

New LabMaster 10 Zi Series – The World's Fastest Oscilloscopes

With the launch of the LabMaster 10 Zi-A Series, LeCroy further extends its technology leadership for real-time oscilloscopes and sets a number of industry firsts:

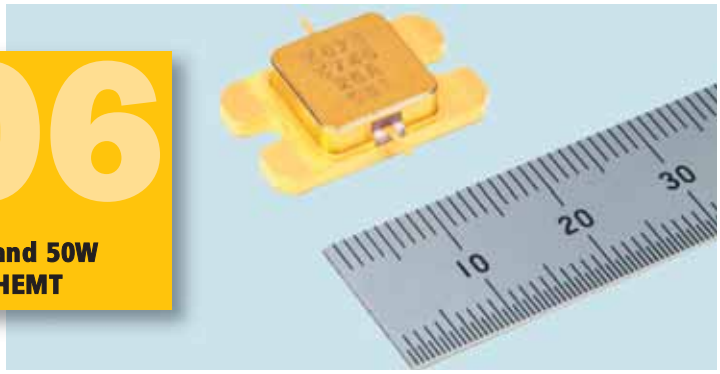
- 65 GHz Real Time Bandwidth
  up to 40 Channels at 65 GHz
  up to 80 Channels at 36 GHz
- 36 GHz 8HP SiGe Chips
- 160 GS/s Single Shot Sample Rate
- 1024 Mpts/ch Analysis Memory
- 30 GHz Trigger Bandwidth
- 100 fs_{rms} Jitter Noise Floor
- 5.2 ps Rise Time

teledynelecroy.com/europe

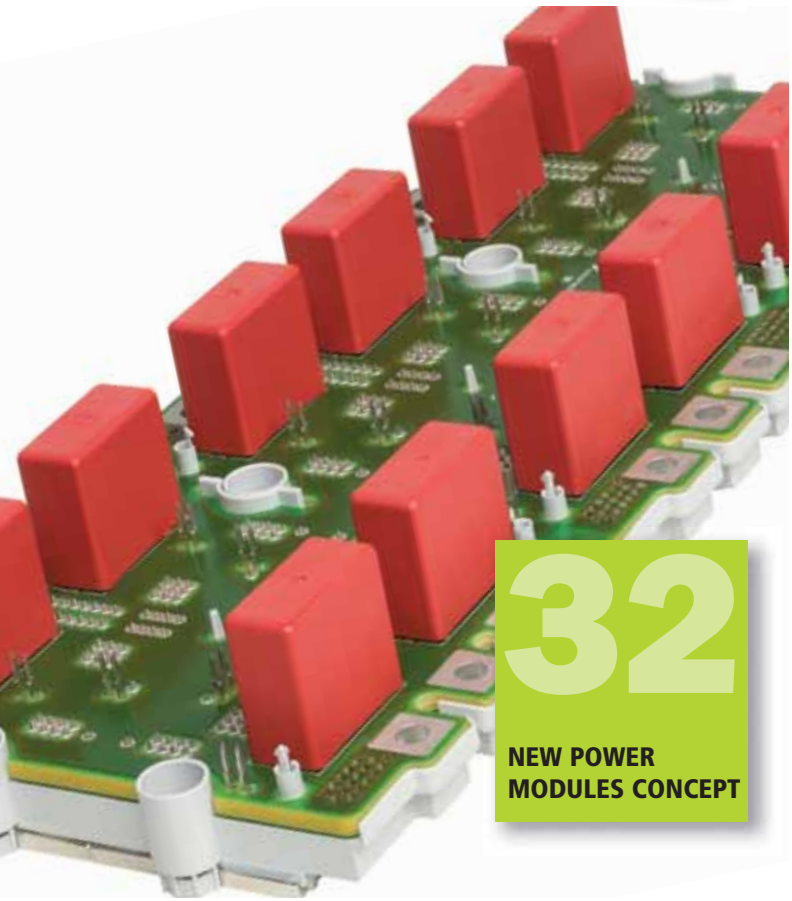
TELEDYNE LECROY
Everywhereyoulook™

REGULARS

Cover prepared by MAXIM
More on pages 10-12



06
Ku-band 50W GaN HEMT



32
NEW POWER MODULES CONCEPT

FEATURES

High Voltage Power Supplies

Bench Variable and Insulation Testing

Founded in 1956 Roband is an independent British company specialising in the design, development and manufacture of electronic power supplies. Roband is totally committed to providing the highest quality units to meet the most exacting standards. BS EN ISO 9001 2000, and BS EN 9100 accredited throughout.

RO- HV 30-1

30kV 30W, 1mA. 266 x 276 x 70mm, 2.5kg. Compact variable high voltage power supply. Polarity, factory preset. Rugged construction ideal for laboratory, test and portable applications.

roband

Quite unique in this day and age

Roband Electronics plc

Charlwood Works • Charlwood • Horley • Surrey • RH6 0BU • England

Tel. **01293 843000** • Fax. **01293 843001**

email. **postmaster@roband.co.uk**

www.roband.co.uk

OPPORTUNITY REMAINS FOR THE ELECTRONICS SUPPLIERS EVEN IN UNCERTAIN TIMES

Global developments in the consumer, computing and telecom markets, are driving increased demand in Europe for more equipment and infrastructure, which ultimately benefits manufacturers in the industrial sector

Our industry's leaders and shapers remain optimistic in the face of challenging financial conditions in the US, the ongoing European debt crisis and a slowing Chinese economy, but to some extent we're the victim of our own success. The semiconductor industry in particular has always promoted demand for innovative new products by driving down costs through greater integration and economies of scale and, despite a general slowing of silicon scaling technology, customers are still finding it hard to resist purchasing the new consumer electronic products on offer.

China has benefitted from the huge growth in demand for the latest smartphones and tablet technologies, but weaker than anticipated global consumer demand has significantly reduced overall electronic components' market growth in China from historical norms of 8% to 10% growth to less than 5% in 2012. In Europe it's the industrial, automotive and aerospace markets that continue to drive business, even though the last ten years' EU consumption, in comparison to the rest of the world, has declined from around 22% to 13%. However, the strength of European designs in the automotive electronics, industrial automation, aviation and healthcare sector, to name a few, remains unchanged, with production in Europe focused on and geared toward these markets.

This general optimism was reflected in the Manufacturers' Authorised Distributor (afdec) group market forecast released by the Electronic Components Supply Network (ecsn) late last year. Analysis of the consolidated returns from the association's membership indicate that the UK and Ireland electronic components market will be flat in 2013, with members anticipating growth to return in the second half of the year, some three months later than the association forecasted in 2011. According to ecsn/afdec chairman Adam Fletcher, last year's decline in the UK/Ireland electronic components markets continued a quarter beyond the association's expectations, but he and his members can see light at the end of this particular tunnel: "Returns from our members forecast that the UK/Eire electronic components markets will continue to improve sequentially throughout 2013."

Global developments, for example in the consumer, computing and telecom markets, are driving increased demand in Europe for more equipment and infrastructure, which ultimately benefits manufacturers in the industrial sector. In line with most of the electronics industry ecsn members are beginning to conclude that uncertainty has become the 'new normal' and along with their supply network partners are adapting their systems and processes to cope with greater dynamic change.

Fletcher believes that the main growth potential for European electronic components distributors in 2013 will probably come from value creation, customer design support, modular solutions and solutions developed in conjunction with integrated circuit manufacturers which he says: "most forward-thing distributors already include in their portfolio".

But Fletcher concluded with a cautious note: "The current extended period of weak demand has resulted in a continued inventory correction right across all global electronic components markets. The lead times for modest volumes of most electronic components are currently less than four weeks, however with many manufacturers reducing spare production capacity it may take some time to bring mothballed capacity back on-line if stronger than forecast growth returns."

EDITOR: Svetlana Josifovska
+44 (0)1732 883392
Email: svetlanaj@sjpbusinessmedia.com

DESIGN: Tania King
Email: taniak@sjpbusinessmedia.com

DISPLAY SALES: John Steward
Tel: +44 (0)20 7933 8974
Email: johns@sjpbusinessmedia.com

SALES EXECUTIVE: Orla Cullen
Tel: +44 (0)20 7933 8999
Email: orlac@sjpbusinessmedia.com

PUBLISHER: Wayne Darroch

ISSN: 1365-4675

PRINTER: Pensord Magazines & Periodicals

SUBSCRIPTIONS:
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com
SUBSCRIPTION RATES:
1 year: £56 (UK); £81 (worldwide)

SJP business media

Follow us on Twitter @electrowo

Join us on LinkedIn http://linkd.in/xH2HNx

HIGH-SPEED ATOMIC FORCE MICROSCOPY ENABLES MOVIE-MAKING ON THE MOLECULAR LEVEL

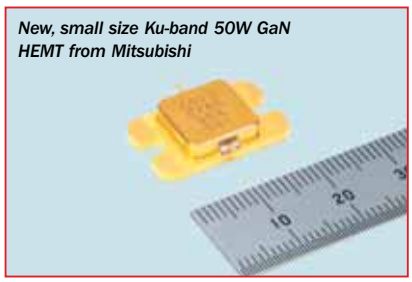
High-speed atomic force microscopy (HS-AFM) is providing the means to produce dramatic footage of moving biomolecules for the scientists at Kanazawa University in Japan.

Toshio Ando and co-workers at the University have developed and used HS-AFM to increase the understanding of several protein systems through microscopic movies of unprecedented spatial and temporal resolution. To produce an image, HS-AFM acquires information on sample height at many points by tapping the sample with the sharp tip of a tiny cantilever. Depending on the application, this might involve recording the amplitude and phase of oscillations, or the resonant frequency of the cantilever.

Ando and co-workers have used very small cantilevers that allow 10 to 20 times the sensitivity of larger, conventional cantilevers. The methods have enabled the team to record cargo-carrying proteins 'walking' on cell filaments, the rotational motion of motor proteins that provide energy in cells, and the hydrolysis of cellulose.

Copies of the team's home-made apparatus are now commercially available through the Japanese manufacturer Research Institute of Biomolecule Metrology in Tsukuba.

Mitsubishi Electric Develops Ku-band 50W GaN HEMT



New, small size Ku-band 50W GaN HEMT from Mitsubishi

Mitsubishi Electric has developed a gallium nitride (GaN) high-electron mobility transistor (HEMT) Ku-band (12-18GHz) amplifer, ideally suited for satellite earth stations. The MGFK47G3745, featuring industry-leading output power of 50W, linear gain of 9dB and power-added efficiency of 30%, is expected to halve the number of high frequency amplifiers used in power transmitter equipment and contribute to greater power savings.

Satellite-based communication, especially in the Ku-band, enables communication to be established under adverse conditions, such as during natural disasters, and in areas where communication facilities are hard to build. Mobile Earth-based stations require in-vehicle portability and must be easy to install, so power-saving measures and smaller power transmitters are highly useful in helping to minimize the size of Earth stations.

In recent years, gallium nitride (GaN) amplifiers have increasingly replaced gallium arsenide (GaAs) amplifiers in microwave transmitters. This is down to their high breakdown voltage, power density and saturated electron speeds.

Going forward, Mitsubishi Electric expects to expand its catalogue of Ku-band satellite Earth stations.

Advantages of The GaN HEMT Ku-Band Amplifier

High output power, efficiency and gain

- High output power of 50W at 24V high-voltage operation
- High power added efficiency of 30%, 10 points greater than the predecessor MGFK44A4045 model
- High linear gain of 9dB achieved with new high-voltage gate structure and optimized layout

Low Distortion

- Output power meeting 3rd-order Inter Modulation (IM3) = -25dBc of 43dBm
- Internally impedance-matched

Samsung And Synopsys Collaborate To Achieve First 14 Nanometre FinFET Tapeout

The long-standing collaboration on FinFETs between Synopsis and Samsung has achieved a critical milestone with the successful tapeout of the first test chip on Samsung's 14LPE process.

The FinFET process offers significant power and performance benefits compared to the traditional planar process, but the move from two- to three-dimensional transistors introduces several new IP and EDA tool challenges including in modeling. So, the multi-year collaboration delivered the basic modeling technologies for 3D parasitic extraction, circuit simulation and physical design-rule support of FinFET devices.

"FinFET transistors can deliver lower power consumption and higher device performance, but they also bring tough challenges," said Dr Kyu-Myung Choi, vice president of System LSI infrastructure design centre at Samsung Electronics. "We chose Synopsys as our FinFET collaboration partner to solve these challenges, because of our successful history together developing 20nm and other nodes. We continue to pool our expertise to deliver innovative FinFET solutions."

The two companies worked closely to develop a test chip that validates Samsung's advanced 14nm FinFET process, as well as Synopsys's DesignWare Embedded Memories, using Self-Test and Repair (STAR) Memory System solution from Synopsys. The test chip enables correlation of the simulation models to the FinFET process and contains test structures, standard cells, PLLs and embedded SRAM. The memory products include high-density SRAM designed to operate at very low voltages and high-speed SRAM to validate the process performance.

First Secure Microcontroller Based On Novel Magnetic Logic Unit is Out Now

Magnetic Logic Unit (MLU) developer Crocus Technology has developed the first in a category of SIM and secure element microcontrollers for mobile payments, access control, tag reading and other applications needing enhanced security and faster performance. The device, with part number CT32MLU, is based on the MLU technology, a rugged CMOS-based magnetic technology which by its nature offers advanced embedded security.

Crocus Technology's MLUs read and write ten times faster than Flash memory. Their footprint is much smaller and the CT32MLU is among the first microcontrollers offering 1.2Mbyte of memory to meet the nano-SIM format, which is 40% smaller than the current micro-SIM format. Applications include smartcards, smartphones and other embedded applications where security is of critical importance.

"CT32MLU breaks the barrier of traditional non-volatile memory that will provide smartcard makers with best-in-class secure element microcontrollers with a much smaller footprint," said Alain Faburel, VP security business unit at Crocus Technology.

According to the company, the CT32MLU1200 is the first in the CT32MLU family, and complies with the highest industry quality and security standards. With its fast read and write speeds the family enables optimized personalization and over-the-air updates. These are important since the chips will be used in NFC-enabled smartphones that need to support many applications.

Crocus will first make the CT32MLU1200, a 1.2MByte SIM and Secure Element, available in both SIM and embedded formats. The development kit is available now.

Snapshot of Crocus Technology

Crocus Technology provides secure microcontrollers for the mobile and security industry using its Magnetic Logic Unit (MLU) technology, which is CMOS based, and with read and write cycles ten times faster than that of Flash memory.

The company was founded in 2006, led by a senior management team formerly from Motorola, AMD, Intel and Gemalto. Its offices are in Santa Clara, US, and Grenoble and Gardanne in France.

In 2011, Crocus achieved two milestones: a joint development agreement with IBM to further advance the MLU architecture, and a joint venture with Rusnano, called Crocus Nano Electronics (CNE), to build and operate an advanced manufacturing facility for magnetic semiconductors.

Loophole

MYK DORMER IS A SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
WWW.RADIOMETRIX.COM

Most ISM band wireless users are at least superficially familiar with the generic European EN300-220 specification for low power radio devices. Take a brief scan of this document and it turns out that receiver specifications fall into three defined categories, depending on what level of reliability and resistance to interferers is needed. The toughest of these is Category 1 defined as: "Highly reliable SRD communication media; e.g. serving human life inherent systems (may result in a physical risk to a person)."

To this end Category 1 defines minimum receiver spurious rejection and blocking levels, which in turn can be considered as representative of the device's ability to resist the effect of interfering signals, both in and out of band. For a typical 25kHz channel spacing device, the limits set are 54dB for adjacent channel rejection, 60dB for spuri and 84dB for blocking. It's easy to write down, but the obvious question is: What do these numbers mean?

"Adjacent channel" refers to rejection of a signal in-band in the next usable channel; in our example 25kHz above or below the wanted carrier. This is usually an emission from a similar device to the one being measured, as it is in the same band.

"Spuri" is a much broader church. It refers, in this case, to the device's specific vulnerable spot frequencies; "image" and "half IF" responses. Without going into a lot of wireless design theory, these responses should be thought of as consequences of the radio architecture. There are usually only two or three specific spot frequencies where an interferer can produce a spurious response.

"Blocking" refers to the radio's ability to reject signals well away from the wanted channel (2MHz or more) but which don't fall into the "spuri" class. These interferers are out-of-band signals and can be very strong, for example broadcast or cellphone transmitters, so blocking rejection is sensibly required to be much higher than adjacent or spuri. Unfortunately, to the user the preceding paragraph is of little use. A better question would be: What is the impact on a practical system of these specifications?

> *This is madness, and as part of a specification which by its own definition is "serving human life inherent systems", it is dangerous madness*

It's all about relative distances. How close can an interfering unit be located to your system's receiver before the performance claimed in the data sheet – and possibly demonstrated in "clean air" trials – gets significantly degraded? This is best shown by example.

Example

Let's assume a social alarm application on 869.2125MHz. These systems use 10mW transmitters, and typically use sensitive (let's say -120dBm) receivers.

According to the Egli model, assuming simple aerials, with no losses or benefits, this system should give an urban range of: 10 x log(1/d^4) = path gain (dB) – 32.4 – 10 x log(1/f^2), or about 390m.

To avoid degradation of this range, an interferer needs to be 10dB below the wanted carrier (typical co-channel performance for a narrowband FSK radio).

If we now consider an in-band (adjacent channel) interferer and assume the receiver's rejection is right on the specification limit, then its path loss will be -120 – 10 + 54 = -76dBm, which corresponds to a range to interfering transmitter of about 17m (an adjacent channel of 60dB would give a range to interferer of only 12m).

From these calculations it can be seen where the actual specification numbers come from; they are set to ensure that a system can still operate with a reasonable density of possible interfering signal sources in the area. In this case the ratio between wanted link range and distance to a +10dBm interferer on adjacent channel is a bit better than 20 to 1. The situation with a similar out of band (image frequency) interferer is similar (60dB spurii spec, 30 to 1).

Unfortunately, there is a problem in the way EN300-220 is phrased. All the Category 1 receiver specifications make sense until you get to one piece of small print. There is a relaxation quoted in section 8.5.3 (limits for spurious response rejection).

"For spurious response tests separated from the wanted signal by less than 0.1% of the centre frequency, the limits are relaxed by 25dB."

As the main spurious response being tested is the image response (at a separation from the carrier of twice the first intermediate frequency), this relaxation becomes relevant for low intermediate frequency designs, which are predominately single chip implementations. 0.1% of 869.2125MHz is about 870kHz. Many single-chip radios, including a number that claim Category 1 performance, have image frequencies well inside this limit, so designs based on them are selling into Category 1 applications.

The usual limit for spurious response under Category 1 is 60dB. The relaxed spec is only 35dB (for interest, if you repeat the calculations in the earlier paragraph this corresponds to a range-to-interferer ratio of only 7:1) and can fall within the crowded 868-869MHz ISM band.

This is an issue because it flies in the face of common sense. Relaxing a specification can only be justified if there is a good technical reason for the relaxation. In this case it is nothing but a commercial decision, to permit inexpensive single-chip designs to address a market previously denied to them. In short:

The Category 1 portion of EN300-220 defines adjacent channel rejection as 54dB minimum for a reason. Low-IF image responses are in-band spurii, in no way different in terms of radio system planning from adjacent, and yet a relaxation of over 20dB is permitted.

This is madness, and as part of a specification which by its own definition is "serving human life inherent systems" it is dangerous madness.

MORE INFORMATION

AN ONLINE READABLE COPY OF THE LATEST VERSION OF EN300-220 CAN BE FOUND AT:
http://www.etsi.org/deliver/etsi_en/300200_300299/30022001/02.04.01_40/en_30022001v020401o.pdf

THE ZERO-TRANSISTOR IC, A NEW PEAK IN IC DESIGN

BILL LAUMEISTER, STRATEGIC APPLICATIONS ENGINEER AT MAXIM INTEGRATED, EXPLAINS HOW A BICMOS INTEGRATED CIRCUIT WITH ONLY RESISTORS AND NO TRANSISTORS CAN SOLVE A KNOTTY DESIGN PROBLEM

This article examines how the mythically "perfect" operational amplifier's gain and temperature coefficient are dependent on external resistor values. It then examines some precision resistor arrays which are manufactured together on a single die and then automatically trimmed to ensure close ratio matching. This process guarantees that the op-amp's gain and temperature coefficient are predictable and reliable, even with large production volumes.

The Perfect and Practical Op-amp

A BiCMOS IC without transistors, that's different! Now that I have your attention, I am trying to make a point. Why would anyone want an integrated circuit (IC) without transistors? Would anyone spend good money for a BiCMOS mask set without transistors?

For the answers we must visit the land of practical operational amplifier (op-amp) applications. And while there, we need to remember the old saying "a chain is only as strong as its weakest link". The mythical, perfect, million-dollar op-amp has infinite gain and a zero temperature coefficient. In Figure 1 that perfect op-amp is configured to provide non-inverting amplification of an input signal.

What controls amplifier gain? More significantly, what controls the gain tolerance and the temperature coefficient? Is it the op-amp or the resistors? The op-amp will be no better than the resistors. Similarly, it is the resistors that dominate the temperature coefficient. Thus precision resistor arrays can have an impact on op-amp performance. We will use some arrays and op-amps as specific examples.

Tolerance in Precision Resistors: Averaging in Manufacturing and What Can Go Awry

Common op-amps offer different operating bandwidths and each device can benefit from the precision resistor arrays; the close specifications of precision resistors are transferred to the amplifier system. Among the transferred specifications are tight gain (as low as 0.035%) and a low temperature-gain coefficient (1ppm/°C typical). Now the importance of precision resistors is becoming clear – chains do have weak links.

Let's look at a simple example in which we will use two 10% tolerance resistors. While our prototype may have typical centre-value resistors, we know that the production run will eventually encounter a situation with R1 and R2 at opposite ends of the tolerance band. During the design, we have to consider these worst-case edges to ensure that the final complex system meets specifications. To deal with this, designers should create an error budget that assigns acceptable errors for each stage. By staying within the budget, you can ensure specification compliance for the whole system.

One trick is to form each resistor from several larger-value parallel resistors. This uses the normal distribution of a manufacturing process to average the tolerance values, thus increasing the probability of achieving the proper value. Of course, this is only true if the normal distribution pattern actually exists.

This is a dangerous assumption if one does not control the manufacturing process. For example, resistor manufacturer A makes or trims the resistor to one edge instead of at the centre value. This

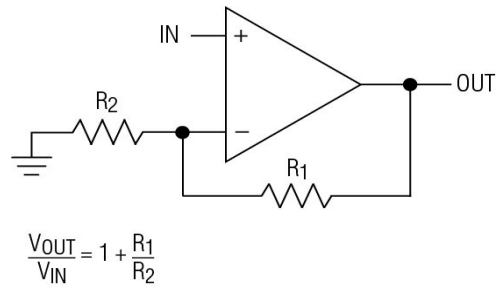


Figure 1: A perfect op-amp non-inverting amplifier circuit

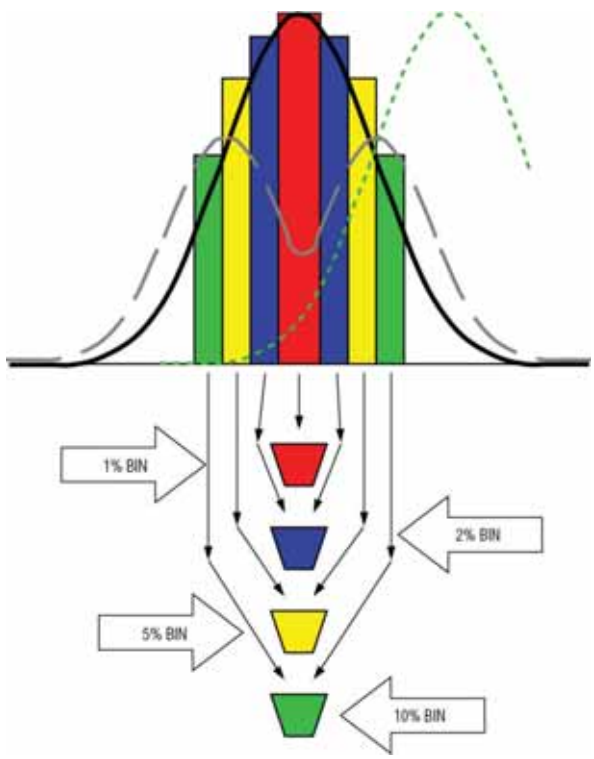


Figure 2: Binning or sorting of manufacturing tolerances

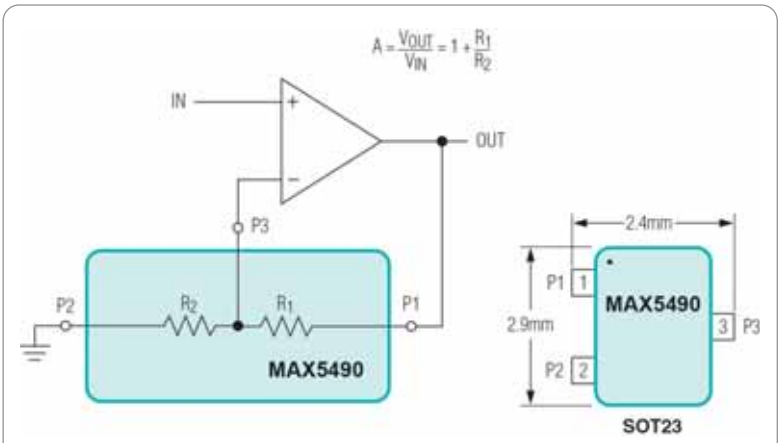


Figure 3: The MAX5490 precision resistor pair

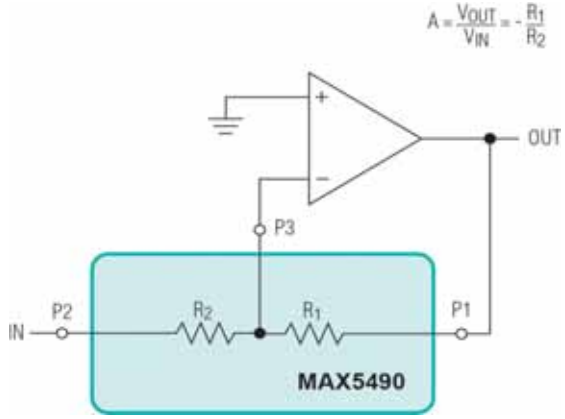


Figure 4: Inverting input op-amp

could happen as a result of a chemistry error, or perhaps the trimming machine is out of tolerance. Worse, resistor manufacturer B makes resistors that follow the normal distribution curve, but they sort or bin the results.

Figure 2 illustrates the normal distribution and the sort selection. Note that each of the bins except 1% is really two bins, one for higher than nominal value and a minus bin for parts lower than the nominal value.

The solid (black line) curve in Figure 2 looks good in a perfect world. However, where we live, not much is perfect. As the manufacturing tolerances move, the number of parts in each bin changes. The tolerance could move to the right (illustrated by the green dotted line), resulting in no yield at 1% tolerance. It could be bimodal (the gray dashed line) with many 5% and 10% tolerance parts and few 1% and 2% tolerance parts.

More importantly, this method seems to make sure that the 2% tolerance parts are only from -1 to -2 and +1 to +2 (no 1% parts). It also appears to remove any 1% and 2% tolerance parts from the 5% bin. We say "seems to" and "appears to" because sales volume and human nature also control the mix. For instance, the plant manager needs to ship 5% tolerance resistors, but he does not have enough to meet the demand this month. He does, however, have an overabundance of 2% tolerance parts. So, this month he throws them into the 5% bin and makes the shipment. Clearly, human intervention skews the statistics.

Then there are other relevant human factors. If an operator is interrupted while unloading the bins, anything can happen. When the operator returns, will he remember to put the parts back in the proper bin? When a few parts spill, the operator does not want to be penalized, so the parts might go back into the most convenient bin.

Then there are human factors when the board is stuffed. The part wanted is 2.52K. The operator is confused: does the correct reel say 2520, 2.533 or 2531? Is the nearest reel the proper one? Alternatively, during re-work if some resistors are dropped, will he pick up the correct part, or will he pick up the resistors he dropped last time? Will the operator admit a mistake or ask for help, taking the risk of some penalty? Human nature says no.

Packaging Resistor Arrays in a Zero-Transistor IC

With so many things to consider, how can a design engineer protect a design from errors? The zero-transistor IC (IC-packaged precision resistor arrays) comes to the rescue. In these integrated arrays, the resistors are very controlled. They have narrow tolerances and, most importantly, the ratio between the two resistors is accurately controlled – after all, it is the ratio that determines the gain. Furthermore, the temperature coefficient is well known and the resistors will track each other, since they are integrated close together on a single die and in a single package. Resistor arrays are also manufactured together on the same wafer and typically automatically tested and trimmed together.

Admittedly test escapes do happen – an operator can dump parts from the bad bin into the good bin. But the places this can happen are minimized to just one station instead of many. Using automatic test equipment (ATE), it is very common to see a physical lock on the bad bin. Such an operating procedure ensures that good parts are removed from the test floor and stowed in inventory, before the bad parts are unlocked and discarded.

As the boards are manufactured, the chance of assembly errors is also reduced, since one package now replaces several discrete resistors. It also requires just a single insertion, rather than multiple components being inserted into the PC board.

If the discrete resistors used in Figure 1 are replaced by a pair of precision resistors (Figure 3), the schematic is basically the same. In fact, resistor arrays often offer a choice of 0.035% (A grade), 0.05% (B grade) and 0.1% (C grade) tolerances. At one part per million, the temperature drift of the Maxim devices is extremely low. The resistance ratio (effectively gain stability) is guaranteed less than 1ppm/°C (typ) over -55°C to +125°C. The end-to-end resistance of the pair is 100kΩ. Five standard and other custom-resistance ratios from 1:1 to 100:1 are available from tiny 3-pin SOT23 packages. The operating voltage across the resistors is greater than most op-amps, up to 80V across the sum of R1 and R2. Additionally, resistance-ratio long-term stability is typically 0.03% over 2000 hours at 70°C.

The MAX5490 precision-resistor pair allows the use of normal op-amp application circuits. Figure 4, Figure 5, and Figure 6 illustrate the simplest common circuits.

The data sheet for the MAX5490 specifies to calculate bandwidth by using:

$$\frac{1}{2\pi RC}$$

where $C = C_{P3}$ and

$$R = \frac{R_1 \times R_2}{R_1 + R_2}$$

C_{P3} is 2pF, so the bandwidth is 3MHz. This assumes that the op-amp has sufficient bandwidth to support the resistor bandwidth.

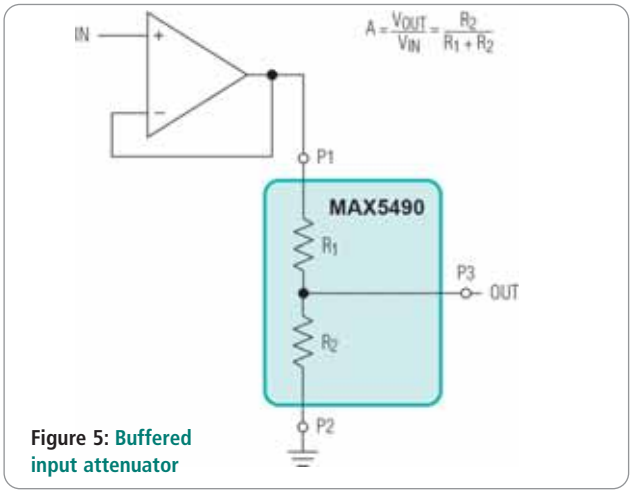


Figure 5: Buffered input attenuator

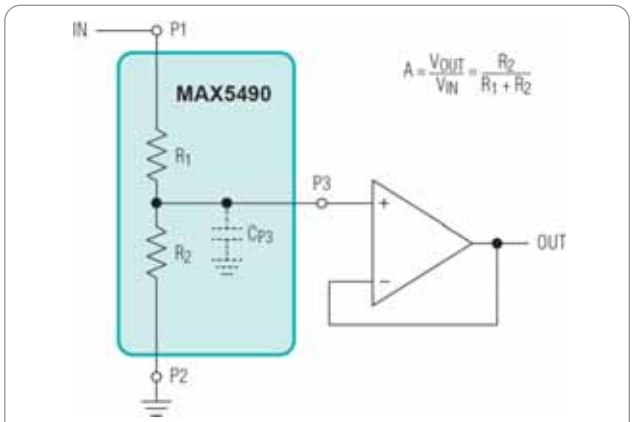


Figure 6: Buffered output attenuator

In our example we used a pair of 50kΩ resistors with the expected low currents. However, as the resistance ratio changes, the current levels rise, causing self-heating. Obviously this must be considered when evaluating the temperature coefficient; the data sheet details the needed calculations to minimize this effect.

While the MAX5490 consists of a centre-tapped 100kΩ resistor, parts with other resistor values are available, such as the MAX5491 (with 30kΩ end-to-end resistance) and the MAX5492 (with 10kΩ end-to-end resistance). Any of these values will be useful in the design of a summing amplifier.

Thus, a zero-transistor IC is not such a ridiculous idea after all, especially when it produces resistors with extremely good tolerances. As a practical matter, great amplifiers depend on the tight resistor-pair ratios guaranteed by the MAX5490, MAX5491 and MAX5492. ●

Andy Evans, senior product engineer at ARM

ARM selects XJTAG for RealView development tools debug and test

"ARM, the world's leading semiconductor intellectual property (IP) supplier, has reduced the time and cost of developing its range of RealView development tools by using the XJTAG boundary scan development system to improve and speed up the process of debugging and testing its high density, multi-layer development boards."

ARM® technology lies at the heart of advanced digital products from mobile, home and enterprise solutions to embedded and emerging applications. ARM's comprehensive product offering includes 16/32-bit RISC microprocessors, data engines, graphics processors, digital libraries, embedded memories, peripherals, software and development tools, as well as analogue functions and high-speed connectivity products.

To support the company's SoC IP, ARM has developed a strong base of development tools, software and hardware products. For example, its range of RealView® development solutions are ideal systems for customers prototyping ARM processor-based products and are suitable for architecture and CPU evaluation, hardware and software design, and ASIC emulation. These development platforms are typically highly complex, high density, twelve-to-sixteen layer board designs, containing multiple high pin-count ball grid array (BGA) devices including processors, ASICs, FPGAs and CPLDs.

"Our development platforms are used extensively across the business and are designed to deliver significant risk reduction and faster time-to-market benefits to our Partners," said Spencer Saunders, engineering manager, platforms, Development Systems, ARM.

"With tens of thousands of pins on each board, we recognized that it would not be possible to validate these circuits in a commercially realistic timescale without the use of a boundary scan test system."

After evaluating the different competitive options, the engineering team at ARM's development facility in Cambridge, UK, selected the XJTAG boundary scan development system. The XJTAG system has enabled ARM to speed up the process of debug and test, get test coverage up to around the 90 percent mark and to significantly improve production yields.

"XJTAG offers incredible power, performance and versatility and can test both boundary scan (JTAG) and cluster (non-JTAG) devices including BGA and chip scale packages," said Andy Evans, senior product engineer, platforms, Development Systems, ARM.

"XJTAG is easy to use, the test scripts for non-JTAG devices follow the familiar top down design flow, and these test scripts are device-centric, making them re-usable from project to project, which saves ARM an awful lot of time."

ARM is currently using XJTAG on its latest generation of RealView platform baseboards, and, because of its built-in design-for-test (DFT) functionality, it has been used right from the very beginning of the design process to help improve the design and reduce respins.

"XJTAG's DFT capability is extremely powerful and saves us a great deal of time, as it automatically handles any netlist changes by adapting to the new circuit connections, thereby avoiding the time-consuming process of manually picking through the netlist for errors," said Spencer Saunders.

"In addition, XJTAG's powerful circuit visualization tool provides us with a simple graphical view of the state of all JTAG pins across the multiple BGA devices and enables us to quickly pinpoint specific faults on our boards and speed up the whole debug process."

opinion

Spencer Saunders
engineering manager
platforms, Development Systems
ARM

"The XJTAG boundary scan system is an extremely powerful, versatile and cost effective product which has enabled ARM to improve and speed up the process of debugging and testing its RealView development tools. With XJTAG, we are now close to meeting our target for 90 percent test coverage and ten-minutes-per-board production test, but we also have a boundary scan system that allows tests to be recorded, refined and repeatedly re-used throughout the development cycle both by our engineering team and our contract manufacturing partners."

Data Bank

Company:	ARM Holdings
Nature of business:	World's leading semiconductor IP supplier
Main product:	16/32-bit RISC microprocessors, data engines, graphics processors, digital libraries, embedded memories, software and development tools, peripherals, analogue functions and high-speed connectivity products
Locations:	ARM has facilities/offices in North America, Europe, the Middle East, Far East and India
Employees:	Approx. 1659
Web site:	www.arm.com

EVERYTHING OLD IS NEW AGAIN IN VIDEO FILTERS

BILL BOLDT AND **MICHAEL RANKINS** FROM FAIRCHILD SEMICONDUCTOR

DISCUSS THE WAYS TO MAKE IT EASIER FOR SET-TOP BOX DESIGNERS TO PUT OLD REQUIREMENTS INTO NEW PRODUCTS AMID THE PLETHORA OF OLD AND NEW VIDEO STANDARDS

Integrated video filters were born as expensive, very high-precision components for video broadcast applications, and were later adapted for cost-sensitive consumer applications such as set-top boxes. The first major integrated video filters appeared in the early 1990s and were used in the first-ever direct broadcast satellite set-top box, and they continue to be used in satellite and cable set-top boxes.

So what do video filters do? For one, they can act as reconstruction filters after the digital-to-analog converter on the output of the video processor. In set-top boxes and DVD equipment they are also used as anti-aliasing filters on the input of a video processor.

In the old days it was easy to select a video filter, just have to count the number of outputs: basically, one filter for composite video (CVBS) or two for S-video. Then DVD players showed up using the triple output scheme of component video. Component video's arrival enshrined the arcane terms of Y, Pb and Pr (or R, G, B), which became standard nomenclature on the back of video equipment. As a consequence, users and designers of video equipment had to count all the way up to six, which is the sum of the analog outputs , i. e. CVBS = 1 , S-video (Y, C) = 2, Component (Y, Pb, Pr) = 3. Figure 1 shows a typical set-top box with the full complement of analog video outputs.

However, things started to really change as higher definition video appeared on the scene and became cheap enough for consumers to afford. Numbers such as 480, 720 and 1080, as well as others outside the US standards, surfaced and were followed by the letters "i" or "p". These number-letter combinations became another part of video's growing jargon library.

Image Definition

So, what do these numbers and letters mean? The number-letter combinations such as 480i, 720p, 1080i and 1080p refer to the number of lines in a video display and if the display is interlaced (i) or progressive (p) scan. Interlaced means that alternate lines on the display are scanned and progressive means the lines are scanned one right after the other.

Interlaced video scanning is a legacy of early 1940's video standards that persist today. Briefly, each video frame (25 per second in Europe, 30 in the US) is sent as two interlaced fields, first the odd-numbered lines, then the even. This was done to optimize the limited bandwidth of the day, and for smooth

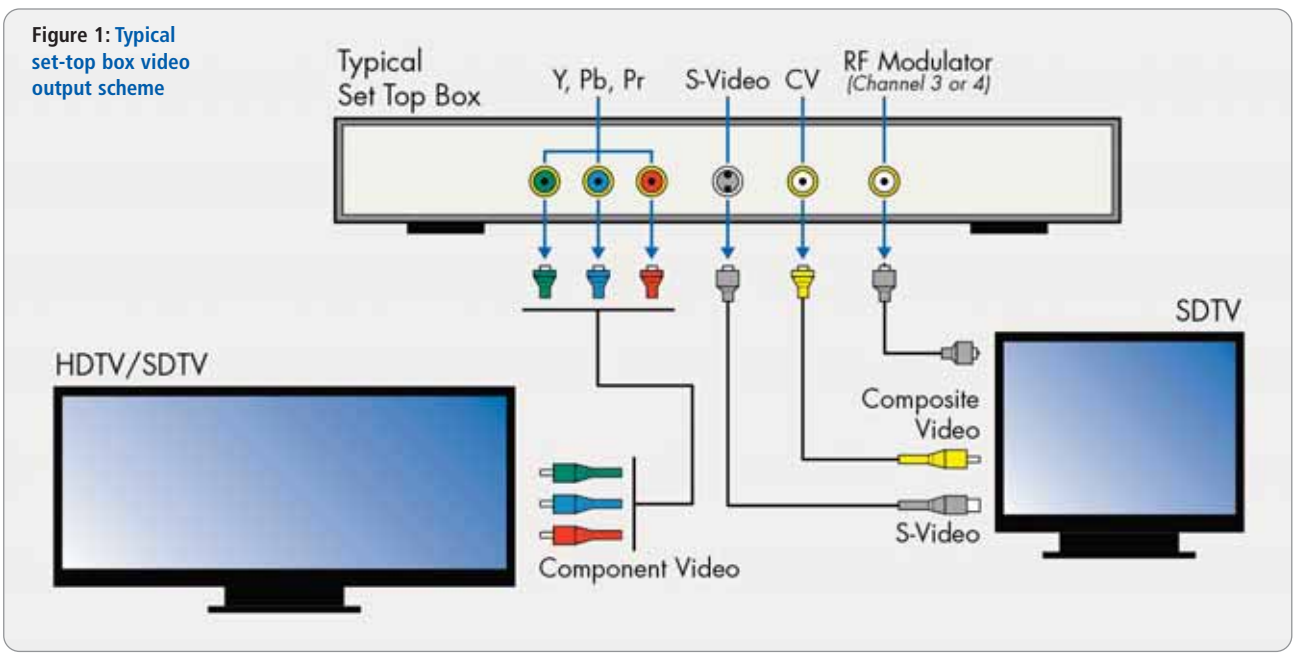
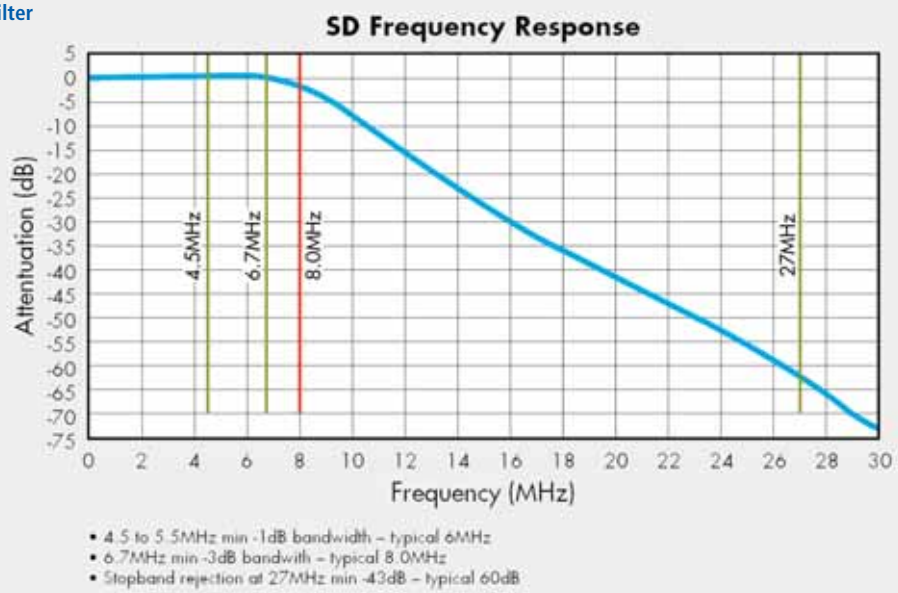


Figure 1: Typical set-top box video output scheme

Figure 2: Typical SD filter frequency response



motion, in conjunction with the human eye's built-in persistence of vision.

Progressive (p) scanning, on the other hand, scans each line in its proper turn; its images are much better, among other reasons because each pixel's location is physically fixed in place, rather than determined by the vagaries of the magnetic fields acting on a beam of electrons.

A shorthand terminology was created to make all this comprehensible to the shopper. The various number-letter combinations were grouped into certain categories under the term "definition", which basically refers to image sharpness. The higher the definition, the better the picture since more lines means more pixels to colour and describe the image.

The naming of video signals and grouping them into definition categories can be a topic that runs many pages, especially when considering all the different standards by region. So, for the purposes of real-world video filter discussions, roughly speaking resolutions below 480p became Standard Definition (SD), 480p became Enhanced Definition (ED), and 720p and 1080i became High Definition (HD) for US standards. Furthermore, many video equipment vendors started to use the term high definition (HD) somewhat loosely.

Figure 3: Typical HD filter frequency response

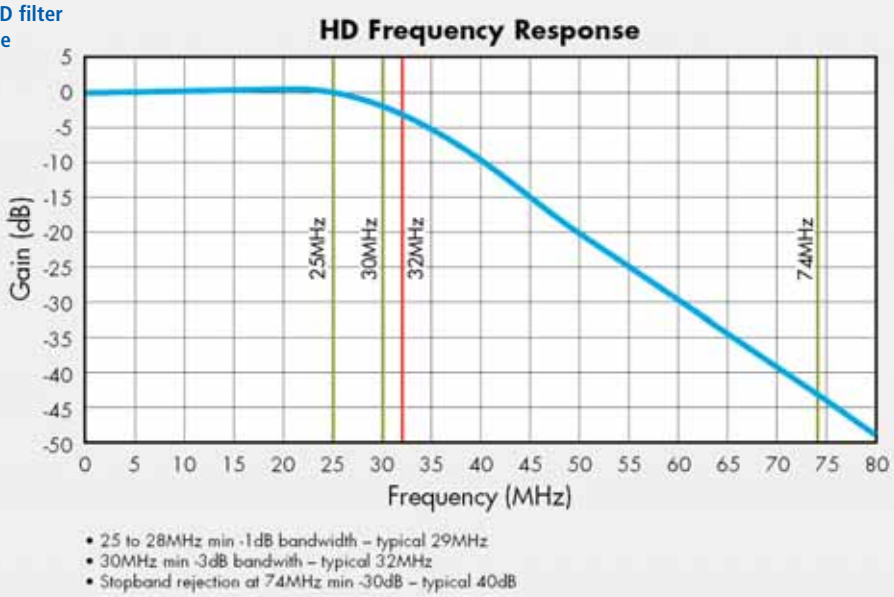
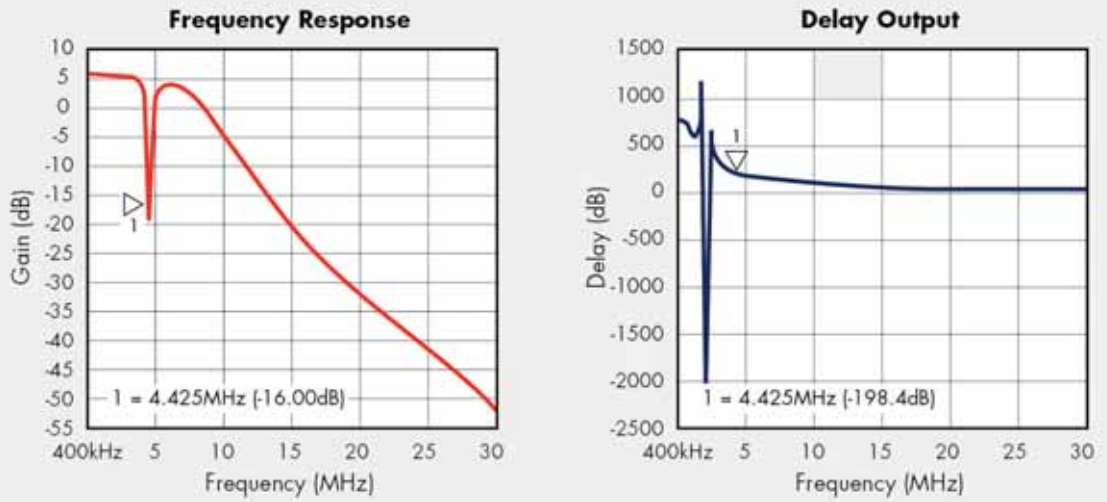


Figure 3: Frequency response of SD video filter with sound notch (gain and delay)



In order to be more precise, terms like HD-ready, HD-ready-1080p and full-HD were coined by video industry associations to try to clarify things, but this met with mixed success and may have just added to the confusion. Thus, to deal with the confusion, video filter makers have decided to ascribe the terms SD, ED, HD and 1080p HD to classify filters according to a filter's cutoff frequency (or pass-band, as these are all low-pass filters) is at:

- An SD filter's cutoff frequency is around 8MHz;
- ED's is around 16MHz;
- HD's is around 32MHz;
- 1080p's is between 65 to 70MHz.

Breaking it out by cutoff frequency is very straightforward and avoids the confusion in naming created by television and set-top box (STB) marketers. Figures 2 and 3 show examples of a typical SD and HD filter's frequency response, respectively.

Compatibility Issues

Having all these new definitions to consider brings an entire new dimension to the problem. Not only does the designer have to consider the number of channels but also their definition at the same time. Furthermore, there are two ways to provide integrated circuit filtering. One is to use a combination of filter ICs and the other is to use a single filter IC that handles all the different channels and definitions needed.

One of the salient and often frustrating features of video products is that older requirements stick around seemingly forever. Backward compatibility is part of the DNA of the video market and is why colour TVs can display black and white signals and HD can be shown on SD screens. This applies to connectors as well. The connectors on the back of set-top boxes can be seen as a history lesson of video connection, from composite video, S-Video, component video to HDMI. Video filters are used in each of these types of connection methods, aside from HDMI, which is digital and thus has no need for analog filters. Component video can be SD, ED or HD and require a different type of filter in each case. In addition to the legacy requirements noted above, there is a very rare thing called a 'sound notch' (Figure 4) that is included on some set-top boxes with an RF cable connector (coax) output.

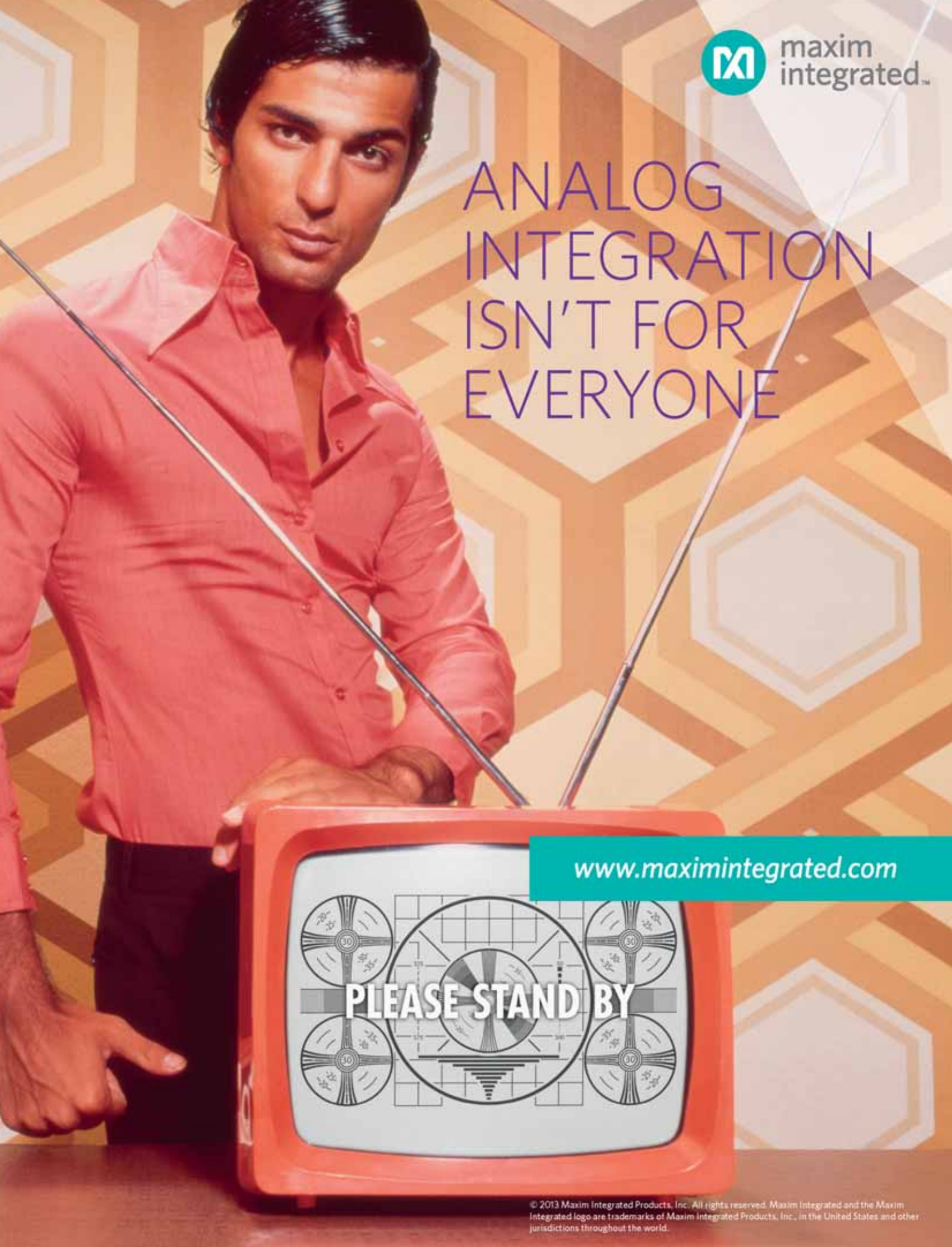
In some traditional set-top boxes the RF output is necessary to filter out the audio carrier at around 4.5MHz (for NTSC systems). The audio carrier is in the pass-band of SD signals and must be removed, which is done very easily by using a narrow sound notch filter. Fortunately, there is a video filter IC with a built-in sound notch filter that was created specifically to do this.

It turned out putting a sound notch on a video filter was a relatively challenging design. Because of its level of difficulty, the life of such an IC filter with sound notch has been very long, even extending to today, even though this type of connection scheme is relatively rare. Though rare, such filters are still around because makers of set-top boxes still have some products in their portfolios that must remain backward compatible.

Protecting from ESD

Another important issue for set-top box makers is electrostatic discharge (ESD). Set-top box makers have standardized on BAV99 ESD protection diodes for discrete filtering. However, integrated video filters not only provide a way to eliminate numerous discrete filtering components but also the diodes. Integrated filters offer ESD protection up to 12KV depending on the particular product. ESD protection is a good idea and designers should not go to market with their video outputs unprotected in order to prevent expensive core TV processing chips from being damaged.

Another concern – and one receiving increasing attention – is reducing stand-by power drain. This is sometimes called 'vampire power' and it is becoming a major environmental concern as a waste of power, since power generation is costly and produces greenhouse gasses. California, for example, recently enacted legislation to reduce vampire power in LCD TVs by requiring that such products be Energy Star compliant. In order to display the Energy Star logo, all devices (TVs, PCs, monitors, printers, etc) must use less than 30 watts of power when inactive. The low-power consumption of Fairchild's video filters help make Energy Star compliance easier. ●



A LOW-VOLTAGE NMOS MOCDBA-BASED CURRENT-MODE UNIVERSAL FILTER AND SINUSOIDAL OSCILLATOR – USING ONLY ONE CIRCUIT

JUN XU AND **CHUNHUA WANG** FROM HUNAN UNIVERSITY IN CHINA PRESENT A CIRCUIT BASED ON LOW-VOLTAGE NMOS MOCDBA, WHICH CAN ACHIEVE CURRENT-MODE UNIVERSAL FILTER AND SINUSOIDAL OSCILLATION FUNCTIONS WITH THE SAME TOPOLOGY

Current-mode techniques have received a wide attention over the last few years, largely due to their high slew rate, wide bandwidth, low voltage and low power-consumption among others. A number of current-mode devices, such as CCII (second generation current conveyor), CFA (current feedback amplifier) and OTA (operational transconductance amplifier) have been widely applied in circuit design, especially in applications such as on-chip RF continuous-time current-mode filters. Recently, an active circuit element called Current Differencing Buffered Amplifier (CDBA) was introduced (Acar and Ozoguz 1999) [1] as a versatile active building block in designing analog circuits. Among its advantages are: (1) high slew rate; (2) wide bandwidth; (3) no parasitic capacitance; (4) low voltage; and (5) low power consumption. As such it has been widely adopted in current-mode signal processing circuits, such as inductance simulator circuits [2-3], sinusoidal oscillator circuits [4-6] and filter circuits [7-18] among others.

Figure 1: MOCDBA

CDBA-Based Current-Mode Universal Filter

There are universal filters that use CDBA which can realize five filter-functions [19-20] but they are restricted to voltage mode. A CDBA-based current-mode universal filter has also been proposed in literature [7], with the circuit realizing current-mode five filter-functions employing two CDBAs, but its topology has to be modified when realizing these different filter functions, not to mention it uses too many passive components.

There's also been development on the CDBA-based KHN (Kerwin, Huelsman, Newcomb) filter and universal filters respectively [21-22]. The circuit in literature [21] involves three CDBAs, two capacitors and six resistors. Its structure is simple and the circuit enjoys low sensitivities. The circuit of literature [22] contains three CDBAs, two capacitors and five resistors. It can realize five filter-functions without a change in its topology and enjoys very low sensitivities.

On the other hand, reference [4-6] proposed some new CDBA-based oscillator topologies. These oscillators share some advantages, such as orthogonal control of oscillation conditions and oscillation frequency, reduced number of components and so on. But, those circuits, both of filters and oscillators, are only limited to the use of CDBA with a single z port (current output terminal), which is not convenient for some applications. This is because:

(1) The through signal and signal feedback cannot be taken

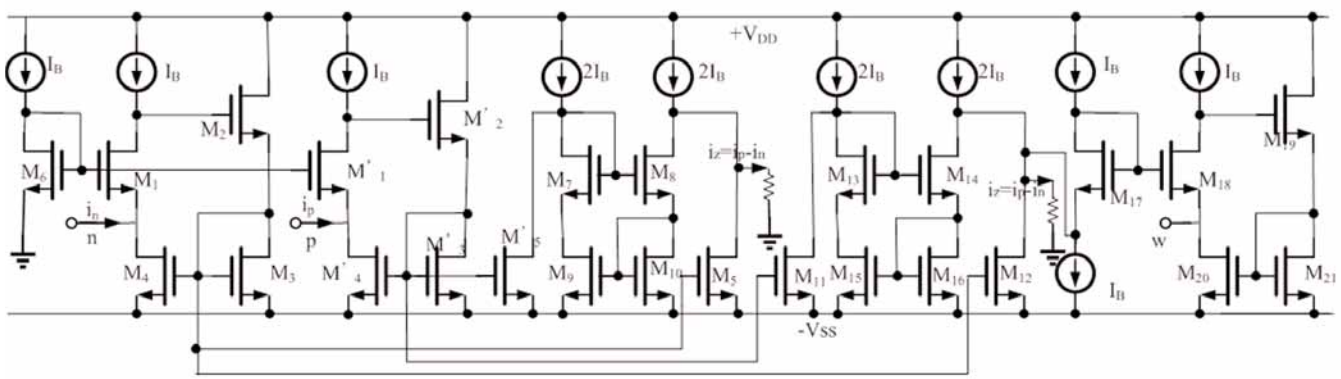


Figure 2: Realization circuit of low-voltage NMOS-based MOCDBA

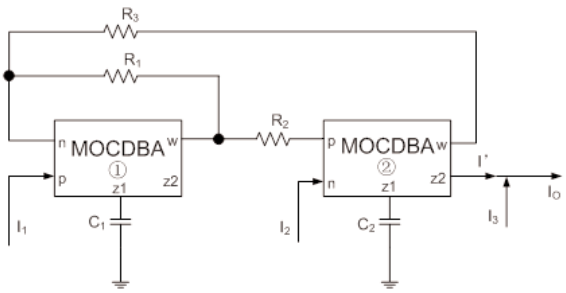


Figure 3: Proposed MOCDBA-based current-mode universal filter

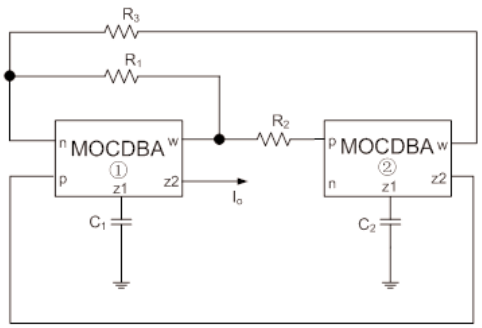


Figure 4: Proposed MOCDBA-based current-mode sinusoidal oscillator

into account simultaneously. When the circuit needs to use signal feedback, the z port's output current is used for signal feedback and can't be used as through-signal or port. However, high output impedance is also used to realize the circuit cascade.

(2) These circuits adopting single z output CDBA don't take full advantage of the component's current output port characteristics, and they use too many active and passive components, making them inflexible. From power-dissipation and manufacturing cost points of view, it is advantageous to minimize the number of active and passive elements. However, Z-Copy CDBA [23-24] was able to resolve these problems.

(3) These circuits can't perform both universal filter and oscillator functions with the same circuit configuration. To date only a few circuits [25] meet this feature and they are restricted to voltage mode only. Thus, we present here a circuit based on low-voltage NMOS Multiple Output Current Differencing Buffered Amplifier (MOCDBA) which can realize both, current-mode universal filter functions and sinusoidal oscillation functions, with the same circuit topology. The suggested filter circuit has a current-mode multi-input single-output structure and can realize lowpass (LP), highpass (HP), bandpass (BP), notch (BS) and allpass (AP) universal functions without having its topology changed.

The circuit's configuration is simple with a minimum number of active and passive components. The natural frequency ω_o and bandwidth BW (ω_o /Q) are independent. Meanwhile, by slightly modifying this filter circuit, a new MOCDBA-based current-mode sinusoidal oscillator is easily obtained, with its oscillation condition and oscillation frequency adjustable independently.

It's easy to see that both filter and oscillator share low active and passive sensitivities and high output impedance. All the capacitors used in the filter and oscillator are grounded, which is important with respect to integrated circuit implementation. Both circuits also have low power-consumption.

The proposed filter and oscillator can be applied in many fields: for instance RF transmitter/receivers, phase-locked loop (PLL) FM demodulators, wireless communication and instrumentation. The filter circuit can also be used in designing active filters instead of surface acoustic wave (SAW) filters used in GSM systems.

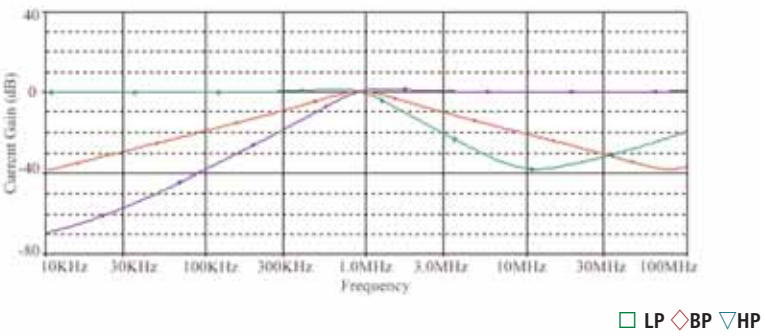


Figure 5a: LP, BP, HP frequency responses of the proposed filter

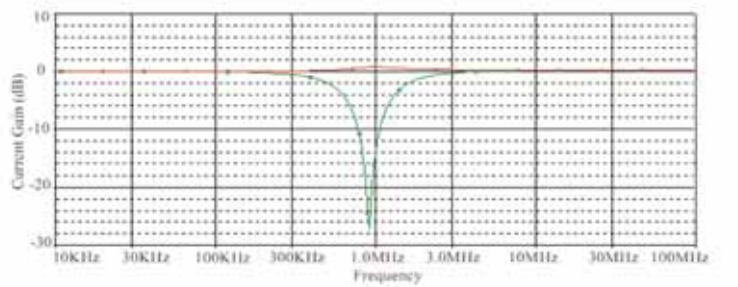


Figure 5b: BS, AP frequency responses of the proposed filter

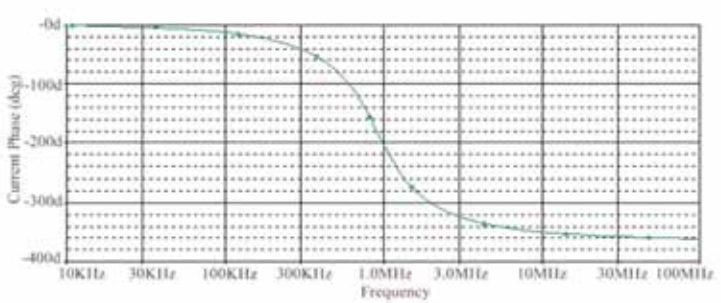


Figure 5c: AP phase responses of the proposed filter

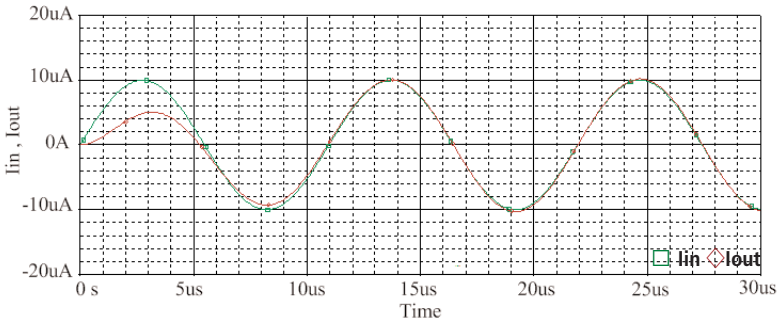


Figure 6: The sinusoidal waveforms response of the proposed filter

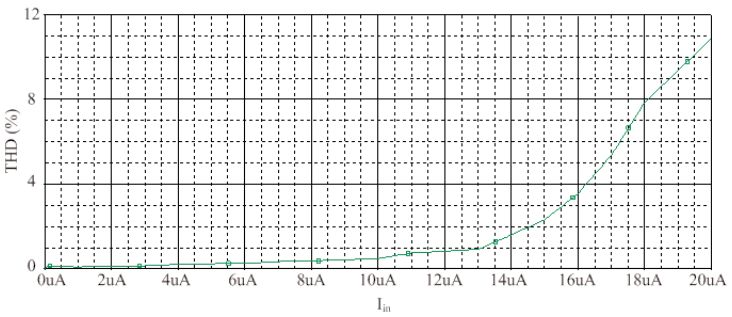


Figure 7: Total harmonic distortion (THD) of the filter

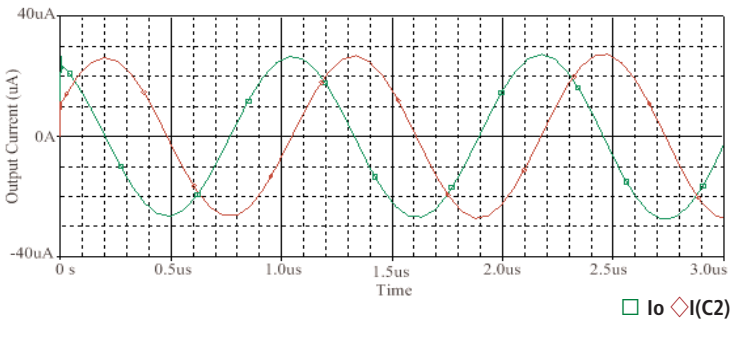


Figure 8a: Transient responses (t = 3us) of the proposed sinusoidal oscillator

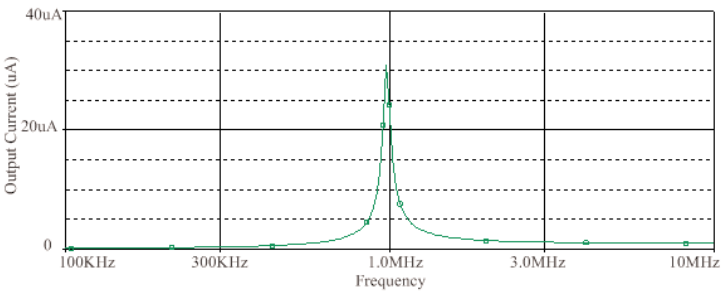


Figure 8b: Frequency responses of the proposed sinusoidal oscillator

CDBA and Its Realization

The schematic of the MOCDBA is shown in Figure 1, where p and n are the positive and negative current input terminals respectively, z is the current output terminal and w is the voltage output terminal. Its current and voltage characteristics can be described by the following matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_w \end{bmatrix} \quad (1)$$

The CDBA basically consists of two unity-gain cells, a current differencing circuit (current substractor) and a buffered amplifier (voltage follower). Usually it can be built using various techniques, and one possible realization is given in Figure 2, which is a low-voltage, multiple output, current-differencing buffered amplifier using only NMOS transistors. This MOCDBA circuit is modified from the circuit [26] and the number of z ports in the circuit can be selected as needed.

Suggested MOCDBA-Based Current-Mode Universal Filter Circuit

Figure 3 shows the recommended current-mode universal biquad filter, which consists of only two CDBAs, two grounded capacitors and three resistors.

By routine analysis, the single output current function realized by this configuration is found to be:

$$I_O = I_1 + I_3 = \frac{s\frac{1}{C_1R_2}I_1 - (s^2 + s\frac{1}{C_1R_1})I_2 + (s^2 + s\frac{1}{C_1R_1} + \frac{1}{C_1C_2R_2R_3})I_3}{s^2 + s\frac{1}{C_1R_1} + \frac{1}{C_1C_2R_2R_3}} \quad (2)$$

From Equation 2 by selecting component values of R1 = R2, we can get the following filter functions:

a) If $I_1 = 0$ and $I_2 = I_3 = I_{in}$ LP response can be realized;
b) If $I_2 = I_3 = 0$ and $I_1 = I_{in}$ BP response can be realized;
c) If $I_3 = 0$ and $I_1 = I_2 = -I_{in}$ HP response can be realized;
d) If $I_2 = 0$ and $I_1 = -I_3 = -I_{in}$ BS response can be realized;
e) If $I_2 = 0$ and $I_1 = -2I_3 = -2I_{in}$ AP response can be realized.

Clearly, the proposed filter can be used as a current-mode three-input single-output universal filter that can realize all standard types of universal biquad filter functions.

Also from Equation 2, the natural angular frequency (ω_o) and bandwidth BW (ω_o/Q) are given by the following in all cases:

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_2R_3}} \quad (3)$$

$$BW = \frac{1}{C_1R_1} \quad (4)$$

From Equations 3 and 4 it is seen that the natural angular frequency (ω_o) is adjustable via resistor R_3 or capacitor C_2 without affecting the bandwidth.

Taking the non-idealities of the CDBA into account, its current and voltage characteristics can be also described by the following matrix equation:

Crystal-free 8-bit USB PIC® microcontrollers cut system costs and power consumption

0.25% clock accuracy enables USB connectivity, eliminating the need for external crystal

Microchip's lowest-cost and smallest-form-factor USB microcontrollers (MCUs), feature pin counts of 14 to 100 pins and are the first 8-bit MCUs to integrate LCD control, battery-backed RTCC, and USB on a single chip.

Microchip's latest USB PIC® MCUs feature internal clock sources with 0.25% clock accuracy to enable USB connectivity with no external crystal. They are also the first USB MCUs to combine pin-counts ranging from 14 to 100, with high peripheral integration and up to 128 KB of Flash. The eXtreme Low Power (XLP) technology also keeps power consumption down to 35 µA/MHz in active mode and 20 nA in sleep mode.

Lowest-cost and smallest-form-factor

The PIC16F145X MCUs give you USB connectivity and capacitive touch sensing, in addition to a wide range of integrated peripherals with footprints down to 4x4 mm.

High-performance touch-sensing with USB

With an integrated Charge Time Measurement Unit (CTMU) and 1.8 V to 5 V operation, PIC18F2X/4XK50 MCUs are pin-compatible with legacy PIC18 MCUs, giving an easy migration to higher-performance.

USB plus LCD control and a RTCC with Vbat

The PIC18F97J94 family gives you USB connectivity with LCD control, and a battery-backed real-time clock calendar (RTCC), all on a single 8-bit PIC® microcontroller.

GET STARTED IN 3 EASY STEPS:

1. Choose a peripheral mix and pin count to suit your application
2. Use the free USB stacks and software drivers for faster design
3. Start developing with low-cost development kits

For more information, go to: www.microchip.com/get/eu8bitUSB

MICROCHIP

Microcontrollers • Digital Signal Controllers • Analog • Memory • Wireless

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & \beta & 0 \end{bmatrix} \cdot \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_w \end{bmatrix} \quad (5)$$

where α_p, α_n and β are current and voltage gains respectively, and $\alpha_p = 1 - \varepsilon_p$, $\alpha_n = 1 - \varepsilon_n$, $\beta = 1 - \varepsilon_v$. Here ε_p, ε_n are current tracking errors and ε_v is the voltage tracking error, with the absolute values of all last three terms being a lot less than a unit value. Using Equation 5, the natural angular frequency (ω_o) and the bandwidth (BW), considering the non-ideal effects, become:

$$\omega_o = \sqrt{\frac{\alpha_{n1}\alpha_{p2}\beta_1\beta_2}{C_1C_2R_2R_3}} \quad (6)$$

$$BW = \frac{\beta_1}{C_1R_1} \quad (7)$$

where α_{pi}, α_{ni} and β_i are the parameters α_p, α_n and β of the ith CDBA (i = 1, 2). The active and passive sensitivities of this universal filter are shown as:

$$\begin{aligned} &S_{R_2}^{\omega_0} = S_{R_3}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}, \; S_{R_1}^{\omega_0} = 0 \\ &S_{C_1}^{BW} = S_{R_1}^{BW} = -1, \; S_{R_2}^{BW} = S_{R_3}^{BW} = S_{C_2}^{BW} = 0 \\ &S_{\alpha_{n1}}^{\omega_0} = S_{\alpha_{p2}}^{\omega_0} = S_{\beta_1}^{\omega_0} = S_{\beta_2}^{\omega_0} = \frac{1}{2}, \quad S_{\alpha_{n2}}^{\omega_0} = S_{\alpha_{p1}}^{\omega_0} = 0 \\ &S_{\beta_1}^{BW} = 1, \quad S_{\alpha_{p1}}^{BW} = S_{\alpha_{n1}}^{BW} = S_{\alpha_{p2}}^{BW} = S_{\alpha_{n2}}^{BW} = 0 \end{aligned} \quad (8)$$

From the above calculations, it can be seen that all sensitivities are constant and less than or equal to unity.

Proposed MOCDBA-Based Current-Mode Sinusoidal Oscillator

From Figure 3, by setting $I_1 = I_2 = I_3 = 0$ and connecting the port p of the CDBA1 and the port z2 of the CDBA2, the proposed MOCDBA-based current-mode sinusoidal oscillator can be obtained as shown in Figure 4.

By routine analysis the characteristic equation of the second proposed configuration can be given by:

$$s^2 + \frac{1}{C_1}\left(\frac{1}{R_1} - \frac{1}{R_2}\right)s + \frac{1}{C_1C_2R_2R_3} = 0 \quad (9)$$

The oscillation condition and the natural angular frequency (ω_o) of this configuration can be determined as:

$$= \qquad R_1 = R_2 \quad (10)$$

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_2R_3}} \quad (11)$$

It is apparent that the oscillation condition and the oscillation frequency of the proposed oscillator circuit can be controlled independently.

Considering the non-ideal effects, Equation 9 can be rewritten as follows:

$$s^2 + \frac{1}{C_1}\left(\frac{\alpha_{n1}\beta_1}{R_1} - \frac{\alpha_{p1}\alpha_{p2}\beta_1}{R_2}\right)s + \frac{\alpha_{p2}\alpha_{n1}\beta_1\beta_2}{C_1C_2R_2R_3} = 0 \quad (12)$$

From this equation, the oscillation condition and the oscillation frequency are revised as:

$$\alpha_{n1}\beta_1R_2 = \alpha_{p1}\alpha_{p2}\beta_1R_1 \quad (13)$$

$$\omega_o = \sqrt{\frac{\alpha_{n1}\alpha_{p2}\beta_1\beta_2}{C_1C_2R_2R_3}} \quad (14)$$

The active and passive sensitivities of the sinusoidal oscillator are shown as:

$$\begin{aligned} &S_{R_2}^{\omega_0} = S_{R_3}^{\omega_0} = S_{C_1}^{\omega_0} = S_{C_2}^{\omega_0} = -\frac{1}{2}, \; S_{R_1}^{\omega_0} = 0 \\ &S_{\alpha_{n1}}^{\omega_0} = S_{\alpha_{p2}}^{\omega_0} = S_{\beta_1}^{\omega_0} = S_{\beta_2}^{\omega_0} = \frac{1}{2}, \quad S_{\alpha_{n2}}^{\omega_0} = S_{\alpha_{p1}}^{\omega_0} = 0 \end{aligned} \quad (15)$$

Simulation and Results

PSpice was used to verify the performance of the proposed circuits. The CDBA is realized as shown in Figure 2. The supply voltages used are $V_{DD} = -V_{SS} = 1.25V$ and the constant bias currents $I_B = 30\mu A$ are realized by employing the basic current mirrors.

The model parameters of 0.5µm CMOS technology are shown in Table 1. The lowpass (LP), highpass (HP), bandpass (BP), notch(BS) and allpass (AP) frequencies respond according to the circuit configuration of Figure 3 are shown in Figure 5. These were the specifications: natural angular frequency $f_o = \omega_o/2\pi$ = 1MHz, bandwidth BW = 0.16MHz and the parameter values of passive elements are $R_1 = R_2 = R_3 = 1k\Omega$, $C_1 = C_2 = 0.16nF$. The circuit's total power consumption is only 2.03mW.

```
.MODEL MOD1 NMOS (LEVEL=3 PHI=0.700000
TOX=9.6000E-09 +XJ=0.200000U TPG=1 VTO=0.6573
DELTA=5.9880E-01 UO=505.1
+ LD=1.9240E-08 KP=1.8169E-04 THETA=1.8930E-01
CJ=5.6415E-04
+ RSH=8.7930E+00 GAMMA=0.5569 NSUB=1.2090E+17
+ NFS=5.9090E+11 VMAX=2.7440E+05 ETA=2.4370E-02
+ KAPPA=3.2050E-01 CGDO=4.0920E-10 CGSO=4.0920E-10
+ CGBO=3.8892E-10 MJ=7.3366E-01 CJSW=2.0000E-11
+ MJSW=6.7865E-01 PB=9.9999E-01)
```

Table 1: Model parameters of 0.5µm CMOS technology

The filter circuit's total harmonic distortion (THD) analysis is also investigated using the PSpice program. A sinusoidal current (10µA/100kHz) was the input signal, checking for the BP response in this simulation. It is found in Figure 7 that for an input current of less than 15µA, the circuit's THD is no more than 2%.

For Figure 4, the parameter values of passive elements are $R_1 = R_2 = R_3 = 10k\Omega$, $C_1 = 0.016nF$, $C_2 = 0.016nF$, so the oscillation frequency $f_o = \omega_o/2\pi$ = 1MHz. Figure 8 shows the simulation results. The circuit's THD is 1.38%. The total power consumption is 2.01mW. As such, the theoretical and simulation results are in good agreement. ●

See the References on page 24

REFERENCES

[1] C. ACAR, S. OZUGUZ. A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters. Microelectronics J, 1999, vol. 30, p. 157-160.
[2] ALI ÜMIT KESKIN, ERHAN HANCIOGLU. CDBA-based synthetic floating inductance circuits with electronic tuning properties. ETRI Journal, April 2005,Volume 27, Number 2.
[3] WINAI JAIKLA, MONTREE SIRIPRUCHYANUN. Current controlled CDBAs based- novel floating and grounded negative inductance simulators. In: The 21st International Technical Conference on Circuits/Systems, Computers and Communications, Thailand, 2006, p.701-704.
[4] SUMAYTEE PISITCHALERMPONG, WORAPONG TANGSRIRAT, WANLOP SURAKAMPONTOM. CDBA-based multiphase sinusoidal oscillator using grounded capacitors. SICE-ICASE International Joint Conference , Oct. 2006, p.18-21.
[5] S. O ZCAN, A. TOKER, C. ACAR, H. KUNTMAN. Single resistance-controlled sinusoidal oscillators employing current differencing buffered amplifier. Microelectronics Journal 31, 2000, p.169–174.
[6] ALI ÜMIT KESKIN. Voltage-mode high-Q band-pass filters and oscillators employing single CDBA and minimum number of components. International Journal of Electronics, August 2005, Vol. 92, No. 8, p.479–487.
[7] ALI ÜMIT KESKIN, ERHAN HANCIOGLU. Current mode multifunction filter using two CDBAs. Int. J. Electron. Commun. (AEU) 59, 2005, 495 – 498.
[8] UGUR CAM. A novel current-mode second-order notch filter configuration employing single CDBA and reduced number of passive components. Computers and Electrical Engineering 30, 2004, 147–151.
[9] WORAPONG, TANGSRIRAT, NOBUOFUJII, WANLOP URAKAMPONTORN. Current-mode leapfrog ladder filters using CDBAs. IEEE International Symposium on Circuit and Systems, 2002, Vol.5, p.57-60.
[10] Y. S. HWANG, Z. H. HUANG, J. J. CHEN. "High-order current-mode filters based on current differencing buffered amplifiers," IEICE Trans Fund, Jan. 2009,vol. E80-A, no. 1, p. 230–232.
[11] MEHMET SAGBAS, MUHAMMET KÖKSAL. A new multi-mode multifunction filter using CDBA. Proceedings of the 2005 European Conference on Circuit Theory and Design, 2005, 2(1): p.225-228.
[12] CEVDET ACAR, HERMAN SEDEF. Realization of nth-order current transfer function using current-differencing buffered amplifiers. INT. J. ELECTRONICS, 2003, vol. 90, no. 4, p.277–283.
[13] C. ACAR, S. OZOGUZ. Nth-order current transfer function synthesis using current differencing buffered amplifier: signal-flow graph approach. Microelectronics Journal 31, 2000, p.49–53.
[14] MUHAMMET KOKSAL, MEHMET SAGBAS. A versatile signal flow graph realization of a general transfer function by using CDBA. Int. J. Electron. Commun. (AEÜ) 61, 2007, p.35–42.
[15] UGUR CAM. A novel current-mode second-order notch filter configuration employing single CDBA and reduced number of passive components. Computers and Electrical Engineering 30, 2004, p.147–151.
[16] SADRI ÖZCAN,HAKAN KUNTMAN,OGUZHAN CICEKOGLU. Cascadable current mode multipurpose filters employing current differencing buffered amplifier (CDBA). Int. J. Electron. Commun. (AEU) 56 , 2002, No. 2, p.67–72.
[17] W. TANGSRIRAT, W. SURAKAMPONTORN. Realization of multiple-output biquadratic filters using current differencing buffered amplifiers. International Journal of Electronics, June 2005, Vol. 92, No. 6, p.313–325.
[18] M.KOKSAL,M.SAGBAS. Second order band-pass filter design using single CC-CDBA. Circuits Syst Signal Process ,2008, 27: p. 461–474.
[19] SUDHANSHU, MAHESHWARI, IQBAL A. KHAN. Novel voltage-mode universal filter using only two CDBAs. Journal of Circuits, Systems, and Computers, 2005, Vol. 14, No. 1, p.159–164.
[20] ALI ÜMIT KESKIN. Multi-function biquad using single CDBA. Electrical Engineering, 2006, 88: p.353–356.
[21] TOKER A, ACAR C, ÖZOĞU S. Current-mode KHN-equivalent biquad using CDBAs. Electronics Letters, 1999, 35(20): p.320-324
[22] FANG WEI, WUJIAN 1I. Current-Mode multifunction filters based on current differencing buffered amplifier. Microelectronics Journal, Vol. 32, No. 2, p.2002.
[23] DALIBOR BIOLEK, RAJ SENANI, VIERA BIOLKOVÁ, ZDENĚK KOLKA. Active elements for analog signal processing: classification, review, and new proposals. Radioengineering, December 2008, Vol.17, No.4, p.15-32.
[24] DALIBOR BIOLEK, JOSEF BAJER, VIERA BIOLKOVA, ZDENEK KOLKA, MICHAL KUBICEK. Z copy - controlled gain - current cifferencing buffered amplifier and its applications. Int. Journal of Circuit Theory and Applications, 2011, vol. 39, no. 3, p. 257-274.
[25] WORAPONG TANGSRIRAT, TATTAYA PUKKALANUN, WANLOP SURAKAMPONTORN. CDBA-based universal biquad filter and quadrature oscillator. Active and Passive Electronic Components, Volume 2008, Article ID 247171, 6 pages.
[26]W.TANGSRIRAT,K.KLAHAN,T.DUMAWIPATA,W.SURAKAMPONTORN. Low-voltage NMOS-based current differencing buffered amplifier and its application to current-mode ladder filter design, International Journal of Electronics, November 2006, Vol. 93, No. 11, p.777–791.

NEW UK Hits the Road This Year

20th – 21st March, Event City, Manchester

1st – 2nd May, Royal Highland Centre, Ingliston, Scotland

25th – 26th September, University of West England, Bristol

With time constraints becoming more common in the workplace, not everyone can justify the time out to attend events and, yet, keep in touch with industry, customers and current trends. Mindful of these conditions, the NEW Events team is taking NEW UK on the road in 2013 with three regional events taking place around the country.

Each event promises the education and networking opportunity as well as the chance to meet customers and potential clients in a local, professional environment. Each will also offer a seminar programme, covering key topics, which should help attract local industry.

"These events offer exhibitors the chance to interact with their customers around the UK over the 1½ days of the show. Being able to network with clients in their region offers people the flexibility to get out and see what exhibitors have to offer when perhaps they cannot make a longer drive to other events – and not having to necessarily take a full day out of the office," said Claire Saunders, Event Director.

The three locations have been selected for their supporting infrastructure and ease of access. The three regional events will take place from:

- 20th – 21st March at Event City in Manchester;
- 1st – 2nd May at The Royal Highland Centre in Ingliston, Scotland;
- 25th – 26th September at the University of West England in Bristol.

All of these locations offer great links to motorway networks and have free parking for exhibitors and visitors.

The events will be open from 1pm – 6pm on the first day and 9.30 – 3.30pm on the second.

For more information email info@new-expo.co.uk or call 01483 420 229

A SINGLE SUPPLY LEVEL SHIFTER WITH DIGITAL FILTER

LING-FENG SHI FROM THE INSTITUTE OF ELECTRONIC CAD AND **GUO-HUA QIN** FROM THE XIDIAN UNIVERSITY, BOTH IN CHINA PRESENT THE DESIGN OF A LEVEL-SHIFTER CIRCUIT WITH NMOSFET AND DIGITAL FILTER TO REALIZE A SINGLE POWER SUPPLY AND SUPPRESS INPUT SIGNAL SPIKES

With the development of smartphones, ambient light sensors and proximity sensors are becoming a hot topic. Generally speaking, the chip will require an I²C interface. However, I²C operation voltage is normally different from that of other components. As such, a level shifter circuit is needed to shift one voltage level to another.

Level shifters typically require two voltage supplies: input logic signal voltage supply V_{DDL} and output logic signal voltage supply V_{DDH}. Figure 1 shows the schematic of a conventional half-latch-based level shifter where the V_{DDL} and V_{DDH} are used. When V_{IN} is at ground, MN_1 is turned off and MN_2 is turned on. Then V_{OUTA} is pulled towards ground due to the conducting path established by MN_2. In this case, if V_{OUTA} reaches V_{DDH} - V_{THMP1}, the positive feedback is triggered as MP_1 turns on and pulls V_{OUTB} high. There is no leakage current path between V_{DDH} and GND.

Similarly, when V_{IN} is at V_{DDL}, MN_1 is turned on and MN_2 is turned off. Then V_{OUTB} is pulled towards ground due to the conducting path established by MN_1. If V_{OUTB} reaches V_{DDH} - V_{THMP2}, the positive feedback is triggered as MP_2 turns on and pulls V_{OUTA} high. Again, no leakage current path exists between V_{DDH} and GND.

Certain literature describes devices with static power consumption but these are not suitable for battery-powered applications; and others with dynamic control signals increase system complexity, especially for arrays of level shifters. In a multi-chip system, there is a very huge congestion in the supply routings as the number of supplies increases. Therefore, use of single supply level shifters greatly reduces the supply routing and layout congestion within the chip when a level shifter is required between different voltage domains. The novel design presented in this article avoids these drawbacks while simultaneously improving speed, stability and dynamic power loss.

Circuit Implementation

The level shifter circuit as shown in Figure 2 is composed of a Schmitt trigger, cross-coupled PMOSFETs (M_2 and M_3), two NMOSFETs (M_4 and M_5) and a novel NMOSFET (M_0) whose source-drain terminal could swap according to V_{IN} and V_{DD}. Its working principle is as follows:
When node V_{IN} is high, both M_5 and M_2 turn on, and node V_{OUT} is at power supply level V_{DD}. While node V_{IN} is low, both M_4 and M_3 turn on and node V_{OUT} is at GND. The operational voltage of I²C ranges from 1.7V to 3.6V, and the chip's internal logic operation voltage is 2.15-3.6V. Therefore, a level shifter circuit is required.

When V_{DD} - $V_{I^2C} > V_{TH}$, the drain terminal voltage of M_0 varies with V_{IN} otherwise it is V_{DD} - V_{TH}. M_1 is used to guarantee that the input voltage of the Schmitt trigger is identical to its operational voltage. Both M_2 and M_5 are used to shift the input voltage of the Schmitt trigger (V_{DD} - V_{TH} or V_{I^2C}) to V_{DD}. A detailed discussion is as follows:

(i) Assume an I²C operational voltage of 1.7V and chip operational voltage of V_{DD} 3.6V. When V_{IN} is high (1.7V), M_0 works in the deep linear area so that V_{DS} = 0V. The drain voltage of M_0 is 1.7V, driving M_2 and M_5. The power supply voltage of the Schmitt trigger is V_{DD} - V_{TH} so the output voltage of the Schmitt trigger is low. In this case both M_3 and M_4 are off. Node V_{OUT} will go up to V_{DD}. If node V_{IN} changes from high to low, the output voltage of Schmitt trigger is sufficient (V_{DD} - V_{TH}) to drive M_4. M_3 turns on and the input voltage of INV1 will be charged to V_{DD}; node V_{OUT} is low. To sum up, the level shifter shifts 1.7V to 3.6V correctly.

(ii) In the second situation, assume the I²C operational voltage to be 3.6V and the chip's operational voltage V_{DD} is 2.15V. If node V_{IN} is high at 3.6V, the drain-source terminals of M_0 will swap. At that time the source voltage of M_0 is V_{DD} - V_{TH}; M_5 turns on and pulls down the input voltage of INV1, driving M_2. When the input voltage of the Schmitt trigger is V_{DD} - V_{TH}, its output voltage reverses to drive M_5; M_2 will turn on rapidly. The input voltage of INV1 will be charged to V_{DD}. Initially node V_{IN} is low and the output voltage of the Schmitt trigger is high (V_{DD} - V_{TH}), driving both M_3 and M_4. At that time the input voltage of INV1 is charged to V_{DD}. Node V_{OUT} is switched from high to low. Obviously, the level shifter can shift 3.6V to 2.15V with a high precision.

Based on the above discussion, we conclude that the novel NMOSFET M_0 will sawp its drain-source terminals when V_{IN} is higher than the supply voltage V_{DD}. It guarantees M_0 drain voltage that varies with either V_{DD} - V_{TH} or V_{I^2C}, and then the level shifter shifts the drain voltage to V_{DD}.

The Schmitt Trigger Circuit

The Schmitt trigger is shown in Figure 3. M_1 is the main switch transistor Both M_2 and M_3 work as a feedback network to control the positive trigger voltage V^+. Assume u_i = 0V initially; it increases step by step, and then all of the NMOSFETs turn off because of their V_{GS} is lower than V_{TH}.

$$V_{GS1} = u_i \quad (1)$$

$$V_{GS2} = u_i - V_{DS1} \quad (2)$$

$$V_{GS3} = u_O - V_{DS3} \quad (3)$$

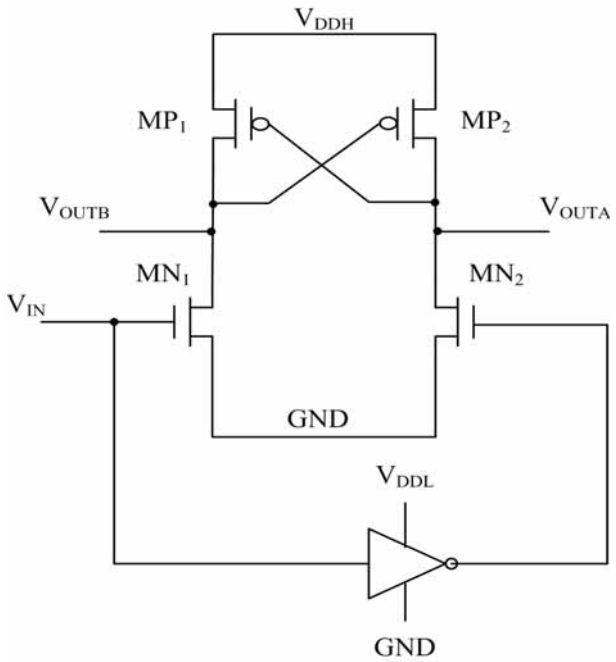


Figure 1: Conventional level shifter

When $V_{GS1} = u_i = V_{IN1}$ M_1 turns on. Assuming M_2 is on, the voltage u_i can be written as Equation 4.

$$u_i = V_{TH2} + V_{DS1} = V^+ \quad (4)$$

The drain-to-source voltage V_{DS1} of M_1 is controlled by a pair of NMOSFETs M_1 and M_3. V_{DS1} decreases gradually with u_i increasing before M_2 reaches the critical conduction-mode point. There will be a discharge path between M_1 and M_2, discharging node V_{OUT} to 0V. The positive trigger voltage is V^+. When M_2 turns on, neglecting bulk effect, the drain-source voltage of M_1 is given by Equation 5.

$$V_{DS1} = V^+ - V_{TH2} \quad (5)$$

At that moment M_1 conducts and operates in the critical saturated area. The voltages across M_1 meet the following equation:

$$V_{GS1} - V_{THN} = V^+ - V_{THN} = V_{DS1} \quad (6)$$

The current flowing through M_1 is given by:

$$I_1 = \frac{\beta_1}{2}(V^+ - V_{THN})^2 \quad (7)$$

$$\beta_1 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \quad (8)$$

At the same time M_3 operates in the saturated area as $V_{GS3} = V_{DS3}$ ($u_o = V_{DD}$). The current through M_3 can be expressed as:

$$I_3 = \frac{\beta_3}{2}(V_{DD} - V^+)^2 \quad (9)$$

$$\beta_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 \quad (10)$$

Due to M_2 working in a critical saturated state, there is no current through M_2, so I_1 is equal to I_3. From Equations 7 and 9, it follows that:

$$V^+ = \frac{V_{DD} + V_{THN}\sqrt{\beta_1/\beta_3}}{1+\sqrt{\beta_1/\beta_3}} \quad (11)$$

From Equation 11, it can be seen that the positive trigger voltage can be regulated by changing the ratio of β_1 to β_3.

$$\frac{\beta_1}{\beta_3} = \frac{(W/L)_1}{(W/L)_3} \quad (12)$$

An analysis of the negative trigger voltage, using the upper half of the

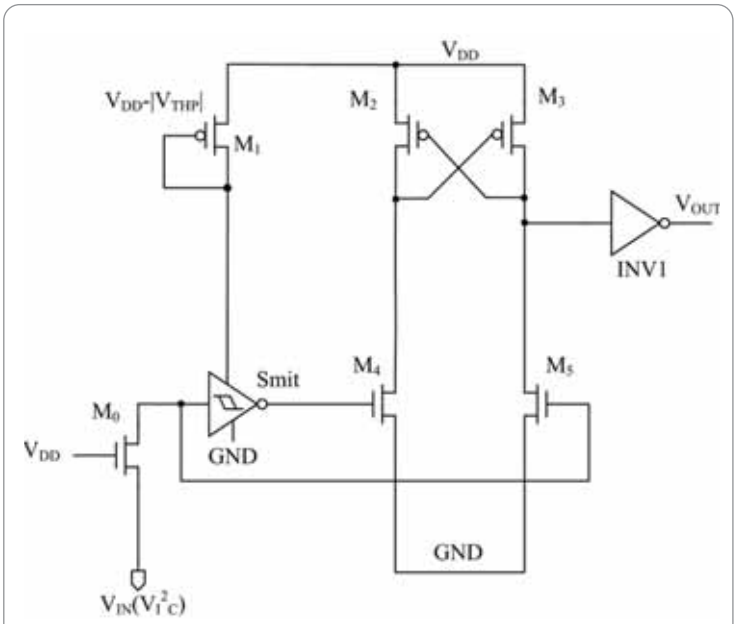


Figure 2: Level shifter with a novel NMOSFET

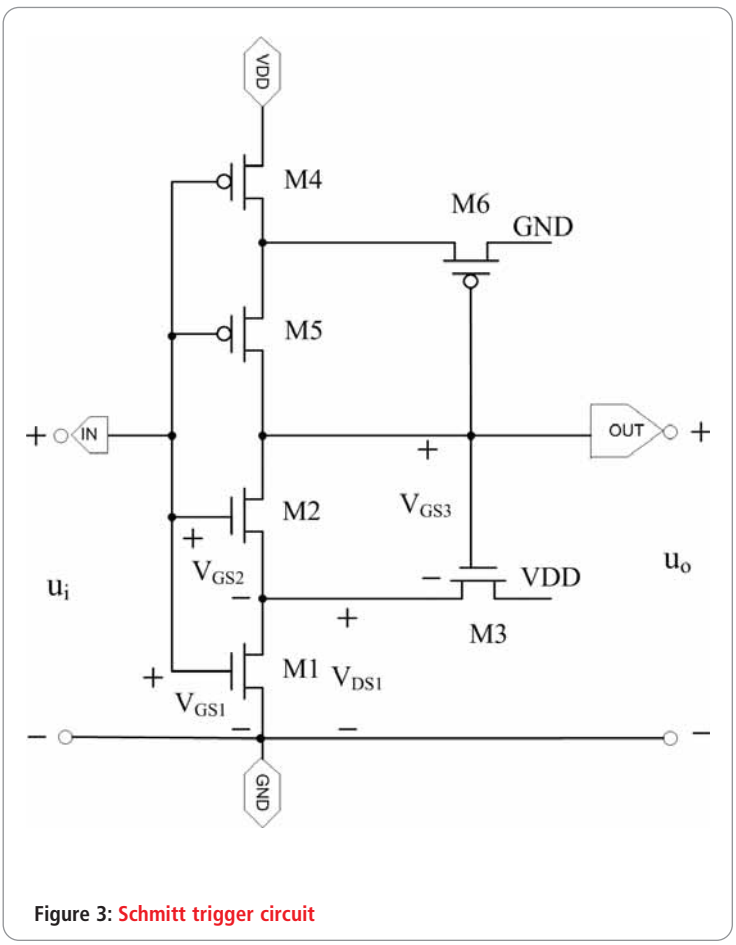


Figure 3: Schmitt trigger circuit

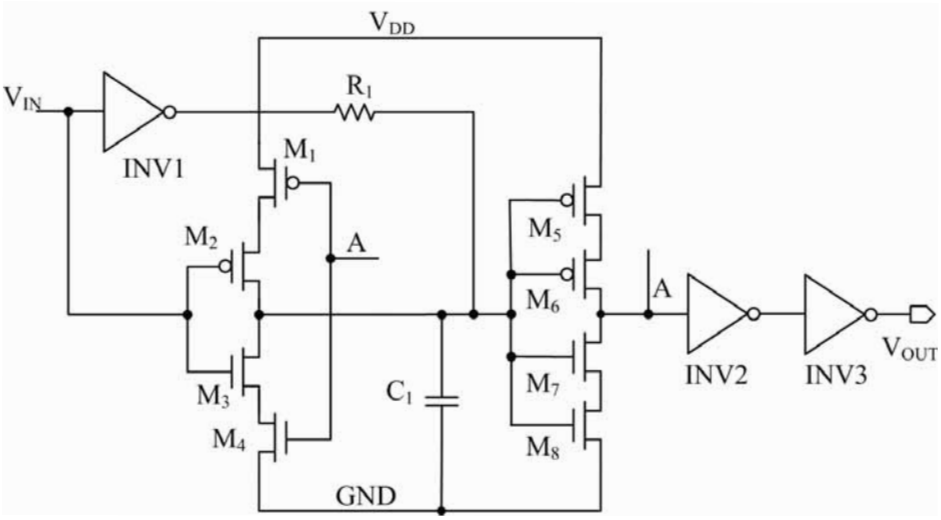


Figure 4: The digital filter circuit

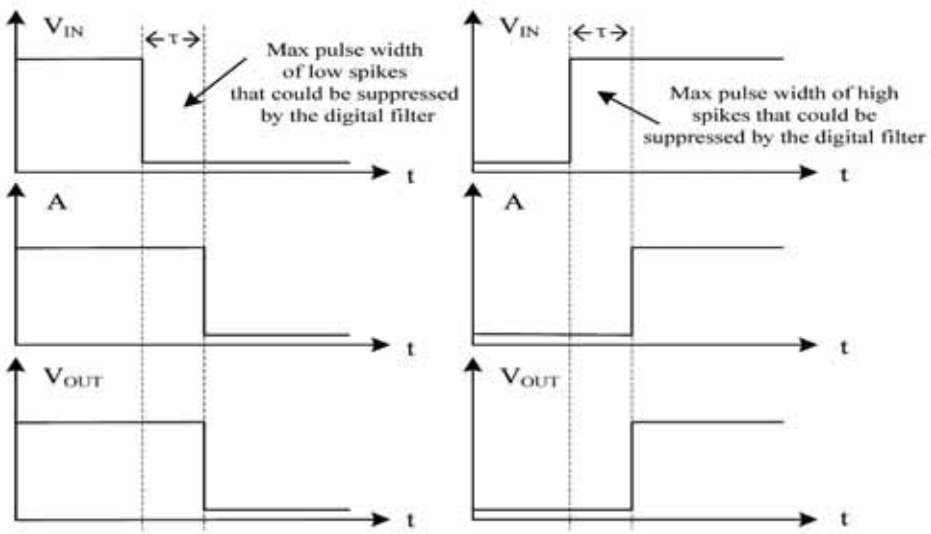


Figure 5: Sketch maps of the two situations: (a) Max pulse-width of low spikes; (b) Max pulse-width of high spikes

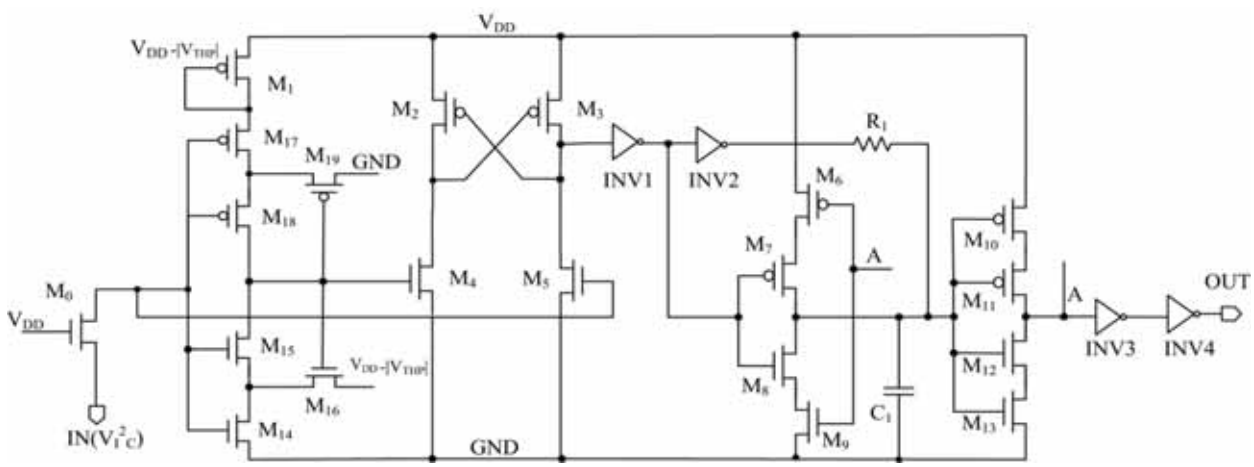


Figure 6: Proposed level shifter

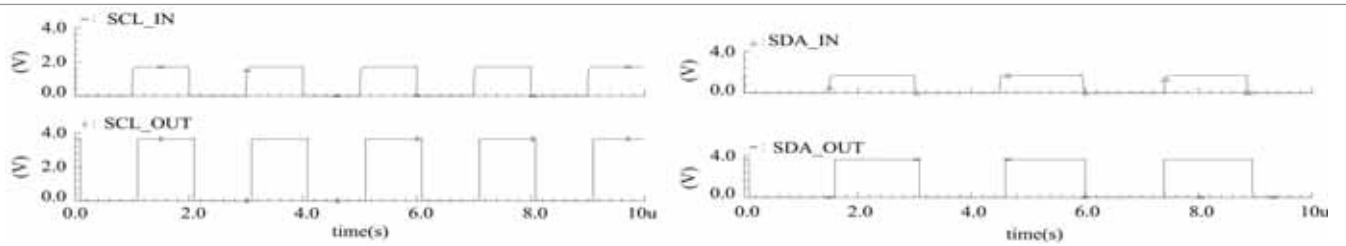


Figure 7: Measured level shift results when V_{I^2C} = 1.7V, V_{DD} = 3.6V

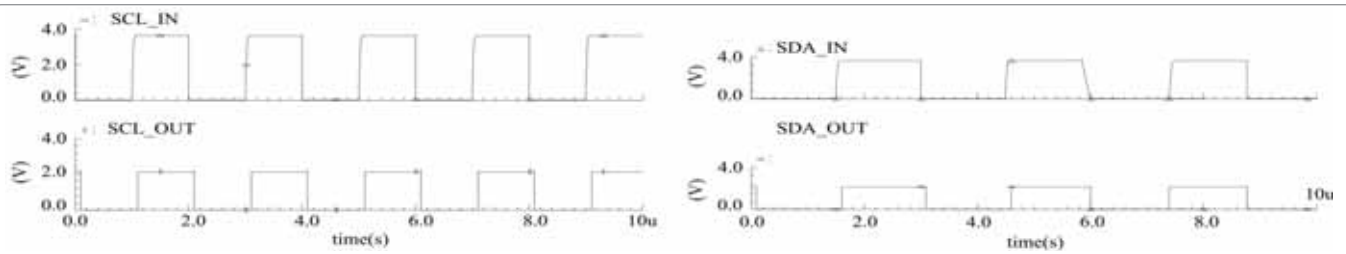


Figure 8: Measured level shift results when V_{I^2C} = 3.6V, V_{DD} = 2.15V

schematic, is similar to that of the positive trigger voltage. Equation 13 is as follows:

$$V^- = \frac{\sqrt{\beta_4/\beta_6}(V_{DD} - |V_{thp}|)}{1+\sqrt{\beta_4/\beta_6}} \quad (13)$$

From Equations 11 and 13, the hysteresis of the Schmitt trigger's input ΔV is written as:

$$\Delta V = V^+ - V^- = \frac{V_{DD} + V_{thn}\sqrt{\beta_1/\beta_3}}{1+\sqrt{\beta_1/\beta_3}} - \frac{\sqrt{\beta_4/\beta_6}(V_{DD} - |V_{thp}|)}{1+\sqrt{\beta_4/\beta_6}} \quad (14)$$

Digital Filter

The digital filter as shown in Figure 4 is used to suppress input signal spikes. Its working principles are as follows:

Assume the input (node V_{IN}) and node A are high, there's no charge on C_1 and the output (node V_{OUT}) is also high. As the input changes from high to low, M_2 turns on and the output of INV1 is high. The current then flows through INV1 and R_1 and charges C_1. When voltage across C_1 reaches the switching voltage of M_5-M_8, node A switches from high to low to drive M_1. Subsequently, the voltage across C_1 is high permanently and the output (node V_{OUT}) switches from high to low. Obviously, node V_{OUT} keeps its status when C_1 is charged.

If V_{IN} is at a high level with a short pulse width of low-level spikes, node V_{OUT} is always high. Similarly, when V_{IN} switches from low to high, M_3 turns on. Then there is a current flowing back into INV1 and R_1 to discharge. As the voltage across C_1 decreases to the switching voltage of M_5-M_8, node A changes from low to high to drive M_4. In this case, the voltage across C_1 is low, permanently. Node V_{OUT} turns high. If V_{IN} is at a low level with a short pulse width of high-level spikes, node V_{OUT} is always low. These situations are shown in Figure 5. The pulse width of the spikes that could be suppressed by the digital filter is determined by the time constant τ dependant on R_1 and C_1:

$$\tau = R_1 C_1 \quad (15)$$

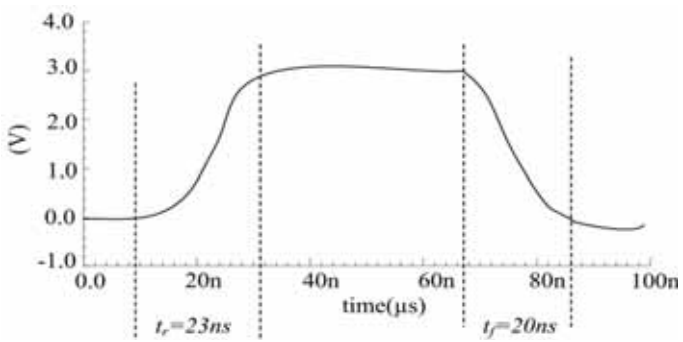


Figure 9: Measured rise time and fall time: (a) High level with low-level spikes; (b) Low level with high-level spikes

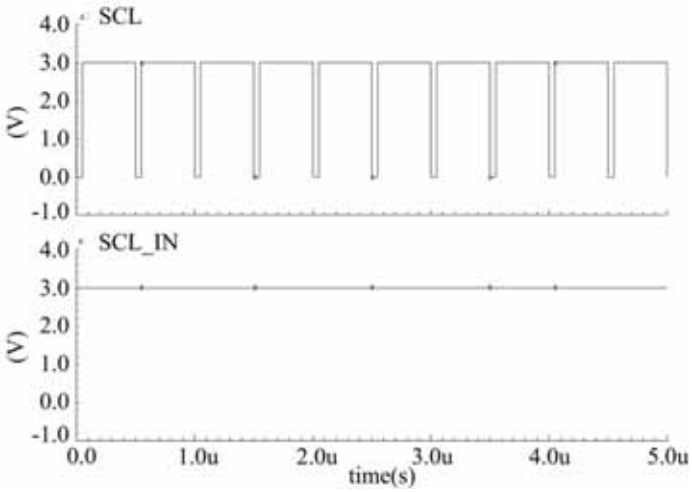


Figure 10a: High level with low-level spikes

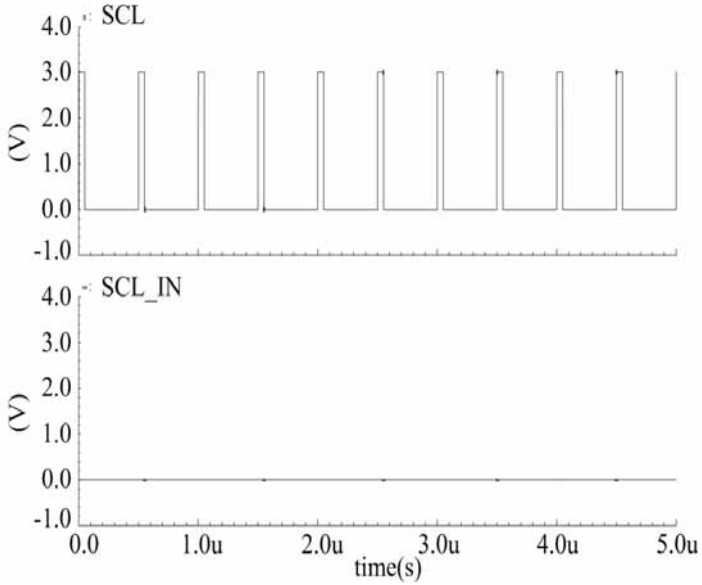


Figure 10b: Low level with high-level spikes

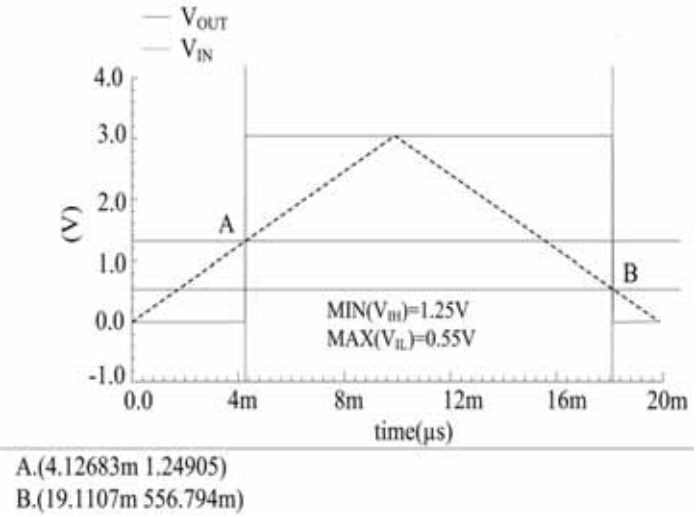


Figure 11: Measured minimum input high voltage V_{IH} and maximum input low voltage V_{IL}

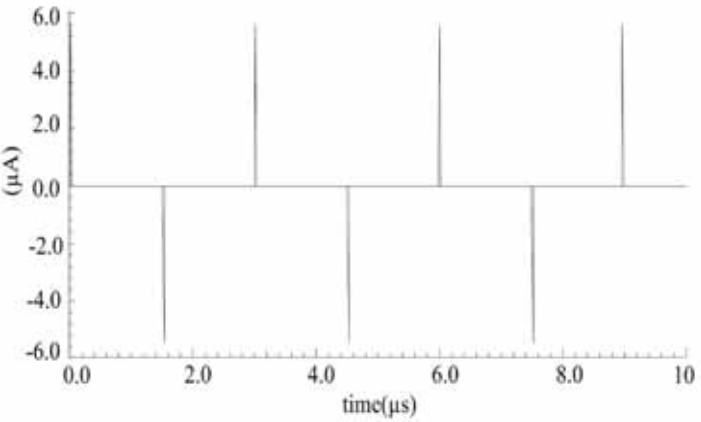


Figure 12: Measured input leakage current for each SDA, SCL pin

Circuit Implementation

The suggested level shifter is shown in Figure 6; its components' parameters are shown in Table 1. To ensure the conventional level shifter circuit operates correctly, an NMOS-to-PMOS (M_4 to M_2 and M_5 to M_3) ratio of 3.25 would be required. In this case we have $V_{THN} = 0.53V$, $|V_{THP}| = 0.73V$ and Equation 14. The hysteresis of the Schmitt trigger input ΔV is:

$$\Delta V = \frac{V_{DD} - |V_{THP}| + V_{THN}\sqrt{\beta_1/\beta_3}}{1+\sqrt{\beta_1/\beta_3}} - \frac{\sqrt{\beta_4/\beta_6}(V_{DD} - 2|V_{THP}|)}{1+\sqrt{\beta_4/\beta_6}} = 0.06V_{DD} + 0.53 \quad (16)$$

Using a typical 3V power supply 3V, the hysteresis of the Schmitt trigger input is approximately 0.71V. Unit resistances and four dummy resistances are used to minimize resistance mismatch. Based on R_1 and C_1 models and parameters, the maximum pulse width of spikes that could be suppressed by the digital filter is approximately 50ns.

Simulation and Test Results

The proposed level-shifter circuit is based on 0.35µm standard CMOS process and is simulated by HSPICE.

As shown in Figure 7, a 500kHz logic signal swinging between 0V and 1.7V is applied at node V_{IN} in Figure 6, and the level shifted level-shifted signals swinging between 0V and 3.6V are obtained at node V_{OUT}.

As shown in Figure 8, a 500kHz logic signal swinging between 0V and 3.6V is applied at node V_{IN} in Figure 6 and the level-shifted signals swinging between 0V and 2.15V are obtained at node V_{OUT}. Figures 7 and Figure 8 demonstrate that the proposed level shifter operates correctly.

Figure 9 shows the simulation results of the rise time and fall time, which are t_r = 23ns and t_f = 20ns respectively. This is sufficient to satisfy the requirements of the application.

Figure 10 shows the capability of the digital filter to suppress spikes at room temperature with 3V supply voltage. The digital filter could eliminate spikes in I²C signal line, preventing damage to the internal logic circuit circuitry.

Figure 11 shows the simulation results of a minimum-input high voltage V_{IL} and maximum-input low voltage V_{IH}. Those values are 0.55V and 1.25V respectively, and the hysteresis voltage is 0.7V. The simulated value is approximately equal to the theoretical value, which proves that the Schmitt trigger works correctly.

Figure 12 shows that the maximum leakage current is approximately 6µA at room temperature with 3V supply voltage, which is low enough for the proposed level shifter to minimize the circuit power loss.

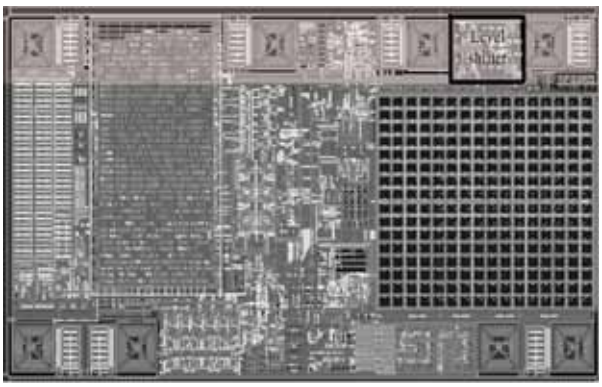


Figure 13: Layout of the level shifter

The circuit is implemented in a 0.35μm CMOS process and its layout is shown in Figure 13. The area of the level shifter is 87 × 96μm^2. There are two signal lines in the I^{2}C interface so two level-shifter circuits are required. To minimize the mismatch of the two, the layout uses a symmetrical structure depicted as a black solid line in Figure 13.

The test waveforms are shown in Figure 14. It can be seen in Figure 14a that the input V_{I^2C} is a 1.7V square wave (red) and V_{DD} 3.6V, the output signal, is a 3.6V square wave (blue). From Figure 14b, the input V_{I^2C} 3.6V is a square wave (red line) and V_{DD} 2.15V, the output signal, is a 2.15V square wave (blue line). Our test results demonstrate that the proposed level shifter can shift 1.7-3.6V on an I^{2}C operational voltage to 2.15-3.6V on-chip internal logic voltage with high precision. ●

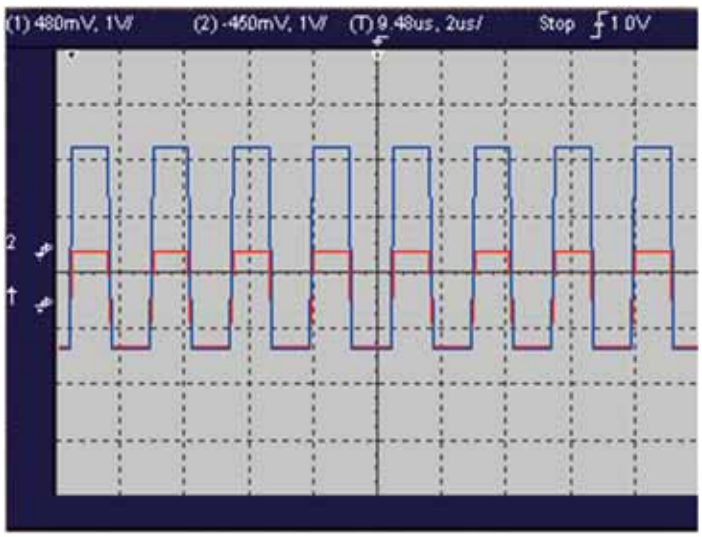


Figure 14a: Test waveform when V_{I^2C} = 1.7V, V_{DD} = 3.6V

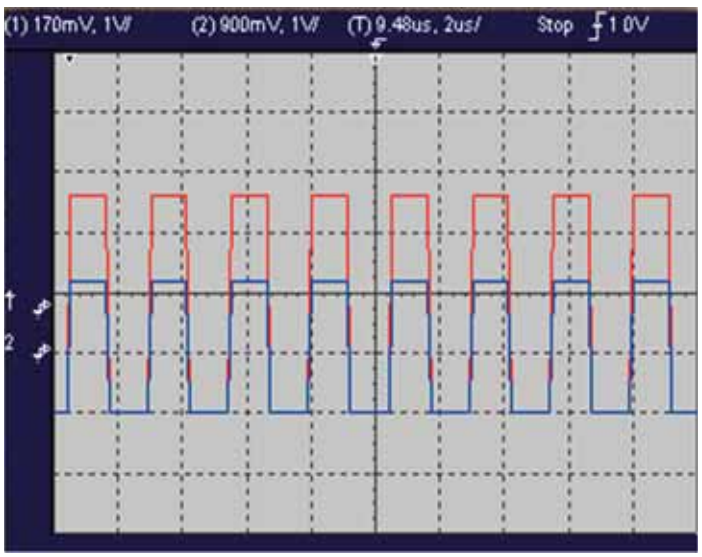


Figure 14b: Test waveform when V_{I^2C} = 3.6V, V_{DD} = 2.15V

(W/L)*number	Components	(W/L)*number	Schmitt trigger	(W/L)*number	Components
(3/0.5)*1	M8	(3/0.5)*2	M14	(2.5/0.5) *1	INV1
(1/1)*1	M9	(3/0.5)*2	M15	(3/0.5) *1	
(4/0.5) *1	M10	(4.5/2)*2	M16	(5/1) *1	INV2
(4/0.5) *1	M11	(4.5/0.5)*2	M17	(3/0.5) *1	
(13/0.5) *1	M12	(2.5/0.5) *1	M18	(5/0.5) *1	INV3
(13/0.5) *1	M13	(2.5/2) *1	M19	(5/0.5) *1	
(6/0.5)*2	R1	2/(14*4)			INV4
(6/0.5)*2	C1	75/14			

Table 1: Parameters of the circuits' components

ASYMMETRICAL PARASITIC INDUCTANCE USED TO REDUCE SWITCHING LOSSES IN POWER MODULES

MICHAEL FRISCH, TECHNICAL MARKETING MANAGER AT VINCOTECH IN GERMANY, AND **TEMESI ERNÖ**, APPLICATION ENGINEERING MANAGER AT VINCOTECH IN HUNGARY,

PRESENT A NEW POWER MODULE CONCEPT THAT COMBINES LOW INDUCTIVE TURN-OFF WITH THE UTILIZATION OF PARASITIC INDUCTANCE

One frequently-encountered design goal in its own right is creating high-efficiency power conversion circuits. This is especially true in the solar inverter business where the aim is to develop the most efficient topologies using components with the lowest power dissipation.

Equally, reducing switching losses is the basis for higher switching frequencies, which leads to a reduction in the size and weight of the passive components. An efficiency improvement from 96% to 99% reduces the requirement for cooling by a factor of four. It is obvious that high efficiency circuits are the smartest way to achieve compact design and highest power density.

Using parasitic inductance and some basic power-electronics rules we can offer a new power-electronics solution based on standard silicon components that can extend traditional designs. The new power module concept combines low inductive turn-off and parasitic inductance for the reduction of turn-on losses. In addition we use three-level switching circuits with fast-switching paralleling based on low forward voltage drop components.

Development Goals

The goal of this development project is to reduce switching losses in power applications of over 100kW with screw-type modules. The main limitations in such applications are the parasitic effects of stray inductance [7,8] and the reverse recovery behaviour of the diodes [5]. The overvoltage spike caused by parasitic inductance will limit the turn-off switching speed. The losses and increased electromagnetic interference (EMI) caused by the reverse recovery behaviour of the freewheeling diode are the drawbacks to increased turn-on switching speed.

First, parasitic inductance is reduced to a minimum to solve the issue with turn-off. The turn-on losses are then reduced. This is achieved by utilizing the parasitic inductance at turn-on by keeping the inductive turn-off behaviour low. The third step in reducing switching losses is to introduce a neutral point clamped (NPC) inverter topology. Finally, a special topology for paralleling MOSFETs with IGBTs is introduced to show the advanced prospects of the idea. The feasibility of the new concept is proven with a power module concept incorporating all the discussed arrangements.

Theory of Switching Losses (Inductive Load)

Power dissipation in power electronics is caused by conductive and switching losses. The conductive losses are defined by the forward voltage drop in the semiconductor. The switching losses are dependent on the switching speed of the transistor, the reverse recovery behaviour of the diode, the serial inductance and other parasitic effects.

In a system with inductive load (see Figure 1), the freewheeling diode conducts at turn-on and the output voltage equals the negative DC-bus voltage (DC-). The transistor then starts to conduct.

As soon as the transistor takes over the total output current, the output voltage will reach the positive DC-bus voltage (DC+). The

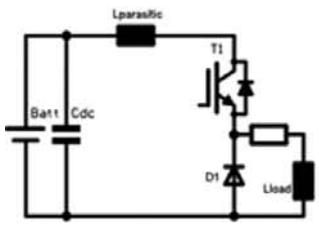


Figure 1: Switching circuit with inductive load

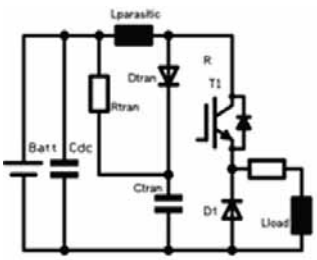


Figure 2: Asymmetrical inductance in a switching circuit with feedback to the main DC-link

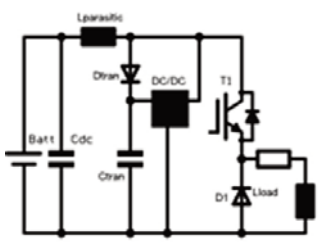


Figure 3: Asymmetrical inductance in a switching circuit with regeneration of the stored energy

diode faces reverse voltage and will conduct in the reverse direction. This causes losses in the diode (E_{REC}) and it increases the current in the transistor. This current peak is often the root cause of EMI in the system.

After the diode is completely recovered and blocking, the current in the transistor will fall back to the level of the output current. The turn-on process is now complete. An increased serial inductance with the transistor will reduce the turn-on losses. The energy stored in the serial inductance is calculated according [9]:

$$E_L = ½*L * I^2$$

At turn-off the voltage at the transistor will reach the DC-bus voltage level. The diode will take over the output current. The overvoltage will cause additional losses but might also destroy the transistor. The use of fast transistors is limited by the inductance and the maximum current, as the voltage peak is dependent on the turn-off speed. The stored energy in the series inductance of the DC-input causes a voltage overshoot according to [1]:

$$V_{CE}(peak) = V_{CE} + L \times di/dt$$

Low Inductive Module Technology

With the new low inductive module technology [3] we achieve:

- Fast and reliable turn-off in high-current power modules;
- Switching loss reduction (turn-off);
- The lower voltage overshoot at turn-off allows the use of fast components;
- The reduced inductance will not reduce the switching losses at turn-on. The turn-off losses will decrease but the turn-on losses of the transistor and the reverse recovery losses in the diode will increase even more [4]. The efficiency of the low inductive circuits will increase with the use of fast components. To lower the turn-on losses without increasing EMI requires ultra-fast freewheeling diodes.

Asymmetrical Inductance

Next we increase the turn-on inductance but lower the turn-off inductance at ultra-low levels. This approach is named 'asymmetrical inductance'. One way to achieve the new switching behaviour is to use the parasitic inductance $L_{parasitic}$ at turn-on, and bypassing it during turn-off. The diode D_{tran} (see Figure 2) conducts the stored energy of the parasitic inductance during turn-off to the integrated capacitor C_{tran}.

The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. With this circuit we are able to release the semiconductor from switching losses but some energy has to be dissipated in the passive components. One option is to increase the efficiency regenerating the stored energy with a DC-DC circuit (see Figure 3).

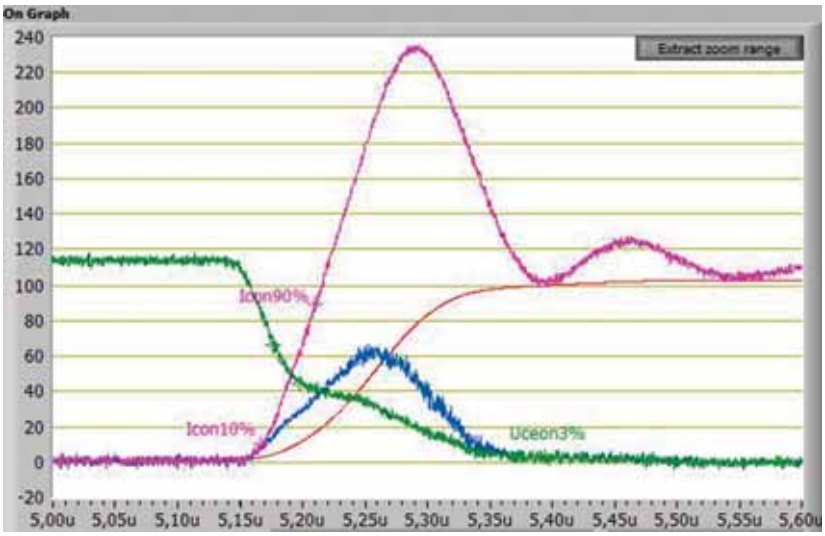


Figure 4: IGBT turn-on characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

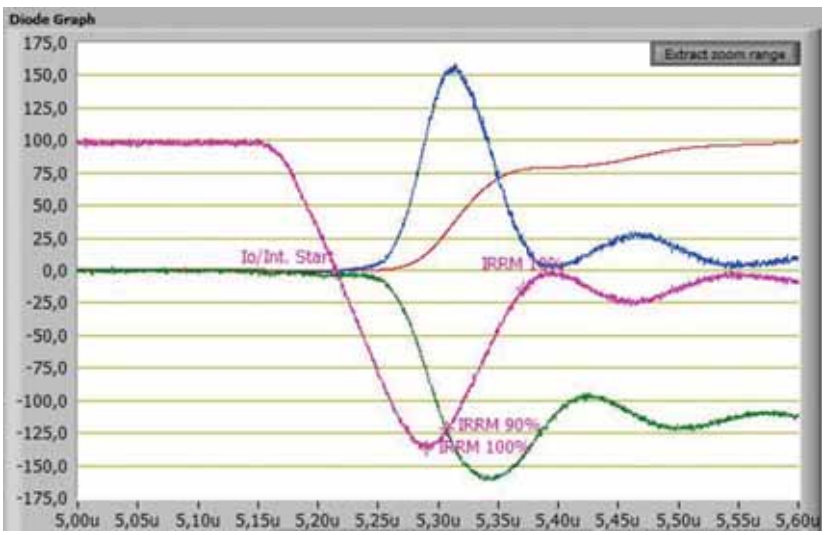


Figure 5: Diode characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

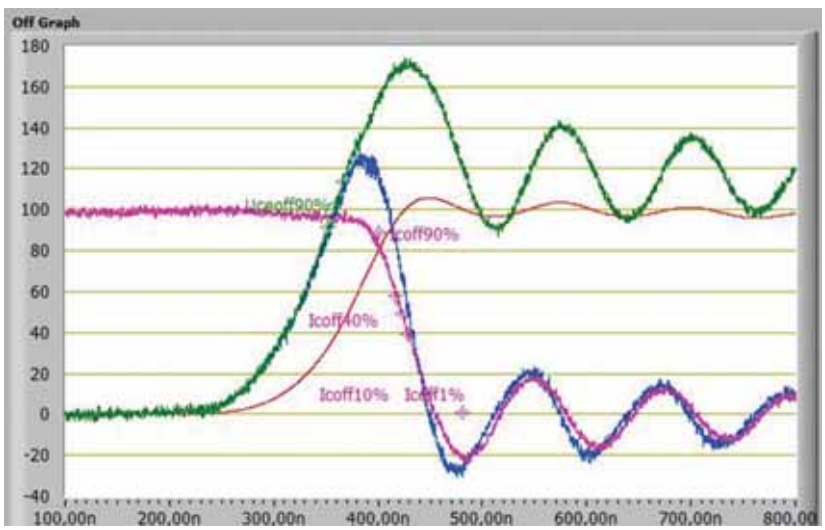


Figure 6: IGBT turn-off characteristics with symmetrical inductance. L[ON] = L[OFF] = 50nH

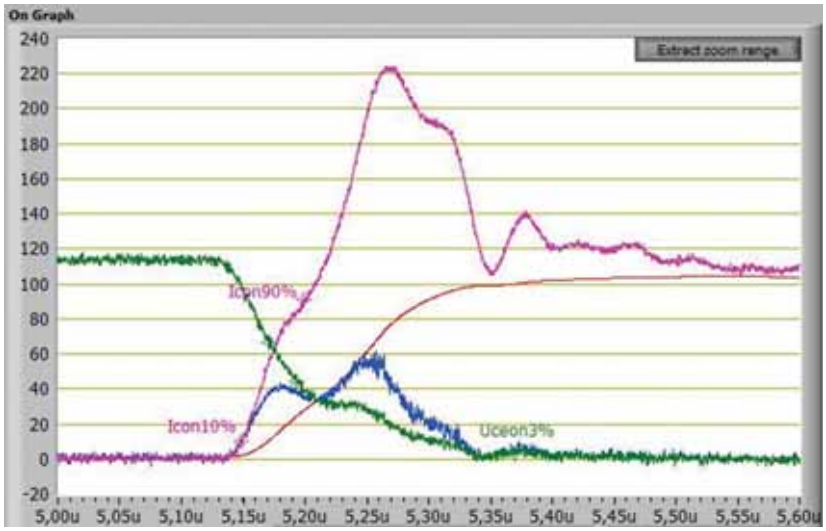


Figure 7: IGBT turn-on characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

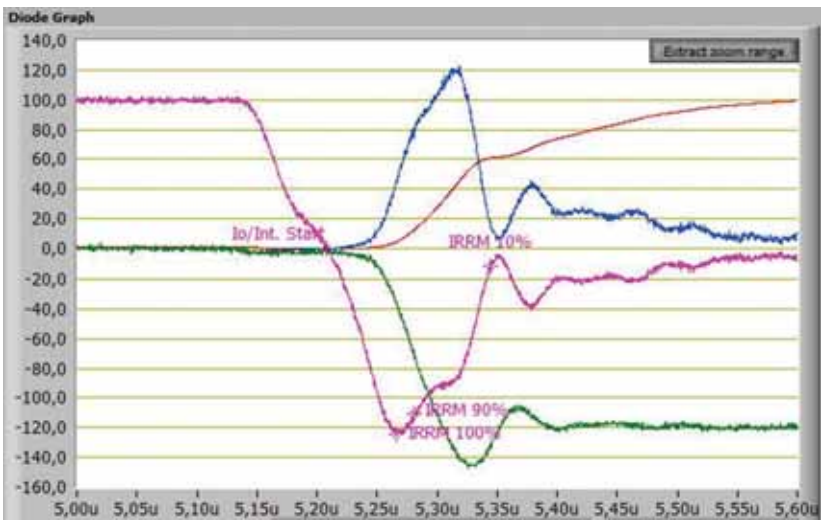


Figure 8: Diode characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

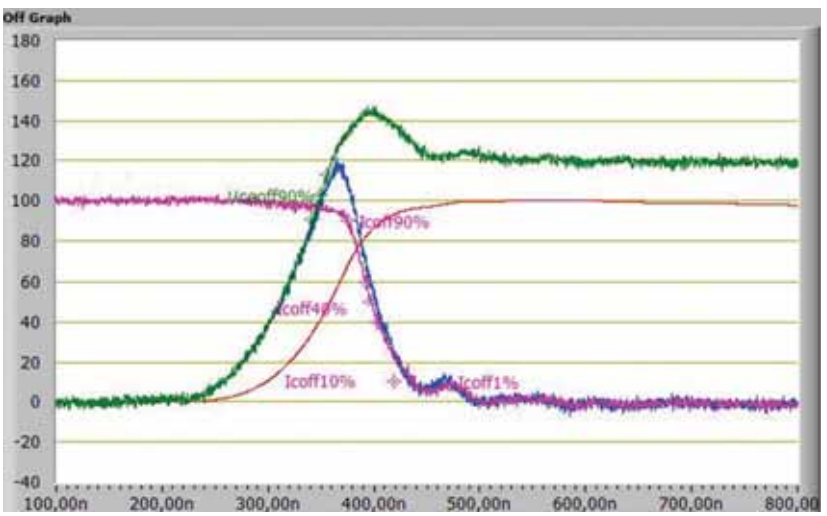


Figure 9: IGBT turn-off characteristics with asymmetrical inductance. L[ON] = 50nH, L[OFF] = 5nH

The idea of asymmetrical inductance is verified with the comparison of different parasitic inductances in a traditional power-module setup and asymmetrical setup with integrated snubber capacitors.

Test conditions include: R_G = 2Ω (±15V), V_{DC} = 600V, I_{OUT} = 400A and an Infineon component – HS 3/1200V/400A.

The results include E_{ON} = 16.92mJ, E_{OFF} = 27.78mJ, E_{REC} = 31.78mJ. The switching losses are fine but more important is the voltage overshooting at turn-off. The most critical case is the turn-off at low temperatures. At 25°C the overvoltage is measured at approximately 180%, which limits the use to 650V. In the test the module failed at 720A/600V/TJ = 25°C.

An identical measurement is then performed with asymmetrical inductance of 50nH at turn-on and 5nH at turn-off.

Results include E_{ON} = 15.487mJ, E_{OFF} = 25.66mJ, E_{REC} = 28.27mJ. The switching losses of the new asymmetrical setup are lower. Surprisingly, not only the turn-off losses are reduced, but all switching losses are reduced. The reason for the loss reduction at turn-on is the reverse recovery behaviour of the circuit. At turn-on the current of the transistor T_1 is increased by the reverse recovery current through diode D_1. After the recovery is complete, the current is reduced but the additional energy is stored in the parasitic inductance $L_{parasitic}$, which causes an overvoltage on the collector of the transistor, compared with the positive voltage in the transient capacitor C_{tran}. So, the energy flows into the capacitor. This reduces the reverse current in the diode and the voltage drop in the transistor, which results in a significant reduction of the switching losses.

With the asymmetrical inductance circuit, it is possible to increase the inductance further to take advantage of the turn-on loss reduction. In a setup with $L_{parasitic}$[ON] = 90nH, $L_{parasitic}$[OFF] = 5nH, we get the following results:

E_{ON} = 12.44mJ, E_{OFF} = 25.77mJ, E_{REC} = 26.70mJ

Asymmetrical Inductance Advantages

With asymmetrical inductance we have the following advantages:

- **Superior switching performance with standard components:** The new circuit improves the efficiency without investing in special components. It is possible to reduce the switching losses with standard components.
- **Reduced EMI:** The increased turn-on inductance reduces peak current in the transistor. This is the major source of EMI.
- **No bus-bars are required:** Inductance in the DC input is now welcome and will cause a further loss reduction at turn-on. Consequently, expensive laminated bus-bars for a low-inductance connection with the DC capacitor bank are not required any more. This might be the most significant advantage of the new approach.
- **Reduced voltage swing of the onboard capacitors.** The onboard capacitors will not

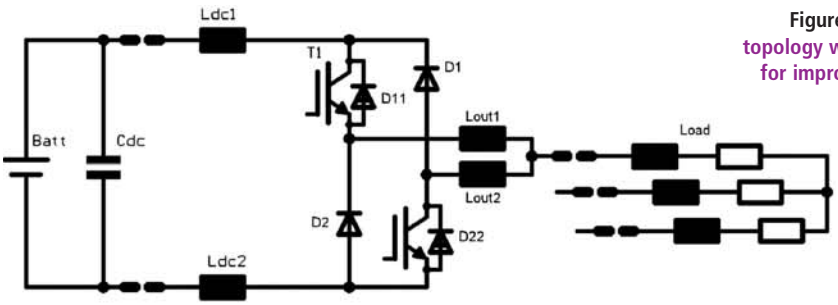


Figure 10: Pseudo half-bridge topology with decoupled branches for improved switching behavior

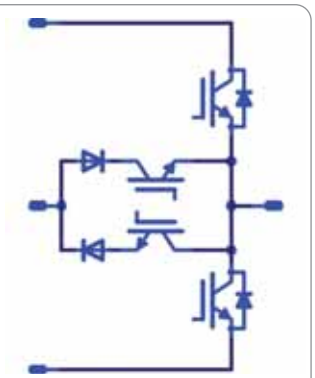


Figure 11: Mixed voltage NPC circuit

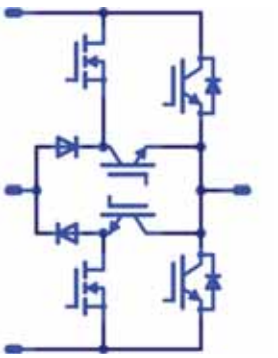


Figure 12: Advanced paralleled NPC circuit

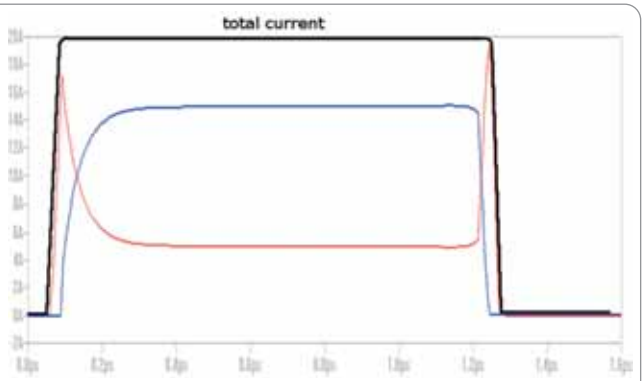


Figure 13: Current sharing in the parallel switch system. Current in the MOSFET (red), current in the IGBT (blue)

discharge during turn-on, reducing the voltage swing and dissipation in the capacitors.

Decoupling of Upper and Lower Transistor

The circuit in Figure 10 is a solution for reducing turn-on losses due to the output capacitance of the complementary switching device and the elimination of cross conduction during turn-on. The goal of this idea is to decouple the output transistors. In this circuit the output is divided into two branches and the parasitic inductance of the output connection is used to decouple the components. The corresponding diodes are connected as shown for achieving a low inductive commutation loop.

The use of multi-level topology as neutral point clamped inverter (NPC) or a mixed-voltage NPC inverter halves the voltage at the switching transistor, which reduces switching losses [2]. On top of this loss reduction, the freewheeling diodes can be selected for only half the voltage, e.g. 600V instead of 1200V.

Advanced Paralleling

In advanced paralleling the target is to merge the advantages of:

- Standard NPC. This topology requires components with half the voltage rating. Faster components are available at low voltage.
- Mixed voltage NPC [6] (see Figure 11). The output current faces only one junction, leading to reduced static losses.
- Parallel switch. This is paralleling of a fast component (e.g. a MOSFET) with a low voltage drop component (e.g. an IGBT). The loss reduction is achieved by rendering the static losses of the switch to the IGBT and the dynamic losses to the MOSFET. Even better is to use a so-called mixed-voltage NPC topology and parallel it with just 600V MOSFETs and 1200V IGBTs (see Figure 12).

In the advanced paralleled NPC topology the original idea of paralleling a MOSFET with an IGBT is maintained (see Figure 13). The MOSFET and the IGBT are turned on simultaneously. The MOSFET is the faster device so it will take over the current at turn-on. The IGBT will turn on with zero voltage. The voltage drop in the IGBT is lower, so the IGBT will take over the majority share of the current. At turn-off the gate signal of the MOSFET is delayed. The IGBT will turn off and the MOSFET will take over the current and turn off with a delay of around 100ns.

Performance Verification of the Advanced Paralleled Topology

Measurements show that the advanced paralleled NPC topology is able to cut the switching losses in half.

The inverter now reaches more than 99% efficiency with a PWM switching frequency of 16kHz. At the switching frequency of 64kHz, the efficiency is still above 98% (see Figure 14). So the main benefit of the advanced paralleled NPC topology is to halve the switching losses, compared to the mixed voltage NPC.

Power Module Definition

The combination of all these ideas leads to the following power module specification:

- 200kVA output power at 20kHz.
- Asymmetrical parasitic inductance with energy regeneration.
- Decoupling of low-side and high-side switches.
- Three level topology.
- Paralleling of fast MOSFETs or IGBTs with components with low static losses.

The power module concept includes:

- 1200V/500A power rating.
- Asymmetrical parasitic inductance with onboard snubber capacitors (5nH turn-off inductance) and DC-DC

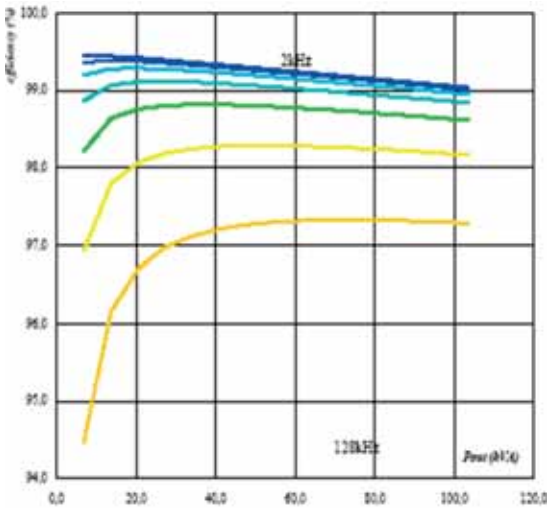


Figure 14: Advanced paralleled NPC: Efficiency vs switching frequency, in steps from 2kHz to 128kHz, is doubling in each step – 2 (blue), 4, 8, 16, 32 (green), 64 (yellow), 128kHz (orange)

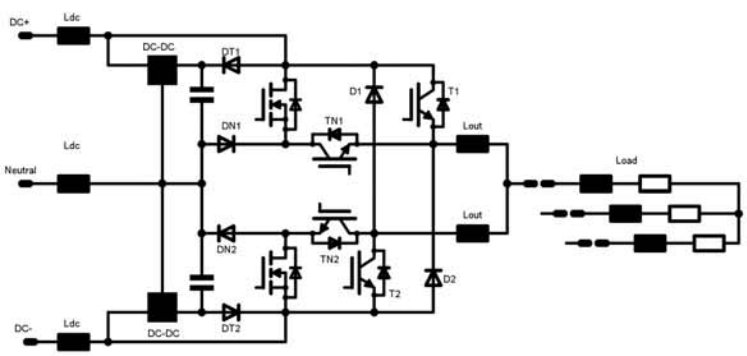


Figure 15: Power module concept for a 3-phase advanced paralleled NPC with asymmetrical inductance and regeneration circuit

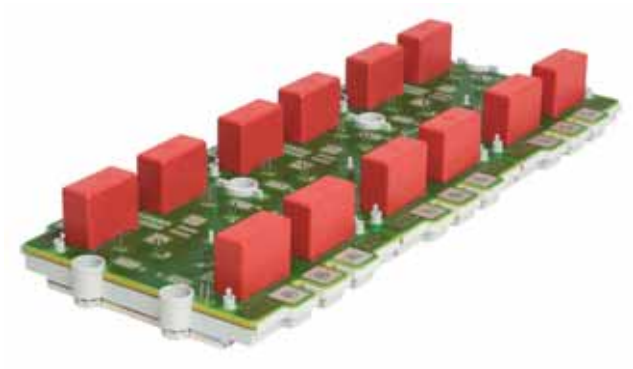


Figure 16: Power module with integrated snubber capacitors and asymmetrical inductance

regeneration circuit.

- Separated outputs for high- and low-side circuits for decoupling of the corresponding switches.
- 3-phase advanced paralleled mixed voltage NPC topology.

The results are shown in Figures 15 and 16. The inductance shown in the schematics is the parasitic inductance of the power module setup.

Increasing the Efficiency of Switching Components

Along with the advantages of new technologies such as SiC or GaN switching devices, it is still possible to increase the efficiency of standard silicon components. To extend traditional power designs we have to remember the basics of power electronics:

- The low-inductance module concept ensures fast and reliable turn-off in high-current power modules and reduces voltage overshoot.
- The power module setup with very low internal parasitic elements is uses external stray inductance for a reduction of switching losses without having to invest in expensive high-speed semiconductor technology. The asymmetrical inductance leads to lower switching losses, reduced EMI and minimized effort for the inverter mechanics. Low-inductance bus-bars are no longer needed either. A flexible low-cost cable connection in the DC link can be used. The increased serial inductance will enable a further reduction of the turn-on losses.
- The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50kHz and above. ●

REFERENCES

[1] Siemens: "IGBT Fundamentals", May 1997
[2] Michael Frisch and Temesi Ernö: "Advantages of NPC Inverter Topologies with Power Modules", Vincotech Germany and Hungary 2009
[3] Michael Frisch and Temesi Ernö: "Power Module with Additional Low Inductive Current Path", Vincotech Germany and Hungary 2009
[4] Wilhelm Rusche and Marco Bässler: "Influence of Stray Inductance on High-Efficiency IGBT Based Inverter Designs", Infineon Technologies, Warstein, Germany 2010
[5] Peter Haaf, Jon Harper: "Diode Reverse Recovery and its Effect on Switching Losses", November 2006:
[6] Akira Nabae, Isao Takahasi, Hirofumi Akagi: "A New Neutral-Point-Clamped PWM Inverter", September/October 1981
[7] Dr Paul Chr. Mourick: "Parasitic Inductivities and Parasitic Oscillations an Overview", 24. Feb. 2011
[8] Dr Eckart Hoene: " Parasitic Effects – An overview", ECPE, Feb. 2011
[9] Helmut Lindner, Dr Harry Brauer, Dr Constans Lehmann "Elektrotechnik", 1982 (page 82)

DIGITAL POWER TELEMETRY REDUCES ENERGY CONSUMPTION AND IMPROVES SYSTEM UPTIME

ACCURATE MEASUREMENT OF THE REAL-TIME POINT-OF-LOAD POWER CONSUMPTION ENABLES THE DESIGN OF INTELLIGENT SYSTEMS THAT MEET THE DESIGN GOALS WITH MINIMUM ENERGY USE. BY **KALIN LAZAROV**, APPLICATIONS ENGINEER, MIXED SIGNAL PRODUCTS AT LINEAR TECHNOLOGY CORPORATION

Although power management is critical to the reliable operation of modern electronic systems, without the means for directly configuring or monitoring key power system operating parameters voltage regulators are perhaps the last remaining "blind spot" in today's systems. Digitally-programmable DC/DC converters have been available for many years, most notably in voltage regulator module (VRM) core power supplies with voltage identification (VID) output voltage control. But the ability to monitor operating status information directly from the voltage regulator, especially real time real-time currents, has been missing.

A principal benefit of digital power system management is reduced design cost and faster time-to-market. Complex multi-rail systems can be efficiently developed using a comprehensive development environment with an intuitive graphical user interface (GUI). Such systems also simplify in-circuit testing (ICT) and board debug by enabling changes via the GUI instead of soldering in "white wire" fixes. Another benefit is the potential to predict power system failures and enable preventive measures, thanks to the availability of real-time telemetry data. Perhaps most significantly, DC/DC converters with digital management functionality allow designers to develop 'green' power systems that meet target performance (compute speed, data rate, etc.) with minimum energy usage at the point-of-load, board, rack and even installation levels, reducing infrastructure costs and the total cost of ownership over the life of the product.

Need for Accurate Lossless Current Measurement

Advances in DC/DC converter design make significant efficiency improvements difficult, and the next generation of power systems will reduce the power consumption through system-level dynamic load balancing. The algorithms controlling point-of-load converters need highly accurate power consumption data in order to fine-tune the models and optimize power distribution. This is where the benefits of real-time telemetry, combined with high analog accuracy, become apparent.

Measuring power consumption with high precision requires a known resistive element to measure the output current. While a calibrated external shunt is accurate, it introduces additional power loss and makes the converters more expensive. A lossless alternative is

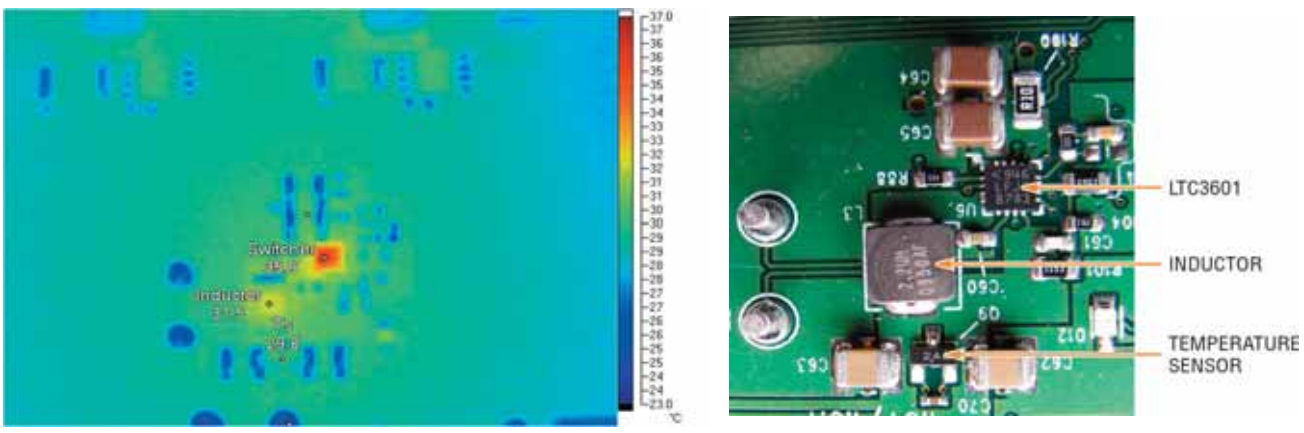


Figure 1: Thermal image of a DC/DC converter showing the difference between the actual inductor temperature and the temperature sensing point

to measure the average voltage drop across the parasitic DC resistance of the inductor (DCR), which saves component count and simplifies board layout. Compared to other lossless measurement techniques such as SenseFET, DCR current measurement is more cost-effective and simpler to use.

One significant drawback of the DCR method is the strong temperature dependence of the inductor resistance, and the difficulty in measuring the exact inductor core temperature. Without proper temperature compensation, a change in inductor temperature of only 1°C corresponds to approximately 0.39% current measurement error. To make matters worse, inductor self-heating of tens of degrees can be observed at high loading levels. The algorithm described next (patent pending) can compensate for all these effects and, when calibrated, achieves accuracy better than ±0.25% across the full temperature and load current range.

DCR Temperature Compensation

Placing a temperature sensor in close proximity to the inductor provides first-order temperature compensation. The accuracy of temperature compensation is increased if the temperature sensor is away from other significant heat sources, such as power FETs. Heat dissipation in the inductor under high load conditions creates transient and steady state thermal gradients between the inductor and the temperature sensor, and the sensed temperature does not accurately represent the inductor core temperature. This temperature gradient is clearly visible in Figure 1, which shows a thermal image of the integrated DC/DC converter LTC3601 providing 1.8V, 1.5A to the output load.

In addition, transient heating/cooling effects have to be accounted for in order to reduce the transient errors introduced when load current changes are faster than the heat transfer time constants of the inductor. Both of these problems are addressed by introducing two additional parameters: the thermal resistance θ_{ls} from the inductor core to the on-board temperature sensor, and the inductor thermal time constant τ. The thermal resistance θ_{ls} [°C/W] is used to calculate the steady-state difference between the sensed temperature T_s and the internal inductor temperature T_i for a given power dissipated in the inductor P_i:

$$T_i - T_s = \theta_{ls} P_i = \theta_{ls} V_{dcr} I_{out} \qquad (1)$$

The additional temperature rise is used for a more accurate estimate of the inductor DC resistance R_i:

$$R_i = R_0\left(1 + \alpha\left(T_s - T_{ref} + \theta_{ls} V_{dcr} I_{out}\right)\right) \qquad (2)$$

In the equations above V_{dcr} is the inductor DC voltage drop, I_{out} is the root-mean-square (RMS) value of the output current, R_0 is the inductor DC resistance at the reference temperature T_{ref}, and α is the temperature coefficient of the resistance. Since most inductors are made of copper, we can expect a temperature coefficient close to $\alpha_{Cu} = 3900\ ppm/°C$. For a given α the remaining parameters θ_{ls} and R_0 can be calibrated at a single temperature using only two load currents:

$$R_0 = \frac{(R_2-R_1)(P_2+P_1)-(R_2+R_1)(P_2-P_1)}{\alpha(T_2-T_1)(P_2+P_1)-(P_2-P_1)\left(2+\alpha\left(T_1+T_2-2T_{ref}\right)\right)} \qquad (3)$$

$$\theta_{ls} = \frac{1}{\alpha R_0}\frac{\alpha(R_1+R_2)(T_2-T_1)-(R_2-R_1)\left(2+\alpha\left(T_1+T_2-2T_{ref}\right)\right)}{\alpha(T_2-T_1)(P_2+P_1)-(P_2-P_1)\left(2+\alpha\left(T_1+T_2-2T_{ref}\right)\right)} \qquad (4)$$

The inductor resistance $R_k = V_{dcr,k}/I_{out,k}$, power dissipation $P_k = V_{dcr,k} I_{out,k}$ and the sensed temperature T_k, $(k = 1,2)$ are recorded for each load current. To increase the accuracy in calculating θ_{ls}, the two load currents should be chosen around $I_1 = 10\%$ and $I_2 = 90\%$ of

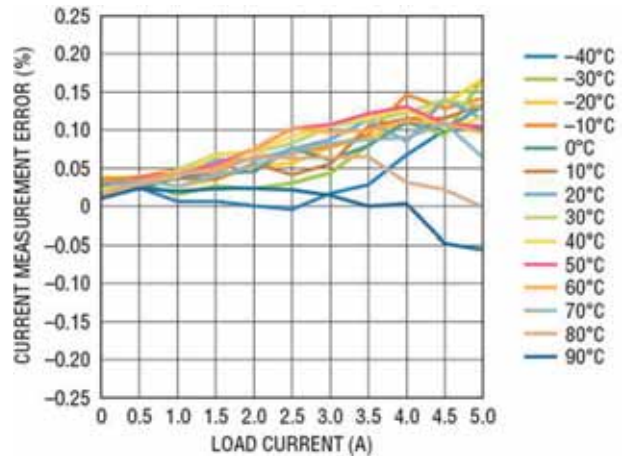


Figure 2: Total current measurement error of the LTC2974 for a DC/DC converter across the full range of temperatures and output currents

HIGH PRECISION DIGITAL TELEMETRY USING LTC2974

LINEAR TECHNOLOGY'S NEW LTC2974 IS A QUAD SYSTEM SUPERVISOR THAT INCORPORATES A 16-BIT DATA ACQUISITION SYSTEM WITH BEST-IN-CLASS ±0.25% TOTAL UNADJUSTED ERROR.

It provides digital read back of output voltages, currents and temperature on all four monitored DC/DC channels, using industry standard PMBus interface. The current measurement uses the described DCR temperature compensation algorithm and achieves order of magnitude higher accuracy compared to the prior solutions (Figure 2). The LTC2974 enables great system flexibility, based on the device's combination of telemetry with precision, fast, hardware supervision; trim DACs and comprehensive set of sequencing; and tracking options. The device's onboard high-reliability EEPROM enables completely autonomous operation, without the need to develop software.

The LTC2974 includes a fault logging capability via an interrupt flag along with a "black box" recorder that stores the state of the converter operating conditions just prior to a fault. Multi-rail system development is facilitated though Linear Technology's LTpowerPlay development software and GUI interface.

the current range of the system.

The inductor thermal time constant τ models the first-order thermal response of the inductor and allows accurate DCR compensation during load transients. During a transition from low to high load current, the inductor resistance increases due to self-heating. If we apply a single load step from the low current I_1 to the higher current I_2, the voltage across the inductor will change instantaneously from I_1R_1 to I_2R_1 and then slowly approach I_2R_2. Here R_1 is the steady-state resistance at the given temperature and load current I_1, and R_2 is the slightly higher DC resistance at I_2, due to the inductor self-heating. Note that the electrical time constant $\tau_{el} = L/R$ is several orders of magnitude shorter than the thermal one, and "instantaneous" is relative to the thermal time constant.

The two settled regions give us the data sets (I_1, T_1, R_1, P_1) and (I_2, T_2, R_2, P_2) and the two-point calibration technique (3-4) is used to extract the steady-state parameters θ_{ia} and R_0 (given a previously characterized 'average' α). The relative current error calculated using the steady-state expression (2) will peak immediately after the load step, and then decay to zero with the inductor thermal time constant τ.

$$\left(\frac{\Delta I}{I}\right)(t) = \alpha\,\theta_{ia}(V_2I_2 - V_1I_1)e^{-t/\tau} \qquad (5)$$

The time constant τ is calculated from the slope of the best-fit line $y = \ln(\Delta I/I) = a_1 + a_2 t$:

$$\tau = -\frac{1}{a_2} \qquad (6)$$

In summary, a single load current step is all that is needed to calibrate the DCR current measurement. The stable portions of the response give us the thermal resistance θ_{ia} and nominal DC resistance R_0, and the settling characteristic is used to measure the inductor time constant τ. After the self-heating parameters θ_{ia} and τ are characterized once for a particular system, only the inductor DC resistance R_0 needs to be calibrated to compensate for the inductor tolerance.

Precision lossless current measurement is key to optimizing power consumption of large systems and allows the development of accurate models. The availability of real-time power consumption telemetry is crucial in the diagnostics of system "health" and can be used to prevent potentially disastrous power system failures. ●

JINXUE SUI, LI YANG, YAN ZHANG AND **AIMING NIE** FROM YANTAI, CHINA, DESCRIBE THE DESIGN OF A LOW-POWER MSP430 MCU DEVELOPMENT BOARD

Design of An Ultra-Low Power Angle Measuring Instrument

Inclination measuring instruments are widely used in many sectors including architecture, geology, aviation, oil exploration and others. Their measuring principle is based on the instruments' sensitivity to gravity. This article suggests a new method of measuring inclination, and includes the design of a new angle-measuring instrument suitable for various engineering applications.

System Design

The proposed measurement system consists of a microcontroller, power supply module, angle measuring device, data display and a test control unit.

The MSP430 microcontroller is based on a 16-Bit RISC mixed-signal processor from Texas Instruments (TI). All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for the source operand and four addressing modes for the destination operands. MSP430 can offer high speed, ultra-low power consumption and overall good performance. In addition, it has clock speed of 16MHz and five low-power modes. Considering its reliability, functionality, compatibility, power consumption and price, it is the perfect MCU for our project.

The data display module uses an LCD screen and a built-in HT1621 driver, also a low-power device.

MMA7361LC Acceleration Data Collection Module

The angle measuring module uses the MMA7361LC sensor which is a low-power, low-profile, capacitive micromachined accelerometer featuring signal conditioning, a one-pole low-pass filter, temperature compensation, self-test, zero-g detect which detects linear freefall, and g-select which allows for the selection between two sensitivities. The zero-g offset and sensitivity are factory set and require no external devices. The MMA7361LC includes a Sleep Mode that makes it ideal for handheld, battery-powered electronic systems.

The default force axis of the accelerometer is the horizontal direction, i.e. the tension is 0 in the direction of the horizontal axis, and the acceleration α is 0. When the accelerometer is tilted, angle θ is produced between the force axis and the horizontal line, so the value of the gravity component can be described as $F = Mg\cos\theta$, the acceleration α on the axis is $g\cos\theta$. Within the 0 to 90 degrees range, the relationship between α and θ is 1:1, in line with the inverse triangle formula $\arccos(\alpha) = \theta$, as shown in Figure 2.

The MMA7361LC is used for detecting gravity acceleration in three axial directions, with the output voltage changing in accordance with movement and direction. When there's no gravity acceleration, its signal output is 1.65V. If it moves, the output voltage will vary depending on the gravity acceleration component of each axis. The signal measurement process is shown in Figure 4.

Inclination Angle Measurement and Conversion

The accelerometer is maintained stationary on the slope as shown in Figure 5. In accordance with Newton's second law: the rate of change of the momentum of the object is proportional to the external force, and occurs in the direction of this external force. At this time, since the accelerometer is stationary relative to Earth, the factor that will change the accelerometer's output voltage is the Earth's gravitational acceleration g in the direction of the sensing axis.

A/D conversion functions are then applied to convert this voltage into a digital value to compute the angle. As shown in Figure 3, when the object is positioned, the gravity component values of X, Y, Z axis are G_{ax}, G_{ay}, G_{az}. Firstly, the X and Y gravity acceleration components

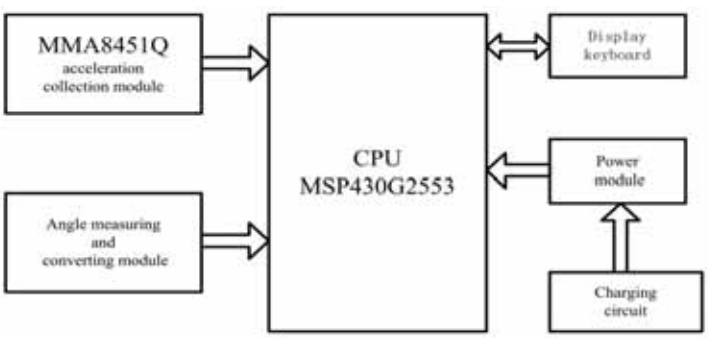


Figure 1: System structure diagram

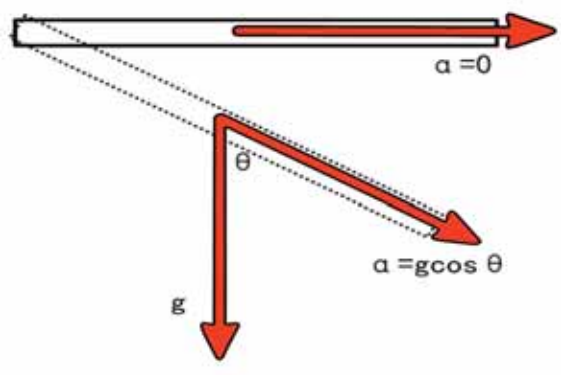


Figure 2: Acceleration

SHANDONG INSTITUTE OF BUSINESS AND TECHNOLOGY IN ANGLE MEASURING INSTRUMENT BASED ON A 16-BIT

THIS NEW REGULAR FEATURE COVERS ISSUES RELATED TO CHINESE RESEARCH AND DEVELOPMENT (R&D)

are calculated through G_{ax} and G_{ay}:

$$G_{axy} = \sqrt{G_{ax}^2 + G_{ay}^2}$$

and then the inclined angle is calculated with Gaxy and G_{az}:

$$\theta = \arctan(G_{axy} / G_{az}).$$

System Hardware Design

The chip features include: a low voltage power supply (1.8V-3.6V), 16MHz clock, five low-power modes; eight inputs, ten 200Ksps ADCs; two 16-bit Timer A, an USCI (universal serial communications interface), UARTs, SPI and IIC functions, a comparator, 16KB Flash memory, 512B RAM and a clock.

Overall system power consumption can be reduced by using the MMA7361LC's sleep mode and interrupt function, relieving the main processor from continuously polling data.

When testing the power consumption of the system, the power supply uses a 2200uf/25V electrolytic capacitor. The LM2577-ADJ booster module raises the voltage to 25V to charge the capacitor. The MCU and the accelerometer use three regulators, keeping the output voltage stable at 3.3V during the capacitor's discharge process, providing power to the whole angle measurement system.

Under the above testing conditions, the capacitor can be used continuously for 60 seconds or longer, and it can be used for measurements more than 10 times, while keeping the system of low power consumption. Thus in daily use, a power supply run by three batteries will last a long time.

System Software Design

In dormant state the MCU detects an interrupt signal to wake up. Following that:

(1) When the button is pressed, an interrupt is produced, entering the corresponding interrupt service sub-program, followed by the data processing program.

(2) After the data processing program begins, the MCU continues to scan the state of the two buttons. If the measurement button is pressed, the next measurement will proceed; if the switch button is pressed, then the display content is switched, and a 10-second timer is set.

(3) At that point the MCU enters hibernation state and waits for the test button to trigger the next measurement.

Testing and Results

The experiment's results can be seen in Table 1.

If the two sensing axis of the accelerometer are working properly, we can achieve more accurate results. The whole system

	Angle (degrees)			Acceleration(m/s2)				
Number	Angle	Measured value	X	X test value	Y	Y test value	Z	Z test value
1	0.0	0.8	0.00	0.20	0.00	0.14	9.80	9.79
2	5.0	5.3	0.00	0.10	0.85	0.91	9.76	9.76
3	10.0	10.9	0.00	0.10	1.70	1.85	9.65	9.62
4	15.0	15.4	0.00	0.06	2.54	2.60	9.47	9.45
5	20.0	20.7	0.00	0.04	3.35	3.46	9.20	9.17
6	25.0	24.9	0.00	0.08	4.14	4.13	8.88	8.89
7	30.0	29.5	0.00	0.24	4.90	4.83	8.49	8.52
8	35.0	35.2	0.00	0.04	5.62	5.65	8.03	8.01
9	40.0	40.1	0..00	0.02	6.30	6.31	7.51	7.49
10	45.0	45.0	0.00	0.02	6.93	6.93	6.93	6.93
11	50.0	50.2	0.00	0.06	7.50	7.53	6.30	6.28
12	55.0	54.8	0.00	0.02	8.03	8.01	5.62	5.65
13	60.0	60.5	0.00	0.14	8.49	8.53	4.90	4.83
14	65.0	65.4	0.00	0.06	8.88	8.91	4.14	4.08
15	70.0	69.4	0.00	0.18	9.21	9.17	3.35	3.45
16	75.0	75.1	0.00	0.14	9.47	9.47	2.54	2.52
17	80.0	80.1	0.00	0.13	9.65	9.65	1.70	1.68
18	85.0	84.7	0.00	0.13	9.76	9.76	0.85	0.91
19	90.0	90.3	0.00	0.19	9.80	9.80	0.00	0.05

Table 1: Measurement data.
Angle precision ±1, acceleration component accuracy ±0.3

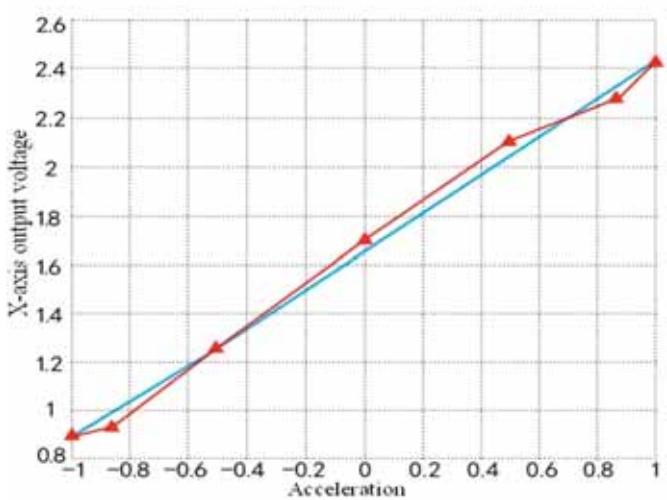


Figure 3: Output response in the direction of the X-axis

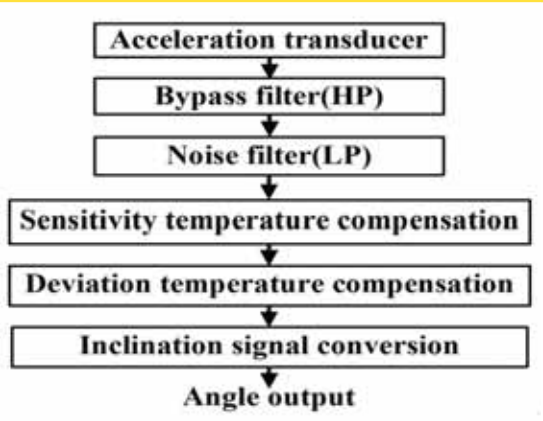


Figure 4: Signal measurement process

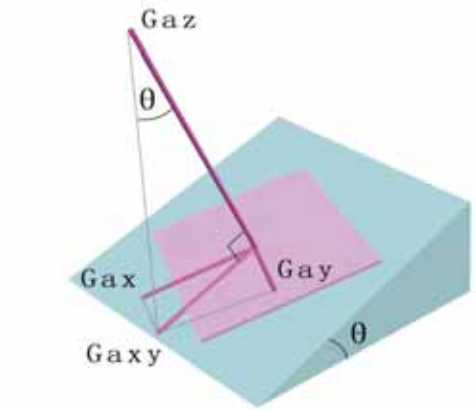


Figure 5: Acceleration measured angle schematic

structure ensures that the interface is connected correctly, the accelerometer is placed on a smooth, vibration free surface. If the accelerometer and the MCU are an integrated solution this will reduce noise interference and the measurements will be even more accurate.

Errors can be introduced into the system by mechanical instability of the device itself. Therefore, if the accelerometer and the MCU are an integrated system placed on a smooth, vibration free surface, and if the two sensing axes of the accelerometer are working properly, their measurements will be even more accurate. ●

Figure 6: Acceleration measured angle schematic

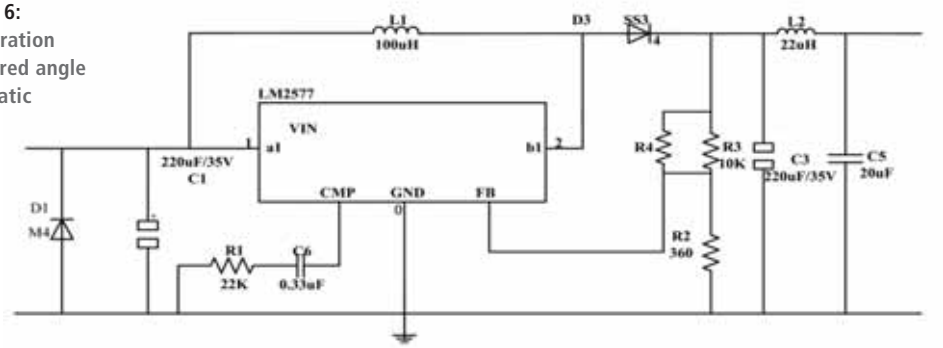
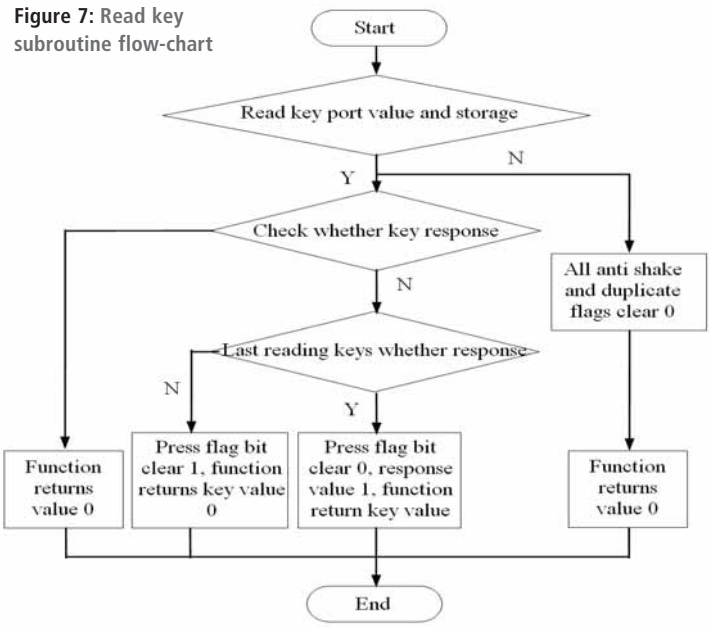


Figure 7: Read key subroutine flow-chart



REFERENCES

[1] MSP430 series 16-bit ultra-low power Microcontroller Theory and Application. Tsinghua University Press, 2004.11.
[2] Qin Long. MSP430 microcontroller modules and integrated system. Electronic Industry Press, 2007.7.
[3] Su Weijia, Wang Xuhui. Application and research of a new accelerometer in angle measurement. Mechanical research and application, 2007,10:62-64.
[4] Xu Xiaoxiang,Chen Wenxiang, Ye Junjun. Design of an angle measuring system based on three-axis acceleration sensors. Sensor World, 2012, 07.
[5] Tina Xiaofang, Lv Qiyong, Xiong Chao. Design of Tilt-Sensor Based on Accelerometer.Chinese Journal of Sensors and Actuators, 2006,19(2):361-365.
[6] Wen Xiangwen, Pan Minghua. Research on characteristic of the inclinator and compensation for its measurement error. Transducer and Microsystem Technologies, 2011, 30(3):84-87.

This work is supported by NSF 60970105; NSF of Shandong Province ZR2010FL015 and ZR2010FL021; Ministry of Housing and Urban-Rural Development of the People's Republic of China (MOHURD) Development science and technology project 2010-K9-26; Department of Housing and Urban-Rural Development of Shandong province Development science and technology project 2011YK059.

THIS IS A MONTHLY COLUMN COVERING ISSUES RELATED TO TEST AND MEASUREMENT (T&M)

Finding That Signal Integrity Sweet Spot

BY **REG WALLER**, EUROPEAN DIRECTOR, ASSET INTERTECH INC

There's a sweet spot – actually many of them – in your computer, smartphone and just about every electronic system imaginable. These are those places where something is happening just the way it should. That is, whatever the process, it's been optimized.

When this happens, everyone's happy, or at least they should be. Unfortunately, hitting these sweet spots is becoming more difficult every day.

Chips are getting so fast, circuit boards are so complex and we're in such a hurry to get product to market fast that validating certain factors that have a big effect on system performance – those sweet spots – does not always have the priority it should. One such factor, and a very important one at that, is the integrity of signals on high-speed SerDes (serializer/deserializer) I/O buses and links to high-speed memories like DDR2/DDR3. It's on these buses where technology is conspiring against us because as bus speeds continue to increase, the sweet spot for signal integrity becomes increasingly difficult to hit.

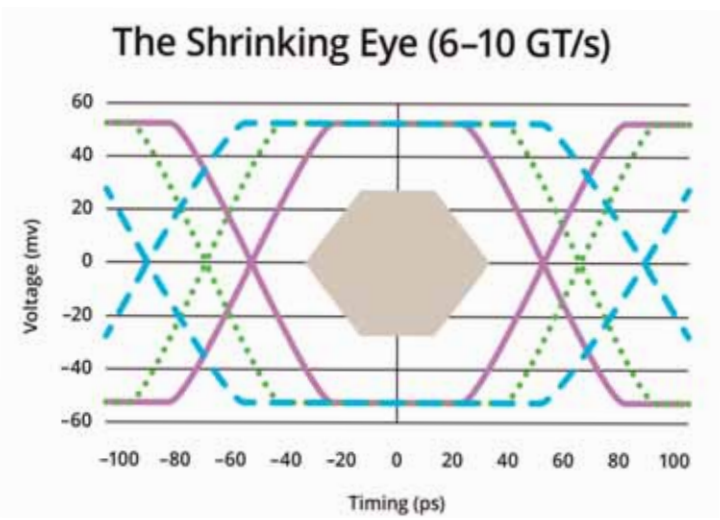


Figure 1: The effect of the increasing bus speeds: 6Gbps (broken line), 8Gbps (dotted line) and 10Gbps (solid line)

Shrinking Eye Diagrams

Factors like jitter, inter-symbol interference (ISI), crosstalk and others can create havoc on signal integrity because operating margins decrease as signal frequencies increase with each new generation of high-speed bus. With each step upward to a higher speed and higher signalling frequency, a chip-to-chip interconnect on a circuit board becomes more susceptible to distortions and anomalies which disrupt bus traffic and stall system throughput.

The composite eye diagram in Figure 1 illustrates the effects of increasing signal frequencies on three generations of a hypothetical high-speed bus and the resulting decreasing operating margins. Increasing bus speeds from 6 Gigabits per second (Gbps) (broken line) to 8Gbps (dotted line) and eventually 10Gbps (solid line) shows how the signalling closes in on the operational 'no-go' zone in the center of the diagram. As frequencies increase, the margin between an acceptable signalling path and the out-of-spec path in the centre of the diagram becomes slimmer.

To avoid slowdowns in bus speeds, signal integrity should be validated during each of the major phases of a system's life cycle, including design/development, manufacturing and when installed in the field. If the signal integrity on a SerDes channel is not what it should be, steps should be taken to correct the problem and improve system performance.

If detected during prototype board bring-up, signal integrity problems could trigger changes in the design. If found during manufacturing, out-of-spec signalling could result in alterations to production processes. If detected in the field as a result of troubleshooting poor performing systems, design changes should be made in the next generation of the system and/or in the manufacturing process in order to reduce returns and warranty claims.

This kind of life-cycle signal integrity validation is not widespread today. To avoid problems that shrinking operating margins can cause, signal integrity validation must become a regular, routine process. All too often in today's hyper-competitive world of low profit margins, signal integrity validation is neglected in order to meet the demands of a quickly closing window of opportunity.

Legacy measurement tools haven't helped the situation either. External, intrusive test tools, based on probing a chip or a board, are losing their effectiveness and becoming too expensive, especially

> *All too often in today's hyper-competitive world of low profit margins, signal integrity validation is neglected*

when one considers the constant pressure on profit margins that most electronic products are under.

In many cases legacy external testers rely on test pads for access to the underlying bus. As signal frequencies increase on high-speed buses, placing a probe on the bus to monitor signal integrity becomes less feasible because of the capacitive coupling effects that probes and test pads implanted in boards have on sensitive bus signalling. In fact, today's best practices in high-speed board design typically prohibit test pads on circuit boards.

Fortunately, some would say trends are already changing when it comes to test and measurement methods. This shift involves a change in perspective and it will facilitate the deployment of signal integrity validation throughout the entire life cycle. I'm referring to tools that are fast, reliable, efficient, cost-effective and economical because they are software-based. These non-intrusive embedded instruments are able to monitor and analyze signal integrity inside chips and boards – from the inside out – instead of from the perspective of an external probe-based tester.

For years semiconductor vendors have embedded instruments into their high-performance devices for chip test purposes. Recently, these embedded instruments have been re-applied beyond their original limited application to provide a more cost-effective and straightforward way to gather empirical signal integrity data by monitoring and reporting data as it is received at the receiver on a chip. With this sort of good, solid data, we've got a better chance of hitting those sweet spots. ●

WHITE PAPER

TO FIND OUT MORE ABOUT THIS TOPIC READ THE WHITE PAPER CALLED "BANDWIDTH TESTS REVEAL SHRINKING EYE DIAGRAMS AND SIGNAL INTEGRITY PROBLEMS" AT: http://www.asset-intertech.com/Products/High-Speed-I-O-Validation/HSIO-Software/e-Book-Shrinking-Eye-Diagram

Belden Adds New Hirschmann PowerMICE

Belden, a global supplier of signal transmission solutions for mission-critical applications, introduces in the EMEA region the new PowerMICE, third generation of the Modular Industrial Communication Equipment family from its Hirschmann product portfolio.

This modular switch for DIN rail mounting offers comprehensive network protection for the first time. The switch incorporates security mechanisms that regulate network access and protect against attacks. These include port security, DHCP Snooping, Dynamic ARP Inspection, IP Source Guard, ingress/egress ACL, sFlow, Storm Control, automatic Denial-of-Service prevention and port access control via 802.1x including multi-client authentication, Radius VLAN/policy assignment and guest/unauthenticated VLAN. Hardware redundancy methods such as PRP (Parallel Redundancy Protocol) and HSR (High Availability Seamless Redundancy) also ensure uninterrupted data communication. As a result, this IPv6-ready switch allows applications to be implemented where both an extremely high level of network security and network availability are required. It can also be seamlessly integrated into PROFINET and EtherNet/IP environments. The integrated PoE Plus function allows for cost-effective power supply for terminal equipment.

The new PowerMICE is available in three basic versions for 12, 20 or 28 ports and

comprises a switch unit with integrated backplane and a 4-port Gigabit Ethernet media module. Depending on the version, the switch can be individually fitted with up to six additional 4-port Fast Ethernet media modules for twisted pair cables, different optical fibre types or I/O functionality.

Media modules can be assembled quickly without tools using a click-in mechanism. Modules can be removed just by using a screwdriver to lift a tab attached to the switch. For applications that require a high level of vibration resistance, modules can also be fastened using screws.

The switch meets all relevant industry standards and also offers high shock and vibration resistance. The temperature range is 0°C to +60°C. Optional versions are also available for ambient temperatures from -40°C to +70°C. Their circuit boards can be specially coated (conformal coating) on request to protect against condensation.

Power can be supplied via 18-60 VDC or 47-57 or 53-57 VDC. In addition, devices can be supplied with power via PoE Plus via the data cable. Depending on the power supply configuration, up to 120 Watts can be supplied via the backplane of the switch.

The switch status can be monitored locally. Detailed information can be displayed via a standard web browser. The integrated SNMP interface offers an additional centralized management function that makes it possible to use network management software such as Industrial HiVision. Configuration and diagnostics can be carried out with HiDiscovery, IHV or via a web interface.

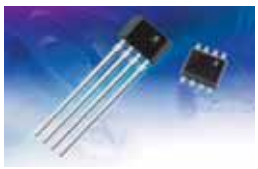
www.hirschmann.com
www.belden.com
or e-mail
inet-sales@belden.com

BELDEN
SENDING ALL THE RIGHT SIGNALS

Belden
Stuttgarter Straße 45-51
72654 Neckartenzlingen
Germany
Phone: +49 7127 14 0
www.Beldensolutions.com

Dual-Channel Hall-Effect Direction Detection Sensor IC

The new A1233 from Allegro MicroSystems Europe is a dual-channel, Hall-effect direction detection sensor IC that provides digital output signals indicating the speed and direction of a rotating target. It is a highly sensitive, temperature-stable magnetic sensing device ideal for use in ring-magnet based speed and direction systems in harsh automotive and industrial environments.



A key feature of the device is the Hall sensing elements are photolithographically aligned to better than 1µm. This accurate mechanical location between the two active Hall elements eliminates the major manufacturing hurdle commonly encountered in fine-pitch detection applications.

The A1233 is a monolithic device containing two independent Hall-effect bipolar switches located 1.63mm apart. It provides excellent speed and direction information for small-geometry targets. Extremely low-drift amplifiers guarantee symmetry between the switches to maintain signal quadrature. A patented high-frequency chopper-stabilisation technique cancels offsets in each channel and provides stable operation over the full specified temperature and voltage ranges.

www.allegromicro.com

KONTRON MICROTCA CARRIER HUBS NOW SUPPORT MTCA.4 SPECIFICATION

Kontron has announced today that the Kontron MicroTCA Carrier Hubs (MCH) AM4904/AM4910 have been upgraded to include support of the MTCA.4 specification. Offering the MicroTCA enhancements for rear I/O and precision timing, the MCHs are ideally aligned with the requirements of high-speed data acquisition and processing applications. Target segments include physical research centres and many other high-bandwidth applications that require increased serviceability packed into a compact form-factor and feature high levels of performance, bandwidth and availability. By supporting four different high-speed fabric variants, including GbE, sRIO, PCIe and 10 GbE, the new Kontron MicroTCA Carrier Hubs build the backbone of practically all data-intensive MicroTCA-based high-performance applications.

Besides deployment in physics applications, other typical scenarios can be found in telecom markets, including 3G, LTE and network test equipment, and non-telecom markets such as military, medical, test and measurement, as well as in image and video processing applications.

www.kontron.com

ADVANCED BUS CONVERTER IDEAL FOR NETWORK-ATTACHED-STORAGE APPLICATIONS

Ericsson has launched the industry's first digitally controlled Advanced Bus Converter aimed at powering Redundant Array of Independent Disks (RAID) and Network Attached Storage (NAS) hard-disk applications that operate with high capacitive loads up to 15 milliFarads (mF). Based on the Ericsson 3E* FRIDA II platform, the BMR456 'High-Cap' series (BMR4560004/018) guarantees stable and accurate 12V bus voltage over the full input-voltage range.

RAID and NAS applications developed for data centres are designed for high performance and reliability and require very stable and smooth bus voltages without disturbances, such as voltage glitches or delays that result from power sources operating with current-mode limitations. Designers will commonly use large arrays of capacitors, often resulting in an average value of 12 to 15mF, to secure that the bus voltages delivered to hard disks and other sub-assemblies are exempt from noise.

The BMR456 uses digital control and embeds a voltage-mode-control algorithm that maintains a tight output voltage between 11.88V and 12.12V and accurately controls the 20ms ramp-up time.

www.ericsson.com/powermodules

NEW CONNECTOR MODULES OFFER MECHANICAL ROBUSTNESS AND SIGNAL

Two new modules have been added to Harting's Han-Modular industrial connector family to provide enhanced mechanical robustness and signal integrity in industrial and transport applications.

Two data cables can be connected per module and the product combines assembly convenience with product compactness. The screening design is independent of that of the housing, and the proven Han D crimp contacts are used. These can be installed into the inserts and arranged to be easily accessible.

Because its mechanical properties meet those of the established Han Quintax connector, the Han Megabit module is ideally suited for applications with the highest mechanical specifications, for example for use as an Ethernet interface in railway carriage connections – with the module taking up only half as much space as conventional solutions. The module is designed for data rates of up to 100Mbit/s, meets Cat.5e performance requirements and can be used with stranded wires with cross-sections between 0.14 and 2.5mm^2 and cable diameters between 5 and 12mm.

www.harting.com

TFC Monolithic Crystal Filters

TFC monolithic crystal filters feature excellent selectivity, small insertion loss and very high reliability. Standard and custom designs are available as discrete and packages units.

The range includes standard 10.70MHz, 21.40MHz, 45MHz fundamental and third overtone designs, and there are six- and eight-pole block filters with the option of matching transformers.

Quartz is the ideal resonator for selective narrow-band filters providing a temperature stable, high Q resonant source together with a low mass and small size.

The TFC data includes a general range of filters available for applications with channel spacing requirements of between ±12.5kHz and ±50kHz complemented by single sideband filters and custom designs available for special applications.

The correct termination of quartz filters is of prime importance to realise the high performance for each design. TFC crystal filters are 100%-tested and for custom-manufactured product a test fixture, representing the correct load, is available for verification by the customer.

www.tfc.co.uk

DESIGN RF AND MICROWAVE TEST LEAD ASSEMBLIES ON THE MOVE

Wavelength Electronics has announced the availability of a new mobile app that enables engineers to specify extremely rugged, high-performance MegaPhase RF and microwave test cable assemblies from their mobile phones, iPod Touch device or iPad tablet. An essential utility for test and measurement and systems engineers who need to specify RF coaxial cables and connectors in the course of their work, the app offers a host of useful features, including cable builder, cable browser, cable specification assistance, RL/VSWR converter, dB per pound converter, product descriptions, complete product datasheets and dBm to Watts converter.

The app not only provides quick product identification and selections, but also allows the user to design custom cables on their mobile device. Quick quote requests can be automatically generated and emailed for rapid response, and custom cables can be built and emailed instantly for a quotation.

The MegaPhase app can be downloaded (< 9MB) free of charge.

www.megaphase.com
www.wavelengthelectronics.co.uk

Farnell element14 Introduces New EZPE Electrolyic Series from Panasonic

The new EZPE Series from Panasonic is now available through Farnell element14. Key features include long product life with high reliability, low ESR, full compliancy with the RoHS directive and high safety with built-in self-healing and self-protecting functions.

The addition of the Panasonic EZPE series offers a number of benefits for applications such as DC link and filtering, IGBT protection, photovoltaic inverters, wind power generation and industrial power supplies.

The Panasonic EZPE series is produced with metallised Polypropylene film and patterned metallisation technology. The special fuse function of the patterned metallisation enables high capacitance, high withstand voltage and a built-in protection function.

Technical Details include rated voltage 500VDC/1300VDC, capacitance range of 10uF to 110uF, capacitance tolerance of ±10%, temperature range of -40°C to +85°C, typical ESR (20°C/10kHz) 4.1mΩ to 22.0mΩ and lifetime spec 100,000hrs at 70°C.

www.premierfarnell.com

LTE/3G MULTIMODE RF TRANSCEIVER ENABLES DEPLOYMENT OF HETNET BASESTATIONS

Maxim Integrated Products introduced the MAX25801, a single-chip multistandard RF to bits small cell radio transceiver. This highly integrated solution requires very few external components to execute an all-band, multimode, multiple-input multiple-output (MIMO) radio design. The MAX2580 design package also includes full system-level reference designs to shorten time to market. This RF transceiver is ideal for mobile operators planning residential, enterprise, or outdoor small cell deployments in their next-generation heterogeneous networks (HetNet).

Anticipating the needs of next-generation HetNet solutions, the MAX2580 provides wideband frequency coverage with programmable channel bandwidths to support all LTE/3G bands and modes. In a single device, the MAX2580 integrates a complete 2 x 2 MIMO RF front-end, including fractional-N frequency synthesizers, high-speed data converters and channel selection filters. Additionally, the MAX2580 features a standard JESD207 data interface to facilitate seamless connectivity with multicore LTE baseband processors.

www.maximintegrated.com

YOKOGAWA LAUNCHES 5TH GENERATION BEST-SELLING POWER METER

The new WT300 series of digital power meters are the fifth generation of Yokogawa's best-selling compact digital power meters: instruments that play a key part in ensuring optimum standards of energy efficiency and conservation by measuring the power consumption of electrical equipment.

Combining accurate and reliable power measurement over a wide power range with flexibility, ease of use and a choice of communication interfaces, the new instruments will help developers and manufacturers of electrical equipment – ranging from domestic "white goods" to lighting systems and air-conditioning equipment, to ensure that their products comply with emerging IEC and EN standards and increasingly complex and stringent specifications on energy efficiency.

Key features of the new instruments include a basic accuracy of 0.1% of reading, guaranteed accuracy over the entire measurement range (from 1% to 130%), a wide measurement range and flexibility to enable users to target different technical and commercial applications.

www.tmi.yokogawa.com

NEW KEMTRON CATALOGUE IS AVAILABLE NOW

UK manufacturer of RFI/EMI shielding solutions Kemtron has published a comprehensive new catalogue in response to customer demand. The 144-page printed catalogue has proved popular with customers who have limited Internet access, or who prefer the convenience of a paper version that they can bookmark, add notes to or use as a working reference tool.

"We have had a fantastic response from customers in countries like Germany, India and Turkey, as well as the UK. They welcome the fact that they can have a printed catalogue when so many suppliers only offer information on the Web," said David Wall, Kemtron's Managing Director.

The catalogue provides detailed product overviews, technical specifications, application information and design considerations for Kemtron's range of RFI/EMI shielding solutions, as well as background information on EMC and useful design tools.

www.kemtron.co.uk

High-End Touch Graphics Solution For Energy-Efficient MCU Applications

Energy Micro and Mjolner Informatics will jointly demonstrate a smartphone-like graphical user interface running on Energy Micro's EFM32 Giant Gecko microcontroller. This demonstration, developed using Mjolner's TouchGFX technology and featuring full touch control, can be seen on Energy Micro's booth at Embedded World. Mjolner will also present a paper in one of the conference sessions at the show to explain more about the features and benefits of TouchGFX for ARM Cortex-M3.

The control of products designed for markets such as home automation, medical, healthcare and industrial applications often depends on a relatively low-cost microcontroller (MCU) platform with limited hardware resources. Increasingly these designs are for handheld, wearable or similar battery-powered devices that also demand a power-saving, low-energy solution. This is all at odds with the type of graphical user interface (GUI) we've become familiar with from our smartphones, e-readers and tablets, which normally requires a powerful and expensive high-end MCU based around a processor core such as the ARM9.

www.energymicro.com

Low-Profile 0805 MLO Diplexer Series Supports Several Wireless Standards

AVX Corporation introduced a new series of low profile, best-in-class 0805 MLO diplexers. Based on its patented multilayer, organic, high-density interconnect technology, AVX's new MLO diplexers incorporate high dielectric constant and low-loss materials to realize high Q printed passive elements, such as inductors and capacitors in multilayer stack-ups.

Featuring low insertion losses, low parasitics, a low profile (< 0.6mm) and excellent solderability, the new 0805 Series diplexers support several wireless standards, including WCDMA, CDMA, WLAN and GSM, and are ideally suited for band switching in dual and multiband systems.

AVX's 0805 Series diplexers measure 2.12mm x 1.28mm x 0.55mm (0.083" x 0.050" x 0.021"), are rated for use in temperatures ranging from -40°C to +85°C, feature a maximum power capacity of 4.5W and are expansion-matched to most PCB materials.

Available in four frequencies and two terminations (Au and Ni/Sn), AVX's 0805 Series diplexers feature standard tape and reel packaging.

www.avx.com

BRIGHT, ROBUST AND LONG LIFE MULTI-ANGLE LED LIGHT TUBES

Optoelectronics firm OMC announced a new version of its rugged, robust and high-brightness multi-angle LED light tube range which can be used to replace traditional light sources in many applications, saving power and lasting much longer than fluorescent products.

These compact, low voltage, linear LED lighting fixtures feature advanced lens/reflector assemblies that provide extremely bright and uniform illumination across a broad and well-defined target illumination area, with a power consumption of just 2.9W per foot of tube. With a slim profile and robust metal housing, the new light tubes are easy to install and require no additional fixtures or fittings – they screw mount to the installation surface using the range of secure, multi-angle brackets provided. The adjustable mounting brackets allow the light to be directed to where it is needed, and low voltage 24V DC operation means that they are safe and simple to power electrically.

www.omc-uk.com

The First PC Oscilloscopes With A USB 3.0 Interface Is Out Now

Pico Technology launches oscilloscopes with USB interface in response to these ports appearing on most new equipment, including computers and laptops. With the new USB 3.0 PicoScopes, large data captures and streaming of large data sets are now much faster.

PicoScope 3207A is a 2-channel USB oscilloscope with 250MHz bandwidth, 1GS/s sampling rate, 256MS buffer memory and a built-in function generator with a basic timebase accuracy of ±2ppm. Other features include digital triggering for accurate, stable waveform display, and equivalent-time sampling, which boosts the effective sampling rate to 10GS/s for repetitive signals.

The PicoScope 3207B has 512MS buffer memory and an additional 32k-sample arbitrary waveform generator with 100MS/s update rate. As the scope obtains its power from the USB port, there is no need for an external power adaptor.

The oscilloscopes are supplied with the PicoScope software for Windows, which turns your computer into a powerful oscilloscope and spectrum analyzer.

www.picotech.com

NEW POWER MOSFETS COMBINE FAST SWITCHING, LOW ON-RESISTANCE AND COST-EFFECTIVENESS

Advanced Power Electronics Corp (USA), the Taiwanese manufacturer of MOS power semiconductors for DC-DC power conversion applications, has announced its highly cost-effective AP9412A family of N-channel enhancement-mode power MOSFETs which feature fast switching and low on-resistance.

Available in SO-8, TO-252 and isolated TO-220CFM packages, the devices have a minimum drain-source breakdown voltage of 30V and a maximum Rds(on) of just 6mΩ. Other characteristics depend on the package chosen. All parts are extremely easy to drive. They are suitable for a wide range of industrial and commercial applications including low voltage applications such as DC/DC converters.

"We specialise in providing parts that simplify the design engineering process by delivering excellent performance at an attractive price level. These new devices are a perfect example," said Ralph Waggitt, President/CEO, Advanced Power Electronics Corp (USA).

www.a-powerusa.com

DIGITAL VIEW LCD CONTROLLER SUPPORTS HDMI AND DISPLAYPORT

Display specialist Ginsbury introduced the Digital View ALR-1920, a new all-in-one LCD interface controller providing support for HDMI, DisplayPort and VGA inputs for TFT LCD panels up to WUXGA (1920 x 1200) resolution. The ALR-1920 provides an extremely flexible controller solution with pre-installed support for over 700 LCD panels from leading display manufacturers such as Samsung, Sharp, LG, NEC, Optrex, Chi Mei and AUO.

Designed for display integrators and monitor developers, the ALR-1920 offers HDMI 1.3, single-link DisplayPort 1.1a and VGA input for resolutions ranging from VGA (640 x 480) to WUXGA (1920 x 1200) or 480i to 1080p video. The ALR-1920 also offers image up-scaling and down-scaling, stereo audio support over HDMI and DisplayPort signals with embedded audio.

The small form-factor ALR-1920 board design features compact dimensions of 107mm (w) x 92mm (h) x 16.65mm (d), offers an onboard power supply with both 12- and 24-volt DC input.

www.ginsbury.co.uk

CAMBRIDGE PHOTONIC SYSTEMS CENTRE INVITES UK TECH INDUSTRY TO INVEST IN STUDENTS

The EPSRC funded Centre for Doctoral Training (CDT) in Photonic Systems Development, set up jointly between UCL and the University of Cambridge, held an Industry Day on 14th January 2013 at Cambridge's William Gates Building. UK Tech companies were encouraged to invest in the Centre's largest ever cohort of students by collaborating in Masters or PhD level research projects relevant to the tech industry's needs.

Companies are invited to consider the opportunity for the Centre's staff and students to help them advance their research and technology strategies and accelerate the commercialisation of research, particularly in photonics, so that the potential growth areas in this field become a focus for the Centre.

The photonics industry is growing rapidly and experts predict that photonic systems will become one of the most significant enabling technologies of the next few decades. Centre Director Professor Alwyn Seeds said: "Graduates from the Centre's four year PhD programme will be the next generation of photonics pioneers with the skills and confidence to drive future technology research, development and exploitation through new products, processes and services. Their skill set is already greatly in demand from companies and research organisations, as photonics becomes fully embedded in electronics-based systems applications ranging from communications to sensing, industrial manufacture and biomedicine."

IVOR CATT, Engineer and Scientist, UK: I part company at the start of "photonics" if Wikipedia is correct in stating: "The term photonics thereby emphasizes that photons are neither particles nor waves – they are different in that they have both particle and wave nature."

All my work relates to waves, and there are no particles. That is because I cannot use something that has not been properly – scientifically – defined.

I do not have access to what are for me the key points about a "particle". For a century we have had no instantaneous action at a distance. Does a particle have volume, or is it solely at a point, with infinite density? If it has volume, and diameter, does the left-hand edge know that the right-hand edge had experienced something? How does the signal travel across the particle? Are there two types of space: that outside particles and that inside a particle?

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: Industry days are extremely important for bridging the gap between industry and doctoral research projects at universities. Companies should be encouraged to attend such events and invest in research projects appropriate to their fields. I hope to see many more such events in the coming months.

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: Do first impressions matter? Student 'open days' enable exposure to the academic staff and the facilities on offer to attract a three-year investment of their time. The stated ethos behind this business open day is to enable "collaborative research". If so, then this initiative is to be welcomed as more than just a "tell us your real-world problems" outreach and marketing exercise.

Currently, with the UK science budget cuts and the threat of the Internet (MOOCs, etc.) to traditional academic business models, universities are receptive to change. The issue here, as always, is that academics see the knowledge transfer process as one-way: from them (academia) to us (industry). This is a cultural issue academics will have to overcome especially if the so-called "Valley of Death" for spin-offs is to be achieved.

MAURIZIO DI PAOLO EMILIO, Engineer, University of L'Aquila and EDM Engineering, Italy: In recent years there have been important advances in research labs around the world to develop increasingly sophisticated ways of using photonic devices in telecommunications and computing systems among others. By using photonics these systems can work with much greater speed and information capacity and be smaller and easier to make. These advantages make photonics an important field both for research and commercial development.

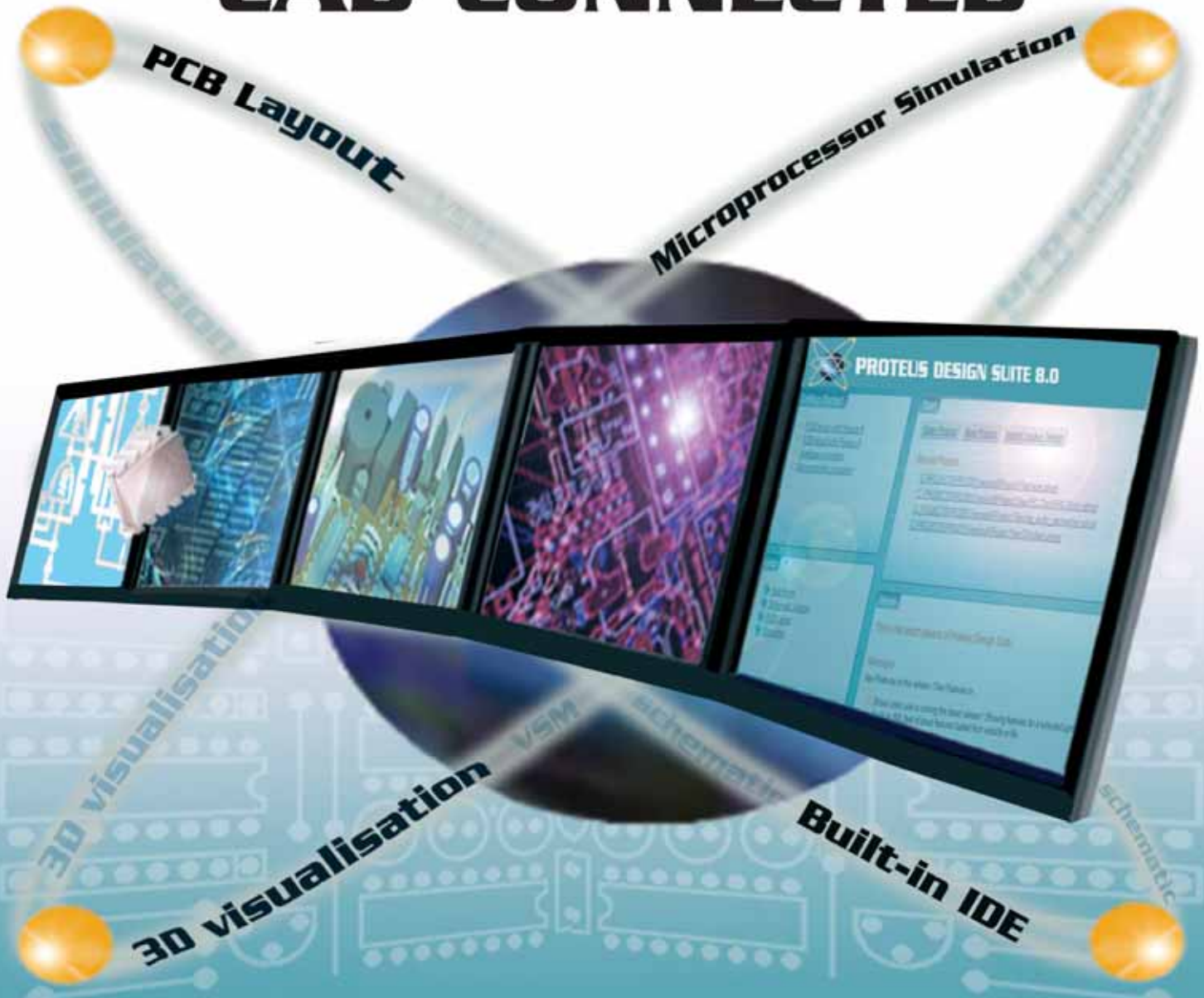
Photonic systems, in particular photonic integrated circuits, can allow optical systems to be made more compact and higher performance than with discrete optical components. They also offer the possibility of integration with electronic circuits to provide increased functionality.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: The photonic sector goes over a period of determining change for the industry. This requires qualified workers at a high educational level. To develop this sector universities must intervene in an effective way to implement a standardised optimization process and increased automation in the industry. Indeed, the development of this sector, which is crucial for the industrial future, implies high scientific research and rather important industry participation in order to promote it. That is why ULC Cambridge Photonic Systems took the initiative to organize an industry day at the University of Cambridge. This effort will help develop the optics and photonic technology of tomorrow.

"Academics see the knowledge transfer process as one-way: from them to us. This is a cultural issue academics will have to overcome especially if the so-called "Valley of Death" for spin-offs is to be achieved

If you are interested in becoming a member of our panel and comment on new developments and technologies within the electronics sector please register your interest with the Editor by writing to svetlana.josifovska@stjohnpatrick.com

CAD CONNECTED



PROTEUS DESIGN SUITE VERSION 8

Featuring a brand new application framework, common parts database, live netlist and 3D visualisation, a built in debugging environment and a WYSIWYG Bill of Materials module, Proteus 8 is our most integrated and easy to use design system ever. Other features include:

- Hardware Accelerated Performance.
- Unique Thru-View™ Board Transparency.
- Over 35k Schematic & PCB library parts.
- Integrated Shape Based Auto-router.
- Flexible Design Rule Management.
- Polygonal and Split Power Plane Support.
- Board Autoplacement & Gateswap Optimiser.
- Direct CADCAM, ODB++, IDF & PDF Output.
- Integrated 3D Viewer with 3DS and DXF export.
- Mixed Mode SPICE Simulation Engine.
- Co-Simulation of PIC, AVR, 8051 and ARM MCUs.
- Direct Technical Support at no additional cost.

labcenter Electronics

www.labcenter.com

Visit our website or phone 01756 753440 for more details

Labcenter Electronics Ltd. 21 Hardy Grange, Grassington, North Yorks. BD23 5AJ.
Registered in England 4692454 Tel: +44 (0)1756 753440, Email: info@labcenter.com

PME1200 Series, Programmable 1200Watt AC-DC Power Supply

Medical Safety Approvals

FEATURES

- Universal AC input with active Power Factor Correction
- DC output Voltage & Current programmable 0-105% of nominal
- 7 models with nominal outputs of 12V, 15V, 24V, 30V, 36V, 48V & 60VDC
- +5V 0.5A or +8V 0.3A Standby Voltage
- Very high efficiency up to 93%
- Intelligent LED indicators for power supply status
- Forced current sharing for parallel operation
- Power OK signal (Power OK Logic 0)
- Remote On/Off & Remote Sense function
- Over load, over voltage & over temperature protection
- Built in I²C serial data bus for programming & monitoring
- Full UL, CSA & TUV medical safety approvals
- Compact dimensions of 267 x 127 x 63.5mm
- Very competitive pricing for OEM quantities

POWER SOLVE

TEL: 44-(0)1635-521858 Email: sales@powersolve.co.uk

www.powersolve.co.uk