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Livingston Explores the Test Implications of Next Generation Data Communication

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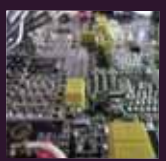
Four key elements of sustainability



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REGULARS

32
Sustainability

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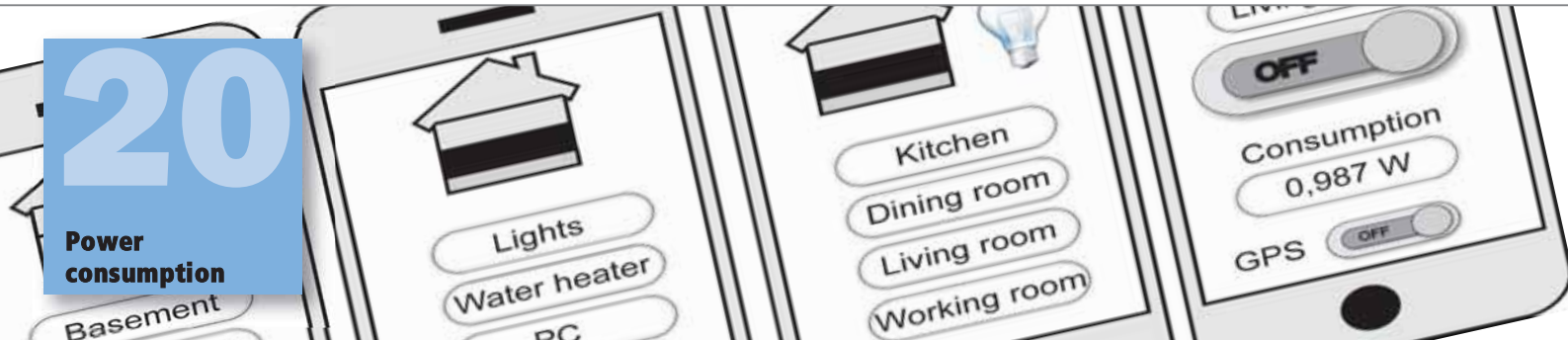
More on pages 8-9

FEATURES



20
Power consumption

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IGBT APPLICATION GROWTH WILL LEAD THE MARKET TO OVER $6BN BY 2018

> *IGBTs are increasingly part of everyday life, in consumer and home appliances especially, which increasingly require inverter-based motor drives for better performance, comfort and efficiency*

After a few hiccups over the past two years, French firm Yole Développement expects a return to steady growth for the IGBT (Insulated Gate Bipolar Transistor) market – specifically from $3.6bn today to $6bn by 2018.

The company states that key applications to fuel this growth include photo-voltaics (PV), wind, rail, UPS, EV/HEV and motor drives.

Motor drives present the largest market for IGBTs; followed by renewable energies – PV and wind. Since the latter rely on government investments, and funding can be unpredictable, Japan and several developing countries will make up for Europe's slowdown, says the firm.

Mass transportation and UPS are based on infrastructure needs, thus the demand for greater efficiency is pushing these markets. As for hybrid and electric cars, questions remain – there will be market growth fuelled by them, but nobody can predict to what extent.

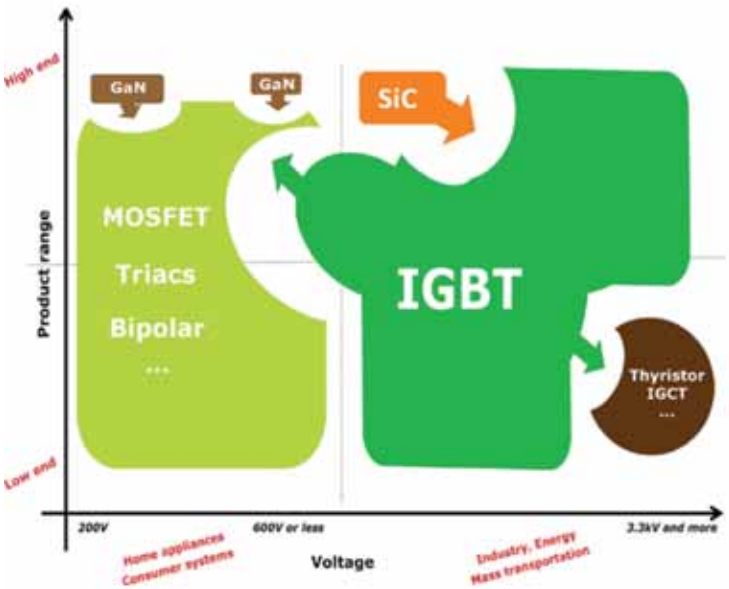
IGBTs are increasingly part of everyday life, in consumer and home appliances especially, which increasingly require inverter-based motor drives for better performance, comfort and efficiency. Consumers are also using more advanced home solutions, like induction-based plates for rice cookers, for example.

In 2012 there was a crisis in the power devices markets, and IGBTs in particular. This is explained by several factors:

- The slowdown of PV installations due to reduction of feed-in tariffs in Europe;
- The slowdown of wind turbine installations in China;
- The rail accident in China that halted the high-speed train production;
- The slow global economic recovery affecting the consumer markets.

Power device technology positioning

(Source: IGBT Markets and Application Trends, Yole Développement, May 2013)



Yole Développement (www.yole.fr) was founded in 1998, and has since grown to become a group of companies providing marketing, technology and strategic consulting, in addition to corporate finance services and media.

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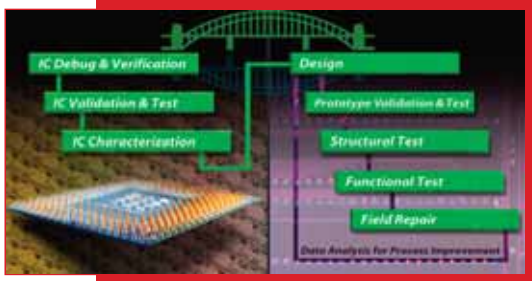


An all-engulfing platform should help with complex embedded designs

Embedded instrumentation supplier Asset InterTech last month acquired software debug tools company Arium in a bid to create a one-stop shop for embedded design engineers, specifically for debug, validation and test, from hardware through to software, and the interaction between them.

Arium's software debug and trace tools complement Asset's own set of tools, part of the ScanWorks platform, which access, manage and control T&M instruments embedded in chips. Arium's hardware-assisted debug tools troubleshoot the code quickly, whilst its trace tools help analyse software transactions and interactions within the design.

"We are unique in this space. Other T&M companies – the rack and stack type of equipment guys – such as Agilent, LeCroy and others – are trying to address this space but none of them can do it as well as we can now," said Reg Waller, Asset InterTech's European Director.

"Everybody is embedding ARM or Intel [processors and chipsets] in their products; even FPGA vendors are embedding those cores into their FPGAs, and [now] we have the tools for both."

There's a growing use of multiple processor cores in designs, as well as use of a greater number of resources, which increases the volume of software required to interface the hardware with the operating system and design applications. Add to this the high-speed buses and new chip packaging technologies and it becomes practically impossible to see what's going on in a system.

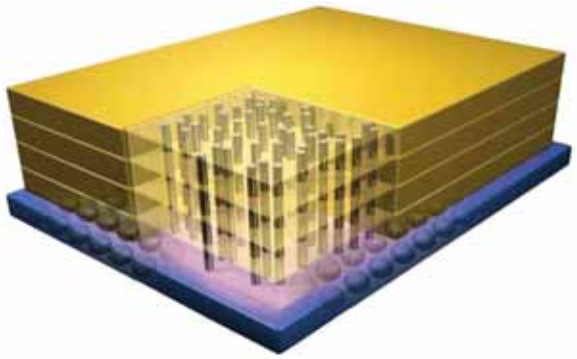
"The designs have become more complex, but now there are better and faster tools and, with them, visibility [into system development] is getting better. These tools also help save on validation, test and debug time. For example, validation used to take months; now it takes days to weeks at the most," said Waller. "But, [with such complexities] the role of the engineer has changed too, especially here in Europe, where an engineer is expected to wear more than one hat."

Waller added that in today's complex environment of embedded design, the key to going forward, keeping costs down and accelerating time-to-market is through an integrated ecosystem, which many are already beginning to offer or be a part of, including Intel. Intel has started embedding its own proprietary set of tools within its chips to enable platform debug, electrical validation and board manufacturing test, called Silicon View Technology (SVT). Asset InterTech tools already interact with Intel's SVT.

The privately-owned Asset InterTech was once part of Texas Instruments (TI). It spun-off in 1995, when it was initially focusing on boundary scan solutions. In late 2007 it acquired Irish firm International Test Technologies (ITT) and with it attained ITT's processor-based hardware debug expertise. It was at that time the company quickly understood that embedded instrumentation is the technology of the future. With its acquisition of Arium, it has closed the gap. The next step for these two companies is to offer an integrated platform for their core tools.

"We could provide the IP for third party vendors, say the FPGA firms, to embed in their FPGAs and configure that IP themselves," added Waller.

Hybrid Memory Cube Consortium Heralds 2013 as Turning Point for High-Performance Memory ICs



Hybrid Memory Cube is a new innovation in DRAM technology

Over 100 developer and adopter members of the Hybrid Memory Cube Consortium (HMCC) announced they've reached consensus for the global standard that will deliver a much-anticipated, disruptive memory computing solution. Developed in only 17 months, the final specification marks the starting point for designers in a wide range of segments, from networking and high-performance computing, to industrial and beyond, to begin designing Hybrid Memory Cube (HMC) technology into future products.

A major breakthrough with HMC is the long-awaited utilization of advanced technologies to combine high-performance logic with state-of-the-art DRAM. With this first HMC milestone reached so quickly, consortium members have elected to extend their collaborative effort to achieve agreement on the next generation of HMC interface standards.

"The consensus we have among major memory companies and many others in the industry will contribute significantly to the launch of this promising technology," said Jim Elliott, Vice President, Memory Planning and Product Marketing at Samsung Semiconductor. "As a result of the work of the HMCC, IT system designers and manufacturers will be able to get new green memory solutions that outperform other memory options offered today."

"This milestone marks the tearing down of the memory wall," added Robert Feurle, Micron's Vice President for DRAM Marketing. "The industry agreement is going to help drive the fastest possible adoption of HMC technology, resulting in what we believe will be radical improvements to computing systems and, ultimately, consumer applications."

As envisioned, HMC capabilities will leap beyond current and near-term memory architectures in the areas of performance, packaging and power efficiency.

"HMC is a very special offering currently on the radar. It brings a new level of capability to memory that provides exponential performance and efficiency gains that will redefine the future of memory," said JH Oh, Vice President for DRAM Product Planning at SK hynix.

One of the primary challenges facing the industry – and a key motivation for forming the HMC – is that the memory bandwidth required by high-performance computers and next-generation networking equipment has increased beyond what conventional memory architectures can efficiently provide. The term "memory wall" has been used to describe this challenge. Breaking through the memory wall requires architecture such as HMC that can provide increased density and bandwidth with significantly lower power consumption.

The HMC standard focuses on alleviating an extremely challenging bandwidth bottleneck while optimizing the performance between processor and memory to drive high-bandwidth memory products scaled for a wide range of applications. The need for more efficient, high-bandwidth memory solutions has become particularly important for servers, high-performance computing, networking, cloud computing and consumer electronics.

The achieved specification provides advanced, short-reach (SR) and ultra short-reach (USR) interconnection across physical layers (PHYs) for applications requiring tightly coupled or close-proximity memory support for FPGAs, ASICs and ASSPs, such as high-performance networking and test and measurement.

The next goal for the consortium is to further advance standards designed to increase data rate speeds from 10, 12.5 and 15Gb/s to 28Gb/s for SR and from 10Gb/s up to 15Gb/s for USR. The next-generation specification is expected to gain consortium agreement by the first quarter of 2014.

The HMC Technology

Hybrid Memory Cube is a new innovation in DRAM memory architecture that sets a new standard for memory performance, power consumption and cost. A single HMC can provide more than 15x the performance of a DDR3 module and yet consumes 70% less energy per bit compared to DDR3 DRAM. Its increased density per bit and reduced form-factor contribute to lower total cost of ownership, by allowing more memory into each machine and using nearly 90% less space than today's RDIMMs.

With performance levels that break through the memory wall, Hybrid Memory Cube represents the key to extending network system performance to push through the challenges of new 100G and 400G infrastructure growth. The technology is heralded to redefine memory and set a new standard of memory that can keep up with the advancements of CPUs and GPUs. Some industry players call it "an absolute game changer" for many applications, including high-performance computing and consumer devices where small size, lower power consumption and high bandwidth are of highest importance.

The HMC Consortium

The HMCC is a collaboration of OEMs, enablers and integrators cooperating to develop and implement an open interface standard for HMC. More than 100 technology companies from Asia, Japan, Europe and the US have joined forces, including Altera, ARM, Cray, Fujitsu, GLOBALFOUNDRIES, HP, IBM, Marvell, Micron Technology, National Instruments, Open-Silicon, Samsung, SK hynix, ST Microelectronics, Teradyne and Xilinx. Continued collaborations within the consortium could ultimately facilitate new uses in HPC, networking, energy, wireless communications, transportation, security and other semiconductor applications.

Additional information, technical support specifications and other tools for adopting the technology can be found at www.hybridmemorycube.org

IMPLEMENTATION OF 100G ETHERNET & THE ASSOCIATED TEST IMPLICATIONS

By Geoff Kempster, Livingston & Dr Jon Bradley, EXFO

In order to cope with our increasing preoccupation with the vast array of bandwidth-heavy multimedia services now being made available, it is predicted that 100G Ethernet communication (as defined by the IEEE 802.3ba standard) will witness widespread deployment throughout the European Union over the coming year. With multi-wavelength parallel optical transmission lines being utilised to carry data, as opposed to the traditional serial transmission approach, 100G Ethernet boasts a much larger data capacity than could have previously been achieved. Thanks to its IP-based architecture, it will be possible for higher levels of operational efficiency to be maintained, as well as provision being made for a wider range of functionality and network flexibility enhancements. This technology is far from being without its challenges though.

Firstly, migration to an IP-based technology requires a completely different test strategy to be employed. The architecture's parallel nature could have a heavy bearing on transmission in terms of signal skew, so greater test scrutiny will be called for here. Furthermore, line interface testing, line-coding modulation analysis, fibre characterisation and transmitter analysis must all be carried out. This is further compounded by the fact that it will still be necessary to support existing communication protocols (such as SONET/SDH, Ethernet and OTN) on the network too. Overall network complexity will thus rise and the variety of different tests needed is therefore destined to expand considerably.

The challenges are certain to become greater with 100G Ethernet testing now moving out of the laboratory and into the field, as large scale installation work begins in earnest. It means a number of additional factors must be taken into account. Field operatives will need access to compact, lightweight and easy to use test equipment that offers a high degree of accuracy. Intuitive operation of equipment will prove crucial, so that tests can be carried out quickly and without the risk of errors being made (avoiding the need to make additional call outs for tests to be repeated).

So that it is not necessary to source a number of different items of test hardware, certain manufacturers have had the foresight to develop products which have the capacity to analyse both 40G/100G and 10G Ethernet networks. EXFO introduced, for this purpose, the FTB-88100NGE Power Blazer, a highly portable, software upgradable field tester that supports 10M to 100G technology and delivers 100% line-rate testing of IP traffic on 100G Ethernet infrastructure. It is possible to preconfigure OTN, Ethernet and SONET/SDH bit error rate test parameters onto the unit before going to the test site - allowing for simple BER testing, without risk of misconfigurations between two remote sites. The FTB-88100NGE has an automated RFC 2544 test suite for 10/100/1000M and 10G/40G/100G Ethernet interfaces with all frame sizes and at full line rate, so that repeatable results are acquired. It has per-lane skew generation and measurement as well as multi-stream traffic generation, traffic filtering, packet capture, ping and traceroute functions.

The emergence of advanced test solutions that can support both legacy and next generation technologies will make the roll-out of next generation communication networks a less daunting prospect. Unfortunately the challenges are not just of a technical nature. As well as specifying the correct equipment, there are questions about how it should be sourced that need to be answered. Often direct purchase may not be appropriate, whereas rental over a certain time period may prove to be better option.

Thanks to its strong relationships with leading manufacturers, such as EXFO, Livingston can supply test engineers with the equipment they need for implementing and maintaining modern, sophisticated communication networks based on 100G Ethernet technology, without having to deal with the logistical or financial problems that sourcing such high value kit normally brings with it. Since it can be dealt with as an operational rather than a capital expense, it does not require heavy upfront investment. Also it alleviates the danger of being left with redundant equipment that no longer generates revenue.

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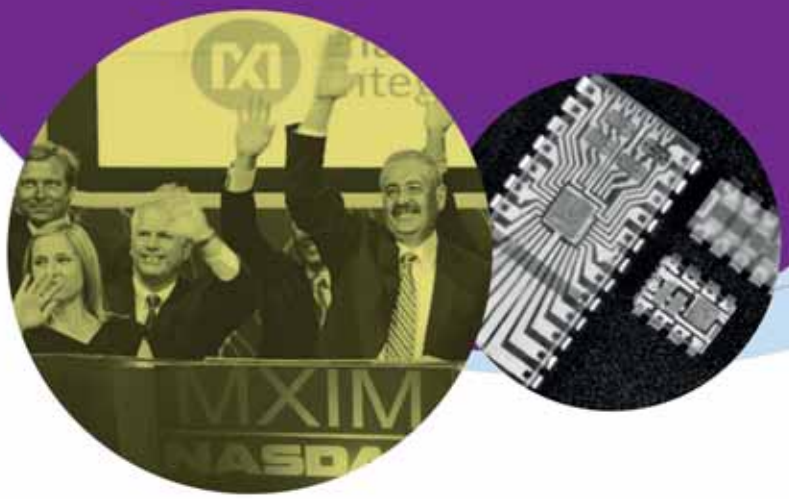

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Engineering resources are – at least in the low power wireless companies where I have worked over the years – always limited. New projects are always competing for bench time with a host of support and administration tasks, and there never seem to be enough engineers to complete the existing work, let alone take on – valuable! – new customer orders. This can make scheduling projects and managing a company's technical resources a difficult and often frustrating exercise. If such a task falls to you, either as an actual "technical manager" or as sales or marketing calling up new project design resources, it is simple human nature for you to want to give as much help as you can. You see engineers struggling with increasing workloads and shortening deadlines, and you want to reduce some of that stress (to get "your" pet project completed sooner and out of genuine human empathy). You look at ways that you can "lend a hand" – but beware! In this direction there lies a terrible pitfall.

Let us take a hypothetical example. A small wireless company manufactures a range of ISM band transmitters, receivers and transceivers. A customer enquiry leads to a request for a new transceiver, but unfortunately the customer's physical product constraints call for a device footprint that fails to match any of the existing transceiver products: they want a unit which is much narrower (although it can be much longer) than any existing products. The technical manager looks at his busy engineers and realizes that a completely new transceiver design job will stretch his department's resources to the limit. At this point he has his "brilliant idea". Rather than involve the engineers (and risk "wasting their time"), he looks at the physical footprint and spots that, although all his transceivers are too big, "a transceiver is just a transmitter and a receiver combined" and he can fit one of his (smaller) receive-only units end-to-end with an existing transmitter and stay inside the size constraints. Further meetings follow, the remaining specifications get defined (based on the datasheets of the two separate modules) and the customer is delighted with this "quick and easy" solution. Then, finally, the 'design' is presented to an engineer, who is told that "all he has to do" is lay out a carrier PCB for the two radio modules and link them to an antenna port with a suitable RF switch – a quick and easy 'do it over a coffee break' job!

> *The result is depressingly uniform: either the entire decision-making process must be unpicked and re-made, or the design goes ahead within highly sub-optimal constraints*

Unfortunately, it doesn't take the unlucky engineer more than a few minutes to notice that this "brilliant design" can never be made to work. It looks fine (if a bit clumsy) on the surface, but he knows things about the products that his technical manager is oblivious to, and while in principle a transceiver is just "a transmitter and a receiver in the same box", those component parts need to be designed to work in harmony with each other. In this particular case, the transmitter outputs an on-channel spurious signal when in the "standby" state which, while significantly below the regulatory limit, is still 50dB above the receiver's input sensitivity threshold, which in turn

requires the antenna switch to have an impossible-to-achieve (within size and cost limits) isolation performance.

The upshot of this sad story is that, after wasting yet more time convincing the manager that his "design" wasn't workable, the engineer still ends up tasked with the (now completely new) design job, but saddled with a shorter time-scale than if the job had been handled properly in the first place.

I wish I could cite this case as an isolated example, but unfortunately this problem (which I have also seen sarcastically referred to as "design by managers") crops up again and again, and it is usually done with the best of intentions. While details differ, the common aspect is that the engineer gets presented with half the job, after vital initial discussions have already happened and after crucial design choices have already been made, by people who are fundamentally ignorant of the actual engineering details of the subject. Typical "design choices" I have seen include:

- Inappropriate choice of frequency band (either wrong for the application environment, or unavailable in the country of use).
- Insistence on the use of radio hardware totally unsuited to the application (insufficient range, inadequate specifications or simply unavailable).
- Wildly optimistic physical size targets (sometimes as extreme as promising the customer a unit that is actually smaller than one of the critical components in the design, like the aerial or the battery).
- Promises to use completely new, untried and undeveloped technologies, without allowing time for basic feasibility work.
- Pointless fine detail stipulations ("The RF path will use this signal processing chip", "the code will be written for that compiler", or "this modem will use GMSK modulation") by staff uninvolved in the final work and/or ignorant of real engineering practice.

The result is depressingly uniform: either the entire decision-making process must be unpicked and re-made, or the design goes ahead within highly sub-optimal constraints. Either way, valuable time is lost or squandered. In any case, this is the polar opposite of the intended result: the engineer's job is actually made more difficult and far more frustrating.

Obviously, it's easy enough to point at past mistakes, but (other than calling for un-realistic staffing levels in the engineering departments) there are a few things which materially can make the engineer's job a lot easier:

- Involve engineering in the project discussions as early as possible, both as a sanity check, a source of ideas and to make scheduling the new tasks in with the existing workload easier.
- Allow enough time, not only for the actual job, but also for any supporting investigations and experiments. A rushed design is never a good design!
- Listen to the customer requirements, but don't then over-reach: going slightly beyond will impress a customer with your technical prowess, but too far and the job can become close to impossible.

Beyond any of these points, however, is one fundamental rule: your company is hiring those expensive engineers for their design skills. Make use of those skills and get the maximum value out of them. Involve them in all levels of the design and specification process and listen to them. It's what they are there for.

DYNAMIC VOLTAGE AND FREQUENCY SCALING BASED ON AN ON-CHIP MICROCONTROLLER SYSTEM

TIEFENG LI, **CAIWEN MA** AND **WENHUA LI** FROM THE XI'AN INSTITUTE OF OPTICS AND PRECISION MECHANICS AT THE CHINESE ACADEMY OF SCIENCES

ANALYSE THE POWER CONSUMED BY ON-CHIP MICROCONTROLLER SYSTEMS AND SUGGEST A NEW ARCHITECTURE ABLE TO REDUCE IT

Power consumption is one of the most prominent topics of interest to designers and it is still needs to be improved upon.

Portable electronic devices (typically powered by batteries) rely on energy-efficient schedules to increase their battery's lifetime; whereas non-portable systems need energy-efficient schedules to reduce their operating cost. Early in the design stage, when generally there's a lack of focus on saving power, designers tend to ignore this issue. However, in the development of microcontrollers and integrated circuit technologies, the system is more complicated and consumes more energy, so it is often desirable to maximize efficiency and yet minimize power consumption in order to achieve the best On-chip Microcontroller System (OCMS).

With the rapid increase of complexity and size of OCMSs, their power consumption needs immediate attention. The CPU is often the major power consumer in such a system, so one strategy to achieve energy saving is via Dynamic Voltage and Frequency Scaling (DVFS), which enables the processor to operate at a range of voltages and frequencies. However, conventional DVFS systems are fully executed by software schedulers in the operating system, and their main drawback is that the scheduler can't accurately track the CPU's performance requirements of the CPU when its frequency continues to increase when idle.

In this article, we discuss a typical hardware DVFS architecture, which can automatically carry out the scaling without involving the software scheduler.

Figure 1: Conventional DVFS based on software only

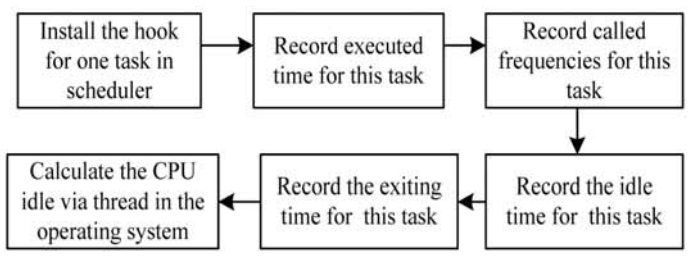
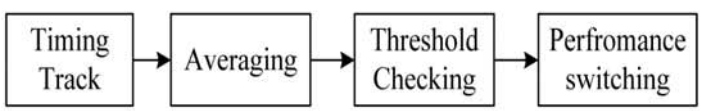


Figure 2: The proposed hardware-based DVFS architecture



Conventional DVFS

In the traditional design of an OCMS, the software scheduler reduces power consumption by estimating the CPU's workload according to the scheduler's frequencies. However, with as CPU technology develops, its main frequency exceeds 1.5GHz. For example, the frequency of an ARM Cortex A9 when dormant is about 1.6GHz.

Obviously, the software approach struggles in such dynamic environments because it can't accurately trace the status of the CPU's workload, because of the OCMS's hardware architecture to lower the power it has to be done with software in the operating system.

By contrast, the DVFS we present here is developed from the hardware side up and offers a remarkable improvement in power savings, because the DVFS is integrated into the OCMS with three different voltages and frequencies, the various performance requirements of the CPU can be addressed by DVFS architecture instantanously, thus the speed and accuracy of tracking the CPU's workload are greatly improved. Even more significantly, all tasks of tracking the CPU workload and predicting its performance can be completed by the hardware automatically, which reduces the burden on the operating system in the OCMS. In this design, the hardware DVFS mainly includes the CPU timing check, averaging algorithm and threshold check.

For the OCMS, its dynamic power formula is as follows:

$$P = \alpha CV2 f \quad (1)$$

where α represents the percentage of the switching logic cells between 0 and 1, C is a constant that represents the circuit load, V is the CPU voltage, and f is the CPU frequency. It's obvious from this equation that CPU power can be lowered by reducing the voltage and frequency.

Traditionally, designers adopt a software method to predict the performance requirement of the CPU according to the sequence of events in the software scheduler. Figure 1 shows one just software DVFS method, which prioritises the tasks in the operating system. Although power can be reduced in this way, it is only efficient when the CPU frequency is not high. Also, it will be difficult to increment the CPU frequency as the software method can't correctly respond to the high frequency of the CPU, as it fails to estimate the performance requirement of CPU in real time. Moreover, what's even more disconcerting is that the conventional software DVFS need to be called frequently in the operating system. To some degree, it is tedious to change the dynamic voltage and frequency by the means of a software scheduler, so to summarise, the current approaches to DVFS can hardly keep up with the dormant frequency increase of the new CPUs, therefore new DVFS methods and technologies have to be considered.

The Proposed Hardware DVFS

To overcome these issues, a hardware DVFS offers a very fast tracking and response speed based on the CPU's behaviour. Figure 2 shows a block diagram of the proposed implementation of this hardware support function, comprising four major function blocks named time tracking, averaging, threshold checking and performance switching.

> Once the hardware DVFS function is enabled, the voltage and frequency of the CPU needn't to be adjusted by the software scheduler over and over again

Due to those new features, the hardware DVFS can not only cut down the software overload coming from the operating system but it can also intelligently respond to the external dynamic environment. Once the hardware DVFS function is enabled, the voltage and frequency of the CPU needn't be adjusted by the software scheduler over and over again. In comparison to the previous software DVFS, it offers much better voltage and frequency accuracy and it lightens the load of CPU timing tracking too.

Timing Check

As shown in Figure 3, the clock divider provides the tracking clock of 3.25MHz that is internally used for time tracking. The tracking clock determines the possible time resolution for specifying the monitoring period duration, as well as for sampling the CPU's idle or active state.

Figure 3: Timing tracking

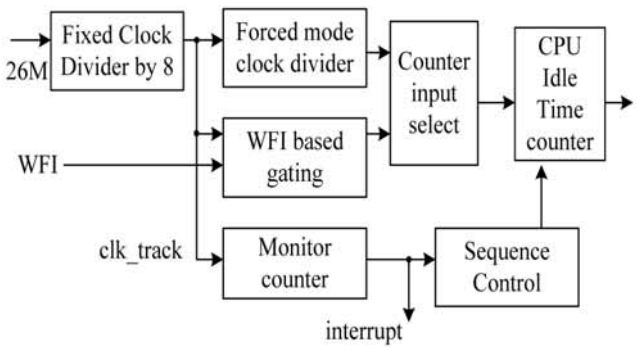
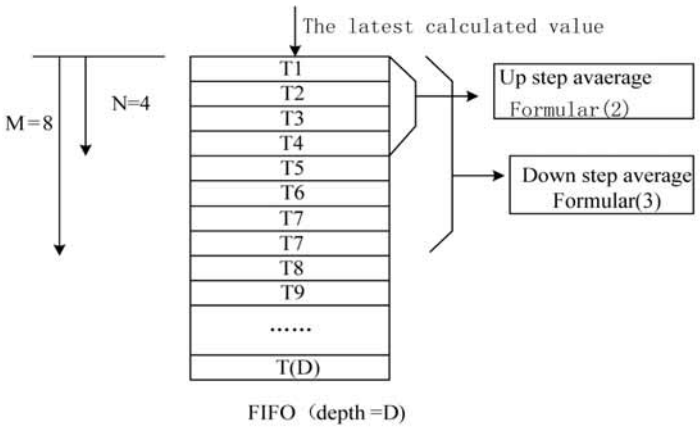


Figure 4: Averaging block



The monitoring counter operates in down-counting mode and decreases its counter value at each rising edge of the tracking clock. It also provides a reload value, which defines the monitoring period used in tracking clock cycles. The reload value is configurable by software through the register interface. When the monitoring counter underflows, counting is restarted applying the reload value.

Whereas in the recommended architecture, the CPU idle time counter operates in up-counting mode and increases its counter value at each rising edge of its counter input signal. The CPU idle time counter is reset by the sequence control

Figure 5: DVFS block diagram

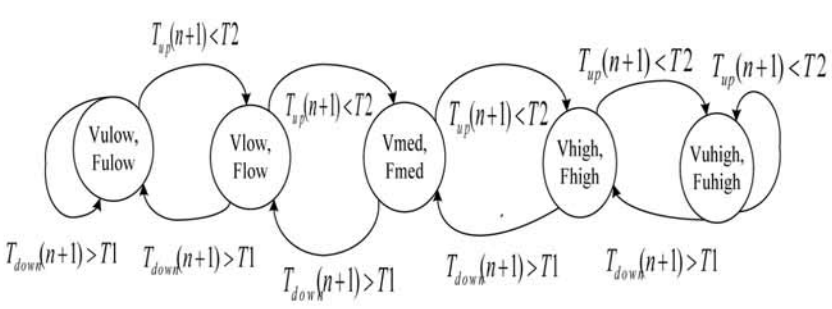


Figure 6: The PLL clock generator

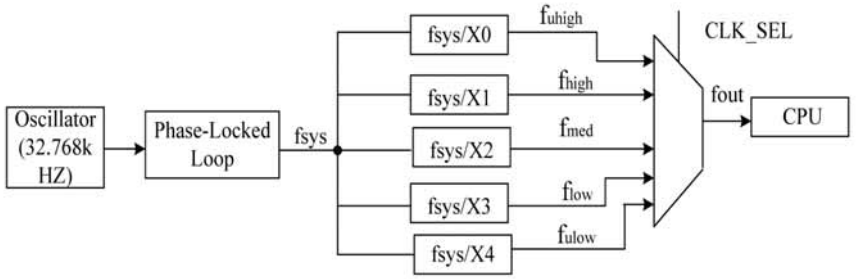


Figure 7: Response number comparison

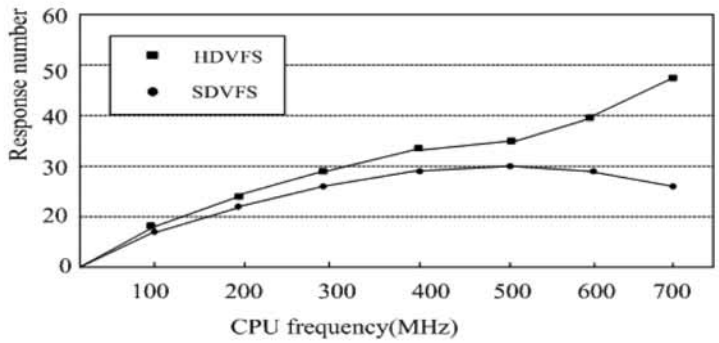
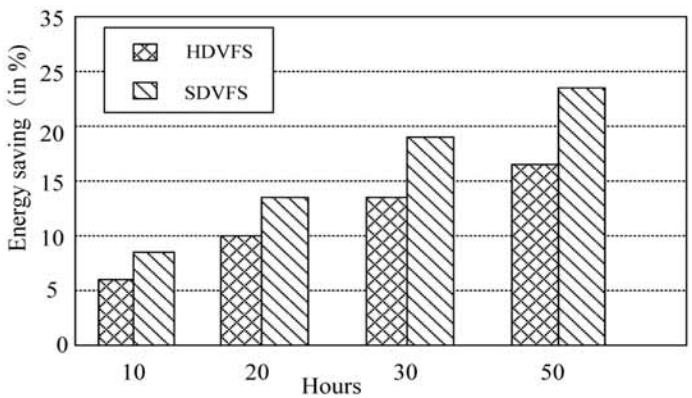


Figure 8: Saving power with the DVFS



logic as described below.

The input signal of the CPU idle time-counter depends on the configured operation mode:

• If forced mode is enabled, the input signal of the CPU idle time counter is the tracking clock, which may be further divided according to the configured setting for the forced mode clock divider.

• If forced mode is disabled, the input signal of the CPU idle time counter is the wait-for-interrupt (WFI) signal based gated tracking clock, i.e. input signal clock edges will only by counted while WFI signal is asserted by the ARM Cortex A9.

The monitoring counters are 16 bits wide, allowing a maximum time of 20 milliseconds for the monitoring period using the 3.25MHz clock. The typical monitoring period is 1ms (3250 clock cycles).

For the forced mode, it can be enabled or disabled according to the actual requirement. If forced mode is enabled, then the input signal for the CPU idle time counter is not gated by the WFI signal. In forced mode, the tracking clock can be divided before it is fed into the CPU idle time counter. The corresponding forced mode clock divider setting can be configured through the register interface. Whenever forced mode is enabled, the configured forced mode divider factor is applied by hardware.

The sequence control logic is triggered when the underflow event of the 'monitoring period' counter occurs. When triggered, the following sequence of tasks must be performed in such a way that a consistent set of data is always used in the processing steps of the hardware support function:

- Latching of the counter value of CPU idle time counter.
- Resetting of CPU idle time counter.
- Activation of an average-ready signal in order to trigger averaging function block.

Averaging Function

The calculation of the average idle times is triggered at each monitoring period boundary and for the two supported scaling steps (down, up). An individual average idle time value is calculated and maintained.

It is also important to note that the Moving Average Algorithm (MAA) is firstly introduced in the averaging block. The MAA not only tracks and samples the idle time of the CPU with small enough intervals, but also executes the accumulation and average calculation of the idle times. The MAA equations are given as follows:

$$T_{up}(n+1) = \frac{1}{N}\sum_{k=0}^{N-1} T(n-k) \quad (2)$$

$$T_{down}(n+1) = \frac{1}{M}\sum_{k=0}^{M-1} T(n-k) \quad (3)$$

where n, M and N are the positive integers and usually M > N > 0. $T_{up}(n+1)$ stands for the average of the idle time from the sampling time 0 to N-1, $T_{down}(n+1)$ stands for the average of the idle time from the sampling time 0 to M-1.

When triggered by the instantaneous idle time calculation function block, the following tasks are performed by the average idle time calculation function block:

• Read current values from time tracking function block and write it to the FIFO.

• For each of the supported two scaling steps, an accumulator and division circuit calculates the current value associated with that scaling step by processing so many values from the beginning of the FIFO as specified by the

configured number of corresponding averaging periods (see also Figure 4, but note that the given averaging period values are examples only).

The FIFO has a depth of 64 words in order to allow averaging up to 64ms, even for a configured monitoring period duration of 1ms. The width of FIFO entries is the same as the width of the CPU idle time counter in the time tracking function block.

Threshold Check

The threshold checking is triggered at each monitoring period boundary when the averaging function block has finished calculating the averaging idle times. For each of the two supported scaling steps (down, up), the calculated average idle time value is compared against the individual threshold value. The values for these threshold limits are configurable by software through the register interface.

When being triggered by the averaging function block, the following tasks are performed by the threshold checking function block:

- Read current values for the two supported scaling steps from the averaging function block.
- Compare these values against the configured threshold values for each of two supported scaling steps and check for exceeding of each threshold (i.e. check for CPU clock scaling step condition being fulfilled) according to:
  - CPU clock scaling down step condition is fulfilled if $T_{down} > T1$
  - CPU clock scaling up step condition is fulfilled if $T_{up} < T2$.
- Generate CPU clock scaling step interrupt if at least one of above condition is fulfilled.

Figure 5 shows an exact transition among three different voltages and frequencies. The threshold checking results for both supported scaling steps are updated once after each monitoring period, but reading the latest results is possible at any point in time.

In an application the CPU can be configured with the scaling down threshold value (T1) and the scaling up threshold value (T2). The two threshold values of the CPU idle time have to be set before the DVFS is requested.

Performance Implementation

As shown in Figure 6, the clock generator includes a Phase-Locked Loop (PLL), a clock divider and a digital multiplexer. The PLL can convert a low-frequency external clock signal that is generated by the on-chip 32.768kHz oscillator to the high-speed internal clock's maximum frequency. Depending on the different frequency requirement, the clock frequency output may be configured by programming the desired P, N and K values according to Equation 4. The PLL output can be defined as:

$$f_{sys} = f_{osc} * N/(P * K) \quad (4)$$

where N, P and K are pre-defined factors according to the actual requirement. The CPU clock is derived from the oscillator clock (f_{osc}), multiplied by N, divided by P and divided by K. The clock output from the clock dividers can be stated as follows:

$$f_{uhigh} = f_{sys} / X0$$
$$f_{high} = f_{sys} / X1$$
$$f_{med} = f_{sys} / X2$$
$$f_{low} = f_{sys} / X3$$
$$f_{ulow} = f_{sys} / X4 \quad (5) - (9)$$

where X0, X1, X2, X3 and X4 are the integers and X0 < X1 < X2 < X3 < X4, f_{uhigh} represents the ultra-high input clock frequency of CPU, f_{high} represents the high input clock frequency of the CPU, f_{med} is the medium input clock frequency of CPU, f_{low} is the low input clock frequency of the CPU, and f_{ulow} is the ultra-low input clock frequency of CPU. Moreover, according to Equations 5-9, we can conclude that $f_{uhigh} > f_{high} > f_{med} > f_{low} > f_{ulow}$.

In practice, depending on the needs, five voltage and frequencies of CPU may be initialized with the following settings:

$$(V_{uhigh}, f_{uhigh}) = (1.30V, 700MHz)$$
$$(V_{high}, f_{high}) = (1.20V, 520MHz)$$
$$(V_{med}, f_{med}) = (1.0V, 360MHZ)$$
$$(V_{low}, f_{low}) = (0.90V, 240MHZ)$$
$$(V_{ulow}, f_{ulow}) = (0.80V, 100MHZ) \quad (10) - (14)$$

Experimental Results Comparisons

Firstly, the accuracy of the response to the CPU performance requirement is evaluated between the conventional software DVFS and the hardware DVFS. In the experiment, the frequency of the CPU is continuously increased. According to Figure 7, we know that the speed of the software DVFS is unable to keep pace with the faster CPUs.

As shown in Figure 8, it is obvious that the hardware DVFS offers more advantages than the software-only DVFS in reducing power consumption, and the effects of saving energy become evident with the delay in running time. Furthermore, compared with software DVFS, the hardware DVFS are better at saving energy. As such, hardware DVFS is an efficient and smart way to save energy. In the future, the hardware DVFS will be dominant in OCMSs because of this higher efficiency.

TAMING ELECTRICAL ENERGY WITH POWER ELECTRONICS

A THYRISTOR IS A SEMICONDUCTOR DEVICE WHICH ACTS AS A SWITCHABLE DIODE, ALSO KNOWN AS A SILICON CONTROLLER RECTIFIER (SCR). HERE, **JEZ WATSON** OF CD AUTOMATION EXPLAINS THE APPLICATION OF THYRISTOR CONTROL FOR SIMPLE AND COMPLEX HEATING LOADS AND FOR TEMPERATURE CONTROL IN OVENS, FURNACES AND OTHER HEAT TREATMENTS

Thyristors can control electrical loads up to 3000kW from simple single-phase heaters up to complex high temperature-coefficient three-phase loads. A machine manufacturer will typically choose a thyristor based on the type of heating element required.

There are essentially six types of load: (1) normal resistive, (2) loads where resistance changes with time, (3) applications where resistance changes with temperature, (4) fast responding loads, and (5) and (6), transformer coupled loads of various types.

In the first case, a normal resistive load applies to any load element with a resistance change of less than 10%, with a typical element made of iron chromium or nickel chromium. Typical firing method is zero-crossing, burst firing or single cycle.

In the second case, where resistance changes with time, resistance starts high when the element is new and decreases with age, then increases again as aging progresses. The typical element type is silicon carbide with phase angle firing.

Figure 1: REVO S

The third case is where resistance changes with temperature, acting as a short circuit when cold, with resistance increasing as temperature increases. Here, the typical element type is molybdenum, tungsten or Super Kanthal, and firing is phase angle plus current limit.

The fourth case is fast-responding loads with high surge currents and where high resolution is required; typically short wave infrared (SWIR) lamp using phase angle firing. Medium/long-wave IR is treated as normal resistive.

Finally, the last two cases apply to transformer coupled loads with high in-rush current on start-up. In the fifth case, the transformer is connected on the secondary winding and the firing method is typically phase angle or soft-start plus current limit. In the sixth case, the transformer connected to the secondary winding and firing method is typically phase angle plus current limit.

> A normal resistance element that does not vary with temperature or time allows a basic type of firing

Load Resistance

A normal resistance element that does not vary with temperature or time allows a basic type of firing. Because temperature response times are not critical, unlike pressure or flow measurement, where quick reaction time is required, simple on-off firing is cheap and adequate.

Time-proportioned on-off or burst firing is used with DC linear type signals, such as 4-20mA current or 0-10V voltage. This will switch bursts off then on for better temperature control.

If the element type used is more complex, for example silicon carbide or Super Kanthal, which operates at high temperatures and varies with time and temperature, the firing method requires more sophistication.

In addition to various firing methods, proportional integral derivative (PID) feedback control may be employed. Supply voltage fluctuations change the power to the load so, to

overcome this effect, the voltage supplied to the load is measured and compared with the power demand from the controller.

A PID controller examines signals from sensors placed in a process, called feedback or error signals. The error signal is used to automatically hold the power at the value requested. When a feedback signal is received, it is compared with the desired value, or set value, and a calculation is made to match it to the set value. Process controllers generally work on the principle of a 'closed-loop'.

Taking a typical application like an oven, the measured temperature, referred to as the process value (PV), is fed into the controller and compared to the set value (SV): the desired temperature. As the temperature rises, the power to the oven is reduced by the controller until the desired temperature is reached.

Most industrial processes such as plastic extrusion require stable, straight-line control of temperature. The example shown assumes that the variable is temperature, but the principles are equally applicable to all analogue variables.

> The integral function, also called 'reset', has one primary goal: to eliminate offsets

The integral function prevents the initial overshoot on power-up, while the derivative function eliminates the temperature instability over time once the set value is achieved and the process is under control. Most heating applications can be handled by proportional control only.

PID Terms

A proportional controller has the ability to vary its output between 0-100%. This enables it to continuously adjust the output so the power input to the process is in balance with the process demand.

The range, or band, where the output power is adjusted, is called the proportional band (PB). The difference between the stabilised PV and SV is called 'offset' and can be reduced by narrowing the proportional band. However the proportional band can only be reduced so far before instability occurs.

This is where the 'integral' term comes in. Integral, also called 'reset', has one primary function: to eliminate offsets. This eliminates the temperature offset condition caused by proportional control on system start-up. To reduce or eliminate overshoot, we must use the D or derivative term of PID control.

In many thermal systems, overshoot (or undershoot) of the set value temperature is perfectly acceptable. However, in some systems this can produce poor quality products or perhaps even damage expensive equipment.

So derivative has one main job: to prevent or greatly reduce overshoot and undershoot. If the temperature rise is too fast, it will begin switching the heater off to prevent overshoot. If the temperature is falling too fast, it will begin switching the heater on longer to prevent undershoot.


Figure 2: REVO Multidrive

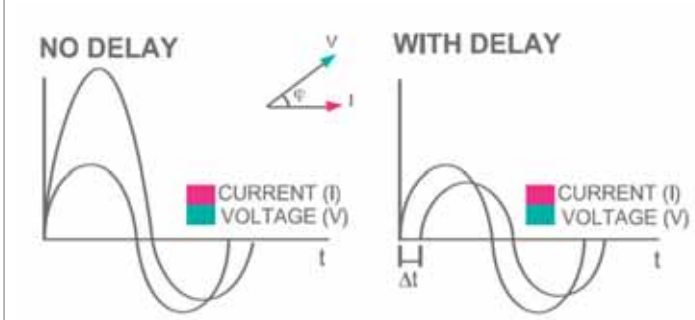


Figure 3: Current voltage with delay and without delay

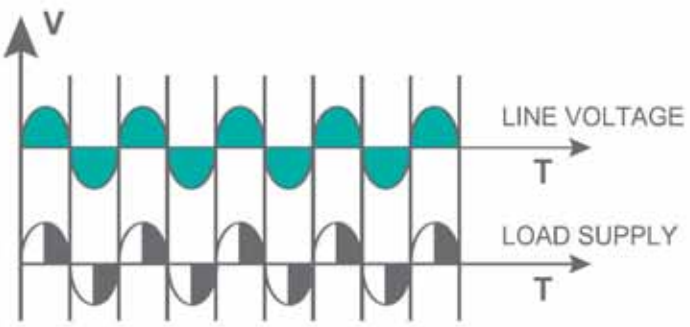


Figure 4: Line voltage verses load supply

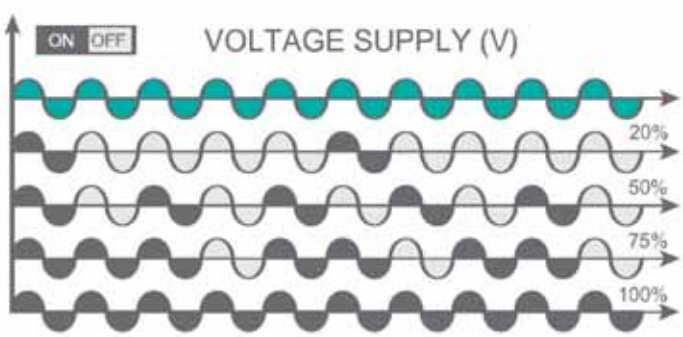


Figure 5: Single cycle voltage supply

Figure 6: Soft start and burst firing voltage supply

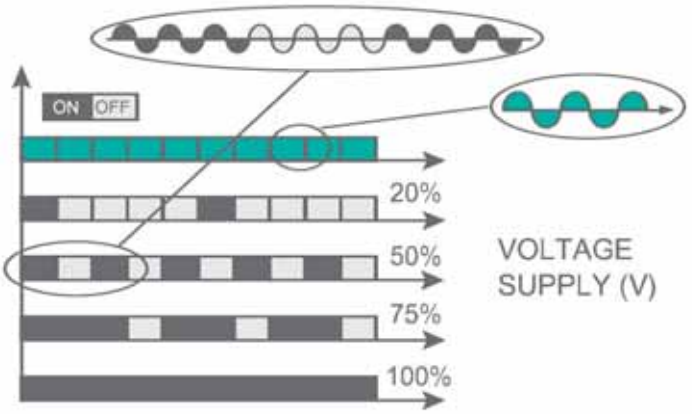


Figure 7: Collins Walker application

Another way to think of derivative is that it opposes change. For example, if the temperature suddenly drops below the SV, derivative opposes the rapid drop by turning the heater full on. Luckily for us, most PID controllers come with automatic PID tuning.

Vacuum Furnaces

A thyristor can also control furnace heating and be integrated into a closed loop PID control system, providing more accurate feedback control of the heat treatment process.

The 4-20mA signal from a controller adjusts the output from the thyristor, then the furnace temperature is fed back to the controller via thermocouples. A thyristor can use 0-10V voltage analogue signals as well, if needed, but some vacuum furnace users prefer to stick with 4-20mA current signals because this provides better control.

Furnace brazing is a semi-automated process in which metal components are joined using a dissimilar lower melting-point material. Furnace brazing allows design and manufacturing engineers to join simple or complex designs for one joint or several hundred joints.

Parts to be joined are normally cleaned, and brazing alloy applied to the surfaces to be joined, and then placed into the furnace. The entire assembly is brought to brazing temperature after the furnace has been evacuated of air to eliminate any oxidation or contamination - the braze alloy liquefies and flows throughout the brazed joints. ●

CASE STUDY

COLLINS WALKER LIMITED

Thyristor control can enhance pollution-free steam generation. Simple on-off switching was found to be too brute a force for electrode boilers over 100kW at Collins Walker Limited, a manufacturer of electric steam and hot water boilers, so CD Automation helped the company to switch from contactors to thyristor control.

An electrode boiler conducts an electric current through water between a pair of electrodes. It is more robust than an immersion type. One of the reasons for this is that it does not use heating elements and associated switching needed to control them.

Collins Walker's immersion boilers have traditionally used relay contactors to control power switching to the elements. Because of their smaller rating, this can amount to a bank of up to 60 contactors on larger boilers. With their associated wiring, contactors can be a source of faults and require regular maintenance.

Although having multiple contactors gives some degree of control, by staging the switching the boiler and the electrical supply can still be subject to power surges. With larger boilers rated at thousands of kilowatts, even Collins Walker's power station customers are concerned about the huge draw when boilers are switched on. The heating elements themselves suffer thermal shock each time the power is switched, and this leads to element failures.

Collins Walker replaced all 60 contactors with a single thyristor, which cut down wiring significantly. Contactors have a finite life and start burning out after prolonged use, giving rise to maintenance issues over time. A solid state thyristor is contactless so there is no arcing of the type that accelerates contactor wear. Because CD Automation's thyristor controllers are designed for ease of installation, Collins Walker was able to configure and set them up in-house without the need for expensive engineering consultancy.

The current handled by the boiler is 850A at 415V. Collins Walker now uses thyristor controllers on all but the smallest boilers – those less than 100kW, which only have one or two contactors. The controllers are programmed to bring in the power gradually, for example starting at 10% for a few seconds before moving on to 20% and so on.

The power is also reduced gradually instead of being abruptly switched off, smoothing the whole process of switching the power on and off. This gradual power process is similar to soft starting on electric motors and has been found to be particularly useful at one of Collin's Walker customers, Jersey Power Station, where the need is to heat water by gradually switching in heater banks.

The thyristor is attached to a programmable logic controller (PLC), forming part of a proportional integral derivative (PID) loop. This helps to anticipate the lag in the system, so the on or off switching occurs just before it is needed.

This prevents thermal overshoot, where the elements are still supplying heat after the set temperature has been reached and the power switched off, making the boiler more energy-efficient. This is only possible with thyristor control as a PID Loop cannot be implemented on a boiler using contactors. A PID temperature controller can take advantage of burst firing, which is a time-proportioned on-off method.

FIRING METHODS

ZERO CROSSING

Zero crossing firing mode is used with the logic output from a temperature controller, so the thyristor operates like a contactor. The cycle time is performed by the temperature controller. Zero crossing minimises interferences as the thyristor unit switches on-off at zero voltage.

BURST FIRING

Burst firing is performed digitally within the thyristor unit at zero volts, producing no EMC interference. Analogue input is used and the number of complete cycles must be specified for 50% power demand. This value can be between 1 and 255 complete cycles, determining the speed of firing. When 1 is specified, the firing mode becomes single cycle.

SINGLE CYCLE

Single cycle is the fastest zero crossing switching method. At 50% input signal, one cycle is on and one cycle is off. At 75%, three cycles are on and one cycle is off. If power demand is 76% the unit performs the same as for 75% but every time the unit switches on the microprocessor divides 76/75 and memorises the ratio. When the sum is one the unit delivers one cycle more to the load. With this firing it is necessary to have analogue input.

DELAYED TRIGGERING

Used to switch the primary coil of transformers when coupled with normal resistive loads (not cold resistance) on the secondary, delayed triggering prevents the inrush current when zero voltage (on-off) is used to switch the primary. The thyristor unit switches off when the load voltage is negative and switches on only when positive with a pre-set delay for the first half cycle.

PHASE ANGLE

Phase angle controls the power to the load by allowing the thyristor to conduct for part of the AC supply cycle only. The more power required, the more the conduction angle is advanced until virtually the whole cycle is conducting for 100% power. The load power can be adjusted from 0 to 100% as a function of the analogue input signal, normally determined by a temperature controller or potentiometer; PA is normally used with inductive loads.

SOFT START PLUS BURST FIRING

This is an additional feature to burst firing. Starting in phase angle mode, the unit ramps from zero to full voltage at a pre-set time, finishing at full conduction for the remainder of the on period. Ideally used to switch small inductive loads, soft start plus burst firing avoids current surge and minimises electrical interference.

POWER CONSUMPTION OPTIMIZATION IN THE SMART HOME

JURE MOČNIK AND **MATJAŽ FINC** FROM RC ENEM AND ISKRA SISTEMI IN KRANJ AND **ANDREJ ŽEMVA** FROM THE FACULTY OF ELECTRICAL ENGINEERING IN LJUBLJANA, SLOVENIA, DESCRIBE A CONCEPT FOR OPTIMIZING POWER CONSUMPTION IN THE SMART HOME USING SMART SWITCHES AND DEMAND SIDE MANAGEMENT (DSM)

The economic growth enjoyed by consumers and their growing dependence on mains-powered systems has pushed energy consumption up by 1.7% per year between 1997 and 2007, with electricity consumption jumping by 33%. Such figures are forcing utility companies worldwide to increase their electricity production but, also, to improve their power grids and facilitate an efficient use of electricity.

A load managing technique called 'load shedding' recently appeared in the energy sector; it's part of demand side management (DSM) in the distribution network. The technique imposes a power shutdown when demand for electricity exceeds that of generation in the network.

Load Shedding

Load shedding is usually used in two cases: when power generation is of insufficient capacity or the distribution infrastructure is inadequate to deliver enough power to the network for normal operation. Despite its benefits, this technique has one very big disadvantage – it activates when energy consumption is at a peak, which is normally at a time when users need electricity the most, such as on a hot day for example, when they want to use air conditioning systems, or on a cold day when they boost their heaters.

Load shedding allows distributers to reduce the user's electricity bill, but this is deceptive. Therefore, energy consumers should ask themselves if they want to participate in such a scheme, where they would give up their comfort in exchange for reducing their electricity bill by up to 5%.

Equally, however, users should be aware that electricity generation is not an unlimited resource and that our consumption habits must change to make the existing energy infrastructure sufficient.

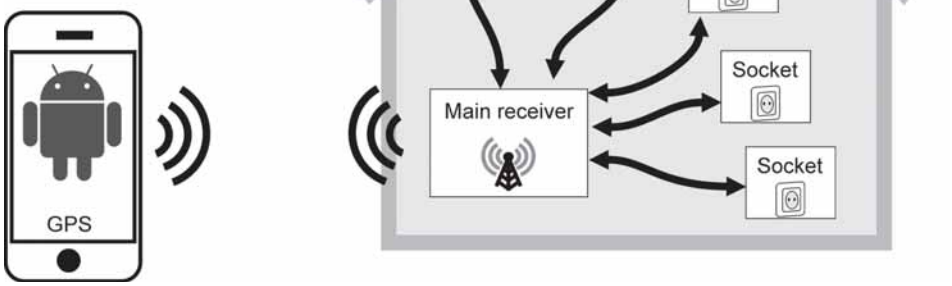


Figure 1: The key elements of the concept

New Power Management Concept

There are systems that have to be permanently powered, such as freezers, refrigerators etc, or activated on demand, such as television sets, computers, heaters, coolers etc, which consequently leads to the conclusion that consumption managing cannot be performed with a single technique. For those devices that are not part of a DSM, their consumption can be simply reduced with a remote control technique. Such a technique would activate and deactivate systems from the home power network when they

are not needed. But how can this be achieved while ensuring creature comforts when required?

To solve these types of problems and at the same time actively participate in DSM, a new concept of power consumption optimization is presented here. The concept is highly user-orientated but with the benefits of load shedding. It is designed with two differently-orientated sections based on a common infrastructure. The first part of the structure regulates the network's voltage profile within the scope of demand side management. It includes time-independent smart home devices such as washing machines, dryers, dishwashers etc, which are part of load shedding controlled by the distributor.

The second but more important part of the structure aims to maintain the luxury in life and yet save electricity at the same time.

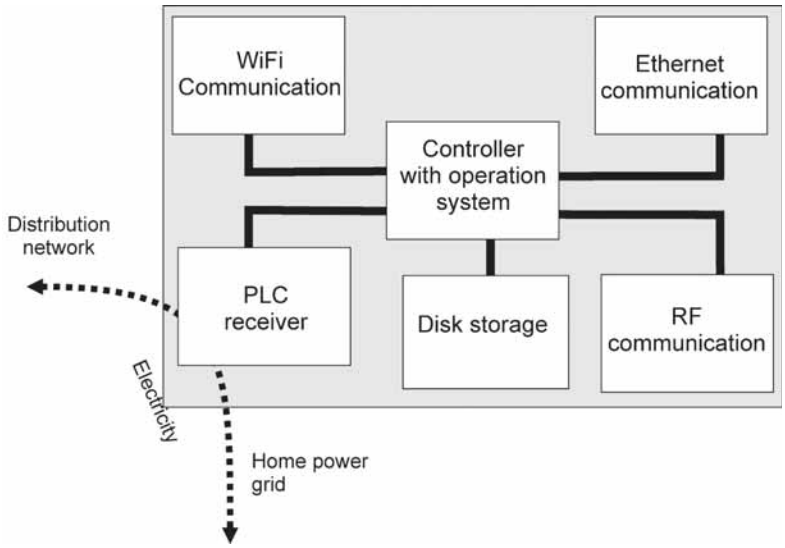


Figure 2: Receiver platform structure

The Structure's Key Elements

Devices such as heaters, lights and others can be controlled by users in two ways. One is through a GPS (global positioning system), where the user relies on a GPS transmitter, found in almost all smartphones nowadays, to send a signal, when in the vicinity of their home. So, for example, if the user is within a 10km zone from home, the water heater in the house will turn on. The advantage of the proposed structure over the timers is in flexibility of system. Unexpected circumstances and daily, changeable, activities can be easily managed with such an approach.

> Energy consumers should ask themselves if they want to participate in such a scheme, where they would give up their comfort in exchange for reducing their electricity bill by up to 5%

The second way of controlling home devices is through the Android/Windows application, where the status of home devices can be monitored and manually changed.

Figure 1 shows the key elements of this concept, which is divided into execution and service parts. The execution elements are built in the smart house and are responsible for the execution of the received commands. On the other side are the service elements (an Android smartphone, GPS tracker) that monitor and control the execution elements remotely.

Smart receivers

The main component of the execution elements is the smart receiver which transfers data between DSM and the execution and service sections. Figure 2 shows the main components and interfaces between all of them. The controller links all the components and controls the information received from each.

The receiver can obtain the data in several ways. First, it can get the information from DSM through a power line communication (PLC) receiver. The second option is to get it from a user's application or through Ethernet. There's also the possibility to get the information through a GPS receiver.

The obtained data is then forwarded on to the controller, which relays the information to the target smart switch in RF (radio frequency) communication based on the ModBus standard. The data is also saved in case there's power loss. The selected RF communication frequency (868MHz) is part of the ultra-high frequency (UHF) spectrum and works as a full-duplex RF system.

The smart switch

The second execution component is the smart switch whose structure is shown in Figure 3. There are three types of switch sockets, which vary depending on the number of output units (one, two or three) and a light switch, which has a minimized structure (there is no DSM button, for example, only one bistable relay, giving it its small dimensions).

At the centre of the smart switch is a microcontroller which communicates with the smart receiver through a unique address in RF technology. The main microcontroller tasks are to control the bistable relays, receive and transmit the data from the measuring centre (which is already measuring all the parameters and is included in the smart switch) and to broadcast the device's status (on or off). This information is then sent to the smart receiver which redirects it to the user's application, where the device can be checked or adjusted.

One of the features of this smart switch is the DSM button which can arrange that a certain socket or a group of them participate in the DSM scheme. The smart switch also includes an internal memory where the measurements are stored. The data is analyzed, sent to the receiver and stored in templates, which are used to auto-recognize the connected devices. The algorithm for the templates is based on a self-learning application, configured by the user.

Android and the Windows applications

At the centre of the service elements are Windows and Android applications, which communicate with the smart receiver. The Windows application is designed to easily create a virtual structure of the home with its smart receiver and smart switches. This

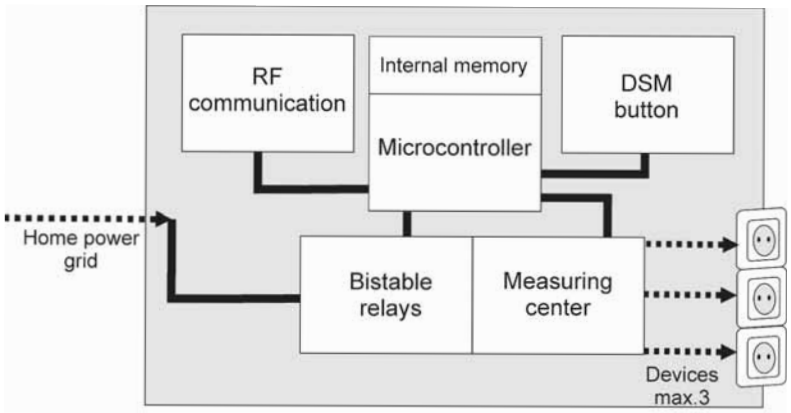


Figure 3: Switch platform structure

application also allows controlling the devices but is rather awkward due to immobility of PCs. A more practical element is the Android application (shown in Figure 4), as it allows easy access to the home network with its devices.

In the last image of Figure 4 it can be seen how easy it is to manage the lights in a living room on the ground floor for example, with an on/off button. The application also contains a monitor which shows how much energy the device consumes. The special feature of this application is the GPS mode, which can automatically manage the device based on the user's distance from home.

Operation Of The Concept

The first step in optimizing energy consumption based on this concept is to run the Windows application and build a virtual house with all its lights, sockets and devices depicted. In this virtual model, the user sets the mode of operation (DSM mode, smart mode or permanently energized mode) for each individual socket. This task is very complex and time-consuming but it greatly simplifies the process that follows. To make the service on the go, it is recommended to install the application into an Android device.

The smart receiver can work in three operating modes simultaneously. The DSM mode is used to connect the devices that are part of load shedding (the user has no control when they are activated). This mode can be easily chosen in the application or by pressing the DSM button on the smart switch. The mode will be activated with the distributor command through the PLC or Ethernet. This mode is suitable for dishwashers, tumble dryers and similar devices.

The second mode is the permanently-energized mode, where the sockets are under constant voltage. This mode is intended for devices that must remain constantly on, such as fridge-freezers for example.

The last mode is the most dynamic of all – the smart mode. It can work in three different ways. When fully automated, it is guided by a timetable and/or a GPS device. If a timetable is used, then the operations are guided by a schedule that's been saved in the smart receiver and obtained from the Windows or Android application. Otherwise, the operations are guided by a GPS tracker. Each device or home socket can be set up in GPS guidance mode, where a radius within which the device will activated is set up. In this case, the GPS device submits the obtained location to the smart receiver inside the home, which activates or deactivates a device. The receiver can also work in manual mode where every command is sent from the Windows or Android application. The transmitter sends out information every 5 seconds until it gets acknowledgement from the receiver (this is done to prevent losing the GPS or RF signal).

There is also a third mode of operation and this one we find is the most useful, as it combines the manual and automatic modes. Some devices are made in a way that full shutdown is not the optimal choice for maintaining optimal consumption, so it is necessary to accommodate them with a specific list in the application. One such device is the water heater, which consumes less energy if its temperature does not fall below a certain limit. In this case, the application offers a special option that allows to set the minimum allowable temperature.

Changing the Ways of Consuming Power

World energy consumption increases by the second and with it there's a greater demand on building new power plants – distributed or concentrated. However, building them is a lasting process and not a short-term solution for providing enough energy. Part of the solution lies in changing user habits, and especially through techniques that optimize energy consumption.

The problem arises because people don't want to sacrifice comfort afforded by electricity, even though this may mean higher energy bills for them. So, a new concept of energy optimization is presented here, which includes the load shedding scheme, guided by demand side management and a smart home structure which can be automatically or manually guided by a GPS or an Android phone. With this concept it is possible to save a lot of energy; how much depends on consumer habits of using electric power.

Our future work will focus on moving this concept on and developing electronics devices from prototype to a commercial system. ●

Figure 4: The Android application

Thales

Thales UK selects XJTAG for software radio testing

"Thales UK needed a fast, extremely versatile and cost-effective boundary scan solution to debug and test complex printed circuit boards (PCBs) used in its market-leading range of software defined radios (SDRs)"

Thales UK's MSN 8100-H software-defined radio (SDR) platform, the first European operational software radio, has been designed as the primary component of a comprehensive high frequency communication network benefiting from the attributes of a versatile, programmable and configurable multi-channel receiver/exciter. This radio is designed for naval and ground based applications and will be used on the Royal Navy's next class of Destroyers, the Type 45, scheduled to enter service in 2009.

As with many of today's network-centric systems, the SDR uses the very latest technology. For example, the baseband boards in the MSN 8100-H are densely populated and use fine pitch high density connectors, as well as large and expensive BGA/FPGA devices, all of which make the boards difficult to test by traditional methods.

To overcome these debug and testing challenges, Thales has adopted the XJTAG system for use by development and production engineers at its Crawley, West Sussex (England) facility. The XJTAG system is also being used by Thales' contract manufacturing partner. Initially, the XJTAG system will be used to debug and test the baseband PCBs that form part of the MSN 8100-H SDR.

"It made sense for us to use the JTAG chain for debug and testing, as more and more devices on our boards were JTAG-enabled – and - we opted for the XJTAG system as it was the best and most cost-effective solution," said Gary Delamare, senior engineer, Thales UK.

"The XJTAG system is truly intuitive – it's almost a plug and play solution. We were up and running within half a day using the tutorial and development board, and test coverage, for digital circuits, is up around the 80 percent mark already."

The XJTAG system is designed to cut the cost and shorten the development cycle of electronic products and provides a unique solution that can test JTAG as well as non-JTAG devices. XJTAG can test a high proportion of a circuit including BGA and chip scale devices, SDRAMs, Ethernet controllers, video interfaces, flash memories, FPGAs, microprocessors and many other devices. XJTAG can be used to debug and test any circuit provided it has at least one JTAG-compliant device present.

The ability to program Flash memories and other non-JTAG devices was an important factor for Thales. By using XJEase (the XJTAG system's high-level test description language for manipulating non-JTAG devices), engineers had a rapid means of programming Flash memories both at the development stage and through into production. "Unlike other JTAG tools, XJEase enables circuit developers to re-use XJEase scripts in different projects," added Gary Delamare. "This portability is really valuable and is not available with traditional programming tools which tend to be tied to one particular processor."

Thales UK's defence activities encompass optronics, air defence, sensors, communications and naval systems. The company is the UK's second largest defence contractor and has been a supplier to the MoD since the First World War. Thales employs 10,000 staff in the UK and 60,000 people in 50 countries.

opinion

Simon Holder
Hardware Design Manager
Thales UK

"XJTAG is a fast, extremely versatile and cost-effective tool for generating high test coverage on PCBs containing both JTAG and non-JTAG devices. The XJTAG system has enabled us to cut the development time for debugging and testing boards by around 20 percent and it has provided the basis for a common design for test strategy, spanning development, first article build, production and field service. We looked at other boundary scan solutions but we opted for XJTAG due to its price and ease of use, and the fact that test scripts are device rather than board-centric, which makes them reusable on different projects."

Data Bank

THALES

Company	Thales UK
Nature of business	UK's second largest defence contractor
Main product	Flight simulation, secure transactions, integrated communications, naval and air defence systems
Customers	Military and industrial
Locations	60 sites across the UK
Employees	10,000 in the UK 60,000 worldwide
Web site	www.thalesgroup.co.uk

IMPLEMENTATION OF A CHEAP AND FLEXIBLE KEYPAD ENCODER

ASSISTANT PROFESSOR **GÖKHAN GELEN** FROM THE GAZIOSMANPAŞA UNIVERSITY IN TURKEY PROPOSES A CHEAP AND FLEXIBLE KEYPAD ENCODER IC DESIGN METHODOLOGY, BASED ON THE PIC16F628A MICROCONTROLLER

In many of microcontroller-based applications, the user interface can be a keypad, which generally includes 12 or 16 keys in a matrix type connection. The hex keypad is a peripheral that includes 16 buttons in a 4 x 4 grid, labelled with the hexadecimal digits 0 to F.

Internally, the structure of the hex keypad is very simple. Wires run in vertical columns (C0 to C3) and in horizontal rows (R0 to R3). These eight wires are available externally, and can be used for evaluation of key states. Each key on the keypad is essentially a switch that connects a row wire to a column wire. When a key is pressed, it makes an electrical connection between the row and column.

Keys Scanning Methods

Various methods are used to evaluate the status of the keys, with the most popular and widely used being the scanning of keys. The keypad scanner is a systematic search. In this method, the column pins and row pins of the keypad are connected to microcontroller's input ports and output ports respectively. The column pins are also connected to supply power by pull-up resistors (10kΩ-100kΩ). Because of these pull-up resistors, the columns are read as logical '1'. The object of the search is to determine if one of the rows of the keypad is shorted to one of the columns. The scanner outputs a '0' to one of the rows, then looks at the column inputs to see whether that '0' shows up. If not, it turns off that row and tries the next row.

There are other methods that reduce pin count. Among them are those that use analog-to-digital converters and those that use keypad scanner chips.

In order to encode the keypad, there are a number of chips, including MM74C922, EDE1144 and DFL-KEY55B. The most popular one is MM74C922, made by a number of manufacturers, including National Semiconductor and Fairchild Semiconductor. However, this chip is now obsolete, even though some electronic component distributors are still selling it.

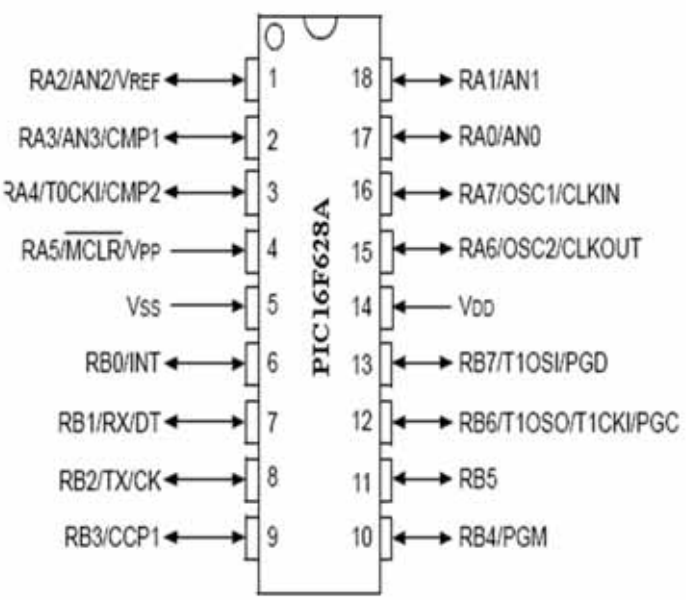
Table 1 gives a brief comparison of the keypad encoder ICs. It can be seen that the price of chips starts from around $4 to $9 per IC. MM74C922 has only parallel output and DFL-KEY55B has only serial output. EDE1144 has parallel output and serial outputs at 2400 and 9600 baud rate. Although MM74C922 requires two external resistors, EDE1144 requires a crystal and eight resistors, and DFL-KEY55B requires an external crystal, two capacitors and 10 resistors.

In addition to these chips, there are some small circuits, such as Storm interface 420 Series and ABTPRO for keypad encoding. These circuits have some extra specifications, such as an LCD driver and a direct connection to computers. Prices start at around $60.

In this article, a cheap and flexible keypad encoder design idea is presented with its specifications listed in Table 2. The proposed keypad encoder is implemented using a PIC16F628A microcontroller. It cost comes to only $2, which is very cheap compared to the other chips mentioned here.

The pin configuration of the PIC16F628A can be changed by source code. So, the flexibility of the proposed keypad encoder is related to the changeable connection pins. Other benefits include selection of baud rate (1200, 2400, 9600 or 19200) and selection of data format (hexadecimal or ASCII). Most importantly, the PIC16F28A chip is still available to buy.

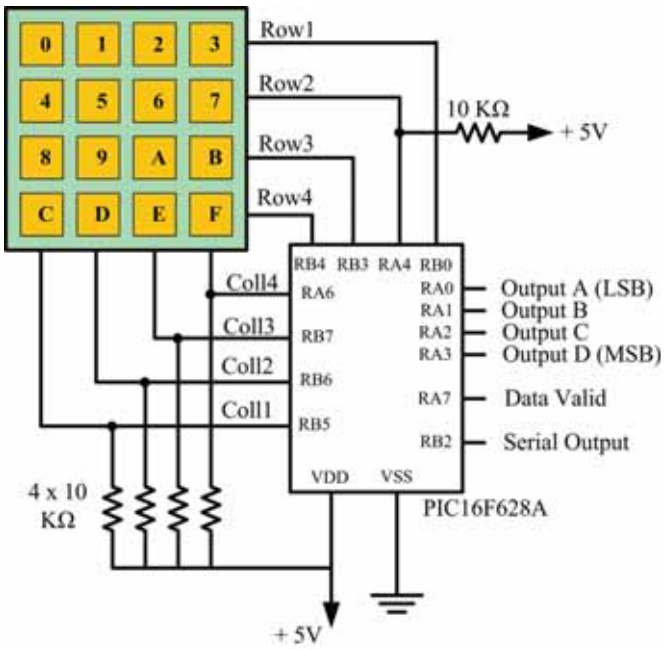
Figure 1: A PIC16F628A microcontroller



The Hardware Of The Keypad Encoder

The proposed keypad encoder IC is implemented using the PIC16F628A microcontroller, as seen in Figure 1. The device

Figure 2: Typical application circuit



comes in four different packages: 18-LEAD PDIP, 18-LEAD SOIC (.300”), 20-LEAD SSOP and 28 LEAD QFN. This means that the proposed keypad encoder can be accommodated in one of these packages depending on the application.

The features of the proposed keypad encoder IC can be summarized as follows:

- Up to 16 keys (4 x 4) encoded per IC;
- Parallel outputs with hexadecimal and ASCII choice;
- Serial outputs with selectable baud rate (1200, 2400, 9600 or 19200) and also with hexadecimal and ASCII choice;
- Data valid output signal for interrupt activation;
- Flexible pin configuration;
- Available in four packages (PDIP, SOIC, SSOP and QFN);
- Only 4 external resistors are required for column pull-up connection and a resistor is required for RA4 pull-up connection. In total, five external resistors are required.
- Supply voltage range = 3.0V to 5.5V.

A typical application circuit is shown in Figure 2, which also shows the connections between a hex keypad and proposed encoder IC based on PIC16F628A.

For encoding a hex keypad, four pull-up resistors are required as explained earlier. These resistors are connected between column pins and the supply voltage. When no key is pressed, a logical ‘1’ will be read , but when a key is pressed, then the data reads as ‘0’. In addition to this, a resistor is required for the RA4 pin of PIC16F628A for the pull-up connection.

Keypad Encoder IC	MM74C922	EDE1144	DFL-KEY55B
Price ($) for One IC	$8.95*	$5.19*	$4.34**
Parallel Output	YES	YES	NO
Serial Output	NO	RS232	YES
Baud Rate	NO	2400/9600	4800
External component requirement	2 capacitors	Crystal and 8 resistors	Crystal 2 Capacitor 10 Resistor
Packages	DIP, SOIC	DIP,SOIC	DIP, SOIC
Operating Voltage	3-15V	4,5-5,5V	2-5,5V

Table 1: Comparisons of some keypad encoder ICs
*The Price is taken from www.jameco.com for PDIP package.
**The Price is taken from www.dafulaielectronics.com for PDIP package.

µC used	Price ($) for One IC	Parallel Output	Serial Output	Baud Rate	External Component required	Packages	Operating voltage
PIC16F628A	$1,73*	YES	YES	1200 2400 9600 19200	5 Resistor	PDIP SCIC SSOP QFN	3-5,5V

Table 2: Some specifications of the proposed keypad encoder
*The Price is taken from http://www.microchipdirect.com for PDIP package.

The Software Of The Keypad Encoder

The software of the keypad encoder is developed in PIC assembly language by using Microchip's MPLAB IDE. This program can be downloaded from www.microchip.com and is free.

Users have the opportunity to modify the source code of the keypad encoder. The assembly code of keypad encoder starts with IC pin assignment code block. The pin connection of the keypad encoder can be modified by changing these assignments by sticking to the hardware limitations as described earlier. Following the IC pin assignment, the baud rate adjustment codes are located. Baud rates can be adjusted by assigning d'103', d'207', d'25' and d'12' to baud rate for 2400, 1200, 9600 and 19200, respectively. After that, the keypad encoder's main codes are located. In the main code, rows are set one by one and columns are read. In order to eliminate key bounce, pressing and releasing of keys is detected and delayed by 20ms. At the last block of code the hexadecimal value and ASCII value of pressed key are found from look-up tables that are defined at the beginning of the code. These values are assigned to the outputs. The assembly code can be found in Figure 3. ●

Figure 3: The project's assembly code

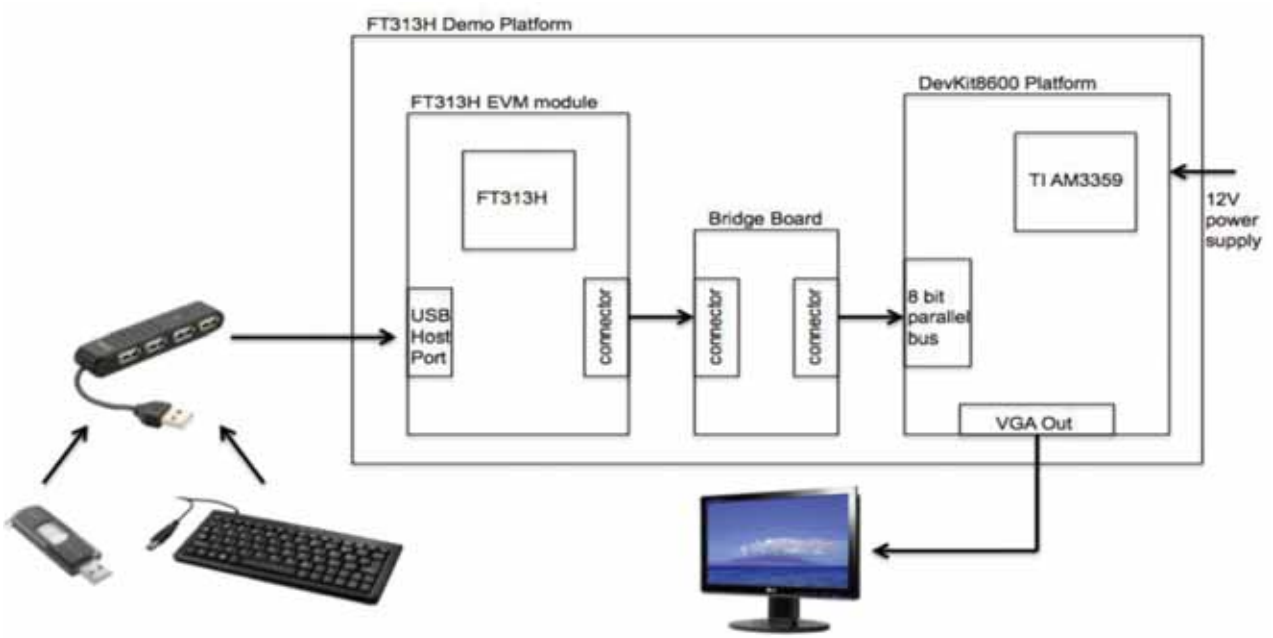
```
;-------------------------------------------------------------------
; This program provides a cheap and flexible hex (16 key)
; keypad encoder
;-------------------------------------------------------------------
        list    p=16F628A
        #include <p16F628A.inc>
        ERRORLEVEL 0,-302       ;suppress bank selection messages
        __CONFIG _CP_OFF & _DATA_CP_OFF & _LVP_OFF & _BODEN_OFF &
_MCLRE_OFF & _WDT_OFF & _PWRTE_ON & _INTRC_OSC_NOCLKOUT
;------------------ IC PIN ASSIGNMENT --------------------------------
                #define row1           PORTB,0     ;first row
                #define row2           PORTA,4     ;second        row
                #define row3           PORTB,3     ;third  row
                #define row4           PORTA,6     ;fourth row
                #define coll1          PORTB,7     ;first   column
                #define coll2          PORTB,6     ;second column
                #define coll3          PORTB,5     ;third column
                #define coll4          PORTB,4     ;fourth column
                #define outA           PORTA,0     ;Output A (LSB)
                #define outB           PORTA,1     ;Output B
                #define outC           PORTA,2     ;Output C
                #define outD           PORTA,3     ;Output D (MSB)
                #define d_valid        PORTA,7     ;Data Valid pin
;------------------ BAUD RATE ADJUSTMENT -----------------------------
baudrate        equ     d'103'          ; d'103' for Baud rate 2400
                                        ; d'207' for Baud rate 1200
                                        ; d'25' for Baud rate 9600
                                        ; d'12' for Baud rate 19200
;------------------ REGISTER ASSIGNMENT ------------------------------
cntr1           equ     0x20
cntr2           equ     0x21
key             equ     0x22
;-------------------------------------------------------------------
                org     0x0000
                goto    start
;-------------------------------------------------------------------
K_T_hex         addwf PCL,F             ; LOOK UP TABLE FOR PARALLEL OUTPUT
                retlw   0x00            ; row1 x coll1
                retlw   0x01            ; row1 x coll2
                retlw   0x02            ; row1 x coll3
                retlw   0x03            ; row1 x coll4
                retlw   0x04            ; row2 x coll1
                retlw   0x05            ; row2 x coll2
                retlw   0x06            ; row2 x coll3
                retlw   0x07            ; row2 x coll4
                retlw   0x08            ; row3 x coll1
                retlw   0x09            ; row3 x coll2
                retlw   0x0A            ; row3 x coll3
                retlw   0x0B            ; row3 x coll4
                retlw   0x0C            ; row4 x coll1
                retlw   0x0D            ; row4 x coll2
                retlw   0x0E            ; row4 x coll3
                retlw   0x0F            ; row4 x coll4
;-------------------------------------------------------------------
K_T_ascii       addwf PCL,F             ; LOOK UP TABLE FOR ASCII OUTPUT
                retlw   0x30            ; row1 x coll1
                retlw   0x31            ; row1 x coll2
                retlw   0x32            ; row1 x coll3
                retlw   0x33            ; row1 x coll4
                retlw   0x34            ; row2 x coll1
                retlw   0x35            ; row2 x coll2
                retlw   0x36            ; row2 x coll3
                retlw   0x37            ; row2 x coll4
                retlw   0x38            ; row3 x coll1
                retlw   0x39            ; row3 x coll2
                retlw   0x41            ; row3 x coll3
                retlw   0x42            ; row3 x coll4
                retlw   0x43            ; row4 x coll1
                retlw   0x44            ; row4 x coll2
                retlw   0x45            ; row4 x coll3
                retlw   0x46            ; row4 x coll4
;-------------------------------------------------------------------
start           movlw 0x07
                movwf CMCON
                call    init
loop            call    scankey
                goto    loop
;----------------key_scan subroutine ------------------------------------
scankey
test            bcf     row1
                bcf     row2
                bcf     row3
                bcf     row4
                btfss   coll1
                goto    test1
                btfss   coll2
                goto    test1
                btfss   coll3
                goto    test1
                btfss   coll4
                goto    test1
                goto    test
test1           call    Delay20
                btfss   coll1
                goto    scnkeys
                btfss   coll2
                goto    scnkeys
                btfss   coll3
                goto    scnkeys
                btfss   coll4
                goto    scnkeys
                goto    test
scnkeys         call    chk_key
test3           btfss   coll1
                goto    test2
                btfss   coll2
                goto    test2
                btfss   coll3
                goto    test2
                btfss   coll4
                goto    test2
```

```
                goto    testend
test2           call    Delay20
                goto    test3
testend bcf     d_valid
                return
;-------------- chk_key subroutine ------------------------
chk_key
                movlw 0x00
                bcf     row1
                bsf     row2
                bsf     row3
                bsf     row4
                btfsc   coll1
                goto    label1
                movlw 0x00
                goto    last
label1          btfsc   coll2
                goto    label2
                movlw 0x01
                goto    last
label2          btfsc   coll3
                goto    label3
                movlw 0x02
                goto    last
label3          btfsc   coll4
                goto    label4
                movlw 0x03
                goto    last
label4          bsf     row1
                bcf     row2
                btfsc   coll1
                goto    label5
                movlw 0x04
                goto    last
label5          btfsc   coll2
                goto    label6
                movlw 0x05
                goto    last
label6          btfsc   coll3
                goto    label7
                movlw 0x06
                goto    last
label7          btfsc   coll4
                goto    label8
                movlw 0x07
                goto    last
label8          bsf     row2
                bcf     row3
                btfsc   coll1
                goto    label9
                movlw 0x08
                goto    last
label9          btfsc   coll2
                goto    label10
                movlw 0x09
                goto    last
label10btfsc    coll3
                goto    label11
                movlw 0x0A
                goto    last
label11btfsc    coll4
                goto    label12
                movlw 0x0B
                goto    last
label12bsf      row3
                bcf     row4
                btfsc   coll1
                goto    label13
                movlw 0x0C
                goto    last
label13btfsc    coll2
                goto    label14
                movlw 0x0D
                goto    last
label14btfsc    coll3
                goto    label15
                movlw 0x0E
                goto    last
label15btfsc    coll4
                goto    last
                movlw 0x0F
last            movwf key
        call K_T_ascii
                movwf key_ascii
                call    out
                return
;-------------- OUT subroutine ----------------------
out
                btfsc   key,0
                bsf     outA
                btfss   key,0
                bcf     outA
                btfsc   key,1
                bsf     outB
                btfss   key,1
                bcf     outB
                btfsc   key,2
                bsf     outC
                btfss   key,2
                bcf     outC
                btfsc   key,3
                bsf     outD
                btfss   key,3
                bcf     outD
                bsf     d_valid
                movf    key_ascii,w
                movwf TXREG
                bsf     STATUS,5
control btfss   TXSTA,TRMT
                goto    control
                bcf     STATUS,5
                return
;-------------- 20 mS Delay subroutine ----------------
Delay20                         ;20ms time delay
                movlw d'66'
                movwf cntr1
B1              movlw d'100'
                movwf cntr2
B2              decfsz  cntr2,f
                goto    B2
                decfsz  cntr1,f
                goto    B1
                retlw   0x00
;-------------- Initialization subroutine ----------------
init
                bsf     STATUS,5
                bcf     row1            ;row1 output
                bcf     row2            ;row2 output
                bcf     row3            ;row3 output
                bcf     row4            ;row4 output
                bsf     coll1           ;coll1 input
                bsf     coll2           ;coll2 input
                bsf     coll3           ;coll3 input
                bsf     coll4           ;coll4 input
                bcf     outA            ;outA output
                bcf     outB            ;outB output
                bcf     outC            ;outC output
                bcf     outD            ;outD output
                bcf     d_valid         ;data valid output
                bsf     TRISB,2         ;serial com.
                bsf     TRISB,1         ;serial com.
                bcf     OPTION_REG,7
                movlw baudrate
                movwf SPBRG
                movlw b'00100100'
                movwf TXSTA
                bcf     STATUS,5
                bsf     RCSTA,7
                clrf    PORTA
                clrf    key
                return

              Program end here ----------------------
                end
```

Figure 3: The project's assembly code (starts on previous page)

Figure 1: Functional block diagram of USB-based video processing circuit



REAL-TIME PROCESSING OF VIDEO CONTENT FROM A USB MASS STORAGE DEVICE VIA LINUX

CHANG YANG AND **LEE CHEE EE** FROM FTDI CHIP DISCUSS A SIMPLE CIRCUIT THAT CAN BE EASILY INTEGRATED INTO ANY SYSTEM DESIGN TO INTRODUCE USB FUNCTIONALITY

There is a growing demand for USB host functionality to feature in non-PC hardware. This is true of portable consumer products such as smartphones, but also it is becoming more commonplace in home entertainment products such as set top boxes and game consoles.

A Simple Circuit for Processing Video for Viewing

The following simple-to-implement circuit demonstrates how stored video content that has been placed onto a USB Flash drive can be processed ready for viewing on a monitor. It also details how the difficulties of adding USB driver support to Linux-based systems can be accomplished so that different USB peripherals can be connected to embedded USB hosts with minimal amount of engineering effort.

Figure 1 shows the basic construction of the video processing circuit. The hardware required for it consists of:

- 1 x Texas Instruments's AM3359-based DevKit8600 platform;
- 1 x VGA 8000 adaptor;
- 1 x bridge board;
- 1 x FTDI's FT313H EVM module;
- 12V power supply;
- 1 x 4-port hi-speed USB hub;
- 1 x USB keyboard;
- 1 x high-speed USB Flash drive (with media player application plus quick launch script copied to its root folder).

The AM3359 500MHz microprocessor has an ARM Cortex-A8 32-bit RISC core and is highly suited to modern multimedia applications. Normally microcontrollers and microprocessors need to have USB drivers written especially for them, if they are to be used in the type of application described here, so that they can operate with connected USB devices. This causes unwanted technical issues, particularly for engineers who are not experienced in such matters, and is likely to extend the development time.

However, the FT313H host controller, which is designed for integrating with Linux-based processors, can access the native USB host stack contained within the AM3359. The device handles the USB protocol, scheduling data and so on, allowing the processing power of the AM3359 to be focused on the fundamental tasks. As split transfers are supported, the host controller IC can deal with USB data coming from both the keyboard and the Flash drive through the hub, with support for the HID class and mass storage class included. The mass storage class enables bulk mode transfers to be executed, which is vital as

video applications need fast transfer rates that can keep up.

The Flash drive in this example circuit, through its connection to the FT313H, is able to transfer data to the AM3359 chip for processing to be carried out. This data is then output to monitor by the AM3359. By incorporating a high-speed USB host controller IC into the circuit, the microcontroller/microprocessor gains access to USB peripherals it would not otherwise be able to. As the system is Linux based, all the native USB class drivers are already available, thus there is no need to develop HID or hub class drivers. DMA transfers help further to expedite the movement of data by limiting the number of instructions needed to fetch data from the bus.

Circuit Set-Up

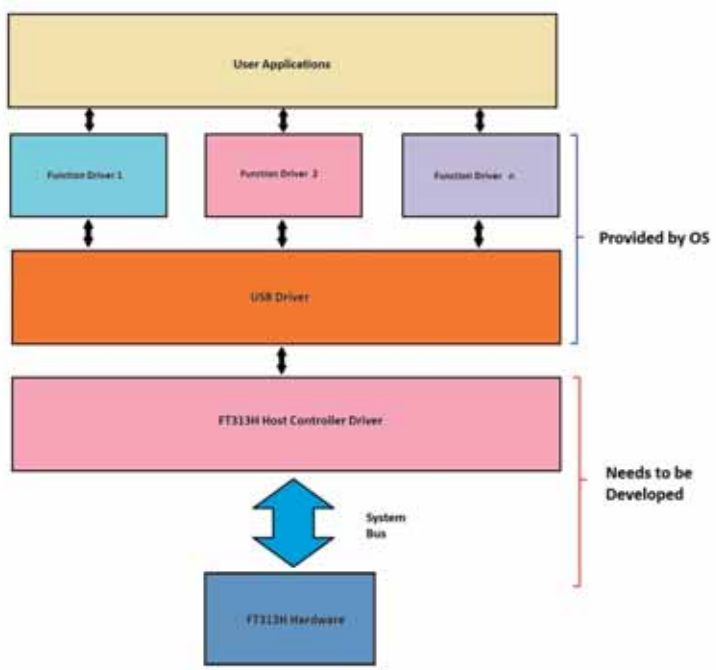
The set-up of the circuit is as follows. With the 12V power supply unconnected, insert the USB hub into EVM module's downstream port, then insert both keyboard and the Flash drive into the USB ports found on the hub. Next, connect the monitor to the VGA port and turn the monitor on. Wait until the login screen shows on the monitor, then using the USB keyboard input the word 'root' (all in lower case) and hit the enter key to login to embedded Linux. Via the keyboard you should next issue the 'cd /media/sda1' command, but be sure to add a space after 'cd'. Finally use the keyboard to issue the './play demo.avi' command to start playing. To stop playing, simply power down the 12V supply.

Integration of a USB 2.0 high-speed compliant host controller needs to consider both hardware and software elements. Outlined in Figure 2 is a breakdown of the system architecture. The USB host software stack normally contains the following layers. From the lowest layer to the highest layer are: the host controller driver (HCD) layer, the USB driver (USBD) layer, USB function driver layer and user applications layer respectively. The HCD is hardware specific. It will directly control the USB host controller

FT313H LINUX USB HOST CONTROLLER

The FT313H Linux USB host controller is designed to be simple to incorporate in circuit designs, as it effectively sits on the system processor bus. Furthermore, because of its strong performance characteristics, it proves to be highly optimised for file transfer applications where there are large quantities of data involved. This 480Mbit/s USB 2.0-compliant IC adds high-speed USB host connectivity capability into system implementations, enabling fast rates of data transfers for interfacing with mass storage devices, in addition to connection with wireless dongles and modular system expansion, through its support of standard USB class drivers. Board level interconnects include a general purpose 8 or 16-bit bus, NOR, or SRAM interface. Its battery charge detection functionality means that as well as mains powered applications such as this, it can also be applied to battery-powered portable applications, allowing control of supply currents to external hardware for operation/charging modes.

Figure 2: Schematic showing USB host software architecture



hardware through platform-dependant system bus. The USBD is a software module which completes the general USB operations, such as USB enumeration, and provides interfacing capacity for function drivers. The function driver is used to serve a specific USB peripheral or class of peripherals, such mass storage devices or printers. User applications provide direct interaction with the end users and enable the utilisation of services provided by the function drivers.

In general, the USBD and function drivers are provided as part of the operating system (OS) such as Linux. However, both the HCD and the platform-dependant system bus access part must be developed separately. As for user applications, both off-the-shelf general applications, such as file manager and USB peripheral specific applications are possible. Of course, the latter ones must be specially developed.

Configuring the System

The host system needs a memory interface to access the AM3359 microprocessor. This is done via the built-in general-purpose memory controller (GPMC) module. For the software part, an embedded Linux OS can be loaded; in this particular case kernel version 3.1.0 has been specified. Here it is critical to select the software modules that will be required. For our example, the necessary USB functionality is provided by the OS and incorporated into the software platform builder. Once the OS kernel build has been completed, the host software integration work consists of two parts. These are:

- The adding of the USB host controller IC as a peripheral for AM3359 through the GPMC;
- The development of the USB host controller's HCD platform driver.

For this embedded system, there are no standard peripheral buses, like PCI or PCI-Express, incorporated into the PC

platform. As a result, all the peripherals behave from a software perspective as if they are directly attached to the central processing unit (CPU). Low-level software – board files to be precise – must be modified when a new peripheral is added, to include the support of that new peripheral. Actual processes including configure pin muxing of the external peripherals, configuration of the access timing for the new peripheral and allocating the necessary resources for the peripheral must all be undertaken.

In order to add FT313H support to the module the user needs to initiate embedded Linux "MACHINE_START" macro, as shown in code segment below:

```
MACHINE_START(AM335XEVM, "am335xevm")
 /* Maintainer: Texas Instruments */
 .atag_offset = 0x100,
 .map_io = am335x_evm_map_io,
 .init_irq = ti816x_init_irq,
 .init_early = am335x_init_early,
 .timer = &omap3_am33xx_timer,
 .init_machine = am335x_evm_init,
MACHINE_END
```

The peripheral initialisation function is controlled by "init_machine" member with value "am335x_evm_init". This function will be executed when the development board boots up. It uses a table-driving method to include the initialisation function for each peripheral, thus it is possible to add the initialisation part into the module's configuration table by adding a new record as following code segment:

```
#ifdef CONFIG_USB_FT313H_HCD
 {ft313_hc_init, DEV_ON_BASEBOARD, PROFILE_0},
#else
 {gpio_keys_init, DEV_ON_BASEBOARD, PROFILE_0},
//Removed because GPMC CS1 conflict with FT313
#endif
```

While "ft313_hc_init" is the function through which the actual initialisation sequence is execute, and the first task it will do is to configure pin muxing for the USB host controller, this is done by calling system pin muxing function using a table defining as follows:

```
static struct pinmux_config ft313_pin_mux[] = {
 {"gpmc_a0.gpmc_a0", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a1.gpmc_a1", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a2.gpmc_a2", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a3.gpmc_a3", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a4.gpmc_a4", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a5.gpmc_a5", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a6.gpmc_a6", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},
 {"gpmc_a7.gpmc_a7", OMAP_MUX_MODE0 |
AM33XX_PIN_OUTPUT_PULLUP},

 {"gpmc_csn1.gpmc_csn1", OMAP_MUX_MODE0 |
AM33XX_PULL_DISA}, // CS
 {"gpmc_ben1.gpmc_ben1", OMAP_MUX_MODE7 |
AM33XX_PIN_INPUT_PULLUP}, // Interrupt

 {NULL, 0},
};
```

Then it will communicate with the GPMC driver to get the memory mapping for the FT313H, as well as its interrupt request number (IRN). This information will in turn be used for building recourse data structure for platform devices. It will also configure the allocated GPMC timing information so it can be matched with the host controller's timing requirements.

When function "ft313_hc_init" is returned successfully, it means that connection to EVM module is configured nicely and FT313H required resource is allocated appropriately. The USB host controller HCD is ready to load.

The HCD contains two parts, one is the platform driver and the other is the general HCD which is effectively the complete HCD function. The latter part is platform independent. The platform driver will make use of the platform device to determine the resource being allocated to the USB host controller and platform independent part of HCD will use this information to access the controller's hardware and complete the requests from the upper layer. If this IC needs to port to another embedded hardware platform, the procedure related to the platform device generation must be re-implemented based on the target platform in question. However, the HCD could be reused.

Easy Addition of USB Functionality

Despite the need for transferring greater quantities of data, the market is still underserved by high-speed host solutions. The circuit discussed here demonstrates the ability of the FT313H, when it is integrated together with a microprocessor/microcontroller unit, to add USB functionality to a system design. It shows the operational benefits of including a USB Linux host IC into Linux-based system designs, so that the system microcontroller/microprocessor can benefit from the native driver support. This means that development can be achieved in a straight-forward manner, with the driver development obstacles averted. ●

DEMO PLATFORM

The demo platform featured in this circuit (into which the DevKit8600 platform, VGA adaptor, bridge board and EVM module can plugged) is commercially available under the product number UMFT313EV. It allows easy integration into embedded designs for system prototyping and validation.

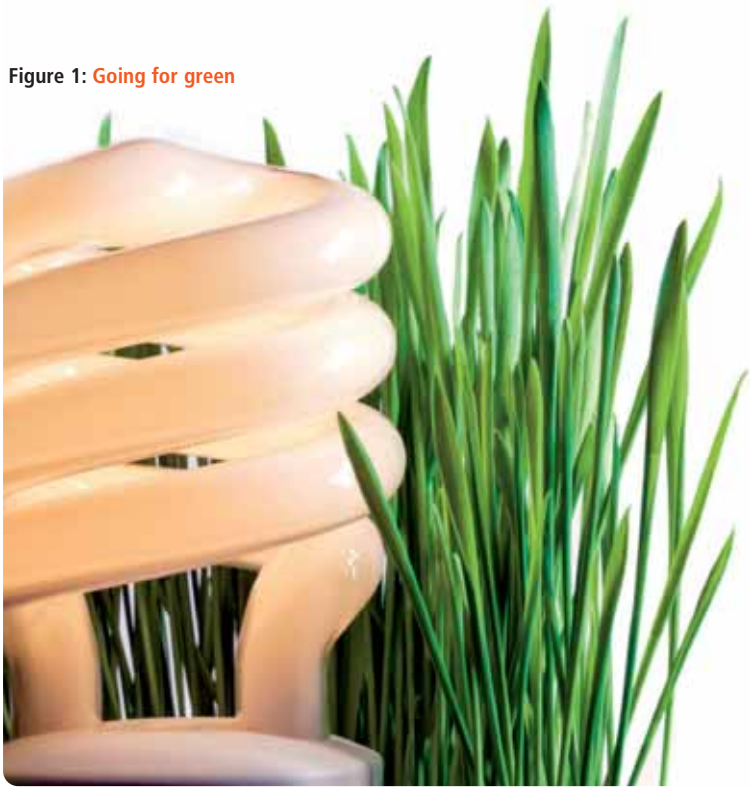


Figure 1: Going for green

REGULATORY COMPLIANCE IS KEY TO THE ELECTRICAL AND ELECTRONICS (E&E) INDUSTRY AND THERE ARE SOME VERY IMPORTANT REGULATIONS TO ADDRESS. BY **XAVIER VITAL**, ECODESIGN DEPARTMENT MANAGER, AND **NICOLE EFFENBERGER**, DIRECTOR OF CLIENT SERVICES AT SGS, A TEST, VERIFICATION AND CERTIFICATION COMPANY

FOUR KEY ELEMENTS OF SUSTAINABILITY IN THE ELECTRICAL AND ELECTRONICS INDUSTRY

Waste of Electrical and Electronic Equipment Directive (WEEE2) governs how Electrical and Electronics equipment (EEE) in Europe is handled at the end of its use. The WEEE directive has been revised and the new version will be adopted by EU member states on or before January 2015.

The member states' WEEE collection rates currently are based on four kilograms of WEEE per inhabitant per year from private households, and these collection rates will continue to apply through to 2015. Beginning in 2016, the collection rates will be based on the total weight of all EEE placed on the market in each member state. From 2016 through to 2018, each member state will establish minimum annual collection rates, which will be at least 45% of the average weight of all EEE put on the market during the three preceding years in that member state.

WEEE2 will have a major impact on manufacturers and importers, and will require them to:

- Organize and finance the collection and recycling of the electrical/electronic waste.
- Inform waste management facilities of the appropriate re-use and treatment information for the products it places on the market.
- Label their product with the appropriate markings.
- Implement ecodesign in order to facilitate product reuse and reduce recycling costs.

RoHS, REACH and Prop 65

As global chemical requirements such as RoHS, REACH and California Prop 65 evolve and become more complicated, electronics companies are developing smart compliance strategies that are cost-effective and prevent unnecessary testing of materials and components. In particular the RoHS Directive has been recently revised; Directive 2002/95/EC has been replaced by Directive 2011/65/EU, or RoHS II, as of January 2, 2013, and some revisions will be phased in over six years. Examples of major changes in the new directive include:

- RoHS is now a CE Marking Directive.

- Expanded product scope: now included are medical devices, monitoring and control equipment and other electrical and electronic equipment not covered by any of the other 10 categories.
- Maximum validity period of exemptions for categories 1-7, 10 and 11 is up to five years, and maximum validity period of exemptions for categories 8 and 9 is up to seven years.
- New obligations for importers, manufacturers and distributors.
- Manufacturers or their authorized representative must submit technical documentation (to show compliance) upon request by a member state enforcement agency, and retain such documentation for 10 years after a covered product is placed on the market.

One of the key changes here is the more stringent requirement for traceability of compliance documentation and retention of that data. The difficulty is that the RoHS directive requires this information for each homogenous material present in the product. This requires a deep understanding and monitoring of the materials and chemicals being used throughout the supply chain.

Smart compliance strategies include:

- Utilizing software to manage information from suppliers.
- Continuous supplier training programs.
- Conducting risk assessments on suppliers and materials and testing where necessary.
- Implementation of a data monitoring program.
- Implementation of a supplier monitoring program.

> The first challenge is usually to understand all the environmental impacts generated by a product over its life

Energy Related Products Directive (ErP)

The ErP Directive essentially helps develop performance requirements for energy-consuming products. It replaces the Energy Using Products (EuP) Directive by expanding the scope to also include products which have an impact on energy consumption during their use. The purpose of this European Directive is to decrease environmental impact with the longer term aim of benefiting both businesses and consumers with better, more efficient products. The ErP takes a staged approach and, over the coming months, a number of products will be required to meet the new requirements for the first time. Requirements are specific to the product groups and usually include:

- Minimum energy efficiency and energy management requirements;
- Product information requirements;
- Technical documentation filings that may be required for control in the context of the CE marking.

Ecodesign – Connecting Environmental Experts with Designers

Some 90% of the corporate carbon footprint of a manufacturer/retailer is embedded in its product's life-cycle. Reducing the global impacts of industry requires implementing ecodesign practices. Ecodesign, which is guided by ISO 14062, is a systematic process that incorporates significant environmental aspects of a product, as well as stakeholder requirements into product design and development.

The first challenge is usually to understand all the environmental impacts generated by a product over its life cycle, from the extraction of the raw material, manufacturing, distribution, use and ultimately disposal or recycling.

The Life Cycle Assessment (LCA) is one of the tools that can be used to support the ecodesign process by providing a global and multi-criteria evaluation of the product's life-cycle. However, LCA requires expertise and may not be the ideal tool to provide to designers or buyers.

Figure 2: Recyclability is addressed in the new IEC/TR 62635 standard

Qualitative checklists can be developed to make the ecodesign process easy for design teams and to stimulate innovation. These ecodesign decision making tools are based on the results of an LCA and on a technical benchmark comparing the environmental performance of competitors' products.

Recyclability – New IEC/TR 62635 Standard

IEC/TR 62635:2012 provides a methodology for information exchange involving EEE (Electrical, Electronic, and Electromechanical) manufacturers and recyclers. It also provides guidance for calculating the recyclability and recoverability rates to provide information to recyclers, evaluate the recyclability and recoverability rates reflecting real end-of-life practices and provide designers with recommendations to implement ecodesign for recycling practices. End-of-life information is an important aspect of ecodesign and environmental risk management.

Supplier Sustainability Involvement Programs

With the rise of outsourced manufacturing to developing

countries, establishment of supplier audit programs is important for assessing the environmental, social and cost performance of suppliers. The Global Social Compliance Program (GSCP) is a business-driven program for the continuous improvement of working and environmental conditions in global supply chains. The GSCP was created by and for global buying companies wanting to work collaboratively on improving the sustainability (social and environmental) of their often shared supply base. To this end, these companies are working on harmonizing existing efforts to deliver a shared, global and sustainable approach based on consensus and best existing practices.

Considering the expansion of outsourced manufacturing to developing countries and the complexity of supply chains, the industry is facing the challenge of increasing the visibility of the environmental and social situation of suppliers to drive continuous improvement. The GSCP guidelines can be used as the starting point to build a sustainable supplier program, allowing companies to:

- Verify the compliance of factories with local regulations.
- Address major environmental concerns such as energy, water, waste, hazardous chemicals, etc.
- Identify potential for improvement and cost reduction.
- Measure risk.
- Increase the awareness of factories and establish an action plan to drive a continuous improvement process.

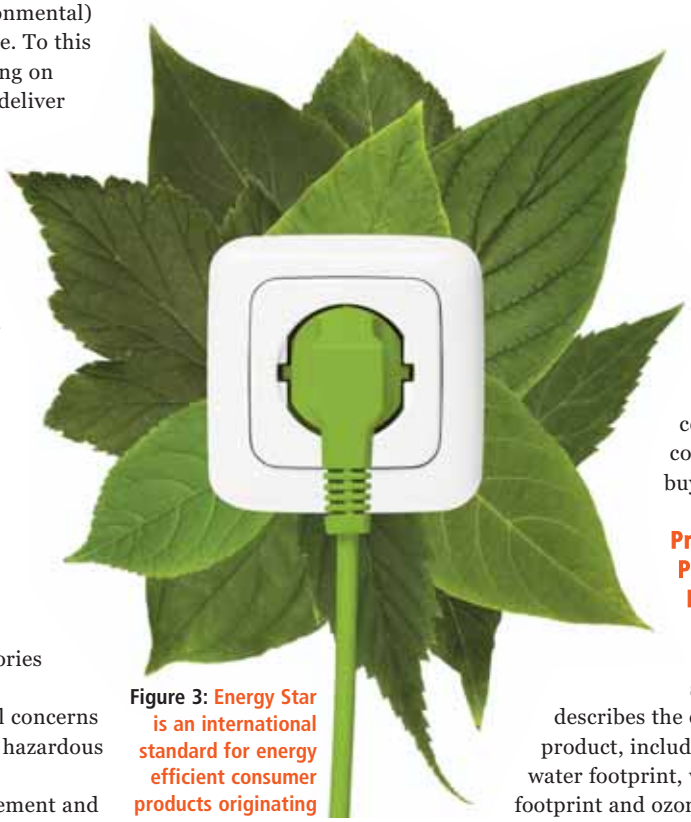


Figure 3: Energy Star is an international standard for energy efficient consumer products originating in the US

Communicating Environmental Features

Market requirements usually exceed other requirements in terms of energy efficiency of electrical and electronic equipment. Energy Star is an international standard for energy efficient consumer products originating in the US. Initiated as a voluntary labelling program designed to identify and promote energy efficient products, Energy Star began with labels for computer and printer products. Over 20 years the scope of the program has been significantly extended, covering various household and professional equipment and even buildings.

Energy Star can be considered a strong market presence, with major retailers or buyers requiring products to be certified. The race has begun: manufacturers are now going beyond the ErP and Energy Star requirements to differentiate their products from those of competitors.

Environmental EPEAT Registry

EPEAT, which stands for Electronic Product Environmental Assessment Tool, is an easy-to-use, on-line tool helping institutional purchasers select and compare computer desktops, laptops and monitors based on their environmental attributes. In February 2013, EPEAT announced its expansion beyond PCs and displays to include printers, copiers and other imaging equipment. To be added to the EPEAT registry, an imaging device must meet at least 33 required environmental performance criteria. Products may achieve higher ratings by meeting up to 26 additional optional criteria. The program, initiated in the US, is progressively being recognized worldwide. Being EPEAT registered can provide a significant competitive advantage for companies selling to public buyers.

Product Environmental Profile – PEP Ecopassport Program

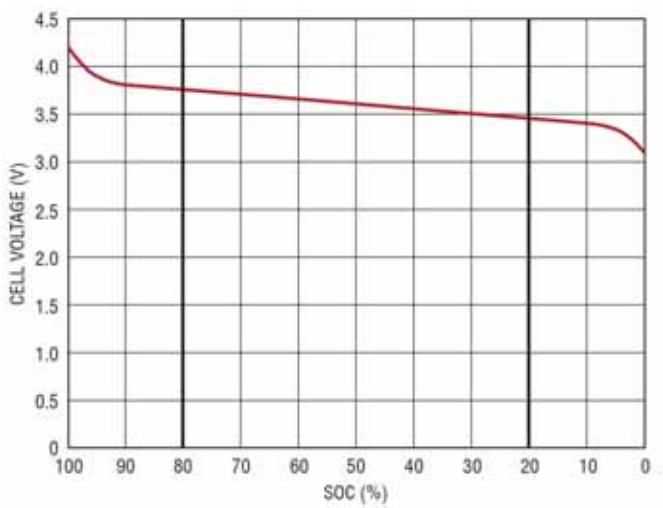
Environmental Product Declaration, or EPD, is a standardized document that describes the environmental impacts of a product, including raw material depletion, water footprint, water toxicity, carbon footprint and ozone layer depletion, as well as other relevant environmental information such as the product's recycling potential or energy consumption. The impact categories are based on LCA. EPDs are primarily intended for use in business-to-business communication. Among various existing EPD programs, the PEP Ecopassport Program is probably the fastest growing. Since its initiation at the end of 2011, the PEP Ecopassport Program has registered more than 1,000 environmental declarations for electrical, electronic, HVAC and refrigeration products.

Companies developing PEPs have recently reported how they were able to save time and money (more than the cost of the creation of the PEPs) by using the information provided in the PEPs. These companies have to submit bids to supply electrical equipment to organizations that have put out a Request For Proposal (RFP). In these RFPs companies are usually asked for information on the environmental impacts of their products. Developing PEPs enables companies to easily respond to these requests, and sales departments have also reported that they believe having PEPs results in greater success in the bidding process. ●

BATTERY MANAGEMENT

GREG ZIMMER, SENIOR PRODUCT MARKETING ENGINEER FOR SIGNAL CONDITIONING PRODUCTS AT LINEAR TECHNOLOGY, EXPLAINS HOW TO ADD REAL VALUE TO BATTERY MANAGEMENT THROUGH PRECISION CELL MEASUREMENTS

Figure 1: Simplified battery discharge curve



The current generation of electric vehicles relies on lithium battery packs with an energy range between 16kWh and 53kWh. A single gallon of fuel contains more than 36kWh of energy. For an electric or hybrid electric vehicle (HEV), or any high power battery system, to compete with an internal combustion engine (ICE) requires squeezing every bit of energy out of the batteries. To accomplish this, each individual cell within the pack has to be carefully monitored and controlled.

High-power battery packs consist of a long string of series-connected cells. Directly connected to each cell is a battery monitor IC, responsible for accurately measuring each cell's voltage. This is not a simple task, as the cells are positioned at various points along a very high voltage string that is subject to horrendous electrical spikes and electromagnetic interference (EMI). A battery management system (BMS) combines the cell voltage with current, temperature and operating history, to continuously assess each cell's condition. It's a tough challenge, but with accurate monitoring and control, the driving range, reliability and safety of the battery pack can be maximized.

Long Lifecycle

Batteries in an HEV or EV are expected to last 10 to 15 years, and they are considered to be at their end-of-life when they have lost 80% of their original capacity. Battery lifetime and reliability are maximized by restricting the operating state of charge by not allowing them to be fully charged or discharged.

A typical battery pack is operated in a restricted range, such as 20% SOC to 80% state-of-charge (SOC). These SOC limits could be adjusted with age and operating conditions, such as high temperature environments. As a result of the limits, battery packs are not utilized to their full capacity. For example, operating a pack with 20% SOC to 80% SOC limits the usable SOC range to 60%. The challenge for the BMS is to operate each cell as close to the limits as possible, without exceeding them. Amplifying the challenge, lithium batteries exhibit a flat discharge curve over their operating range. As a result, there is a very small change in cell voltage over the operating range and the battery monitor must make very accurate measurements as part of the SOC calculation.

To illustrate the importance of cell measurement accuracy, consider the simplified lithium battery discharge curve shown in Figure 1. This curve has a constant 5mV/% (SOC) slope across the operating region. A battery pack operating within a 20% to 80% SOC range and a similar discharge characteristic will face a big penalty for poor cell voltage measurement accuracy.

As shown in Figure 2, if the battery monitor has a cell voltage measurement error of ±10mV, a measured cell voltage of 3.75V could actually correspond to a real cell voltage between 3.74V and 3.76V. This corresponds to an actual SOC range from 76% to 80%. As a result of this measurement inaccuracy, the operating range must be restricted by a 'guard band' to ensure that the operating limits are not exceeded. In this example, the operating range must be restricted to the measured range of 22% to 78% instead of 20% to 80%. If the pack is expected to maintain the same range, a BMS with this accuracy will require additional battery capacity to compensate for the guard-band restrictions. Considering the 60% usable SOC, the battery must be oversized by > 7% to compensate for cell measurement inaccuracy of ±10mV. For an HEV using a 5kWh pack costing $3000 ($600/kWh), this translates to additional $214.

> To compete with an internal combustion engine (ICE) requires squeezing every bit of energy out of the batteries

This argument can be extended to highlight the "guard-band penalty" for various cell measurement errors and its dependence on the SOC range. As shown in Figure 3, a system with only 1mV of measurement error requires less than 1%

oversizing, even when the pack is restricted to an SOC range of 25% to 75% (50% usable SOC).

Cell Balancing

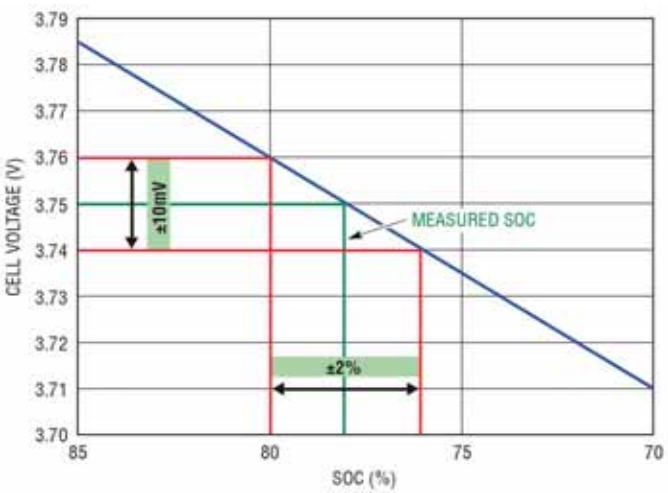
Although most lithium cells are generally well matched when first acquired, the SOCs of a long string of cells will diverge over time and charge cycling. This is due to small variations in cell characteristics and localized operating conditions, which can lead to small differences in self-discharge and load current. To avoid operating any cell beyond its SOC range, as the SOCs diverge, the total operating range will be slowly constricted by the most unbalanced cells. To address this, nearly all battery management systems include cell balancing.

With passive balancing, cells with higher SOC are discharged to normalize the SOC for all cells – a low cost, simple balancing method. However, it has significant limitations: it only operates by removing charge. It wastes energy, as a function of the amount of imbalance, and it generates significant heat. This means that the balancing current must be kept relatively small, typically 5% or less of the cell capacity. As a result, passive balancing is primarily limited to operation offline and it requires significant time to complete. Passive balancing becomes less effective as the variations in SOC increase and, over time, SOC variation will increase due to diverging cell capacity.

Cells lose capacity as they age, a process that can differ from cell to cell due to a number of factors, such as gradients in pack temperature and variations in cell manufacturing. With differences in capacity, cells will more readily become imbalanced. Allowing just one cell to operate beyond the SOC limit will simply exacerbate this problem by premature cell aging.

Relying solely on passive balancing becomes increasingly difficult, as capacities diverge. To address the limitations of passive balancing, new battery management systems are implementing active balancing, with which charge is moved between cells, rather than being dissipated with passive balancing. Active balancing can operate both during the charge and discharge cycles. When charging the pack, the active balancer can move charge from the weaker cell to the stronger cell. When discharging the pack, charge can be moved from the stronger cell to compensate the weaker cell. Instead of wasting energy, charge is transferred through a highly efficient circuit, such as a flyback converter. As a result, heat generation is limited, the balancing current is higher and the balancing time is significantly reduced. This allows for active balancing while the pack is in use, where it can ensure extraction of the maximum energy from each individual cell. New ICs, such as

Figure 2: Guard-band requirements for ±10mV cell measurement error



Linear Technology's LTC3300 and LT8584, are enabling active balancing in automotive battery packs.

Ideally, active balancing should be enabled as the cells reach the ends of the SOC range. To illustrate, consider a pack containing many cells with uniform capacity and one "weak" lower capacity cell. If all cells are charged to 80% SOC and then discharged, the SOC of the weak cell will slowly diverge from the rest of the cells. The BMS must determine a suitable point to enable the balancer to keep the weak cell operational, while the other cells are continuing to discharge. Figure 4 shows the SOC divergence during the discharge cycle, for two examples; one with a cell that has a capacity difference of 2% from the rest of the pack, and another that differs by 8%.

The BMS cell measurement error sets a limit for determining the relative condition between cells. With a ±2% SOC measurement error (±10mV), cells could be out-of-balance from each other by as much as 4% before the cell measurements would reliably detect the situation. Enabling an active balancer at a well-defined point along this discharge curve would be virtually impossible without cell measurement accuracy much, much better than ±10mV.

Measurement Accuracy

The implication for measurement accuracy is not limited to active balancing. From this example, a 4% SOC difference translates to a capacity variation of more than 6.6%. For an automotive battery that reaches its end of life after 20% reduction, this is significant unrecovered capacity. More importantly, a change in cell capacity is a key indicator of its health, and an unrecognized capacity change could be a serious issue.

The importance of cell measurement accuracy becomes clearer when considering the complications beyond this simple example. For example, most packs will have a continuum of capacity variation, with more subtle and harder to detect SOC divergences. Also, cells will not likely be aligned at 80% SOC

Figure 3: Dependence of the guard band on cell measurement error

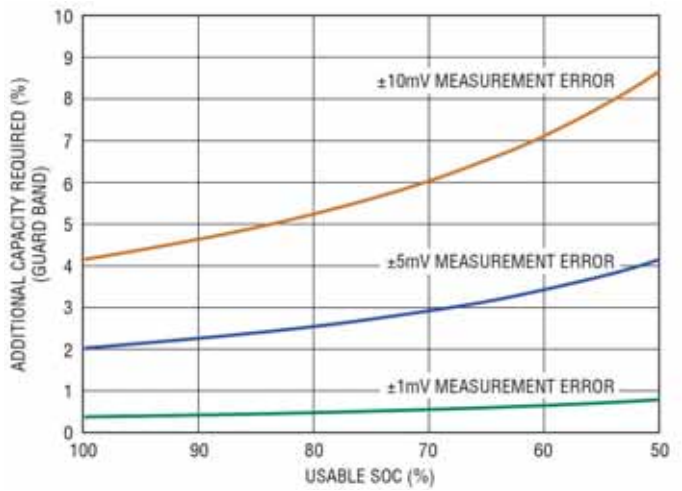
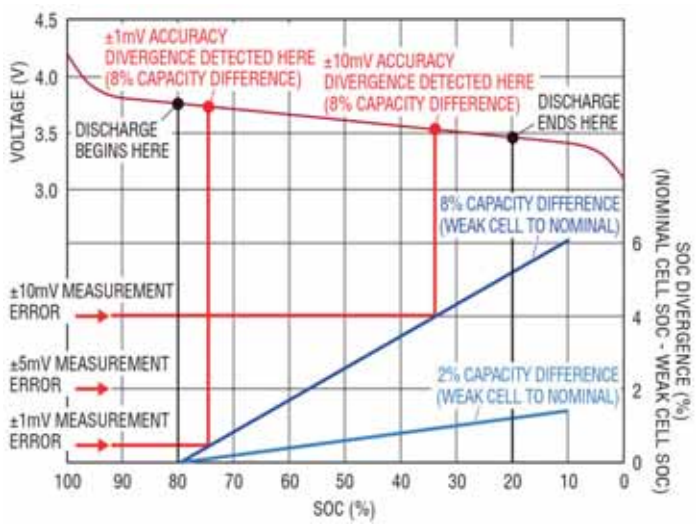


Figure 4: Detecting cell capacity differences depend on measurement accuracy



when discharging begins, possibly further masking capacity variation. It's also important to note that multiple parameters are required for an SOC calculation. Measurement inaccuracy of these other parameters does not lessen the need for accurate cell-voltage measurements. To the contrary, compromising on cell voltage accuracy will likely widen the distribution of battery life.

The voltage reference within the battery monitor is the primary determinant of measurement error. Any change in the voltage reference directly degrades the cell measurement accuracy. The current generation of battery monitors relies on bandgap voltage references. In theory, bandgap references are ideal for integration into complex integrated circuits, such as a battery stack monitor, because they require little die space, low power and low overhead voltage. However, bandgap references are sensitive to mechanical stress, IR reflow and humidity, resulting in thermal hysteresis and long-term drift. For precision instrumentation that is required to maintain very high accuracy for more than 15 years, there is a better choice. The newest battery monitors, such as Linear Technology's LTC6804, incorporate a sub-surface Zener voltage reference. Sub-surface Zener voltage references provide outstanding long term stability and accuracy over time and operating conditions. Using this approach, the LTC6804 is able to guarantee a total cell voltage measurement error of less than 1.2mV.

> Allowing just one cell to operate beyond the SOC limit will simply exacerbate the cell imbalancing problem by premature cell aging

Cell Management

The accuracy of the battery monitor is not limited to the accuracy of the measurement itself. Cell measurements need to be considered in the context of the automobile, where there is significant electrical noise and transients from inverters, actuators, switches, relays, etc. This noise is embedded within the cell signal and, if accuracy is important, it has to be removed.

A modest level of noise reduction can be achieved by placing an RC filter on each cell; using a higher-order filter circuit on each cell is impractical, due to cost and board space limitations. A modest amount of noise can be removed by processing many samples from each signal measurement; given the large number of cells, the massive data to be transmitted to a central processor makes this impractical, as well. A practical and effective solution is to remove noise within the battery monitor. As an example, Linear Technology's LTC6804 uses delta-sigma ADCs with built-in third order noise filtering. This is in contrast to a wideband SAR ADC, where fast acquisition has limited value for a signal corrupted by noise. To optimize speed and noise reduction, the LTC6804 delta sigma ADCs can operate with different corner frequencies, ranging from 26Hz to 27kHz. For the automotive environment, the delta sigma approach is quite effective.

As high powered battery systems continue to advance into the mainstream, demands on the battery monitoring electronics will not relent.

To achieve the driving range, reliability and safety demanded of electric vehicles, requires careful consideration of every small source of lost performance. To extract every bit of usable energy requires implementing cutting edge technologies, such as active balancing. It also requires the most accurate and stable cell voltage measurement possible. ●

High Voltage Power Supplies

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YANHUA LIU AND **ZONGSHEN LAI** FROM THE INSTITUTE THE EAST CHINA UNIVERSITY IN SHANGHAI, PROPOSE A TELEVISION CHANNEL RECEIVERS WITH DIGITAL AUTOMATIC

Low-Cost Testing of Mixed-Signal SoCs

With recent strides in integrated circuit (IC) technology, system-on-chip (SoC) devices are adopted everywhere. A typical mixed-signal system contains a microprocessor, embedded memory, analog module and other functional modules. With such complexity on board, these devices need a large number of testing resources, including digital, analog and radio frequency (RF) channels.

In the semiconductor industry, the common testing system for mixed-signal SoCs is mixed-signal ATE or RF ATE (which includes an RF signal generator and measurement). However, such systems are very expensive and increase the testing costs considerably. Some research shows that using RF ATE, test cost accounts for up to 30% of the total cost, therefore, using low-cost ATE would be preferable, if a comparable testing ability could be achieved.

Figure 1: The working principle of DVB-S

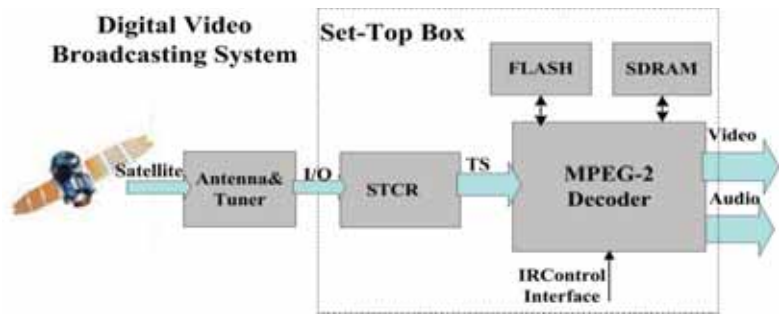
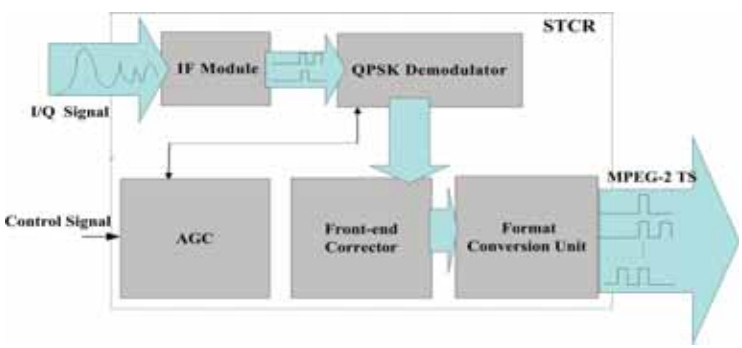


Figure 2: Block diagram of an STCR



Satellite Television Channel Receiver

One typical mixed-signal SoC is the satellite television channel receiver (STCR) – key part of a set-top box. Its main function is to receive intermediate frequency (IF) signals and demodulate them.

Testing STCRs requires RF ATE in conventional testing methodology as digital and mixed-signal ATE cannot generate IF signals and is expensive. In this article we propose a much cheaper functional test solution for STCR using a low-cost digital ATE – the Advantest T6575.

> *The GSCP was created by and for global buying companies wanting to work collaboratively on improving the sustainability (social and environmental) of their often shared supply base*

Figure 1 shows the working principle of a satellite digital video broadcasting system (DVB-S). The satellite signal is received by the receiver antenna, and is then amplified, down-converted and filtered. Following that, the signal is converted into an In-phase/Quadrature (I/Q) signal, which is then demodulated and decoded by the STCR, with a frequency between 1MHz and 38MHz (IF signal).

The output signal of the STCR is MPEG-2 transport stream (TS) – a standard digital stream which contains video and audio information. The MPEG-2 TS is decoded by an MPEG-2 decoder and converted into video and audio for television.

In a set-top box, STCR is a core chip that receives the I/Q signal. Figure 2 shows the STCR's structure. It includes an IF module, quadrature phase shift keying (QPSK) demodulator, automatic gain control (AGC), front-end corrector and format conversion unit. The I/Q signal is received and converted into a

OF MICROELECTRONICS CIRCUITS & SYSTEMS FROM LOW-COST TESTING METHODOLOGY FOR SATELLITE TEST EQUIPMENT (ATE)

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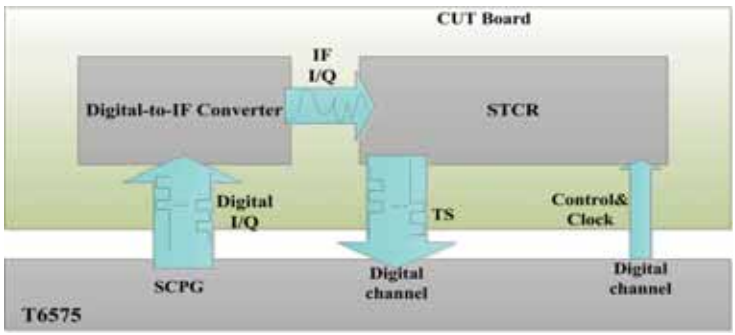
Figure 3: Block diagram of the proposed test methodology



digital signal by the IF module. The strength of the converted digital signal is improved by the AGC and then demodulated by the QPSK demodulator and corrected by the front-end corrector. The corrected signal is finally converted into an MPEG-2 TS by the format conversion unit.

Low-Cost Testing Methodology Design

Manufacturing test subjects the chip under test (CUT) to several functional tests. To test the functioning of an STCR, an IF signal is needed as a stimulating signal, which is similar to the I/Q signal. Then, MPEG-2 can be captured from the STCR and analyzed by the ATE to detect any functional failures.

In conventional testing, RF ATE such as Advantest T2000 is the only choice for testing STCRs because the mixed-signal ATE cannot generate high frequency analog

Figure 4: Schematic of the digital-to-IF converter

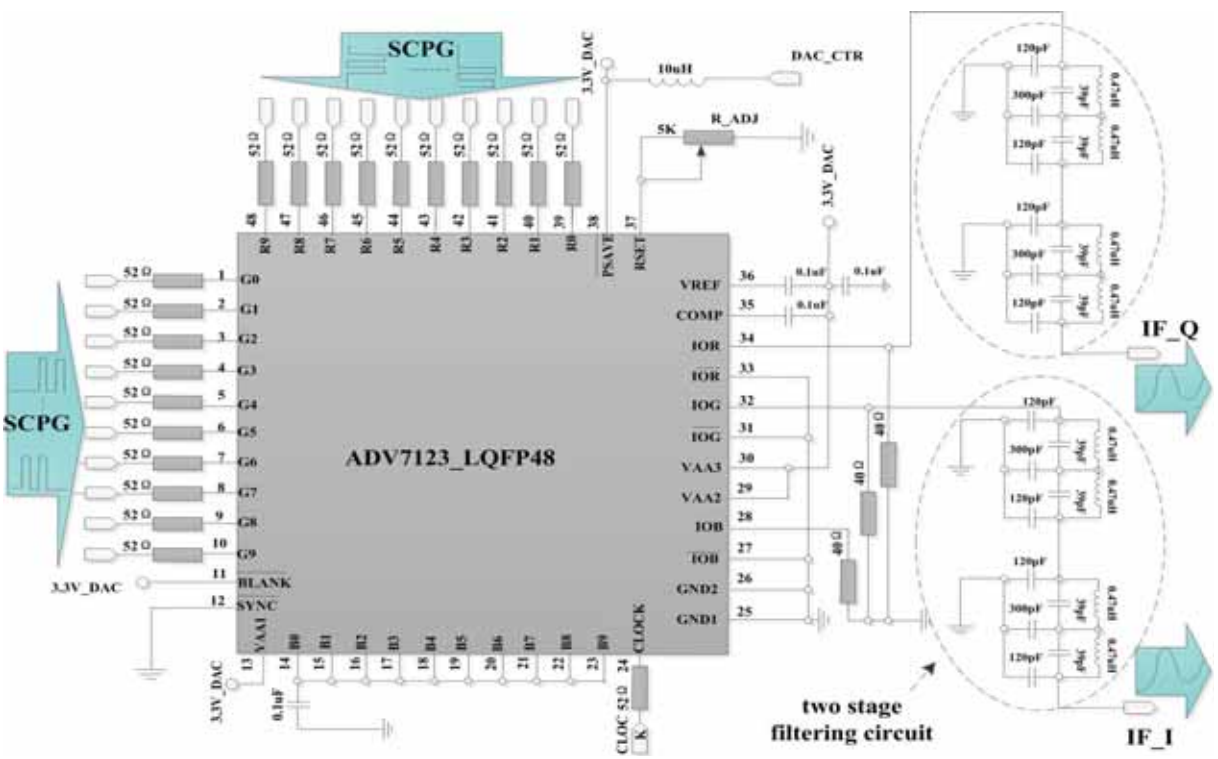


Figure 5: The converter module

signals such as IF or RF signals. However, T2000 is very expensive and results in high testing cost of about $0.32 for one STCR.

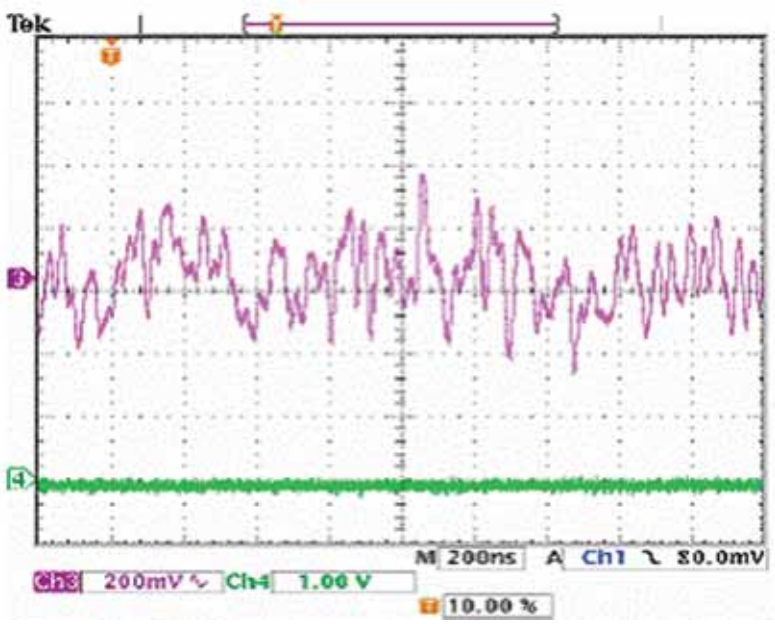
Digital ATE Advantest T6575 is much cheaper but cannot generate IF analog signals, as it does not have an RF signal generator. But, if STCR can be tested on T6575 instead of the T2000, testing costs will be decreased significantly. For these reasons, we propose a low-cost testing methodology which can achieve functional test of STCR on the T6575. Figure 3 shows the block diagram of the proposed testing methodology.

In Figure 3, the scan pattern generator (SCPG) is a common testing component in most digital ATE, which is also included in the T6575. SCPG can generate high-speed digital signals up to 125MHz. To generate IF signals, we have designed a digital-to-IF converter which converts high-speed digital I/Q signals into analog I/Q signals in an intermediate frequency. The analog I/Q signal can be used as the stimuli for the functional test of STCR. The control and clock signals can be provided by the digital channel of the T6575. The output TS is then captured and analyzed by the T6575. The key to this testing methodology is the digital-to-IF converter. The converter must have anti-noise capability and generate stable analog I/Q signals. Based on the above requirements, we chose the ADV7123 chip and designed the converter as shown in Figure 4.

ADV7123 is a high speed, digital-to-analog converter on a single chip. As Figure 4 shows, digital I/Q signals generated by the SCPG are inputted into pins G0~G9 and pins R0~R9, respectively. The output signals of pins IOR and IOG are analog I/Q signals in intermediate frequency. The control signal and clock signal are inputted into pins DAC_CTR and CLOCK respectively, which are supplied by the digital channel of T6575. However, all these signals have constraints and strict formats, provided by the STCR's designer. The two-stage filtering circuit is designed to guarantee the stability of the analog I/Q signal in Figure 4.

Figure 5 shows the digital-to-IF converter. All power supplies, clocks and digital signals are supplied by the data cable from the T6575.

Figure 6: Captured IF signal



Test Results

Figure 6 shows an IF signal captured from one MMCX connector. The waveform satisfies the functional test of STCR and can be used as the stimulating signal. By using the proposed testing methodology testing costs drop to $0.20 for one STCR, which is roughly a 37% saving on conventional testing methodologies.

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CLARION EVENTS

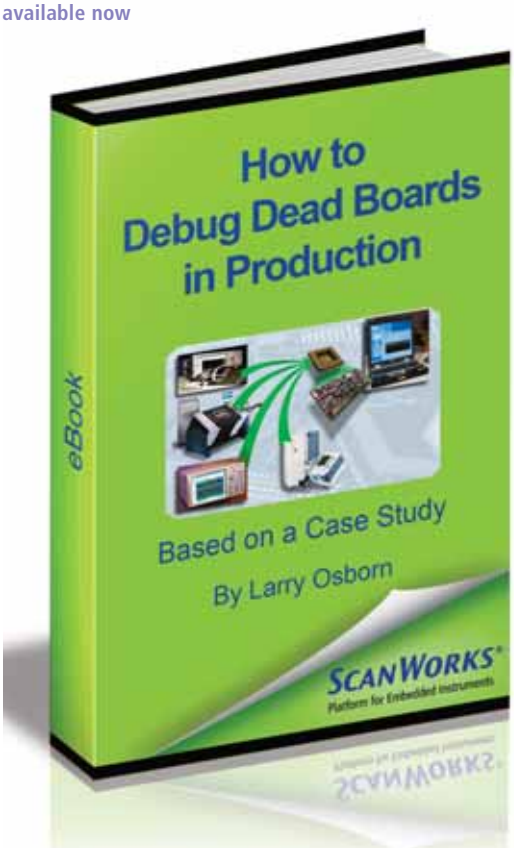
A MONTHLY COLUMN ON TEST AND MEASUREMENT (T&M) ISSUES

To Bin Or Not To Bin? That Is The Question For Improving Manufacturing Yields

BY **REG WALLER**, EUROPEAN DIRECTOR, ASSET INTERTECH INC

You may have heard circuit board production people talking about the bone pile. That's those unsellable, fully assembled boards over in the corner that won't boot or otherwise can't be brought up. In lots of cases, that pile of dead boards simply won't go away. In fact, it tends to grow, cutting into a manufacturer's profit margins.

Figure 1: *'How to Debug Dead Boards in Production'* is available now



Today, the problem of dead boards is only getting worse because production deadlines are so tight that there's very little time left for board debug to recover the investment already sunk into the bone pile. Fortunately, with the right tools and a low-tech 'binning' methodology adopted by chip makers years ago, the problem can be brought under control and manufacturing yields increased.

Cost-wise it's fairly typical today for a high-end telecom or server board to run into the $10,000 to $20,000 range. When that's the case and even when the cost of the board is a lot less, just a few dead boards can have a chilling effect on the bottom line. The usual way to test these boards in production is functional test, which assumes the board will boot, but when it won't, manufacturers are stuck. What manufacturers need are tools that don't assume any board functionality and a methodology that minimizes debug efforts so that production deadlines are not jeopardized.

Methodology

Let's tackle the methodology first. Years ago, semiconductor manufacturers struck upon a testing methodology that can be referred to as binning. The supplier would start the process by applying basic parametric tests when the die was still part of a wafer or was placed in a package.

When a device passed one test, a more stringent test would be applied. If a device failed a narrowly focused test, the device would be placed in a narrowly focused 'bin' or fault category. This is done for two reasons. First, debug time is reduced because the focus of the problem area is narrow. It's not like finding a needle in a haystack as the debug technician or engineer knows where to look. Second, fault data can form a feedback loop for making adjustments to manufacturing processes and thereby eliminate the causes of ongoing faults and improve production yields. The same principles can be applied to testing dead circuit boards in production.

The objective of binning dead boards is to narrow the focus of the repair technician to one of a few likely causes of the

problem, so that repair can be completed quickly and cost effectively. When we're developing production test suites, we often strive for total, comprehensive testing, but if the test is too broad or if the test suite cannot be compartmentalized, you can spend too much time testing a board, only to find that the problem was relatively easy to diagnose, such as a faulty power rail. An early power test could have stopped further testing and caused the board to be placed in a certain bin representing power failures. Knowing this, the repair group would only spend debug time examining issues that relate to the power devices on the board.

Let's say you're monitoring the board production flow and a consistent trend involving a certain power device begins to emerge. This data can go into a feedback loop that might lead to the replacement of one power device with another that solves the problem. The end result is fewer boards in the bone pile.

Tools

As mentioned before, you'll need tools that don't assume any functionality on the part of circuit boards. Test technologies that take advantage of onboard and on-chip design for test (DFT) structures like embedded instrumentation are quite effective here. For example, most processors have a debug port. Some tools find their way onto a circuit board-under-test via the debug port on the processor to perform at-speed functional tests without the board being functional.

> *The objective of binning dead boards is to narrow the focus of the repair technician to one of a few likely causes of the problem, so that repair can be completed quickly and cost effectively*

Of course, there's a lot more to this whole process than can be described here, so if you're interested in this topic, there is a new eBook that goes into it in much greater detail. Appropriately enough, the eBook is called *'How to Debug Dead Boards in Production'* and it's based on case study data gathered in a real-world manufacturing setting. Find it at **http://www.asset-intertech.com/ Footer/eBooks/How-to-Debug-Dead-Boards-In-Production-Case-Study.** ●

Anglia Appointed UK Distributor For Honeywell Sensing And Control

Anglia Components has been appointed as the UK and Ireland distributor for Honeywell Sensing and Control, giving its customers access to one of the world's broadest electronic sensor and switch portfolios.

"Honeywell Sensing and Control is a perfect fit with Anglia's strong portfolio of analog and digital semiconductors. It allows us to offer the complete signal chain from detection and measurement through transmission of data to monitoring and control," said David Potts, Divisional Marketing Manager for Semiconductors at Anglia.

Anglia will offer the full Honeywell Sensing and Control portfolio of more than 50,000 sensing and switching devices. Its portfolio covers all of the major parameters used to monitor the performance and control of industrial, medical, aerospace and other systems in the world today. These include pressure, temperature, speed, position, current, force, airflow, oxygen, infra-red and humidity sensors. Anglia will also offer Honeywell switches, controls, precision aerospace products and other electromechanical devices.

www.anglia-live.com

M12/RJ45 ADAPTOR FOR FLEXIBLE 8-WIRE ETHERNET APPLICATIONS

Harting introduced a new compact M12/RJ45 adaptor to provide flexibility in the implementation of 8-wire Ethernet systems in the demanding industrial environment. The adaptor has been designed in compliance with IEC 61076-2-109 and meets the requirements for Cat 6A and Performance Class EA. Both straight and angled versions are available.

With har-speed M12 Harting bases the Ethernet network on a sustainable M12 foundation. The har-speed M12 differs significantly from today's M12 connectors for Ethernet because it is based on a 4-pair connector face with paired shielding. This allows har-speed M12 to be used for Ethernet transfer rates up to 10 Gigabit. The new Harting har-speed M12 connector is, therefore, capable of complying with the high requirements of the transfer class EA, respectively the Cat 6A. For the first time an M12 cabling system can be used for relevantly high data performance and permanent sustainability.

www.harting.com

THREE-PHASE MOSFET MOTOR CONTROL IC

The new A4915 from Allegro MicroSystems Europe is a 3-phase MOSFET motor control IC that is designed for pulse width modulated (PWM) current control of 3-phase brushless DC motors. The A4915 is capable of high-current gate drive for six all N-channel power MOSFETs. An internal charge pump ensures gate drive down to 7V supply and provides limited gate drive down to 5V. A bootstrap capacitor is used to generate a supply voltage greater than the source voltage of the high-side MOSFET: a requirement for N-channel MOSFETs.

Internal synchronous rectification control circuitry with centre aligned PWM is provided to improve power dissipation in the external MOSFETs during PWM operation. Internal circuit protection includes latched thermal shutdown, dead-time protection and undervoltage lockout. Special power-up sequencing is not required.

The A4915 is targeted at both the industrial and consumer markets for end applications including power tools, lawn and garden equipment, pumps, and household appliances.

www.allegromicro.com

PIEZORESISTIVE SILICON PRESSURE SENSORS IN A ROBUST HOUSING WITH RANGES UP TO 10 BAR (150 PSI)

First Sensor presents the new Sensortechnics HRO pressure sensors for gage and differential pressure measurement in a wide range from 10 mbar up to 10 bar (4 inH2O to 150 psi) full scale. The robust HRO pressure sensors are calibrated and temperature compensated and can be used with dry and non-corrosive gases. The completely analogue signal conditioning ensures mV output signals with nearly unlimited resolution.

The special HRO housing design offers ideal protection against possible stress during sensor mounting. The outer package is mechanically decoupled from the inner part holding the highly stable silicon sensing element. The HRO sensors provide a miniature SIL housing with mounting holes for convenient, space-saving PCB-mounting. Two pressure ports allow for easy tubing connections.

www.sensortechnics.com/hro

Rohm Receives "Quality Award" From Continental

Rohm Semiconductor has been given the "Quality Award" by the Continental Automotive Group. This special award is presented in alternate years to suppliers from the electronics and mechanical engineering sectors in recognition of outstanding performance in quality improvement. Christian André, President of ROHM Semiconductor, was very pleased about this recognition: "The prize reflects the fundamental importance of quality management which is part of our company mission since its foundation in 1958. Quality to us is a holistic approach covering product performance, costs, service, environmental aspects and delivery. We are committed to deliver added value to our customers that makes a difference."

Based on a systematic annual appraisal of more than 900 strategic suppliers, the Automotive Group identifies those companies that have turned in an outstanding performance in the various material segments. In total, sixteen winners received their Automotive "Supplier of the Year 2012" Awards as well as two special awards for "quality" and "innovation".

www.rohm.com/eu

CAMLOCK INTRODUCES DURABLE MINIATURE SWITCHLOCK RANGE

UK-based industrial locking company Camlock Systems is launching a new range of extensively tested miniature switchlocks. The range includes single pole and double pole types, with options on head profile and key combinations.

The miniature switchlocks have been successfully tested in excess of 20,000 cycles. They are V0 fire resistant, they operate in temperatures between -20°C to +65°C and are rated for currents up to 5A at 115V AC.

The locks offer full functionality through Camlock's proven Series 21 locking mechanism. They come in ultra compact proportions, boasting an overall body length of just over 3cm and a small 16mm x 13mm mounting hole size.

The new locks can be specified keyed alike or keyed to differ, and up to 200 different key combinations are available.

They are available with the key either trapped or free in the locked position, and they can be supplied to the 801 and 901 key combinations.

www.camlock.com

Power Integrations Launches LYTSwitch-0 Family of Highly Integrated LED-Driver ICs

Power Integrations introduced LYTSwitch-0 ICs, a new series of devices within the LYTSwitch family, offering a unique combination of simplicity, reliability and efficiency. LYTSwitch-0 ICs are ideal for cost-sensitive, non-isolated, non-dimmable GU10 bulbs and other space-constrained bulb applications.

LYTSwitch-0 devices feature efficiencies of more than 90% and deliver constant current with better than ±5% regulation in typical applications. Power factor is greater than 0.8 at 115VAC and 0.55 at 230VAC, meeting ENERGYSTAR V1 draft 3 consumer lighting standards for North America and Ecodesign Directive Lot 19 part 2 for Europe.

"RDR-355 describes a GU10 LED driver using the LYTSwitch-0 IC and just 13 components. The device's small size and high efficiency eliminate the need for heatsinking or potting of the LED driver, reducing manufacturing cost," said Andrew Smith, product marketing manager for Power Integrations.

Key applications include low-cost LED light bulbs such as GU10 and candelabra styles.

www.powerint.com

NEW ROTARY POSITION SENSORS FROM BOURNS NOW AVAILABLE FROM TTI, INC.

Bourns's new AMM20B non-contacting multi-turn rotary position sensor and AMS22U non-contacting analog rotary position sensor for applications that require frequent adjustment can now be ordered from TTI, Inc. Both sensors are designed to meet the specifications of heavy-duty applications requiring long cycle-life and high reliability.

AMM20B features a 12-bit resolution and factory programmable electrical angle from 1080 to 3600 degrees. Highly resistant to vibration and shock as well as to fluid and dust ingress, the AMM20B sensor is programmable at factory for zero position, offers a rotational life of up to 50 million cycles and is fully RoHS-compliant.

The single-turn AMS22U non-contacting analog rotary position sensor features a 1/8" shaft supported by dual ball bearings and a factory programmable electrical angle from 10 to 360 degrees. Available in a servo mount configuration with a rotational life of up to 100 million cycles, it is programmable at factory for zero position.

www.ttieurope.com

AVX INTRODUCES INNOVATIVE TESTING PROCESS FOR TANTALUM CAPACITORS

AVX Corporation has developed an innovative and extremely effective new process for the manufacture and test of high-reliability tantalum capacitors. Initially introduced to members of the military and aerospace industries at a Tantalum Hi-Rel Symposium held in Biddeford, Maine, in January, AVX's new Q-Process was also presented in a technical paper at the Capacitor and Resistor Technical Symposium (CARTS) International conference in Houston, Texas, in March. Well received by participants in both events, the Q-Process stands poised to replace the Weibull Reliability Assessment as the industry standard for tantalum capacitors. Driven by MIL standards and used to characterize the reliability of tantalum capacitors for decades, Weibull has become less relevant in recent years due to widespread improvements in manufacturing and testing technology.

AVX's highly effective new Q-Process has received a provisional patent and is now available for small case size medical grade tantalum capacitors. It will available for military and aerospace product lines later this year.

avx.com/docs/techinfo/Qprocess.pdf

MOUSER ELECTRONICS NOW STOCKING PLESSEY SEMICONDUCTORS

Mouser Electronics is now globally distributing Plessey Semiconductors's complete range of products, including Plessey's multi award-winning EPIC sensor and MAGIC GaN LEDs.

Plessey's EPIC (Electric Potential Integrated Circuit) sensors can be used in contact mode for measuring bio-electric signals like ECG, EMG, EOG and EEG, or in non-contact mode for measuring disruptions in the electric field caused by human body movement. Additionally, Mouser's stock includes Plessey's new Gallium Nitride (GaN) High Brightness (HB) LEDs, manufactured using cost-effective GaN-on-Silicon processes.

"We always aim to provide design engineers with the latest technologies so that they can create state-of-the-art designs. Plessey has built its global brand recognition over the decades by being a true innovator in the electronics industry, always pushing the boundaries to deliver novel and clever solutions," said Mike Scott, Mouser Vice President of Semiconductors.

Michael LeGoff, Plessey's CEO, added: "We are excited to have Mouser distributing our products globally."

www.mouser.com/Plessey-Semiconductors

MOUSER ELECTRONICS

Harwin's Hi-Rel Connector Families Go Into The Stratosphere

Harwin is congratulating the team at Warwick University on the successful launch and recovery of the maiden flight of its WUSAT nano-satellite, which depends on Harwin's high reliability Datamate and Gecko connector families to provide signal and power connection, despite the challenging operation conditions.

The Warwick University team launched 'CubeSat' (a small satellite typically measuring just 10 x 10 x 10cm and a mass of 1.33kg) to assess the possibilities for various payloads and development. The team has based control, power and communications systems on the Arduino platform and data from sensors included on separate PCBs was captured on SD cards.

With this level of systems payload, a miniature and lightweight yet very high-reliability interconnect system is required, so the WUSAT team is evaluating Harwin's 2mm Datamate signal and power connector family, and the company's recently-launched 1.25mm Gecko connector range that can handle up to 2A.

www.harwin.co.uk

NEW PROFILED LIGHTBARS FROM OMC PROVIDE EVEN ILLUMINATION

OMC has announced the launch of its ProfiLED Lightbar product family, which reduces cost and offers an improved appearance, especially in low and medium volume applications.

Unless production volumes are very high, the cost of developing a custom lightbar is prohibitive for most applications. Instead, designers often use several standard square or rectangular units in combination. However, this approach gives rise to high materials and assembly costs, and the finished product has unsightly dark lines where the arrays join. Using the same approach as it adopts in its ProfiLED Backlight range of LCD backlights, which employ LED edge-lighting and an acrylic lightguide to achieve uniform, consistent illumination, OMC can now offer alternatives to lightbars in a vast range of colours. Devices can vary from 2mm to 7mm in height and can be produced in a huge range of bespoke shapes and sizes with little or no set-up cost and very low MOQs.

www.omc-uk.com

NEW CALIBRATION SOLUTION FOR RENT VIA LIVINGSTON

Test equipment sourcing specialist Livingston has put facilities in place that will greatly assist customers struggling with the cost and logistical problems presented by carrying out recalibration. It will henceforth offer them the option to calibrate their own equipment by renting calibrators from its inventory.

For smaller companies, involved in installation work or serving the industrial space, it is often hard to justify the heavy investment needed for acquiring calibration equipment, as the stock of test instrumentation being held is not enough to ensure regular utilisation of the calibrator. As a result the calibrator is left idle and the money spent on it is effectively wasted. Likewise, sending single pieces of instrumentation off for calibration is not very cost effective, as there is a considerable mark-up involved each time. It can prove to be far more attractive, both financially and operationally speaking, to simply rent a calibrator once year to re-calibrate all the company's instrumentation in one short period.

www.livingston.co.uk

CSS ANNOUNCES ELECTRONICS CAPABILITIES

Connecticut Spring & Stamping (CSS), a manufacturer of precision parts for the aerospace, medical, firearms and defence industries worldwide, announces its wide range of springs and stampings for the electronics industry.

Known for its extremely rapid turnaround time capabilities, CSS works in conjunction with customers from product development and prototyping and continuing on through high volume production. For one recent innovative circuit breaker application designed for areas where space is at a premium and the ability to upgrade electrical systems is critical, CSS consulted on the wire sizes, loads and spring designs, and then provided prototypes and engineering samples on a fast-track basis to meet the customer's product launch timetable. With CSS's consignment program, parts are manufactured and shipped directly to a customer's warehouse and the customer is not invoiced until the parts are actually used.

"CSS specializes in collaborating with electronics customers to achieve their design objectives, " said Steve Dicke, vice president of sales and marketing at CSS.

www.ctspring.com

Rack-Mount Equalizers Help Optimize Satcom Performance

Now available from Link Microtek is a series of rack-mount amplitude/slope equalizers that will enable L-Band satellite communications designers to optimize the performance of their systems.

Manufactured by US company MITEQ, the equalizers come in two versions – DL1E and RL1E – which provide dual-channel and 1:1 redundancy operation, respectively.

Offering independent gain and slope adjustment, the new units are designed to eliminate RF/IF cable run losses and compensate for L-Band cable frequency roll-off. The series includes models covering the frequency ranges 950-1450MHz, 950-1750MHz and 950-2150MHz.

Both types of equalizer feature hot-swappable RF modules and fully redundant hot-swappable power supplies to maximize system availability, and the RL1E redundancy unit can be set for automatic or manual switchover.

Remote control is provided as standard via a user-selectable RS485/RS422 interface, while RS232 and 10/100Base-T Ethernet interfaces can be specified as options.

Operating from a 90-250VAC input, the equalizers are suitable for use in ambient temperatures ranging from 0 to 50degC.

www.linkmicrotek.com

REAL-TIME SPECTRUM ANALYSIS OPTION FOR AGILENT PXA SERIES AVAILABLE FROM ELECTRO RENT EUROPE

Today's advanced aerospace/defence and communications systems must operate effectively in an increasingly cluttered spectral environment.

The Real-Time Spectrum Analysis (RTSA) option for the PXA X-Series of signal analyzers from Agilent Technologies provides unmatched performance for the identification of elusive or intermittent signals.

In applications such as radar, electronic warfare, military and commercial communications, the probability of intercept (POI) is the key benchmark for real-time spectrum analysis. When configured for real-time spectrum analysis, the Agilent PXA can detect intermittent signals with durations as short as 3.57µs, with 100% POI.

As an Agilent premier rental partner, Electro Rent has provided the PXA series of spectrum analysers to its customers since their introduction. Electro Rent can now supply the new RTSA option for the PXA on the same rental or leasing terms.

Agilent's real-time PXA provides 75dB spurious-free dynamic range across analysis bandwidths of up to 160MHz.

www.electrorent-europe.com

MICREL LAUNCHES NEW HIGH SENSITIVITY LIMITING POST AMPLIFIERS FOR 10GBPS FTTH PON

Micrel launched the SY88053CL and SY88063CL limiting post amplifiers. The devices are ideal for FTTH XGPON and 10GEPON OLT (Optical Line Terminal) applications supporting the build out of next generation PON networks. This product family is also suitable for use in fibre optic transceiver modules for multi-rate applications up to 12.5Gbps supporting Ethernet, Fibre Channel, OTN and CPRI/OBSAI data rates. Production samples and pricing are available from Micrel.

Both devices incorporate fast SD Assert and LOS De-Assert times across the entire differential input voltage range of 5mVPP to 1800mVPP which enables improved link efficiency and optimization. Electrical hysteresis of 4dB is provided across a wide LOS/SD threshold range of 3mVPP to 30mVPP. Integrated 50 Ohm input and output impedances optimize high speed signal integrity while reducing external component counts and in turn, cost. The TTL compatible JAM input enables a SQUELCH function by routing back the LOS or SD signal.

www.micrel.com

MICREL®
Innovation Through Technology®

SMALL INDUSTRIAL SUBRACKS FOR CONTROL CABINETS

For small measurement, control and instrumentation units that are built into control cabinets along with a PLC controller, Pentair has developed a compact Schroff industrial subrack. This is based on the established europacPRO platform of 19" subracks and is 3U high, 205mm deep and just 28 HP wide.

The mounting brackets of the subrack feature keyholes for easy fixing to the mounting plate on which appropriate bolts or screws are provided. The subrack is available with or without a rear hood. A drilled plate is inserted to provide a top cover. A bolt-on cover plate is also available as an option.

The new industrial subrack is available in two versions: one version is prepared to accommodate a backplane, while the other is designed for the use of connectors. Fitted with a suitable backplane, power supply unit and ventilation unit, this subrack can be used, for example, as a small CompactPCI system with up to five plug-in boards.

www.schroff.biz/subracks

COMPANIES CREATE ANTIMICROBIAL SWITCHES TO FIGHT INFECTIONS

Arcolectric (an Elektron Technology connectivity brand) and BioCote Ltd are offering a range of switches and covers with built in BioCote antimicrobial technology, providing integral protection from a wide range of micro-organisms, including bacteria, mould and fungi.

Recent high profile reports on antibiotic resistance have highlighted the need for robust infection-prevention strategies, helping to eliminate antibiotic resistant organisms before they can cause infection. Arcolectric can incorporate BioCote active silver ion technology into any of its ranges of rocker, push-button and double-pole switches, as well as dust and splash resistant covers. This reduces the presence of bacteria by up to 99.9%, with no decrease in efficacy for the expected life span of the component, offering equipment manufacturers a key differentiator for the laboratory, healthcare and food processing sectors.

Antimicrobial switches are available now

"Switches and controls are often the first contact point for a user when they interact with a product, making these high traffic areas a key target in the fight against microbial contamination. Integration of BioCote's innovative antimicrobial technology into our components represents an important step forward, providing our customers with a straightforward enhancement that will benefit end users without impacting on equipment design or manufacture," said John McVeigh, Product Manager for Arcolectric.

JAN DIDDEN, Audio Expert and Publisher of Linear Audio, The Netherlands: I am sure Arcolectric's initiative is well-meant, but it is not at all clear that this is a good thing in the long run. It has become increasingly clear that our very clean and germ-free environment has adverse effects on the human body's capability to deal with new bacterial and viral threats. Exposure to infection sources is necessary to keep the immune system 'trained' and vigilant for new unknown threats. The case has been made that children who no longer have opportunities to play in the dirt have a statistically greater chance to contract allergic diseases, for example. When the USSR collapsed in the late 80s, and with it part of its health system, one effect was a decrease in the incidence of asthma in children!

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: Switches are the first contact points for users wishing to interact with electrical equipment. Thus, harmful microorganisms can easily be transmitted from infected persons through the use of such devices. Antimicrobial switches will help to reduce bacterial contamination and protect the users. This is certainly very important, especially for people using electrical equipment while working in the food industry, as it will reduce cross-contamination and the presence of bacteria by a significant amount.

> Antimicrobial switches will help to reduce bacterial contamination and protect the users; this is certainly very important, especially for people using electrical equipment while working in the food industry

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Nowadays, scientific and technological innovators offer an important part of their products for the service of humanity. In this context we note that the collaboration between Arcoelectric and BioCote Ltd has introduced commercially available products with microbial protection. Indeed, the modern world has many public places, such as hospitals, catering establishments, schools, shopping centres etc, where preservation of health is very important and yet the risk of microbial infection is very high in them. BioCote is one of the first to come up with anti-microbial protection for everyday switches, maybe others will follow suit. BioCote, in collaboration with industrial partners, has made a very beneficial scientific and technological breakthrough, despite its commercial nature. Indeed, by reducing the microbial contamination, one improves the human's hygienic conditions and, thus, reduces the exposure to threats caused by microbial contamination. In the end, ensuring preventive health protection is much better than medical care.

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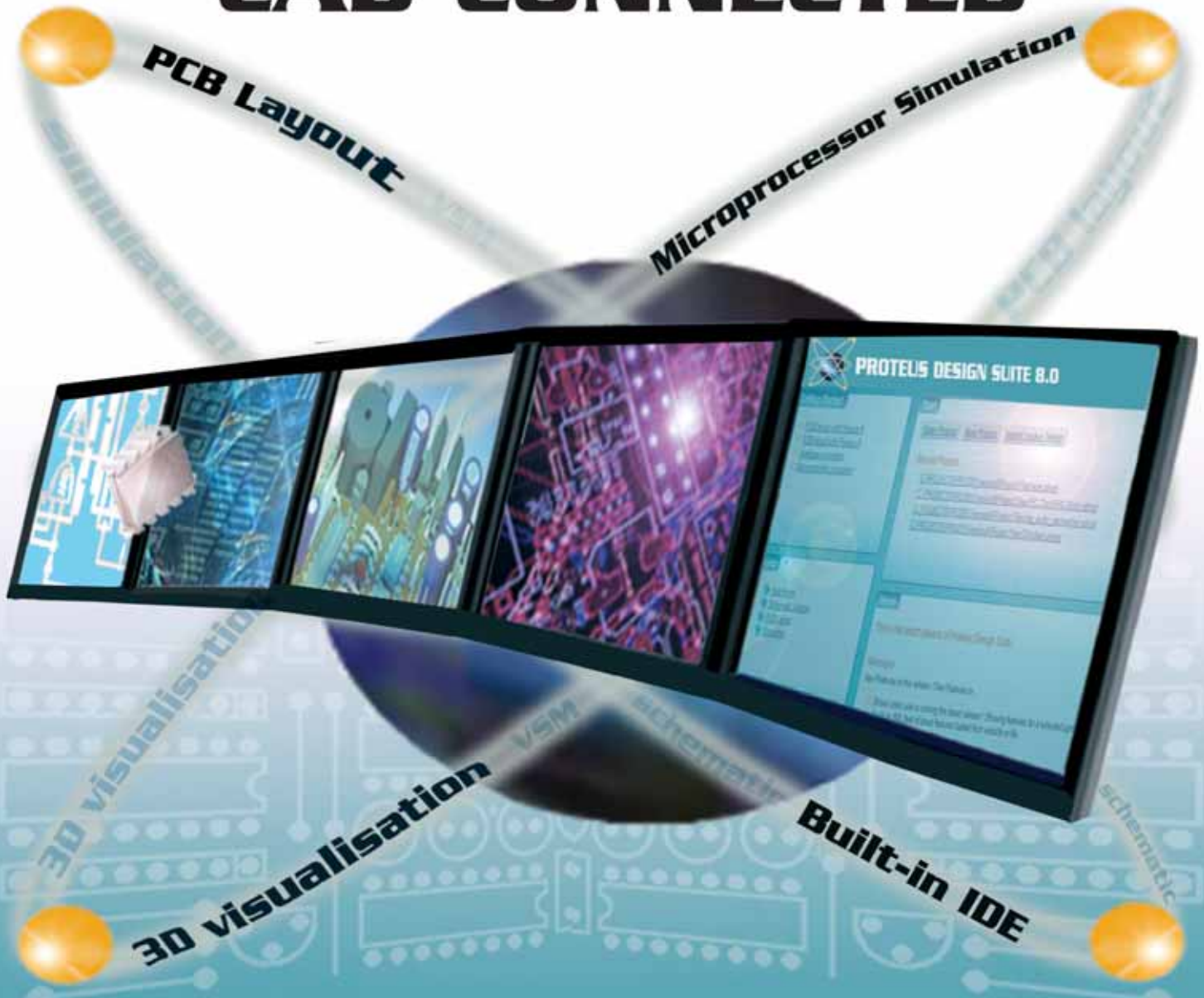

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