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More on pages 8-9

REGULARS

05 **TREND**
WOMEN ENGINEERS IN THE 21ST CENTURY

06 **TECHNOLOGY**

10 **THE TROUBLE WITH RF...**
RESPONSE TIME
by **Myk Dormer**

38 **R&D FROM CHINA**
IMAGE SEGMENTATION USING ARTIFICIAL INTELLIGENCE APPROACHES

42 **EVENT**
PRODUCTRONICA

44 **T&M COLUMN**
by **Reg Waller**

46 **PRODUCTS**

50 **LAST NOTE**

06 Technology

46 Products

FEATURES

12 **MAKING SENSE OF CURRENT SENSE TRANSFORMERS**
Paul Lee, Director of Business Development at Murata Power Solutions UK, describes some pitfalls to avoid and techniques to employ to achieve best performance in current sense transformers. He uses a high-frequency current transformer as an example but the principles apply equally at low frequencies

20 **SMART SENSOR CONTROL**
Rich Miron from the Digi-Key Technical Content Team outlines the key requirements to consider in the design of accurate sensing systems

26 **VARIATIONS ON THE COMPLEMENTARY FOLDED CASCODE TRANSIMPEDANCE STAGE IN DISCRETE AUDIO FREQUENCY POWER AMPLIFIERS**
Michael Kiwanuka examines Samuel Groner's arrangement and variations of the complementary folded cascode transimpedance stage in discrete audio frequency power amplifiers, and evaluates these against the conventional J. E. Thompson topology

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WOMEN ENGINEERS IN THE 21ST CENTURY

> *There is still more to be done if we hope to meet the demand for more candidates entering the engineering profession and to fill the skills gap*

The latest annual skills survey carried out by the Institution of Engineering and Technology (IET) showed that the percentage of women in the engineering workforce (7%) has not changed significantly over the last five years. This is surprising considering the corresponding evidence that the industry is facing a skills shortage and is projected to have 2.74 million job openings from 2010 to 2020. Currently, the UK is only producing around 46,000 engineering graduates per year and an increase in women entering the industry could significantly make up the surplus needed.

The IET's 2013 skills survey concluded that Professional Engineering Institutions (PEIs), employers and industry need to encourage more students with the appropriate educational background to pursue engineering careers, especially women. To achieve this, perceptions of engineering must be challenged so it is seen as a positive career choice, relevant to the 21st century and suitable for both men and women. It is not just students whose perceptions should be targeted, but also parents and teachers who advise young people on career paths.

There is an urgent need for better careers information and advice and guidance to promote the engineering profession. The benefits that a career in engineering can bring needs to be emphasised, so young people should know that STEM (science, technology, engineering and maths) subjects aren't necessarily harder than other subjects.

In recent years, apprenticeships have received more and more support from the government and they are finally being recognised as a rewarding alternative to a university placement. However, the government must continue with this support and ensure that the quality, not just the quantity, of the apprenticeships available is high. Whether it be the government, the PEIs, teachers or the ambassadors like myself, we all have a responsibility to take action to encourage more women into engineering.

The IET's Young Woman Engineer of the Year awards are a great way to recognise young talent within the industry, but they also create ambassadors and role models for other young girls looking into engineering. Being an YWE award winner is not just about the title, all winners are expected to spend the next year fulfilling ambassadorial duties encouraging other young girls into engineering.

Earlier this year, along with eight other PEIs, the Institution of Engineering and Technology signed the Diversity in Engineering Concordat, which pledged commitment to equality within the profession.

The document outlined three objectives that all Institutions involved must adhere to. These are: to communicate commitment to equality and inclusion principles, to monitor and measure progress and to increase diversity amongst those in professional membership and registration.

The IET also runs its own Women's Network, which provides a strong support system and information hub for women engineers. It provides office space for the Women's Engineering Society (WES) and the WES Prize is awarded as part of the Young Woman Engineer of the Year ceremony.

The IET's dedicated education programme – IET Faraday – is specifically designed to attract girls as well as boys to engineering through a series of in-school engineering tasks and activity days. In addition, the Institution also has a long association with the WISE Campaign, which encourages young women to study Maths and Physics and to consider careers in science, engineering and construction.

However, there is still more to be done if we hope to meet the demand for more candidates entering the engineering profession and to fill the skills gap. If we can appeal to half of the UK population, and raise the number of women in the workforce from 7%, then the UK economy will benefit greatly from a booming engineering industry.

Jessica Jones was an IET Young Woman Engineer of the Year 2012 finalist, and received the Intel Inspiration Award for Entrepreneurship. She is currently studying Astrophysics at Cardiff University, while working on the patent for new fibre optic sensing technology and looking to launch her own company

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MAXIM INTEGRATED ALIGNS PRODUCT PORTFOLIO TO GROWTH SECTORS

Maxim Integrated aligns product portfolio to several growth markets

Maxim Integrated is positioning its product portfolio to meet the demands of the growing industrial, medical (including wearable health monitoring devices), embedded security and communications (which includes mobile payment) sectors.

"According to iSuppli, industrial markets are growing at 9% per year, the second fastest growing market after smartphones. According to ABI Research there will be 100 million wearable devices by 2016. And there's a new trend for mobile payments, which by 2017 there will be some $1.5 trillion of," said Christopher Neil, senior VP of the Industrial and Medical Group at Maxim. "We are aligning our business to [these] end markets."

In the quest to have smart homes, factories, cars, grids and healthcare, devices need to become 'smart' too, with much higher integration of functionalities and yet consume lower power and fit in smaller packages. In addition, they have to be more secure too.

He says the company has very good expertise and products that will meet these demands. Including low power transceivers, security, sensors, micros, interfaces and switches and so on, "nearly half of our business is highly integrated products rather than building blocks," he said. Where necessary, however, Maxim will continue to acquire further expertise, as is the case with its recent $605m acquisition of Volterra Semiconductor, a developer of highly integrated power management for cloud computing and networking. Cooperation is not ruled out either, as Maxim forges relationships with innovators like Clearbridge VitalSigns and Orbital Research, with which it recently developed wearable medical electronics fitted into shirts – called the Fit shirt.

For rapid prototyping Maxim is offering 15 different Pmod-compatible peripheral modules, which are plug-in hardware modules with pre-written software drivers and workhorse functions, such as DACs, transceivers, time clocks, clock oscillators and many others. The modules are compatible with existing FPGA platforms and can be ported to other platforms too.

It's All Change at Renesas

It's been all change at Renesas recently, with a $1.5bn cash injection, simplified management structure, reduced workforce and a lower number of facilities in the effort to turn around its fortunes. The $1.5bn investment came from a customer-government combo, where companies such as Toyota, Nissan, Canon, Nikon, Panasonic, Denso, Keihin and Yaskawa Electric put up part of the money, and the rest from the Innovation Network Corporation of Japan (INCJ).

Renesas is now concentrating on primarily three business areas: automotive, industrial (including home automation) and wireless network infrastructure.

"These long-lifecycle product markets fit well with our DNA," said Rob Green, who is stepping down as the European president to be replaced by Gerd Look, formerly in charge of the automotive group at Renesas.

"By 2020 we'll see semi-autonomous cars that will be able to park themselves. Will they be fully automated by 2025? [To make this happen] we will need communications, computing, cameras and radar. Our own challenge is to develop a product portfolio to support all this," confirmed Look.

Another concept Renesas wants to build on is the smart factory, which is particularly taking hold in Europe.

"Renesas is very strong in the process automation and factory automation markets – with award-winning technologies," said Look. "We have standard products, Ethernet, sensors, MPUs, industrial switches, visualisation systems that will support these markets."

Renesas's own microcontroller families the RX, RH850 and RL78 will continue to be part of its future product offerings, in addition to new platforms, ASSPs and SoCs that the company wants to continue to build. "Our strengths are microcontrollers, SoCs and power electronics – and these are set to grow," said Green. "[but] for developing new technologies we will not do everything ourselves; we will consider partnering with others."

RS Components Launches DesignSpark Mechanical to Help Designers with 3D Prototyping

RS Components continues steady on its path of innovation with the launch of DesignSpark Mechanical, free 3D modelling and assembly software.

Despite its name immediately suggesting a tool for mechanical engineers, it is rather applicable to all engineering disciplines, and particularly electronics and electrical engineers who might want to rapidly create 3D models to accelerate engineering design easily and without the high costs and long learning curves typically associated with other MCAD software packages.

Most MCAD packages are either parametric, history-based modelers or direct modelers.

In the workflow of a parametric, history-based modeller, the order of features is important. A user can also go back in the history of the design and change properties.

In the workflow of a direct modeler (which is not history-based), the order of features and when they have been created is not important, but they don't have any parametric functionality. DesignSpark Mechanical combines the features of a direct modeler with parametric functionalities, which designers will find very useful for fast design iterations. With its four basic functions (pull, move, fill and combine) and Windows type shortcuts such as cut/paste and redo/undo, design proves intuitive and easy, and hence more fluid. Designs can be shared with colleagues, and modified by them, making it a much easier functionality than traditional parametric-type, history-based modelers. DesignSpark Mechanical can export to STL formats for printing a design on desktop 3D printers.

Keith Reville, RS Components Global Marketing Director at the launch of DesignSpark Mecanical

According to RS Components's recent figures, in the first two weeks since its launch, there have been over 50,000 downloads of DesignSpark Mechanical from the company's online engineering community site DesignSpark.com.

RS Componets plans further enhancements to its DesignSpark offerings in the future, but it also continues to improve its website, with e-commerce playing a pivotal role. "We see a huge opportunity and we want to make our e-commerce even better," said Keith Reville, RS Componets's global marketing director.

DO YOU HEAR THAT?

By Greg Quirk, Mouser Electronics

Audio. It's hard to imagine a world without sound. It's amazing how much sound enhances our viewing experience. In the U.S. alone, the average home has 2.9 television sets, with 56% owning at least one HD TV – making it the fastest adopted technology over the past two decades. However today, what viewers see on screen often exceeds what they hear. This can be understandable because the majority of audio systems for most consumers is provided directly from the sets.

Audio for portable devices lags even further behind. For handheld devices, the speakers are not significantly large to push enough air to generate enough volume (provide the highs and lows) to make it an enjoyable experience. To help counter this problem, headphones come into play. Most every portable device, whether it's an MP3 player or media player, comes with some form of headphones. But to keep costs down, they are typically not of high quality.

Given the meteoric popularity of portable media devices, including smartphones, tablets, MP3 players, portable DVD players, and many others, the headphone market is poised to generate over $700M by 2012. Consider that by 2015 expectations are that there will be over 250 million tablets sold, and over 1.6 billion smartphones globally by 2017. That's a huge market for any add-on device, especially when you take into account that headphones are considered a necessity by most consumers.

STYLE

There are a number of different aspects to consider when looking for headphones. First is the style – on-ear, over-ear and in-ear. Each has a different purpose, and comfort can vary from person to person. Some chose not to wear in-ear because they constantly fall out. Others do not like on-ear or over-ear because they can put pressure on your head. It all comes down to what is going to work best for your needs and preferences.

APPLICATION

Second is the application. The headphones for someone working at a call center or a DJ are going to have very different features and functionality than someone who flies a lot and requires noise cancelation. For industrial jobs, headphones can even be created to meet certification standards, such as the Occupational Safety & Health Administration (OSHA), that combine safety with audio capabilities, such as being able to converse with someone over a microphone. Since 2004, the Bureau of Labor Statistics has reported that more than 125,000 workers have suffered significant, permanent hearing loss. In 2008 alone, BLS reported 22,000 hearing loss cases.

The regulations for hearing safety require that a worker is not exposed to more than a certain decibel level per day for an allotted period of time. The amount of time changes based on the sound level, but for a typical eight hour day the employee should not be exposed to more than 90 decibels without hearing protection.

PERMISSIBLE NOISE EXPOSURES (OSHA Website)	
Duration per day, hours	Sound level dBA slow response
8	90
6	92
4	95
3	97
2	100
1 1/2	102
1	105
1/2	110
1/4 or less	115

QUALITY

Third, you have to consider the audio quality. There are many companies that make audio amplifiers, including Texas Instruments and Maxim. One of the key metrics for headphone amplifiers is the impedance, which start around 10 ohms for low-end headphones and reach 50 ohms or more for professional quality sets.

The signal-to-noise ratio is also important in determining how much volume the headphones can produce. A higher SNR will result in louder volume being generated – unless it's combined with a good frequency range, usually around 30hz – 18khz (although most headphones claim to have at least a 20hz – 20khz range).

The better the quality of the headphones, the higher manufacturing costs due to the quality of the materials and the additional components that are implemented to produce the sound, which is why the free headphones given with an iPod are nothing compared to a $400 (or more) pair of high-quality headphones.

NOISE CANCELLATION

In situations with constant sounds, noise cancellation is a boon. When travelling on an airplane or bus, turning on noise cancellation reduces outside noise by using a microphone to replicate the sound at an inverse frequency. The technology was first thought of in 1978 by Dr. Amar Bose, who came up with the concept while on a flight. Eight years later, noise cancelling headphones were successfully trialed for pilots on around-the-world flights, with the first commercial products being offered in 2000. Since then, noise cancelling technology has been adopted by many manufacturers. Some consumer products, like the Sony Walkman, include noise cancellation in the actual device instead of relying on headphones.

CONNECTIVITY

The final consideration is how the sound travels to the headphones. Traditionally a physical cord is connected from the set to the device, but wireless technology improvements have let consumers cut the cord. However, there is a trade off between the convenience of not having physical wires and the power requirements, the complexity of a wireless headset, as well as audio quality loss since the signal must be compressed. Almost all smartphones and tablets, not to mention many MP3 players, have BlueTooth functionality that enables this connection.

While there are other options available, such as RF, infrared, FM, and many others, BlueTooth is the connectivity method of choice. The low power and commoditized cost, combined with a relatively low signal loss over short range to prevent interference, plus two-way transmission make it ideal for most headset applications.

CONCLUSION

Summing up: Prices for headphones vary drastically, starting from a few dollars for low-end sets to thousands for extremely high-end audiophile headphones. Even if a company can get a fraction of the addressable market for their product (whether it's an actual headset or any component inside), the sheer quantity that the market can purchase along with the tremendous growth that it's experiencing from tablets, smartphones and MP3 players makes it a very interesting prospect.

For more information please visit the section Audio of our Applications & Technologies webpage at uk.mouser.com

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Response Time

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"Correct and full specification, at the start of the project" is an axiom so often repeated that it is fast becoming a cliché. It is no less true in the low power wireless sector than any other, but problems frequently arise when the end user is unaware of the relevance, or the impact on the design, of one or more of those specifications.

An excellent case in point is the response time of a system. Even in control applications it is very easy (once more obvious issues such as frequency allocation, transmitter power and, hence, range have been thrashed out) to stipulate a link data rate, and think that the job is done. Unfortunately, data rate is only half the problem. It is more meaningful to identify the actual process being controlled and determine the required minimum time delay between a stimulus or control input change at the "transmitter" end of the link and the corresponding output or state change at the "receiver". Even in simple control systems this critical response time is subject to a huge range of variations:

- In process control applications, where the radio link is reporting a sensor state in a process to an automated system controlling that process, the response time is critical: ten milliseconds can be too slow for such an application and, if the radio link is inside a real-time positional feedback loop, even tenths of a millisecond can be too much.
- Where a human operator is directly controlling an observed process ("push the button/turn on the light") then the response time can be considerably slower, owing to the reaction time and cognitive delay of the operator. Surprisingly, delays of at least 100ms, and often over 250ms, are perfectly acceptable.
- Alarms, and annunciators (or in plainer terms: doorbells) can tolerate longer delays – tens of seconds or more. (In this case it is enough for the user to know that the alarm state is being transmitted. The actual activation of the alarm can wait).
- Remote sensing, such as environmental temperature or humidity monitoring, tide gauges or intruder alarms, can tolerate even longer delays: tens of seconds or minutes, and depending on the application and the rate of change of the parameter being measured, sometimes more.

> *Response time is frequently forgotten about when initial requirements are drawn up, but can be the most important of all the parameters influencing a design*

As you can imagine, from a radio system design point of view, the response time parameter is of overwhelming importance. A fast response requires a high data rate (sufficient data to signal the control event to be sent over the link, and decoded) but high data rate alone is not enough: the hardware must initiate communication rapidly too. If a transmitter takes a second (for example) to power-up, a high data rate will not subsequently compensate for that slow response. (This can be a serious issue with "network" radio products, where data rate is high but acquiring or logging onto the network can be very slow indeed. It may be possible to implement some sort of "hot standby", but this must be designed in from the start). Where response times are less critical, the system designer can use this fact to advantage. It becomes possible to use just the sort of networked architectures mentioned above, or beneficial tradeoffs can be made in terms of response time versus link data rate (and sensitivity, and thus range per transmitter milliwatt).

Finally, as the system response time moves into the "minutes, or hours" area, a fresh set of design challenges are likely to appear, as such "monitoring" systems are very often battery-powered and, so, also require very low power consumption. This can call for very low duty cycle techniques and dedicated low power hardware.

To conclude: response time is frequently forgotten about when initial requirements are drawn up, but can be the most important of all the parameters influencing your design. Specify it properly and you can avoid many of the headaches usually associated with control system design. Ignore it, and the results can range between an inefficient, over-specified solution at best, to a cripplingly expensive re-design later on. ●

Imagination Technologies

Durgesh Patel, Senior Design Engineer

Mark Dunn, VP Engineering with Simon Payne, CEO XJTAG

Graham Deacon, Director of Verification

Imagination develops SoCs faster using XJTAG boundary scan

"Imagination Technologies, a leading IP innovator, is using XJTAG boundary scan to accelerate development of System-on-Chip designs based on industry-leading multimedia IP. Using the system to debug early test hardware, engineers are able to develop tests even before prototype boards are delivered, and to identify any manufacturing flaws within minutes before commencing design verification."

Imagination Technologies provides comprehensive System-on-Chip (SoC) design services including fully bespoke solutions or standardised platform implementations, based on Imagination's industry-leading IP portfolio. The IMGworks group develops complete SoC solutions using Imagination's IP cores, and works with chip companies as well as leading consumer-product brands targeting mobile- and multimedia-products markets.

"We have developed a state-of-the-art design flow, to provide a fast and low-risk path to production for our customers, says Mark Dunn, VP of Engineering at IMGworks. "Speed is vital, as our customers are typically aiming for a very short market window and rely on us to help them beat their competitors to market."

As a part of its IP development flow, Imagination builds small numbers of boards and test chips for verification purposes, and also produces development systems as necessary for specific customer contracts. The hardware is usually complex, typically having high I/O interconnect density with complex FPGAs and many signals running on internal layers that cannot be probed. "When the first prototypes come back from manufacturing, everything is new: the board, the software, the chip design," explains Graham Deacon, Director of Verification. "Obviously we want to start design verification quickly, so we need a fast way to track down any production defects."

Historically, Imagination's engineers have used socket-based testing to identify hardware faults. This has involved configuring the FPGA to carry out functional tests. Connectivity is very difficult to check in any other way, according to Deacon. In practice, however, significant resources must be committed to develop effective board-level tests by changing the function of the board. "It can involve a couple of weeks of effort," he suggests.

A faster and more efficient approach was needed, but although the team at Imagination had knowledge of various boundary scan test systems, only XJTAG offered the functions and ease of use they were looking for. "XJTAG's engineers demonstrated the system using our own assemblies, which gave us complete confidence that we could quickly produce the tests we need," says Mark Dunn.

Imagination is now using XJTAG to test and debug prototypes, test assemblies and customer development boards. Highlighting the system's convenient and powerful features such as the built-in connectivity test, Graham Deacon explains that connectivity testing and further tests using XJTAG are performed directly after the initial power check on any new board. "XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready." Test execution time is usually around 10 minutes, and the tests filter out the majority of assembly flaws, whereas socket-based tests used to take over one hour to execute.

"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible for debugging in the laboratory. It's a powerful engineering tool, which is perfect for our requirements," says Dunn.

opinion

Mark Dunn
VP Engineering, IMGworks
Imagination Technologies

"XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready. Testing with XJTAG is our first action after the initial power-up check of a new board, and we are able to test a high proportion of each board for any manufacturing defects within around ten minutes."

"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible in a lab debug environment. It's a powerful engineering tool."

Data Bank

Imagination

Company	Imagination Technologies
Nature of business	Flexible and customizable IP for customer SoC applications
Main product	POWERVR, META, and ENSIGMA IP core technology families
Customers	Consumer electronics markets such as digital radio & audio, mobile phones, personal media players, navigation & driver information, mobile internet devices, digital TV & set top box, mobile TV...
Location	HQ Kings Langley, UK Offices in Far East, India, USA
Web site	www.imgtec.com

MAKING SENSE OF CURRENT SENSE TRANSFORMERS

PAUL LEE, DIRECTOR OF BUSINESS DEVELOPMENT AT MURATA POWER SOLUTIONS UK, DESCRIBES SOME PITFALLS TO AVOID AND TECHNIQUES TO EMPLOY TO ACHIEVE BEST PERFORMANCE IN CURRENT SENSE TRANSFORMERS. HE USES A HIGH-FREQUENCY CURRENT TRANSFORMER AS AN EXAMPLE BUT THE PRINCIPLES APPLY EQUALLY AT LOW FREQUENCIES

Current sense transformers (CTs) are commonly used for monitoring, control and protection, and can be as simple as a single winding on a toroidal core to sense the current in a wire passing through the core.

A CT operates in exactly the same way as any magnetic transformer and follows the basic rules that voltage and current are transformed in the ratio of the primary and secondary winding turns; load impedance is transformed in the ratio of the square of the turns; and the volt-second product applied to any winding must average zero over each switching cycle.

Figure 1 shows a schematic of a CT. It depicts a simple two-winding ideal transformer with infinite secondary inductance, zero winding resistances, perfect coupling and no parasitics. As such, if terminated with a pure resistance, it would have a response from the slowest varying DC to any high frequency at any current with no losses or distortion.

A real CT (shown in Figure 2) has a finite value of magnetising or winding inductance L*m* and the parasitic components of leakage inductance L*lk*, winding resistances R*p* and R*s*, coupling capacitance C*c*, winding self-capacitances C*p* and C*s*, and core loss R*loss*. R*f* is the secondary impedance reflected on the primary. The core can also magnetically saturate. These practical characteristics, which interact with the external circuit, limit the performance of the CT, summarised by its accuracy $\frac{V_b}{I_t}$ or ability to reproduce a perfectly scaled representation in voltage V*b* of the primary current I*t* when terminated with a resistance R*b*.

Low frequency accuracy is defined by the magnetising inductance L*m*, secondary winding resistance R*s* and burden resistor R*b*. This is because R*s* in series with R*b* reflects to the primary of the transformer in the square of the turns ratio *n* and appears in parallel with L*m* as:

$$R_f = \frac{R_b + R_s}{n^2}$$

The sensed current I*t* therefore divides R*f* and L*m* with only the partial current through R*f*, reflecting the current through R*b* and indicating a lower than expected value. As the frequency reduces, so does the impedance of L*m*, increasing the error. Current through L*m* does not appear in the transformer's secondary winding.

Current Loss

So how much current is 'lost' through L*m*? If the measured current is a sine wave then the current splits in the ratio of the complex impedance R*f* to the impedance of L*m* = ωL*m*. Manipulation of the relationships gives the following result for accuracy $\frac{V_b}{I_t}$:

$$\frac{Vb}{It} = \frac{R_b}{n}\left[\left(1 + \frac{L_{lk}}{n^2 L_m} + \frac{R_s}{R_l} + \frac{R_b}{R_l} + \frac{\omega^2 C_s R_b L_{lk}}{R_l} + \frac{C_s R_b R_s}{L_m n^2}\right) + j\left(\omega R_b C_s + \frac{\omega R_b C_s L_{lk}}{n^2 L_m} + \frac{\omega C_s R_b R_s}{R_l} + \frac{\omega L_{lk}}{R_l} - \frac{R_s}{\omega L_m n^2} - \frac{R_b}{\omega L_m n^2}\right)\right]^{-1} \quad (1)$$

Inspection of the equation shows that accuracy tends to $\frac{R_b}{n}$, the ideal result, at mid frequencies, where ωL*m* n^2 >> R*s* or R*b* and if C*s* and L*lk* are small and R*loss* high. At lower frequencies, the terms $\frac{R_s}{\omega L_m n^2}$ and $\frac{R_b}{\omega L_m n^2}$ begin to dominate and accuracy suffers. However, this can be counteracted by reducing R*b*. This is shown graphically in Figure 3 using the Murata Power Solutions 53200C 200:1 CT as an example, which has L*s* = 8mH, C*s* = 30pF, L*lk* = 50µH and R*s* = 34Ω. Accuracy is plotted for burden resistors R*b* of 50, 100 and 200 ohms, with the Y axis volts-per-amp scale normalised to unity. The improvement in low frequency bandwidth with reducing R*b* can be clearly seen. The phase advance from sensed current to indicated voltage is also plotted, see Figure 4.

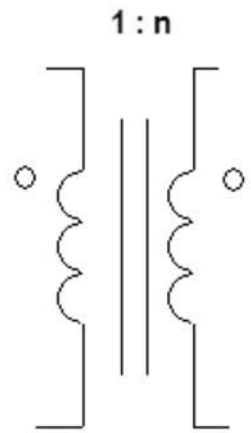

Figure 1: An 'Ideal' CT

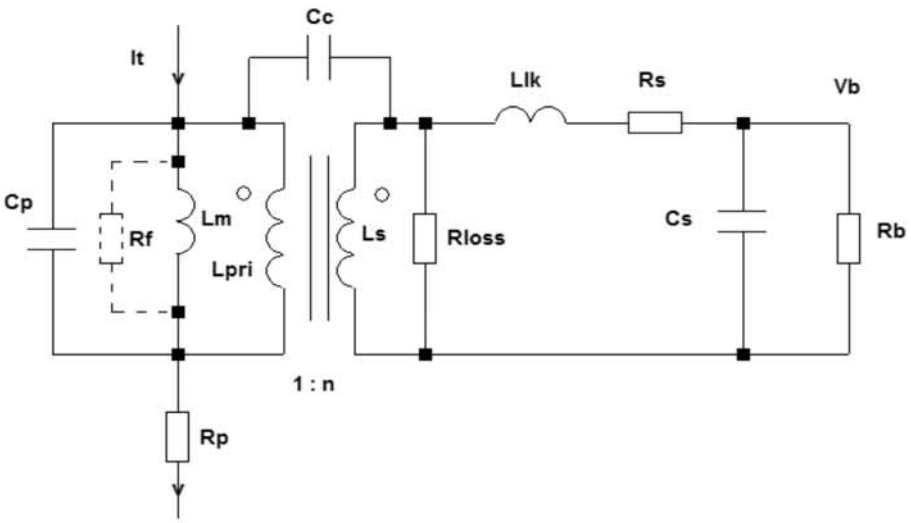

Figure 2: Real CT with parasitics and termination Rb

The low frequency bandwidth limit is also where the core begins to magnetically saturate. A version of Faraday's law can be used to derive flux density B from voltage, core cross-sectional area A*e* and winding turns n:

$$B = \frac{V_{rms}.10^6}{4.44\,F\,A_e\,n} \quad (2)$$

Substituting in our equation for accuracy, rearranging and ignoring high frequency terms, the maximum rms current before saturation occurs can be expressed as:

$$I_{tmax} = \frac{B_{sat}R_b\omega A_e n_{sec}}{\sqrt{2}Acc(R_b+R_s)10^6} \quad (3)$$

where B*sat* is the maximum flux density for the material used, typically 0.4 Tesla, and Acc is the accuracy computed in Equation 1 for the frequency in question $F = \frac{\omega}{2\pi}$. This is plotted in Figure 5, showing that saturation occurs well below the rated bandwidth but again improves with reducing R*b*. The maximum current of 10A within the rated bandwidth of this product is a thermal limit. B*sat* does decrease with temperature, typically by about 20% from 25 Celsius to 100 Celsius, which should be allowed for. Note that the sensed current itself does not directly cause saturation as it ideally transforms to burden resistor current rather than magnetising the core. It is the 'diverted' current into the magnetising inductance that causes saturation.

At higher frequencies, C*s* and the decreasing effective value of R*loss* start to shunt away current from R*b* and the accuracy falls. C*s* can be minimised by making the secondary winding a single layer, which is easier with fewer turns, arguing for selection of CTs with lower turns ratios, perhaps 50:1 for best high-frequency performance. Core losses depend on the material and increase exponentially with frequency at constant flux density but are mitigated by the fact that flux density decreases linearly with frequency, everything else being equal. It can be expected that the permeability of the ferrite falls off with increasing frequency-reducing inductance, but this has minimal effect.

Lower values of R*b* also improve the high frequency bandwidth, as can be seen in Figure 3. It can be seen that the rated high-frequency bandwidth of this part, 500kHz, is very conservative with a useful response up to several megahertz, especially with a lower burden resistor value.

Improvement Techniques

It is clear that a low value of burden resistor directly improves low and high frequency bandwidth, so what is the disadvantage of reducing R*b*? Simply that less voltage is developed across it for the same sensed current, perhaps making the circuit more prone to noise pickup. In some situations, CT reset time can be affected adversely (see later).

If the primary current is a unipolar or bipolar square wave, the 'lost' current into the magnetising inductance increases from zero with time according to I*m* = Et/L*m*, where E is the decreasing voltage dropped across the corresponding decreasing current through R*f* with time t. The effect is, therefore, not linear and V*b* follows the relationship:

$$V_b = \frac{I_t R_b L_{sec}}{n(t_{on}(R_b+R_s)+L_{sec})} \quad (4)$$

The practical effect of this is to show an exponential 'droop' at the top of the voltage waveform V*b*. From the

relationship it can be seen that reducing R*b* or increasing L*sec* lessens the amount of droop in a given time. Using the Murata 53200C CT again as an example, with a square wave sensed current of 10µs duration, its recommended value for R*b* = 200Ω gives 22.6% droop while R*b* = 50Ω gives just 9.5%, shown in Figure 6.

A more common sensed-current waveform has a rising, approximately linear current superimposed on the square wave, as shown in Figure 7. The rising current could for example be magnetising current in a flyback transformer or reflected output storage inductor current in a forward converter transformer. When the droop effect is added to these waveforms, it could be that the voltage across R*b* still shows a net decrease, representing a problem if the circuit is intended to detect overcurrent above a certain level. Also, in current mode control of switched-mode converters, droop must be limited to give a net positive slope for V*b*, necessary to initiate switch turn-off. Note that the amount of droop is, in turn, affected by the positive slope of the sensed current itself with the accuracy of the voltage V*b* now given by:

$$V_b = \frac{(I_{tk}+\frac{di}{dt}t_{on})R_bL_{sec}}{n(t_{on}(R_b+R_s)+L_{sec})} \quad (5)$$

where I*tk* is the starting value of the rising current with slope $\frac{di}{dt}$ (A/µs). Figure 7 shows an example of the 53200CT with a 1A step current rising linearly to 2A over 10µs. The plot 'Droop, R*b* = 200R' is that which would occur with a constant 1A sensed current.

Applying Equation 5 shows that the resultant slope of the V*b* waveform is actually lower than that given, by simply adding the droop and rising sensed current calculated separately, requiring perhaps less droop to be tolerated to give a net positive slope for V*b* if the $\frac{di}{dt}$ of the sensed current were less. Remember, the droop is actually exponential so the slope of the waveform at V*b* tends to a constant, higher value over time.

A more realistic waveform for a pulsed current with rising peak value is shown in Figure 8, with skew and ringing on the rising and falling edges.

The Effect Of R*b* On Bandwidth

As expected from the analysis of the effect of R*b* on bandwidth, reducing R*b* reduces the edge skew somewhat. The inherent values of C*s* and L*s* have an effect, although ringing is damped by R*b* and core losses. Skew caused by L*s* is the time it takes for the current through it, I*s*, to reach the settling value, nominally $\frac{It}{n}$. This in turn is driven by the voltage across L*s* during the skew time according to $\frac{dIs}{dt} = \frac{E}{Ls}$.

E is driven from the primary voltage by the turns ratio, varying and not very determinate, depending on the source impedance of the external driving circuit and its compliant voltage.

Coupling capacitance C*c* rings with L*s* if the primary and secondary of the transformer share the same ground, or if the grounds have significant mutual capacitance, which is commonplace. If this represents a problem in the circuit, toroidal current sense transformers with a single primary turn such as the Murata Power Solutions 5600C series can have lower values of C*c* than bobbin-wound types, such as the 5300C series.

With pulsed square wave currents, low-end bandwidth, effectively the maximum pulse width allowed, T*onmax*, is dependent on what droop or inaccuracy can be tolerated in the V*b* waveform and, ultimately, the saturation of the transformer core is given by:

$$T_{onmax} = \frac{B_{max}A_e}{V_p} \quad (6)$$

The primary voltage V*p* depends on the chosen value of R*b* and sensed current I*t*, and decreases as I*t* diverts increasingly into magnetising current with time. Including this effect T*onmax* for a square-wave-sensed current is given by:

$$T_{onmax} = \frac{B_{max}n^2A_en_{pri}L_{sec}}{I_tL_{sec}(R_b+R_s)-B_{max}n^2A_en_{pri}(R_b+R_s)} \quad (7)$$

A sensed current with rising value $\frac{di}{dt}$ from an initial value of I*tk* yields the quadratic:

$$T_{onmax}^2L_{sec}(R_b+R_s)\frac{di}{dt} + T_{onmax}\left(L_{sec}(R_b+R_s)I_{tk} - B_{max}n^2A_en_{pri}(R_b+R_s)\right) - B_{max}n^2A_en_{pri}L_{sec} = 0 \quad (8)$$

Using the example of the 53200C CT, for a sensed current of 10 A, T*onmax* calculates to be 23µs, 40µs and 63.5µs with R*b* = 200, 100 and 50 ohms respectively. If the current has a rising value $\frac{di}{dt}$ of 0.1A/µs from the initial value of 10A, from Equation 8, T*onmax* decreases to 21.1µs.

Even if a CT is used within its rated bandwidth and current, consideration must be given to the duty cycle of unipolar sensed current.

Flux in any transformer must be allowed to return to zero or 'reset' between successive pulses, otherwise residual flux adds on successive cycles and can ultimately cause 'staircase saturation' of the core.

CTs fed with symmetrical sine waves or bipolar pulsed currents do not suffer from the problem since flux is actively driven to equal positive and negative values each switching cycle. The CT primary will often be

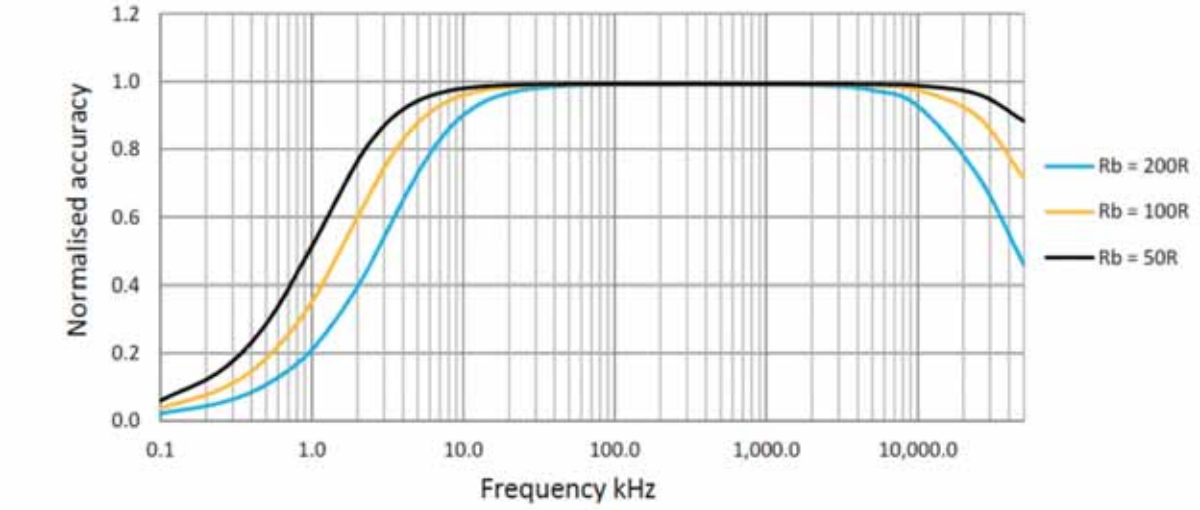

Figure 4: Bandwidth - Murata 53200C CT

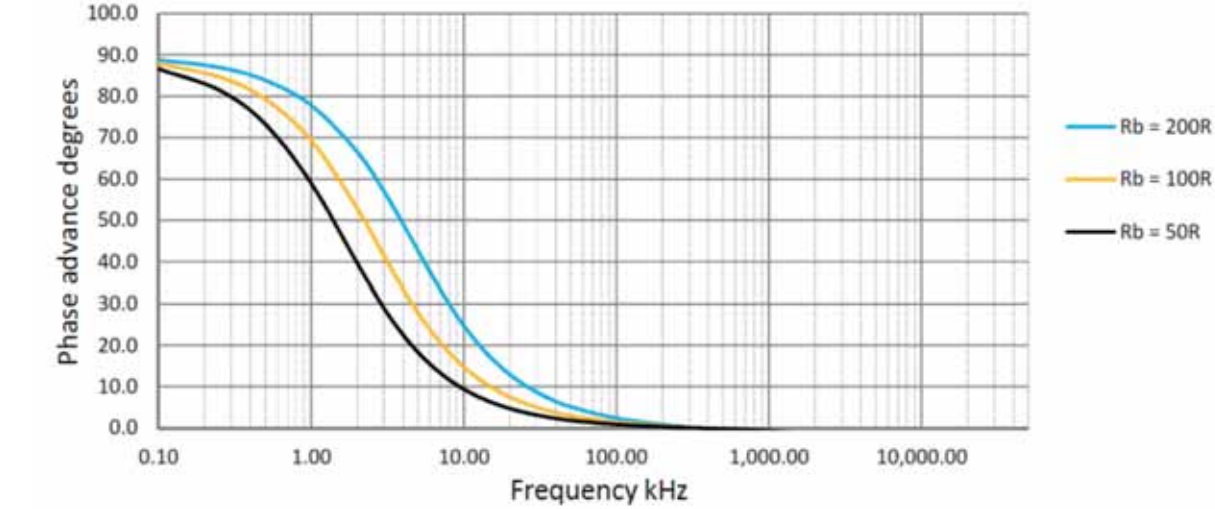

Figure 4: Phase advance It to Vb - Murata 53200C CT

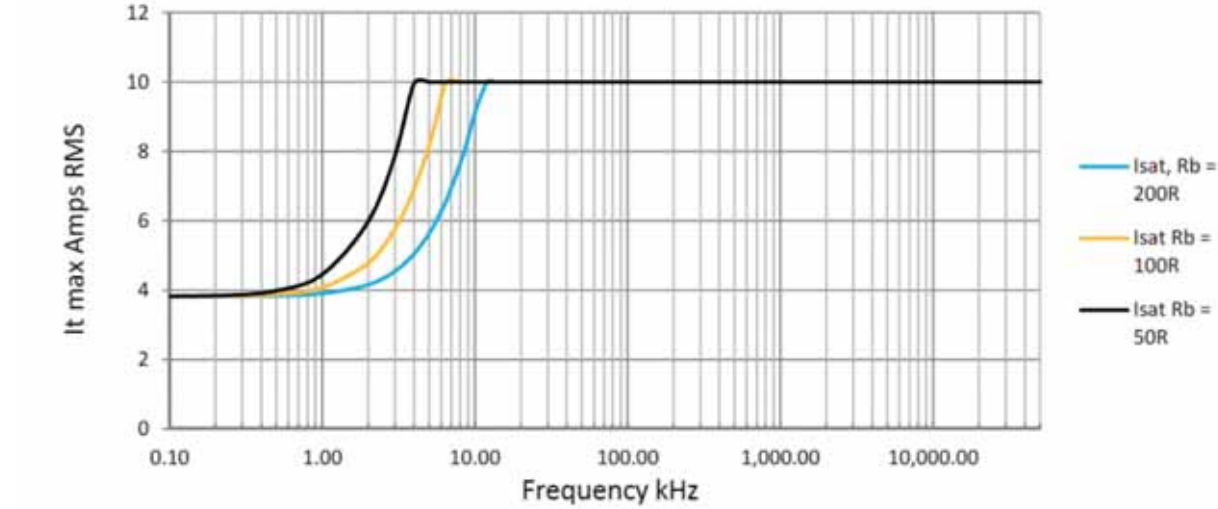

Figure 5: Maximum primary current - Murata 53200C CT

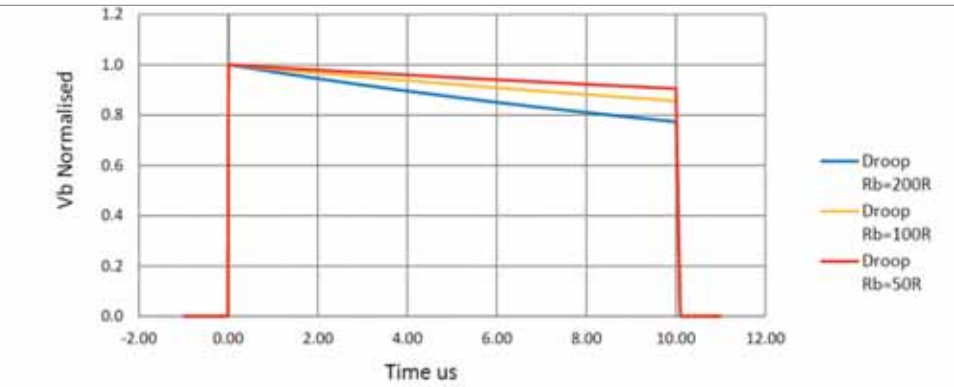

Figure 6: 'Droop', Murata 53200C CT

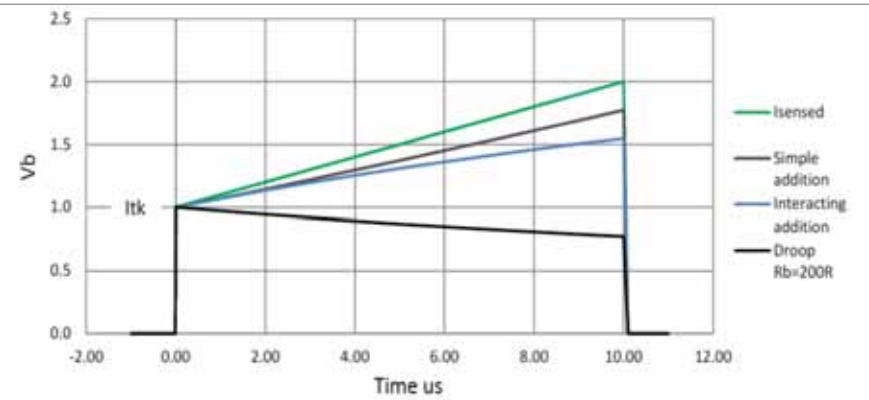

Figure 7: Droop and Sensed current interacting - Murata 53200C CT

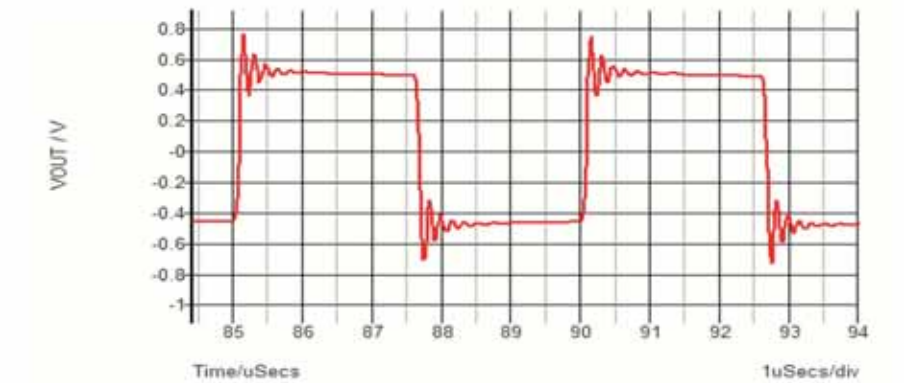

Figure 8: Ringing and skew on edges

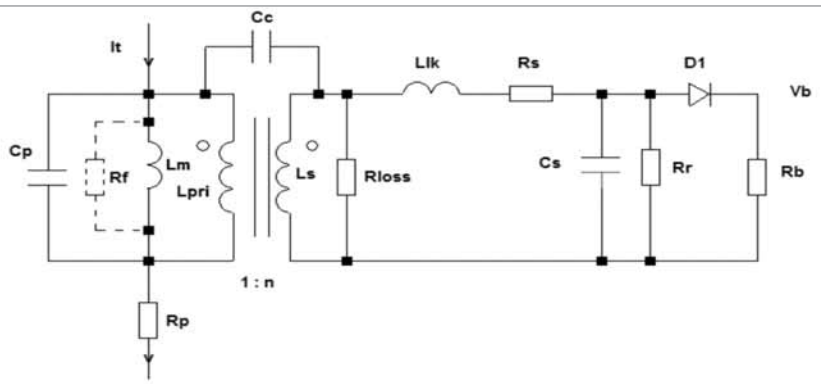

Figure 9: Sensing unipolar waveforms

coupled through a capacitor to guarantee that volt-second equality is always preserved and that there is no net DC through the sense winding.

Core Energy

In the circuit of Figure 2, when the sensed current goes to zero, energy in the core $\frac{1}{2}L_m I_m^2$ generated by the magnetising current causes both winding voltages to reverse; the resistive path on the secondary winding provides a route for current to continue to flow and energy to dissipate in R*b* and R*s* and in core losses. The secondary current starts at value $(-)\frac{I_m}{n}$ and rises exponentially to zero, with time to a final current given by:

$$t_{final} = \frac{L_s}{R_s+R_b} ln\left(\frac{i_{initial}}{i_{final}}\right) \quad (9)$$

The reset time can be lengthy; for example, for the 53200 CT with a burden resistor of 200Ω, the time for the reset current to fall to 10% of its initial value is 78µs. This time is so long that the effects of C*s*, R*loss* and L*lk* are negligible. This is an example of where reducing the value of the burden resistor does not produce a beneficial effect.

In practice, unipolar current waveforms are sensed with the circuit of Figure 9. Here a diode blocks the reset current and R*r* can be a high value giving fast reset, as long as there is also no reset current path around the primary of the transformer. The practical limit is that the secondary reset voltage increases in proportion and must be kept within the reverse breakdown limit of D1.

In real circuits, the secondary winding capacitance sinks current and limits the speed of reset, and also limits the voltage during reset. If all the magnetising energy from the transformer resonantly transfers to the capacitor, the maximum possible peak voltage V*r* is:

$$V_r = \frac{i_m}{n}\sqrt{\frac{L_s}{C_s}} \quad (10)$$

For our example CT, with L*s* = 8mH, n = 200, C*s* = 30pF, and for a primary magnetising current of 2A peak, the secondary reset voltage V*r* would be 163V.

It would be tempting to leave out R*r* altogether and just ensure that D1 could stand 163V reset plus any cathode voltage for minimum reset time. Remember, however, that the reverse voltage also appears on the primary winding by transformer action, in this case:

$$(-)\ \frac{163}{n} = -0.815\ V.$$

If, for example, the CT were in the emitter of a bipolar transistor or low threshold MOSFET, held off by 0V on its base or gate, this voltage could turn on the transistor, possibly with disastrous consequences.

The effect is exacerbated by the fact that D1 adds to the R*b* voltage drop reflecting to the primary, causing additional magnetising current and, hence, reset voltage according to Equation 10, compared with the bipolar sensing arrangement of Figure 2. A Schottky diode is often preferred for D1 for this reason, but itself has limited reverse-voltage capability. A fast recovery diode should anyway be used, since the recovery current acts to delay reset.

As an example, Figure 10 shows the simulated resonant reset achieved with the circuit of Figure 9 with R*r* = 10kΩ and with 1N4148 and 1N4003 diodes showing the effect of the long recovery of the 1N4003. The plot is the voltage on the secondary of the CT with a 10V, 5µs positive pulse followed by reset. Equation 9 gives the time for reset current to fall to a specified value with (R*b* + R*s*) replaced with (R*r* + R*s*), so now with D1 fitted and R*r* = 10k, under the same conditions, reset reduces from 78µs to 1.8µs. Other reset schemes are possible including forcing reset current from an external supply to achieve duty cycles of greater than 95%.

In summary, commercially available current sense transformers are characterised under specific conditions. Being aware of the effects of termination impedance and associated components can enable the designer to optimise his performance for best accuracy over the widest frequency or pulse width range often exceeding the headline specifications of the part.

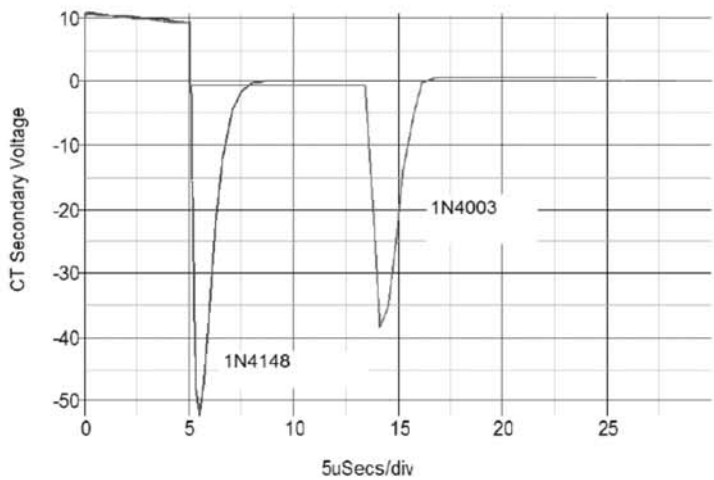

Figure 10: Reset with fast and slow diodes

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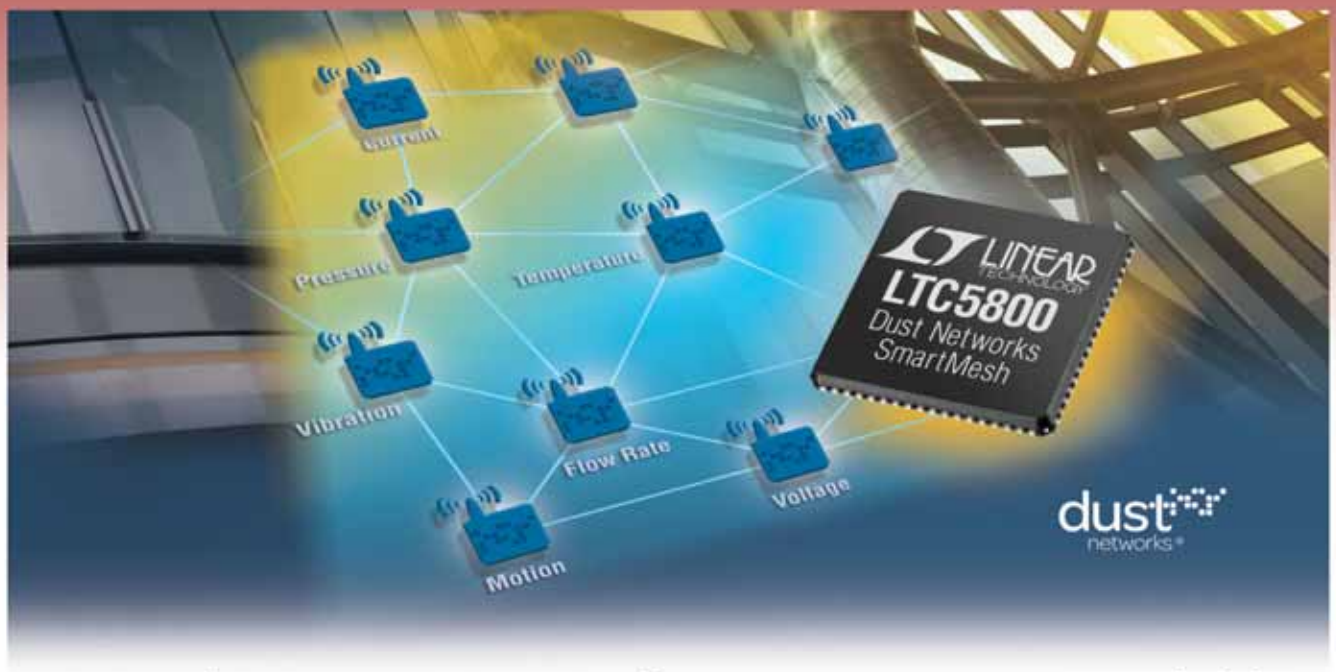

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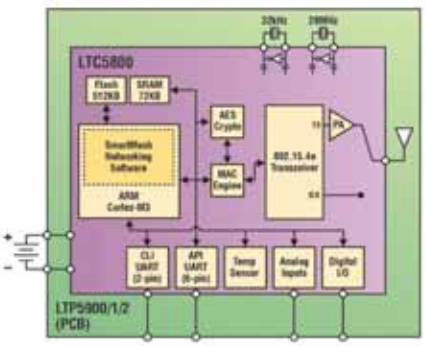

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FREE 3D DESIGN TOOL SAVES TIME AND MONEY FOR ALL ENGINEERS

There are many challenges faced by engineers today, and the common thread that links them is 'time': lack of time caused by a higher volume of projects, shorter time-to-market windows, and shrinking engineering departments leading to a loss of specialist knowledge and skills.

At the same time, the relationship between the electronic and the mechanical design engineer has evolved. Whereas 15 years ago these two functions were distinctly separate, today's end products are much more focused on aesthetics, which has led to the circuit and the mechanical aspects, such as case design, being done in parallel.

This merger of the engineering disciplines has introduced complexities to the design flow that can result in major bottlenecks, often adding weeks or more to a project. Access to tens of thousands of freely downloadable 3D models, which RS has offered for some three years now, has gone some way to help claw back this lost time, with each model download potentially saving the engineer up to two days of manual creation. And yet, only 5% of the world's engineers currently have access to powerful 3D modelling tools, largely limited to CAD specialists who have trained for many months, or even years, to become conversant with the complexities of traditional feature-based 3D CAD tools. This low figure is no surprise when you consider the prohibitive costs of these tools, which restricts their use to larger companies with the budget to invest in them.

Thanks to a recent collaboration between RS Components and 3D modelling software vendor, SpaceClaim, these two major barriers to entry have been lifted through the availability of DesignSpark Mechanical, a 3D solid modelling and assembly tool that is simple to use and totally free of charge.

DesignSpark Mechanical employs a powerful methodology called 'direct modelling', which is very different from traditional feature- or parametric-based 3D CAD software. The tool uses simple gestures that enable real-time editing and instant feedback, making it possible for engineers and others to create geometry and easily explore ideas and product concepts in 3D. All basic designs can be achieved quickly and easily via the use of the software's four basic tools – Pull, Move, Fill and Combine – in addition to its employment of familiar Windows keyboard shortcuts such as cut/paste, undo/redo, which makes it highly intuitive for new users.

The software can also be used as a complementary 3D tool in the product development process for the creation of early concept designs, for instance, alongside 3D CAD tools that are already in use today. The tool can remove bottlenecks in the early design process by allowing changes and additions in seconds, rather than having to wait for the CAD department using the traditional 3D tools to rework the design.

3D designs can also be exported in STL, the standard file format to enable rapid prototyping builds through 3D printers and computer-aided manufacturing, in addition to providing the ability to quickly obtain Bill-of-Materials (BOM) quotes via the RS website. The tool can also import circuit layout files in IDF format from any PCB design tool, including the award-winning DesignSpark PCB software.

DesignSpark Mechanical has been developed to be inclusive. Any engineer, regardless of experience, can learn to use it quickly, and it costs absolutely nothing. Available in multiple languages, the tool enables engineers all over the world to bring innovative products to market quickly, avoiding the bottlenecks that so frequently stifle creativity.

DesignSpark Mechanical is available for free download via www.designspark.com/mechanical with support available through the DesignSpark community at **www.designspark.com.**

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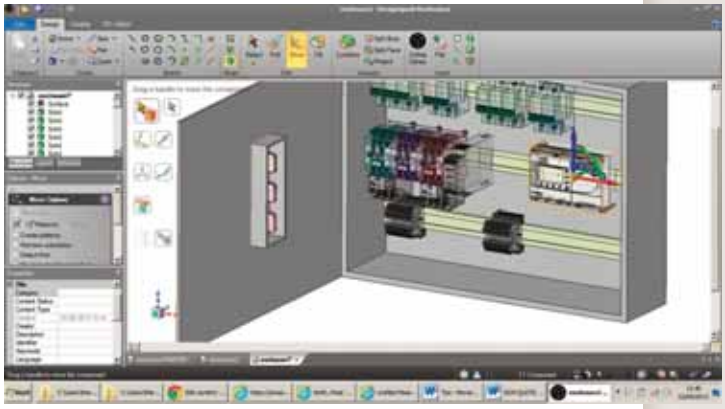

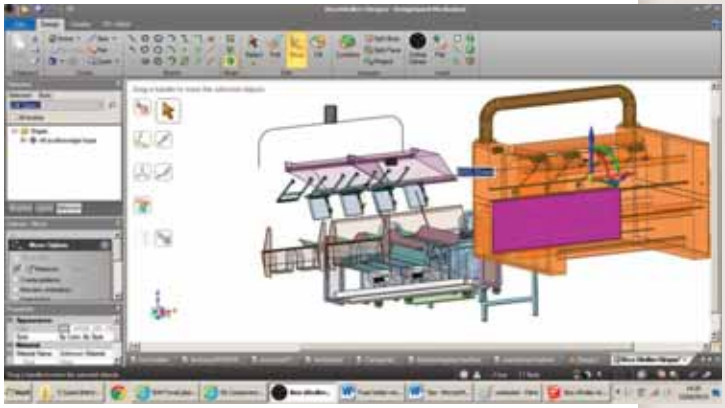

SMART SENSOR CONTROL

RICH MIRON FROM THE DIGI-KEY TECHNICAL CONTENT TEAM OUTLINES THE KEY REQUIREMENTS TO CONSIDER IN THE DESIGN OF ACCURATE SENSING SYSTEMS

The growing demand for sophisticated monitoring and automation, from the home to the high seas, calls for efficient and effective techniques for connecting large numbers of sensors and actuators to a host system that may range from a few meters distant to hundreds of miles away.

Industrial controls have traditionally heavily relied on sensors to detect metrics like position, temperature or pressure for controlling various processes such as chemical production, filling of containers or mechanical assembly tasks. As companies seek to reduce human intervention to improve quality and reduce headcount for lower costs, there is increased demand for sensors.

Adding further to this demand, large numbers are being deployed in applications and locations where typically they have not been used. The smart building phenomenon is one example; it is becoming more common for offices, factories and even private homes to incorporate networks of sensors that detect human presence, ambient light, room temperature and air quality, enabling controllers to optimize lighting, HVAC (heating, ventilation, and air conditioning) and other settings for comfort and energy efficiency.

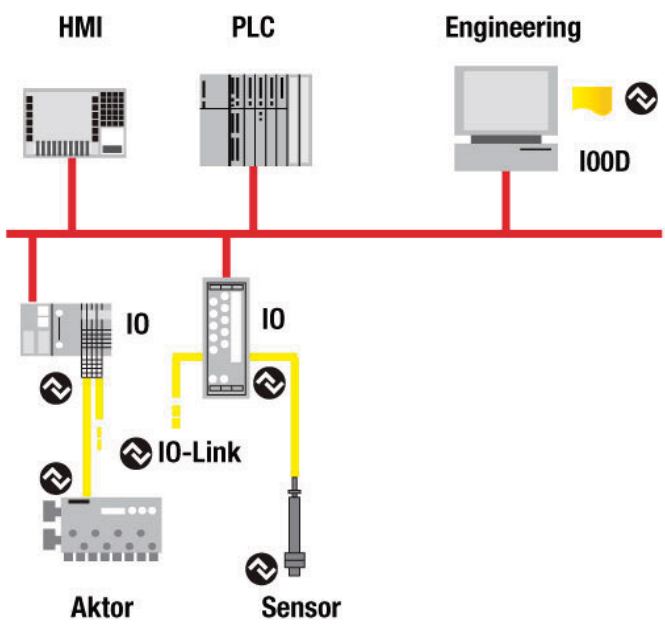

Figure 1: IO Link simplifies sensor interconnections in a number of ways, including allowing the use of standard cables

Simplifying Connectivity

With growing reliance on increasing numbers of networked sensors, in controlling industrial processes for example there is a need for more efficient and practicable techniques for connecting sensors to the host system.

IO Link (Figure 1) is standardized as IEC 61131-9 and allows for point-to-point connections between sensor/actuator devices and a master connected to a network such as Ethernet or Profibus. A master may have multiple ports, each providing a connection for one IO Link device.

IO Link provides for smart interactions between the master and the device, allowing user-controllable frame lengths from 2 to 32 bytes and a range of data rates. Device parameters are stored on the master, simplifying replacement of a failed device with an identical unit. In addition, the device contains an IO Device Description (IODD) file with manufacturer and functionality information, as well as an internal device ID, which comprehensively identifies the device to the master.

IO Link specifies a 3-wire connection to the device, which enables standardization of cable assemblies and interfaces for connecting various types of sensors and masters from different manufacturers.

An IO Link sensor or actuator may contain an IC such as the Maxim MAX14821 IO-Link device transceiver, which acts as the physical layer interface, operating in conjunction with a microcontroller running the data-link layer protocol. Similarly, the MAX14824 IO Link master transceiver provides a physical link layer for use in master controllers. In-band SPI addressing and selectable SPI addresses enable this device to be used for connecting up to sixteen devices. Its 12MHz SPI interface ensures low latency in such high port-count applications.

Smarter Sensors

Sensors and transducers can become smart devices with the inclusion of a microcontroller, implementing functions such as calibration, signal processing and more sophisticated capabilities that offload decision making from the central controller. Figure 2 illustrates the main sensing, signal conditioning, microcontroller and network-interface functions of a temperature sensor using a thermocouple or Resistance Temperature Detector (RTD).

A key challenge when designing sensors, particularly for industrial applications, lies in capturing and conditioning the very small-amplitude signals produced by the sensing element. In particular, industrial applications tend to be subject to high levels of electrical noise and surge voltages that require precision analog circuitry to convert the raw sensor output to a digital signal that can be accepted by the microcontroller or digital signal processor. TI has a number of analog front-end ICs for various sensing applications,

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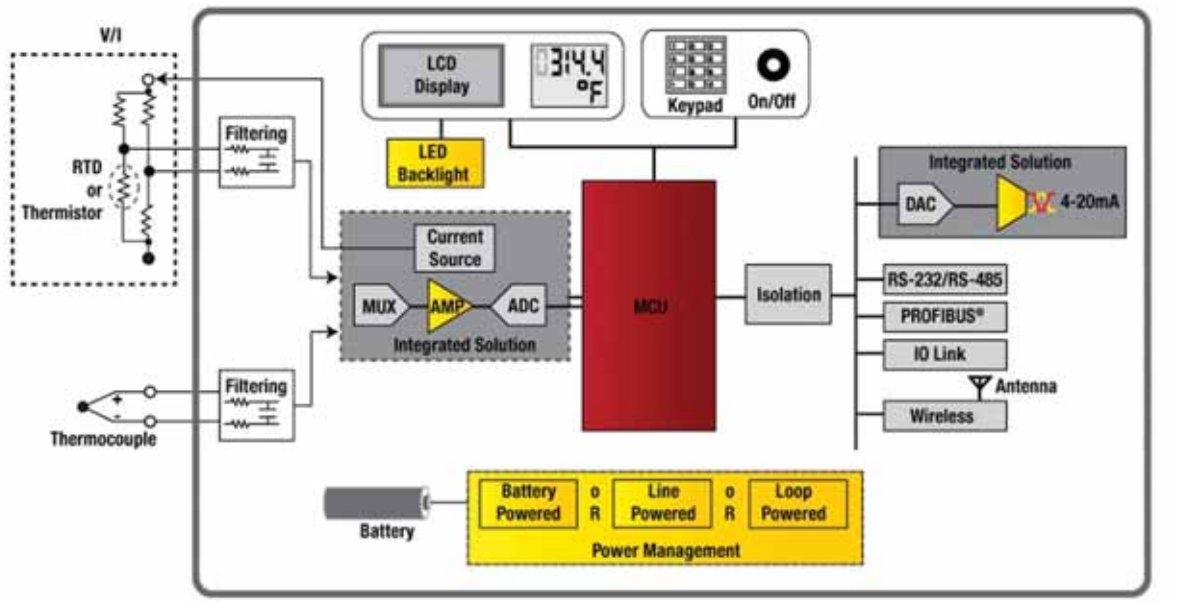


Figure 2: Smart-sensor architecture featuring precision analog front-end circuitry

including temperature sensing, which provide a single-chip solution to this challenge.

The ADS1248 24-bit 2ksample/s analog-to-digital converter (ADC) is optimized for use in temperature sensors and integrates a low-noise programmable gain amplifier (PGA), a precision ADC with digital filter and a low-drift voltage reference. A precision current source is also integrated, which can be used to supply a thermistor or other RTD-type temperature sensor. A microcontroller can be used to handle the network interface and host communications, as well as other functions such as a local display, if needed.

Similarly, TI offers the PGA309 voltage-output programmable sensor conditioner, which is optimized for use with bridge-excitation type sensors, such as piezo-resistive or ceramic film pressure sensors. It features built-in circuitry to compensate for sensor linearization errors, span, offset and temperature drift, and calibration. It is also able to detect if the sensor develops a fault.

TI also has a variety of discrete, precision ADCs such as the ADS1274, capable of up to 144ksamples/s, allowing use with sensors such as flow meters.

Standardizing Interfaces

There are, however, some barriers to the rapid development of smart sensors and, hence, the growth of the smart-sensor market. These include various incompatibilities between sensing materials or techniques and microelectronic circuitry, which can prevent close integration or co-packaging of the sensor and smart circuitry.

Perhaps more important is the fact that sensor producers may not want to build multiple variants for connecting to numerous network standards such as Ethernet, Profibus or others. Indeed, the sensor builders may not want to deal with network-connectivity aspects at all.

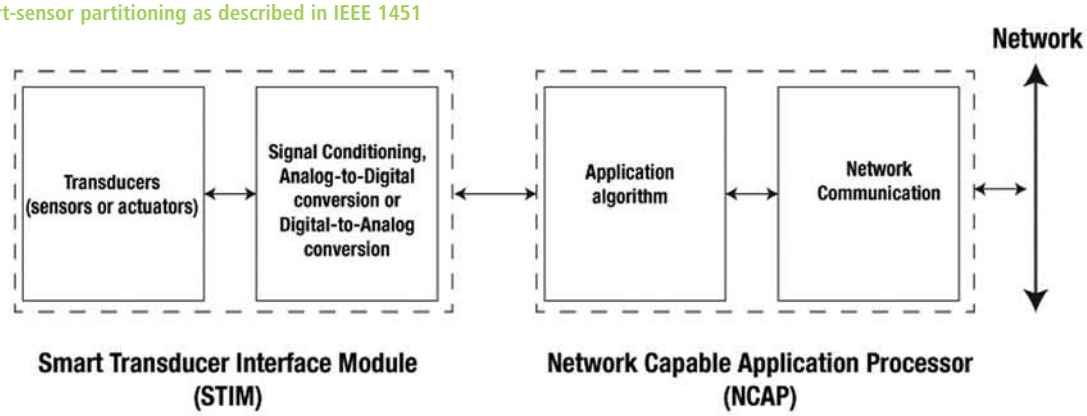
The IEEE 1451 standards were developed to address these types of issues, proposing standardized interfaces between the sensing and network-connectivity functions of a smart sensor. Figure 3 illustrates how the IEEE 1451 initiative models and partitions the sensor to allow such standardization.

Partitioning the sensor effectively enables a compliant sensor module from any manufacturer to plug into a compliant network-interface module from any other manufacturer. The network-interface module may support Ethernet, Profibus or another type of connectivity. In addition, the IEEE 1451 framework proposes a standard Transducer Electronic Data Sheet (TEDS), to be contained within the transducer module, which describes the transducer to the host network. Hence, the resulting unit comprising the smart-sensor and network-interface modules can connect directly to the network as a plug-and-play unit. This can reduce human error when connecting sensors to the network, simplify installation and maintenance of smart-sensor networks, and allow sensors to be replaced or upgraded quickly and easily with minimal downtime.

> A key challenge when designing sensors, particularly for industrial applications, lies in capturing and conditioning the very small-amplitude signals produced by the sensing element

Various aspects and principles of IEEE 1451, particularly the TEDS and STIM standard, have been employed in commercial sensor products to facilitate smart interfaces and network connectivity. IEEE 1451 also provides the basis for the Java Distributed Data Acquisition and Control (JDDAC) platform, which enables Java applications to connect to a wide variety of sensors and actuators.

Figure 3: Smart-sensor partitioning as described in IEEE 1451



Long-Range Connectivity

With a suitable network interface, smart sensors are able to communicate using a diverse range of standards. These may be application-specific, such as Controller Area Network (CAN), Highway Addressable Remote Transducer Protocol (HART), Profibus or an Industrial Ethernet derivative such as EtherCAT. Equally, general-purpose connectivity such as standard Ethernet or Internet Protocol (IP) may be supported. With IP support and an embedded web server, the smart sensor can be connected to the Internet, which provides the opportunity to monitor the device from almost anywhere in the world.

Connecting wirelessly to smart sensors is also desirable for a number of reasons. Within a single industrial site, wireless networking using a standard such as ZigBee permits easy scaling or adaptation of the network without requiring extensive new infrastructure. This may be implemented using an IEEE 802.15.4 radio transceiver, or a smart or wireless microcontroller such as the STM32W family from STMicroelectronics, which contains a 32-bit ARM Cortex-M3 microcontroller and integrated IEEE 802.15.4 radio.

With the rapid growth of the Internet of Things (IOT) and other applications, such as telematics, requiring machine-to-machine (M2M) connectivity over cellular networks, a variety of embedded modems is available, supporting cellular standards such as GSM, GPRS/EDGE and CDMA, permitting connection to networks used in various territories worldwide.

An embedded modem such as the Multi-Tech MTSMC-C1-N16-SP is a dual-band 800/1900MHz CDMA2000 device that also supports Ethernet and Wi-Fi access and is pre-certified to applicable network standards. It utilizes the standard embedded-modem pin-out established by Multi-Tech, and can be interfaced directly to a UART or microcontroller via a serial connection.

Relying on Smart Sensors

Reliance on smart sensors to help manage resources and enhance productivity will continue to grow. Careful attention to analog design is necessary for accurate sensing. Single-chip AFEs (analog front-ends) are available, which overcome these challenges when working with specific sensor types.

As more sensors are deployed and new sensing scenarios emerge, efficient and error-resistant methods are needed for connecting sensors to networks and central controllers, while allowing monitoring by human supervisors. Careful consideration of the interfaces between smart sensor and network-interface functions, taking advantage of sensor-specific standards and the wide variety of networking and communication standards, allows many types of systems to be monitored and controlled accurately within a local area or across distances of hundreds or even thousands of miles. ●

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VARIATIONS ON THE COMPLEMENTARY FOLDED CASCODE TRANSIMPEDANCE STAGE IN DISCRETE AUDIO FREQUENCY POWER AMPLIFIERS

MICHAEL KIWANUKA EXAMINES SAMUEL GRONER'S ARRANGEMENT AND VARIATIONS OF THE COMPLEMENTARY FOLDED CASCODE TRANSIMPEDANCE STAGE IN DISCRETE AUDIO FREQUENCY POWER AMPLIFIERS, AND EVALUATES THESE AGAINST THE CONVENTIONAL J. E. THOMPSON TOPOLOGY

Some time ago, Samuel Groner published an intriguing paper [1, 2] in which he suggested that the shortcomings in respect of slew asymmetry and power supply rejection of the classical two-stage voltage gain topology (attributed to J. E. Thompson by Messrs Russell and Solomon [3]) may be ameliorated by adopting a complementary push-pull folded cascode arrangement for the second stage.

Groner's arrangement and novel variations thereof are examined here and their performance evaluated against that of the conventional Thompson topology to establish whether the extra complexity is worthwhile.

The Thompson Topology

The circuit in Figure 1 contains the fundamental elements of the majority of modern high-performance voltage amplifiers and, thus, constitutes an invaluable reference against which the merits of alternative approaches may be judged [4]. A thorough appreciation of its virtues and limitations is therefore essential.

It consists of a transadmittance input stage (TAS for concision) in the form of differential pair Q13, Q14, with emitter-degeneration resistors, R2, R4, Widlar's current mirror [5, 6] Q15, Q16 and a so-called tail in the form of amplified negative feedback (ANF) current source Q29/Q30. The TAS is effectively a voltage-controlled current source (VCCS) whose output current is proportional to the differential input voltage. At frequencies preceding the amplifier's first non-dominant pole, input stage transadmittance gain may, with negligible error, be assumed to be equal to its DC transconductance.

The impedance at Q14's collector is negligible, virtually eliminating Miller feedback through its collector-base intrinsic capacitance. This transistor is effectively an emitter follower and, consequently, its comparatively low net input capacitance permits the connection of large feedback network impedances before the pole at its base becomes significant [7].

Emitter degeneration in the TAS (R2 and R4) constitutes series-applied local negative feedback, which trades a measure of transconductance for enhanced linearity, and is conducive for trouble-free stabilisation without mandating the use of an inordinately large slew-rate sapping Miller feedback capacitor across the second stage. The gain block represents the output stage, which is usually a unity voltage gain complementary symmetry buffer of substantial current gain.

The current mirror facilitates differential-to-single ended conversion and forces equality of collector currents in the differential pair [8]. This minimises DC offset at the output of the amplifier and is a necessary requirement for the elimination of second order distortion generated by the input stage [9].

The mirror also doubles the symmetrical current sourcing and sinking ability of the stage over that obtainable with a resistive load. Degeneration resistors R12 and R13 promote equality of currents in the mirror by swamping variations in the base-emitter voltages of its transistors Q15 and Q16.

The ANF active current source Q29/Q30 vastly improves the common-mode and power supply rail rejection ratios of the stage over those attainable with a simple resistive source. However, a resistive load does not amplify its internal noise and, therefore, possess the advantage of producing somewhat less noise than would be generated by the current mirror or active current source.

Capacitor C1 filters out residual power supply ripple in the bias current established by resistors R21 and R29 [10]. The temptation to connect C7 directly across Q30 should be resisted as this would simply couple supply ripple directly into the current source.

The second stage, comprising Q17, Q18 and ANF current source Q19/Q20, is effectively linearised and converted into a near-ideal transimpedance amplifier stage (TIS) by local shunt (voltage) derived-shunt (current) applied (viz. admittance) frequency dependant negative feedback courtesy of the Miller compensation (or stabilising) capacitor.

The TIS is effectively a current-controlled voltage source (CCVS) at the frequencies of interest, and ideally requires infinitely large source and load impedances for maximal transimpedance gain. These conditions are best realised in practice by employing a first-stage current mirror and a high current gain output buffer.

Minor loop negative feedback due to C_c reduces the TIS's input impedance pro rata with increasing frequency, making it negligible (virtually zero) compared to the TAS's output impedance. The local feedback loop also reduces the TIS's output impedance, reducing distortion generated by the non-linear loading of a class-B (or AB) output stage on the second stage [11].

Although the second stage is often [12] referred to as the 'voltage amplifier stage' (VAS), this is technically incorrect, as it

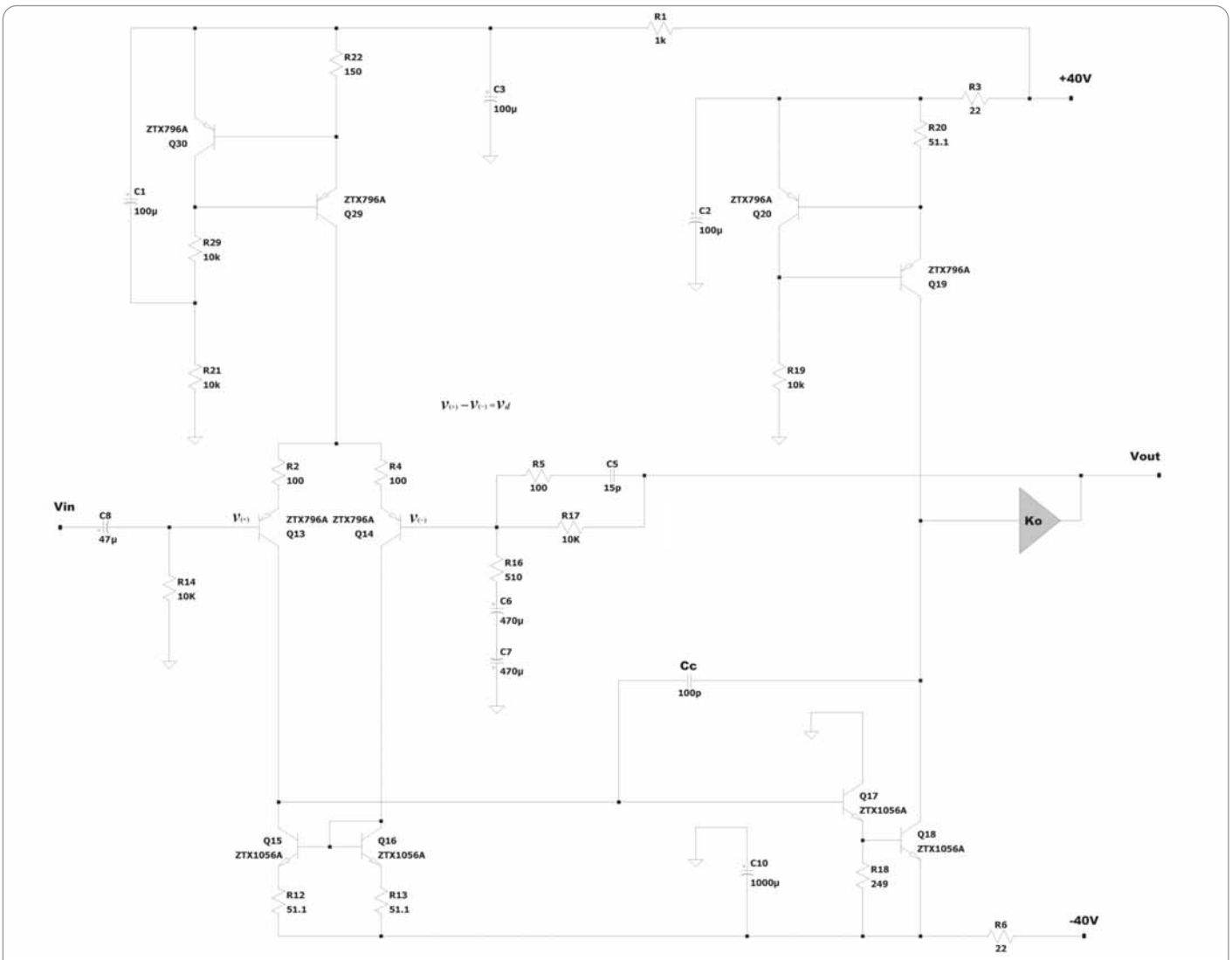

Figure 1: Thompson's two stage topology

implies that the stage is a voltage controlled voltage source (VCVS). In fact, a closed-loop VCVS is synthesised by the application of shunt (voltage) derived-series (voltage) applied negative feedback, which clearly does not obtain with the TIS.

Forward path transimpedance gain local to the second stage is, to a good first approximation, merely the product of its current gain and the effective impedance at its output. Thus emitter follower Q17 increases forward-path gain local to the TIS (and therefore minor loop feedback through) by increasing the second stage's effective current gain.

With this topology and with the polarity of the TIS in Figure 1, the limiting power supply rejection ratio (PSRR) is defined by the negative supply rail. This is because the TIS, whose low impedance emitter sits on the negative supply rail, couples supply rail ripple to the output of the TIS at the same single pole rate as major loop transmission falls with increasing frequency. This gives a PSRR of only 53dB at ripple frequency (100Hz), which deteriorates dramatically thereafter at a single pole rate to 0dB at ultrasonic frequencies (Figure 2).

Power supply rejection was established in LTspice by inserting an AC voltage source in series with the DC power supply and merely plotting the AC frequency response at the output of the amplifier. An ideal unity gain voltage controlled voltage source was used to model the output stage.

The TIS is not as vulnerable to the introduction of ripple from the positive supply because its output is shielded by ANF current source Q19/Q2. The ANF current source possesses a high output impedance due in part to the fact that its loop transmission exceeds 40dB to at least 10kHz; the beneficial effect of this is evident in simulation by supplying the TAS with an ideal current source with the TIS's ANF current source in situ: positive supply rejection is found to exceed 80dB across the audio band.

The RC filters R1/C3 and R3/C2 in the positive supply rail and R6/C10 in the negative supply rail not only guarantee a minimum power supply rejection of about 75dB and 95dB for the negative and positive supplies respectively at ripple frequency (100Hz), they also vastly increase the PSRR at ultrasonic frequencies. This is desirable because it significantly attenuates any ultrasonic voltage, such as radio-frequency interference (RFI), on the supply rails which may otherwise drive the amplifier into slew limiting. In the context of this article, however, it is the unfiltered negative supply PSRR of Thompson's topology (Figure 2) that is of interest as it is this that Groner's arrangement seeks to improve.

Another, mostly aesthetic, inadequacy of the Thompson

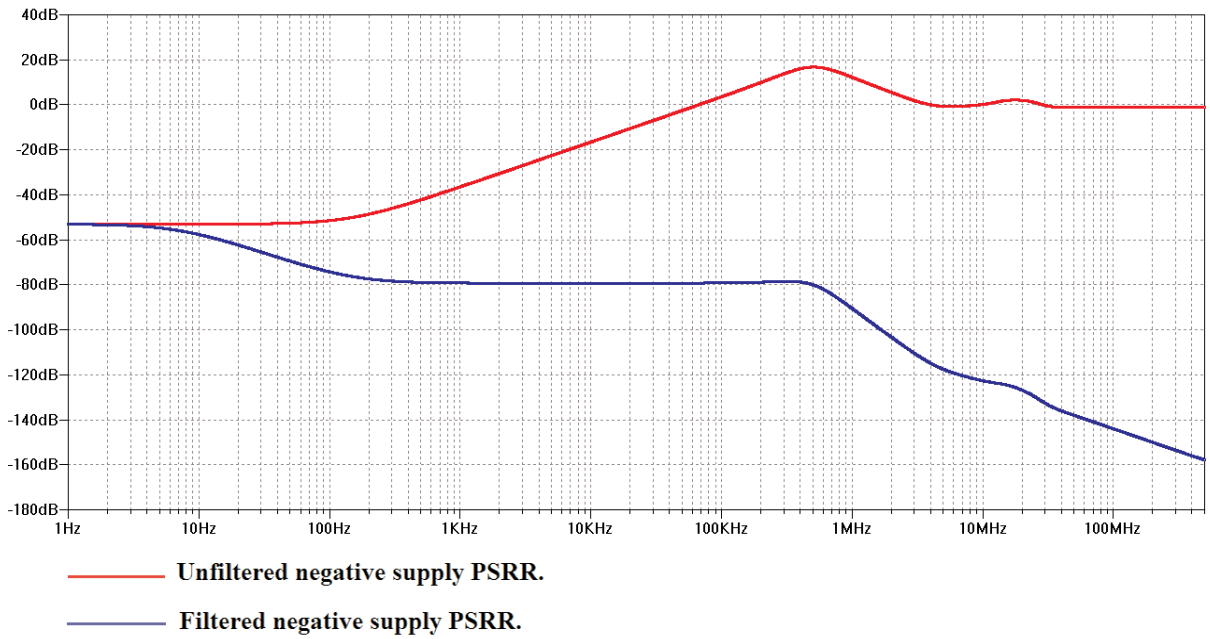

Figure 2: Simulated negative rail PSRR of Thompson's two stage topology of Figure 1

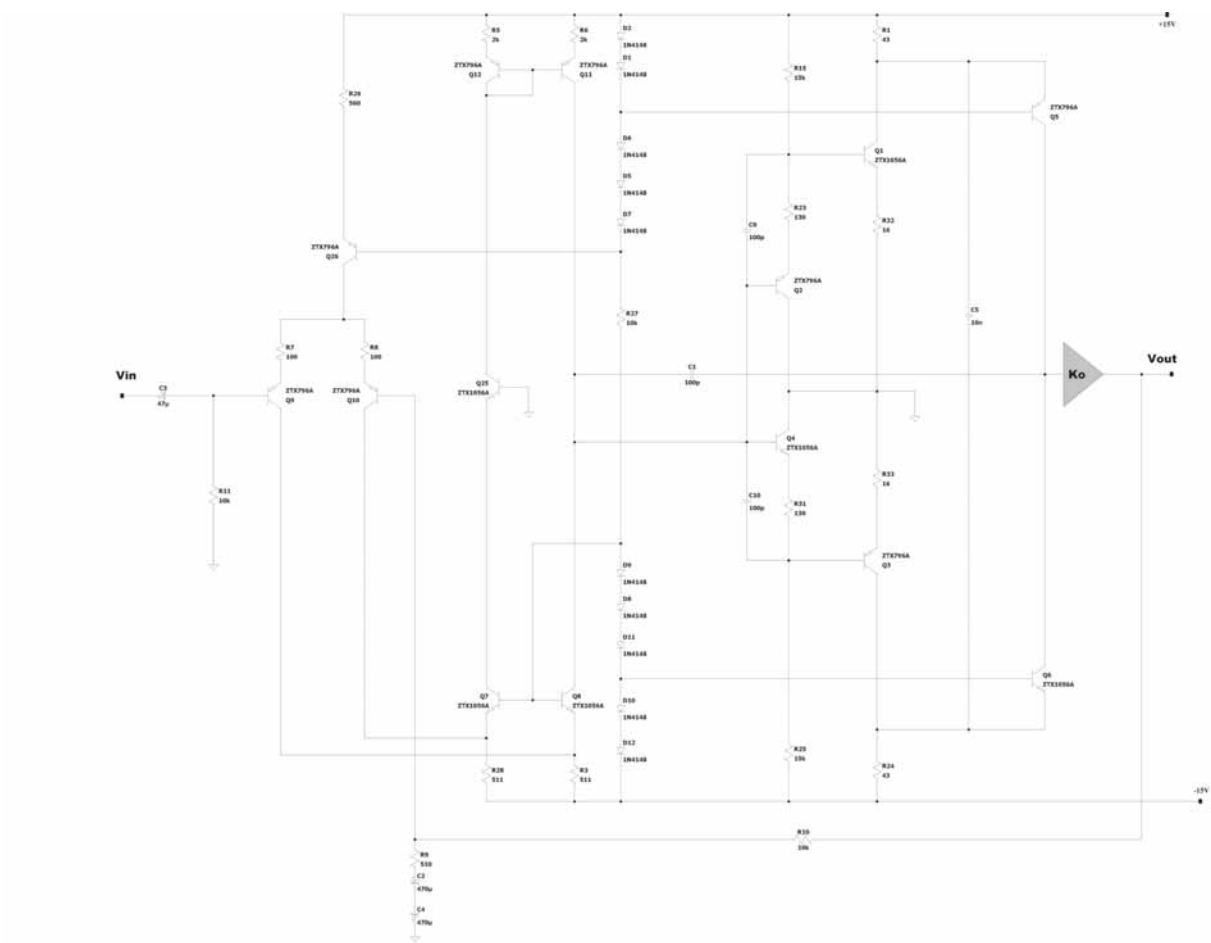

Figure 3: Groner's amplifier with complementary folded cascode TIS

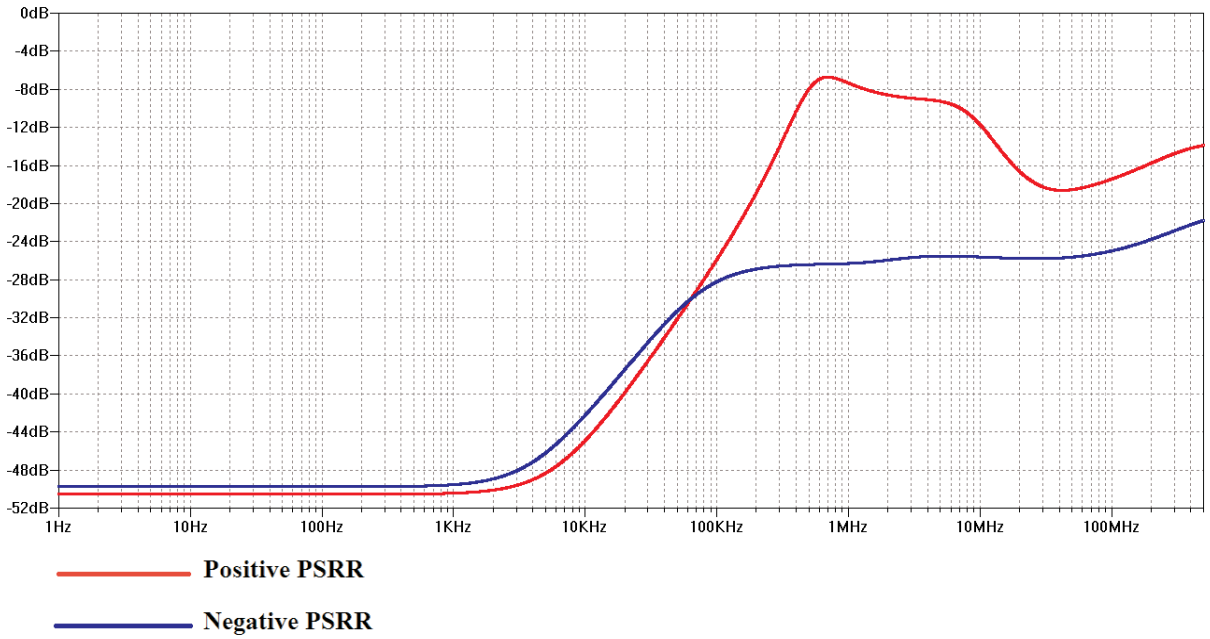

Figure 4: Simulated PSRR of Groner's amplifier

arrangement that Groner's circuit seeks to eliminate is its slew asymmetry. With the polarity of TIS in Figure 1 positive slew rate is appreciably smaller than the negative slew rate. This deficiency in slew rate for positive voltage swings occurs because a significant amount of current that would otherwise service the compensation capacitor is instead siphoned off by parasitic shunt capacitance to ground at the TIS's output [13, 14]. No such impediment exists for negative slew as the second stage transistor Q18 is capable of sinking as much current as the TAS can supply through the compensation capacitor.

Groner's Complementary Folded Cascode TIS

Groner sought to improve the mediocre negative PSRR of the Thompson topology by anchoring the TIS to ground by means of a pair of complementary folded cascodes Q1/Q5 and Q3/Q6 (Figure 3). Emitter followers Q2/Q4 bias the common emitter transistors Q1/Q3 and ensure that the input of the TIS is roughly at ground potential. The TAS is, of necessity, an arrangement of differential-input folded cascodes whose current output is level shifted to the potential at the TIS's input.

The inclusion of emitter followers Q2/Q4 means that there are three transistors in series in the TIS's forward path; this makes the minor (compensation) loop unstable. Consequently, feed-forward capacitors C9/C10 are required to improve minor loop stability margins by shunting the emitter followers Q2/Q4 out of the forward path at ultrasonic frequencies.

In general, including more than two transistors in the minor loop makes it unstable; compensation of the minor loop is then necessary, typically by means of a small (47pF~1nF) shunt capacitance to ground at the TIS's output. This is not a good idea with the Thompson topology as it merely exacerbates slew asymmetry, but shouldn't be a problem with Groner's arrangement as the push-pull TIS should, in principle, provide all the current required to drive the shunt capacitance.

Alas, the positive and negative rail power supply rejection of this topology (Figure 4) is not a significant improvement on the mediocre unfiltered negative rail performance of the Thompson arrangement. For both negative and positive power supply rails, PSRR is roughly 50dB sustained to about 2kHz whereupon it rapidly deteriorates.

Groner maintains that using a regulated power supply for the TAS and emitter followers Q2/Q4 should improve power supply rejection dramatically. This, taken at face value, seems like an elegant solution not least because, as Groner observes, the TAS and emitter followers Q2/Q4 need only be energised from lower regulated voltage rails directly derived from the supplies connected to the complementary folded cascodes and the output stage. The amplifier's power supply rejection would then effectively be defined only by the complementary folded cascodes.

This notion was tested in LTspice by merely connecting a pair of ideal DC voltage supplies, independent of those powering the complementary folded cascodes, to the TAS and emitter followers Q2/Q4. A copy of the circuit was made and an AC voltage source connected in series with the positive DC voltage source energising the complementary folded cascodes in the first circuit; a second AC voltage source was then connected in series with the negative DC voltage source powering the complementary folded cascodes in the second circuit. The frequency response (effectively the power supply rejection) with respect to the output of each circuit was then obtained (Figure 5).

Regrettably, the improvement in power supply rejection is a barely perceptible 4dB with respect to the positive supply at ripple frequency. There was virtually no change detected in negative supply PSRR.

These results demonstrate that the complementary folded cascodes are the weakest link in the design as far as power supply rejection is concerned. This is because the low impedance emitters of common base stages Q5/Q6 of the folded cascodes are all but connected directly to the supply rails, since the values of their emitter resistors R1 and R24 are negligible.

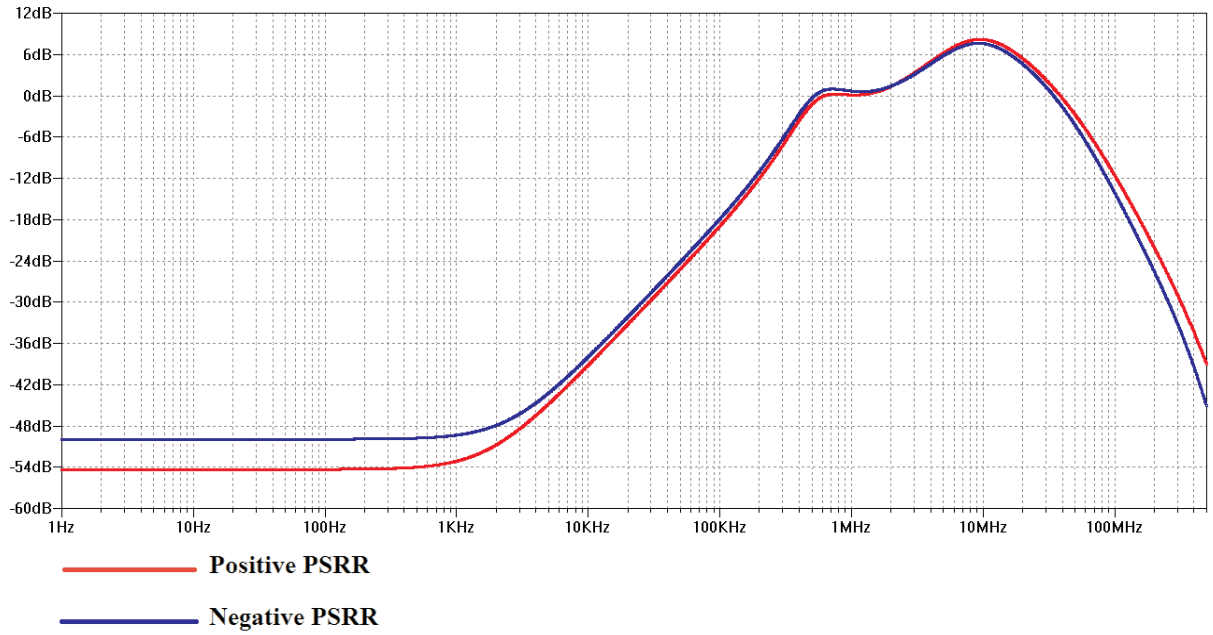

Figure 5: Simulated PSRR of Groner's amplifier with ideal DC voltage supplies powering the input stage and emitter followers isolated from those energising the complementary folded cascodes

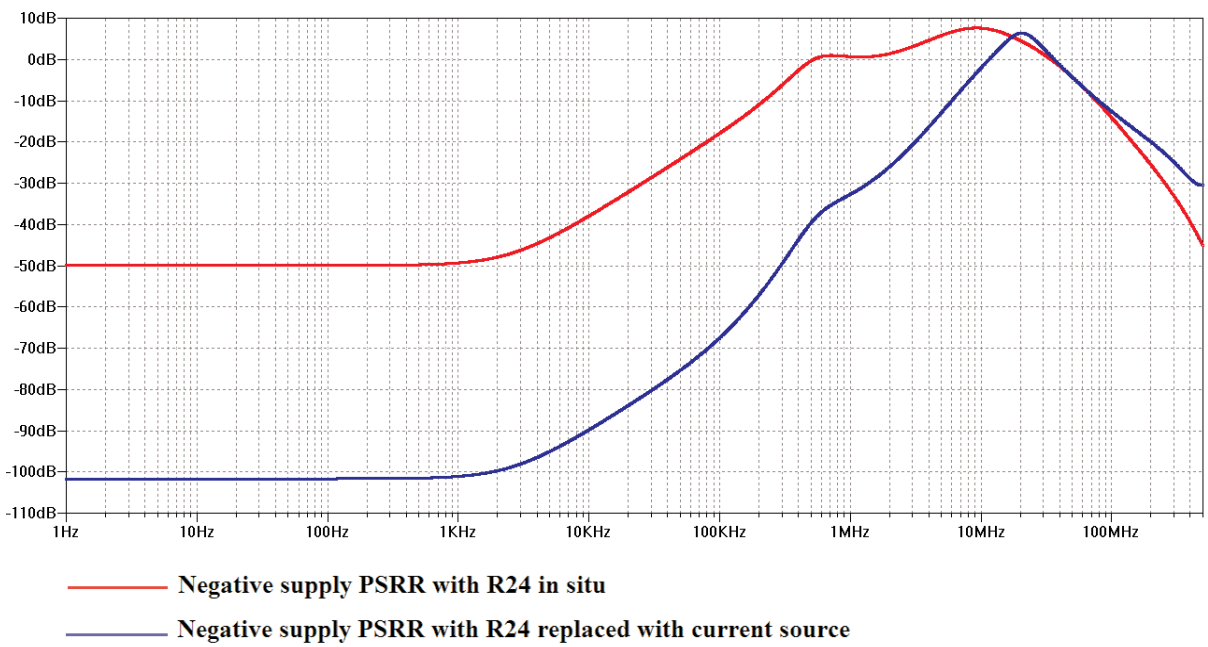

Figure 6: Simulated negative supply PSRR of Groner's amplifier with R4 in situ and with it replaced with an ANF current source. Ideal DC voltage supplies were used for the input stage and emitter followers Q2/Q4 independent of those energising the complementary folded cascodes

Supply rail ripple is, therefore, coupled virtually unchecked through the emitters of Q5/Q6 to the output of the TIS, and explains why the positive and negative power supply rejection of Groner's arrangement is just as poor as that due to the unfiltered negative supply of the Thompson topology of Figure 1.

That the emitters of common base transistors Q5/Q6 are the means by which supply rail ripple passes to the output of the TIS was demonstrated by replacing emitter resistor R24 with an ANF current source while retaining the ideal power supplies for the input stage and the emitter followers Q2/Q4. Power supply rejection with respect to the negative supply rail powering the negative polarity folded cascode was then found to exceed 100dB to approximately 1kHz whereupon it deteriorates as the current source's parasitic capacitances take effect and its loop transmission, as well as that of the amplifier's major loop, declines (Figure 6).

Clearly, as is the case with the Thompson arrangement, Groner's design should benefit from simple RC filtering of the negative and positive power supplies to the TIS in addition to

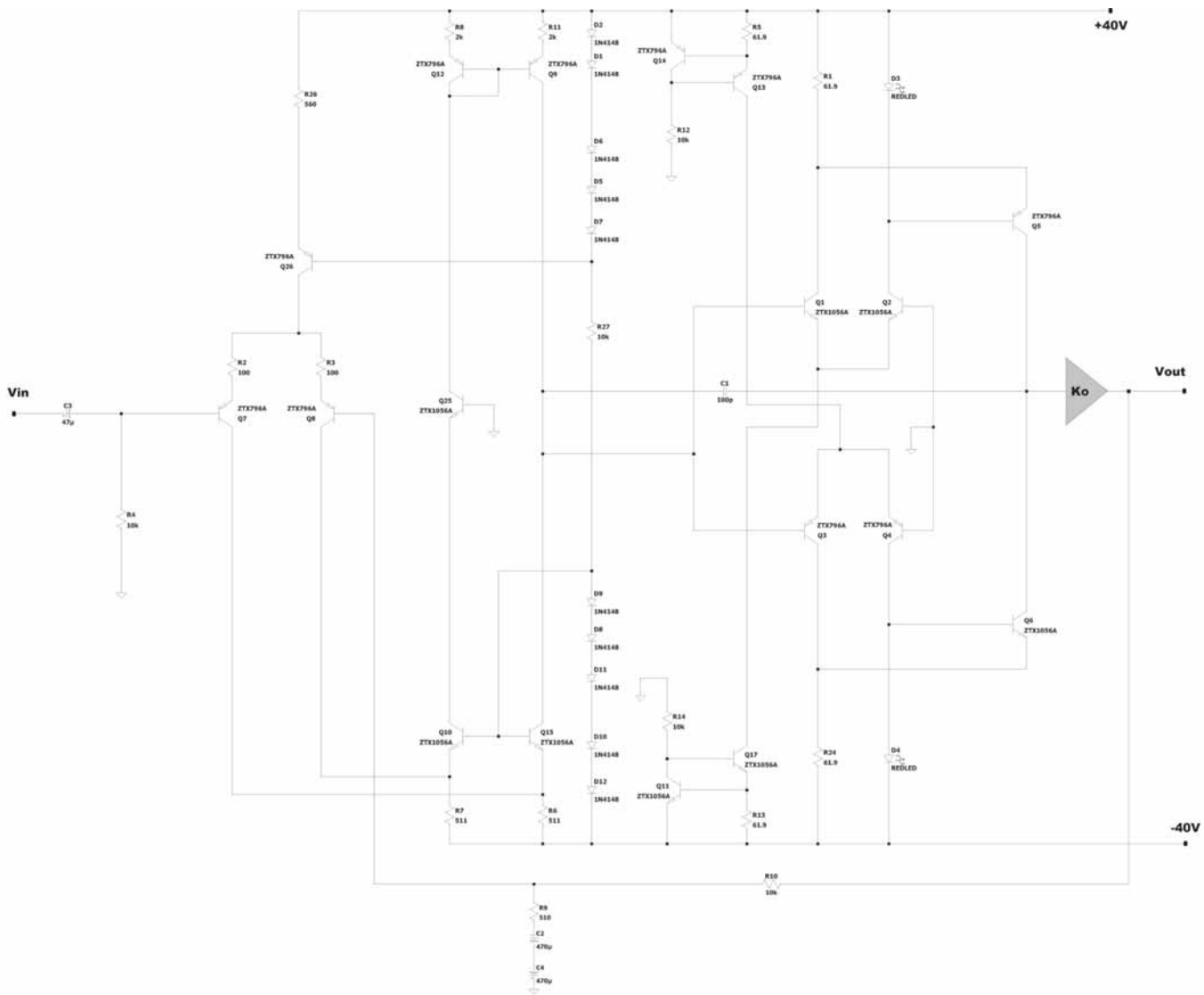

Figure 7: Amplifier with differential complementary folded cascode TIS

ANF current source biasing of the folded cascodes. Note that although there is another potentially major entry point for negative supply ripple through the emitters of the input stage's common base transistors Q7/Q8, there is virtually nothing to be gained in PSRR terms from using regulated supplies for the input stage and emitter followers Q2/Q4 unless the ingress of ripple through the TIS folded cascodes is attended to by replacing resistors R1/R24 with ANF current sources.

Since resistor R1 provides a fixed current, push-pull action occurs with Groner's TIS because an increase in the current demanded of common base transistor Q5 can only be met by an equivalent decrease in the collector current of common emitter transistor Q1. Similarly, the required reduction in the collector current of Q6 is necessarily accompanied by an equivalent increase in the collector current of Q3. Therefore, the peak AC current swing available at the output of the TIS is equal to the quiescent current in each of the common emitter transistors Q1/Q3.

Consequently, the standing collector current in common base transistors Q5/Q6 has to be greater than that of the common emitter transistors Q1/Q3 if the common base transistors are not to be alternately cut off at the limit of their current excursions. It is therefore essential to set the quiescent currents in the common emitter and common base sections of the complementary folded cascodes to the desired relative amounts accurately and precisely.

Resistors R23, R32, R31 and R33 are essential for establishing the quiescent collector currents of common emitter transistors Q1/Q3. Without these resistors the standing currents in these transistors would be undefined, and, accordingly, setting the quiescent current in common base transistors Q5/Q6 would be impossible.

The problem is that inserting R23/R31 in series with the emitters of emitter followers Q2/Q4 reduces their quiescent current; resistors R15/R25 need to be reduced by an amount equal to the values of R23/R31 to maintain a constant current in each of the emitter followers.

This is necessary to accurately establish the voltages across R23/R31 since it is these voltages which appear across R32/R33 and therefore set the quiescent currents in common emitter

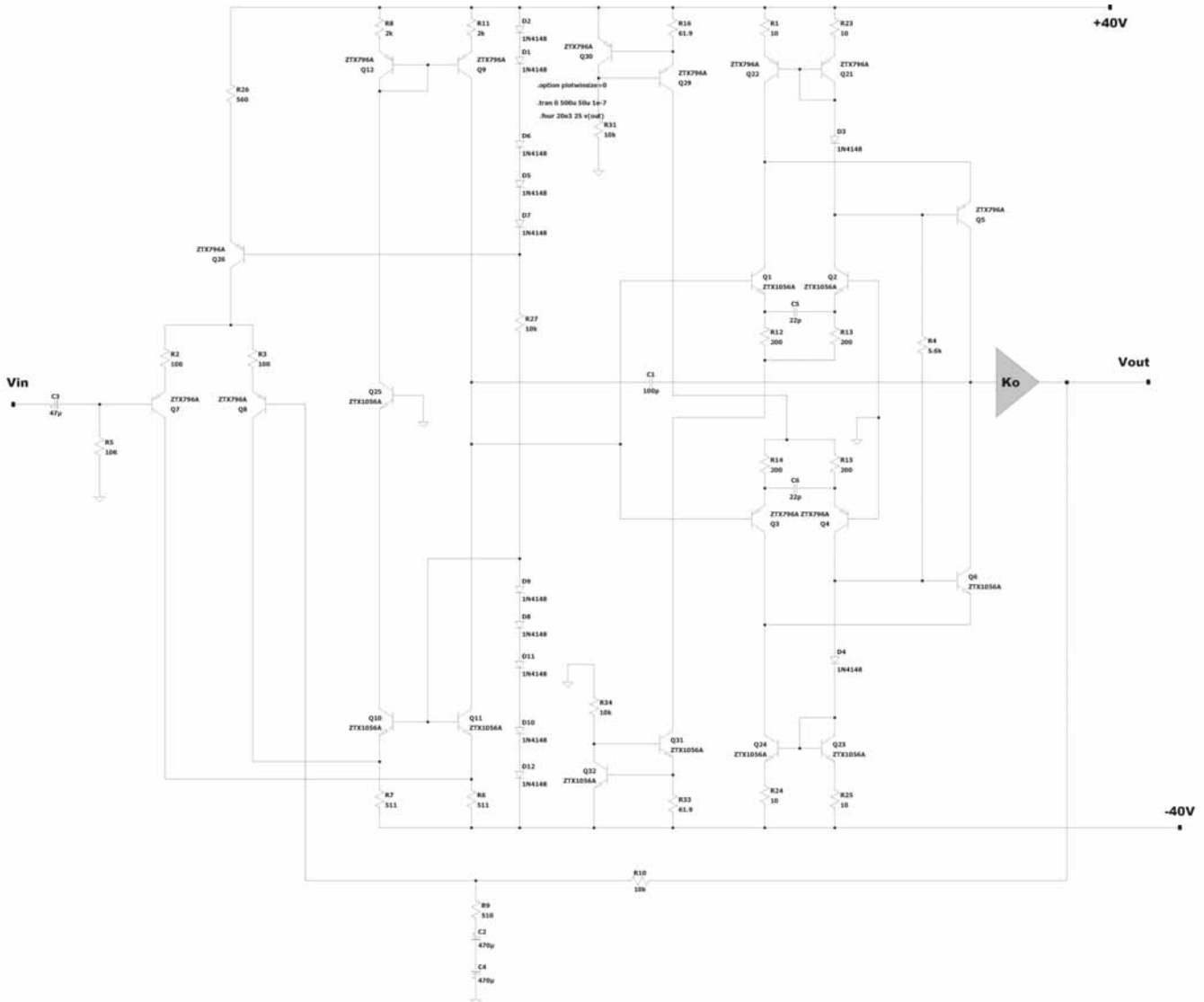

Figure 8: Amplifier with differential current boosted complementary folded cascode TIS

transistors Q1/Q3. However, because resistors are available only in discrete preferred values, maintaining the desired invariant standing currents in emitter followers Q2/Q4 when R23/R31 are introduced is a forlorn hope. Consequently, setting the quiescent collector currents of common emitter transistors Q1/Q3 with accuracy and precision would be tedious and difficult.

Indeed, Groner acknowledges that the values of the resistors biasing common emitter transistors Q1/Q3 would have to be determined experimentally. This is inelegant and unwelcome, especially if large scale industrial production is envisaged.

Current source biasing of the emitter followers Q2/Q4 is, therefore, essential to establish with accuracy the voltages across resistors R23/R31. Thus, with the standing currents in the common emitter and common base elements of the complementary folded cascodes accurately set to their optimal relative levels, push-pull action does, in fact, occur in the TIS, and the slew asymmetry which is the only putative disadvantage of the Thompson arrangement of Figure 1 is abolished.

Incidentally, Groner contends that capacitor C5 dramatically enhances the push-pull action of the TIS by causing it to operate in Class AB. That this is not true is established by noting that C5 is connected to the emitters of the common base transistors in the complementary folded cascodes. These emitters are firmly anchored by their respective voltage references and, as a result, capacitor C5 cannot in any way vary the collector currents of the common base transistors.

The Differential Complementary Folded Cascode TIS

When it became clear that the emitter followers Q2/Q4 in Groner's TIS required current source biasing, it was then apparent that the increased component count could be put to use more elegantly and efficiently by converting the emitter followers to the grounded base configuration instead. The grounded base transistors are then emitter-coupled to the common emitter transistors of the complementary folded cascodes, and the current sources used to bias each emitter-coupled pair (Figure 7).

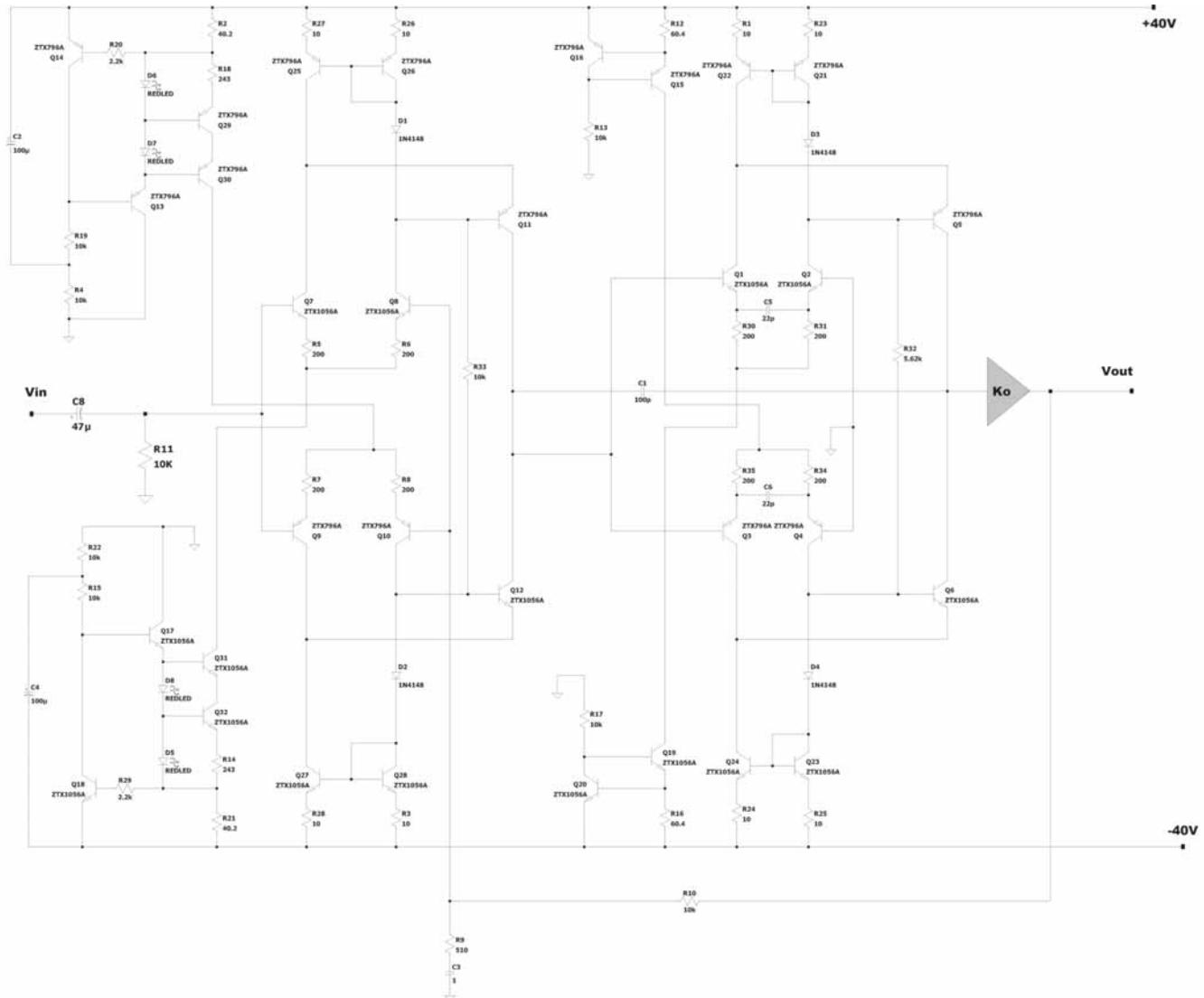

Figure 9: Amplifier with differential current boosted complementary folded cascode TIS and TAS

The feed-forward capacitors required to stabilise the minor (compensation) loop in Groner's arrangement are now redundant since there are effectively only two transistors in series in the forward path of the TIS; the grounded base transistors Q2/Q4 (Figure 7) only serve the purpose of anchoring the TIS to ground and do not appear in the signal path. Consequently the stability margins of the minor loop with this arrangement are more than adequate and are of the same order as those of the buffered TIS in the Thompson topology of Figure 1.

The power supply rejection of this arrangement is a little better than that of Groner's circuit principally because the emitters of common base transistors Q5/Q6 in the TIS are connected to their respective supply rails through low value resistors R1/R24. Replacing these resistors with ANF current sources is mandatory if good power supply rejection (sustained to at least 1kHz) is to be obtained. When this is done, the secondary negative supply ripple entry route through the emitters of common base transistors Q10/Q15 in the input stage may be attended to by either replacing resistors R6/R7 with ANF current sources, or using smaller regulated supplies for the input stage derived from those of the TIS and the output stage.

The Differential Current Boosted Complementary Folded Cascode TIS

Current source biasing of the TIS's complementary folded cascodes can be more elegantly accomplished by using current mirrors (Figure 8). Quiescent current in the complementary common base transistors Q5/Q6 is established by cross-coupling resistor R4. Contrary to intuition replacing this resistor with an active current source does not significantly improve power supply rejection.

The buffered current mirrors double the peak push-pull output current for a given input compared to Groner's circuit (Figure 3) and the circuit of Figure 7. The current mirrors also double the forward path gain of the TIS compared to that of the differential complementary folded cascode arrangement of Figure 7. However, the increased number of transistors in the

minor loop means that minor loop stability margins (in the absence of compensation elements R12, R13, R14, R15, C5 and C6) are significantly reduced compared to those of the buffered TIS in the Thompson arrangement of Figure 1, but are still more than adequate, with a phase margin of the order of forty-five degrees.

If even greater minor loop stability margins are required, then the TIS can be straightforwardly degenerated with resistors R12, R13, R14 and R15 to reduce minor loop transmission (Figure 8). The small emitter-coupling capacitors, C5 and C6, then introduce a zero in the vicinity of the unity minor loop gain frequency, further enhancing minor loop stability margins; minor loop phase margin increases to roughly eighty-five degrees, which is of the same order as that of the buffered TIS in the Thompson circuit.

The differential current boosted complementary folded cascode topology was apparently invented by Shinichi Kamijo [15] who used it as a single voltage gain stage in his amplifiers.

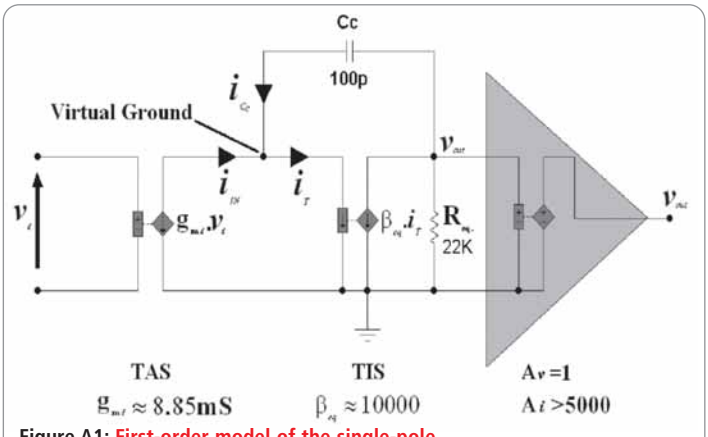

Figure A1: First-order model of the single-pole compensated voltage gain block

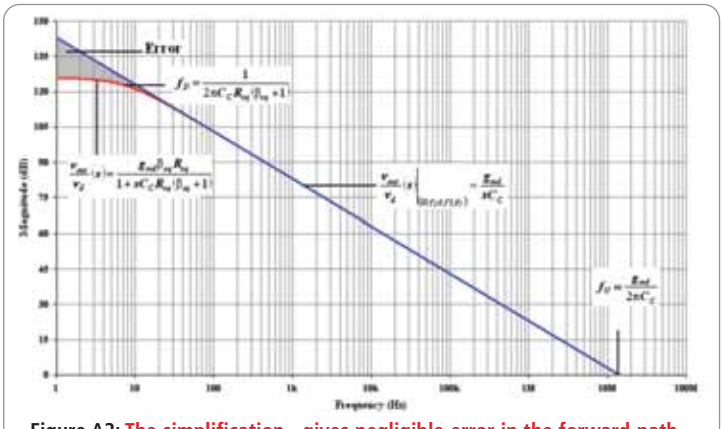

Figure A2: The simplification gives negligible error in the forward-path transfer function at the frequencies of interest

Pole Splitting

The presence of the first non-dominant pole may be accommodated by performing a second order analysis in which the TIS is more accurately modelled by a voltage controlled current source (VCCS) with finite input and output shunt impedances [4, 16], which give rise to two dominant poles (Figure A3). Capacitors $\mathbf{C}_{eq1}$ and $\mathbf{C}_{eq2}$ represent the equivalent shunt capacitance at the input and output nodes of the TIS, while the effective shunt resistance is represented by $\mathbf{R}_{eq1}$ and $\mathbf{R}_{eq2}$ respectively.

Tedious but rudimentary nodal analysis at the input and output of the TIS demonstrates that single-pole feedback compensation causes the first two dominant system poles to move apart, while the finite input voltage v_i generates a so-called feedforward current i_f through $\mathbf{C}_C$. Ultimately, the forward current gives rise to a non-minimum phase (RHP) zero when $\mathbf{C}_C$ short-circuits the TIS's load, $\mathbf{R}_{eq2}$ //$1/\mathbf{sC}_{eq2}$, so that $i_f = g_{m1} \cdot v_i$ and $v_{out} = 0$.

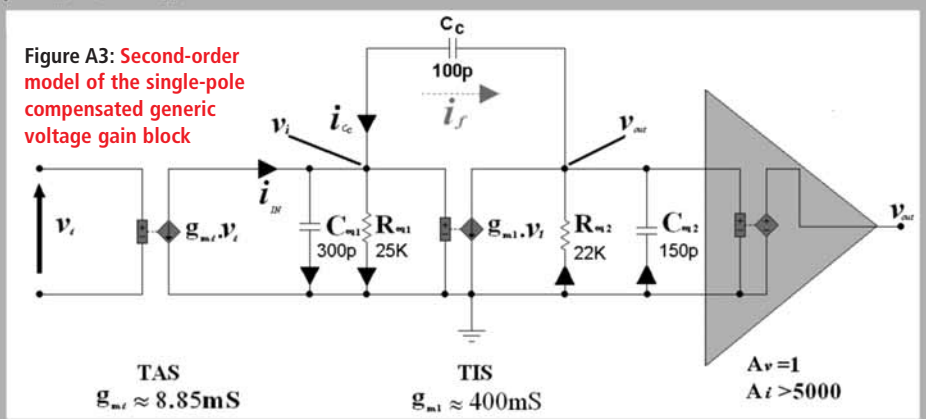

Figure A3: Second-order model of the single-pole compensated generic voltage gain block

However, it would appear this is the first time its use as a transimpedance stage (TIS) has been published.

Indeed, the differential current boosted complementary folded cascode circuit can also be used as the input stage (TAS) where it gives twice the transconductance of the ordinary differential pair with a current mirror used in the Thompson topology (Figure 9). Thus, if the compensation capacitor remains the same and the unity loop gain frequency is to remain unchanged, the degeneration resistors in the input stage of Figure 9 have to be doubled with respect to those used in the input stage of the Thompson circuit and Groner's arrangement.

In contrast to the simple

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At the TIS's input node:

$$-g_{md}.v_d - v_i.sC_C + v_{out}.sC_C - v_i.sC_{eq1} - v_i/R_{eq1} = 0$$
(17a)

And at the TIS's output node:

$$v_i.sC_C - v_{out}.sC_C - g_{m1}.v_i - v_{out}.sC_{eq2} - v_{out}/R_{eq2} = 0$$
(18a)

Solving Equation 18a for v_i and substituting the result into Equation 17a eliminates v_i:

$$\frac{v_{out}}{v_d}(s) = \frac{g_{md}g_{m1}R_{eq1}R_{eq2}(1 - sC_C/g_{m1})}{s^2R_{eq1}R_{eq2}(C_CC_{eq2} + C_CC_{eq1} + C_{eq1}C_{eq2}) + s\{R_{eq1}(C_C + C_{eq1}) + R_{eq2}(C_C + C_{eq2}) + g_{m1}C_CR_{eq1}R_{eq2}\} + 1}$$
(19a)

or

$$\frac{v_{out}}{v_d}(s) = \frac{K(1 - sC_C/g_{m1})}{s^2R_{eq1}R_{eq2}(C_CC_{eq2} + C_CC_{eq1} + C_{eq1}C_{eq2}) + s\{R_{eq1}(C_C + C_{eq1}) + R_{eq2}(C_C + C_{eq2}) + g_{m1}C_CR_{eq1}R_{eq2}\} + 1}$$
(20a)

Where K is the forward path gain at DC:

$$K = g_{md}g_{m1}R_{eq1}R_{eq2}$$
(21a)

From Equation 20a:

$$P_1|_{C_C=0} = -1/(R_{eq1}C_{eq1}) \text{ and } P_2|_{C_C=0} = -1/(R_{eq2}C_{eq2}).$$

The denominator in Equation 19a is a second order polynomial and provided $C_C >> C_{eq1} \vee C_{eq2}$, the local loop is stable and assuming the poles are real it may be expressed as the product of two first-order factors:

$$Denominator(s) = (1 + s/P_1)(1 + s/P_2) = 1 + s(1/P_1 + 1/P_2) + s^2/(P_1P_2)$$
(22a)

By merely equating coefficients it is apparent that:

$$P_1 \approx -1/(g_{m1}R_{eq1}R_{eq2}C_C),\ P_2 \approx -g_{m1}C_C/(C_{eq1}C_{eq2} + C_{eq1}C_c + C_{eq2}C_C) \text{ and } Z = g_{m1}/C_C.$$

Where P_1 is the dominant pole, P_2 the first non-dominant pole and Z the right half plane zero.

Therefore, $|P_1| \propto 1/(g_{m1}C_C)$ and decreases as the product $(g_{m1}C_C)$ increases, while $|P_2| \propto (g_{m1}C_C)$ and increases with increasing $(g_{m1}C_C)$. Rough estimates of the variables C_{eq1}, C_{eq2}, R_{eq1} and R_{eq2} in (Figure A3) were obtained from a simplified hybrid-π (VCCS) BJT model, derived from 2N5551 datasheet characteristics, with g_{m1} modified to accommodate the current gain provided by emitter-follower Q17 (Figure 1). SPICE simulation of Figure A3 shows that P_1 moves down from 21kHz, in the absence of C_C, to 7Hz with C_C in-situ, while P_2 moves from just 48kHz to over 70MHz (Figure A4).

The system therefore maintains a much wider bandwidth with dominant pole feedback compensation than would accrue if such a characteristic were realised by merely increasing shunt-capacitance at the input or output nodes of the TIS. This is unacceptable [17] as it adversely loads the TIS's collector, severely compromising second-stage linearity.
Moreover, dominant pole shunt compensation at either the TIS's input or output node would leave $\mathbf{P}_2$ virtually unchanged, and, consequently, the system's unity loop-gain bandwidth would necessarily have to be much less than 21kHz to guarantee stability when the major feedback loop is closed.

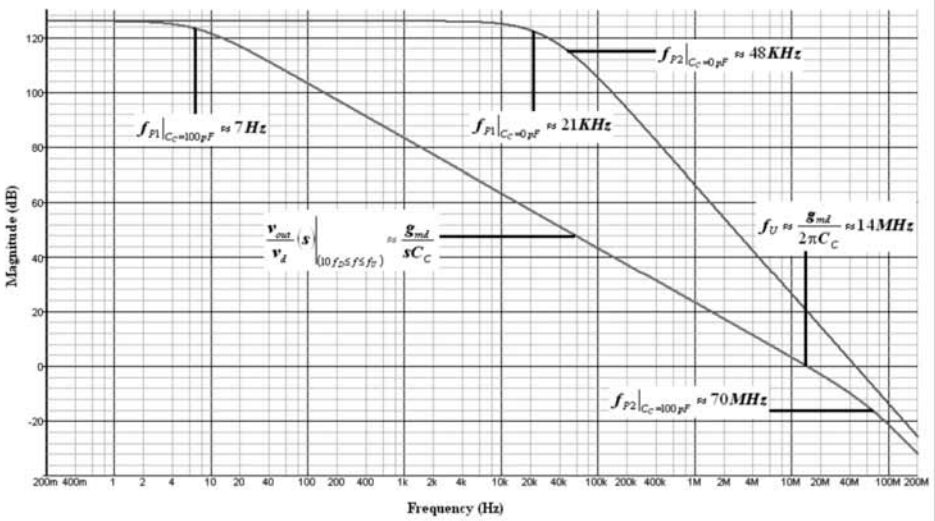


Figure A4: The apparent migration of dominant poles due to Miller-effect compensation on the forward path's frequency response (red trace). The green trace is the uncompensated forward path's frequency response

The RHP zero (not shown in Figure A4) has the magnitude response of an LHP zero (i.e. magnitude response 'breaks up') but the phase response of an LHP pole (i.e. phase response 'breaks down' or tends to -90 degrees in the limit) and might therefore be expected to compromise stability margins. This, however, is of no concern in discrete power amplifiers with an all-BJT second stage as $\mathbf{g}_{m1}$ is invariably much larger than $\mathbf{C}_C$ which ensures that the RHP zero resides well beyond the unity-gain bandwidth of the amplifier.
Determining system singularities in this fashion helps develop a vivid appreciation of circuit behaviour, but is only of academic interest to the designer of discrete amplifiers, as the solutions depend on imprecisely known variables such as $\mathbf{C}_{eq1}$ and $\mathbf{C}_{eq2}$ which, moreover, also vary dynamically.
In practice, the first-order approximation of Equation 16a is all that is required to determine the value of first stage transconductance and the corresponding size of compensation capacitor needed to ensure that non-dominant system singularities, including output stage poles, are relegated to well beyond the unity loop-gain frequency. For the practicing engineer, the design-stage analysis of second-order circuit behaviour is the province of SPICE simulators.

differential pair with a current mirror used in the Thompson circuit, matching of differential pair collector currents in the input stage of Figure 9 is not guaranteed. However, even order distortion generated as a result is cancelled at the stage's output where push-pull action occurs, and the quiescent collector currents of the complementary common base transistors Q11/Q12 are, for practical purposes, perfectly matched. Note that due to the slight imbalance in differential pair standing currents the DC offset at the output of the amplifier is likely to be somewhat worse than that of the Thompson circuit.

The power supply rejection of the novel circuits of Figure 8 and Figure 9 was found to surpass that of the Thompson arrangement with unfiltered supplies at ripple frequency only if regulated supplies for the input stage are used. The regulated supplies need only consist of a Zener diode and a resistor, as Groner pointed out.

Conclusion

Groner's circuit and the novel variations thereof achieve somewhat better power supply rejection at ripple frequency than the Thompson arrangement with unfiltered power supplies provided all circuit elements in the TIS are biased with active current sources and regulated power supplies are used for the input stage. However, this is achieved at more than twice the cost of Thompson's arrangement, and the increase in circuit complexity is daunting. Moreover, to extend good power supply rejection to ultrasonic frequencies, simple RC filtering would still have to be used with Groner's circuit and the novel variations discussed here.

Nevertheless, push-pull action in the complementary folded cascode TIS of Groner's circuit and its variants does virtually guarantee symmetrical slew; slew rate can simply be increased by increasing the size of the degeneration resistors in the input stage so that the compensation capacitor can be reduced for the same unity loop gain frequency. This is achieved without running into the Thompson circuit's slew rate brick wall defined by its second stage's inability to supply the requisite current to the compensation capacitor. However, this is not a significant advantage over the Thompson arrangement, whose limiting slew rate is more than adequate for the majority of medium power domestic applications.

Miller Compensation: A First-order Analysis

The generic two-stage voltage gain block with minor-loop compensation (Figure 1) is modelled in Figure A1 by a differential voltage controlled current source (VCCS) driving a TIS consisting of a current controlled current source (CCCS) and load resistor $\mathbf{R}_{eq}$, which is the means by which the TIS's output current is expressed as a voltage.

Resistor $\mathbf{R}_{eq}$ represents the modulus of the effective impedance at the output of the TIS, and comprises the parallel combination of the TIS's output impedance and the output buffer's input impedance. The TIS's current gain β_{eq}, is merely the product of the current gains of transistors Q17 and Q18.

It is assumed here that the minor feedback loop defined by $\mathbf{C}_C$ is stable, and that the amplifier's unity-gain frequency f_U is sufficiently low so that non-dominant poles have negligible effect on its open-loop transfer function.

At DC the TIS, comprising Q17 and Q18 in Figure 1, possesses a low input resistance compared to the TAS's output resistance. As local feedback through $\mathbf{C}_C$ increases beyond the dominant pole frequency, the TIS's input impedance rapidly tends to zero; the TIS's input is then virtually at ground potential, and the entire output voltage may be deemed to appear across $\mathbf{C}_C$.

Invoking Kirchoff's current Law with respect to the output node (Figure A1):

$$-i_{C_C} - \beta_{eq} i_T + \frac{(0 - v_{out})}{R_{eq}} = 0$$

$$\Rightarrow$$

$$i_{C_C} + \beta_{eq} i_T + \frac{v_{out}}{R_{eq}} = 0 \qquad (1a)$$

Similarly at the input node:

$$i_{in} + i_{C_C} - i_T = 0 \qquad (2a)$$

Since shunt-applied negative feedback makes the TIS's input node a virtual ground at the frequencies of interest, then:

$$i_{C_C} = sC_C v_{out} \qquad (3a)$$

Substituting Equation 3a into 1a:

$$sC_C v_{out} + \beta_{eq} i_T + \frac{v_{out}}{R_{eq}} = 0 \qquad (4a)$$

Substituting Equation 3a into 2a:

$$i_{in} + sC_C v_{out} - i_T = 0 \qquad (5a)$$

Equation 5a is multiplied by β_{eq} as a prelude to eliminating i_T:

$$i_{in}\beta_{eq} + sC_C v_{out}\beta_{eq} - \beta_{eq} i_T = 0 \qquad (6a)$$

Thus, adding equation (4a) to (6a) eliminates i_T:

$$i_{in}\beta_{eq} + sC_C v_{out}\beta_{eq} + sC_C v_{out} + \frac{v_{out}}{R_{eq}} = 0 \qquad (7a)$$

$$\Rightarrow$$

$$\frac{v_{out}}{i_{in}}(s) = -\frac{\beta_{eq} R_{eq}}{1 + sC_C R_{eq}(\beta_{eq} + 1)}$$

Since $(\beta_{eq} >> 1)$, then it may be assumed with negligible error that $(\beta_{eq} + 1) \approx \beta_{eq}$, and

$$\frac{v_{out}}{i_{in}}(s) \approx \frac{-\beta_{eq} R_{eq}}{1 + sC_C R_{eq}\beta_{eq}} \qquad (8a)$$

(see Box 1 below)

But:

$$i_{IN} = -g_{md} v_d \qquad (9a)$$

Thus, the amplifier's forward path gain is given by:

$$\frac{v_{out}}{v_d}(s) \approx \frac{g_{md}\beta_{eq} R_{eq}}{1 + sC_C\beta_{eq} R_{eq}}$$

or:

$$\frac{v_{out}}{v_d}(s) \approx K \cdot \frac{1}{1 + sC_C\beta_{eq} R_{eq}} \qquad (10a)$$

Where K is the forward path gain at DC:

$$K = g_{md}\beta_{eq} R_{eq} \qquad (11a)$$

$$1 = \frac{g_{md}\beta_{eq} R_{eq}}{1 + \omega_U C_C\beta_{eq} R_{eq}} \qquad (13a)$$

$$\Rightarrow$$

$$f_U \approx \frac{(g_{md}\beta_{eq} R_{eq} - 1)}{2\pi C_C\beta_{eq} R_{eq}} \qquad (14a)$$

In practice, only forward path gain well beyond the dominant pole frequency is of interest and, with respect to equation (9a), the condition $(\beta_{eq} R_{eq} \to \infty)$ is invoked, so that:

$$\left.\frac{v_{out}}{v_d}(s)\right|_{(10 f_D \approx f \approx f_U)} \approx \frac{g_{md}}{sC_C} \qquad (15a)$$

Equation 14a becomes:

$$f_U \approx \frac{g_{md}}{2\pi C_C} \qquad (16a)$$

Equation 15a is valid only at frequencies well beyond the dominant pole. This is demonstrated by the plot of Figure A2 using typical values (Figure A1); the finite gain of the TIS introduces significant error at DC and infrasonic frequencies.

Box 1:

First stage transconductance $\mathbf{g}_{md}$ in Figure 1 (with degeneration resistors R_2 and R_4) is given by $g_{md} \approx (r_e + R_2)^{-1}$.

The intrinsic emitter resistance $\mathbf{r}_e$ in each TAS transistor is merely the reciprocal of the stage's undegenerated transconductance $\mathbf{g}_{mo}$, viz. $\mathbf{r}_e \approx 1/\mathbf{g}_{mo}$, and $\mathbf{g}_{mo} \approx \mathbf{qI}_C/\mathbf{KT} = \mathbf{I}_C/\mathbf{V}_T$.

Where $\mathbf{K}$ is Boltzmann's constant ($\sim 1.38\times10^{-23}$ joules/Kelvin), $\mathbf{T}$ the absolute temperature, (Kelvin), $\mathbf{q}$ the electronic charge ($\sim 1.6\times10^{-19}$ coulomb) and $\mathbf{V}_T$ the thermal voltage ($\sim$ 26mV at room temperature).

Thus, at room temperature and with the component values in Figure 1, $\mathbf{g}_{md} \approx \left[(38.5\times 2\mathbf{mA})^{-1} + 100\Omega\right]^{-1} \approx 8.85\mathbf{mS}$.

YANG LIU, KUNYUAN HU, YUNLONG ZHU, LEI ZHANG AND AUTOMATION AT THE UNIVERSITY OF CHINESE ACADEMY OF INSPIRED IMAGE SEGMENTATION ALGORITHM BASEDON PULSE OPTIMIZATION

Image Segmentation Using Artificial Intelligence Approaches

Image segmentation is of great importance in computer vision, face recognition, medical imaging, digital libraries and video retrieval among others. Accurately segmenting an image is always a hot topic.

Image segmentation results in a set of areas that collectively cover the entire image, or a set of contours extracted from the image that has a special meaning. All of the pixels in an obtained area are similar in respect some certain characteristics or computed parameters, such as colour, intensity or texture. However, adjacent regions tend to be significantly different in those same characteristics.

Image Segmentation

Traditional image segmentation methods fall into five categories: pixel, region, edge, edge-and-region hybrid and clustering-based segmentation. However, these types of algorithms commonly suffer from problems such as high computational costs and long computational time.

In this work, we introduce a new bio-inspired image segmentation algorithm based on a pulse coupled neural network (PCNN) and particle swarm optimization (PSO). The image was firstly segmented by PCNN and then the PSO algorithm was used to automatically set parameters of PCNN, so that the segmentation performance would be adjusted adaptively. Experiments were carried out to show its effectiveness with high segmentation accuracy.

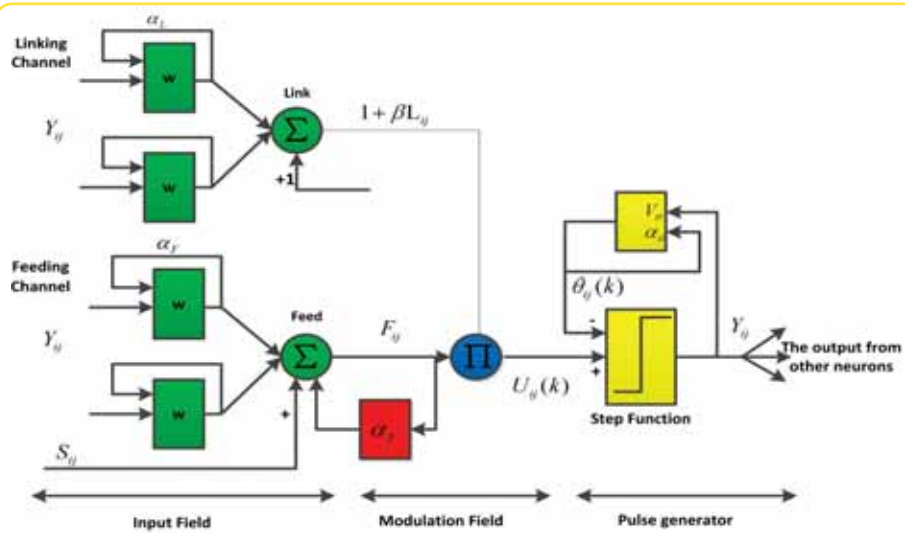


Figure 1: Typical PCNN model

Pulse Coupled Neural Network (PCNN)

A PCNN is a biology-inspired neural network based on the work by Eckhorn et al and experimental observations of synchronous pulse bursts in the visual cortex of animals.

As illustrated in Figure 1, a typical PCNN neuron consists of three parts: input, modulation and pulse generator fields. Each neuron receives signals from both external sources S_{ij} and other neurons through the input fields. The signals reach the neuron through two different channels: the F channel is used to receive feedback input, which contains the external input signal; and the L channel is used to receive a linked input derived from other neurons. The input field can be seen as a leakage integrator, and it simulates the dendritic part of the corresponding biological neuron. In the modulation field, signals from both, the linking channel and feeding channel, are combined in a non-linear manner into the internal activity U_{ij}, which is a simulation of the electric potential of the biologically inspired neuron.

As its name applies, the last field takes charge of the pulse-generating activity firing. It utilizes an adaptive threshold variable Y_{ij} to control the firing event that operates as a step function. Generally, a neuron fires only when the internal activity associated with it is larger than the value of the threshold. If a neuron fires, the threshold associated with it would rise immediately to a very high value, preventing the neuron from further firing. The time interval between two firing events of a specific neuron is called the refractory period. If the neuron does not fire, its corresponding threshold would decay exponentially over time, until it becomes smaller than the neuron's internal activity, which then enables the neuron to fire.

Although the PCNN model can simulate the synchronous firing phenomenon effectively, it is not so easy to use, because of its many parameters. Therefore, to solve the practical problems, some simplified models are used more often.

Here, we consider a simplified model as shown in Figure 2, in which only four parameters are applied: w, β, α_θ and V_θ, (where w is the right of synaptic connectivity, β is coupling strength, α_θ is the attenuation coefficient and V_θ is the threshold amplitude coefficient), which greatly eases its application while maintaining the key features of PCNN. It should be noted that the value of w is almost always the same.

HANNING CHEN FROM THE SHENYANG INSTITUTE OF SCIENCES IN SHENYANG, CHINA, INTRODUCE A NEW BIO-COUPLED NEURAL NETWORK AND PARTICLE SWARM

THIS REGULAR FEATURE COVERS CHINESE RESEARCH AND DEVELOPMENT (R&D)

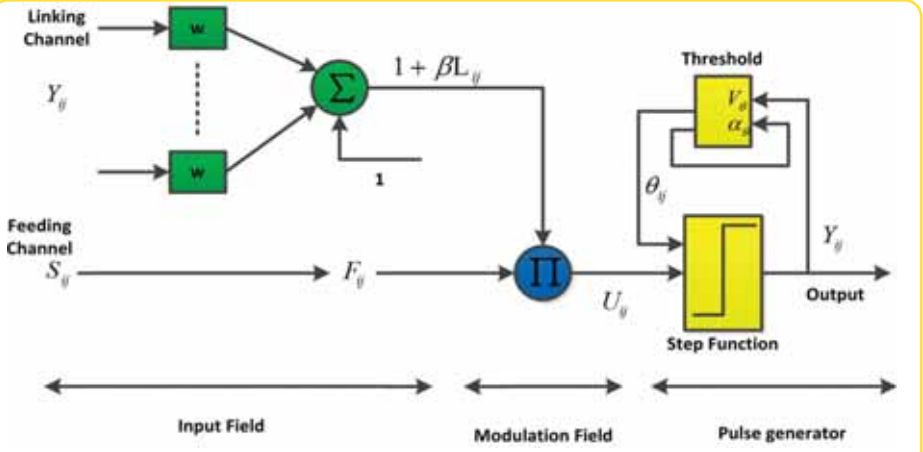


Figure 2: The simplified PCNN model

Particle Swarm Optimization (PSO)

In recent years, researchers in the fields of evolutionary computation have modeled co-evolution as an optimization process. Drawing inspiration from cooperative interactions within a school of fish or bird flocks (also called social interaction), the most successful swarm intelligence system, namely particle swarm optimization (PSO), has been presented. The particle swarm algorithm is a population-based optimization tool, where the system is initialized with a population of random solutions and the algorithm searches for optima by updating generations.

In the PSO model, the potential solutions of each optimization problem can be seen as a bird in search of space, which is called particle. Each particle has a velocity vector which determines the direction and rate of movement, and a position vector that determines the particle's current position. All particles have a fitness value determined by the optimized function. After several iterations, we can obtain the optimal solution.

We focused on a coding of the particles position. Each individual position of the initial population is randomly generated, which matches the corresponding fitness values. The basic model of PSO is illustrated in Figure 3.

In mathematical terms, each individual's direction of movement is manipulated according to the following equations:

$$v_i^{t+1} = \chi(v_i^t + c_1 r_1(pbest_i - x_i^t) + c_2 r_2(gbest - x_i^t)) \quad (1)$$

$$x_i^{t+1} = x_i^t + v_i^{t+1} \quad (2)$$

where the ith particle is represented as

$$x_i = (x_{i1}, x_{i2}, ...x_{iD})$$

the rate of velocity for particle $_i$ is represented as

$$v_i = (v_{i1}, v_{i2}, ..., v_{iD})$$

pbest is the best position found so far of the ith particle; *gbest* is the best position of any particle in its neighbourhood; *x* is known as constriction coefficient; *c1* and *c2* are learning rates; r_1 and r_2 are two random vectors uniformly distributed in [0, 1]; and *t* is the time step.

PCNN and PSO based Image Segmentation Algorithm (PCNN-PSO)

Colour image segmentation using PCNN is a pixel-based segmentation method. In the use of PCNN for image processing, it is accepted that a neuron corresponds to a pixel. The number of neurons is equal to that of pixels of an input image, and every neuron or pixel has a corresponding pixel or neuron. Then, every neuron is linked to its corresponding pixel and neighbouring neurons. The luminance of every pixel is the feedback input of its corresponding neuron, and the output of a neuron is linked to its neighbouring neurons.

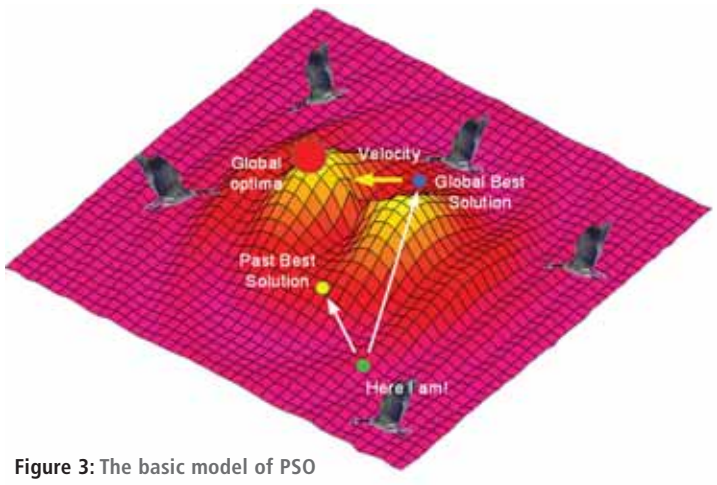


Figure 3: The basic model of PSO

With the PCNN method, different images may require different parameters, therefore an adaptive adjusting method of parameters is needed. In this work, we introduce a PSO algorithm to adjust the parameter β, α_θ and V_θ of PCNN adaptively, according to the overall features of the images used. Here the output image which has the largest image entropy will be selected as the final segmentation result. Figure 4 gives a flow chart for the PSO-based PCNN model (PCNN-PSO).

For clarity, the following algorithm is presented to show the steps of segmentation with our proposed PCNN-PSO method. It can be described as:

1) Initialize the simple PCNN network: set S such that the value of each neuron is the grey level of the corresponding pixel, set Y as 0, and θ such that all values of its elements are the grey level of the pixel which has the highest value; initialize F as S.
2) Input the original image and then get the basic parameters of the PSO algorithm. Set the maximum number of iterations.

a. Start the cycling operation.
b. Decode the particle; input the β, α_θ and V_θ values of each particle to PCNN and calculate the entropy value

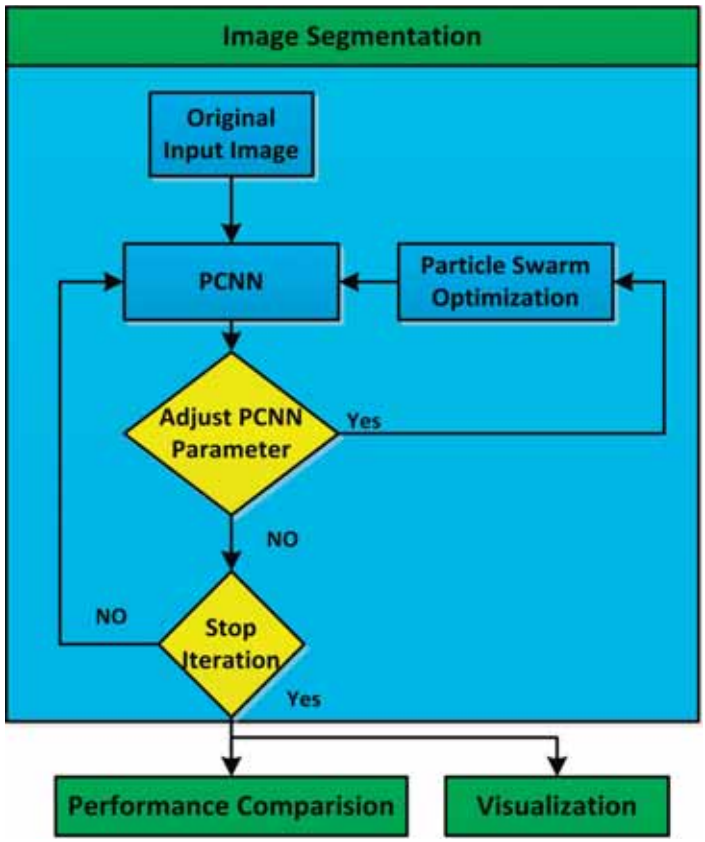


Figure 4: The PCNN-PSO algorithm

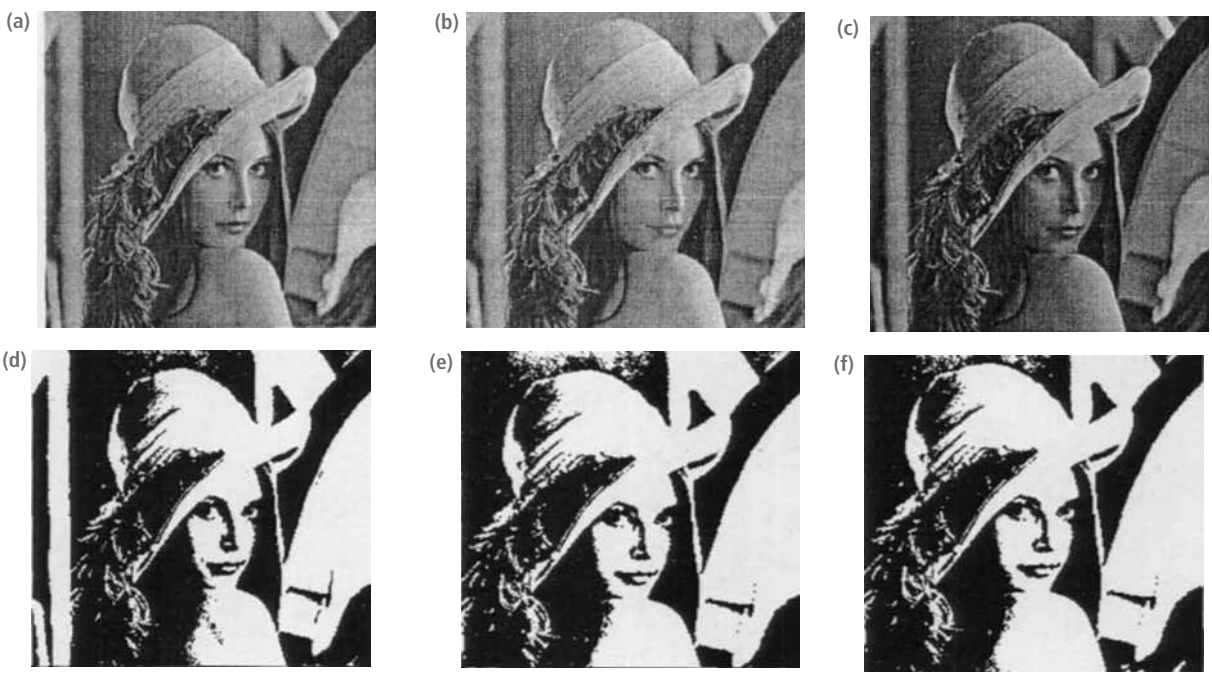


Figure 5: Segmentation result of different brightness and contrast:
(a) (b) (c) are the artworks with different brightness and contrast;
(d) (e) (f) are segmentation results of different brightness and contrast

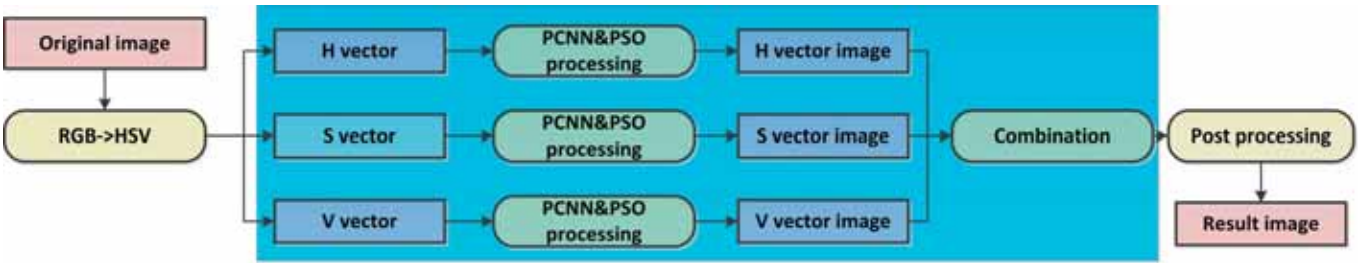


Figure 6: Colour image segmentation based on PCNN-PSO

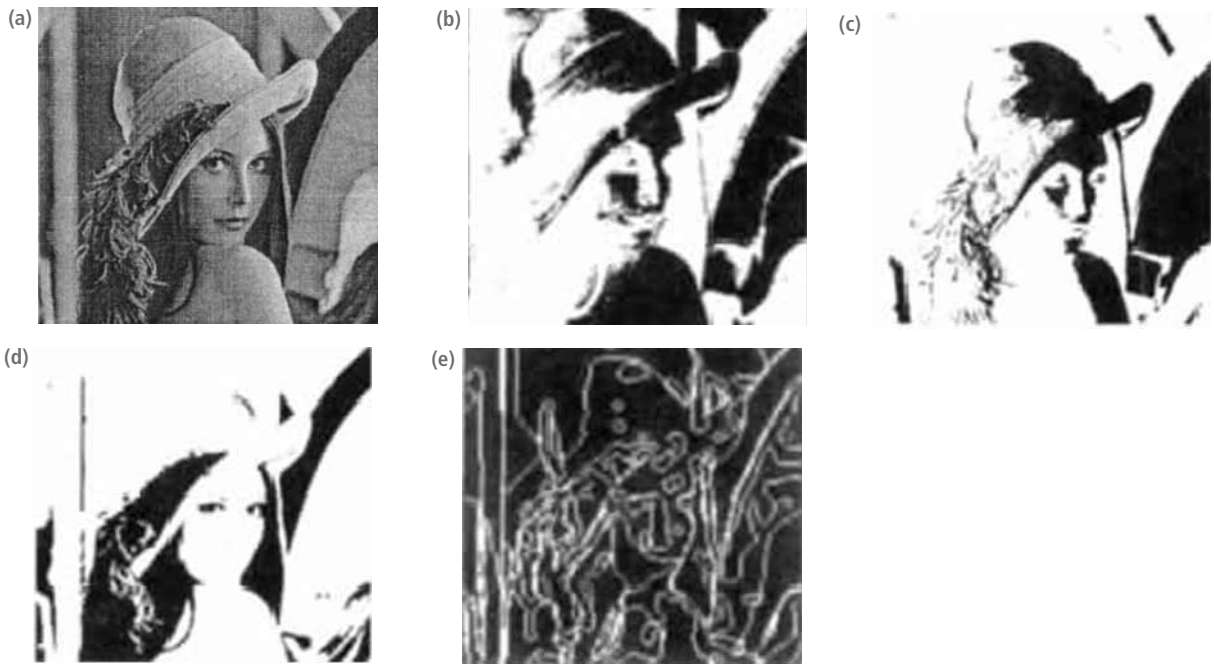


Figure 7: The colour image segmentation of the HSV:
(a) Artwork; (b) The divided image of the H vector; (c) The divided image of the S vector;
(d) The divided image of the V vector; (e) The image of the final segmentation result

of the resulting image and the fitness of particles.

c. Update particle position and velocity.

d. The computation is repeated until the maximum number of iterations is met or the desired system requirements are obtained.

e. Output the final image segmentation result.

Experimental Results

The simulation result of the PCNN-PSO performance on a grey-scale image is shown in Figure 5. Figures 5a, b and c are the original images with different brightness and contrast; whereas Figures 5d, e and f are segmentation results of different brightness and contrast images based on PCNN-PSO.

It can be seen that with the new image segmentation method based on PCNN-PSO, the segmentation results depend mainly on the intrinsic properties of the image; there is no obvious relationship between the segmentation result and the brightness and contrast of the image. The detail of the image is very clear and the image's shape is obvious. The algorithm greatly increases the flexibility and efficiency of PCNN and makes it possible for the application of PCNN in image segmentation to be implemented in hardware.

In another simulation study, we converted the RGB (red, green, blue) image into HSV (hue, saturation, value) space. Here, H represents different colours, S represents the colour density and I represents the colour's luminance. We eliminated the relevance of each component and applied the proposed PCNN-PSO to each vector (see Figure 6). We then applied the mature technology used in gray imaging to achieve colour image segmentation. Figure 7 shows the simulation result of the colour image.

This work was supported in part by the National Science and Technology Support Program under Grant 2012BAF11B04, the National Natural Science Foundation of China under Grant 61105067 and 61174164, and the Engineering research centre of the IOT Information technology integration of Liaoning Province open-funded projects.
Corresponding author: Hanning Chen

productronica 2013

20th international trade fair for innovative electronics production

12-15 November 2013

Munich

Innovation In The World Of Electronics Production

productronica runs from November 12 – 15 in Munich and is the only trade fair of its kind that portrays the entire value chain in electronics production – from software to process control, from technologies to applications and from products to system solutions. Some 1,200 exhibitors from more than 35 countries will give visitors an overview of all of the industry's segments and cover the various markets around the world.

Highlight Segments

As an international trade fair for innovative electronics production, productronica is one of the most important platforms for promoting key topics in the market. The fair focuses on future-orientated topics as well as established industry segments. As in the past, four highlight topics were selected for this year's fair that will also be the focus of forums, roundtable discussions and a special show:

- **Coilware manufacturing**;
- **Manufacturing technologies for cables and connectors**;
- **Industry 4.0: Efficient production management in manufacturing**;

On the first day of the fair, the panel of prominent speakers at the CEO roundtable will discuss the topic "Industry 4.0 – Opportunities and Challenges for a Competitive Production of Tomorrow".

- **Electronic Manufacturing Services (EMS)**.

Special Shows

In addition to the exhibition, special shows will give participants a unique look at various hot topics via vivid demonstrations, a diverse range of lectures and discussion events. For example, topics such as electromobility or energy-storage technologies will be presented based on practical, innovative solutions. The special show on coilware manufacturing aims to depict the entire value chain, from the refinery to materials, distributors, machines and final applications. It is being organized by the Electrical Winding & Insulation Systems (EWIS) Society in the German Electrical and Electronic Manufacturers' Association (ZVEI).

Another special show is dealing with automotive electronics. Car manufacturers use electronics to differentiate their products, for driving performance, engine control, the interior, or safety technology. In contrast to consumer electronics, automotive electronics and its products must meet extremely high standards when it comes to long service life, thermal stability, vibration and shock resistance, robustness and reliability.

VDMA Productronics is working with the Fraunhofer Institute for Institute for Reliability and Microintegration to organize a special Automotive Electronics show in Hall B2 (Stand 227). It will cover the following main topics: reliability, sensor technology, power electronics, interiors and LEDs.

PCB & EMS Marketplace

productronica 2013 will increase its focus on the topics of circuit boards and electronic manufacturing services with a platform known as the PCB & EMS Marketplace; Hall 3 will be dedicated to these two sectors. The marketplace will have a prominent, central location and give exhibitors and visitors various ways to gather information on PCB manufacturing and EMS.

The PCB & EMS Marketplace is a central meeting place for exhibitors and visitors alike. It is also productronica's way of placing special emphasis on these topics.

A new feature at this year's fair is the Interactive Corner, which is an additional opportunity for an intense and direct exchange of information, especially for visitors. There will also be a Speakers Corner, which will feature a number of lectures and panel discussions on the industry's latest hot topics.

Cleanroom Event Stage

The Cleanroom Event Stage in Hall B2 (Stand 381) will give the important sector 'production under cleanroom conditions' its own platform at productronica.

In various interactive live sessions, visitors will be given an in-depth look at everything from setting up, equipping and operating a cleanroom to testing the measuring equipment, logistics, machine delivery, cleaning and utility feeds (hookups) in cleanrooms. The topic of clothing, including dressing procedures and how to launder cleanroom clothing, as well as the layout of the machines and design elements to satisfy cleanroom standards, their suitability for cleanroom use, recording various parameters and the use of robot arms (biorob) will also be covered.

Up to date and comprehensive about productronica is at:
www.productronica.com

Peak Group Features ATE And Mass Interconnect Systems

At NIDays 2013, the Peak Group, a National Instruments Alliance Partner, is featuring its latest developments in automated test systems as well as test solutions using mass interconnect products from Virginia Panel Corporation (VPC).

Peak is a proven provider of automated test and measurement solutions, supporting every stage of the assembly process from component testing to highly complex functional solutions.

The company has over 25 years' experience of providing innovative test solutions in the military, aerospace, rail, automotive, power generation and industrial electronics markets. "Our holistic approach ensures that all aspects of the product lifecycle are supported, from prototype through to service and repair", comments Technical Sales Manager Karl Miles.

Peak offers intelligent integration of COTS (commercial off-the-shelf) equipment with custom-designed mechanical, electronic and system software elements. Comprehensive installation and commissioning procedures are deployed to merge Peak's test systems with customers' processes, followed up with hands-on training and the provision of detailed documentation.

See us at Productronica on stand number A1.159.

www.thepeakgroup.com
Hall A1, Stand 159

MicroCare Corp. Introduces Non-Halogenated, VOC-Free Flux Remover at Productronica

MicroCare Corporation will again exhibit cleaning products at Productronica Munich this November. One of the most important new products on show will be the new VOC-Free Flux Remover–UltraClean. It complies with international environmental regulations by using an all-new halogen free/non-chlorinated formula that contains no volatile organic compounds (VOCs). It is also packaged in a GHS-complaint dispenser with safety phrases translated in 14 languages. This ensures EU REACH compliance and an easy fit into mandatory hazard communication training programs.

Packaged in a convenient aerosol, it is tailored to perfectly clean flux, paste and oils typical to electronics production lines. Unique in the industry, the cleaner may be dispensed directly from the aerosol can, or to further reduce costs and enhance cleaning performance; it can be dispensed using the MicroCare TriggerGrip cleaning system.

VOC-Free Flux Remover–UltraClean cleans rosin fluxes, synthetic fluxes, 'no-clean' fluxes as well as hard-to-clean solder pastes used to assemble and manufacture of printed circuit boards.

www.microcare.com
Hall A4 Stand 515

A MONTHLY COLUMN ON TEST AND MEASUREMENT (T&M) ISSUES

Embedded Instrumentation Passes a Milestone

BY **REG WALLER**, EUROPEAN DIRECTOR, ASSET INTERTECH INC

Last year I wrote an article about how embedded instrumentation is closing the test and measurement gap that inevitably occurs between the introduction of a new, more advanced generation of technology and the T&M equipment needed to debug, validate and test it. That article made the point that embedded instrumentation is narrowing this gap considerably and making up for some of the shortcomings of legacy testers and external instruments.

Just recently, embedded instrumentation achieved a major milestone of its own when members of the Institute of Electrical and Electronics Engineers (IEEE) began final balloting on the ratification of a new industry standard for embedded instrumentation, the IEEE P1687 Internal JTAG (IJTAG) standard.

A standard like IJTAG is critical because without it every organization or company developing embedded instruments or the tools to use them will simply take its own path. Each semiconductor vendor, for example, who is embedding instruments into its chips will have its own operational methods, interface mechanisms and tools. Engineers wanting to take advantage of embedded instruments have had to learn the methods of each provider. Moreover, developers were hard pressed to re-use their favourite instruments in another design because the interface to embedded instruments has not been standardised and, as a result, their portability has been severely limited.

Some of this has already changed as an IEEE working group has developed the IJTAG standard over the last several years. In fact, evidence of an IJTAG ecosystem recently emerged at the International Test Conference (ITC) this September in California. At that conference, prominent EDA chip-level tools providers Mentor and Synopsys demonstrated their already available tools for instrument and access network creation and insertion, rules checking, verification (simulation) and test vector generation. A complete ecosystem for any new technology would involve tools for creation or generation of the technology, integration with other technologies and usage or operational tools. All three of these phases were demonstrated. Synopsys and Mentor showed that their tools could embed instruments into an ASIC and an FPGA equally. Then the instruments were operated and managed by a board-level IJTAG tool, ASSET InterTech's ScanWorks platform. So, even before final ratification of the standard early next year, ITC conference attendees could observe an extensive IJTAG tools ecosystem featuring an automated chip-to-system-level integration and operational strategy.

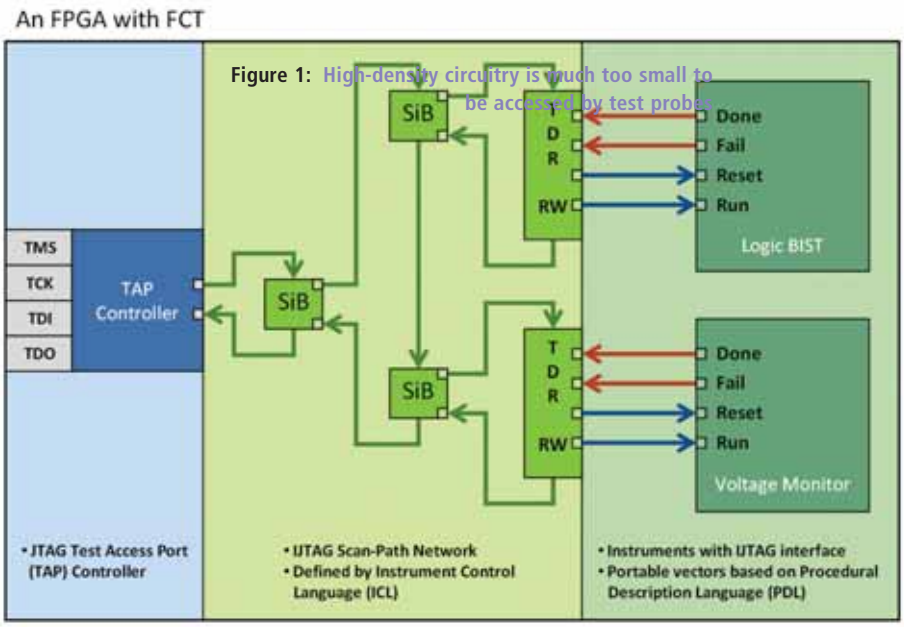


Figure 1: High-density circuitry is much too small to be accessed by test probes

Speaking the IJTAG languages

Two of the key components defined by the IJTAG standard are the languages it defines. The Instrument Connectivity Language (ICL) describes the on-chip network of embedded instruments that might be deployed inside an FPGA, for example. In addition to validating and characterising the FPGA's operations, these same IJTAG instruments could be re-

> *A standard like IJTAG is critical because without it every organization or company developing embedded instruments or the tools to use them will simply take its own path*

used later at the system-level to validate, test and debug prototype circuit boards, as well as in production after the board design has moved into high-volume manufacturing. At the board level, the embedded IJTAG instruments are accessed by way of a related standard, IEEE 1149.1 boundary-scan, which is commonly known as JTAG. The board's JTAG connector must be linked to the FPGA's 1149.1 Test Access Port so that engineers can operate the embedded IJTAG instruments.

The other IJTAG language is Procedural Description Language (PDL). Engineers will use PDL to define the test vectors or operational procedures that are applied directly to instruments. PDL lets the engineer control and automate the execution and scheduling of embedded instruments independent of any IJTAG access network they may be connected to.

Figure 1 shows an example of an extremely simple IJTAG on-chip architecture featuring just two embedded instruments. Such a network could easily grow to hundreds, if not thousands of instruments.

Even if the on-chip network were to grow to thousands of instruments, the IJTAG working group has included capabilities to ensure the network's flexibility and ease of use. For example, a Segment Insertion Bit (or SIB in the block diagram) lets engineers manage the network, accessing each instrument or groups of instruments to turn them on or off. An individual instrument might also be isolated from the others on the network while it executes its tasks. The SIBs connect or disconnect network segments to the main architecture to accomplish many of these tasks.

The Future is Embedded Instrumentation

Processors keep getting faster, on-board buses accelerate, chips become denser with exponentially more circuitry, which means circuit board density increases too. All of the inevitable advancements we sometimes take for granted have not only increased the gap between technology and T&M, but in addition we now know that advanced technology is moving beyond the reach of legacy T&M methods like intrusive probe-based instruments and testers.

In many cases, the only way to effectively debug, validate and test many chip and board designs, as well as production units, is with embedded instrumentation. Fortunately, we've seen that the tools ecosystem for embedded instrumentation is already in place. The future is now. ●

NEW FLAME RETARDANT EMC SHIELDING GASKET FROM KEMTRON

Kemtron, the British manufacturer of RFI/EMI shielding gaskets, materials and components has launched a flame retardant, low smoke, low toxicity EMC shielding gasket which is tested and approved to the international standard UL94V-0 by Underwriters Laboratories for flame retardancy, file number E344902. Also tested for smoke density to BS 6853:1999: Annex D.8.3 and oxygen index to BS EN ISO 4589-2:1999, confirming the material meets the requirements for minor internal use on vehicles category 1a, such as gaskets for electronic enclosures, is making it highly suitable for applications in underground transportation, trains and other safety critical applications.

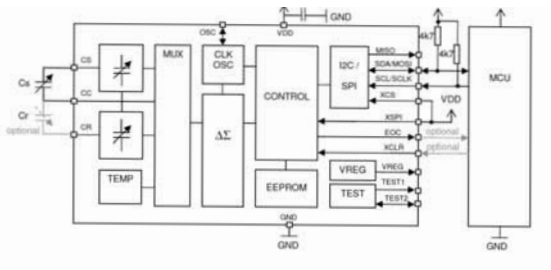
The material is nickel-coated graphite loaded into silicone elastomers, product code SNG-FR. This allows the gasket to provide a highly electrically-conductive path between mating flanges of an electronics equipment enclosure giving a high level of RFI/EMI shielding. The material can be supplied as an extruded strip in various profiles, "O" rings or flat die cut gaskets.

www.kemtron.co.uk

Low-Power Capacitive Sensor Signal Interface IC

Micro Analog Systems Oy launched MAS6510, a 24-bit piezo resistive sensor signal interface IC intended primarily for MEMS-based pressure sensor modules.

The device uses a ratiometric capacitance to digital (CDC) principle employing a delta-sigma (DS) conversion technique, giving very good noise performance. Its current consumption is extremely low (48µA, one pressure conversion in a second with 17-bit resolution) and it can operate at low supply voltage from 1.8V to 3.6V, making it an ideal solution for interfacing a capacitive sensor in power consumption critical portable applications. The effective number of bits (ENOB) of the CDC is 17 bits. The over sampling ratio (OSR) of the DS-converter has five values to choose from for further optimization between conversion accuracy, speed and current consumption. Two capacitance measurement modes are supported and the output can be proportional either to capacitance difference (CS-CR) or to capacitance ratio (CS-CR)/CS.



www.mas-oy.com

THIRD GENERATION, HIGH PERFORMANCE, PROGRAMMABLE, UNIVERSAL FREQUENCY TRANSLATOR FOR 100GBPS INTERFACES

Integrated Device Technology (IDT) launched the third generation of its Universal Frequency Translator (UFT) family of timing devices for high-performance optical networks, wireless base stations and 100 Gigabit Ethernet (GbE) interface applications. The new UFT devices are the industry's only single-chip programmable solutions capable of generating eight different output frequencies with less than 300-femtoseconds RMS phase jitter over the standard 12kHz to 20MHz integration range.

The IDT 8T49N28x UFT family of timing devices offers eight independently-programmable clocking outputs with the flexibility to apply virtually any input frequency and select virtually any output frequency. The devices' high level of integration and low jitter eliminate the need for separate frequency translation, redundancy management and jitter attenuation devices – empowering system designers to save cost and board area by consolidating those functions into a single device. In addition, the devices offer significant flexibility in configuration and ease-of-programmability with IDT's Timing Commander software.

www.idt.com/go/clocks

IQD INTRODUCES NEW CUSTOM CRYSTAL FILTER PRODUCT PLATFORM

IQD has launched a new custom crystal filter product platform at the European Microwave Week 2013 event. The IQXF-1000 series is a range of bandpass filters with centre frequencies from 1.4 to 200MHz, based around fundamental and third overtone mode crystals. These 2- to 12-pole crystal filters can operate over a temperature range of -55 to +85 degrees C with a bandwidth @3dB from ±2kHz and with the passband ripple as low as 0.5dB and insertion loss down to 2.5dB.

Proprietary simulation software is utilised to offer prospective customers rapid feedback on their crystal filter application requirements. What makes the design software a competitive advantage is the embedded algorithm that calculates the necessary relationship between critical resonator parameters within the matched set of crystals used in the filter design. To more reliably determine the filter behaviour in production, the algorithm takes into account production equipment process limitations.

www.iqdfrequencyproducts.com

SIC Goes From Strength To Strength

A recent industry report by one of the leading UK financial analysts has highlighted SIC Ltd as one of the strongest growth businesses within its sector, well exceeding industry averages. The UK Electronic Cable Assemblies Industry report compiled by Plimsoll Publishing Limited assesses each of the industry's largest 117 companies and details a comprehensive study of their performance against an industry standard benchmark, providing a trusted, independent performance assessment.

SIC's business growth is a result of a multitude of efforts to a single goal, becoming a stronger supplier for its customers to make it the number one choice in the UK for electronic assembly manufacture. The company has invested heavily in ensuring that its business operates to maximum efficiency in all aspects, from the latest technology and machinery in the production area, maintaining ISO9001 along with sector-specific quality accreditations, a complete overhaul of the environmental system and achieving ISO14001 to become a 'greener' manufacturer.

THE RIGHT RELAY FOR ALL APPS: PANASONIC PHOTOMOS

The mobile app easily, quickly and flexibly guides to the PhotoMOS relay best suited for individual requirements. A clear and straightforward navigation with three different search options for users (both primary and secondary), developers and purchasers helps find the optimum component.

The app is optimized for Android and iOS (iPhone) and can be downloaded for free. The differentiated product search makes it easy to find exactly what's needed within the Panasonic Electric Works product portfolio of several hundred different PhotoMOS relays.

Panasonic PhotoMOS relays unify the advantages of semiconductor technology and the typical characteristics of electromechanical relays. Modern semiconductor technology enables fast, quiet, bounce-free switching, even in miniature sizes.

www.panasonic-electric-works.co.uk

Boiler Temperature Sensors from ATC Semitec

ATC Semitec has added to its wide range of temperature probes a series of temperature sensors for use in gas boilers and electric heating appliances; they are also suitable for a variety of temperature applications where a neat, cost-effective solution is required.

Insertion, screw-probe, push-fit and clip-on sensors are all available with the main thermistor resistance values used in the boiler industry; 5kohm, 10kohm and 12kohms. Both brass and nickel-plated housings are available with 1/8"BSP gas threads. Integrally-mounted connectors are based on industry standard 2.5mm pitch terminations.

The pipe-clip sensors are IP67 rated and cover a wide range of pipe diameters from 13-28mm. Very simple to install, they clip securely to the relevant pipe diameter giving a typical response time of less than one second. These clip-on temperature sensors are rated for use from -40/+140°C continuously with an accuracy of ±1°C at 25°C.

www.atcsemitec.co.uk

MULTIPLE SIGNAL TRANSMISSION IN SMALL SPACE FROM WEIDMÜLLER OMNIMATE PORTFOLIO

Customers wanting to reliably transmit as many different signals as possible in a very small space, along with optimum packaging for their electronics are turning to the Omnimate portfolio of products and services to meet their needs.

Omnimate is a complete package of solutions, consisting of components and services for signal processing and power electronics in the industrial environment. In particular, the Omnimate Signal, Power, Housing And Services portfolio is a highly tailored range of device connections and housing products.

Omnimate Signal ensures customers have the right connection system available at all times, with a choice of extremely compact PCB terminals and connectors.

Omnimate Power components provide a maximum level of safety up to 600V in compliance with UL standards. Omnimate Housings deliver a wide range of housing platforms, which guarantee a high level of modularity, as well as individual designs specifically for challenging applications, whereas Omnimate Services design in application specialists assist from specification to individual series production.

www.weidmuller.co.uk

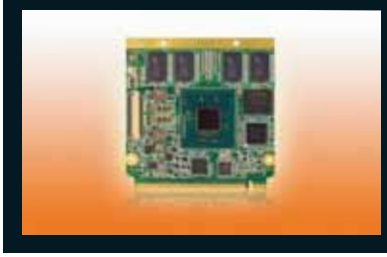
CONGATEC'S FIRST QSEVEN MODULE WITH INTEL ATOM PROCESSOR E3800 FAMILY

congatec has announced immediate availability of the conga-QA3 Qseven module based on the Intel Atom processor E3845. All modules are fitted with ceramic capacitors, making them ideal for industrial mobile applications in harsh environments. New features include an ample L2 cache, which can be shared by multiple cores, and a much faster Intel HD graphics unit compared with the previous generation. This turns new applications into visual experiences.

The modules support Intel Advanced Encryption Standard New Instructions (Intel AES-NI) set, which is more relevant than ever in practical application. This allows developers to offload particularly compute-intensive packaging and encryption routines of the well-known cryptographic algorithm AES (Advanced Encryption Standard) into hardware, thereby enabling high performance encryption without putting a significant burden on the CPU cores.

The conga-QA3 comes in five different Intel Atom processor-based versions (formerly code-named "Bay Trail") for high scalability.

www.congatec.com



HIGH-VOLTAGE BRUSHLESS DC MOTOR DRIVER IC FOR AUTOMOTIVE APPLICATIONS

The new A4900 from Allegro MicroSystems Europe is a high-voltage (600V) MOSFET gate-driver IC designed for driving brushless DC motors. This new device is designed for high-voltage motor control in hybrid and electric vehicles and 48V automotive battery systems such as electronic power steering, air-conditioning compressors, fans, pumps and blowers. The A4900 is also available in a non-automotive version for high-voltage industrial and commercial applications.

The new device incorporates six gate drives capable of driving a wide range of N-channel IGBT or power MOSFET switches. The gate drives are configured as three high-voltage high-side drives and three low-side drives. The high-side drives are isolated by up to 600V to allow operation with high bridge (motor) supply voltages, and use a bootstrap capacitor to provide a voltage higher than the supply gate drive voltage needed for N-channel FETs. Each FET can be controlled with a TTL logic level input compatible with 3.3V or 5V logic systems.

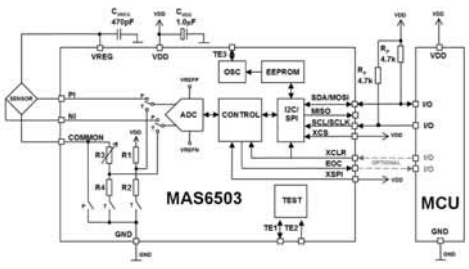
www.allegromicro.com

High Resolution, Low Power, Piezoresistive Sensor Signal Interface IC

Micro Analog Systems Oy announced MAS6503, a 24-bit piezoresistive sensor signal interface IC, primarily intended for MEMS-based pressure sensor modules. The device uses a ratiometric AD-converter principle employing a delta-sigma conversion technique, giving very good noise performance. Its current consumption is extremely low (18.3µA, one pressure conversion in a second at maximum resolution and including sensor bridge current) and it can operate at low supply voltage from 1.8V to 3.6V, which makes it an ideal solution for interfacing a piezoresistive sensor in power consumption critical portable applications. The effective number of bits (ENOB) of the ADC is 17.4 bits. The over sampling ratio (OSR) of the delta-sigma converter has five values to choose from for further optimization between conversion accuracy, speed and current consumption.

The MAS6503 also features supply voltage monitoring mode, which is especially useful in battery-operated systems. The external sensor bridge can be used to sense pressure and temperature, using the built-in sensor sampling switches.

www.mas-oy.com



EXTENDING TRANSMISSION PATHS IN 10GBIT/S NETWORK CABLING

The new Harting Ha-VIS preLink(R) Extender permits the easy extension of transmission paths in 10Gbit/s network cabling systems, as well as allowing unused cables to be reactivated and extended until the next required connection.

This new addition to the company's innovative Ha-VIS preLink(R) cabling system not only enables the simple extension of transmission paths in data network cabling: it also allows fire zones to be bridged and subscriber ports to be directly connected to the terminal block connector without the need for intermediate patching.

Even unused cables can be reactivated and extended to the next required connection. The installer simply assembles the Ha-VIS preLink(R) termination module onto both ends of the cable to be extended. The terminated cable ends are then inserted into the Ha-VIS preLink(R) Extender. A flexible shield clamp transmits the cable shield potential.

The extender itself can be directly mounted on walls, in cable ducts or in a switch cabinet via two 3.2mm diameter fixing holes.

www.harting.com

New PFM DC/DC Converter from Advanced Power Electronics Corp

Advanced Power Electronics Corp (USA) has announced APE1910-HF-3, a Pulse Frequency Modulation (PFM) DC/DC converter with a low quiescent current of around 30μA and shutdown current less than 1uA.

Available in a small RoHS/REACH-compliant halogen-free SOT-23-5 package, the APE1910-HF-3 features a wide input voltage range from 1.2V to 12V. It features a switching current limit (typ) of 350mA, a high output voltage of up to 34V. Using a PFM design, the product provides high efficiency across a broad range of load.

"With a small package size and requiring only a small number of external components, the APE1910-HF-3 offers a low cost and space-saving solution for step-up voltage conversion," said Ralph Waggitt, President and CEO, Advanced Power Electronics Corp (USA).

Established in Taiwan in 1998, Advanced Power Electronics Corporation supplies MOS power discrete components, IGBTs and Power ICs which enable cost-effective efficient solutions for new and existing power applications.

www.a-powerusa.com

NEW, ULTRA-LOW DENSITY FPGAS FROM LATTICE ENABLE ALWAYS-ON SENSOR

Lattice Semiconductor launched new ultra-low-density iCE40 FPGAs, delivering very flexible, single-chip sensor solutions for making a new generation of context-aware, ultra-low-power mobile devices possible. The new additions to the iCE40 FPGA family allow customers to integrate more functions into a smaller space. In packages as small as 1.4mm x 1.48mm x 0.45mm, they are small enough and affordable enough to fit almost anywhere, reducing board space and system complexity.

With hard IP for strobe generators, I2C and SPI interfaces, the new iCE40LM FPGAs deliver near-zero latency to the mobile market, enabling context-aware systems with the real-time capturing of user and environmental inputs with minimal delay or error. This gives designers a platform for their mobile products to deliver media-rich experiences based on movement, travel direction, location and other interactions with the environment.

The small size of the new iCE40 FPGAs enables integration of advanced functions such as IrDA, barcode emulation, service LED and more.

www.latticesemi.com/iCE40

EXTENDED RANGE OF RFI/EMI SMD SPRING CONTACTS FROM HARWIN

Harwin has expanded its range of EZ-Spring contacts with different contact styles and heights. Part of the EZ-BoardWare range of PCB hardware products, the surface-mount spring contacts, also known as Spring Fingers or Grounding Contacts, are now available in 15 different sizes, ranging from 1.7mm to 7.25mm free height (1.20mm to 6.35mm minimum working height) and are suitable for both vertical and horizontal contact actions.

Designed for easy assembly onto PCBs, EZ-Spring Contacts are used as grounding or shielding contacts in contact with metal frames or shields, or even for general electrical connection between PCBs or similar. Mounted in a row, the contacts can provide an excellent RFI shielding connection for metal doors or other cabinet enclosures. The contact design ensures positive contact with the mating surface, and is tolerant to both wiping and sliding action.

Individual clips are supplied in tape and reel packaging for automated placement, and reduce manufacturing costs by eliminating time-consuming secondary assembly operations.

www.harwin.co.uk

MOUSER SPEEDS DESIGNS BY OFFERING TI WEBENCH DESIGNER TOOL

Mouser Electronics is now offering an online software design tool from Texas Instruments that delivers customized designs in mere seconds. WEBENCH Designer lets designers generate, optimize and simulate designs that conform to their unique specifications. This TI design tool gives designers the advantage of being able to make value-based tradeoffs at a design, system and supply chain level before their design is committed to production. WEBENCH is ideal for a variety of designs, including power, lighting, filtering, clocking and sensing.

Mouser Electronics supports the complete design with its breadth of in-stock product from TI and other leading suppliers. WEBENCH returns a complete Bill of Materials.

"TI WEBENCH Designer tools give design engineers a compelling, proven way to quickly and accurately simulate power converter circuits," said Kevin Parmenter, Mouser's Director of Technical Resources. "Designers can be assured that when they build a circuit, it will work successfully as simulated in the intended application, reliably over time and temperature."

www.mouser.com

MOUSER ELECTRONICS

Two New High-Temp/Harsh Environment MLCC Series From AVX

AVX Corporation has updated its advanced SpiCalci 8.0 SPICE modelling software with the addition of two new high temperature multilayer ceramic capacitor series for power electronics employed in harsh environment applications such as down-hole oil drilling. Now featuring the SMX-style stacked, switch mode power supply (SMPS) MLCCs and SXP-style encapsulated, radial-leaded MLCCs SpiCalci 8.0 helps design engineers validate circuits before they are built by allowing them to simulate frequency performance plots and other data for specific AVX components.

Both series which are rated for up to 200°C and exhibit low ESR, ESL and DC leakage in addition to excellent high frequency performance. They are available in two dielectrics (C0G and X7R/X9U), designed to exhibit low ESR/ESL, rugged mechanical shock and vibration capabilities, and a wide frequency response in high pulse, high current and high temperature applications up to 200°C.

Both series are also well suited to DC filters in high power, high frequency motor drives and high pulsed-current circuitry.

www.avx.com

Panasonic's Short And Long Stroke Micro Switches Available Through TTI Inc

TTI Inc now stocks Panasonic's robust EVQPL series short stroke micro switches and EVPAS series long stroke micro switches featuring many different push force varieties.

New rubber dome type EVPAS series switches have a size of 6mm x 6mm (square) x 5mm with only two terminals. The rubber dome feature enables a dustproof structure with a silent superior snap and extra soft feeling. Available with a stroke of 1.0mm or 1.3mm and equipped with an actuator (push plate), the switch guarantees high operability for a wide range of applications, such as operating switches for electronic car equipment, operating switches for mobile devices, and electronic music instruments.

Further technical details include a travel of 1.0mm or 1.3mm, excellent solder ability with two terminals, excellent light-touch operation feeling, an operating temperature range of -40˚C up to +85˚C, and 30k-100k lifecycles with a variety of push forces 1.6N, 2.0N, 2.5N, 3.0N and 3.5N. Reflow soldering is also available.

www.ttieurope.com

SHORTAGE OF DIGITAL EXPERTISE THREATENS TO LIMIT GROWTH PROSPECTS OF UK PLC

Recent research by Korn/Ferry Whitehead Mann revealed a digital-skills gap in the boardrooms of the UK's largest companies which may threaten growth prospects. The survey found that only one 'digital' Non Executive Director (NED) was appointed to the FTSE 100 in the whole of 2012 and just 1.7% of FTSE 100 NEDs can be classed as 'digital'. 'Digital' NEDs are defined as those executives that have spent the bulk of their careers either in companies where the Internet is central to the business model or in strategic roles focused on leveraging the Internet.

The situation was only marginally better in the FTSE 350, with eight such 'digital' NED appointments being made in 2012 – a pace that hasn't picked up in five years. Companies have added executives with marketing, human resources and legal backgrounds to their boards at a much faster rate than they have appointed those with digital expertise. This is despite the fact that the UK now has the largest digital economy in the G-20 by proportion of GDP.

PROFESSOR DR DOGAN IBRAHIM, Near East University in Nicosia, Cyprus: The survey carried out by Korn/Ferry International is very important as it has revealed the shortage of 'digital' Non Executive Directors across the UK. NEDs play an important role in policy making, planning and monitoring the performance of executive directors and management. The need for experienced digital NEDs will undoubtedly help to bring new opportunities and challenges to companies engaged in technology, particularly since most industries have digital exposure.

Perhaps the solution is to appoint more NEDs with digital expertise instead of appointing those with traditional skills such as marketing, accounting and legal fields. The NEDs should ideally come from digital industries, such as engineering, IT and related fields.

BARRY MCKEOWN, RF and Microwave Engineer in the Defence Industry, and Director of Datod Ltd, UK: NEDs have no place in an unquoted company; in PLCs they are essential for governance. Unless PLCs are Luddites, I fail to see how this, so-called 'lack of digital expertise' threatens to limit growth.

Tomorrow's executives cannot possibly fail to be immersed in today's digital environment. Arrangements favouring specialisation play well to their erection and retention. These silos need to be taken down and all executives educated in the skills of the digital economy, such that future technological improvements can be easily assimilated. Accordingly this report's authors have missed the whole point of why NEDs are required in PLCs.

MAURIZIO DI PAOLO EMILIO, PhD Engineer, University of L'Aquila/INFN, Italy: Technology has a great potential to bring about change. The Internet is bringing a revolution along with it. Access to information, combined with global supply and demand, is reshaping established conventions and destroying old-world definitions. Interconnected societies are the global engine that transforms people from employees to micro entrepreneurs.

Industry estimates suggest there will be some 50 billion devices connected to the Internet around the world by 2020 – more than eight for every man, woman and child. These will range far beyond phones and tablets to include coffee machines, washing machines, fridges to cardiac heart monitors and even cows, which would be monitored for milk output via a Wi-Fi link.

HAFIDH MECHERGUI, Associate Professor in Electrical Engineering and Instrumentation, University of Tunisia: Communication and information technologies have helped make the new economy a digital one. This digital economy is in the middle of growth and is the principal lever of innovation across all sectors, such as trade, industry, services, agriculture and so on.

The digital revolution continues to transform production, distribution and indeed consumption processes, as well as our lifestyles. So, when the new report concerning 'digital' NEDs highlights a situation where there's a lack of such executives across these sectors, then we should stand up and listen. After all, any organization can play an important role in the digital space, which has proven to be crucial for the development and growth of any industry.

Industry estimates suggest there will be some 50 billion devices connected to the Internet around the world by 2020 – more than eight for every man, woman and child

Considering the UK is one of the world's industrial leaders, then PLCs should be obliged to restructure, at least by:

- Allowing access to digital networks.
- Developing digital content.
- Encouraging diversification of their digital services and, therefore, users.
- The restoration of governance and the ecosystem of the economy as a whole.

It is also necessary to encourage the small and medium-size companies (SMEs) to have their executives be 'digital'. Finally, I want to add that 'going' digital is a growth- and job-creation factor, so it is crucial to continue to support this field and its inclusion in all sectors.

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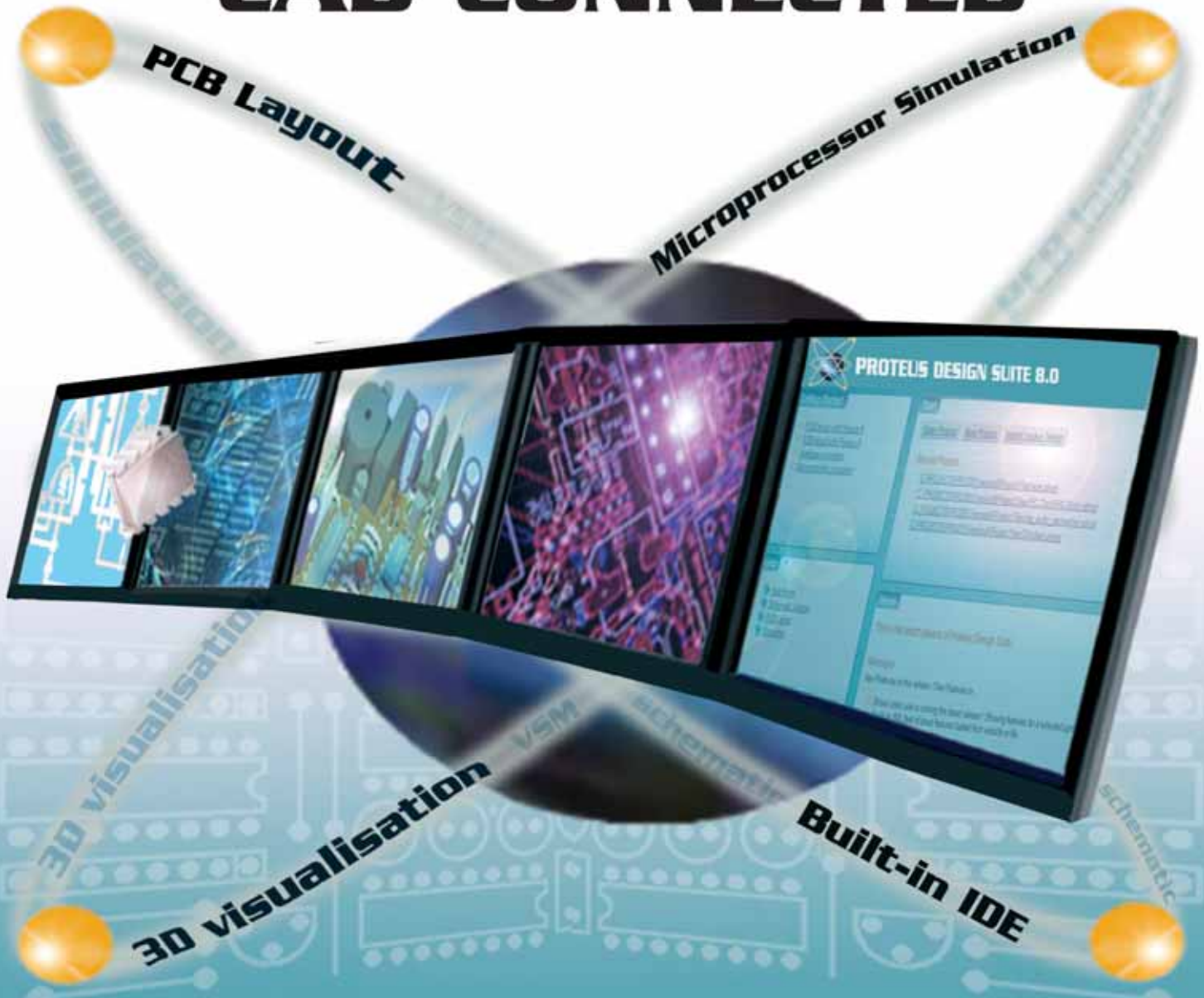

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