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INADEQUATE SECURITY IN SMARTPHONES

Mobile applications have become increasing popular in recent years, and modern smartphones can now offer such an array of apps it is often hard to imagine life without them. But whilst these apps make everyday lives more convenient, they are also providing hackers with new and easier ways to steal data.

It could be argued that when mobile applications first materialised, they were seen as no more than amusing gimmicks, allowing friends to impress one another with what their new smartphone could do. At first, businesses found it hard to envision the potential benefit from utilising mobile apps. This, however, soon changed and businesses started to embrace them as viable solutions for their operational needs.

Sadly, there is often a complete lack of understanding of the security threat posed by mobile applications, leaving businesses unable to fully appreciate the risk they are accepting by adopting them. For example, 'secure' storage applications are commonly used as a way to store passwords, intellectual property (IP), banking details and other sensitive information. While these applications claim to be secure, the reality can be very different. A hacker with malicious intent can easily extract that information. If an employee uses such an app, and their phone is stolen, it could lead to company information being stolen.

It has often been said that there is more technology in a modern smartphone than the rocket that sent man to the moon. For sure smartphones are more powerful than a standard desktop computer in the early 2000s. We all know that hackers targeted desktops, and now the spotlight can be turned onto mobile applications as a new vector of attack.

Recent articles and presentations by security experts across the globe have highlighted just how inadequate mobile application security currently is. Commonly identified issues range from sensitive data being stored and transmitted without protection, inadequate server side protections, inefficient user protection and more.

At times, attempts at securing mobile applications can be observed, but these are often poorly implemented. Such an example would be an application encrypting sensitive data, but then leaving the decryption key within the application code. This is similar to using a safe to contain important items, but then writing the lock combination on the side. At best it creates a false sense of security, at worst the data will be stolen.

> *It has often been said that there is more technology in a modern smartphone than the rocket that sent man to the moon*

There are a number of factors as to why the current security landscape of mobile apps is so poor. Developers may be more focused on creating an application that is exciting and visually appealing, they may be under time pressure to get an application released ahead of the competition, or it may simply just be that they don't know how to make their applications secure.

Not so long ago, if you were to walk into a bookstore and search for a book on developing mobile applications, you would be hard pressed to find one which had any real focus on security, at best it may have a page or two covering the subject. But, within the last twelve months, an increasing amount of news articles have begun to highlight the real threat of mobile application security. Groups of security experts, such as those at the OWASP Mobile Security Project, are beginning to supply the information needed to assist both developers and security experts in developing secure mobile applications.

OWASP has already created a number of popular testing frameworks relating to various areas of information security. The Mobile Security Project, although in its infancy, already provides a working methodology, which highlights current key threats facing mobile apps, key areas of testing that should be performed on all mobile apps to ensure security, and also provides information for developers wishing to make their apps more secure.

There is a need for businesses to consciously acknowledge the threat posed by mobile applications if they want to exploit the potential business benefit afforded by new technology, and take proactive steps to ensure they are not left vulnerable. Ensuring that mobile applications are properly assessed can help in providing a more secure solution, and mitigate potential threats.

Information Risk Management Plc (IRM) is an international information security consultancy (www.irmplc.com)

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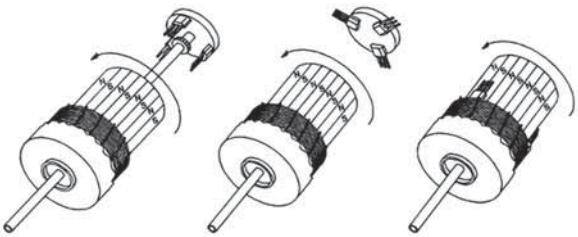
NEW GENERATION BLDC MOTOR SENSORS REMOVES THE NEED FOR CHOPPER STABILISATION



Honeywell Sensing and Control's new ***non-chopper-stabilized sensors*** *for use in brushless DC (BLDC) motors*

Honeywell Sensing and Control has developed new sensor technology for use in brushless DC (BLDC) motors that eliminates the need for chopper stabilization, resulting in a product that has faster response time, greater accuracy and minimal electrical noise. At the heart of the new technology is a quad Hall element and proprietary programming.

Honeywell tested the new non-chopper-stabilized sensors against a number of traditional chopper-stabilized products – including those with claimed higher sensitivity. The test involved mounting and centering samples as close to each other as possible, so all are in the same environment, on a circular target with 48 magnetic pole pairs used to trigger the product samples. All results were measured against a Top Dead Center (TDC) trigger that had a very fast response time.

Results showed that the non-chopper stabilized parts had a repeatable output with a response time between 10µs and 20µs faster than chopper-stabilized products, including the high-sensitivity samples. Testing also showed that even if the repeatedly issues could be overcome, the chopper-stabilized sensors still showed a slower response time resulting in lower efficiency.

BLDC motors are growing in popularity due to their higher energy efficiency using electronic commutation versus mechanical commutation to control power distribution to the motor. However, most BLDC motor designers turn to chopper stabilization to counterbalance the sensitivity and stabilization issues.

With new technology such as Honeywell's, OEMs can get all the high sensitivity and stability requirements across a range of temperatures that are required in different sectors, such as robotics, portable medical equipment and HVAC technologies, and appliances where quieter and more efficient motor performance is of critical importance.

The Fabric Revolutionising Wearable Electronics Is Now On General Sale

ElekTex, the electro-conductive fabric touch-pad from Eleksen, is being offered for sale to all interested parties through Metis Partners, Glasgow-based intellectual property (IP) specialist firm.

ElekTex is used for making flexible, durable and rugged fabric touch-screen interfaces. It heralds a new era of wearable electronics and smart clothing, and also new types of consumer electronics systems, industrial wear and toys among others.

Despite its flexibility, the Eleksen sensor product is very durable, having been tested in over one million operations. It has also undergone very stringent automotive standards' testing (including puncture testing).

Because of its construction, using fabric conductive-ribbons instead of wires, it is not easily damaged during assembly, unlike many other electromechanical alternatives. It is extremely light-weight, particularly in comparison to standard switches and controls, which points to its possible application in future generations of road and air transport.

Now Metis Partners is offering buyers the once-in-a-lifetime chance to purchase Eleksen's intellectual property (IP) assets, including an international patent portfolio protecting the technology's USP (unique selling proposition), i.e. the ability to produce fully controllable electronics via integrated sensors on items such as clothing and accessories.

"The international protection of its 30 patent families means that its potential for global exploitation is immense. We are fully anticipating keen interest in Eleksen from a wide spectrum of potential buyers," said Nat Baldwin of Metis Partners, who is in charge of co-ordinating the sale.

"Eleksen has revolutionised the way people can use electronic devices and has done away with the need for hard touch-pads," he added.

The ElekTex wearable electronics technology is now available to anyone interested in it through Metis Partners in Glasgow

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*A shipping charge of £12.00 will be billed on all orders of less than £50.00. All orders are shipped via UPS for delivery within 1-3 days (dependent on final destination). No handling fees. All prices are in British pound sterling and include duties. If excessive weight or unique circumstances require deviation from this charge, customers will be contacted prior to shipping order. Digi-Key is an authorized distributor for all supplier partners. New product added daily.

ecia ecsn CEDA

REDEFINING DISTRIBUTION: THE DIGI-KEY DIFFERENCE

Snowflakes drift across a cold, grey sky, blanketing the veritable sea of cars and trucks outside of a large, unassuming building in northern Minnesota. Outside the scene is quiet and serene, but inside, the flurry of activity is a stark juxtaposition. Each day, an average of 16,000 packages are packed and shipped from this single facility in the small town of Thief River Falls, Minnesota. The uninitiated would most likely have no idea that this rural community of less than 9,000 people houses the sixth largest electronic component distributor in the world. Shipping electronic components worldwide from such a remote location is one of many ways in which Digi-Key Corporation eschews traditional methods and beliefs regarding electronic component distribution.

This business revolution began in 1972 with an idea and a motivated ham radio enthusiast. While in college, Dr. Ron Stordahl assembled and began selling a digital electronic keyer kit for sending radiotelegraph code for ham radio operators. It was called a "digi-keyer". While sourcing parts for his own projects, he saw a need for individual components by enthusiasts such as himself who were unwilling or unable to purchase the large quantities of components sourced directly from manufacturers. He began selling his excess parts and soon a company was born, offering customers just the right number of components for their particular project.

Jumping forward 40+ years, Digi-Key continues to be one of the fastest growing electronic component distributors in the world, surpassing $1.5 billion in annual sales. The company's success is directly related to a unique perspective on traditionally held tenets of the electronic component industry. Digi-Key's innovative approach continues to reap unparalleled growth for the company, reflected in double-digit growth figures for 2013 when compared with a flat-to-down industry average, as well as in the company's continual ranking as the industry's most preferred distributor by independent studies.

So what does make Digi-Key different?

A NEW HYBRID MODEL EMERGES

Most distributors fall into one of two categories: high-service (formerly known as catalog) or broad line. The consensus throughout the industry is that you can adhere to one or the other, providing the type of services associated with that category of distributor. However, today's next-generation of engineers and purchasers are searching for more than just a channel through which to source parts. Supply chain services, expert technical support, and rich online content are just a few examples of the additional value customers expect to find when choosing a distributor.

Digi-Key has developed a distribution model that bridges the gap between these types and ushers in a new way of thinking with regard to sourcing electronic components. The company's hybrid, "Prototype to Production®" model emphasizes a commitment to the engineer and the purchaser, supporting the design process from inception, through new product introduction, all the way through to production.

The model marries the largest selection of in-stock product in the industry with a wealth of online resources. Customers can access datasheets, white papers, technical articles and videos, as well as 24/7 tech support via www.digikey.co.uk. Digi-Key also employs a unique, "virtual" FAE model, where each Applications Engineer is based in the Thief River Falls facility. Each AE is able to leverage the collective knowledge of the group and provide a much higher level of service to the customer.

Digi-Key's hybrid model provides a unique stability and resistance to industry trends. As the market fluctuates, the company's flexibility and ability to weather swings in demand and market shortages has allowed for consistent, steady growth for the company, even through unforeseen natural disasters and interruptions in business continuity, such as the 2010 recession.

ONE MILLION IN-STOCK COMPONENTS, HASSLE-FREE BUYING

One of the strongest differentiators Digi-Key offers is the company's unequaled breadth of product. The company stocks over one million electronic components in their 74,000 square meter facility. This is the broadest portfolio of electronic components available for immediate, "off-the-shelf" delivery in the industry, and provides unmatched value for their customers.

Keeping such a significant amount of products in stock is very different from the historical patterns throughout the industry. Traditional, broad line distributors are highly focused on inventory turns, with the goal of stocking as little inventory as possible. Digi-Key focuses more on fill-rates, with the ultimate goal of maintaining 95-percent in-stock levels for the products carried. Larger competitors need to concern themselves with return on working capital, Wall Street demands, and other public company expectations while Digi-Key can focus its energy entirely on what is best for the customer.

The company's unique hybrid model lends itself well to keeping an exceptionally high volume of components in stock, as the variety of types of buyers turning to Digi-Key for their component needs

allow the company to "burn down" excess inventory rather quickly. From the end customer's perspective, the value of immediate part availability and rapid fulfillment is one of Digi-Key's primary strengths over the competition.

In addition, Digi-Key is an authorized distributor of each product sourced from their over 650 suppliers. This assurance of quality, manufacturer-direct product gives customers peace of mind when choosing products for use in their designs and projects. With counterfeiting concerns on the rise, Digi-Key's model ensures that the end customer is acquiring genuine parts, from authorized sources.

Digi-Key's overall goal is to provide the easiest possible way to buy electronic components. Customers can go to the website and click "buy" with the knowledge that the products will be in stock and available for immediate shipment anywhere in the world. With website traffic that rivals consumer sites such as Amazon, as a business-to-business ecommerce giant, Digi-Key understands how to serve customers by making it fast and easy to purchase parts online.

The ease of use enjoyed by customers prompted a move into production quantities, as customers often asked, "It was so easy to manage the first transaction; if I need 1,000 pieces can you have them ready?" Customer demand led the company into developing a strategy to support production level quantities of electronic components. Customers soon found that Digi-Key was able to effectively service these types of orders from the currently available inventory pool.

FINDING THE SWEET SPOT: HIGH-MIX, LOW VOLUME

Though the company has moved into the production space, they are not looking to unseat the largest broad line distributors. Digi-Key has found a niche in the "high-mix, low volume" space, supporting prototyping and short production runs, as well as filling stock deficiencies with larger customers.

"We are not in the long-run production business. We are an ideal source for production runs of anywhere from 100 to 100,000 units. Runs of a million or more units really do not fit with our model," said Mark Larson, Digi-Key President. "Digi-Key's strong inventory position allows the company to provide a flexible option for companies looking to produce short production runs, as well as supporting shortages and unexpected usages within larger corporations."

Digi-Key understands the complexities of the product design process and is committed to providing the best possible systems and tools to support both the design engineer and the purchaser – from prototype to production. The entire model is built around the company's broad and deep inventory model that leverages what consumer organizations know to be true – long tail is a differentiator. Not unlike large retailers like Wal-Mart, buyers know that in the world of electronic components, if it exists, most likely they can find it at Digi-Key – faster and easier than anywhere else.

In addition to serving the engineer ordering one or two parts online, Digi-Key's model scales to support larger volume buyers who have special requirements such as special pricing, supply chain offerings, forecasting, bonded inventory and other customized services. With over 300 resources dedicated to managing assigned customer accounts, Digi-Key has the same level of expertise as the larger broadline distributors, complementing the company's proficiency in ecommerce and online services.

PRIVATE COMPANY, PUBLIC RESULTS

One would think that to achieve such incredible results, a company must be public, leveraging investors to propel the company forward. This is another way in which Digi-Key separates itself from other top electronic component distributors. As a privately held organization, the company has more freedom when it comes to reporting strategies and financials and is exempt from some of the pressures and demands of investors. Instead of answering to Wall Street, company leaders feel strongly about the company's unique ability to focus first on the best interests of the customer.

"Digi-Key has always been privately owned. This allows us a unique advantage over the majority of traditional distributors," noted Larson. "While there are benefits to a public designation, we feel that being private allow us to focus less on stockholders and more on improving the service we provide to our customers. You might say that our customers are the 'stockholders' whom we ultimately report to. Our continued top rankings in customer preference and exponential organic growth over the past decade are clear indicators that we are doing things right."

2014 AND BEYOND

As Digi-Key continues to expand globally, the company is focused on continuing to provide the same level of service, enjoyed by current customers over the past 40 years, to more and more customers worldwide. The company's next-generation approach to the way in which they conduct business has turned the industry on its head, and they do not intend to stray from this tradition of innovation. Digi-Key's hybrid model has become the gold standard in distribution, and is well positioned to adapt to fluctuating market changes. Learn more by visiting **www.digikey.co.uk.**

Snake Oil

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Engineer-time is always a valuable resource and, like all such resources, it is natural to be miserly with it. Engineering managers increasingly tend to view as rank heresy any activities other than "chained to the bench all day, working". This, in turn, reduces the availability of their engineers for any other function, such as talking to the suppliers of the very parts these engineers need to use.

Unfortunately, when a supplier does come up with something worth advertising (such as, in the low-power radio industry, a new RF part) and sends out the sales representatives to drum up interest, there is an increasing reluctance to actually "waste" engineer-time meeting them. But someone does!

Imagine yourself as a manager, talking with a supplier of those potentially useful parts, with no technical staff at your meeting. Can you see the potential risk here?

You are walking into this minefield if:

1. The suppliers promise you a new device, or system, or method of doing things that is at least ten times better than anything you think you currently have. It has more range for the same power, it has really impressive support tools, and they show you product BOMs that cost less than anything you currently have. Sounds awesome, right?!

2. You meet one (or more) promising new customers and, based on the manufacturer-supplied information rather than actual engineering input, you and the customer "design" a wonderful new product, right down to the estimated bill of materials costing and the physical size. It doesn't need much (if any) engineering input because the new way is so wonderful. You know it'll work, because you've seen the demonstrations.

3. You present the finished design to engineering to rubber stamp and "do half a day of layout and write a bit of code". The job will be done in a coffee break, won't it?

4. Only at that point will the actual limitations of the device pop up (see box) and you're left with a guaranteed failure and a lost customer, because any actual RF design that your engineers can produce either won't fit the mechanical limits, the price, or the (promised) performance.

Allowing non-technical staff to specify the technology or component parts used in a future design without input from the engineers who will be executing that design is lunacy, yet it happens time and time again

I'm not saying this is inevitable, but be careful. I wish I could say that I have only seen something like this happen once, but where the subject has a technical content there is no substitute for engineering input, as early in the planning stage as possible, and definitely before irrevocable decisions have been made (such as promises to customers).

Allowing non-technical staff (procurement managers, sales and marketing) to specify the technology or component parts used in a future design without input from the engineers who will be executing that design is, when looked at in isolation, lunacy, yet it happens time and time again.

Gamble a few hours of that all too expensive engineering effort; get the people who are using the parts to talk directly to the suppliers – it will save a fortune in the long run. ●

THE MISSING LINKS?

Here are a few subtle things that the supplier isn't telling you – or they might be, but without an engineer there to ask embarrassing questions, no-one will notice until it's too late:

- **The device is in a sci-fi package that your factory can't place.**
- **The lead time is two years, and sample silicon is six months away.**
- **The MOQ (minimum order quantity) is a hundred thousand parts.**
- **Only pre-production (and not fully working) silicon is available.**
- **The chip actually costs twice as much as a discrete implementation.**
- **It looks like it meets a specific spec, but actually (in the fine print) doesn't.**
- **It looks like it meets a specific spec, but only with £5 of external parts.**
- **The demo BOM cost doesn't include a proper TCXO, or input filters.**
- **There is no AF output, and/or no AF input... Or no RSSI.**
- **The software interface is amazingly awkward.**
- **It takes half a second to initialise if powered up from cold.**

I have actually experienced all of these at one time or another.

QSI Corporation

QSI Corporation deploys XJTAG through development, production and service

In activities spanning board development, contract assembly, and after-sales service, XJTAG boundary scan is enabling QSI Corporation, the American developer of rugged embedded systems, to shorten time-consuming test tasks and pinpoint hard-to-find faults such as bad vias in multi-layer boards – and deliver powerful capabilities without requiring expensive add-ons.

QSI Corporation, located in Salt Lake City, Utah, USA, designs and manufactures rugged Human Machine Interface (HMI) modules and Mobile Data Terminals (MDT) for industrial OEMs and commercial vehicle systems integrators. The company's products include character and graphic terminals tested to comply with standards such as NEMA, IP, MIL-STD, CE, and UL. The terminals withstand high levels of shock, vibration, humidity, and other environmental conditions. They are programmable, customisable, and feature many configurable hardware options to match customers' exact needs.

The boards for QSI's HMI and MDT products are assembled by a manufacturing partner, which tests the finished boards using fixtures provided by QSI. However, if a defect prevents the core logic from operating, the fixture cannot be used. QSI has overcome this challenge by incorporating the XJTAG boundary scan system into the test equipment provided. The run-time-only XJTAG variant, XJRunner, makes this a cost-effective option. QSI is also using XJTAG in their own technical departments, including engineering and product servicing.

Because the company's products are subjected to rigorous usage in the field, QSI aims to provide responsive service and repair facilities for their customers. Using conventional test techniques to diagnose faults in returned units, service engineers could expect to spend more than one hour per board to probe all of the data, address and control lines. "Using XJTAG in our service department has taken a one- to two-hour task and solved it in 15 minutes," explains Eric Anderson, Electrical Test Engineer at QSI.

According to Anderson, two of the most powerful aspects of XJTAG that have enabled this dramatic speed up are the XJEase high-level scripting language and the graphical environment that helps users set up projects and visualise the circuit under test. "The scripting language is a very powerful feature that allows us to test almost any device connected to the processor. We are using it to test components from LEDs to ROMs," Anderson continues. "Moreover, we can test devices supporting interfaces such as I^2C and SPI without having to buy expensive add-ons, which some other systems require. XJTAG provides online libraries that allow us to test these devices at no extra cost."

Describing XJTAG's graphical application, XJAnalyser, Anderson highlights the control it provides as being central to reducing test and debugging time. "XJAnalyser gives us complete control of most of the pins of a processor," he says. "We are able to toggle individual pins, which has helped trace obscure faults like bad vias in minutes rather than hours."

The QSI engineering group is also using XJTAG to bring up new designs. The company's latest board has two JTAG devices, and Anderson says the engineering team has used XJTAG to program and test one of the devices, and then to test the remainder of the product. "There is so much freedom in XJTAG that other testers do not provide. As engineers, we want to be able to control every part and see exactly what is happening at any place in the system. XJTAG gives us that freedom," he concludes.

opinion

Eric Anderson
Electrical Test Engineer
QSI Corporation

"XJTAG has taken a one- to two-hour task and solved it in 15 minutes. The XJEase scripting language is a very powerful feature that allows us to test almost any device connected to the processor. We can test devices from LEDs to ROMs, and can also test I^2C and SPI devices without having to buy expensive add-ons."

"We can also toggle individual pins to trace obscure faults within minutes. As engineers, we want to be able to control every part and see exactly what is happening at any place in the system. XJTAG gives us that freedom."

Data Bank

QSI CORPORATION

Company	QSI Corporation, HQ USA
Nature of business	Design and manufacture operator interface terminals for industrial, commercial and vehicle applications
Main products	Rugged, configurable human machine interface (HMI) and mobile data terminal (MDT) products
Customers	Industrial OEMs and commercial vehicle systems integrators
Location	Salt Lake City, USA
Incorporated	1983
Web site	www.qsicorp.com

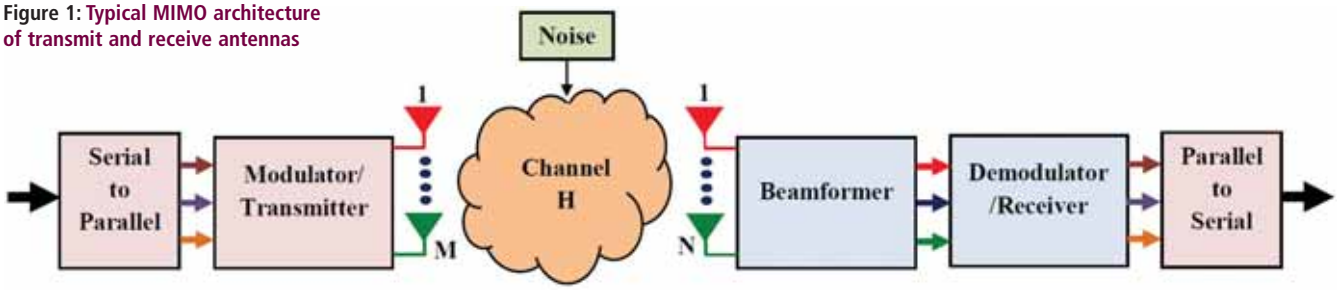


Figure 1: Typical MIMO architecture of transmit and receive antennas

NOVEL BEAMFORMING ALGORITHM FOR ULTRA WIDE BAND USED IN THE MIMO ARCHITECTURE

JAWWAD AHMED, MUHAMMAD MOINUDDIN AND **KAMRAN RAZA** FROM THE FACULTY OF ENGINEERING AT IQRA UNIVERSITY IN PAKISTAN PROPOSE A NOVEL METHOD FOR ADAPTIVE BEAMFORMING WITHIN THE UWB FREQUENCY SPECTRUM

The major issue with ultra wide band (UWB) and other types of wireless systems is the presence of interference. One impairment known as fading refers to interference in the received signal due to multiple arrivals via different paths. This produces significant variations in signal power and, therefore, it is considered destructive.

Fading generates severe distortion in radio signals. It occurs because of multipath propagation of radio signals and the relative movements of the mobile device [1].

In order to achieve higher data rate and good quality of service (QoS), it is desirable to eliminate the effects of fading without added power or increased bandwidth. One such method is 'diversity' [2], where a Multiple Input Multiple Output (MIMO) system made of a UWB antenna array is used to achieve various types of diversities.

A MIMO system can be called 'smart' if it combines its signals with a 'movable' or 'switchable' beam pattern in order to connect to the user in the desired direction. To perform this function, a smart antenna requires certain signal processing and adaptive computation, performed with adaptive beamforming algorithms [3].

There are several types of beamforming algorithms around, however if broadly classified, they belong to two major groups: supervised (or non-blind) algorighms, where a training signal is required to adjust the array weight vector; and unsupervised (or blind) algorithms, which require no training signal for weight adjustment.

A widely used supervised computational methodology for adaptive filter is known as the Least Mean Square (LMS) algorithm [4]. One of its efficient variants that uses beamforming in UWB systems is known as Constrained LMS (CLMS) [5].

Here we propose a novel algorithm for adaptive beamforming in MIMO systems, which we call Constrained Least Mean Fourth (CLMF) algorithm. Simulation results show that its performance and effectiveness are much better than existing CLMS algorithms for UWB systems.

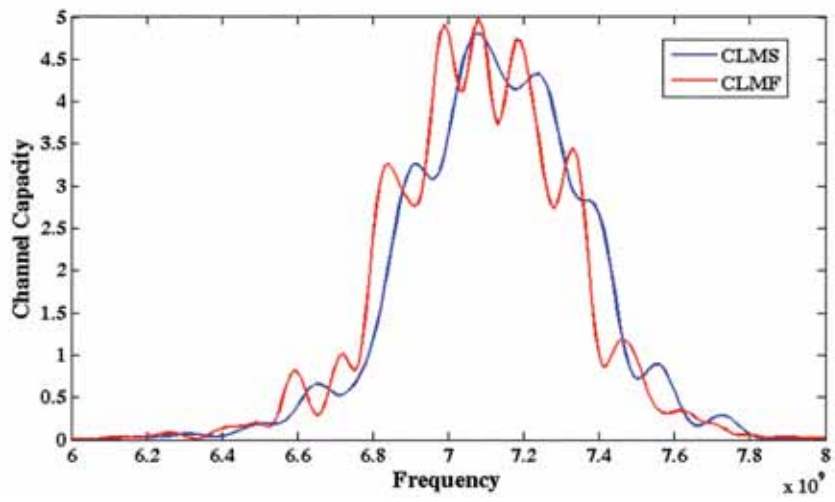


Figure 2: Channel capacities through CLMS and CLMF beamforming algorithms

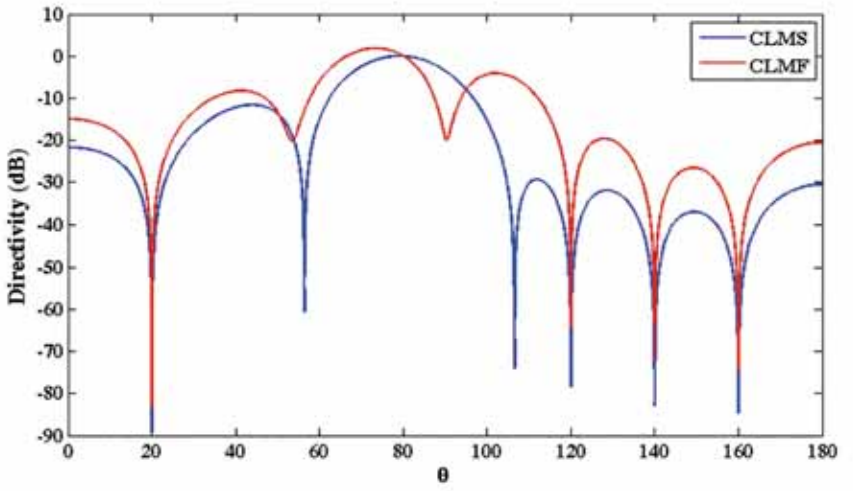


Figure 3: Directivity estimation for CLMS and CLMF beamforming algorithms

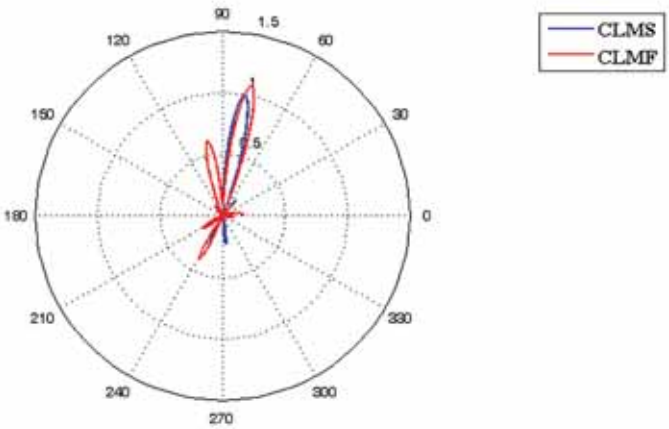


Figure 4: Radiation pattern using the CLMS and CLMF beamforming algorithms

MIMO Architecture for UWB Systems

The advantages of multiple receive antennas have been exploited for several decades [6]; however the use of multiple transmit antennas is a comparatively new concept [7]. Because of the advantage of combined transmit and receive diversity, MIMO antenna systems are widely used in UWB systems. A typical MIMO architecture of M transmit and N receive antennas is shown in Figure 1.

Two different advantages can be achieved by employing multiple antennas. First, very effective diversity system operation is achieved; and second, these multiple antennas are used to transmit several parallel data streams, which increases chanel capacity. A MIMO system has M×N diversity if it has M transmit and N receive antennas [8].

Existing Beamforming Algorithms

The adaptive beamforming in MIMO systems can effectively be achieved using supervised algorithms. Several are available, including LMS, Recursive Least Square (RLS), LMF and their linear and constraint variants, and CLMS, the algorithm most widely used in MIMO beamforming.

LMS (Least Meaning Square)

The LMS algorithm was introduced by Windrow and Hoff in 1959 [4]. It is the simplest algorithm and does not require any correlation matrix or matrix inversion. The standard weight update equation for LMS is:

$$\mathbf{w}(k+1) = \mathbf{w}(k) + \mu e^{*}(k)\mathbf{x}(k) \quad (1)$$

where w(k) is the weight vector at time k, and μ is a constant known as step size. e(k) is between the desired and actual output. The input to the LMS filter is represented by x(k).

Constrained Least Mean Square (CLMS)

The CLMS algorithm was proposed by Frost [9]. It adjusts the sensor array coefficients in real time to receive a signal of desired direction while attenuating other signals from undesired directions. The basic constraint equation of the algorithm is:

$$\min_{w} E[|e(k)|^2] \ \text{s.t}\ \mathbf{C}^{H}\mathbf{w}(k) = \mathbf{z} \quad (2)$$

where C is an N×N_c constraint matrix and z is the constraint vector having N_c constraint elements. N is the number of taps in the weight vector. The final weight update equation of CLMS is given as:

$$\mathbf{w}(k+1) = \mathbf{P}[\mathbf{w}(k) + \mu e^{*}(k)\mathbf{r}(k)] + \mathbf{F} \quad (3)$$

where P is an N×N projection matrix and F is an N×1 vector. Both are developed through a constraint matrix C [5, 10]. Moreover r(k) is the receive signal, propagated through a parallel MIMO system. If there are M transmit and N receive antennas in the MIMO system, the expression for r(k) is given as:

$$\mathbf{r}(k) = \mathbf{A}\,\mathbf{s}(k) + \mathbf{v}(k) \quad (4)$$

where A is the channel matrix of order N×M, s(k) is the parallel transmitted signal vector of order M×1, and v(k) is the Gaussian noise vector of order N×1.

The New Beamforming Algorithm for MIMO

In contrast to CLMS, we propose a new algorithm CLMF, which is much better for MIMO beamforming in the UWB range.

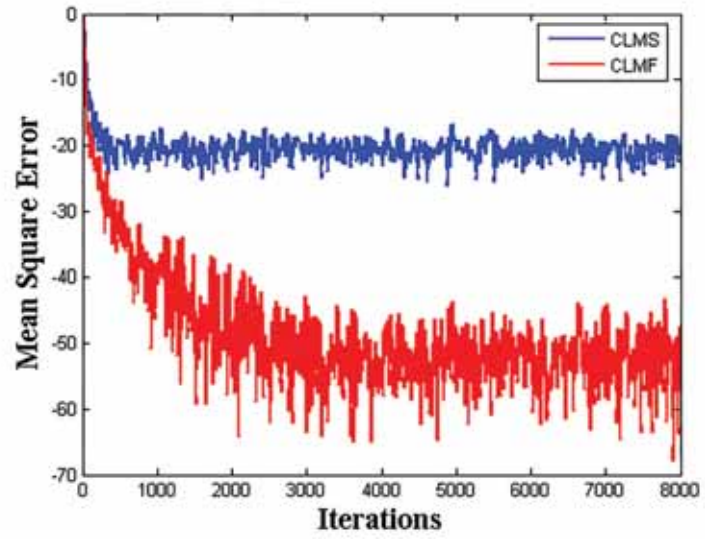


Figure 5: Rate of convergence using the CLMS and CLMF beamforming algorithms

The constraint equation for the proposed algorithm is given as:

$$\min_{w} E[|e(k)|^4] \ \text{s.t}\ \mathbf{C}^H\mathbf{w}(k) = \mathbf{z} \tag{5}$$

The weight update equation is as follows:

$$\mathbf{w}(k+1) = \mathbf{P}[\mathbf{w}(k) + \mu e^*(k)|e(k)|^2\mathbf{r}(k)] + \mathbf{F} \tag{6}$$

Simulation results have shown that the proposed CLMF algorithm is far more effective and reliable in achieving good radiation patterns, higher directivity, fast convergence rate and maximum channel capacity in UWB operation.

We investigated and compared the proposed CLMF algorithm with the existing CLMS algorithm for the following parameters which are of prime importance in any UWB system:

Channel capacity

Channel capacity can be described as the maximum rate of information that can be reliably transmitted over a communication channel. Figure 2 shows the channel capacities obtained in the UWB frequency range using existing CLMS and suggested CLMF algorithms. It can be seen that channel capacity with CLMF is higher at the centre frequency of 7.1GHz than with the existing CLMS algorithm.

Directivity

The directivity of an antenna is the relative comparison of its radiation intensity in a specific direction with that of an isotropic radiator in the same direction. Figure 3 shows comparative directivities in all directions, with the maximum at 75 degrees. It is obvious that the directivity of CLMF is higher than that of CLMS at the desired angle.

Radiation pattern

An antenna's radiation pattern is its radiation properties graphically represented with 3D coordinates. Directions of stronger radiation are called 'lobes'. The major lobe is always in the direction of maximum radiation intensity. Figure 4 shows the major lobes of radiation at 75°, obtained through CLMS and CLMF. Again, CLMF produces more gain than CLMF.

Rate of convergence

The rate of convergence is the speed at which a convergent sequence approaches its limit. Highly efficient systems have higher rates of convergence. Figure 5 indicates the convergence rate patterns for the CLMS and CLMF algorithms. It is clear that CLMF not only has a faster rate of convergence but also it has the lowest value of mean square error. ●

REFERENCES

[1] Z. Ren, G. Wang, Q. Chen, and H. Li, "Modelling and simulation of Rayleigh fading, path loss, and shadowing fading for wireless mobile networks," Simulation Modelling Practice and Theory, vol. 19, no. 2, pp. 626–637, 2011.

[2] N. Sachdeva and D. Sharma, "Diversity: A fading reduction technique," International Journal of Advanced Research in Computer Science and Software Engineering, ISSN, vol. 2, no. 6, pp. 58–61, June 2012.

[3] B. D. Van Veen and K. M. Buckley, "Beamforming: A versatile approach to spatial filtering," ASSP Magazine, IEEE, vol. 5, no. 2, pp. 4–24, 1988.

[4] B. Widrow, P. Mantey, L. Griffths, and B. Goode, "Adaptive antenna systems," Proceedings of the IEEE, vol. 55, no. 12, pp. 2143–2159, December 1967.

[5] O. L. Frost III, "An algorithm for linearly constrained adaptive array processing," Proceedings of the IEEE, vol. 60, no. 8, pp. 926–935, 1972.

[6] K. W. Forsythe, D. W. Bliss, and C. M. Keller, "Multichannel adaptive beamforming and interference mitigation in multiuser CDMA systems," in Signals, Systems, and Computers, Paciffc Grove, Calif. Conference Record of the Thirty Third Asilomar Conference on, vol. 1. IEEE, 2427 October 1999, pp. 506–510.

[7] A. Wittneben, "Basestation modulation diversity for digital simulcast," in Vehicular Technology Conference, 1991. Gateway to the Future Technology in Motion, 41st IEEE. IEEE, 1922 May 1991, pp. 848–853.

[8] J. Bach Andersen, "Antenna arrays in mobile communications: Gain, diversity, and channel capacity," Antennas and Propagation Magazine, IEEE, vol. 42, no. 2, pp. 12–16, April 2000.

[9] O. L. Frost, "An algorithm for linearly constrained adaptive array processing," Proceedings of the IEEE, vol. 60, no. 8, pp. 926–935, 1972.

[10] J. F. de Andrade, M. L. R. de Campos and J. A. Apolinario, "An L1-Norm Linearly Constrained LMS Algorithm Applied to Adaptive Beamforming", 7th Sensor Array and Multichannel Signal Processing Workshop (SAM), IEEE pp 429-432

HIGHLY LINEAR AND LOW-POWER CMOS LOW-NOISE AMPLIFIER FOR UWB RECEIVERS

JIAN LIU AND **CHUNHUA WANG** FROM THE COLLEGE OF INFORMATION SCIENCE AND ENGINEERING AT HUNAN UNIVERSITY, CHINA, PRESENT A HIGHLY LINEAR, LOW-POWER AND HIGH-GAIN CMOS COMMON-GATE (CG) LOW-NOISE AMPLIFIER (LNA) FOR UWB RECEIVERS. THE PROPOSED LNA USES CURRENT-REUSE, FORWARD-BODY BIASING, SHUNT-SERIES PEAKING AND POST-DISTORTION TECHNIQUES

In February 2002, the Federal Communications Commission (FCC) allocated 7500MHz of spectrum for unlicensed use of ultra-wideband (UWB) devices in the 3.1 to 10.6GHz frequency band [1]. The benefits of UWB technology include low power, high data-rates (up to 1Gb/s), low cost and lower interference.

UWB LNA

Being the first block of a UWB receiver, the UWB low-noise amplifier (LNA) plays a crucial role in amplifying received signals while adding little noise to them. As such, it must meet several stringent requirements, including broadband input matching, flat and high power gain, low noise figure (NF), high linearity and low power consumption.

Before now, a number of UWB LNAs based on CMOS technology have been developed [2-8]. The distributed amplifier (DA) is one of the most popular architectures for the wideband LNA design, as it provides good wideband input matching, flat gain over a wide range of frequencies and a higher third-order intercept point (IIP3) – a measure for weakly nonlinear systems and devices [2-4]. On the other hand however, the DA LNA consumes a great deal of power, occupies a large chip area and its power gain is quite low.

Resistive feedback is a good solution for obtaining wide bandwidth and flat power gain [5-7], but having to use a resistor in the feedback path reduces the power gain and degrades the noise performance.

Recently, a new topology in LNA design has been introduced, based on the cascade, with a Chebyshev input matching filter, which provides good wideband input matching and high power gain [8]; the NF, however, is degraded by the insertion loss of the filter.

A big challenge in designing UWB LNAs is the stringent linearity requirement over a wide frequency range, due to the large numbers of in-band interferences in the UWB system, and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [9] in a reconfigurable receiver. Furthermore, while the transit frequency (f_T) increases with technology scaling, the linearity worsens due to lower supply voltage and high-field mobility effects [9]. As a result, wideband linearization techniques are a research hotspot.

Linearization Techniques

A linearization approach for high-frequency wideband applications is desired. Up to now, several techniques have been proposed to improve the linearity of the LNA circuit, including the optimal biasing technique [10-11], which by optimizing the overdrive voltage ($V_{gs}-V_{th}$) can be used to achieve a peak in IIP3. However, the bias voltage range for an IIP3 peak is very narrow, making the linearity boosting very sensitive to process variations.

The derivative super-position (DS) method [12-14] uses an additional transistor's nonlinearity to cancel that of the main device. It involves MOS transistors working in triode mode [12] or in the weak inversion region [13-14]; therefore, with this method it is difficult to match the transistors working in different regions, resulting in linearity improvement highly sensitive to pressure-volume-temperature (PVT) variations.

The body biasing technique [15] is suitable for improving linearity; instead however, it degrades gain and noise performances. In [16], the post-distortion technique is applied to improve linearity. Because all transistors operate in the saturation region, it avoids the input matching degradation and it offers a robust increase in linearity.

New UWB LNA Based on Common Gate

In this article, a highly linear, low-power UWB CG-LNA is proposed. CG-LNAs have become more popular for UWB systems, thanks to their simpler input matching network, better linearity, lower power consumption and better input-output isolation, compared to common-source (CS) LNAs.

However, as we all know, the power gain of the CG LNA is

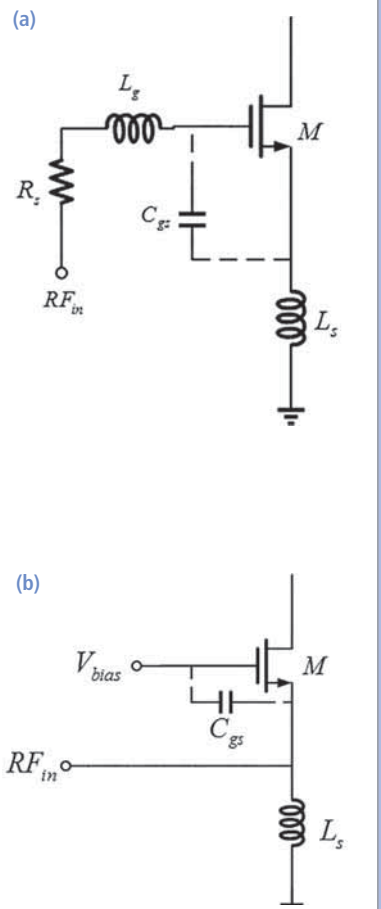


Figure 1: (a) Common-source LNA (b) Common-gate LNA

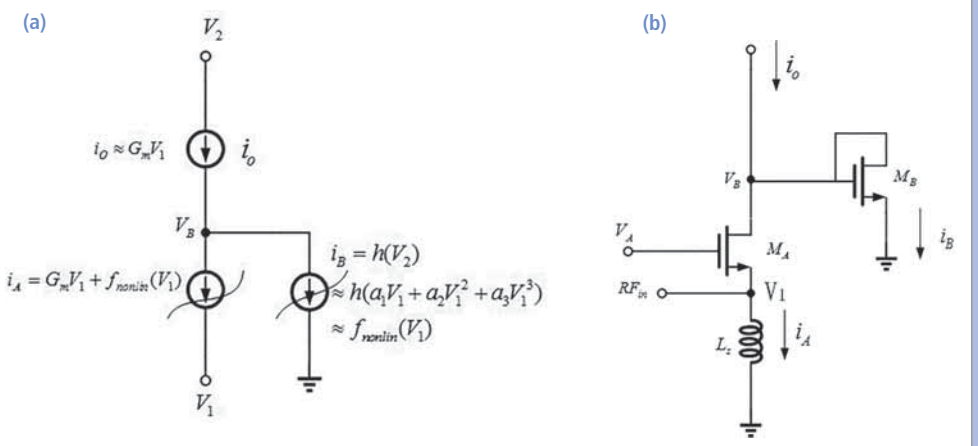


Figure 2: The schematic of the post-distortion technique. (a) Conceptual idea of the post-distortion technique; (b) Circuit implementation of post-distortion technique

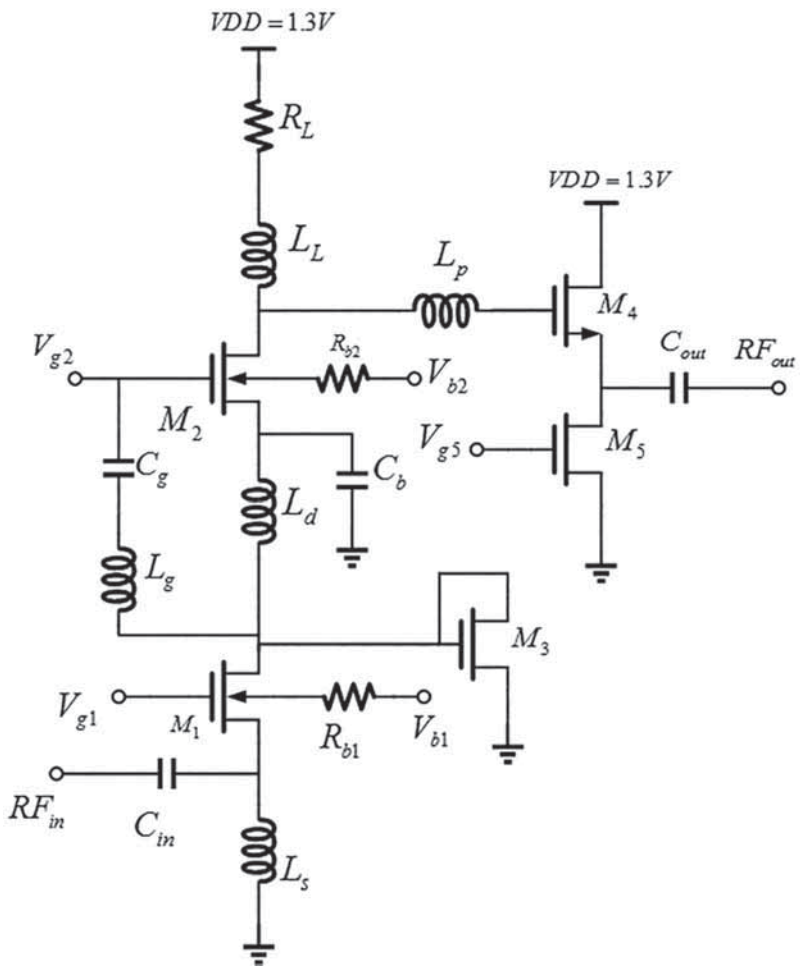


Figure 3: Schematic of the proposed LNA

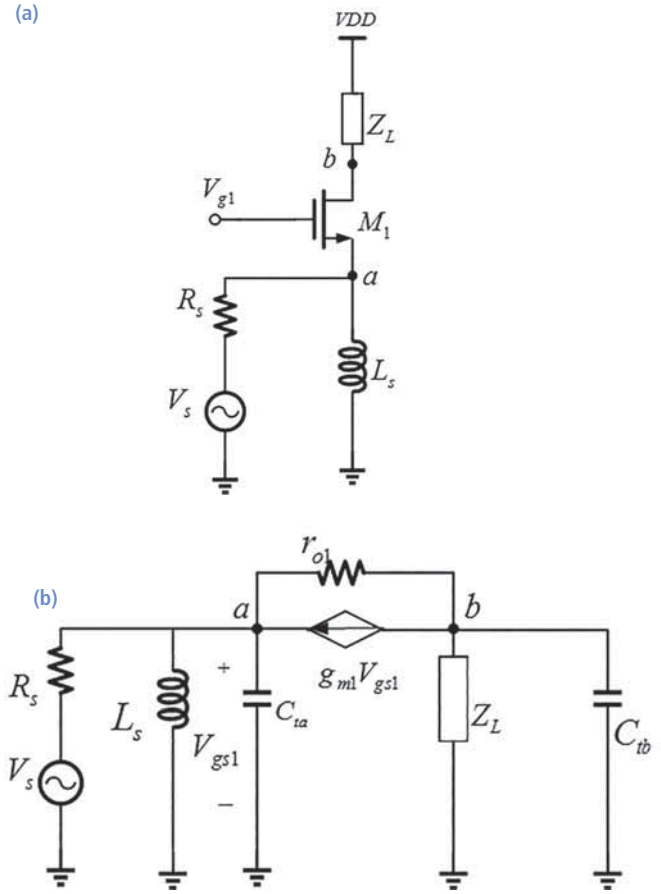


Figure 4: Schematic diagrams of the CG input stage: (a) circuit topology; (b) small signal equivalent circuit

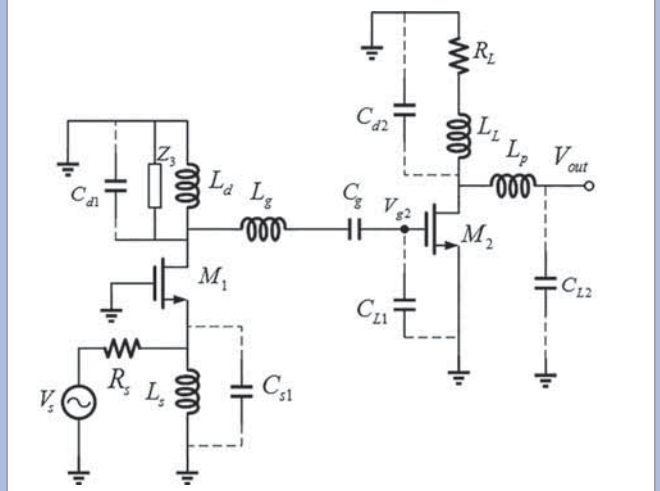


Figure 5: Equivalent schematic of the proposed LNA

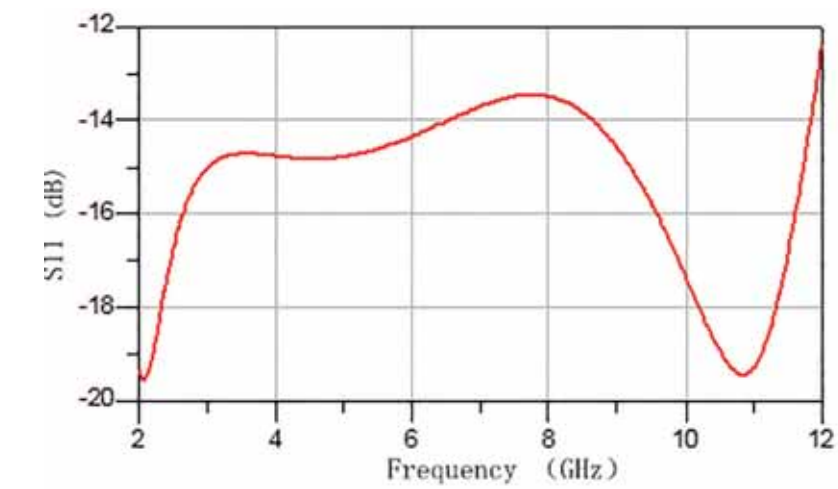


Figure 6: Input reflection coefficient (S11)

Table 1: Circuit parameter values

Devices	Design values
M_1(um)	124/0.18
M_2(um)	48/0.18
M_3(um)	9/0.18
M_4(um)	25/0.18
M_5(um)	30/0.18
L_s(nH)	4.4 nH
L_d(nH)	6.6
L_1(nH)	2.5
L_g(nH)	3.0
L_p(nH)	2.9
R_L(ohm)	50
R_{b1}(ohm)	5000
R_{b2}(ohm)	5000
V_{g1}(V)	0.59
V_{g2}(V)	0.94
V_{g5}(V)	0.6
V_{b1}(V)	0.29
V_{b2}(V)	0.29
C_{in}(pF)	5.1
C_{out}(pF)	3.4

insufficient [17], so a CS amplifier is used as a second stage. The proposed LNA circuit utilizes current-reuse and forward body biasing techniques to achieve low power consumption. In addition, shunt-series peaking techniques are used to extend the 3dB frequency bandwidth. Meanwhile, a post-distortion technique is employed to improve the linearity performance of the proposed LNA.

Input Stage Analysis

Based on the input matching characteristics, the published CMOS UWB LNA architectures can be divided into two major groups: common source (CS) and common gate (CG) LNAs [18]. The general topology of these architectures is shown in Figure 1. Figure 1a shows a conventional CS low noise amplifier (LNA) that requires at least two inductors (L_g, L_s) for simultaneous noise and input matching (SNIM). As we know, the input matching network of the CS low noise amplifier has series resonance. Assuming that the channel resistance r_s and the gate-drain parasitic capacitance C_{gd} are negligible, the quality factor (Q) of the CS LNA can be derived as:

$$Q_{CS} = \frac{1}{\omega_0 g_m L_s} \tag{1}$$

$$\omega_0 = \frac{1}{\sqrt{(L_g + L_s)C_{gs}}} \tag{2}$$

Substituting (2) into (1) yields:

$$Q_{CS} = \frac{\sqrt{(L_g + L_s)C_{gs}}}{g_m L_s} \tag{3}$$

where ω_0, g_m, L_g, L_s and C_{gs} represent the resonant angular frequency of the input impedance, the transconductance of the metal-oxide semiconductor field-effect transistor (MOSFET), the gate inductor, the source inductor and the gate-source parasitic capacitance, respectively. This architecture is inherently narrowband because of its high Q value, and achieving a wideband input match to the signal source in the presence of parasitic capacitances is quite difficult.

Figure 1b shows a typical CG LNA. The input matching network of the CG LNA has a parallel resonance. The Q of the CG LNA can be expressed as:

$$Q_{CG} = \omega_0 \frac{C_{gs}}{g_m} \tag{4}$$

$$\omega_0 = \frac{1}{\sqrt{L_s C_{gs}}} \tag{5}$$

By substituting (5) into (4), the Q_{CG} can be re-expressed as:

$$Q_{CG} = \frac{C_{gs}}{g_m \sqrt{L_s C_{gs}}} \tag{6}$$

Since L_s is intended to block RF leakage to ground, the L_s value of the conventional CG LNA is higher than that of the CS LNA, so the Q_{CS} value is higher than the Q_{CG} value. Also, obtaining a wideband input match and absorbing parasitic capacitances are relatively simple and are less affected by process variations in the case of CG topology. To sum up, the CG LNA is a suitable topology for wideband input matching.

Forward Body Biasing Technique

Portable applications such as WLAN transceivers, cell phones and sensor networks have to meet stringent performance requirements with the lowest power consumption to conserve battery life. The most efficient approach for reducing power consumption is through power supply voltage scaling.

In the proposed LNA circuit, the forward body biasing technique is employed to further reduce the threshold voltage (V_{th}). The threshold voltage of MOSFET is well known as:

$$V_{th} = V_{th0} + \gamma(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}) \tag{7}$$

where V_{th0} is the threshold voltage when $V_{bs} = 0$, γ is the body-effect coefficient, φ_f is the surface potential, V_{bs} is the voltage between body and source. Usually, $V_{bs} \le 0$, so $V_{th} \ge V_{th0}$. In order to reduce V_{th}, we let $V_{bs} > 0$, so $V_{th} < V_{th0}$. The typical value of V_{th} is about 0.5V; in the proposed LNA, $V_{bs} = 0.29\,\text{V}$, $V_{th} = 0.43\,\text{V}$.

Theory of Post-Distortion Technique

In order to obtain better linearity, the post-distortion (PD) technique is used in the proposed LNA circuit. The PD technique utilizes an auxiliary transistor's (M_B) nonlinearity to cancel that of the main device (M_A). As we can see from Figure 2b, the auxiliary transistor (M_B) taps voltage V_B and replicates the nonlinear drain current of the main transistor (M_A), partially cancelling both second- and third-order distortion terms [19]. The transistor M_B linearizes M_A as follows: First, the drain currents of M_A and M_B can be modelled as (8) and (9):

$$i_A = g_{1A}V_1 + g_{2A}V_1^2 + g_{3A}V_1^3 \tag{8}$$

$$i_B = g_{1B}V_B + g_{2B}V_B^2 + g_{3B}V_B^3 \tag{9}$$

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}},\quad g_2 = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2},\quad g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3} \tag{10}$$

where I_{DS}, V_{GS}, V_1, V_B are the drain current of the transistor, the gate-to-source voltage, the source voltage and drain voltage of M_A, respectively. Next, suppose V_B is related to V_1 by:

$$V_B = -c_1V_1 - c_2V_1^2 - c_3V_1^3 \tag{11}$$

According to Kirchhoff's circuit laws (KCL):

$$\begin{aligned} i_o &= i_A + i_B \\ &= (g_{1A} + c_1 g_{1B}) V_1 \\ &+ \underbrace{(g_{2A} - c_1^2 g_{2B} - c_2 g_{1B}) V_1^2}_{\substack{secondnd-order \\ distortion}} \\ &+ \underbrace{(g_{3A} - c_1^3 g_{3B} - g_{1B} c_3 - 2 g_{2B} c_1 c_2) V_1^3}_{\substack{third-order \\ distortion}} \end{aligned} \quad (12)$$

In order to obtain a good IIP3, the third-order distortion of the output current – the third term in Equation 12 – should be adjusted close to zero by adjusting the gate bias and size of M_A and M_B. From Equation 12 we find that M_B is added to introduce an additional degree of freedom g_{1B}, g_{2B} and g_{3B} for linearity optimization. The expression IIP3 is given by Volterra series analysis as follows [20]:

$$IIP3 = \frac{1}{6R_s \{Z_s(\omega)\} |H(\omega)| |A_1(\omega)|^3 |\varepsilon(\Delta\omega, 2\omega)|} \quad (13)$$

$$\varepsilon(\Delta\omega, 2\omega) = g_m^{\cdot\cdot} - g_{CGS} \quad (14)$$

where:

$$g_{CGS} = \frac{2}{3}(g_m^{\cdot})^2 \left\{ \frac{2}{g_m + g(\Delta\omega)} + \frac{1}{g_m + g(2\omega)} \right\} \quad (15)$$

IIP3 is mainly affected by $\varepsilon(\Delta\omega, 2\omega)$. Equations 13 to 15 imply that linearity can be improved by reducing $g_m^{\cdot\cdot}$, but that when $g_m^{\cdot\cdot}$ becomes negligibly small, $\varepsilon(\Delta\omega, 2\omega)$ becomes dominated by the second term, which is proportional to the square of $g_m^{\cdot}$.

The post-distortion technique employs an additional folded diode to minimize $g_m^{\cdot\cdot}$ and $g_m^{\cdot}$ simultaneously. Since the bias current and transconductance of M_B are much smaller than that of M_A, the post-distortion technique does not degrade the NF and gain.

Circuit Design and Analysis

The LNA was designed and simulated in the TSMC 0.18um CMOS process. Figure 3 presents the schematic of the proposed LNA, including the output buffer (M4, M5). The current-reused configuration can be considered as a two-stage cascade amplifier, where the first stage is the CG amplifier (M1) and the second stage is the CS amplifier (M2). The signal amplified by M1 is coupled to the gate of M2 by a series resonance (L_g and C_g), while the source of M2 is bypassed by C_b (C_b determines the low frequency band expansion and gain flatness).

The circuit saves power through reuse of the bias current. As we know, the power gain of the CG topology LNA is low, so a CS amplifier with gain-peaking technique, which consists of R_L, L_L and M_2, is employed in the second stage. To reduce the threshold voltage of the transistor, the forward body biasing technique is employed in this design. The post-distortion technique is utilized in the first stage (M3), reducing the nonlinearity of the main device (M1). The circuit parameters of the proposed LNA are summarized in Table 1.

Input Matching

Most RF instruments and coaxial cables have a standard impedance of 50Ω, thus the input stage of the amplifier is required to match to 50Ω for proper termination [21]. For simplicity, the body effect is ignored.

The CG input stage of the proposed LNA is shown in Figure 4. The input impedance can be derived as:

$$\begin{aligned} Z_{in}(\omega) &= \frac{1}{g_{m1} + \frac{1 - \omega^2 L_s C_{ia}}{j\omega L_s} + \frac{(1 - g_{m1} Z_L) + j\omega Z_L C_{ib}}{(r_{o1} + Z_L) + j\omega r_{o1} Z_L C_{ib}}} \\ &\approx \frac{1}{g_{m1}} \end{aligned} \quad (16)$$

where C_{ia} and C_{ib} are the total capacitance at nodes a and b, respectively. C_{gs1}, g_{m1} and r_{o1} are the gate-to-source capacitance, the transconductance and the output resistance of M_1, respectively. Z_L is the CS stage equivalent load impedance. As Equation 16 indicates, the input impedance approximates $1/g_{m1}$ over the frequency band of interest. Here, $g_{m3} << g_{m2}$; g_{m2} and g_{m3} are the transconductance of transistor M_2 and M_3, respectively. The input impedance $Z_{in}(\omega)$ seen from R_s of the CG LNA is about the same with and without the transistor M_3 present. Therefore, M_3 does not significantly affect input matching. Through simulation, we see that the input matching is good when g_{m1} approaches 26ms.

The achievable maximum power gain also depends on output impedance matching. In the proposed LNA, a simple source follower, consisting of M_4 and M_5, is employed for output impedance matching.

Gain Analysis

If the source of M_2 is perfectly grounded by C_b, the equivalent schematic of the proposed LNA can be redrawn as in Figure 5, showing the proposed LNA created by the two-stage amplifier. The first stage is a CG amplifier and the second stage is a CS amplifier. For simplicity, body effect is not considered. Voltage gain of the first stage A_{V1} can be expressed as:

$$A_{V1} = \frac{V_{g2}}{V_s} = \frac{g_{m1} Z_x}{\{Z_x + R_s(1 + g_{m1} Z_x)\}(1 + sC_{L1} Z_g)} \quad (Z_t \ \| \ r_{o1}) \quad (17)$$

Table 2: Performance summary and comparison to previously reported LNAs

Reference	[3]	[4]	[8]	[17]	[20]	This work
Maximum gain (dB)	10	8.6	15.3	14.8	11.7	18.9
Minimum NF (dB)	3.8	4.2	2.8	3.9	3.6	1.9
BW (dB)	2.7-9.1	0.03-6.2	2.5-11.7	2.4-11.2	1.5-8.1	3-11
S11 (dB)	<-10	<-16	<-10	<-12	<-9	<-13
IIP3 (dBm)	-	+1.8	-	-11.5	14.1	10
Area (mm^2)	1.57	1.16	1.04	1.1	0.58	0.7
P_D (mW)	7	9	11.6	3.4	2.62	3.1

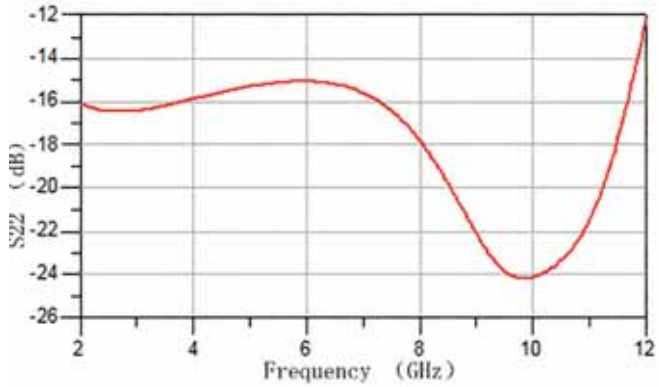


Figure 7: Output reflection coefficient (S22)

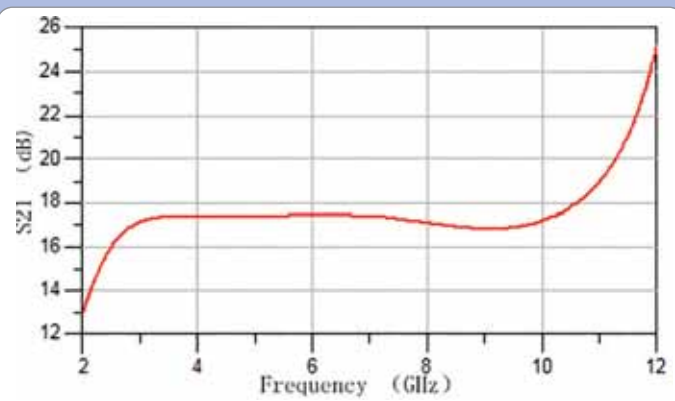


Figure 8: Power gain (S21) of the proposed LNA

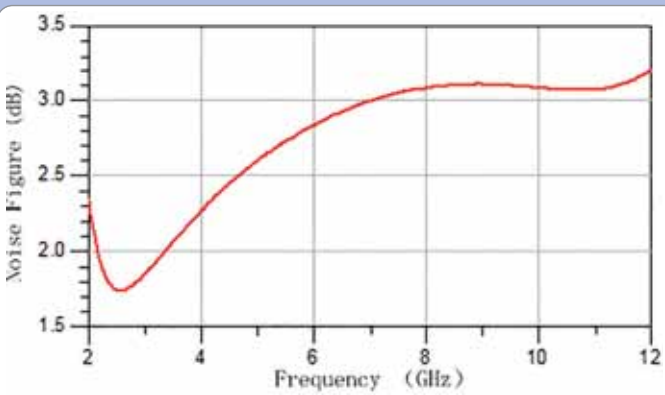


Figure 9: NF of the proposed LNA

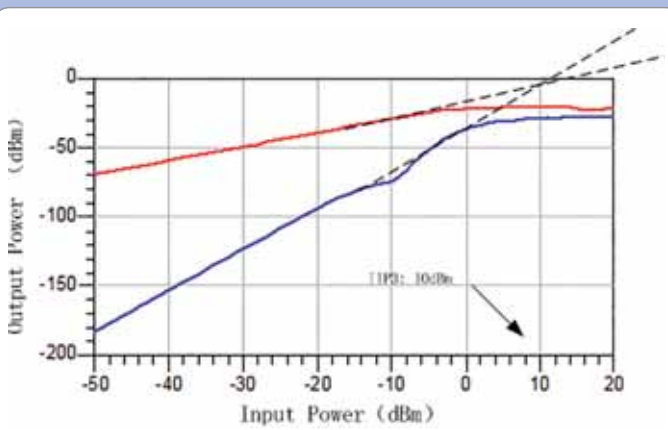


Figure 10: Input third order intercept point (IIP3) of the proposed LNA

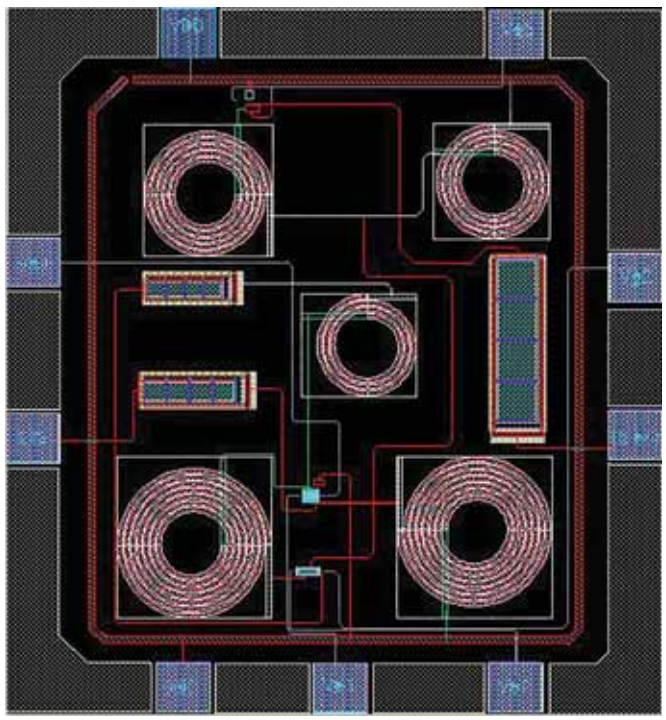


Figure 11: Layout of the proposed LNA

where:

$$Z_s = sL_s \| \frac{1}{sC_{s1}} \tag{18}$$

$$Z_d = sL_d \| Z_3 \| \frac{1}{sC_d} \tag{19}$$

$$Z_g = sL_g + \frac{1}{sC_g} \tag{20}$$

$$Z_1 = Z_d \| (Z_g + \frac{1}{sC_{L1}}) \tag{21}$$

where g_{m1}, r_{o1}, R_s, C_{s1}, C_{d1} and Z_3 are the transconductance of M_1, the channel resistance of M_1, the input source resistance ($R_s = 50\Omega$), the source parasitic capacitance, caused by C_{gs1} (the gate-to-source parasitic capacitor of M_1) and the drain parasitic capacitance, caused by C_{gd1} (the gate-to-drain parasitic capacitor of M_1), the equivalent impedance of M_3, respectively. In addition, C_{L1} is the parasitic load capacitance of the second stage. Here, the direct current (DC) blocking capacitors (C_{in} and C_{out}) are ignored for simplification.

The voltage gain of the second stage A_{V2} is given by:

$$A_{V2} = \frac{V_{out}}{V_{g2}} = \frac{-g_{m2}Z_{out2}}{1 + s^2 L_p C_{L2}} \tag{22}$$

where:

$$Z_{out2} = r_{o2} \| Z_L \| (sL_p + \frac{1}{sC_{L2}}) \tag{23}$$

$$Z_L = (R_L + sL_L) \| \frac{1}{sC_{d2}} \tag{24}$$

g_{m2}, r_{o2}, C_{L2} are the transconductance of M_2, the channel resistance of M_2, and the total loaded capacitance at the second stage output, respectively. Additionally, C_{d2} is the calculated parasitic capacitance at the drain of M_2, which is produced by the gate-to-drain parasitic capacitor (C_{gd2}). The overall circuit frequency response of S_{21} has a great flatness and higher power gain because of the cascaded combination of the first and second stage.

Noise Analysis

The first stage of a receiver is typically a low noise amplifier, and its noise figure is critical to the whole receiver circuit. For simplicity, the parasitic effects, body effects and the influence of M_3 on noise performance are ignored.

In the proposed LNA, the mean square noise voltage $\overline{V_{ns}^2} = 4kTR_s\Delta f$, the mean square noise current $\overline{i_{nd1}^2} = 4kT\gamma g_{m1}\Delta f$, $\overline{i_{nd2}^2} = 4kT\gamma g_{m2}\Delta f$ and $\overline{i_{nR}^2} = 4kT/R_L\Delta f$ are produced by the source resistor R_s, the channel noise of M_1, M_2 and the load resistor R_L, respectively. k, T, γ and Δf are Boltzmann's constant, the absolute temperature in degrees Kelvin, the thermal noise coefficient with a value from 1 to 2 in the saturation region of a short-channel Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and the noise bandwidth in hertz, respectively.

The noise factor of the proposed LNA can be expressed as:

$$F = \frac{V_{n,out}^2}{(A_V)^2} \times \frac{1}{V_{ns}^2}$$
$$\approx 1 + \frac{1}{(A_{V1})^2 R_s} \times [(\frac{Z_1}{1 + sC_{L1}})^2 \gamma g_{m1} + \frac{\gamma}{g_{m2}} + \frac{R_L}{g_{m2}^2 (R_L + sL_L)}] \tag{25}$$

where $V_{n,out}^2$ is the total noise at the output and A_V is the total voltage gain. The total voltage gain A_V can be obtained by Equations 17 and 22. From Equation 25 we can see the effects of g_{m1} and g_{m2} in achieving a lower NF. In order to obtain a low NF and low power consumption, g_{m1} should be a low value.

However, on the contrary, this would adversely affect the total NF because a low g_{m1} value would lead to the gain of the first stage being low. Alternatively, from Equation 25 we also find that a high g_{m2} value is beneficial for achieving a low NF. However, this increases power dissipation, so it is necessary to optimize g_{m1} and g_{m2}. Because both transconductances depend on the transistor width (W_1 and W_2), in the proposed LNA design the optimal value of W_1 and W_2 are 124um and 48um, respectively.

Simulation Results

The proposed ultra-wideband LNA is designed and simulated by Advanced Design System (ADS) software using a TSMC 0.18um RF CMOS process. Thanks to current-reuse and forward-body biasing techniques, the proposed LNA's supply voltage falls to 1.3V and it consumes only 3.1mW of power. The simulated input reflection coefficient S11 is plotted is Figure 6, which shows that S11 is less than -13dB from 3GHz to 11GHz. Figure 7 shows the simulated output reflection coefficient S22, showing that S22 is less than -14dB over 3-11GHz.

Power gain (S21) of the proposed LNA is plotted in Figure 8, where we can see that from 3GHz to 11GHz, the voltage gain ranges from 16.8dB to 18.9dB. As a result of shunt-series peaking technique, S21 has better flatness and a higher voltage gain.

The NF performance of the proposed LNA design is plotted in Figure 9, which shows that the range of NF is 1.9dB to 3.2dB between 3GHz and 11GHz. The IIP3 of the proposed LNA is plotted in Figure 10, which features a simulated IIP3 of 10dBm. Figure 11 shows the layout of the proposed LNA, with total chip area of 0.87x0.81mm^2 including the input and output pads.

Table 2 summarizes the performance of the proposed LNA and compares it with previous designs.

Based on the simulated results, the proposed LNA is suitable as a building block in highly linear, low power RF front-end for UWB systems. ●

REFERENCES

[1] G. Roberto Aiello ,and Gerald D. Rogerson, "Ultra-wideband Wireless Systems," IEEE Microwave Magazine, pp. 36-47, Jun. 2003.

[2] Ren-Chieh Liu, Chin-Shen Lin, Kuo-Liang Deng, and Huei Wang, "A 0.5-14-GHz 10.6-dB CMOS Cascode Distributed Amplifier," in IEEE International Symposium on Very Large Scale Integrated (VLSI) Circuits Digest of technology Papers, pp. 139-140, Dec. 2003.

[3] Yueh-Hua Yu, Yi-Jan Emery Chen and Deukhyoun Heo, "A 0.6-V Low Power UWB CMOS LNA," IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS," vol. 17, NO.3, MARCH 2007.

[4] Frank Zhang, and Peter Kinget, "Low Power Programmable-Gain CMOS Distributed LNA for Ultra-Wideband Applications," IEEE International Symposium on Very Large Scale Integrated (VLSI) Circuits Digest of technology Papers, pp. 78-81, Jun. 2005.

[5] Herbert Knapp, Dietmar Zoschg, Thomas Meister, Klaus Aufinger, Sabine Boguth, and Ludwig Treitinger, " 15 GHz Wideband Amplifier with 2.8 dB Noise Figure in SiGe Bipolar Technology," IEEE International Symposium on Radio Frequency Integrated Circuits (RFIC) Digest of technology Papers, pp. 287-290, 2001.

[6] Stefan Andersson, Christer Svensson, and Oskar Drugge, "Wideband LNA for a Multistandard Wireless Receiver in 0.18 um CMOS," IEEE Solid-State Circuits Conference, pp. 655-658, 16-18 sept. 2003.

[7] Ranjit Gharpurey, "A Broadband Low-Noise Front-End Amplifier for Ultra Wideband in 0.13 um CMOS," IEEE Custom Integrated Circuits Conference, pp. 605-608, 3-6, Oct. 2004.

[8] J.Y. Lee, J.H. Ham, Y.S. Lee, and T.Y. Yun, "CMOS LNA for full-band ultra-wideband systems using a simple wide input matching network," IET Microw. Antennas Propag., vol. 4, Iss. 12, pp. 2155-2159, Dec. 2010.

[9] Wei-Hung, Gang Liu, Boos Zdravko, and Ali M. Niknejad, "A Highly Linear Broadband CMOS LNA Employing Noise and Distortion Cancellation," IEEE Journal, Solid-State Circuits, vol. 43, no. 5, pp. 1164-1176, May 2008.

[10] Sudip Shekhar, Jeffrey S. Walling, and David J. Allstot, "Bandwidth Extension Techniques for CMOS Amplifiers," IEEE Journal, Solid-State Circuits, vol. 41, no. 11, pp. 2424-2439, Nov. 2006.

[11] Vladimir Aparin, Gary Brown, and Lawrence E. Larson, "Linearization of CMOS LNA'S Via Optimum Gate Biasing," International Symposium on Circuits and Systems (ISCAS), vol. 4, pp. 748-751, 23-26 May 2004.

[12] Yong-Sik Youn, Jae-Hong Chang, Kwang-Jin Koh, Young-Jae Lee, and Hyun-Kyu Yu, "A 2 GHz 16dBm IIP3 Low Noise Amplifier in 0.25 um CMOS Technology," IEEE Conference, Solid-State Circuits, vol. 1, pp. 452-507. 2003.

[13] Vladimir Aparin, and Lawrence E. Larson, "Modified Derivative Superposition Method for Linearizing FET Low-Noise Amplifiers," IEEE Trans., Microwave Theory and Techniques, vol. 53, no. 2, pp. 571-581, Feb. 2005.

[14] Tae Wook Kim, "A Common-Gate Amplifier With Transconductance Nonlinearity Cancellation and Its High-Frequency Analysis Using the Volterra Series," IEEE Trans. Microwave Theory and Techniques, vol. 57, no. 6, pp. 1461-1469, Jun. 2009.

[15] Aya Mabrouki, Thierry Taris, Yann Deval, and Jean Baptiste Begueret, "CMOS Low-Noise Amplifier Linearization through Body Biasing," IEEE International Symposium on Radio Frequency Integration Technology (RFIT), pp. 150-153, Jan. 2009.

[16] Namsoo Kim, Vladimir Aparin, Kenneth Barnett, and Charles Persico, "A Cellular-Band CDMA 0.25-um CMOS LNA Linearized Using Active Post-Distortion," IEEE Journal, Solid-State Circuits, vol.41, no.7, pp. 1530-1534, Jul. 2006.

[17] J.-Y. Lee, H.-K. Park, H.-J. Chang, and T.-Y. Yun, "Low-power UWB LNA with common-gate and current-reuse techniques," IET Microw. Antennas Propag., vol.6, Iss.7, pp.793-799, May 2012.

[18] Muhammad Khurram, and S.M. Rezaul Hasan, "A 3-5 GHz Current-Reuse - Boosted CG LNA for Ultrawideband in 130 nm CMOS," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol.20, no.3, pp.400-409, March 2012.

[19] Heng Zhang, and Edgar Sanchez-Sinencio, "Linearization Techniques for CMOS Low Noise Amplifiers: A Tutorial," IEEE Trans. Circuits and Systems, vol.58, no.1, pp.22-36, Jan.2011.

[20] Heng Zhang, Xiaohua Fan, and Edgar Sanchez Sinencio, "A Low-Power, Linearized, Ultra-Wideband LNA Design Technique," IEEE Journal, Solid-State Circuits, vol.44, no.2, pp. 320-330, Feb. 2009.

[21] P. Andreani, and H. Sjoland, "Noise optimization of an inductively degenerated CMOS low noise amplifier," IEEE Trans. Circuits and Systems-II: Analog and Digital Signal Processing, vol.48, iss.9, pp.835-841, Sep.2001.

JOINT OPTIMIZATION OF PRINTED MONOPOLE ANTENNAS

FOR UWB APPLICATIONS USING HEURISTIC APPROACH

IN THIS ARTICLE, **MUHAMMAD ZUBAIR** AND **MUHAMMAD MOINUDDIN** FROM THE FACULTY OF ENGINEERING AT IQRA UNIVERSITY IN PAKISTAN, USE AN HEURISTIC APPROACH TO JOINTLY OPTIMIZE TWO BASIC MICROSTRIP PATCH ANTENNAS FOR EFFECTIVE USE IN UWB APPLICATIONS

Ultra Wideband (UWB) is the most suitable technology used in wireless communication today, offering low power consumption and very high data-rates over short distances. It sends short duration pulses over a broad spectrum and, although initially aimed at commercial radar systems, it has found a variety of applications, including in consumer products and wireless personal area networks (PANs). Because of the wide signal, UWB transmission supports high data rates, typically 480Mbps up to 1.6Gbps, within a radius of few meters. The data rate, however, drops at longer distances.

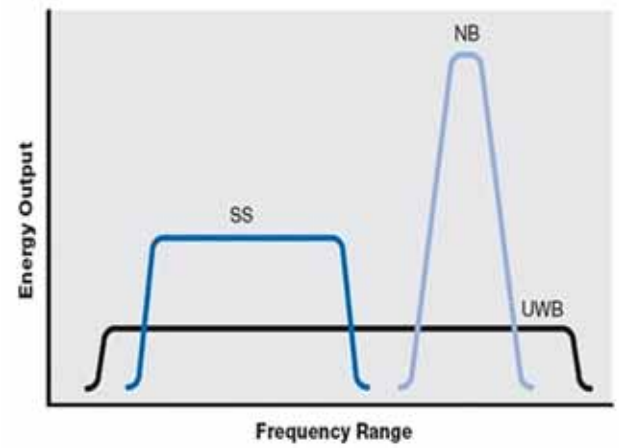


Figure 1: Bandwidth comparison of narrowband (NB), spread-spectrum (SS) and ultra-wideband (UWB) technologies [2]

This radio technology spans over an extremely wide bandwidth, and its comparison with the narrowband (NB) and spread spectrum (SS) technologies, such as Bluetooth for example, can be seen at a glance in Figure 1.

To reduce any possible interference from other electronic systems, in 2002 the Federal Communications Commission (FCC) allocated a bandwidth of 7.5GHz (from 3.1GHz to 10.6GHz) to UWB applications [1]. This bandwidth however, can be greater than 7.5GHz by varying some of its geometrical parameters and dimensions [3].

Because of their wide bandwidth and (approximate) omnidirectional characteristics, printed monopole antennas (PMAs) are the most suitable for UWB wireless technology. The omnidirectional pattern of a PMA is very similar to that of dipole antennas; however unlike dipole antennas, PMA is available in many geometrical shapes [4-7]. Each geometrical shape offers different performance, serviceability and manufacturing cost. In order to achieve optimized values of these parameters, numerous optimizing techniques and algorithms can be used.

In this article, we use an heuristic approach to jointly optimize two basic microstrip patch antennas for effective use in UWB applications. We 'tune' these two different shaped antennas for the same bandwidth and quality factor using joint cost function of deviation error. The declining cost function shows that the optimized design of these antennas is equally suitable over the

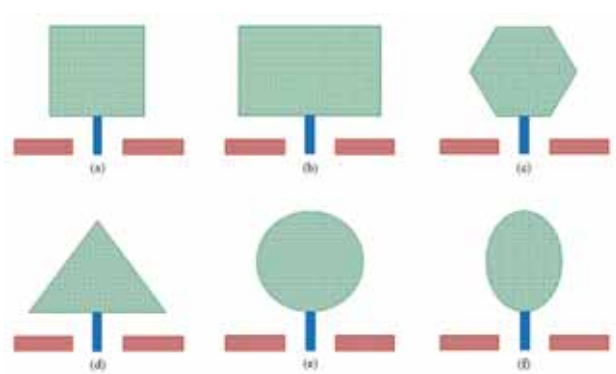


Figure 2: Printed (a) square, (b) rectangular, (c) hexagonal, (d) triangular, (e) circular and (f) elliptical monopole antennas

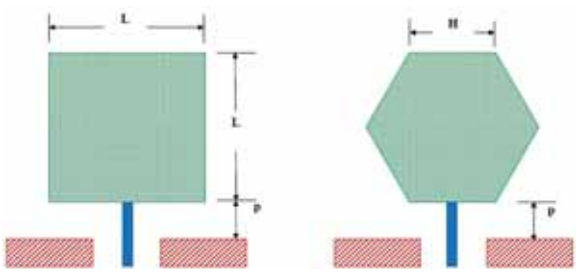


Figure 3: The geometric shapes of PSMA and PHMA

entire spectrum of UWB applications. The simulations are carried out with Matlab and the results validated with the reported cost function.

Design Considerations of UWB Antennas

As mentioned earlier, UWB radio communication provides extremely high data rates due to the transmission of very short pulses. This is also the main reason why tracking the transmitted data is so difficult in this communication range, increasing data security. Moreover, the power consumption of UWB systems is quite low compared to narrowband systems, and there's no multipath fading either.

Due to these attractive features UWB systems are employed in many applications such as radar, home networks, position location and tracking, Wireless Body Area Networks (WBANs) and others [8].

The major challenge in implementing a UWB system is designing a suitable antenna. Here are a few design parameters and characteristics required for a UWB antenna:

1. It must have extremely high impedance bandwidth.
2. It should offer an omnidirectional radiation pattern, which allows user mobility and freedom. The omnidirectional antenna radiates the radio waves in all directions, which implies low directivity and uniform gain [3], [9].
3. The radiation efficiency of UWB antenna must be very high and the transmitted power spectral density must be very low. FCC has specified the upper limit of transmit power spectral density as -41.3dBm/MHz [1], [9-10].
4. In order to maximize the radiation efficiency, the inductance and dielectric losses in the antenna must be minimized [11]. A typical radiation efficiency value should be greater or equal to 70% [3].
5. It should have linear phase throughout the frequency spectrum. This causes a constant group delay for the given range of frequencies, hence the transmitted short duration pulses will have almost no dispersion, which leads to effective operation of the system [3], [11].
6. The return loss of the UWB antenna for the entire frequency range should be less than -10dB [3].

Since a UWB system is mainly employed for indoor applications, it's essential that the antenna is compact, of low weight and small size, and preferably planar [3], [9].

Printed Monopole Patch Antennas

PMAs are widely used in ultra wideband communications due to their omnidirectional radiation pattern. They come in various shapes, including square (PSMA), rectangular (PRMA), hexagonal (PHMA), triangular (PTMA), circular (PCMA) and elliptical (PEMA) [10], as shown in Figure 2.

In our project, we will optimize two basic antennas – PSMA and PHMA. We used a 'genetic' algorithm to optimize their geometric parameters, making them suitable for the same lower-band edge frequency (f_L), quality factor (Q) and frequency bandwidth (BW).

The most decisive parameters for UWB antenna are lower band edge frequency and bandwidth, instead of resonance frequency. The maximum height of the monopole antenna and matching of the impedance with a 50-ohm microstrip are related to lower frequency and bandwidth respectively [5].

The PMA is a type of microstrip antenna with its ground plane at infinity. It can be treated as a cylindrical monopole with large effective diameter. The lower frequency of all regular shapes PMAs with different feed configurations can be calculated using the following analogy. A generalized modified relation for lower edge frequency of PMA is:

$$f_L = \frac{7.2}{[(L + r + p) \times k]}\ GHz \quad (1)$$

where L is the height of the planar monopole antenna (taken as an equivalent cylindrical monopole), r is the effective radius of equivalent cylindrical monopole (obtained by equating the areas of the planar and cylindrical monopole antennas), p is the length of the feed line (of 50Ω) to the antenna, and k is the empirical constant with value of 1.15 for the commonly used FR4 substrate (if the dielectric constant of the substrate is ε_r = 4.4 and the thickness h = 0.159cm); all the variables are measured in centimeters.

Equation 1 is the genetic equation for PMA; however the equations for L and r are different for PSMA and PHMA.

For PSMA, the equations for L and r are as follows:

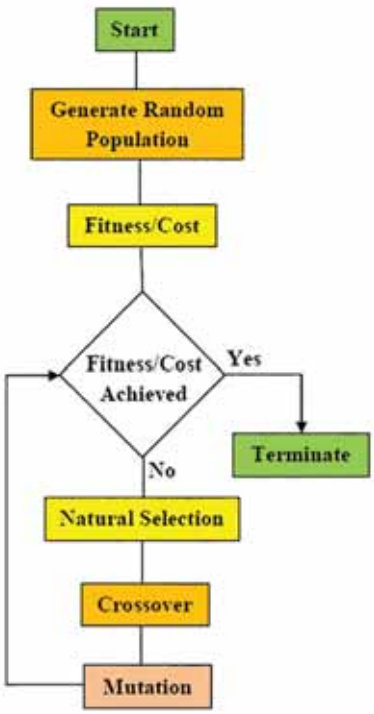


Figure 4: Flowchart of the genetic algorithm

$$L = W\ (width)\ cm \quad (2)$$

$$r = \frac{L}{2\pi}\ cm \quad (3)$$

Using the Equations 2 and 3, Equation 1 for PSMA then becomes:

$$f_L = \frac{14.4\pi}{[L(2\pi + 1) + 2\pi p]k}\ GHz \quad (4)$$

where L is the length of square monopole antenna as shown in Figure 3, and p and k are the same as described for Equation 1. For PHMA, the equations for L and r are as follows:

$$L = \sqrt{3}H\ cm \quad (5)$$

$$r = \frac{3H}{4\pi}\ cm \quad (6)$$

Applying them to Equation 1 for PHMA, it then becomes:

$$f_L = \frac{28.8\pi}{[24.76559237H + 4\pi p]k}\ GHz \quad (7)$$

where H is the length of the sides of hexagonal monopole antenna

Table 1: Optimized values for PSMA at lower frequencies of 4.0, 3.5, 3.1, 2.5, 2.0, 1.5 and 1.0 GHz

Sr. No.	Observed Parameters	Desired	Calculated	Geometric Dimensions	
				L (cm)	p (cm)
1	Frequency (GHz)	4.00	3.998560868	0.863941516	0.564338654
	Bandwidth (GHz)	6.60	6.601439132		
	Quality Factor	0.99	0.986202650		
2	Frequency (GHz)	3.50	3.496726345	1.108775620	0.505251839
	Bandwidth (GHz)	7.10	7.103273655		
	Quality Factor	0.86	0.857087594		
3	Frequency (GHz)	3.10	3.105535295	1.451600616	0.333405523
	Bandwidth (GHz)	7.50	7.494464705		
	Quality Factor	0.76	0.765562318		
4	Frequency (GHz)	2.50	2.502994467	1.789385446	0.427176755
	Bandwidth (GHz)	8.10	8.097005533		
	Quality Factor	0.64	0.636148403		
5	Frequency (GHz)	2.00	2.001752276	2.296423936	0.465783334
	Bandwidth (GHz)	8.60	8.598247724		
	Quality Factor	0.54	0.535732687		
6	Frequency (GHz)	1.50	1.500102249	3.278684911	0.373124722
	Bandwidth (GHz)	9.10	9.099897751		
	Quality Factor	0.44	0.438204518		
7	Frequency (GHz)	1.00	1.000317503	5.280986219	0.137401072
	Bandwidth (GHz)	9.60	9.599682497		
	Quality Factor	0.34	0.339207149		

as shown in Figure 3, and p and k are the same as described for Equation 1.

The quality factor (Q) of the ultra wideband antenna sets the limits for its extended performance. The factor may be evaluated by calculating the central frequency (f_C) of the antenna as the geometric mean of the upper (f_H) and lower (f_L) frequencies [11-13].

Following are the equations of the central frequency, bandwidth (BW) and quality factor for ultra wideband antennas:

$$f_C = \sqrt{f_H f_L}\ GHz \tag{8}$$

$$BW = f_H - f_L\ GHz \tag{9}$$

$$Q = \frac{f_C}{BW} = \frac{\sqrt{f_H f_L}}{f_H - f_L} \tag{10}$$

The value of f_H (upper band edge frequency) is set at 10.6GHz, as allocated by the FCC in 2002 [1]. Using the equations set above, and describing a combined cost function for both antennas, we achieve the joint optimized results by employing genetic algorithm (as heuristic approach).

Sr. No.	Observed Parameters	Desired	Calculated	Geometric Dimensions	
				H (cm)	p (cm)
1	Frequency (GHz)	4.00	4.002577856	0.576406813	0.758967903
	Bandwidth (GHz)	6.60	6.597422144		
	Quality Factor	0.99	0.987298672		
2	Frequency (GHz)	3.50	3.504342688	0.658358315	0.783274445
	Bandwidth (GHz)	7.10	7.095657312		
	Quality Factor	0.86	0.858941496		
3	Frequency (GHz)	3.10	3.100251381	0.744169702	0.415233728
	Bandwidth (GHz)	7.50	7.499748619		
	Quality Factor	0.76	0.764371843		
4	Frequency (GHz)	2.50	2.499883008	0.922888447	0.990115603
	Bandwidth (GHz)	8.10	8.100116992		
	Quality Factor	0.64	0.635508675		
5	Frequency (GHz)	2.00	2.002270027	1.152248756	0.894193896
	Bandwidth (GHz)	8.60	8.597729973		
	Quality Factor	0.54	0.535834231		
6	Frequency (GHz)	1.50	1.500468441	1.537595249	0.157648815
	Bandwidth (GHz)	9.10	9.099531559		
	Quality Factor	0.44	0.438275637		
7	Frequency (GHz)	1.00	1.000182142	2.306693001	0.228453558
	Bandwidth (GHz)	9.60	9.599817858		
	Quality Factor	0.34	0.339179416		

Table 2: Optimized values for PHMA at the lower frequencies of 4.0, 3.5, 3.1, 2.5, 2.0, 1.5 and 1.0 GHz

Genetic Algorithm

Genetic algorithms (GA) are heuristic optimization algorithms classified under the large set of evolutionary algorithms (EA). The key idea of GA is based on the process of natural evolution. It is used to obtain optimized solution to a problem employing natural evolutionary processes, such as mutation, inheritance, crossover and selection etc.

In GA, the evolutionary process starts with randomly-generated chromosomes (strings of population). These chromosomes carry optimized solutions to an optimization problem and gradually move toward more optimized solutions in each generation (iteration). Normally, the solutions are represented in the form of binary strings; however, other encoding patterns are also possible. The fitness of every individual in the population is examined and evaluated in each generation and, on the basis of their fitness values, multiple individuals are selected. These newly selected individuals are then modified by mutation and crossover to achieve the fittest individuals for the next iteration. The algorithm normally terminates when a number of targeted iterations are completed or some predefined fitness level (threshold level) is achieved. The typical GA process is shown in Figure 4.

The process is described as follows:

1. **Initialization**: Initialize all the variables and randomly generate a population of chromosomes, based on a number of variables. The generated population contains the probable solution of the problem.
2. **Fitness/Cost Evaluation**: Using the desired fitness/cost-function evaluate the fitness/cost-value of each chromosome in the population.
3. **Selection**: On the basis of the evaluated results, select the best chromosomes (of maximum fitness or minimum cost) in the population and call them 'parents'.
4. **Crossover**: By employing probabilistic approach, crossover the parents to find new 'offspring'.
5. **Mutation**: Randomly select new individuals from the offspring to form a new population.
6. **Examine**: Terminate the program if the number of targeted iterations are completed or a predefined fitness level (threshold level) is achieved. If the termination is not possible, go to step 3 with the new population.

The parent chromosomes are statistically selected on the basis of maximum fitness or minimum cost values, yet the best solution is not guaranteed. This is the main problem of the selection process that the 'best gene' (best solution) may not be achieved in the truncation process [14].

Optimizing The Cost Function

In our project we are evaluating the lower band edge frequency, bandwidth and quality factor for both UWB antennas. Generalized equations of error for both of them, namely frequency error ($Error_{fL}$), bandwidth error ($Error_{BW}$) and quality factor error ($Error_Q$) are as follows:

$$Error_{f_L} = e_1 = f_{L\,desired} - f_{L\,calculated}\ GHz \tag{11}$$

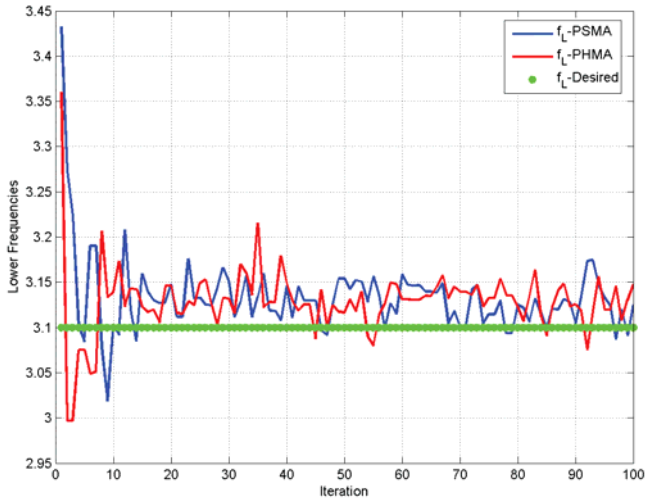


Figure 5: Optimized values of lower frequencies for PSMA and PHMA, compared to the desired value

$$Error_{BW} = e_2 = BW_{desired} - BW_{calculated}\ GHz \tag{12}$$

$$Error_{Q} = e_3 = Q_{desired} - Q_{calculated} \tag{13}$$

In order to observe the collective effect of errors due to above three parameters, mean square error (MSE) relations are employed for both antennas:

$$MSE_{PSMA} = \sum_{i=1}^{3} w_i e_{i(PSMA)}^2 \tag{14}$$

$$MSE_{PHMA} = \sum_{i=1}^{3} w_i e_{i(PHMA)}^2 \tag{15}$$

Here w_i are the random weights for all the errors. For this work, we have kept the total sum of all three weights equal to one, whereas the e_i are the three different errors (separate for PSMA and PHMA) using Equations 11 to 13.

The joint mean square error (cost function) for both antennas is given in Equation 16:

$$Cost\ Function = \frac{(MSE_{PSMA} + MSE_{PHMA})}{2} \tag{16}$$

Using the genetic algorithm we have minimized this cost function to get optimized geometric dimensions for both antennas for the same lower band edge frequency, bandwidth and quality factor. The geometric dimensions for PSMA are the length (or width) of the square monopole L and the length of the feed line from the ground surface p; whereas the geometric dimensions for PHMA are the length of the sides of the hexagon monopole H and the length of the feed line from the ground surface p.

Tables 1 and 2 show the optimized geometric dimensions of the PSMA and PHMA antennas respectively. Different sets of frequency, bandwidth and quality factor have been recorded in Tables 1 and 2. Against each set, jointly optimized values of L, H and p have been achieved for PSMA and PHMA.

Although numerous readings have been observed, the graphical optimization results are shown for one specific set only. As the FCC

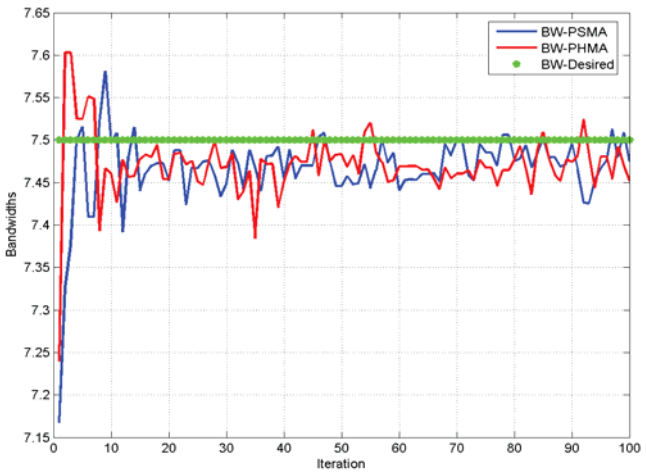


Figure 6: Optimized values of bandwidths for PSMA and PHMA, compared to the desired value

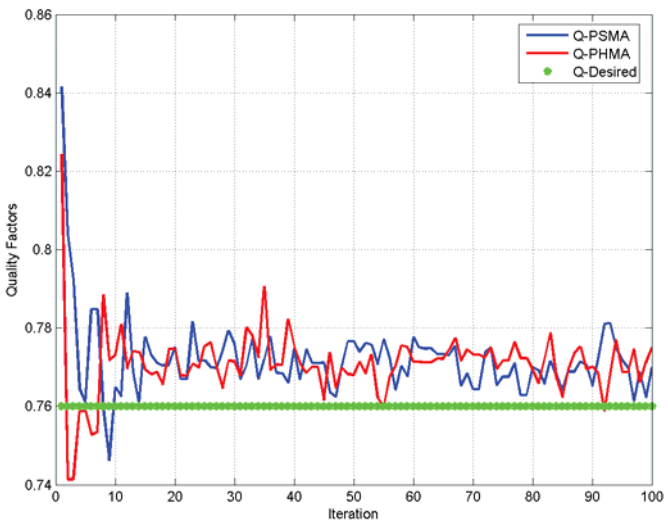


Figure 7: Optimized values of the quality factors for PSMA and PHMA, compared to the desired value

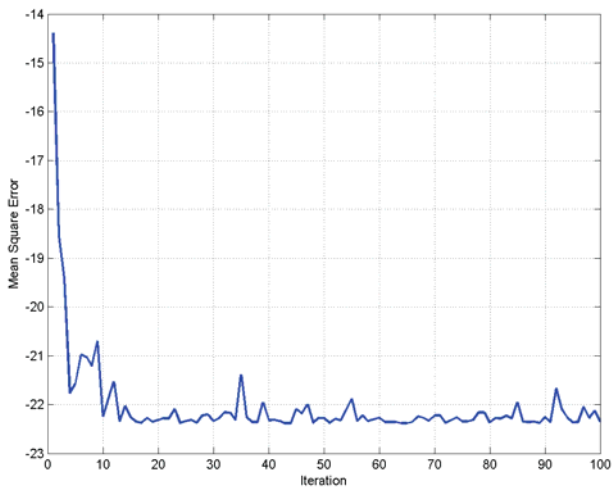


Figure 8: Optimized value of the joint cost function of PSMA and PHMA

allocated 3.1 GHz as the lower end frequency of the UWB spectrum, all the following graphical representations are for this value.

Figure 5 to Figure 8 show the iterative calculated values of the lower edge band frequency (f_L), bandwidth (BW), quality factor (Q) and joint cost function for PSMA and PHMA respectively with 100 iterations.

Future Recommendations

Ultra wideband width wireless communication is the most suitable technology to achieve very high data rates within short radius. Many different types of antennas can be designed and optimized to be suitable. Further emphasis could be placed on improving the quality factor and S-parameters while widening the bandwidth of the UWB spectrum. ●

REFERENCES

[1] Federal Communications Commission, Washington, DC, "FCC report and order on ultra wideband technology", 2002.
[2] A white paper by Intel, "Ultra-Wideband Technology – Enabling high speed wireless personal area networks", 300982-002 US, 2005.
[3] E. G. Lim, Z. Wang, C. U. Lei, Y. Wang and K.L. Man, "Ultra Wideband Antennas – Past and Present", IAENG International Journal of Computer Science, 37:3, IJCS_37_3_12, August 2012.
[4] M. Hammoud, P. Poey, and F. Colombel, "Matching the input impedance of a broad band disc monopole", Electronics Letters, vol. 29, no. 4, pp. 406–407, 1993.
[5] N. P. Agrawall, G. Kumar, and K. P. Ray, "Wide-band planar monopole antennas", IEEE Transactions on Antennas and Propagation, vol. 46, no. 2, pp. 294–295, 1998.
[6] H. G. Schantz, "Planar elliptical element ultra-wideband dipole antennas", in Proceedings of the IEEE Antennas and Propagation Society International Symposium, vol. 3, pp. 44–47, USA, June 2002.
[7] G. Kumar and K. P. Ray, "Broad Band Microstrip Antennas", Artech House, Boston, Mass, USA, 2003.
[8] S. Ullah, M. Ali, M. A. Hussain and K. S. Kwak, "Applications of UWB Technology", arXiv:0911.1681v2 [cs.NI] 27 Jul 2010.
[9] N. Hecimovic and Z. Marincic, "The Improvements of the Antenna Parameters in Ultra-Wideband Communications", Ericsson Nikola Tesla, d.d., Krapinska 45, Zagreb Croatia.
[10] K. P. Ray, "Design Aspects of Printed Monopole Antennas for Ultra Wideband Applications", in Hindawi Publishing Corporation International Journal of Antennas and Propagation Volume 2008
[11] Schantz, Hans, "The Art and Science of Ultra-Wideband Antennas", Artech House, 2005.
[12] L. J. Chu, "Physical Limitations of Omni-Directional Antennas". Journal of Applied Physics, v. 19, Dec. 1948, pp. 1163-1175.
[13] J. McLean, "A Re-Examination of the Fundamental Limits othe Radiation Q of Electrically Small Antennas". IEEE Transactions on Antennas and Propagation, v. 44, n. 5, May 1996, pp 672-675.
[14] S. M. Sait and H. Youssef, "Iterative Computer Algorithms in Engineering", IEEE Computer Society Press, January 1995.

CURRENT-MODE 3.1-10.6GHZ HIGH LINEARITY UP-MIXER FOR UWB TRANSMITTERS

SICHUN DU, HONGXIA YIN, WENBIN HUANG, GUANGXIANG ZHANG AND **ZHIWEN LIANG** PROPOSE A CURRENT-MODE 3.1-10.6GHZ UP-MIXER FOR UWB SYSTEMS, IMPLEMENTED IN A 0.18μM CMOS PROCESS

The ultra wideband (UWB) system with its high data rates, low power consumption and easy co-existence with other communications systems is becoming widely used in short distance communications and wireless Personal Area Networks (PANs) [1]. In general, the UWB frequencies range from 3.1-10.6GHz, and are divided into five groups and 14 bands.

The Up-Conversion Mixer

The up-conversion mixer is a crucial building block in a UWB transmitter [2]. Its design involves tradeoffs between conversion gain, linearity, noise figure, power consumption and isolation [3].

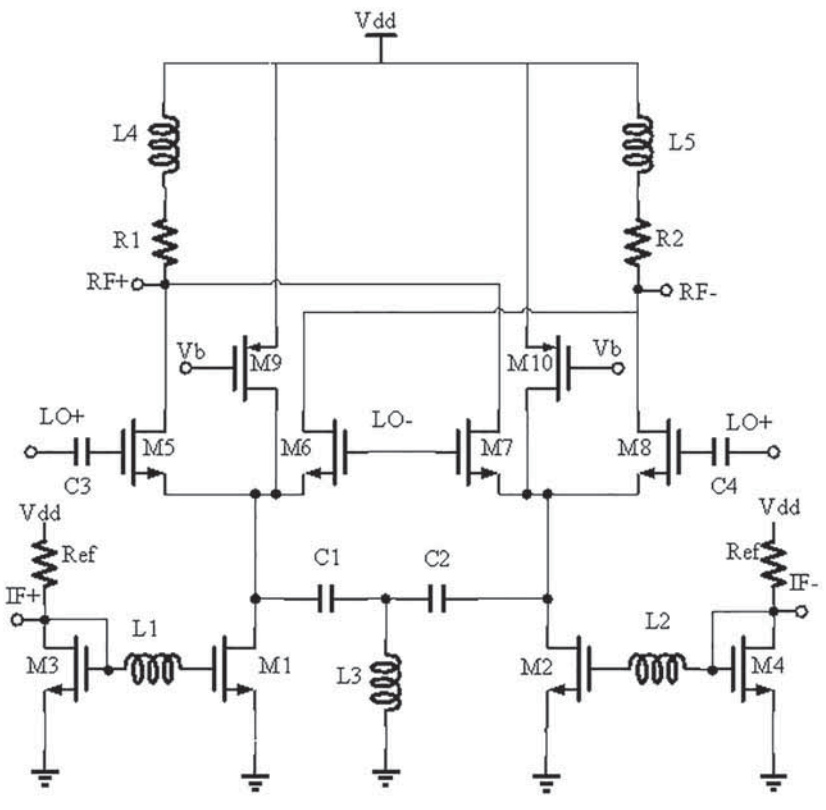


Figure 1: Schematic showing the proposed current-mode up-mixer circuit

Over the years, several topologies for UWB up-mixer applications have appeared, including a modified Gilbert cell mixer that combines a source inductor and a current bleeding technique [4-5]. Although this solution offers improved linearity, the conversion gain is degraded.

Folded switching mixers adopt a current reuse topology [6-7], reducing both power consumption and the supply voltage. However, this circuit suffers from limited conversion gain and relatively poor linearity.

As for voltage-mode circuits, the impedance of the internal nodes is usually large and so is this circuit's power dissipation.

Unlike voltage-mode circuits, current-mode circuits have low impedance at the internal nodes, and signal information is carried by time-varying current. Thus, the voltage at each node can be low, resulting in higher linearity and wider bandwidth [8-10], making current mode circuits suitable for UWB system applications.

In this article, a current mode, 3.1-10.6GHz, high-linearity and low-power up-conversion mixer is suggested. Both the current mirror and current bleeding techniques are adopted to boost linearity. In addition, an inductance peaking technique and an LC network inserted in the common source node of the switching section help improve noise and conversion gain.

Mixer Design

The circuit schematic of the proposed current-mode up-mixer is shown in Figure 1. The structure is based on the Gilbert cell, which offers the advantages of port-to-port isolation and even-order distortion. Transistors M1-M4 form the input current-mirrors, instead of having to use a conventional transconductance construction or any additional voltage to current (V-I) conversion. Note that extra V-I conversion will lead to greater power consumption due to the existing internal high-impedance nodes.

Transistors M5-M8 work as switching cores to modulate the current provided by the current mirrors. Meanwhile, by setting an appropriate bias voltage level for these transistors, they can

LO(GHz) Power	3.432	3.96	4.488	5.016	5.544	6.072	6.60
Pin (dBm)	5.30	9.03	9.62	8.07	7.47	7.32	7.45
Pout (dBm)	9.26	13.70	14.93	13.88	13.64	13.71	13.89
LO(GHz) Power	7.128	7.656	8.184	8.712	9.24	9.768	10.296
Pin (dBm)	7.85	8.65	10.10	12.62	14.75	13.01	11.96
Pout (dBm)	13.20	13.74	15.78	17.79	19.34	17.04	15.44

Table 1: The simulated IIP3 and OIP3 vs LO frequency

operate in either the triode or the cutoff region, which is considered ideal switch. The current sources formed by M9 and M10 improve linearity and do not reduce the conversion gain of the mixer [11]. A T-type LC network (C1, C2, L3) is inserted in the common source nodes of the switch M5-M8 to further improve linearity and gain.

The input of the current mirrors in the proposed mixer consists of M1, M2 L1 and R_{ef}, as shown in Figure 2. Here, the input current signal directly sends signals to the switch stage through the input current mirror, which is different from the conventional Gilbert mixer, where the transconductance stage transforms the voltage into current. The input signal is amplified by setting up a different channel widths of the transistors M1 and M2, according to the target values of the proposed mixer's gain and power dissipation. The precise channel width of the transistors is determined mainly through software simulation, such as Cadence Spectre, for example.

Assuming both M1 and M2 are biased in to saturation, the relationship of I_{out} and I_{Ref} is as follows:

$$\frac{I_{out}}{I_{Ref}} = \frac{W_2 L_1}{W_1 L_2} \quad (1)$$

Here W1, L1 and W2, L2 are the channel width and channel length of the transistors M1 and M2 respectively. Different from the common current mirror, this current mirror has a small inductor L1 to improve linearity.

T-Type LC Networks Analysis

The T-type LC network comprises C1, C2 and L3, appearing as two symmetrical L-type networks (Figure 3). C_p represents the total parasitic capacitance of the LO switching stage and R_p is the equivalent resistance of the M5-M8. Linearity and conversion gain performance will suffer due to IF signal leakage to ground via C_p. So the T-type LC network can be resonant with C_p for the improvement of linearity and conversion gain. The admittance of the resonant network can be written as:

$$Y(\omega) = j\omega C_p + \frac{j\omega C_1}{1 - 2j\omega^2 L_3 C_1} \quad (2)$$

Then, L3 is selected to satisfy the following equation:

$$L_3 = \frac{C_1 + C_p}{2\omega^2 C_1 C_p} \quad (3)$$

The T-type is a band-pass network. It's difficult to improve the linearity of all 14 sub-bands in a UWB system, but the linearity degrades more severely at higher frequencies. In order to upgrade the linearity performance of the up-mixer at the higher frequency bands, the resonant frequency is set at the high frequency range. Moreover, because the LC network absorbs the parasitic capacitance C_p to ground, the conversion gain at the higher frequencies also improves.

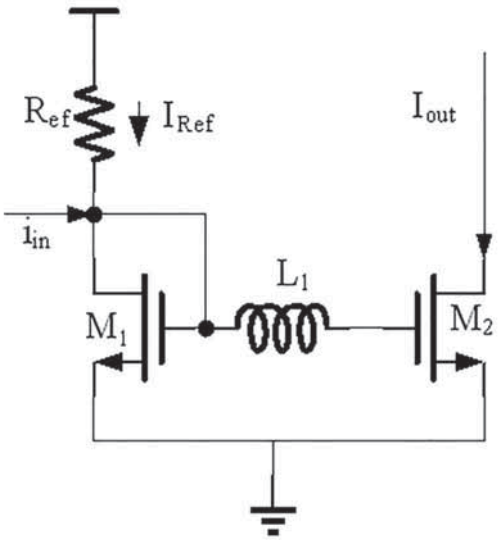


Figure 2: Plot of the input current mirror in the mixer

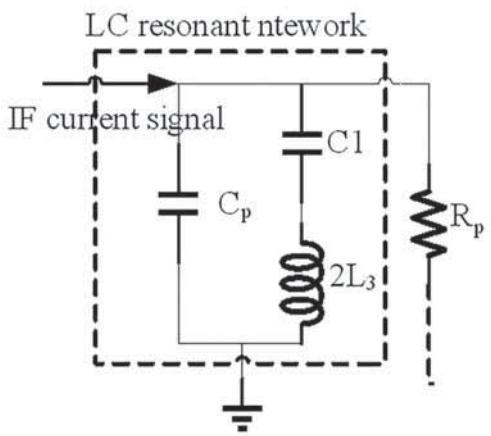


Figure 3: Plot showing the equivalent circuit of the leakage resonant network

Current Bleeding Technique

Linearity and low power dissipation are the most significant performance parameters in the design of a UWB up-conversion mixer. Lower power consumption can be achieved by reducing the supply voltage, but linearity and conversion gain will

Ref Parameters	This work	[4]	[5]	[6]	[7]	[8]
Technology	0.18μm	0.18μm	0.13μm	0.25μm	0.18μm	0.18μm
Frequency (GHz)	3.1-10.6	3-5	6-8	3.1-5	1-11	3-5
IIP3 (dBm)	5.3-14.75	9.8-13.5	-	-7.6	-5--2 (P1dB)	11.6-13.8
CG (dB)	3.5-6.5	2.3	0	3.8	-6	6.5
Noise figure (dB)	15.3-16	19	7	8.4	-	12-13
Chip area (mm^2)	0.56	0.82	0.64	0.36	-	0.88
Voltage/power(V/mW)	1.2/4.5	1.2/7.1	1.8/4.2	1.5/1.95	2.5/25	1/11

Table 2: Performance summary and comparison with other mixers

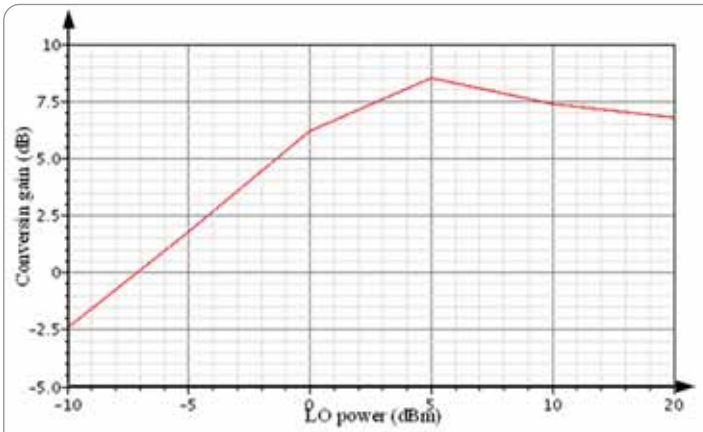


Figure 4: The mixer's conversion gain is plotted here as a function of LO power at 5GHz frequency with IF power of -30 dBm

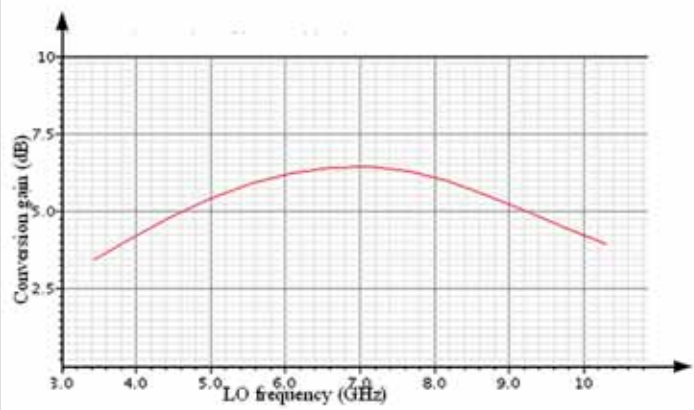


Figure 5: The mixer's conversion gain is plotted here as a function of LO frequency

deteriorate. By adopting a current bleeding technique, formed of two PMOS transistors M9 and M10, high linearity, lower power dissipation and acceptable gain can be achieved simultaneously. The current source which comprises M9 and M10 can provide current to the switching stage, and will not influence the voltage headroom of the input and load stages. In addition, a shunt inductance peaking technique is utilized to flatten conversion gain in the high frequency band.

Simulation Results

The proposed UWB current-mode up-conversion mixer is designed and simulated using the CHRT018IC 0.18μm CMOS process. Post-layout simulation conditions of this design are the following: the IF signal power and frequency are -30dBm and 264MHz respectively. Local oscillator (LO) power is set to 0dBm, and the LO frequency is the centre frequency of the 14sub-band of UWB system. The post layout simulation results of the proposed full-band up-conversion mixer shows that conversion gain is 5±1.5dB and the third-order input intercept point (IIP3) is 5.3-14.75dBm across the desired frequency range of 3.1-10.6GHz. The noise figure of the mixer is 15.3-16dB, and the power consumption is 4.5mW at a supply voltage of 1.2V.

Figure 4 shows conversion gain versus LO power. The LO power is set at 0dBm for the consideration of a reasonable conversion gain and lower power consumption. In addition, an appropriate LO power level can control the transistors in the switching stage.

Figure 5 shows that conversion gain versus the LO frequency of the UWB current mode up-conversion mixer is 3.5-6.5dB, and conversion gain variation of the mixer is 3dB over the full band. As the gain of the transmitter is mainly provided by the power amplifier, it is acceptable for the transmitter to provide this gain level.

Two tone inputs have been performed for the simulation of IIP3. The input frequencies of the two tones are 264MHz and 264.5MHz respectively, with 0.5MHz separation. Figure 6 shows that the maximum value of the simulated IIP3 is 14.75dBm at LO frequency of 9.24GHz. Because the mixer has an additional inductor in the input current mirror and the T-type networks in LO switch stage, linearity performance is much improved compared with the conventional Gilbert mixer cell over the full frequency band, and especially in the high frequency band.

Table 1 shows the complete simulated IIP3 of the mixer when the LO power is 0dBm. Figure 7 shows the single-sideband (SSB) noise figure (NF) of the mixer is 15.3-16dB. As the noise figure is not the most important parameter, the simulated result is acceptable for a UWB transmitter.

The layout of the proposed up-mixer is shown in Figure 8. The chip area including pads is 0.7×0.8mm. This layout was designed by Cadence's Virtuoso and verified by Calibre.

Performance of the proposed up-mixer is summarized in Table 2, and compared with other mixers. It can be seen that the mixer attains high linearity, reasonable conversion gain and noise figure across the frequency range from 3.1GHz to 10.6GHz. ●

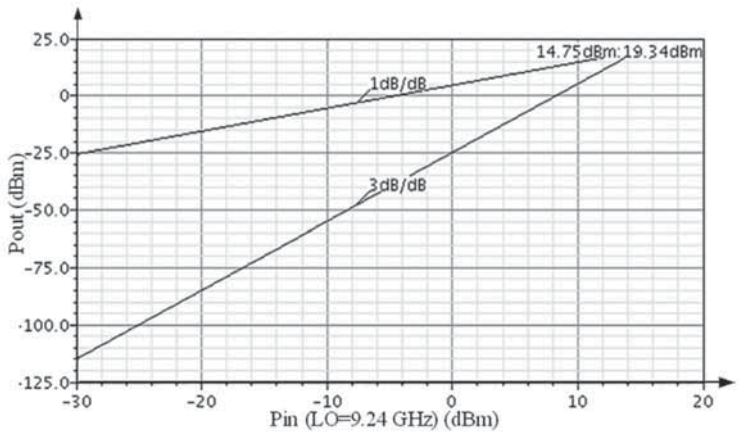


Figure 6: This plot shows the simulated IIP3 at the LO frequency of 9.24GHz

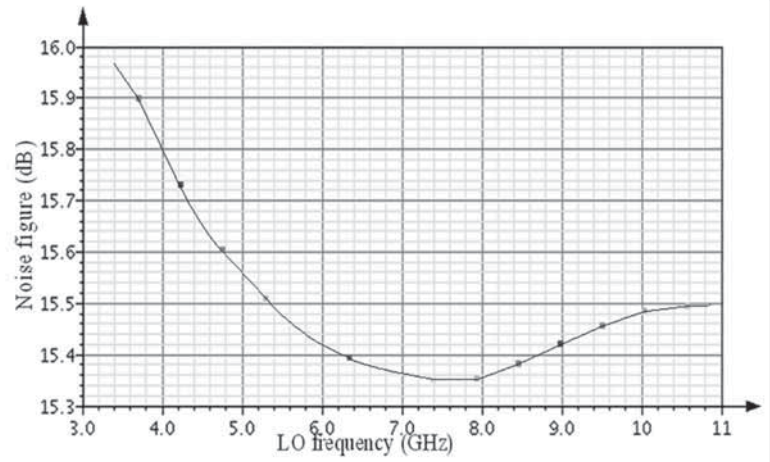


Figure 7: The mixer's SSB noise is plotted here as a function of LO frequency

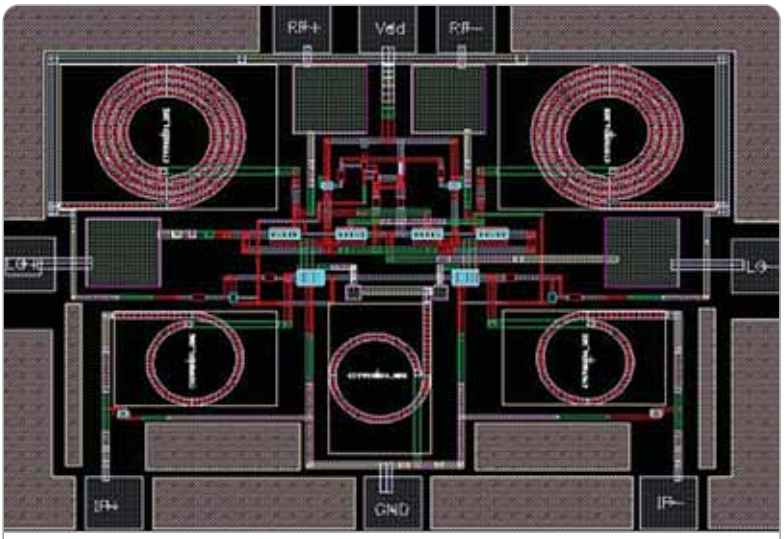


Figure 8: Layout of the current-mode mixer fabricated with on-chip passive circuit elements as a single chip

REFERENCES

[1] Federal Communications Commission, Washington, DC, "FCC report and order on ultra wideband technology", 2002.

[2] A white paper by Intel, "Ultra-Wideband Technology – Enabling high speed wireless personal area networks", 300982-002 US, 2005.

[3] E. G. Lim, Z. Wang, C. U. Lei, Y. Wang and K.L. Man, "Ultra Wideband Antennas – Past and Present", IAENG International Journal of Computer Science, 37:3, IJCS_37_3_12, August 2012.

[4] M. Hammoud, P. Poey, and F. Colombel, "Matching the input impedance of a broad band disc monopole", Electronics Letters, vol. 29, no. 4, pp. 406–407, 1993.

[5] N. P. Agrawall, G. Kumar, and K. P. Ray, "Wide-band planar monopole antennas", IEEE Transactions on Antennas and Propagation, vol. 46, no. 2, pp. 294–295, 1998.

[6] H. G. Schantz, "Planar elliptical element ultra-wideband dipole antennas", in Proceedings of the IEEE Antennas and Propagation Society International Symposium, vol. 3, pp. 44–47, USA, June 2002.

[7] G. Kumar and K. P. Ray, "Broad Band Microstrip Antennas", Artech House, Boston, Mass, USA, 2003.

[8] S. Ullah, M. Ali, M. A. Hussain and K. S. Kwak, "Applications of UWB Technology", arXiv:0911.1681v2 [cs.NI] 27 Jul 2010.

[9] N. Hecimovic and Z. Marincic, "The Improvements of the Antenna Parameters in Ultra-Wideband Communications", Ericsson Nikola Tesla, d.d., Krapinska 45, Zagreb Croatia.

[10] K. P. Ray, "Design Aspects of Printed Monopole Antennas for Ultra Wideband Applications", in Hindawi Publishing Corporation International Journal of Antennas and Propagation Volume 2008

[11] Schantz, Hans, "The Art and Science of Ultra-Wideband Antennas", Artech House, 2005.

[12] L. J. Chu, "Physical Limitations of Omni-Directional Antennas". Journal of Applied Physics, v. 19, Dec. 1948, pp. 1163-1175.

[13] J. McLean, "A Re-Examination of the Fundamental Limits othe Radiation Q of Electrically Small Antennas". IEEE Transactions on Antennas and Propagation, v. 44, n. 5, May 1996, pp 672-675.

[14] S. M. Sait and H. Youssef, "Iterative Computer Algorithms in Engineering", IEEE Computer Society Press, January 1995.

BEYOND THE CONNECTION:
SFP+ FIBER OPTIC TRANSCEIVER THERMAL AND EMI CONSIDERATIONS

HIGH DATA-RATE OPTICAL TRANSCEIVERS (SFP+) MEET TODAY'S DEMANDING APPLICATIONS OF HIGHER BANDWIDTH AND PORT DENSITY, INCLUDING THE CHALLENGES RELATED TO EXCESS HEAT AND EMI EMISSIONS. BY **MATTHEW SCHMITT, DAVE DEDONATO** AND **PATRICK RECCE** OF TE CONNECTIVITY

High data-rate, small form-factor, pluggable, optical transceivers (SFP+) are the industry's answer for demanding applications of higher bandwidth and port density.

Figure 1 shows examples of SFP+ optical transceivers in single and multiple port configurations, including 1x2, 1x4 and 1x6 cages. The higher performance and density of these devices result in challenges related to excess heat and EMI emissions; however, there several ways to address these concerns.

Thermal Performance

There are many internal and external variables that affect thermal performance of pluggable I/O products and dictate whether or not a cooling solution is required. Unfortunately, there is no clear answer to this question and, therefore, system architects must consider many options and restrictions when designing end products.

The form-factor of the product must be taken into account, as different configurations have unique airflows. A "pizza box" (either a 1U or 4U) mounted in a standard rack may have front-to-back airflow or side-to-side airflow. A blade-style switch or equipment may be mounted vertically within an enclosure in a standard rack, a configuration that almost always has bottom-to-top airflow.

The number and density of ports mounted on the PCB must also be well thought-out. These ports can be single-port cages, 1xN ganged cages, 2xN stacked cages, or a combination of all three. This is in addition to other I/O connectors at the face of the product.

The spacing between these cages must also be taken into account, as well as port density, ambient air temperature, airflow, allowable temperature rise and backpressure created by baffling.

Finally, heat dissipation of the optical transceiver itself must be considered. Older SFP optical transceivers usually operate at lower power but newer SFP+ optical transceivers use more power. Commercially-available optical transceivers are rated up to 70°C, with extended-temperature-range transceivers operating up to 85°C. Newer SFP+ modules used in short-reach and long-reach applications are still dissipating 1W or less, but extended reach and fixed DWDM (dense wavelength division multiplexing) transceivers can range from 1.25-1.5W per port.

The industry has found that trying to cool these higher-wattage transceivers in SFP+ stacked cages is quite challenging. Managing the temperature of the inner-lower row of ports that are not exposed to airflow is especially difficult.

Figure 1: Examples of SFP+ optical transceiver modules

Experimental Proofs

Figure 2 shows the results of an experiment done by TE Connectivity (TE) that simulated the conditions in a rack-mounted router with 24 data ports, comprised of six 1x4 ganged cages. The cages are stacked in three stacked pairs. Airflow is moving across the entire assembly from left to right. Table 1 provides details of the test setup. The red numbers in Figure 2 show individual SFP+ ports that are running at temperatures in excess of the 70°C operating limit.

Airflow	500 LFM (measured by airflow chamber and not by anemometer probe)
Backpressure	0.25 inches of water (controlled by baffle)
Altitude	Sea level
Temperature	Room ambient (results adjusted for 55°C ambient)
Power	1.5 watt per transceiver
Air gap above cage	50mm
Air gap below PCB	9.5mm
Temperature rise limit	70° C

Table 1: Thermal test setup parameters

In order to improve the thermal characteristics, TE has added ventilation holes strategically in both the cage body and in the latch plate. Figure 3 shows a side view of the cage assembly that includes side-wall perforations. Figure 4 is a close-up view of the latch plate that includes the two thermal vent holes. The perforations in the cage body were optimized in size and shape in order to minimize the

Figure 2: Thermal data recorded using standard SFP+ stacked 2x4 cages

potential for EMI leakage. The two thermal vent holes added to the front of each latch plate still allow for the use of two light pipes.

The results of these simple modifications to the test setup demonstrate a remarkable improvement in thermal performance (Figure 5). None of the ports in the revised test exceed the 70°C limit under identical test conditions.

Figure 3: Side view of the cage assembly that includes side-wall perforations

EMI Emissions

Many variables affect EMI emissions, such as leakage from optical transceivers, type of board-level components (integrated chips, power supply module, etc.) and other improperly shielded connectors used in today's communications equipment. If these EMI emissions are not properly contained within a chassis, such disturbances may degrade or limit the effective performance of the electrical circuit or prevent the end product from passing FCC emissions standards. These effects can range from a decrease in performance to a total loss of data transmission.

TE has identified two components that improve EMI performance. The first component is the gasket retention plate, shown in Figure 6a, which acts as a backer plate for the conductive elastomeric gasket that interfaces with the inside of the front bezel. Modifying the gasket retention plate to provide more attachment points to the cage body reduces EMI emissions between the cage body and gasket retention plate. The redesigned "right-angle" gasket retention plate can be seen attached to the cage body in Figure 6b.

Figure 4: Close-up of the latch plate that includes the two thermal vent holes

The second component identified for improvement is the latch plate, which is the component that separates the bottom port from the upper port. This component also houses the light pipes that transmit light from LEDs mounted on the PCB to the front face of the cage assembly. Industry standards dictate the design of the latching mechanism, so this was left unchanged, but within the latch plate a secondary component was added to improve EMI performance and prevent leakage. The optimization of the gasket retention plate and the addition of the component to the latch plate yielded a significant improvement in EMI performance in the 10-15GHz range (Figure 7).

As data rates and packaging densities continue to increase, more attention must be given to containing EMI and addressing thermal considerations. ●

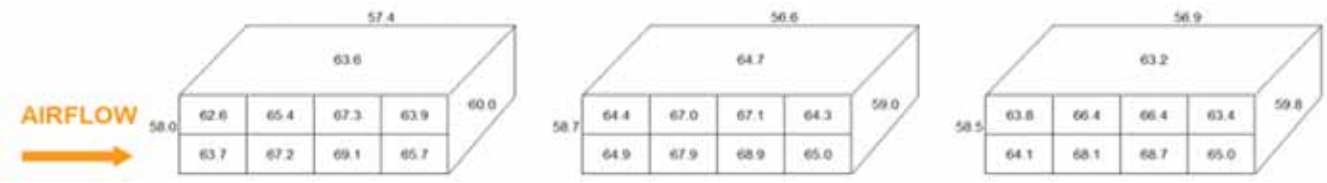


Figure 5: Improved thermal performance resulting from enhanced airflow

Figure 6a: Standard gasket retention plate

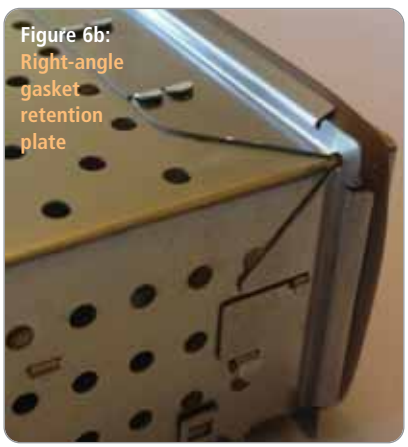


Figure 6b: Right-angle gasket retention plate

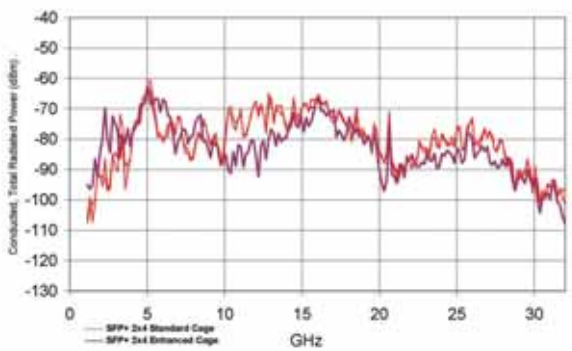


Figure 7: EMI test data comparing standard SFP+ stacked cages versus SFP+ enhanced cages

THIS IS A NEW COLUMN, PRESENTING A SERIES OF SIMPLE ARDUINO PROJECTS. ARDUINO IS AN OPEN-SOURCE ELECTRONICS PROTOTYPING PLATFORM, BASED ON FLEXIBLE, EASY-TO-USE HARDWARE AND SOFTWARE

Building An Arduino-Based Scrolling Sign

BY **BROCK CRAFT**

In this project we will use the Arduino Uno board and an LED matrix with a common cathode. Figure 1 shows the display and its pinouts.

The Sure LE-MM103 matrix is a two-colour display with red and green LEDs. Each of the dots on the front of the matrix has two LEDs behind it. You can choose to use one or the other as there aren't enough output pins on the Arduino Uno to do both colours. This project uses only the red LEDs, so Figure 1 only shows the LED matrix pin numbers you need to use for the red LEDs.

If you use the Jameco display, there are only red LEDs, so there are fewer pins on the bottom. Take a closer look at Figure 1; there are a lot of pin numbers here. Notice that the Arduino Pins 2 through 9 are indicated on the left. Each of these is connected to the Arduino's digital outputs through a 1kΩ resistor. In each of the rows, all the cathodes of the LEDs are connected to the same digital output. This is why the display is referred to as a common-cathode display.

Each of the columns is also connected to the Arduino digital output pins. The top row of labels (10 through A3) indicates the columns each Arduino pin is connected to. The Display Pin Number tells which pin on the back of the matrix is connected to which LED (only the red LEDs pin numbers are shown).

The code will control the individual LEDs by providing current to the columns and a path to ground on its row. For example, setting Arduino digital output in Pin 2 to LOW and Pin 10 to HIGH provides a pathway for electricity to flow through the LED and it lights up. If you set the pins the other way around, however, the LED will not light up.

There are two LEDs for each of the 64 positions on the matrix. In this project, your code goes through each of the red LEDs at each position to light it or turn it off. When you wire up columns on a two-colour LED matrix, you connect the red LED pins (23, 20, 17, 14, 2, 5, 8 and 11). In the illustrations, I show how to connect the red ones. If you prefer, you can connect to the green LEDs (pins 24, 21, 18, 15, 1, 4, 7 and 10).

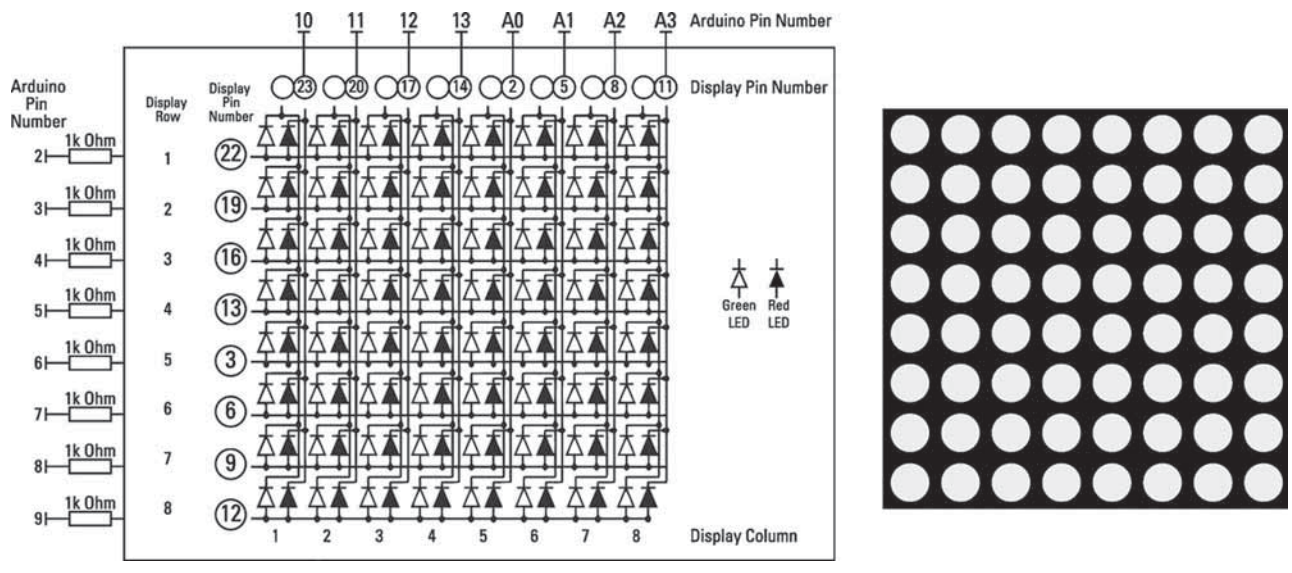


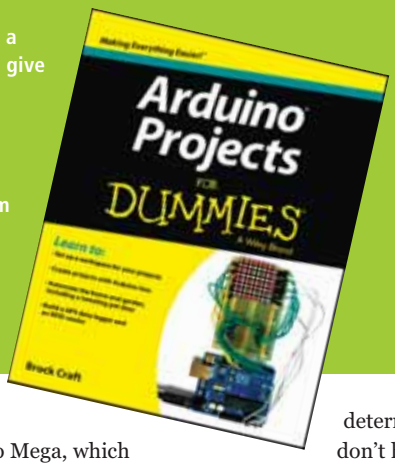
Figure 1: LED matrix display and schematic. Only the pin numbers for the red LEDs are shown

WIN THE 'ARDUINO PROJECTS FOR DUMMIES' BOOK

Brock Craft is a Lecturer in the Department of Computing at Goldsmiths, University of London. He drew extensively on his practical experience with Arduino to write *'Arduino Projects For Dummies'*. We have a couple of copies of this book to give away.

To enter please supply your name, address and email to the Editor at svetlanaj@sjpbusinessmedia.com

The winner will be drawn at random and announced at the end of the series.



If you want to use both colours of LED, you could use an Arduino Mega, which has 54 digital I/O pins, but you'd need to modify the code accordingly.

Pay close attention to the difference between the Arduino pin number, the LED matrix row and column numbers, and the LED matrix pin numbers. If you are using a different LED matrix than the chosen example, you will need to identify which LED pin corresponds to a labelled row or column, and then connect that LED pin (not the LED pin number in the diagram) to the indicated Arduino pin number.

On the underside of the matrix, notice that the pins are in two columns. Each of the LEDs is connected to a pin for its anode and a shared pin for the cathode. Look closely and you may see that Pin 1 is labelled at the lower-right side of the display, under the clear resin. If your matrix isn't labelled, check your data sheet to identify which is Pin 1.

There is no standard pinout for LED matrix displays. You might find that on your display – even if it's a common cathode display, the pins do not match the one in this project, in which case the code will not work. Refer to the data sheet for your matrix to determine which pins to connect. If you don't have the datasheet, a PDF of it should be available from the website of your supplier.

If you are using the specific matrix display in the example, follow the layout in Figure 2, otherwise refer to your datasheet to figure out which LED pins to connect to which Arduino pin.

Also follow Figure 2 to connect the Arduino pins to your resistors and LED matrix. It's good to be very detail oriented at this stage and to double-check your connections. You're not likely to damage anything if you wire it incorrectly, but the matrix won't display correctly if something's wrong.

More on this project is available in Brock Craft's book 'Arduino Projects For Dummies'

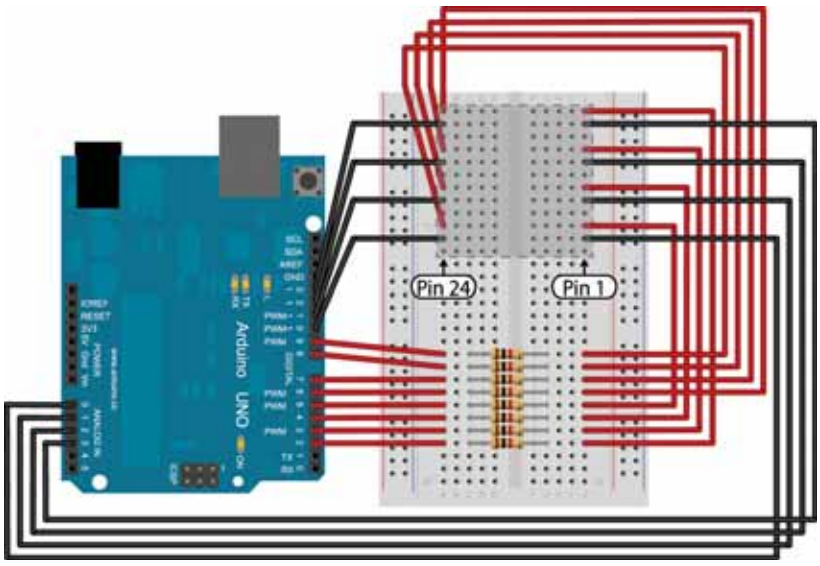


Figure 2: The breadboard layout for your scrolling sign

MEETING THE 'ALWAYS ON' DEMANDS OF THE INDUSTRIAL ELECTRONICS MARKET

STUART HUTCHINGS FROM BULGIN DISCUSSES THE USE OF ROBUST CONNECTIONS IN INDUSTRIAL ELECTRONICS, AND LOOKS AT HOW THE LATEST HIGH-POWER, WATERPROOF, PUSH-PULL CONNECTORS MEET THESE NEEDS

Figure 1: 7000 Buccaneer series from Bulgin

In today's 'always on' world there is an ever-increasing need to ensure uninterrupted connectivity in the harshest environments – equipment is expected to operate continuously, with minimal downtime.

The demand for robust connections presents manufacturers with quite a challenge, requiring the production of durable, environmentally-sealed connectors capable of withstanding even the most severe conditions. Reliability is a crucial consideration for every industry, since failure of a single connection may result in lengthy downtime and significant revenue losses while the fault is diagnosed and repaired.

In the past, equipment was frequently hard-wired, with little emphasis on downtime or cost of maintenance, often making it necessary to request a service engineer call-out. Although hard-wiring provides a secure connection, its big disadvantage is the length of time it takes for the repair. With the ongoing drive towards reducing equipment downtime while simultaneously reducing maintenance costs, the benefits of modular system design using components secured by 'fit and forget' connectors become ever more evident. The use of easy-to-assemble connectors enables engineers to seamlessly exchange components in need of servicing or repair, without specialist tools or training, minimising the length of time equipment is unavailable for use.

> Frequently, electronic connections must be made in the field and this can present difficulties for installation engineers when termination requires contacts to be soldered or crimped

Finding Suitable Solutions

Robust and safe solutions for a broad range of applications are always being sought, and this has sometimes involved connectors that may not have been designed for that specific environment. Frequently, military-type connectors for aircraft or tanks are adopted, due to their rugged, robust construction. Some of these connectors may be environmentally-sealed, but are not necessarily intended for the selected end application. For example, aircraft wiring tends to use open harness cable looms with seals around each individual wire or conductor.

By comparison, in the industrial environment cables are more open to the elements, and a cable jacket is used to prevent water or dust penetrating into the cable core or equipment, or damage caused by direct exposure to sunlight, for example. As a consequence, while military connectors have the inherent capabilities needed to meet many demanding applications and are commonly used, they are not entirely suitable as they are unable to seal around the cable jacket, so additional accessories are required to ensure correct sealing for use in an industrial environment.

Another key requirement for industrial electronics is easy assembly and installation. Frequently, electronic connections must be made in the field and this can present difficulties for installation engineers when termination requires contacts to be soldered or crimped. While these types of connection are fine in a workshop environment, where appropriate tools are available, an installation engineer working in the field will not always have the necessary equipment to hand. Furthermore, not all of these connectors will have been designed as sealed components, and additional accessories may be required to create a fully-sealed product.

Connectors with push-pull or twist-lock mating mechanisms provide everything necessary to complete a sealed connection and simplify this process considerably, eliminating the need to order a variety of different components, as well as the associated risk of an engineer being unable to terminate a connection due to missing, or incorrect, parts. Correct cable retention is also


Figure 2: Bulgin PMX6034 rewirable flexconn

essential and is a potential issue when adapting connectors designed for other applications; aircraft cables tend to be cleated, but this may not be the case in an industrial environment where outdoor cables may whip. Tried and tested sealing techniques are vital, ensuring the correct level of cable retention and sealing.

Manufacturers have developed a variety of very successful metal and plastic connectors to meet the demands of the industrial electronics market, such as Bulgin's Buccaneer 6000 Series of power and data connectors, and the company's new range of larger diameter Buccaneer 7000 Series of compact, environmentally-sealed 25A, 600V couplings.

Safe And Secure Connectivity

In industrial electronics, water and dustproofing are important considerations. As well as the obvious electrical hazard associated with water, salt water, dust and, particularly, cement dust, can erode contacts fairly rapidly, quickly rendering an unprotected connector useless. Traditional screw coupling waterproof connectors are very effective, but may take some time to connect, which can be a major drawback. It can also be difficult to determine how tight the connections need to be to ensure an effective seal is achieved and successful coupling may be 'installer dependent'.

Connectors play an essential role in an incredibly diverse range of applications. As interest in renewable energy continues to grow, one potential application for easy-to-assemble, 'fit and forget' connectors is solar technology, where many individual solar inverters must be networked to maintain power distribution across the grid; advanced electronic control is vital to enable a stable energy supply to be created. Solar inverters are connected to solar panels via single-pole connectors, and higher-power AC output connectors are required to carry current back to the grid.

Constant power distribution and process control are essential for industrial automation purposes, as well as for large weighing equipment and transportation applications, such as the specialist vehicles used to inspect rail tracks. Robustness is vital; the connectors used for these applications must withstand considerable stress, and durability is a prerequisite, if unplanned downtime is to be avoided. Rugged, rapid-locking connectors with positive feedback enable a perfect seal to be achieved every time, without the need for technical expertise or specialist tools.

Waterproof Solutions

Waterproof connectors are equally crucial for many applications. Temporary lighting and sound systems at concert venues require a secure, stable power supply, relying on durable, waterproof connectors capable of accommodating large cables; this is equally true for architectural lighting and signage. These connectors are also ideal for water features such as fountains, offering a robust mains interface for pumps and underwater lighting. For marine applications, typically winches, lighting and control equipment, connectors must be both waterproof and resistant to salt-water corrosion. In these situations, the use of plastic connectors, rather than metal, can be beneficial.

Interchangeable plastic and metal connectors enable a wide variety of different applications to be accommodated. Plastic couplings, manufactured from a blend of PBT (polybutylene terephthalate) and polycarbonate, significantly reduce the risk of moisture accumulating within the connector. They are light and versatile and have the advantage of being less prone to attack by salt water, as well as being comparatively inexpensive. They are also UV stable, making them ideal for long-term use in outdoor applications. In addition, these UL94 V-0 rated self-extinguishing connectors are halogen-free, ensuring that no toxic gases are produced in the event of a fire.

While cost-effective plastic connectors may be the preferred solution in many situations, other applications require a more robust and rugged material. In cases where electromagnetic compatibility (EMC) is an issue, metal connectors may be more suitable, providing continuation of the cable screen from the cable through to the mating connector and completing the Faraday cage. The option to use interchangeable metal and plastic connectors provides maximum flexibility.

Customers requiring protection from electromagnetic interference (EMI) may choose to combine a metal connector with the corresponding plastic mating connector, reducing the cost as much as possible. Equally, for some applications a plastic connector may be the ideal solution, yet the cable-mounting half of this interface may need the additional strength of a robust metal connector to ensure it is not damaged in use. ●


Figure 3: Bulgin Buccaneer 6000 series

DELIVERING HIGH-RELIABILITY SOLUTION TO THE DEVELOPMENT OF PORTABLE LIFE-SUSTAINING DEVICES

SYNCARDIA'S TOTAL ARTIFICIAL HEART IS THE ONLY FOOD AND DRUG ADMINISTRATION (FDA), HEALTH CANADA AND CE APPROVED TOTAL ARTIFICIAL HEART IN THE WORLD. **PAUL COLLINS**, SENIOR MARKETING COMMUNICATIONS SPECIALIST AT SMITHS CONNECTORS, DISCUSSES THE SYSTEM'S INTERCONNECT NEEDS

Due to a shortage of donors, transplant waiting lists are often quite long and, during this time, the mobility and quality of life for patients is restricted due to the size, weight and non-portability of life-sustaining equipment. Hence, the need for smaller portable devices for which total reliability is crucial.

SynCardia Systems of Tucson, Arizona, manufactures such systems, and in particular the temporary "Total Artificial Heart", which acts as a pre-transplant support for patients suffering from end-stage biventricular failure and waiting for a heart transplant.

The Challenge

For patients being kept alive by the Total Artificial Heart, the wait for a donor heart has typically been one of forced hospital confinement, tethered to a large console that powers and monitors the system. SynCardia's "Big Blue" driver is the only FDA-approved driver for powering the Total Artificial Heart in the United States, but weighs 190kg. So, SynCardia began to develop a suitable portable substitute for Big Blue that would permit stable patients to be discharged from hospital and live in the comfort and familiarity of their homes while waiting for donors.

Figure 1: HyperGrip Cover latest medical application connectors from Smiths Connectors

Perfect Solution

SynCardia's research and development produced the Freedom portable pneumatic driver as an alternative power source to its hospital-based Big Blue driver. The Freedom driver is currently undergoing an FDA-approved Investigational Device Exemption (IDE) clinical study in the United States.

Issues of crucial concern to SynCardia during the development stages of the Freedom driver was to make certain that total signal integrity and reliability were maintained. This challenge included a critical need for reliable and dependable interconnect systems within the product. SynCardia turned to Smiths Connectors, a provider of high reliability interconnection product with a proven track record of success in the medical device industry.

A key design need for SynCardia, from an interconnect technology perspective, was a requirement for unique keying capabilities to ensure that incorrect mating did not occur. To address this need, Smiths Connectors introduced three different connectors that are not intermateable and are in different colours.

Since this is an ambulatory application, the customer further requested that one of the connectors and cable assemblies in the mix could be placed at a right angle to the driver so that it would not protrude, minimising the risk of snagging.

The Smiths Connectors and SynCardia engineering teams created a specialized interconnect design that combined Smiths's Hypertac HyperGrip connector series with its D-series solution, and successfully addressed the unique demands and requirements of this life-sustaining application. Specifically, the operating environment comprised two Hypertac Hypergrip connectors containing two custom inserts, two power contacts and two signal contacts. These are green and yellow, to meet the colour-coding requirements of the application. Additionally, a custom-made black-coloured D series plug and cable assembly with a right-angle strain relief was further designed for use in the driver. ●

> The Smiths Connectors and SynCardia engineering teams created a specialized interconnect design that successfully addressed the unique demands and requirements of this life-sustaining application

PUSH/PULL PLASTIC CONNECTORS

HyperGrip push/pull plastic connectors from Smiths Connectors are designed specifically for medical applications. Medical devices and instruments, such as the SynCardia Freedom driver, require multiple connector interfaces and, to avoid incorrect mating, HyperGrip connectors are colour-coded and feature a keying system that makes it simple for operators to connect to the proper receptacle.

The HyperGrip Series provides the high cycle-life, low insertion force and contact performance needed in many applications. Custom inserts can also be designed to address the unique needs of various operating environments.

The Hypertac D Series is another highly reliable product from the Smiths Connectors range of high-performance interconnect solutions designed for critical medical applications. The D01 and D02 series are available in the black colour, have push/pull latching, are available in cable-to-panel and cable-to-cable configurations and in a high impact plastic body. The D Series provides medical equipment designers with reliable connections across a broad range of devices such as defibrillators, monitors, infusion pumps and laboratory equipment. The slightly larger D02 used in the SynCardia application provided an excellent solution for the Freedom driver environment.

Figure 2: HyperGrip family of coloured connectors

Figure 3: The Freedom heart

Figure 4: Coloured connectors ensure correct mating

Electronics Design: Emitter Follower

MAURIZIO DI PAOLO EMILIO, PHYSICS PH.D AND TELECOMMUNICATIONS ENGINEER, PREPARES THIS SERIES OF ARTICLES ON ELECTRONICS FUNDAMENTALS

Microelectronics has changed our lifestyles, with mobile phones, digital cameras, laptop computers and other devices becoming an integral part of our daily life. In this series I will analyze the principal circuits that make up many electronics systems and, in particular, I will give a practical and theoretical approach to some of them.

Emitter Follower

The emitter follower is particularly useful for applications where high input impedance is required. It is typically used as a buffer in a wide variety of circuits.

Emitter follower is a common collector transistor configuration. It can be easily designed as an RC circuit. The emitter follower is also known as a voltage follower, or a negative-current feedback circuit, with high input impedance and low output impedance.

The outline of the emitter follower is shown in Figure 1 and its corresponding equivalent small-signal circuit in Figure 2. The forward diode resistance is indicated as r_{π}.

We can calculate the effective resistance seen from the B side of the circuit by:

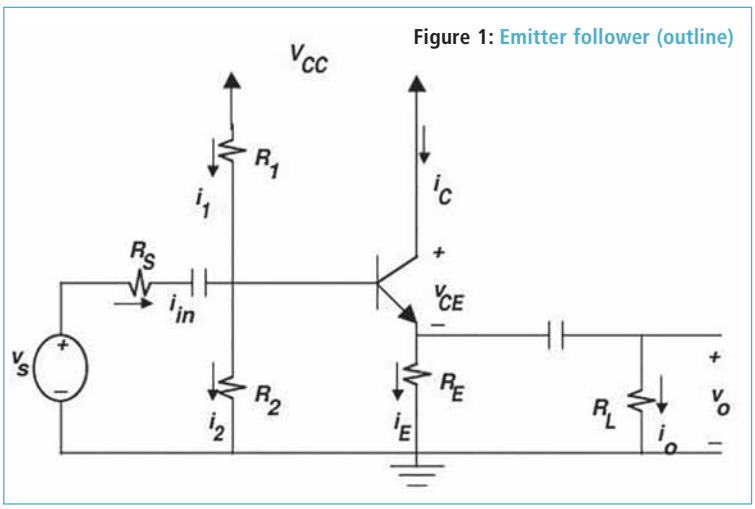
$$R_{ib} = r_{\pi} + (\beta + 1)R_E // R_L \approx (\beta + 1)R_E // R_L$$

This value is relatively high. In general, $R_E // R_L$ (parallel of R_E and R_L) is around kΩ and β ~ 100, so the resistance seen from the B side is in the hundreds of kΩ.

It is evident from Figure 2 that input resistance depends on load resistance. Let us name the input resistance as R_{in}:

$$R_{in} = R_B // R_{ib}$$

The effective resistance is the parallel between R_{ib} and R_B.



A common-collector configuration can be used as an amplifier in such a circuit, where a large input resistance is needed; a typical application is a pre-amplifier circuit.

From the voltage gain equation $A = V_o/V_i$ it follows:

$$A = \frac{V_0}{V_s} = \frac{R_E // R_L}{r_e + (R_E // R_L)} * \frac{R_{in}}{R_s + R_{in}}$$
$$r_e = r_{\pi} / (\beta + 1)$$

It becomes evident that as long as $r_e << (R_E//R_L)$ and $R_s << R_{in}$ the gain approaches unity.

Designing an Emitter Follower

The emitter follower can be designed using the main steps described below:

- **Choose a transistor:** the transistor should be selected according to the system requirements.
- **Select emitter resistor:** selecting a working point (for

Figure 2: Emitter follower (small-signal equivalent circuit)

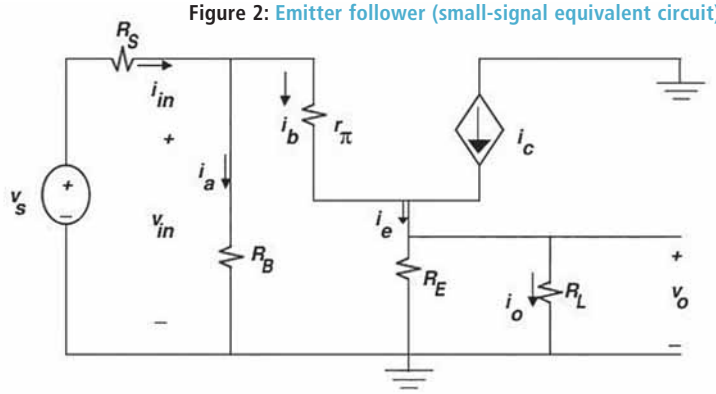


Figure 3: Emitter follower (example with 2N3904)

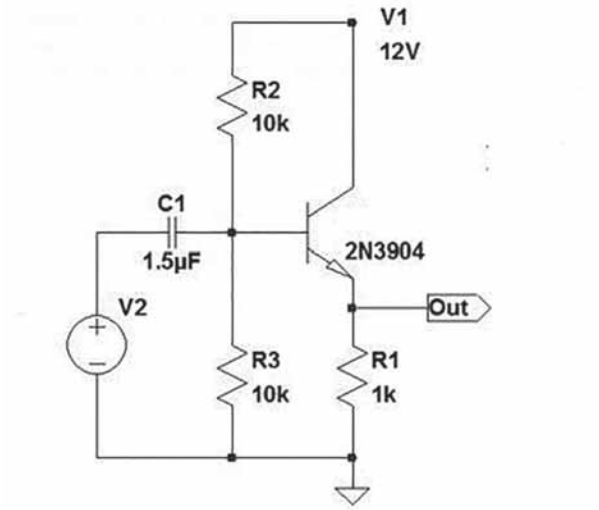


Figure 4: Simulation with P-Spice (gain)

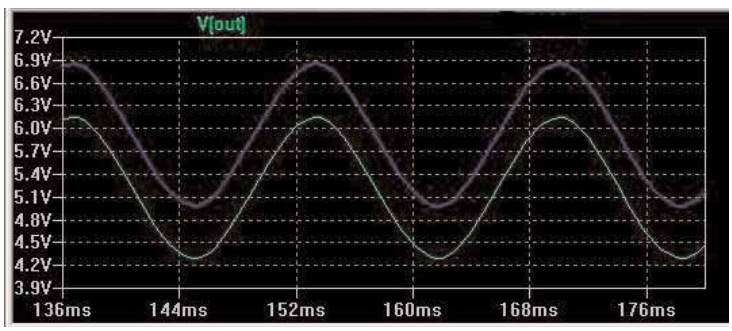
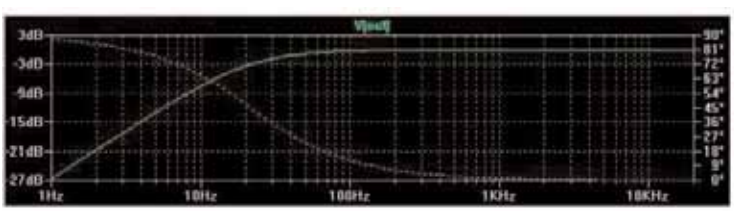


Figure 5: Simulation with P-Spice (frequency response)



example select an emitter voltage of about half the supply voltage).

- **Determine the base current**: base current is the collector current divided by β (or h_{fe}).
- **Determine the base resistor values:** select the value of the resistor(s) to provide the voltage required at the base.
- **Determine the value of the input and output capacitor:** Its value should match the impedance of the input/output circuit at lowest frequency of operation.

When using the emitter follower circuit, there are two main practical points to note:

- **The collector may need decoupling:** in some cases the emitter follower may oscillate, in particular if long leads are present. One of the easier ways to prevent this is to decouple the collector from ground with very short connections, or by placing a small resistance between the collector and the power supply line.
- **The input capacitance affects the RF:** the base emitter capacitance may reduce the impedance of the input circuit for signals above 100kHz.

The emitter follower circuit is particularly useful for applications where high input impedance is required

One design of an emitter follower is shown in Figure 3, with a P-Spice simulation in Figures 4 and 5. This configuration can be typically used in AC-coupled applications. It's important that the frequency response and bias voltage on the base are planned for. In the circuit shown here, there's an added voltage divider, consisting of R2 and R3, and an AC-coupled capacitor, C1. Their component values need to be calculated.

An important aspect of the emitter follower is its relative immunity to temperature instability. When the current in the collector increases (changing β), the voltage across the emitter resistor also increases. This acts as negative feedback, since it reduces the voltage difference between base and emitter (V_{BE}), which drives the transistor to conduct more current, so thermal stability is maintained.

Southern Electronics

FIVE, Farnborough

12 – 13 of February 2014

Southern Electronics Sets New Benchmark

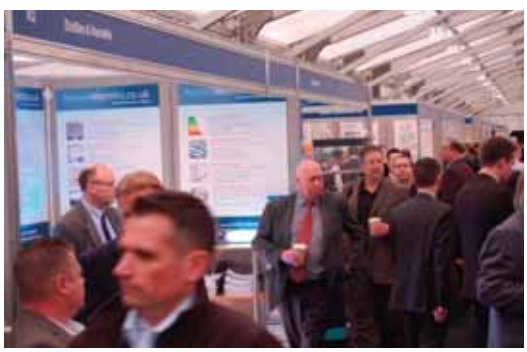
Southern Electronics, the UK's longest-running electronics show, returns to FIVE (Farnborough International Venue & Events) on February 12th and 13th 2014. At 15,000 square meters, the purpose-built event venue alongside Farnborough Airport is now larger than five of the halls at the NEC combined, making it by far the largest electronics event in the UK.

The 2013 show was the largest and most successful in its ten-year history, with both attendance figures and exhibitor numbers exceeding previous events. This year looks set to break this record yet again.

With a strengthening economy and tax incentives stimulating capital investment, demand for exhibition space is high as companies seek to take advantage of the increasingly favourable conditions.

Around 100 new exhibitors join the roster for 2014, taking the total close to 800. The profile of some of these newcomers, such as BAE Systems and Olympus, gives some indication just how important a marketplace the show has become; another is how many companies return to Farnborough year after year. Blundell Production Equipment returns to show its range of tooling and machinery for the PCB assembly industry, as do Blakell Europlacer and Juki Automation. Other names from the PCB industry exhibiting again in 2014 include Hampshire-based Spirit Circuits and pan-European manufacturer Eurocircuits, together with Falcon PCB and Beta Layout.

Southern Electronics will also host a wide selection of component suppliers. Big names like RS Components and Anglia are joined by hundreds of niche suppliers offering thousands of sub-assemblies and component parts, from plastic to wire-wound components, PSUs, sensors, spacers, doors, buttons, handles and enclosures among many other products and systems. Other suppliers at the show are REO, Harwin, G&B Projects, Electrolube, Finder plc, G. English Electronics, Pickering Electronics, Midas Components, Nexus (GB), TDK-Lambda (UK) and Tesa UK.



Sub-contract services are well represented too, by a whole range of firms offering a slew of services from cable manufacture to full-box build. Some names to look out for here include Briton EMS, Arrival Electronics, SIC, CT Production, Broxton Industries and Tenkay Electronics.

The format of the show makes it very attractive to some of the more interesting engineering-based SMEs from across the UK and Europe, many of which do not exhibit elsewhere. From this accessibility comes the second unique feature of Southern Manufacturing & Electronics – the diversity of suppliers that take part.

"It is no exaggeration to say that pretty much every kind of industrial product or process is represented at the show. There simply isn't another event like it in the South," said Phil Valentine, Show Director.

Technology Trails And Seminars

Technology trails guide visitors around the event, allowing them to make the most efficient use of their time at the show. The trails include all aspects of a particular activity, enabling visitors to make a range of useful contacts very efficiently. For example, the aerospace trail may include precision machining along with electronics sub-assemblies and components.

The show's free technical seminar programme has become something of an institution, allowing visitors free access to presentations from business experts and leading academic figures. Past topics have included advanced manufacturing techniques, designing for commercial success, selling abroad, CE marking and updates on EU regulations, presentations on 'lean manufacturing' and how to market successfully.

A full list of seminars is available from the website, together with the all-important and highly recommended pre-registration form. Entry to Southern Manufacturing & Electronics and participation in the technical seminars is free. Simply register at **www.industrysouth.co.uk**.

FIVE Farnborough is easily accessible by road or public transport. On-site car parking is free and a free shuttle bus operates between the show venue, Farnborough Main and North Camp railway stations. Visitors can interact with many of the show's exhibitors in the official LinkedIn group at: http://linkedin.industrysouth.co.uk, or learn the latest news by following @industry_co_uk #southmanf on Twitter or visiting http://blog.industrysouth.co.uk

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New Connectors On Show At Southern Manufacturing 2014

Binder UK is showing a wide range of circular connectors on Stand D50 at Southern Manufacturing 2014, and will also feature the new series 770 NCC that is IP67 unmated.

Originally designed for medical equipment, the 770 Series NCC is designed so that the contacts are protected to IP67 when not connected without the need of a protective cap. This makes it ideal for all types of portable and hand-held measuring equipment, control devices and other applications where it is an advantage to make rapid set-up changes. The efficiency of the design achieves a product life in excess of 5,000 mating cycles.

Series 770 is a panel-mount receptacle in which the electrical contacts are protected from water, dust and foreign particles by a spring-mounted lid when unmated. When the cable plug is mated the contact cover is pushed inside the receptacle body, the contacts engage and the connector is locked with a quarter turn of a bayonet-locking collar.

www.binder-connector.co.uk

PEAK GROUP AND SIMPLICITY AI FEATURE ATE AND MASS INTERCONNECT SYSTEMS

At Southern Electronics 2014, The Peak Group is featuring its recently announced partnership with Simplicity AI to provide integrated test solutions based on National Instruments's industry-standard platforms along with Peak's test hardware and fixturing technology and Simplicity AI's advanced test and measurement software.

Peak Production Equipment, based in Letchworth, UK, is a proven provider of automated test and measurement solutions, supporting every stage of the assembly process from component testing to highly complex functional solutions. Peak is also the exclusive UK agent for the mass interconnect systems made by Virginia Panel Corporation, which are extensively used as interfaces within the automatic test sector.

Simplicity AI, based in Farnborough, UK, provides a range of advanced technical products and engineering services for test, measurement, control and automation, with a particular emphasis on developing automatic test and measurement software built around industry-standard platforms. The company's Tequra software suite aims to reduce the cost and risk involved with test software development, deployment and maintenance.

www.thepeakgroup.com

HARTING FEATURES INTEGRATED INDUSTRIAL SOLUTIONS FOR THE SMART FACTORY

At Southern Electronics, Harting will feature its comprehensive range of integrated solutions for the smart factory of the future under the heading of "the fourth industrial revolution". Products on show include interconnectivity products for smart network infrastructures and smart power systems, RFID hardware and software for implementing automatic ID within the industrial environment and the latest generation of connectors for wire-to-board and board-to-board interfaces. The Harting Technology Group's electronics assembly operation – Harting Integrated Solutions (HIS) – will also be demonstrating its backplane and sub-assembly capabilities.

New networking products include the Ha-VIS mCon 3000 range of Ethernet switches, which enable the construction of complex and efficient network structures and are optimised for use in harsh industrial environments. The high demands on reliability and safety in industrial settings mean that managed Ethernet switches need to become more efficient, and the new Harting switches address this challenge by offering high availability, network security, monitoring capabilities and high reliability.

www.harting.com

TRIPLE OUTPUT LINEAR PSU PROVIDES UP TO 8 AMPS

Aim-TTi has extended its PL series of linear regulated laboratory power supplies to include a triple-output model, the PL303QMT.

Unlike most triple-output PSUs, all three outputs are full performance with CV/CI modes, simultaneous voltage/current metering and switchable remote sense; total power is 228W. The PL303QMT has two identical 30V/3A outputs with quad-mode switching which provides independent, tracking and true parallel modes, the latter providing 30V/6A from a single output. The third output offers 0-6V at 0-8A, very high current for a linear regulated unit. The resolution for this output is increased from 10mV to 1mV and current resolution of 1mA is maintained up to 8A with a selectable low-current range with 0.1mA resolution.

The unit is compact being 3/4 rack width (320mm) by 3U high (130mm). A rack-mount kit is available which can accommodate the PL303QMT alone or in combination with any single output PL or PLH model.

www.aimtti.com

ZUKEN ANNOUNCES FIRST EDM SYSTEM FOR ELECTRICAL AND FLUID DESIGN

Zuken has introduced the first data management solution specifically designed to manage E3.series design data in its native format. E3.EDM (Engineering Data Management) builds on Zuken's E3.series and Contact Software's CIM DATABASE EDM platform to provide data and process management integrated into E3.series for wire, harness, cable, control system and fluid design.

E3.EDM is the first solution that enables native data management of E3.series data, thereby empowering electrical and fluid design processes in key areas. Electrical and fluid design have specific requirements for data and process management that, until today, have not been covered by existing engineering IT solutions. E3.EDM closes a significant gap in the engineering process and, thus, helps boost productivity and design quality.

By using the native E3.series data model, designs are managed on a sheet and device level, enabling engineers to work the way they prefer to work, rather than adapting their work process to the EDM tools.

www.zuken.com/e3edm

Swissbit Introduces Secure Micro SD Card Product Family PS-100u

With the new security product line of the PS-100u Series, Swissbit AG is extending its successful flash memory product line by dedicated security products. This storage solution in Micro SD form-factor enables highly secure solutions by an embedded secure element. Solution providers can turn mobile and embedded systems into secure devices by using the Swissbit secure Micro SD as root of trust.

The new PS-100u product family comprises three editions suitable for PKI, voice encryption and contactless use. The Standard Edition PS-100u SE fits best into authentication and PKI use. The card is supported by leading middleware vendors in mobile, desktop and tablet use cases to ensure a seamless design in into existing security infrastructures.

The Voice Edition PS-100u VE provides Elliptic Curve Cryptography. The big computation and security advantage combined with small certificate sizes make the PS-100u VE card ideal for online key and certificate exchange.

www.swissbit.com

Five-Year Warranty on New Excelsys UltiMod Modular Power Supplies

Excelsys Technologies has introduced its new highly competitive UltiMod range, the first in its class to carry a five-year warranty. Designed to offer users unrivalled price/performance and simplify both selection and procurement, the new UltiMod series of power supplies provides up to 12 outputs and 1200W in a compact 1U format.

The Excelsys UltiMod is simple to configure for any application. Two versions of the Input AC front ends (powerPacs) are available to accommodate either 4 or 6 output modules. Both powerPacs carry dual certification, EN60950 for industrial applications and 2 x MOPP, EN60601-1 3rd Edition for medical applications. The UX4 delivers up to 600W and can be populated with up to 4 powerMods, the UX6 delivers up to 1200W and can be populated with up to six powerMods. All UltiMod products can withstand shock > 60G, per MIL STD 810G and will start-up at -40°C.

www.excelsys.com

2.54MM PITCH VERSION OF HAR-FLEXICON SMD PCB CONNECTION SYSTEM FROM HARTING

Harting has introduced a 2.54mm pitch version of its har-flexicon miniature rapid-connection system for printed-circuit boards (PCBs) incorporating surface-mount devices (SMD).

Har-flexicon is tailored to the market demand for screwless rapid termination technology and economical processing for miniature electronic assemblies. It is designed to be compatible with SMT and reflow soldering processes, as well as with automatic loading systems using pick-and-place technology.

The new system, incorporating SMD PCB terminals and connectors with 2.54mm spacing, enables the flexible, field-installable rapid connection of individual wires with push-in spring-force termination technology, and a stable basis for surface mount connectivity.

Rigid and flexible conductors are available with cross-sections from 0.14-0.5mm². Straight and angled components with 2-12 positions are available for the PCB. For cross-sections up to 2.5mm², reflow products with push-in spring force termination technology with a pitch of 3.50/3.81mm and 5.00/5.08mm are available as PCB terminals and PCB connectors.

www.harting.com

TWO NEW MODELS IN THE YOKOGAWA'S FAMILY OF SOURCE MEASURE UNITS

Two new instruments have been added to the Yokogawa GS610 and GS820 family of source measure units (SMUs): the GS610 Model 7655 is a battery simulator unit which simulates the internal resistance changes of batteries as an aid to failure analysis, while the GS820 Models 765601/Z and 765602/Z are 50V output versions for testing higher-voltage components such as LEDs and power transistors.

Yokogawa's single-channel GS610 and multi-channel GS820 source measure units are high-accuracy, high-speed programmable voltage and current sources that incorporates both generation and measurement functions, as well as USB interfaces and USB storage functions.

The instruments feature high-power output, with a maximum output voltage and current of 110V and 3.2A, respectively, a basic accuracy of 0.02%, and pulse widths down to 100µs. These performance levels, coupled with the fact that the units can operate as current sources or current sinks, make them ideally suited to measuring and evaluating the electrical characteristics of a wide range of devices.

http://tmi.yokogawa.com

DIGI-KEY SEARCH ACCELERATOR ENRICHES USER EXPERIENCE AND ACCESS TO OVER THREE MILLION PARTS

Digi-Key Corporation recently announced new website features including a new 'search accelerator', making it faster and easier for customers to search for electronic components. This new feature kicks off a series of global website improvements designed to accelerate information access and simplify the ordering process.

Digi-Key used the results of a recent "Voice of the Engineer" research study to identify and prioritize the most valuable website features and upgrades. The website improvements are focused around advanced search capabilities including multi-attribute filters and easy-to-search product categories.

"Our customers are telling us they want access to more parts, faster – and we listened!" said Tony Harris, Digi-Key CMO. "We solicited feedback from our internal application engineers to prioritize what matters most. As a result, we're announcing this set of valuable website updates that will improve the entire online customer experience."

www.digikey.co.uk

SIC – Manufacturing Excellence for the Medical Industry

When it comes to the medical industry, the choice of components used within all devices is of critical importance. Increasingly, more and more products used daily by medical professionals have wiring harnesses and cable assemblies at their heart and the importance of reliable components cannot be underestimated.

At SIC we have a strong track record as a trusted supplier to a number of major medical equipment manufacturers within this industry and as a result, we understand that quality is paramount in all we do. All of our products are assembled in-house with robust manufacturing processes, backed up with ISO9001 quality accreditation. To further support our commitment to this demanding industry, we have recently invested in a brand new piece of machinery to enable us to manufacture specialised cables of up to 30 AWG to the extremely tight tolerance levels that are demanded within this industry.

www.sicltd.com

Evaluation Kit For 3-Phase Brushless DC Motor Driver IC

Available from Allegro MicroSystems Europe is a new product evaluation kit to design the company's A4915 3-phase MOSFET controller IC. The evaluation kit consists of a printed-circuit board containing everything required to spin and control a brushless DC (BLDC) motor. All the user has to do is provide a voltage supply and the motor itself.

The A4915 incorporates on-chip Hall commutation and a unique speed control input, which takes an analogue voltage and generates a pulse-width-modulated (PWM) output with a variable duty-cycle.

This arrangement makes it possible to efficiently control a BLDC motor with little or no microprocessing power, resulting in a 75% reduction in PCB space compared with alternative solutions on the market.

The A4915 evaluation kit is fully compliant to 50V and includes everything needed to spin a motor. Six all N-channel power MOSFETs are mounted on the evaluation kit and can supply 30A peak and 20A nominal run current at room temperature.

www.allegromicro.com

Harwin Wins 2013 Elektra Passive and E/Mech Product Of The Year Award

Harwin's Gecko family of 1.25mm pitch hi-rel connectors won the 2013 Elektra Product of the Year Award in the Passive & Electromechanical category.

Harwin's Scott Flower, Product Manager for Gecko Connectors, who is also the chief designer of the Gecko family, received the award, saying: "We are delighted that Gecko has been received so positively in the market. Winning an Elektra is a validation of Harwin's policy of keeping all key design and manufacturing processes in the UK."

Harwin's low profile G125 series connectors are designed to offer high performance in a miniature package. The 1.25mm pin spacing results in a 35% space saving over other high-performance connectors such as Micro-D.

www.harwin.co.uk

AVX PRESENTED "COMMERCIAL VS HI-REL QUALIFICATION METHOD COMPARISON" AT MRQW 2013

AVX Corporation delivered a presentation entitled "Commercial vs Hi-Rel Qualification Method Comparison" at the 2013 Microelectronics Reliability and Qualification Working Meeting (MRQW). A forum for the open discussion of reliability and qualification issues for microelectronics intended for use in space systems, MRQW 2013 took place on December 10-11, 2013 at The Aerospace Corporation in El Segundo, US.

AVX Fellow Ron Demcko addressed the differences between commercial and high-reliability capacitor design, processing and qualification for space systems. He discussed base metal electrode (BME) testing and reliability for an array of capacitors with varying case sizes, voltages and values, which will support the recent European Space Agency (ESA) decision to allow the companies responsible for building its space systems to purchase and employ high-reliability BME capacitors from AVX in their designs.

BME technology enables the development of high-reliability capacitors capable of exhibiting an enormous range of capacitance values in an extremely compact physical case.

www.avx.com

NEW AP4034 FAMILY OF POWER MOSFETS FOR DC-DC CONVERTER APPLICATIONS

Advanced Power Electronics Corp (USA) has introduced the new AP4034 family of 30V N-channel enhancement-mode power MOSFETs in several popular package alternatives to meet differing cost/performance points. All the AP4034 MOSFETs provide fast switching performance and feature a low typical gate charge of 15nC for good switching performance.

With the best thermal performance of the three, AP4034GMT-HF-3 MOSFETs benefit from a low maximum on-resistance of 8mΩ and a drain-source current rating of 44.3A. The devices come in a PMPAK5x6 package with an integrated thermal pad and with a standard SO-8 footprint compatible with other enhanced 5x6mm power packages.

The AP4034GM-HF-3 is in a standard SO-8 package, which is widely used for commercial and industrial surface-mount applications, and offers a maximum on-resistance of 9mΩ and drain-source current rating is 13A.

AP4034GYT-HF-3 MOSFETs have the same low maximum on-resistance of 9mΩ, with a drain-source current rating of 15.5A but offer improved thermal performance even with a smaller 3mmx3mm foot print.

www.a-powerusa.com

MOUSER ELECTRONICS CONTINUES RAPID GROWTH IN EUROPE

Mouser Electronics announced that during 2013 it has outstripped the general distribution market in Europe and expects to achieve year-on-year revenue growth figures of above 30%. During Q4 -2013, the company enjoyed its best ever European quarter performance and September, October and November were all-time record months.

This market-leading performance, coupled with future aggressive growth plans, positions Mouser for further significant European growth in 2014.

"In Europe we are well ahead of our revenue targets and have grown our customer base by over 30% with new business coming from every industry sector," said Graham Maggs, European Marketing Director at Mouser. "Semiconductors now represent over 40% of our sales, and, importantly, we have seen an 11% increase in the sales of parts that were introduced by the manufacturer in the last 12 months (NPI sales). These facts lead to the conclusion that we are now accepted as the design-fulfillment distributor of choice and go-to place for newest components."

www.mouser.com

TEAM WITH GAN SYSTEMS WINS $2M TO DEVELOP NEW TRANSPORTATION TECHNOLOGIES

GaN Systems has partnered with Arkansas Power Electronics International (APEI) in a successful bid for funding from the $45m US DoE programme aimed at developing new vehicle technologies to improve fuel efficiency and reduce transportation costs. The APEI-led team, also including Toyota Motor Engineering and Manufacturing North America Inc, the University of Arkansas National Center for Reliable Electric Power Transmission and the US National Renewable Energy Laboratory, has been awarded $2m as one of the 38 different projects the DoE is funding across the US.

The team will develop new electric motor traction drives for hybrid electric vehicles based on gallium nitride (GaN) and silicon carbide (SiC) power semiconductors. These new technologies will replace traditional silicon semiconductors in automotive power electronics to herald a new generation of highly efficient and lower cost systems.

Girvan Patterson, CEO of GaN Systems said: "The DoE initiative is a very exciting opportunity for the industry."

www.gansystems.com

Most Advanced MachXO3 FPGA Family Yet

Lattice Semiconductor launched its ultra-low density MachXO3 Field Programmable Gate Array (FPGA) family, the world's smallest, lowest-cost-per I/O programmable platform aimed at expanding system capabilities and bridging emerging connectivity interfaces using both parallel and serial I/O. By matching advanced, small-footprint packaging with on-chip resources, the MachXO3 family puts affordable innovation into the hands of system architects by simplifying the implementation of emerging connectivity interfaces such as MIPI, PCIe, GbE and more.

The ultra-low density MachXO3 FPGA family gives customers a single programmable bridge that lets them build differentiated systems using the latest components and interface standards. With advanced package technology solutions that eliminate bond wires to enable lowest-cost and increased I/O density in a small footprint.

"The MachXO3 family allows designers to address the disparity among the components within their systems with minimal impact on cost, footprint, and power consumption," said Brent Przybus, Senior Director, Product and Corporate Marketing.

www.latticesemi.com/MachXO3

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www.labcenter.com

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