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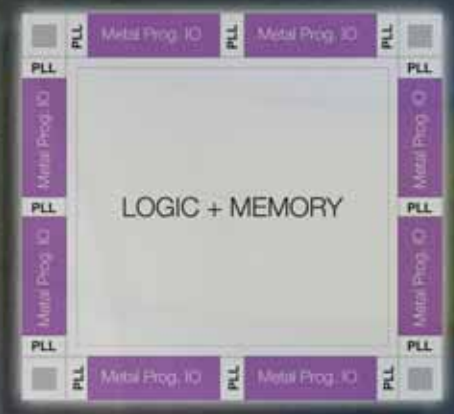




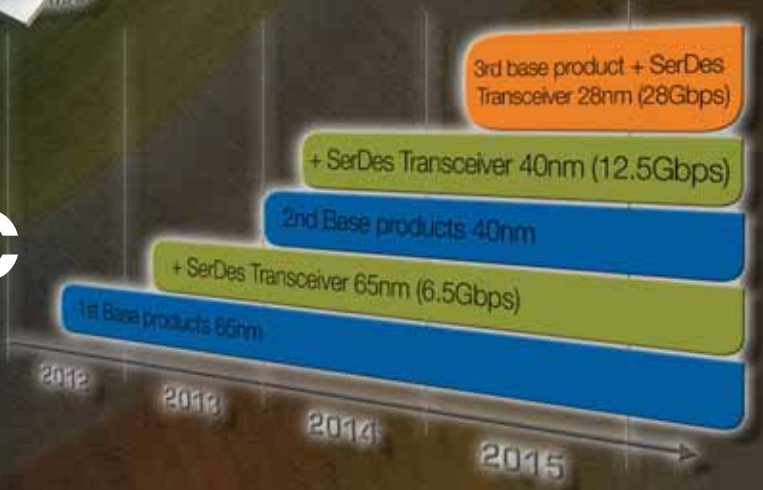


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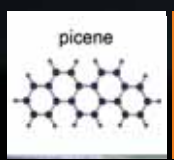


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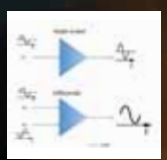

**Special Report**
Embedded system design

**3D Modeling**
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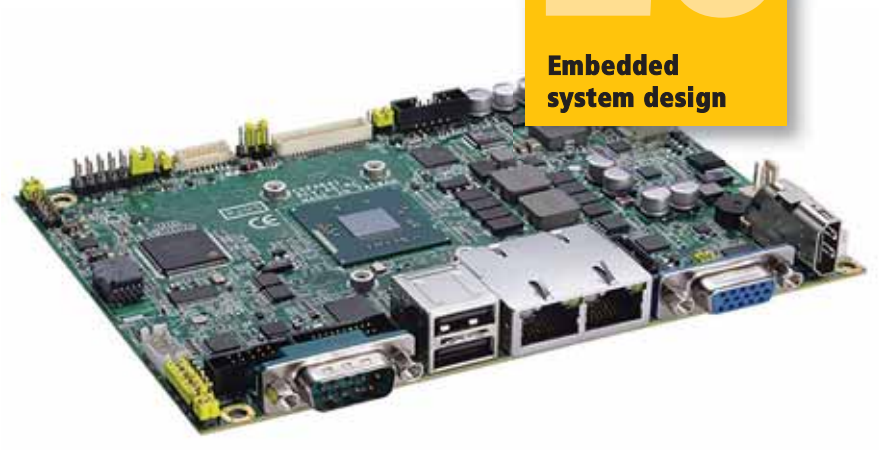

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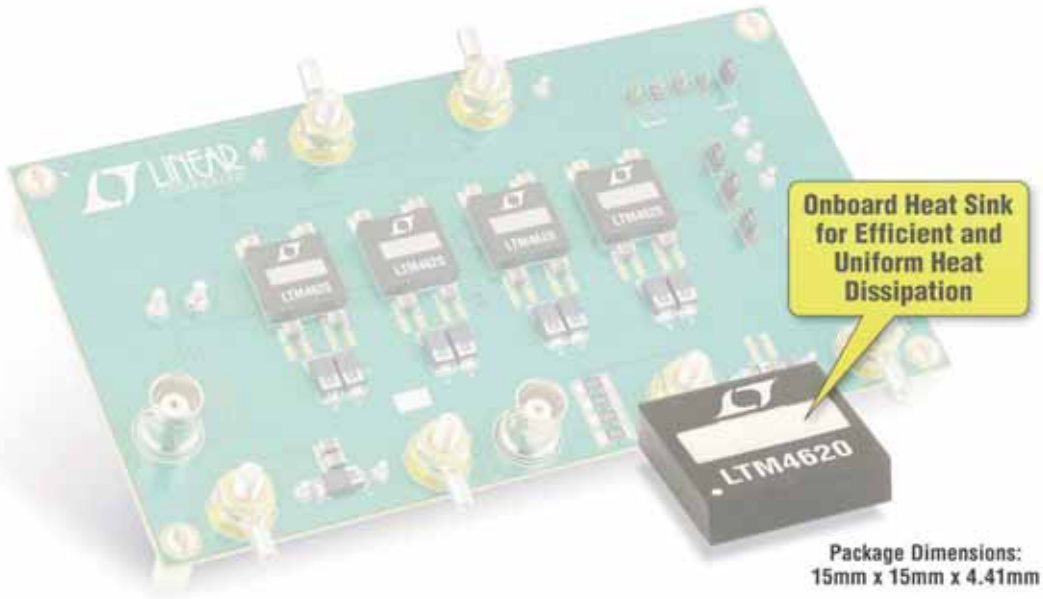


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# NEW SECURITY CHALLENGES FOR 2014

**Security experts have been saying recently that the network perimeter is dead and the boundaries that firewalls have established between the 'inside' and the 'outside' are disappearing; the static and physically established boundaries are dead because they cannot adapt quickly to changing threat and business requirements. This should change with Software-Defined Networking (SDN).**

In 2014, we will see adaptive perimeters or intelligence-based enclaves that dynamically serve business needs and defend against advanced threats. Self-forming enclaves are also proactive as they dynamically partition the network so no threat can bring down the business. SDN is one of the most exciting new capabilities of security architecture and, this year, SDN innovation will emerge, making it harder for bad guys to wreak havoc.

## "Security Of Everything"

Cisco has it right when it points to a future called "The Internet of Everything". Unfortunately, this means that certain things in our lives that were traditionally out of reach for the bad guys are now within it. 2014 might not be the "Internet of Everything" yet, but it will be the "Internet of Some Things", and those "some things" will need to be resilient to the threats present online. For everything we operate, we will need to answer the question: If it was compromised, how would it behave differently? While we are used to asking these questions of our computing devices, now we will need to ask this of our cars, home automation systems and even home appliances.

## Physical Authenticity Weakens With 3D Printing

We know a technology is disruptive when, on one hand, we can print out a firearm, and on the other we can print out a splint that saves a child's life. Such is the case with 3D printing. In our society, we still believe that the cost of copying something physical is high enough so there is low probability that criminals would counterfeit it. With 3D printing dropping in price, however, clever criminals will begin to copy physical objects that, by themselves, can provide authentication or access. Examples might include concert badges (maybe even backstage passes) and physical keys for simple locks. This will be a real threat any time a physical object alone is enough proof to gain access.

> *It's creepy, but if someone put a tracking device on us, how would we know?*

## Tracking Devices

I know it's creepy, but if someone put a tracking device on us, how would we know? We already have so many personal computing items in our pockets emitting radio signals, it would be a real task to detect such a tracker. In 2013 several start-ups introduced tiny devices that when attached to or embedded in objects can be tracked from a smartphone via a complicated mesh of peer-to-peer networks. The intended uses are to find objects such as keys, wallets, bags or even pets, but the bad guys are already thinking up nasty ways to exploit this very personal device. We may be getting to the point where next time someone hands us a gift we will have to scan it for 'bugs'.

If some of this technology sounds like it's come straight out of "The Matrix" then a crucial consideration for 2014 is a security strategy, as it is time to realize there are virtually no limits to today's technology innovations. Unfortunately, that also means that there are hardly any limits to the opportunities for today's online attackers. Attackers' inroads to corporate and personal data and assets continue to multiply, while their skills and resources also continue to grow.

The good news is that these same innovations are also part of the security solutions we have available today. It is time to look beyond our firewalls, antivirus and other conventional tools and embrace new, more progressive means of securing our networks in 2014 and beyond.

*Tim 'TK' Keanini is CTO at Lancope, network visibility and security intelligence company (www.lancope.com)*

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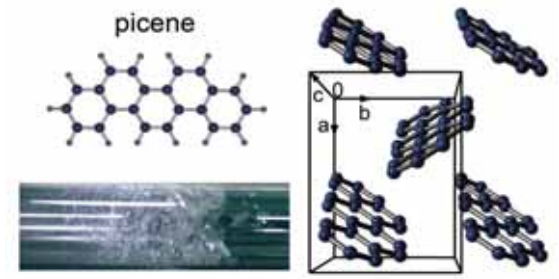
# "WE ARE USING CHEMISTRY TO PRODUCE NEW PHYSICS," SAYS A JAPANESE PROFESSOR

*Illustration of the structure of picene and a photograph of solid picene synthesized by Professor Yoshihiro Kubozono*




Research undertaken by a team at Okayama University promises a raft of innovative applications based on solid picene and organic superconductors, graphene and other functional materials.

Picene is a hydrocarbon found in the pitchy residue obtained in the distillation of peat tar and petroleum. When intercalated with potassium or rubidium and cooled to below 18K, picene exhibits superconductive properties.

"Our recent discovery that solid picene – a wide-bandgap semiconducting hydrocarbon – doped with potassium becomes superconducting at 7K and 18K is a good example because physicists are investigating the role of alkali dopants in organic compounds. We are the only group in the world focusing on superconducting picene," said Professor Yoshihiro Kubozono at the Department of Chemistry at Okayama University.

"We are using chemistry to produce new physics," he added. The results will lead to developing superconducting devices that use extremely low energy.

The project launched in July 2010 is part of a wider programme for the development of science and technology for a sustainable low-carbon society. Other areas of research at the Centre include high-efficiency organic solar cells, produced with new dielectric materials; high-performance organic field effect transistors (FETs), manufactured with low-energy-consumption processes; new types of superconductor-based organic materials; materials for high-temperature superconductors; and organic type system materials for optical energy conversion.

"The 13 internationally renowned scientists at the Centre are making steady and significant contributions toward realizing our mission," said Kubozono.

The 'Program for Promoting Enhanced Research Universities' will also invite and fund scientists from all over the world to conduct research at the Centre for up to three months.

# Embroidered Antenna Marks A New Wave Of Radio Technology Applications

Two UK universities have developed an embroidered antenna suitable to be woven into clothing. The researchers from Nottingham Trent University and Loughborough University have already shown a prototype garment, fabricated after optimising and altering conventional embroidery machinery.

Non-traditional yarns incorporate the conductive threads that make up the antenna. It is similar in size to a brand logo or emblem that is sewn or embroidered onto clothing.

"Monopole antennas are bulky, heavy and prone to breaking. They also attract unwanted attention for the military during covert and secure operations. This new design solves such problems by being small, lightweight, flexible and weather-resistant," said Professor Tilak Dias, leader of the Advanced Textiles Research Group at Nottingham Trent University.

The antenna's capabilities, including its operation in the MHz frequency range, were tested at Loughborough University's anechoic microwave measurement chambers.

"Producing an effective, flexible, fabric antenna presented many technical challenges, but working with our colleagues at Nottingham Trent University over the last three years we have been able to develop a working prototype which could be adapted to a multitude of applications," said Professor Yiannis Vardaxoglou, head of the Wireless Communications Research Group at Loughborough University.

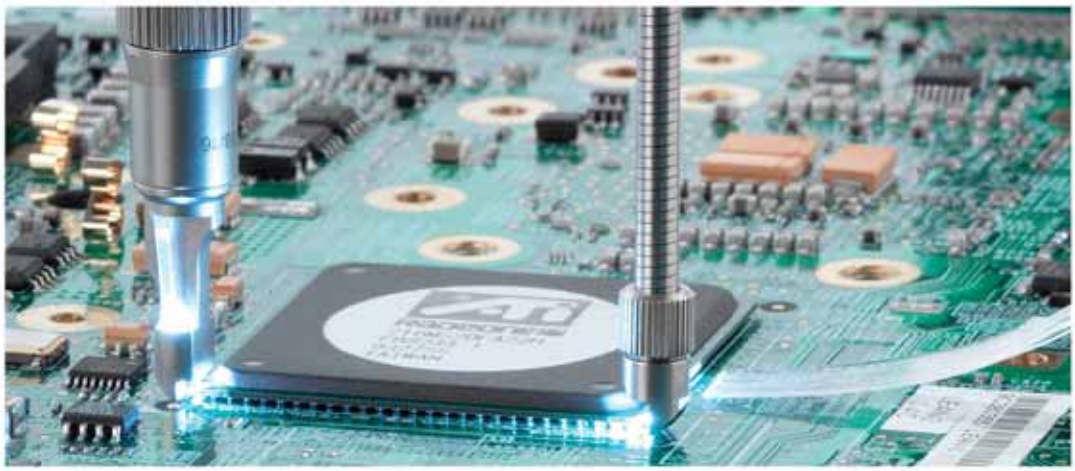
In addition, the embroidered antenna can be applied to any garment with a process that is quicker and cheaper than methods used to create traditional antennas.

Search and rescue teams could particularly benefit from the newly designed antenna, which is fully flexible, lightweight and water-resistant.

The consortium has been able to produce the antenna with grant funding of around £465,000 from EPSRC's Innovative electronics Manufacturing Research Centre (IeMRC).

*The new embroidered antenna is similar in size to a brand logo or emblem that is sewn or embroidered onto clothing*

# Elite Electronics



## Elite Electronics selects XJTAG boundary scan for accuracy and ease-of-use

**"Electronic Manufacturing Services Provider, Elite Electronics, based in Northern Ireland and the USA, specialises in building advanced assemblies for high-tech customers, particularly in the medical and power electronics sectors. Seeking to enhance in-house test capabilities by adding boundary scan, Elite's engineers chose XJTAG for its powerful user-friendly features and excellent support."**

**Elite Electronic Systems of Enniskillen, Northern Ireland, provides Electronic Manufacturing Services to customers locally and worldwide, offering facilities for advanced high-speed surface-mount assembly and final box build, as well as design and production of bespoke cables and harnesses. Its customers are active in diverse markets, and include leading brands in power generation, power monitoring, audio, scientific, and medical equipment sectors.**

To extend the test options available for customers, as well as increasing test coverage and speeding up diagnostics, Elite's Technical Manager, Mark McBride, decided to add boundary scan testing to the company's capabilities. Boundary scan testing can verify connections and check for correct operation of components without requiring direct physical access to device pins, delivering advantages such as shorter test duration, faster fault diagnosis and enhanced testability, particularly if a board contains devices with hidden I/O pins, such as BGAs or Chip-Scale Packages (CSPs).

After evaluating a number of boundary scan test systems, Mark McBride decided that XJTAG was the best choice for Elite's test department. "The structure of the system, the user interface, and the training and support provided convinced us to select XJTAG," he confirms. "Our engineers have become productive quickly, working at a high level without needing to be boundary scan experts."

Embedded computing boards are typical of the types of assemblies built on Elite's production lines. These contain components such as processors, FPGAs, DSPs and application-specific chips, many of which are boundary scan compliant and so can be tested directly using the XJTAG system. The boards also contain other non-JTAG devices, and so take advantage of XJTAG's extended capabilities for testing these via nets connected to boundary scan compliant devices. These include memory ICs, Digital-to-Analogue Converters (DACs), Ethernet controllers, connectors, switches, LEDs and many others. XJTAG is also able to program devices such as Flash chips and CPLDs.

"One of the most valuable aspects of using XJTAG is the system's ability to determine the precise locations of faults within processor-based assemblies," adds Keith Irvine, Test Supervisor. "This helps us identify the causes of any defects quickly, and then determine remedial action."

In particular, Elite's engineers were keen to use boundary scan for testing BGA devices. Since BGA I/O pins cannot be probed, pinpointing a faulty connection can be extremely difficult. "The XJAnalyser tool is extremely useful for examining BGA connections. We can set and toggle pin values, and trace signals easily with the help of colour coding and variable zoom levels, to identify faults such as shorts and opens."

The team at Elite also promotes XJTAG to customers, so that designers can optimise for boundary scan testing at the early stages of each new product lifecycle. "So far we have encouraged four of our customers to make contact with XJTAG, and invited them to our on-site training, to see how they can take advantage of the gains in productivity and quality that can be achieved."

## opinion

**Mark McBride, Tech Manager**
**Keith Irvine, Test Supervisor**
**Elite Electronics**

"The structure of the system, the user interface, and the training and support provided convinced us to select XJTAG. Our engineers have become productive quickly, working at a high level without needing to be boundary scan experts."

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| Customers | Diverse range of market sectors including Power, Medical, Audio Automotive, Industrial, Consumer... |
| Locations | Enniskillen, Northern Ireland Ridgeway, South Carolina, USA |
| Incorporated | 1986 |
| Web site | www.elitees.com |

# FIT-FAST STRUCTURED ARRAYS UNLEASH CUSTOM-IC PERFORMANCE AT FPGA VOLUMES

By Franz Hachmöller, Senior Product Marketing Engineer, Toshiba Electronics Europe

A new architecture featuring standard cells configured using a small number of metal layers significantly shortens development time and reduces NRE costs allowing low-volume projects to benefit from ASIC-like performance and power consumption.

Designers targeting a custom IC must typically choose between implementing their design in either an FPGA or standard-cell ASIC. An FPGA is usually the most economical solution if the intended production volume is low, since up-front costs are very low although the per-unit cost is relatively high compared to an ASIC.

The overall cost for an ASIC is calculated by a combination of the per-unit cost, which is much lower than the FPGA case, and also Non-Recurring Engineering (NRE) costs such as the costs of masks, package design and test development. The impact of the longer lead-time for an ASIC solution, in terms of potential opportunity costs, should also be considered. On the other hand, implementing a given design in an ASIC can result in higher performance and lower power consumption compared to an FPGA.

These factors have to be taken into account at the beginning of a project, to determine whether an ASIC or FPGA will provide the best solution. Ultimately the decision must be a "best-fit" compromise between the combined engineering and per-unit costs for the production volume, and the importance of factors such as time to market, chip performance, power consumption and die size.

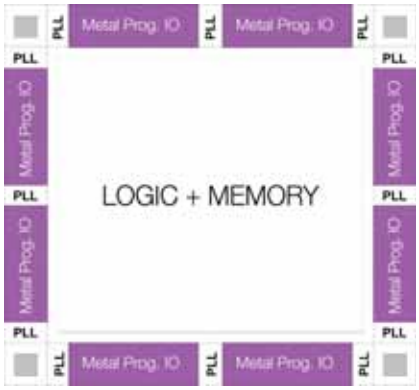



**Figure 1. Key features of the FFSA metal-configurable standard cell.**

Choosing between FPGA or ASIC is easier at the extremes: where low volumes are needed and fast time to market is important, an FPGA is usually most suitable. If volumes are high and a longer lead time can be accepted, and factors like power consumption are important, an ASIC can offer the best solution.

For projects that lie in the middle ground, particularly in terms of the intended production volume, the choice can be more difficult. Some FPGA vendors may offer a cost-down path by transferring the customer's completed FPGA design into a "harder" device similar to a structured ASIC. However, where offered, this tends to be for high-end FPGAs only.

A new type of structured array from Toshiba can now provide a better deal for custom-IC projects at lower volumes than are typically needed to justify a standard-cell ASIC. Toshiba's Fit-Fast Structured Array (FFSA) reduces NRE costs by up to five times compared to a standard-cell ASIC, while also reducing RTL-to-prototype time from around 25 weeks to just five weeks. Unit cost, power and performance are similar to a standard-cell ASIC. Compared to an FPGA, on the other hand, an equivalent FFSA can occupy up to 80% less die area allowing up to five times faster operation, while consuming only 10% of the power.

## INNOVATIVE CONFIGURABLE ARCHITECTURE

Toshiba's FFSAs are based on Metal-Configurable Standard-Cell (MCSC) technology. This allows custom devices to be fabricated on pre-designed and pre-manufactured base wafers that contain an optimised logic and block memory structure as shown in figure 1. This gate array has its own internal power structure, minimizes the die size and reduces interconnection distances.

Starting with this standardised platform, the gates are configured using four metal masks and four via layers. The FFSA's cell-based array occupies a smaller silicon area than the Look-Up-Table (LUT) based core of an FPGA, and also eliminates the FPGA's bulky interconnect fabric.

Minimising the metal layers needed to configure the gates helps significantly reduce NRE costs and turnaround time compared to a conventional standard-cell ASIC. In addition, as a metal-only configurable platform, FFSA considerably reduces development time for derivative products. This allows design teams to produce multiple ASIC designs cost-effectively, if needed to provide differentiated features or tailor end products for different regional markets.

The FFSA standard-cell library supports over 500 logic functions. Versatile memory resources include native dual-port/single-port memory blocks, which are configurable for different depths and widths, providing flexibility comparable to that of FPGA memory.

The FFSA provides flexible PLLs with a wide frequency range.

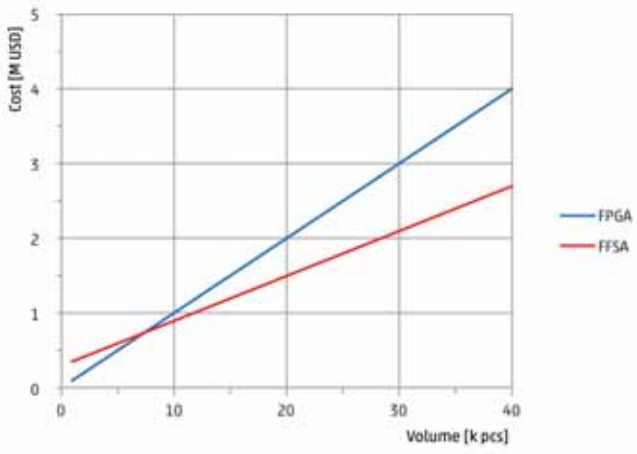



**Figure 2. Cost comparison showing FFSA can deliver a cost-effective solution at production volumes below 10,000.**

The I/Os are configurable and contain firm DDR/LVDS PHYs and configurable SerDes transceivers supporting a variety of common protocols as shown in table 1.

The first two available FFSA series are the SA5 series, and the SA5S, which has 6.5Gbit/s transceivers in addition to the basic SA5 features. Both are fabricated in 65nm process technology and integrate up to 15.1 million gates, 20.5Mbits of SRAM and over 1200 I/Os. At 65nm, the FFSA's cell structure, absence of LUTs, and use of direct metal connections instead of programmable interconnect array allows a significant reduction in die size compared with a 40nm FPGA.

Toshiba is now introducing the new SA6 and SA6S series FFSAs at 40nm. These platforms integrate more logic gates and memory blocks, and also feature 12.5Gbit/s transceivers in the SA6S. Looking further into the future, the SA7 FFSA series is planned in 28nm process technology.

## COST EFFECTIVE AT FPGA VOLUMES

FFSA devices can be produced in packages that are pin-compatible with existing FPGA designs, thereby providing customers with practicable route to reducing both the cost and power consumption of their designs while also boosting performance. Device operation and timing are guaranteed, effectively simplifying replacement of FPGAs on existing boards. Additionally, the seamless migration methodology guarantees electrical compatibility of I/Os thereby helping engineers maintain system-level or board-level signal integrity. It is also worth noting that bill-of-materials costs can be reduced since the lower power dissipation of FFSA devices reduces dependence on thermal-management components such as heatsinks.

To gain a realistic cost comparison, consider the example of a custom IC design targeted at a low-end FPGA costing $13 per unit at 20,000 pieces per year over a lifecycle of 10 years. The total number of pieces ordered suggests a total cost of $2.6 million. Consider the same design migrated to an equivalent FFSA costing $8 per unit. Benefiting from a relatively low NRE cost of $0.3 million, the total lifetime cost is $1.6 million netting a saving of $700,000.

The savings over a high-end FPGA design can be even greater. A project targeting a $100 FPGA, assuming 10,000 pieces per year over five years, will have a total project cost of $5 million. This compares with $3.3 million to implement the same design targeting a $60-per-unit FFSA including the NRE cost of $0.3 million. Figure 2 shows the relative cost for solutions based on FPGA and FFSA. FFSA allows customer designers to take advantage of the lower power consumption and higher performance of an ASIC at low production volumes that are not cost effective for a standard-cell ASIC.

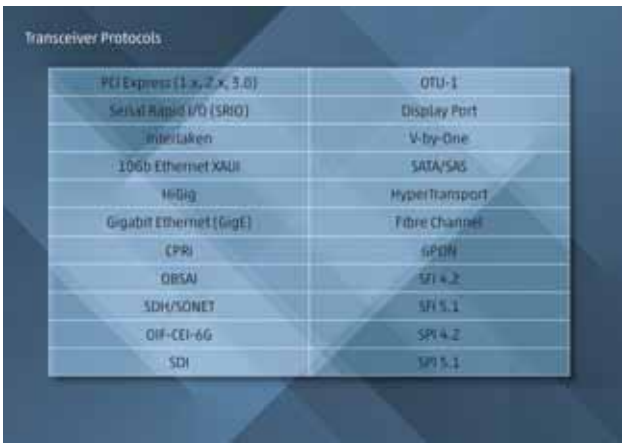



**Table 1. FFSA transceiver protocols**

## DESIGNING WITH FFSA

Figure 3 describes a typical FFSA development schedule, from design start to delivery of fully tested production units. Activities shown in blue are the responsibility of the FFSA supplier. Activities in green are under the control of the customer. The design flow illustrated uses methodologies that are already proven in the ASIC industry, helping ensure a low overall design risk.

Moreover, the IP blocks available to support FFSA design projects are also proven in numerous successful ASIC designs, and Toshiba continues to grow its portfolio. Several CPUs including the ARM® Cortex™-M3, various AMBA interconnects and common interfaces such as UART, SPI and I2C are already available. Popular high-speed serial interfaces and up to 10Gb Ethernet are among the connectivity standards supported, while various DSP functions such as an AES codec, High-Definition (HD) display controller, V-by-One® High-Speed transmitter and H.264 720p/1080p encoders are also available.

## CONCLUSION

FFSA provides a new choice for designers of custom ICs. Delivering most of the performance and power advantages of a standard-cell ASIC, but with significantly lower NRE costs, this new class of device offers a cost-effective alternative to FPGAs at volumes down to a few thousand units per year.

**www.toshiba-components.com**

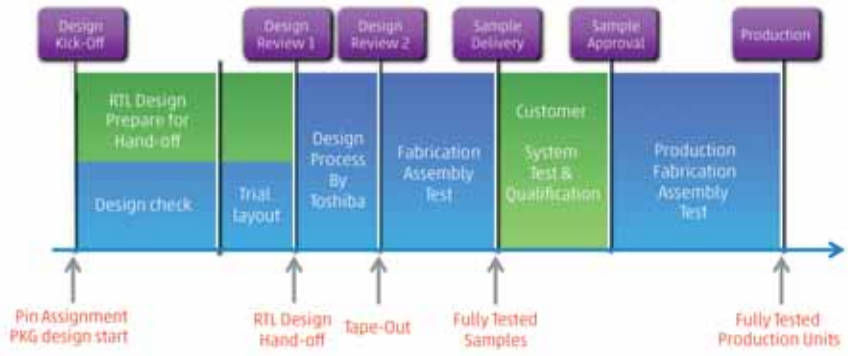



**Figure 3. The full RTL-to-production design flow is robust, yet significantly faster than the turnaround time for a standard-cell ASIC.**

# Shy Bairns Get Nay Sweets

## Getting Your Supplier To Design What You Need

**MYK DORMER** IS A SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD
WWW.RADIOMETRIX.COM

Low-power radio companies are – for the most part – small, technologically-agile organisations, led by their engineers or technically-skilled managers. They re-invest a large proportion of their turnover into product innovation, producing a constantly-evolving range of designs on the leading edge of market requirements.

Sounds familiar? I didn't think so.

Ten years ago my description above might actually have held some truth, but since the start of the recent financial crisis, our sector of the engineering industry has been infected with the same managerial disease that has crippled mainstream companies since the mid-eighties: decision making and strategic planning have moved away from staff (at all levels) who understand the products, technologies and underlying science, into the hands of those concerned only with short-term financial and operational management issues. This manifests as a trend towards companies that operate hand-to-mouth, governed only by a focus on short-term profit to the exclusion of all else. It can almost be dated from the point that the term "engineer-led company" became a derogatory epithet, instead of a description of a type of technologically-orientated organisation.

> *Decision making has moved away from staff who understand the products, the technologies and the underlying science, into the hands of those concerned only with short-term financial issues*

While I might disagree with the technologically-blind management strategies the wireless industry is now being ruled by, I also appreciate the unhappy truth that this disease is probably incurable. I have heard the all too believable (in the immediate term) excuses that "difficult financial circumstances require more efficient structures"; I have been told that "the banks insist" on this or that restriction; and I am painfully aware how much easier it is to manage only by immediate turnover and balance sheet, rather than trying to plan strategically into a technologically-fluid distant future. As a realist I reluctantly conclude that a return to engineering-led management is unlikely, but as an engineer I can see the serious problems that the "new methods" are causing.

I realise that the preceding comment reads like the start of some sort of radical technocratic manifesto, and from the point of view of the customer it hardly matters if their supplier of wireless hardware is run by engineers, accountants or magic pixies, but there is one vital point where the change I am describing is already beginning to have an effect on the end user: it is no longer the case that each year brings a crop of new designs, with useful features and improvements over the "older" designs. Without forward planning, the engineering departments of wireless companies are being prohibited from either designing new hardware or developing and expanding the existing range "for the sake of it". Instead, engineer-time is directed back into supporting existing production activities, or is parceled out in miserly amounts to sales-originated, sales-specified, "customer specific" projects, where an immediate short-term payback can be justified. Unfortunately, this results not only in a general technical stagnation, but also a fragmentation of a company's product range, as it changes from a consistent, generally-applicable "tool box" of radio devices to a random selection of "what the last man asked for, but didn't buy" products, which may have interesting features but will be unlikely to fit a mainstream application.

As an engineer in a low-power

wireless company I have been forced to accept this frustrating status quo, but does not mean that we have to accept that the entire wireless module sector is going to degenerate into a mixture of stagnant, obsolete designs and random, unplanned incoherence. If the manufacturing company managers cannot be made to plan for the future, perhaps the specifying engineers in the end-user companies can pick up the torch. I have a few suggestions:

- Look carefully at the existing product range of your module suppliers and look for consistent families of products. If the feature that you need (such as a different frequency band or power level, for example) isn't there, then it is worth querying it. As likely as not, the product you are asking for exists on a prototype bench, or in a design archive somewhere.
- Do not rely on catalogues, websites or published datasheets. Published materials often lag months, if not years, behind the actual state of the art in your supplier's organisation, and it can take longer to get an "official" datasheet written, or a management decision to include a product in the catalogue, than the design of the product takes to complete.
- Take the time to make human contacts in your supplier's organisation. Speak directly to sales staff, technical support people and, where possible, the engineering staff themselves. Make your requirements known, ask questions and make suggestions. A customer inquiry carries a hundred times the weight of any internal development request.
- Don't be fobbed off with formulaic "we don't make that" answers from low-end sales operatives. Keep on asking until you are speaking to someone who either will properly explain to you (reluctantly) why they can't supply what you are asking for or (more likely) will work with you to turn your requirement into a realistic product. Don't be surprised if they give you "magic questions" to ask through official sales channels that will then unlock permission for them to work on the technology you need.

> *Don't be fobbed off with formulaic "we don't make that" answers from low-end sales operatives*

- Above all, to paraphrase what I have said in the title, carefully plan what you want. Then clearly, and insistently, ask for it. You will be amazed what engineers can do if they are allowed to. Your requests, queries and specifications are the key.

# INTERFACING ACCESSORIES ON ANDROID

## ACCESSORY INTERFACES SIMPLIFY THE DEVELOPMENT OF EMBEDDED ANDROID APPS, EXPLAINS **DAVID FLOWERS** OF MICROCHIP TECHNOLOGY

Whilst mobile phones and tablet computers began life as embedded platforms, they now run on operating systems similar to that of a standard PC. They have become multi-threaded and even multi-core devices capable of simultaneously running multiple applications, maintaining multiple types of connectivity and providing the user interface. For the consumer, this delivers higher expectations, whilst for the application developer it delivers opportunities as well as challenges.

The opportunities include enabling mobile devices to interface to other electronic devices, such as personal fitness equipment and medical/health devices. The challenges lie in that developing new mobile apps can demand a very different set of design skills, especially for developers more familiar with creating applications on smaller processors.

### Understanding Threading

A sound knowledge of threading is important for all developers of mobile apps because it is central to the mobile devices' ability to run multiple operations simultaneously. Threading is the division of a programme execution within a process which creates two sets of code that can run simultaneously. Whilst one set of code waits for an event to occur before it can continue, the other thread must be able to carry on running. Without proper threading, the app's user interface would lock up and become non-responsive as tasks such as connecting to the Web, or via Bluetooth or USB, would block the thread for an unspecified amount of time.

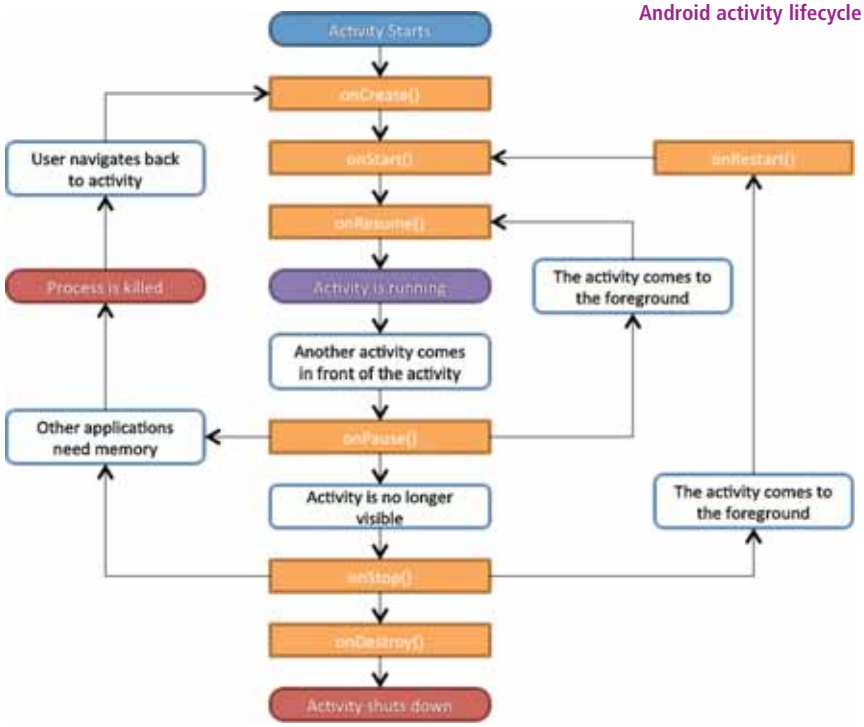
> The challenges lie in that developing new mobile apps can demand a very different set of design skills, especially for developers more familiar with creating applications on smaller processors

Threading also introduces the problem of concurrency into programme development. When two or more threads are running simultaneously, it is possible to have very complex data access issues when data needs to pass between two threads, or when the same data needs to be read or modified by two threads. Since each thread's execution time is unknown, it is possible to be modifying the variable in one thread at the same time a second thread is trying to read it. Java provides the answer to this with the use of a synchronised keyword: this allows developers to create sections that lock onto a shared object so that, if a thread is inside the synchronised section, no other thread can enter that section until the first thread has left it.

In Figure 1, the synchronised functions are used to ensure that variables 'a' and 'b' are modified together, resulting in the same sum. Without synchronisation, it would be possible for one thread to call the updateVariables() function 'b' in the code, just after 'a' has been incremented but before 'b' has been decremented, when a second thread calls the getSum() routine, resulting in a sum that is different for that brief moment of time.

Figure 2 shows how a synchronised section can be used instead of a synchronised function to achieve the same effect. Using a synchronised section allows other variables and functions within the parent object to continue to be used, since the lock is only placed on variable 'a' instead of the entire parent object. As synchronisation statements are slightly more complex and susceptible to errors, care must be taken to use the appropriate method for each function.

Android activity lifecycle



```
private Integer a = 0, b = 0;

public synchronized void updateVariables() {
        a += 1;
        b -= 1;
}

public synchronized Integer getSum() {
        return a + b;
}
```

**Figure 1:** Synchronised functions

```
private Integer a = 0, b = 0;

public void updateVariables() {
        synchronized(a) {
                a += 1;
                b -= 1;
        }
}

public Integer getSum() {
        synchronized(a) {
                return a + b;
        }
}
```

**Figure 2:** Synchronised keywords

```
public class PushbuttonMessage {
        private boolean pressed = false;
        public PushbuttonMessage (boolean state) {
                pressed = state;
        }

        public boolean isPressed() {
                return pressed;
        }
}
```

**Figure 3:** Create a class to be used as a message

```
private final static int BUTTON_EVENT = 1;

PushbuttonMessage pbMsg = new PushbuttonMessage(false);

/* Get a new message with the "what" of BUTTON_EVENT, and the button message
 that was just created */
Message msg = handler.obtainMessage(BUTTON_EVENT, pbMsg);
msg.sendToTarget();
```

**Figure 4:** Create a message and send it to a handler

Java also enables data or events to be passed safely between threads using handlers and messages. A handler is similar to a mailbox: Messages can be placed in a handler which then presents the first message to the thread, as soon as the associated thread is no longer busy. This method can be used to pass information about events or data between threads.

## Overriding Lifecycle Changes

Android activities or apps go through lifecycle transitions which occur when changes on the phone or tablet could affect the application. When developing applications targeted for the Android OS, it is important to understand the activity lifecycle because even simple user interactions, such as rotating the screen, sliding out a keyboard or receiving a call, can cause lifecycle changes in an application.

Many of the system resources an activity can request also specify that they must be freed on certain lifecycles states. For example, broadcast receivers are used to detect certain events that happen on the USB bus, such as when the device is detached. The broadcast receiver, however, needs to be unregistered when the application pauses and re-registered when the application resumes.

The Android OS provides a way to override the default behaviour of each of these events, so that developers can add any functionality required at these lifecycle transitions. To override a lifecycle function, simply use the state name as a function with the @Override keyword before it.

When overriding a lifecycle function, always use the super keyword to call the parent functionality that is being overridden. This ensures that the other steps normally occurring in that lifecycle change will still occur. Failure to do this can result in the

```
private final static int BUTTON_EVENT = 1;

private Handler handler = new Handler() {
        @Override
        public void handleMessage(Message msg) {
                switch(msg.what) {
                case BUTTON_EVENT:
                        /* Now that we know we have a button message, we know that the
                         object associated with the message is a PushbuttonMessage.
                         Create a PushbuttonMessage and cast the object to it so that
                         we can access its members */
                        PushbuttonMessage pbMessage = (PushbuttonMessage) msg.obj;
                        if(pbMessage.isPressed() == true) {
                                //do something here
                        }
                }
        }
};
```

**Figure 5:** Implement a handler to receive and decode a message

```
@Override
public void onResume() {
        super.onResume();

        //your stuff here
}
```

**Figure 6:** Override the onResume() function

```
<uses-permission android:name="android.permission.INTERNET" />
```

**Figure 7:** Add permission for an app to use the Internet

```
UsbManager = (UsbManager)getSystemService(Context.USB_SERVICE);

UsbInterface intf = device.getInterface(0);

UsbDeviceConnection connection = manager.openDevice(device);

connection.claimInterface(intf, true);

UsbEndpoint endpointOUT = intf.getEndpoint(0);

connection.bulkTransfer(endpointOUT, buffer, buffer.length, timeout_ms);
```

**Figure 8:** Connect via the USB Host API and despatch a packet

application crashing or failing to build. It is also important to realise that, sometimes, it matters where the parent functionality is called within the function. For lifecycle changes on the creation side of the cycle, onCreate(), onStart(), onResume(), the super function is typically called at the start of the function. For the lifecycle changes on the destruction side of the cycle, onPause(), onStop(), OnDestroy(), it is usually important to have the super call near or at the end of the function.

One method of working around the issue of having to handle various lifecycle changes is to move some of the handling of objects that need to survive these transitions to a service. Using a service for the data-connectivity objects can also allow multiple activities to share the same data connection.

## Wireless Communication

The three main connectivity interfaces are: USB, Bluetooth and Wi-Fi. However, these methods depend on the version of the OS, as well as the hardware features that are available on the device.

Wi-Fi is probably one of the easiest and best-documented interfaces available for app development. If the target accessory includes an HTTP server, the browser on the phone or tablet can be used to eliminate the need for a custom application. There are also different telnet/ftp applications available that can also eliminate custom development. If a custom application is required, Java offers network APIs and there is ample reference material on how to use them.

> Before version 2.3.4 of the Android OS, the USB port was used exclusively by the device manufacturer, making it unavailable to application developers

There is, however, one Android OS-specific item that needs to be added to the application before the app is able to use the networking API. In the AndroidManifest.xml file, the activity that is accessing the network API needs permission to do so by adding the line depicted in Figure 7.

One major limitation when using an Android device's Wi-Fi for accessory interfacing is that Android does not currently support ad-hoc networking, so a network infrastructure is required before the Wi-Fi accessory can operate. This may be realistic for some applications, such as a thermostat in a house that will always have Wi-Fi connectivity to the home router, but unrealistic for nearly all mobile accessories.

Different Android OS versions offer support for different Bluetooth devices. The Android v2.x versions support the Serial Port Profile (SPP), although not all devices with these OS versions are capable of using the feature. The SPP profile is useful for creating custom applications that do not have a predefined data format. For more specialised accessories, v3.x introduced support for the headset and Advanced Audio Distribution Profile (A2DP), whilst Android OS version 4.x introduced support for the Health Device Profile (HDP).

## USB Connectivity

One of the most recent methods for downloading data from an Android device is USB. Before version 2.3.4 of the Android OS, the USB port was used exclusively by the device manufacturer, making it unavailable to application developers. This changed with the v2.3.4 and v3.1 Android OS updates, allowing developers of Android accessories to use the USB port.

Android version 3.1 then introduced a USB Host API, allowing developers to use standard USB peripherals plugged into a suitable Android device. The OS also has built-in support for some USB device classes, such as Human Interface Device (HID) and Mass Storage Devices (MSD). These built-in drivers allow these USB peripherals to be used seamlessly, just as they are used on a standard computer. For peripherals without built-in support, the USB Host API allows app developers to connect and communicate directly to the USB endpoints through a simple, low-level API set.

In order to gain permission for the USB Host API, the app needs to declare use of the library in the AndroidManifest.xml file, as shown in Figure 9.

Setting up a device filter enables an application to auto-launch when a specific peripheral is plugged into the USB port. In the AndroidManifest.xml file, an intent filter must be created and associated with the USB_DEVICE_ATTACHED event, and that must be associated to a filter file such as "xml/device_filter.xml".

The device_filter.xml file contains information about the devices that should cause the app to launch. This can be either by the Vendor ID (VID) and Product ID (PID) pair, or by the class, subclass and protocol set.

It is also possible for application developers to be less specific by not including every attribute in the tag. In the absence of a product-ID attribute, for example, any matching vendor-ID device can cause the app to launch.

## OpenAccessory USB

To enable USB capability in Android devices without hardware support for the USB Host, Google added the OpenAccessory framework onto the standard USB drivers in the Android devices.

```
<uses-library android:name="android.hardware.usb.host" />
```

Figure 9: Enable an app by permitting access to the USB Host API

Figure 10: Auto-launch an app when a device is attached in USB Host mode

```
<intent-filter>
        <action android:name="android.hardware.usb.action.USB_DEVICE_ATTACHED" />
</intent-filter>
<meta-data android:name="android.hardware.usb.action.USB_DEVICE_ATTACHED"
 android:resource="@xml/device_filter" />
```

```
<?xml version="1.0" encoding="utf-8"?>
<resources>
        <usb-device vendor-id="1240" product-id="516"/>
        <usb-device class="256" subclass="256" protocol="5"/>
</resources>
```

Figure 11: Set-up a filter for a device to launch an app in USB Host mode

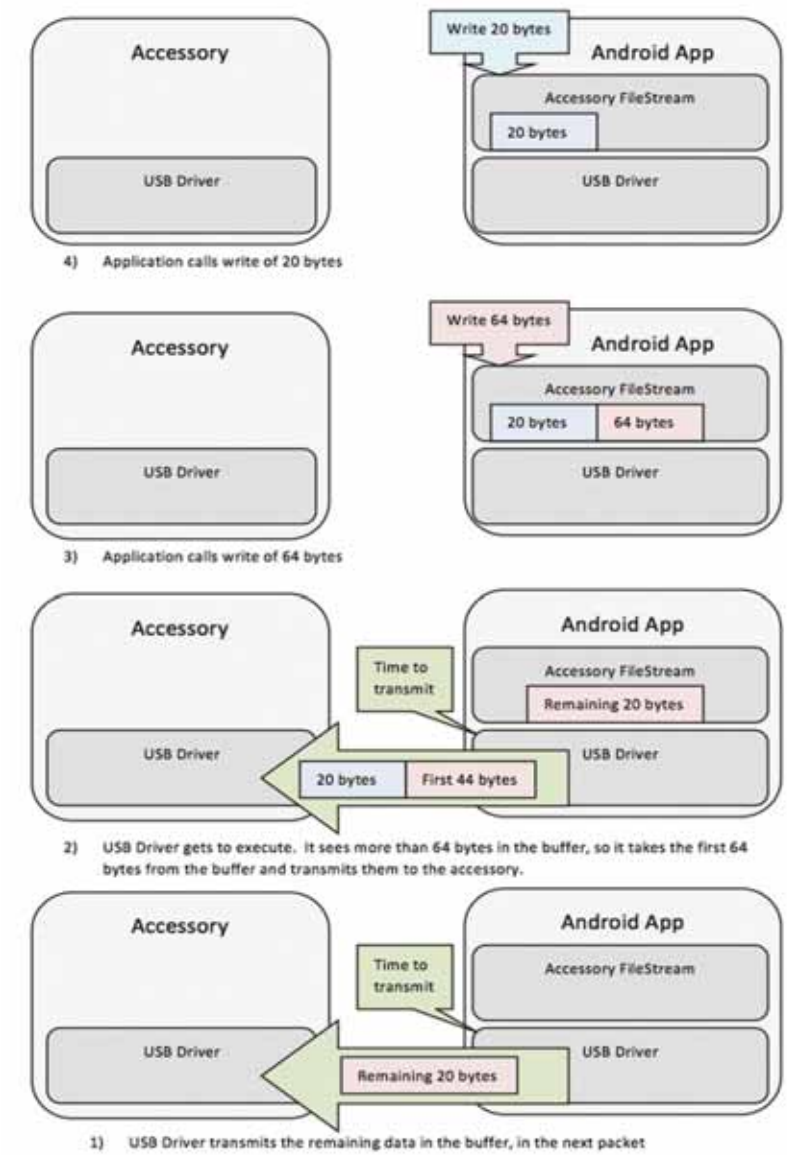



Figure 12: Data packing and fragmentation

This enables accessory developers to use standard USB port functionality for custom USB traffic.

The OpenAccessory protocol achieves this by first exchanging a few custom, vendor-class, device-level control transfers to the USB port, as developed by the manufacturer of the device. These commands switch the USB drivers into an accessory mode and cause the USB peripheral to detach from the bus and reattach in accessory mode, with Google's vendor-ID and one of two specific product-IDs. In this mode, there is a vendor-class interface that can be accessed by an application.

The interface that OpenAccessory presents to the application is like the FileStream format. Data is written and read from the stream, similar to the way a file is read and written. This differs from most firmware implementations for USB peripherals, in which the interface is based on the USB packet size. The issues that result from this difference need to be understood by the app developer and the accessory firmware developer.

The Android device's USB driver receives a file stream and, therefore, it does not recognise or understand the potential logical breaks in the data for specific commands. The data from two separate calls to the app's write function can bring packets together into the same USB packet. The firmware needs to be aware that a received USB packet could contain information from two separate calls to the write function from the app.

A single call from the app to the write function could also be fragmented across multiple USB packets. The USB driver on the Android device will break the data into packets and send them to the accessory and the accessory must be able to reassemble data into the appropriate format.

Packing and fragmentation can also occur together. For example, the OpenAccessory framework currently uses 64-byte packets. If the app calls the write function twice, back to back, the first call sends 20 bytes of data, and the second call sends 64 bytes of data. As such, it is possible for the two sections of data to be packed together into an 84-byte block of data, depending on when the USB driver takes the data from the stream and sends it over the bus. The USB driver then needs to break this stream of data into USB-sized packets, by

```
<uses-library android:name="com.android.usb.accessory" />
```

**Figure 13:** Set-up a filter for a device to launch an app in USB Host mode

```
<intent-filter>
        <action android:name="android.hardware.usb.action.USB_ACCESSORY_ATTACHED" />
</intent-filter>
<meta-data android:name="android.hardware.usb.action.USB_ACCESSORY_ATTACHED"
 android:resource="@xml/accessory_filter" />
```

**Figure 14:** Launch an application in OpenAccessory mode

```
<?xml version="1.0" encoding="utf-8"?>
<resources>
<usb-accessory manufacturer="Microchip Technology Inc." model="Basic Accessory Demo"
version="1.0" />
</resources>
```

**Figure 15:** Use a filter to determine which devices will launch the app

sending the first 64 bytes of data, followed by a packet of 20 bytes. The first packet, however, contains the 20 bytes of data from the first write and 44 bytes from the second write. The second packet of 20 is the remaining data from the second write.

The final challenge is to understand how USB bulk transfers are formed. According to the USB specification, USB bulk transfers are complete when the exact amount of expected data is sent and a packet smaller than the endpoint size, or a zero-length packet, is sent. To complete a transfer of a block of data that is an exact multiple of the endpoint size, currently 64 bytes, accessory developers must follow this with a zero-length packet. Failure to send zero-length packets, when required, can result in the data remaining in the Android USB driver without being transferred to the OpenAccessory FileStream and, as such, never being transferred to the app. The OpenAccessory framework also requires permission in the AndroidManifest.xml file, as shown in Figure 13.

The device can auto-launch an app based on string information passed during the steps required to enter accessory mode. This is done through xml files that are similar to the USB Host API, see Figure 14.

The OpenAccessory framework's most significant drawback is that it is an optional add-on library in the Android OS. Some manufacturers, therefore, have chosen not to include it, so it is not possible to assume that every device with a suitable OS version will support this functionality. Support may also be included in one version of the product, but withdrawn in subsequent versions.

The release of the Android 4.1 Jelly Bean introduced version 2 of the Android Open Accessory (AOA) protocol, which gives accessory developers two new features: the addition of support for digital audio output and Human Interface Device (HID) controls from accessory mode.

## Digital Audio

Support for digital audio output allows easy creation of audio docks with Android devices. Whilst an audio dock was possible with AOA version 1, it required the designer to create a custom protocol and use a custom application. Any standard application would still output audio via the headset or speakers. With AOA version 2 all core audio on the Android device is routed to the USB port, allowing the audio to work with any app or feature on the device. AOA version 2 also allows the audio interface to be accessed with or without launching the app when docked. Not sending the manufacturer or model string to the Android device before it enters accessory mode still permits the accessory to be docked without being launched.

## Interface Controls

Human Interface Device (HID) controls from accessory mode were previously only available in USB Host mode. With AOA version 2, accessories can send HID reports to the associated Android device and to the OS to control the user input. This is useful for audio dock controls as well as for the further development of control devices such as mice, keyboards and joysticks.

## Understanding Accessory Interfaces

Understanding the capabilities and limitations of accessory interfaces is crucial for transforming a hardware design into an effective Android accessory. Skills such as threading, wireless communication, using Android as a USB host and digital audio will probably all have to be mastered. ●

**FURTHER INFORMATION:**

Development resources for the challenges discussed in this article, including free firmware and example Android accessories, can be found on the Microchip websites for www.microchip.com/android, /USB, /wifi and /bluetooth.

# EMBEDDED SYSTEMS FOR VISION-BASED DRIVER ASSISTANCE

**MICHAEL STAUDENMAIER** AND **DR STEPHAN HERRMANN** FROM FREESCALE HALBLEITER GMBH GIVE AN OVERVIEW OF THE APPLICATIONS AND BENEFITS OF CAMERA-BASED ACTIVE SAFETY SYSTEMS, INCLUDING FUTURE TECHNOLOGIES FOR VISION PROCESSING

In the last few decades, the number of casualties on the road has dropped significantly, due partly to the high penetration of safety systems like airbags or electronic stability control. However, this trend slowed down in recent years and the accident statistics show no further reduction in fatalities [1]. One reason is the ever increasing and more complex traffic; another is driver distraction by communication equipment like smart phones whilst driving.

Advanced driver assistance systems (ADAS) will help establish a positive trajectory towards zero fatalities. One such feature is 360° sensing based on camera and radar sensors to provide the driver with a natural view of the car surroundings, to capture all hazards at a glance. In addition, the driver will be assisted in emergency situations by semi-autonomous systems.

## Regulations and Features

In the effort to further reduce road casualties and accidents, many countries are preparing regulations that involve driver assistance systems. One example is the Euro NCAP rating that will include active safety systems and help increase car buyer's awareness of such systems.

Another important factor for the mass-adoption of active safety systems is their affordability. The more people can afford such a system, the safer driving will become. The aggressive shrink path of semiconductor technology will make them even more attractive for the mass market.

Due to higher sensor resolutions and more advanced algorithms, performance requirements increase with every generation. In addition, the mounting position of a camera module behind the windscreen implies a high ambient temperature of 105°C. These contradictory requirements make power consumption one of the biggest technological challenges to camera-based driver assistance systems.

## Camera-Based Solutions

Multi-purpose front-camera solutions for headlamp control, lane keeping, traffic-sign recognition and collision avoidance today use CMOS imagers with resolution of up to 1.2 Megapixels at 30 frames per second. The resolution will further increase with next generation sensors.

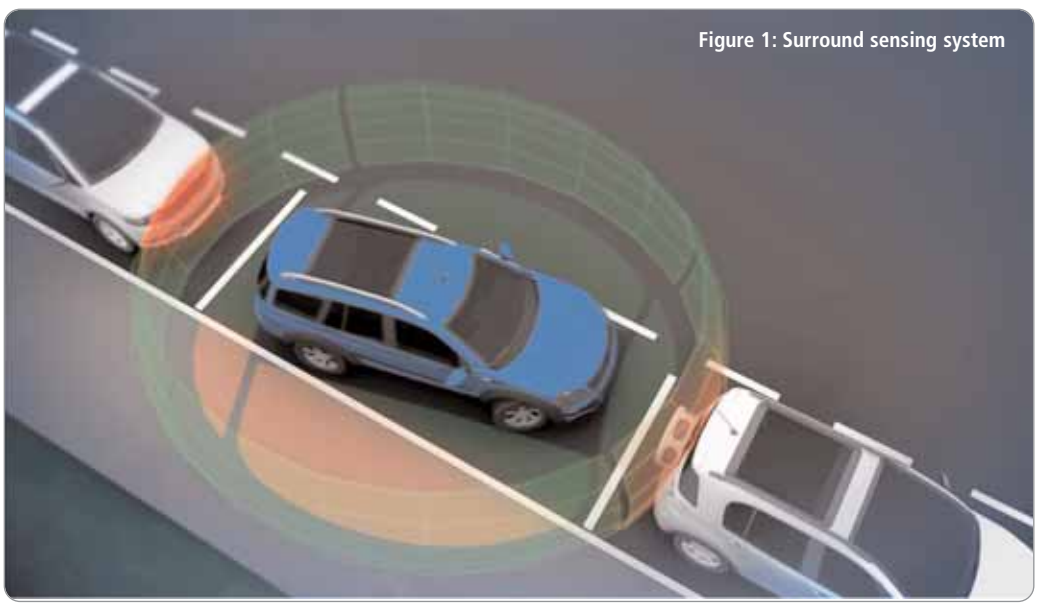


Figure 1: Surround sensing system

Complex algorithms are required for reliable object-detection, even under difficult weather and lighting conditions. Semi-autonomous driver assistance, like lane keeping, emergency braking or traffic jam assist, requires ASIL D safety level with algorithmic redundancy and massive computational power. Today's camera solutions use several processing elements, like dedicated hardware accelerators, FPGAs, DSPs and general-purpose processors; such camera modules consist of several devices on the printed circuit board.

The need for miniaturization and cost reduction requires a higher level of integration. Until

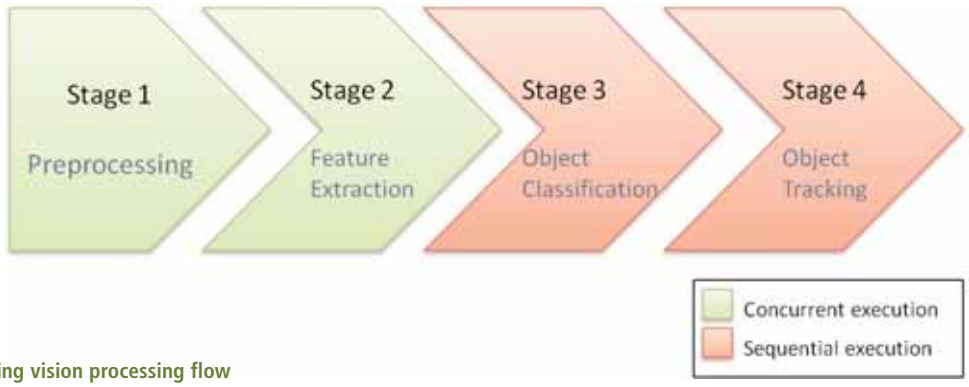



**Figure 2:** Computing vision processing flow

recently, a more general and fully programmable integrated solution for high-performance camera systems was hindered by the maximum power dissipation acceptable within the installation space. Progress in the field of semiconductors and the development of highly optimized programmable architectures using a highly parallel computing approach make such single-chip solutions possible.

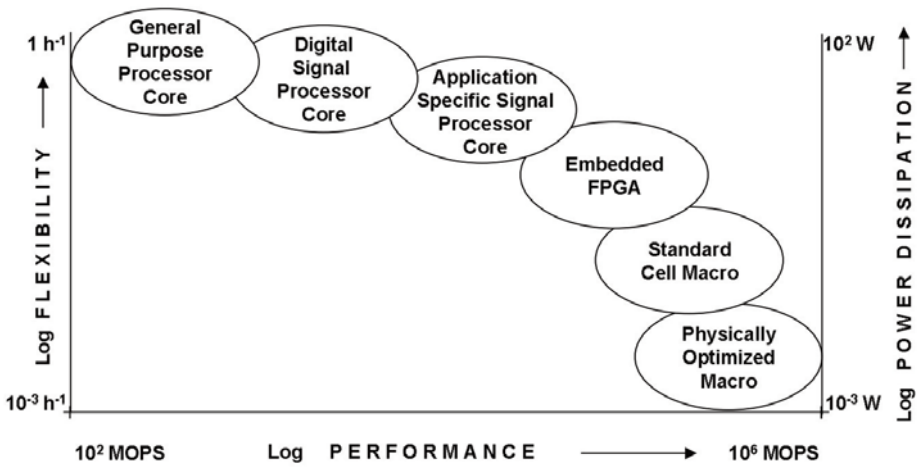



**Figure 3:** Processing architecture options

## Processing Steps for Vision Computing

The different stages of image processing have distinct characteristics. The first stage does the sensor data pre-processing, such as filtering and image enhancement. The required operations work on a sliding window of limited size and are often well suited to highly parallel processing. Each pixel is processed and the number of operations per second is huge, but the data flow can be organized using relatively small local memory.

The second processing stage extracts features, e.g. edges or corners, from the image. This processing often also works on a pixel basis using a sliding window and, from that perspective, has parallelization features similar to the pre-processing step. The resulting extracted features are either pixel-orientated or descriptor-orientated. Descriptor-orientated features will use complex data structures with highly condensed data maps.

The third stage does object classification based on feature maps. The detected objects result in greatly reduced amounts of data. Unlike pixel-based processing of previous stages, the object detection algorithms have complex control flows resulting in a random data access pattern. The required processing performance on the feature processing level is still high, as the evaluation of many different features in combination with a rich classification data base is required to achieve robustness and an acceptably low false-detection rate.

The fourth stage tracks the detected objects over several frames, implements a comprehensive model of the environment around the car and assesses the situation to trigger actions. Again, the required processing is highly non-linear, but the amount of data is relatively small.

To quickly adapt to evolving algorithms and changing market requirements, all stages require flexibility and programmability. Due to the different characteristics of processing and data access, each stage requires a different processing architecture to achieve the best performance at the lowest power consumption. Figure 3 shows the typical architecture options and their characteristics regarding flexibility, performance and power dissipation.

## Dedicated Hardware Accelerators Solutions

Dedicated accelerators offer the highest performance at the lowest power consumption (see Application Specific ICs and Physically Optimized ICs in Figure 3). The architectures usually consist of a set of hardware modules capable of performing a specific image processing task with a specialized data path, compared to simple MAC operations. Each processing block is highly optimized, but has limited flexibility. The set of fixed function hardware accelerators is implemented as a sub-system and integrated in an architecture capable of coping with the high data bandwidth (see Figure 6). Usually, the implemented functionality is tailored to a specific class of processing and reuse of the vision processing accelerator for different applications, for example where video compression is very limited.

Typical functional blocks used in a dedicated hardware

Figure 4: Image rendered with Sobel filtering

Figure 5: Harris corner detector

accelerator for vision processing include:

- FIR-filters (finite impulse response filter) with parameterizable filter kernels, such as:
- Scaling filters to generate a pyramid of smaller versions of the high-resolution input image;
- Sobel filtering as shown in Figure 4.
- Histogram calculation of image statistics.
- Motion analysis using special data types (e.g. feature-based) or higher level of regularity (e.g. block-matching).

Dedicated hardware accelerators are the most efficient way to implement a specific processing task from the power/cost perspective. The features are limited to exactly the required functionality, and the data flow is highly optimized. However, the biggest drawback is limited flexibility, so dedicated accelerators are well suited for mature algorithms, which don't require major changes with every new device generation.

Due to their fixed functionality, dedicated accelerators should be used for common and non-differentiating parts of the processing chain. Due to their power efficiency, maturity of algorithms and their highly parallel structure, dedicated hardware accelerators are the best choice for the first processing stage in vision processing, e.g. image enhancement for visual quality. These dedicated-function units are often implemented as a processing pipeline, in which the data is streamed through the processing units. Thus, they add little processing latency and can operate on local memory.

## Field-Programmable Devices

Field-Programmable Gate Arrays (FPGA) offer a high degree of flexibility. FPGAs are well suited to algorithms with a high degree of inherent parallelism, like pixel-based processing, and therefore fit well into the first and second stages of the vision processing pipeline. The FPGA programming model supports unlimited parallelism, so FPGAs scale well due to the parallelism of the algorithms.

However, high flexibility comes at a cost. One challenge is to achieve functional safety, as the mechanism for reconfiguration can become a single point of failure. In addition, FPGAs generally use more power because of their internal physical structure that has significant interconnect overhead. This interconnection structure also leads to increased production costs (mask layers) for the silicon itself. With volumes picking up in the driver assistance market there is a strong push towards highly integrated single-chip solutions with several megabytes of memory included. This implies challenges for the FPGA as they need significantly more metal layers for their interconnect fabric. The additional production layers add manufacturing cost to the integration of memory and standard cell logic.

## Digital Signal Processors

Digital Signal Processors (DSP) offer a good compromise for handling algorithms with parallel pixel processing, along with processing custom data structures or complex control flows, making them efficient for stage two and three of the vision processing pipeline.

Very Long Instruction Word (VLIW) DSPs today have high complexity and long pipelines. Thus, the number of cores in a DSP system is much more limited compared to architectures with very simple cores. DSPs scale well when increasing frequency with every new generation, but as the increase of frequency has slowed with recent generations, a single DSP will no longer be sufficient in the future for many applications. DSP-based solutions will see limitations in scalability, while as yet there's no established, transparent, programming model for multi-core DSP applications.

Meanwhile, DSPs also see strong competition from RISC architectures as their signal processing capabilities for parallel operations get closer to those of native DSPs with every new generation, by using integrated co-processors with vector SIMD architectures. Compared to RISCs, DSPs still provide advantages by using Harvard architecture with multiple data buses offering higher data throughput, memory operands or specialized access patterns for unaligned data. The VLIW allows doing the data addressing in-parallel with data processing. Both RISCs and DSPs typically provide single digit of thousand MIPS, which is at least one order of magnitude below what is achieved with dedicated architectures or FPGAs.

## Graphic-Processing-Unit Based Solutions

Graphic Processing Units (GPU) fall into the category of Application Specific Instruction-set Processors (ASIPs), see Figure 3. Using GPUs for parallel processing tasks, like computer vision tasks, is very popular in the desktop PC arena, where powerful graphic cards offer the possibility to use the processing elements originally integrated for OpenGL shaders as a general purpose, massively parallel, programming environment.

Elsewhere in the high-performance computing domain, GPUs have already replaced DSPs in many areas. One driving reason is the availability of powerful GPU architectures with hundreds of shader units at relatively low cost, driven by the consumer market. Another reason is the availability of OpenCL or proprietary CUDA programming models supporting unlimited parallelism, so GPUs provide very good scalability and a future-proof roadmap.

Embedded Multi-Core Processing Units (MPUs), like Freescale's i.MX6 family, have powerful GPUs integrated and are used to accelerate vision-processing tasks. An embedded GPU normally offers significantly fewer parallel processing units than a dedicated accelerator or an FPGA, and the instruction set is less flexible than that of a DSP. Therefore, GPUs fit well for parts of stage two and three of the vision processing pipeline. Up to now, the power envelope available in embedded systems has not allowed full pixel processing with a GPU, because of the huge functions overhead for graphic and general high-performance computing, not required for computing vision tasks. The additional hardware not required for vision processing not only consumes power, but also adds significant cost to the embedded platform. One example is support for floating-point operations, which isn't required by the first stages of the vision processing pipeline.

Another factor is the bandwidth limitation to external memory. While state-of-the art desktop PC graphic cards usually have at least a 256bit-wide memory bus at 1GHz, this is not a viable solution for the embedded space due to the power envelope available.

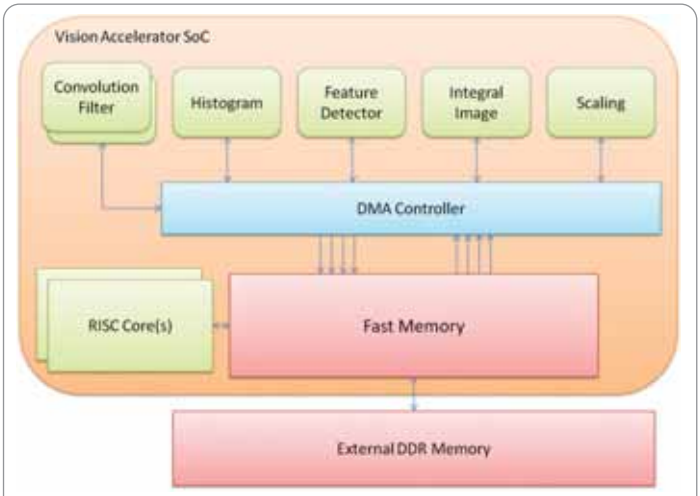



**Figure 6:** Dedicated hardware accelerator sub-system

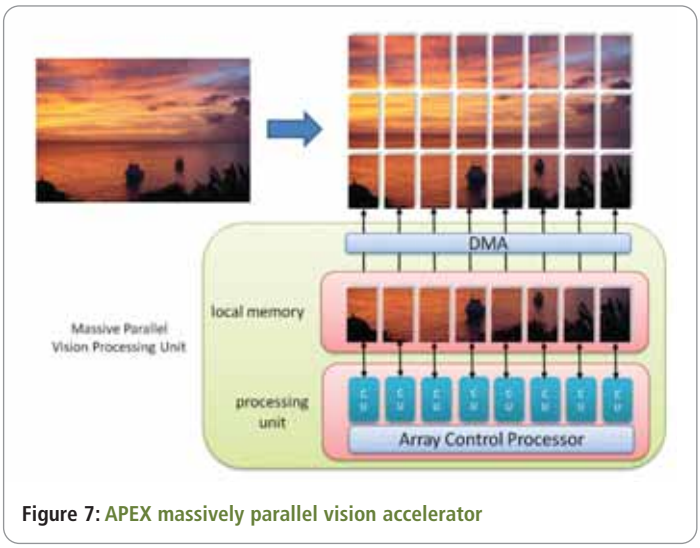



**Figure 7:** APEX massively parallel vision accelerator

GPUs are very good at speeding up algorithm development on a PC leveraging a powerful graphics card, but they are not efficient for embedded vision processing.

## Massively Parallel Systems

Another type of ASIP are massively parallel systems, which are well suited to the compute-intensive pixel processing part of stage 1 and 2 of compute vision. The programmability of such a solution leads to great flexibility and allows definition of the functionality by software. Employed there they usually have a significant portion that can be distributed to parallel processing units. Those algorithms use a rather linear program flow, which can be distributed well to a grid of many small and simple cores.

In contrast to GPUs, a massively parallel vision accelerator can be optimized for the specific requirements of the application, e.g. optimization of the Computation Units (CU), which are equivalent to shaders in GPUs. For vision use, float functionality is not a strict requirement and can easily be replaced by fixed-point arithmetic. This allows removing the float units from all the CUs, which leads to a significant saving of die size.

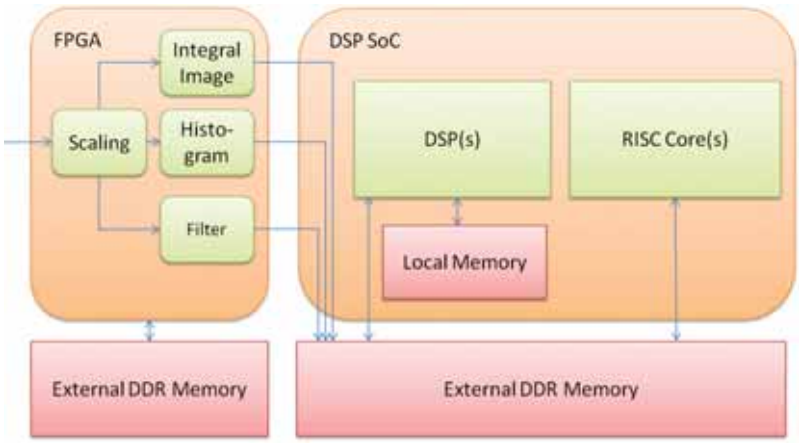



**Figure 8:** FPGA and DSP hybrid solution

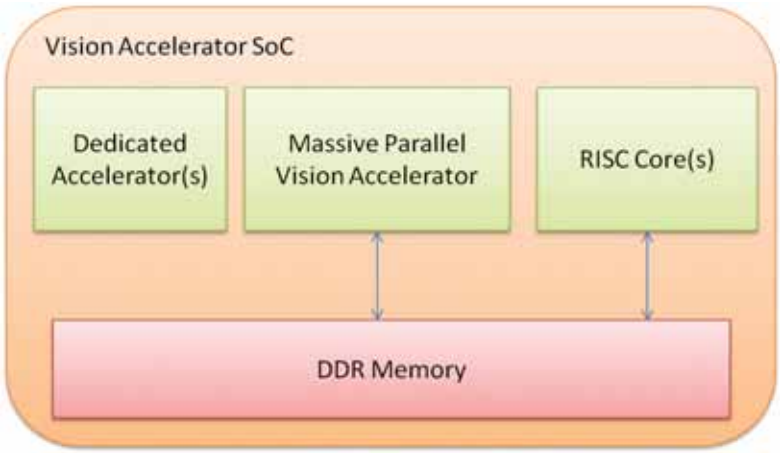



**Figure 9:** Homogeneous parallel vision system

Another area of optimization is data flow and memory access – as memory access for pixel processing is usually predictable and linear, this path can be optimized for the specific application and even assisted by special hardware like DMAs. The optimization results in an ASIP for compute vision that is not only significantly smaller but also consumes substantially less power. Freescale offers a dedicated compute vision solution for rear-view camera applications employing a homogeneous parallel vision accelerator called APEX.

## Hybrid Solutions

Due to the different characteristics of the vision processing pipeline stages, a complete system solution must consist of a mix of different processing architectures for lowest cost and power consumption. One or more RISC cores are always used to host stage four of the vision processing pipeline, the operating system and the application software. In the current phase of the driver assistance market, which isn't yet mature and shows rapidly evolving functionality with every new generation, FPGAs and DSPs combined on a printed circuit board with a RISC core are widely used for flexibility (see Figure 7). However, power consumption remains a challenge for this hybrid solution and is the main limitation on performance. The need for several devices, including high pin-count DDR memory interfaces, adds significant cost to the printed circuit board and limits miniaturization of the camera module, which is highly desired by car makers. For the future high-volume camera solutions required to achieve a high NCAP rating in Europe, there is a strong push from the market towards fully integrated single-chip solutions, to include all processing elements and a large amount of memory.

For the pixel-based processing steps of stages one and two of the vision processing pipeline there are competing processing architectures with individual advantages and disadvantages. In the solution of Figure 8, stage one is implemented on an FPGA and stage two is split between an FPGA and a DSP. Since FPGAs add manufacturing complexity to a fully integrated System-on-Chip (SoC) and are not optimal in terms of power consumption, the mature parts of stage one, i.e. the scaling, histograms and FIR for camera input processing, should be implemented in a dedicated accelerator, which provides lowest power consumption and lowest cost (see Figure 8). The rest of the pixel-based processing of stage one and two, requiring software-programmable flexibility, should be hosted on a massively parallel vision processor like APEX. The advantage is lower power consumption, compared to executing these tasks on a general-purpose DSP, and the availability of a programming model supporting unlimited parallelism.

GPUs are not an efficient alternative for vision processing due to their significant overhead, most of which is not required, and due to the limiting bandwidth of the DDR memory. The parts of stage four processing, hosted on the DSP in Figure 7, already contain a high degree of processing with a complex control flow for object classification. These algorithms can be executed without a big loss of efficiency on RISC cores with a DSP extension. The resulting SoC solution is a very good tradeoff between low power consumption, system cost and flexibility. It also offers very good scalability for today's systems and future generations.

Two programming models are sufficient for a fully integrated vision-processing platform to efficiently address all the different processing stages and allow a high level of software reuse.

## Standardized Programming Model

Software is a significant cost factor since the software complexity of an ADAS system is massive and requires extensive testing and qualification to comply with safety and reliability requirements. Therefore, increasing software reuse is key to reducing the overall development cost and time-to-market.

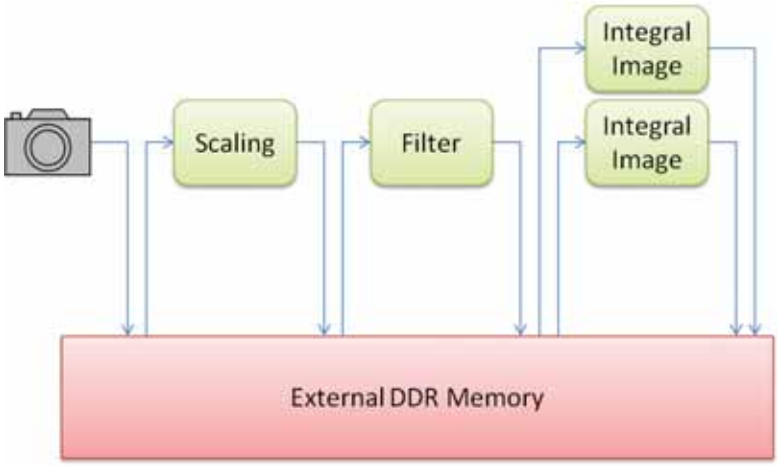



**Figure 10:** Processing graph with intermediate DRAM buffer

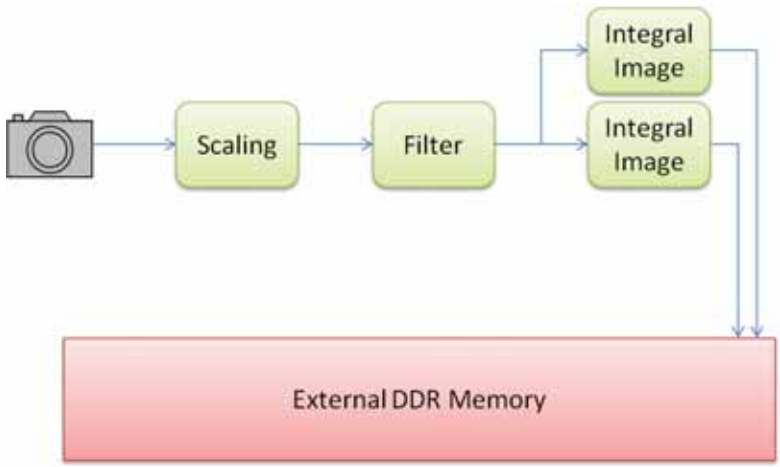



**Figure 11:** Optimized processing graph

Today there are several porting steps necessary that require significant development efforts. First step is to port from the basic algorithm development environment, which is typically a PC, to the embedded target. Most system suppliers use different embedded platforms in parallel, which often requires porting to another embedded architecture. As the software (especially in the first two processing stages) is very hardware-dependent to be able to fulfill the performance and power requirements, the porting efforts are very significant. The solution to ease transition and increase portability is to use a standard programming model for parallel processing and to provide tooling to abstract the specific architecture characteristics.

One area where this model is already successfully established is graphics, where software can be ported from the PC to various embedded platforms, even without modification. Each porting step requires a complete test and qualification, which contributes significantly to the total development cost. Increasing portability without the need for modification will have a huge effect on the development cost and time-to-market.

Freescale, therefore, plans to support the massively parallel compute industry standard OpenCL [2] in its next generation compute vision platforms. While OpenCL nicely abstracts the massively parallel compute platform, the challenge is to maintain the very good performance/power ratio of the ASIP while becoming compliant with a standard API.

Massively parallel compute standards like OpenCL up to now were not specified with embedded ADAS applications in mind. The preferred execution model as such is to use external memory buffers for intermediate results as illustrated in Figure 9.

The increased DRAM traffic of such an execution model is a serious problem for the embedded world, since the bandwidth limitation is the performance bottleneck and leads to significantly higher power consumption. To mitigate that situation might even be require extending existing standards to better support streaming processing of data on chip as illustrated in Figure 10.

Performing several processing steps without pushing the intermediate results out to external memory not only has the potential to save significant power but also makes the solution more cost-effective since it reduces the DRAM bandwidth required. The extensions considered would enable a graph-oriented processing with highly optimized data flow suited for the usual processing steps in compute vision.

Another positive effect of using a standard API common in the PC area is that it allows use of a standard PC with OpenCL-enabled graphic cards for development, meaning software development can start long before the target platform is actually available.

This set-up allows implementing and testing algorithms on a similar massively parallel system and re-factoring the algorithms for the new programming trend; but for performance estimation on the target platform, PC graphic cards provide only a limited insight. A higher integration, and a flexible and standardized programming model, are advantages that make it attractive for Tier 1 suppliers to port their vision software to the new architecture. Such a new architecture allows sustaining the huge software investment in ADAS, since it allows re-use in future ADAS solutions without fundamental rewrite, not only reducing the cost but also significantly reducing the time-to-market.●

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# SATISFYING THE EVOLVING REQUIREMENTS FOR MAINSTREAM FPGAs

Mainstream FPGAs and SoC FPGAs continue to drive to the largest number of designs in a wide variety of applications. However the definition of mainstream FPGAs continues to evolve and devices which were appropriate for mainstream applications yesterday fail to satisfy the needs of todays rapidly evolving applications. Todays mainstream FPGAs typically fall in the capacity range below 150K logic elements. This capacity range can implement sufficient custom functionality required of the majority of mainstream target applications without exceeding cost or power design constraints. When combined with the right selection of dedicated 'hard' logic mainstream devices can offer a more attractive combination of capacity, features, performance, low-power and lower total cost of ownership to address the bulk of programmable designs.

The dedicated functions that are most desired in todays mainstream applications include features like on-chip SRAM and Flash blocks; arithmetic functions for improving numeric computations like those for digital signal processing; high-speed serial interfaces and protocol specific logic; DDR memory controllers; and embedded Microcontroller Subsystems. The selection of the dedicated logic elements on a mainstream device can be a difficult balancing act. However, adding functionality not used by the majority of applications will increase the cost without sufficient advantages. Not putting in the right dedicated blocks means that most designs will use more programmable fabric, increasing cost and power requirements.

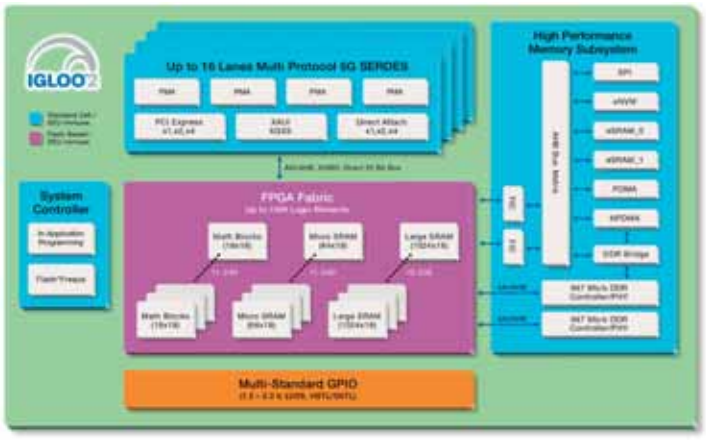
One solution to this dilemma is to develop multiple device families targeted for different applications requirements. If a common platform can be used for multiple families the FPGA manufacturer can leverage this infrastructure while more efficiently addressing multiple target markets. Microsemi's approach to the FPGA mainstream market illustrates this type of strategy with the IGLOO2 FPGA and SmartFusion2 SoC FPGA families. Both these device families leverage Microsemi's established on-chip Flash-based non-volatile FPGA fabric. This fabric uses an efficient four-input Look Up Table (LUT4) architecture with block/distributed RAM, DSP blocks and 5G SERDES and with up to 150K logic elements brings these devices into the mainstream application space. The selection of dedicated functions on the two families is different however and thus they target different application segments.

One of the most common mainstream FPGA application areas is for bridging multiple dissimilar interfaces. This is the modern 'glue logic' application for programmable devices and is probably the single most common type of design. Key requirements for a mainstream FPGA in these applications are a large number of high-speed serial ports and sufficient on-chip and off-chip memory bandwidth to keep up with the serial port requirements. Microsemi has architected IGLOO2 devices to target these types of applications by starting with the above described fabric and then adding 5G SERDES along with dedicated logic to support common protocols. A unique high-performance memory subsystem is also included that provides 64KB of on-chip SRAM, up to 512KB on-chip non-volatile Flash memory, and up to two high-speed LPDDR/DDR2/DDR3 memory controllers.

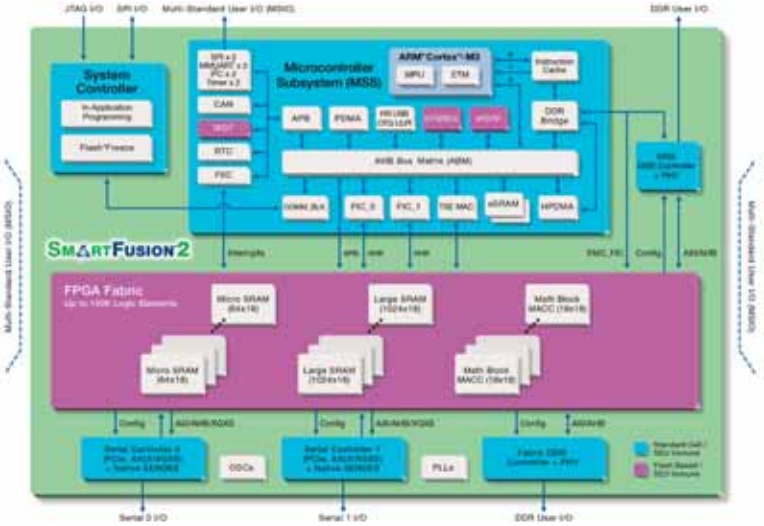
Another large segment of the mainstream market requires not only the data storage and movement capabilities previously describe, but also significant control and computation capabilities. In these applications data must also be operated on for tasks like packet inspection, audio or video processing, sensor measurement or a host of other operations. Complex decisions may need to be made that are more appropriate for an MCU to manage. A common approach, like that taken by Microsemi with SmartFusion2 is to add a full featured ARM Cortex-M3 based Microcontroller subsystem. The Microcontroller subsystem is an efficient method for implementing control functions and can also provide significant computational capability. FPGA fabric can even be used for hardware acceleration if additional data processing bandwidth is required.

FPGA families that build on a common architecture to address different applications segments using different dedicated blocks is the way forward. This strategy can be used to successfully satisfy competing mainstream FPGA requirements as they no doubt will evolve and change over the next several years.

**Example Mainstream FPGA-Microsemi's IGLOO2 FPGA**




**The Best In-Class Mainstream SoC FPGA-Microsemi's SmartFusion2 SoC FPGA**



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# BRUSHLESS DC MOTOR DRIVER DESIGN USING FPGA-BASED ARCHITECTURE IN EMBEDDED SYSTEM DESIGN

**HALIT OZTEKIN, EMRE OLMEZ** AND **FEYZULLAH TEMURTAS** FROM BOZOK UNIVERSITY IN TURKEY AND A. GULBAG SAKARYA UNIVERSITY IN TURKEY

PRESENT AN IMPLEMENTATION OF A BRUSHLESS DC MOTOR DRIVER DESIGN AND APPLICATION USING BZK.SAU.FPGA MICROCOMPUTER

Field Programmable Gate Arrays (FPGAs) play an important role in electronic system design. For academic purposes or small budget projects, FPGAs are an extremely convenient solution, especially because of their short programming times.

Brushless DC motors have high moment/current and high moment/inertia ratios. Robust construction, high efficiency and low maintenance increase the application reach of BLDC motors.

In this study, a brushless DC motor driver design and application were implemented using BZK.SAU.FPGA microcomputer. A standard parallel port interface was designed and added to the microcomputer architecture for controlling peripheral devices. The circuit supplying the necessary electrical power for the motor was designed with Mosfets in the form of a three-phase bridge. Motor control was implemented by a program code for the BZK.SAU.FPGA and, also as an alternative, by a hardware controller designed at logic level.

## Reduced Costs

Anand Sathyan et al designed a low-cost digital PWM controller to reduce the cost of BLDC motor applications; its simplicity allows it to be implemented as an ASIC; experimental verification of this controller is performed in an FPGA [1-2]. Whereas, Bogdan Alecsa and Alexandru Onea realized a BLDC motor speed control implementation with Xilinx's low-cost FPGA, called Spartan-3E [3].

Cheng-Tsung Lin et al implemented a sensorless, four-switch, three-phase BLDC motor control with an FPGA too. Control operation costs were reduced by decreasing the number of switches and removing the position sensor [4].

Another sensorless, four-switch BLDC motor control was implemented by M. Shanmugapriya and Prawin Angel Michael [5].

Ming-Fa Tsai et al modelled a BLDC motor and its driver using Matlab/Simulink and Modelsim. Control was implemented as the code generated in the simulation environment was downloaded into an FPGA [6].

In our study, educational-purpose BLDC motor driver was implementated using BZK.SAU.FPGA, an educational-purpose microcomputer, developed for supporting Computer Architecture & Organization and Operating Systems courses. It is modular in nature; see its block diagram in Figure 1.

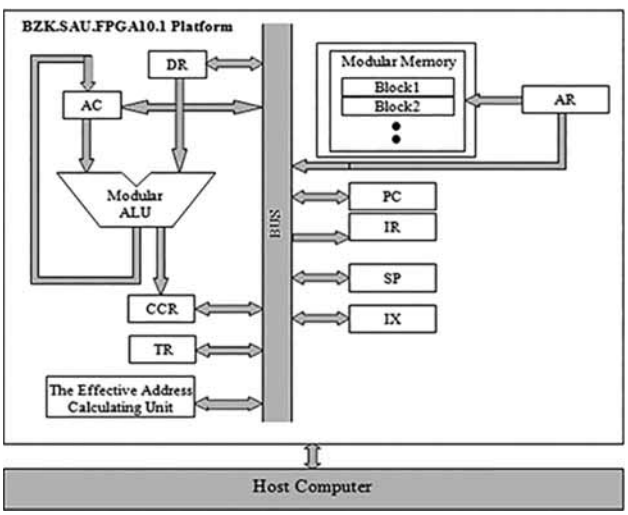


**Figure 1:** Block diagram of BZK.SAU.FPGA

A block diagram of our proposed design is shown in Figure 2. BLDC motor control was realized by energizing the required motor windings to produce maximum torque, according to the motor's 3-bit Hall sensor information. The circuit supplying the necessary electrical power for the motor was designed with Mosfets in the form of a three-phase bridge.

The microcomputer receives position information from the Hall sensor and sends trigger signals to the driver circuit, which then produces the required voltage for the motor. Communication between the microcomputer, Hall sensor and driver circuit was via the microcomputer's parallel port.

## BLDC Motor

Due to their higher efficiency and lower maintenance compared to conventional DC motors, brushless DC motors are becoming more widespread in the fields of industrial electronics, home appliances, automotive and robotics [3].

A brushless motor is constructed with a permanent magnet rotor and wire-wound stator poles. Electrical energy is converted into mechanical energy by the magnetic forces between the permanent magnet rotor and the rotating magnetic field induced in the wound stator poles [8]. A simplified form of a brushless DC motor is shown in Figure 3.

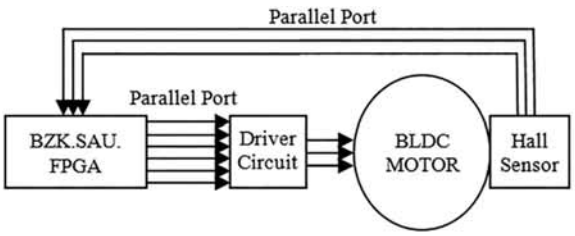


Figure 2: General structure of the controller

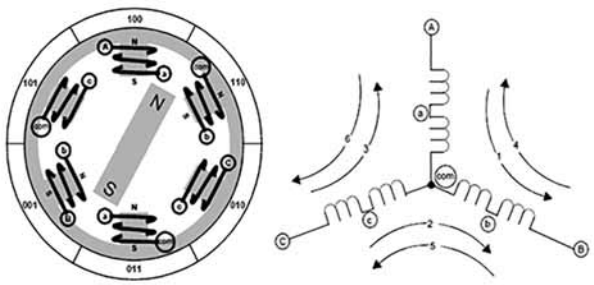

Figure 3: Simplified BLDC motor diagrams [8]

The BLDC motor commutation is energizing the motor windings to produce the maximum torque by sensing the rotor position. The easiest way to sense the rotor position is with a Hall sensor. Many BLDC motor manufacturers supply motors with a three-element Hall-effect position sensor. Figure 4 shows the relationship between the sensor outputs and the required motor drive voltages. A circuit in the form of a three-phase bridge applies high-level and low-level voltages to the motor terminals. The three-phase bridge circuit for our study was designed with N-channel and P-channel Mosfets.

## The Parallel Port Interface

In our project, the preferred method to control the BLDC motor was with data from the Hall sensor, which was then sent to the driver circuit through the parallel port interface – IEEE 1284: Parallel Ports standard [9]. A standard parallel port consists of data, status and control ports. The data port allows 8-bit read/write, the control port allows 4-bit read/write and the status port allows 5-bit read operations.

BZK.SAU.FPGA has two 8-bit registers for accessing peripheral devices. The input register is used to retrieve data from the peripheral units, and the output register to send data to the peripheral units. BZK.SAU.FPGA provides access to these registers with two commands: the IN command receives 8-bit data in the input register and writes it to the 16-bit accumulator's least significant 8 bits; and the OUT command receives the least significant 8 bits of the 16-bit accumulator and writes it to the output register. A block diagram of the designed interface is shown in Figure 5, whereas Table 1 describes the module's pins.

In order to read the data from the peripheral devices, the first operation is selecting the port with IN_S[1] and IN_S[0] pins. After that the INPORT input needs to be set to logic 1. Similarly, for sending data the OUT_S[1] and OUT_S[0] pins select the port and the OUTPORT pin enables the write operation.

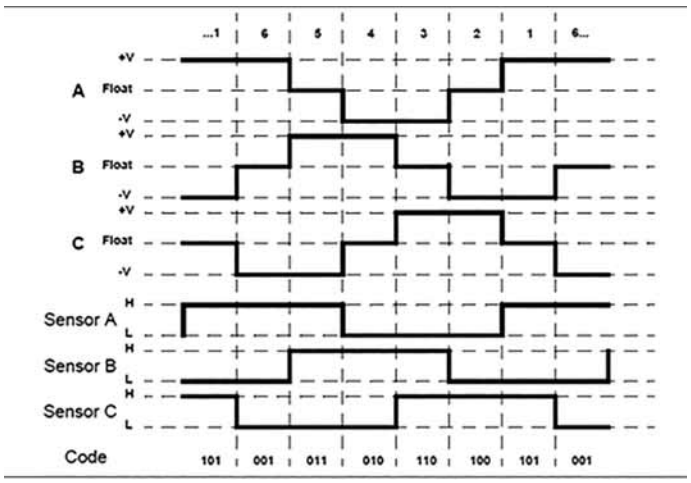


Figure 4: Sensor versus drive timing [8]

| PIN NAME | | TYPE DESCRIPTION |
|---|---|---|
| STATUS[7..0] | Input | Incoming Data from status port |
| OUT_REG[7..0] | Input | Incoming Data from output register |
| IN_S[1..0] | Input | Select port to read. "00" data, "01" status , "10" control port |
| OUT_S[1..0] | Input | Select port to write. "00" data port, "10" control port. |
| INPORT | Input | Enable port to read |
| OUTPORT | Input | Enable port to write |
| CONTROL[7..0] | In/Out | Incoming/Outgoing Data from/to control port |
| GPIO[7..0] | In/Out | Incoming/Outgoing Data from/to Data port |
| IN_REG[7..0] | Out | Outgoing Data to Input register |

Table 1: Pin description of the parallel port module

The designed parallel port module consists of eight 4x1 Muxes and eight 1x4 DeMuxes. In order to understand the operation of the module, the structure of 4x1 Mux and 1x4 DeMux should be well understood. In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and switches the selected input into a single line [10]. According to the S0 and S1 selection inputs, data will be transferred to the desired output channel. Conversely, a demultiplexer (or demux) is a device taking a single input signal and, selecting one of many data output lines, connects it to the single input [10].

In this design the multiplexers select the port to be read and

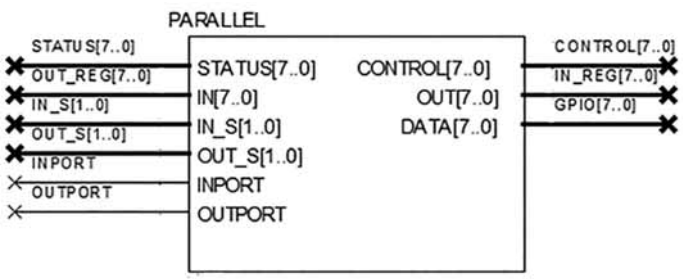


Figure 5: The parallel port module

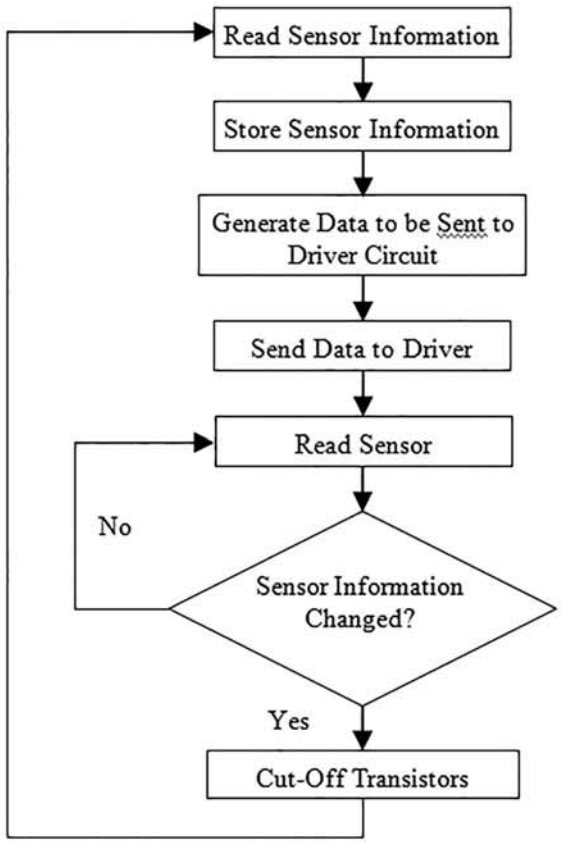


**Figure 6:** Flow chart of the BLDC motor control process

the demultiplexers the port to write into. Depending on the multiplexer's select pins, the data in the data port, status or control ports is transferred to the input register. Also, the data in the output register is routed to the data port or control port according to the multiplexer's select pins. So 8-bit data can be transferred by eight 4x1 multiplexers and eight 1x4 demultiplexers. The data and control ports are both input and output ports. To avoid conflict at these points, tri-state buffers are used.

During the input command, the buffers at the front of the multiplexers are active and the port is in input mode. During the output command, the buffers at the demultiplexers' output are active and the port is in output mode.

According to information from the Hall sensor, the control code generates data to be sent to the driver circuit. Before writing a program code, creating a flow chart of the process provides a much better understanding of the necessary steps to complete the work. Figure 6 shows the flow diagram of brushless DC motor control. BZK.SAU.FPGA's instruction set consists of 59 instructions, with seven of them being used in this program; descriptions of these commands are given in Table 2.

## Alternative Logic Level Controller

In this study, an alternative hardware controller was also designed at absolute logic level, instead of using a microcomputer. Block diagram of the designed logic controller is shown in Figure 7. The controller basically consists of three main parts: sensor detection logic, commutation logic and deadband generation logic.

The sensor detection logic continuously monitors the change in the Hall sensor data to detect the moment when the motor moves from one state to another.

The turn-off delay time of the transistors is longer than the turn-on delay time. Before driving the new group of transistors, we should ensure the current group is driven to cut off. The time it takes for this to transpire is called 'dead time'.

| INSTRUCTION NAME | DESCRIPTION |
|---|---|
| IN | Reads from parallel port |
| OUT | Sends data to parallel port |
| STA | Takes data from accumulator and writes it into specified address |
| LDA | Takes data from specified address and writes it into accumulator |
| CMP | Compares the data in the accumulator with the specified data |
| BZR | Performs branching according to the results CMP command |
| BRA | Performs unconditional branching |

**Table 2:** Instructions used in the program code

| START: | IN | READ PORT |
|---|---|---|
| | STA $FE00H | Store to address FE00H |
| | LDA $FE00H | Read from address FE00H |
| | CMP #XXXXH | If XXXXH=0005H then Label[X]←Label[1]<br>If XXXXH=0004H then Label[X]←Label [2]<br>If XXXXH=0006H then Label[X]←Label [3]<br>If XXXXH=0002H then Label[X]←Label [4]<br>If XXXXH=0003H then Label[X]←Label [5]<br>If XXXXH=0001H then Label[X]←Label [6] |
| | BZR Label[X] | |
| Label[X]: | LDA #YYYYH | If Label[X]=Label[1] then AC←25H<br>If Label[X]=Label[2] then AC←25H<br>If Label[X]=Label[3] then AC←25H<br>If Label[X]=Label[4] then AC←25H<br>If Label[X]=Label[5] then AC←25H<br>If Label[X]=Label[6] then AC←25H |
| | OUT | Send data to port |
| PRead: | IN | Read port |
| | CMP #FE00H | Compare with the data in the address FE00H |
| | BZR PRead | If equal Branch to "PRead" (Sensor data is not changed) |
| | LDA #0007H | Else Load accumulator 7H (Turn-off all transistors) |
| | OUT | Send to port |
| | BRA Start | Branch to "Start" Label |

**Table 3:** Program code

The sensor detection logic consists of D type flip-flops and a comparator circuit. The sensor data is transferred to the output of the flip-flops with each falling edge of the clock signal. The comparator circuit continuously compares the input and output of the flip-flops. If a change occurs, the output of the comparator falls down to logic 0 and triggers the deadband generator to compensate for the dead time.

The designed deadband generator is actually an 8-bit special counter. This counter counts from 0-7 and it remains constant when it reaches 7, until reset. When the output of the comparator in the sensor detection logic falls down to logic 0, the deadband generator is reset to 0 and counts up to 7 again. The elapsed time during this process is used as dead time.

The commutation logic generates the data for switching the transistors according to the data received from the sensor detection logic by considering the dead time.

## Comparisons

Because the BZK.SAU.FPGA is open source, modular structure designers are allowed to interfere with the architecture of a running computer. This way the motivation for designers to design original systems is increased. In our project, motor control was implemented by writing a program code for the BZK.SAU.FPGA microcomputer and, also, as an alternative, by a hardware controller designed at absolute logic level, providing an opportunity to compare these two methods in terms of ease of design, flexibility, running speed and so on. As a result, it was seen that the prepared design can be used for educational purposes and, moreover, it creates the basis for a microprocessor-controlled, industrial, brushless DC motor driver. ●

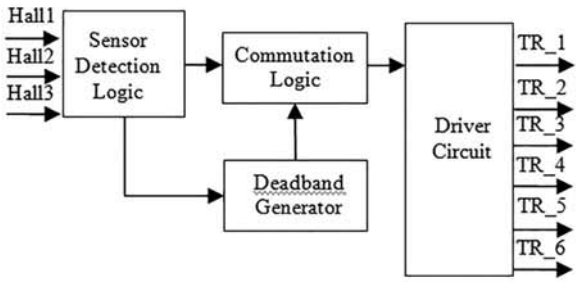


**Figure 7:** Block diagram of the logic controller

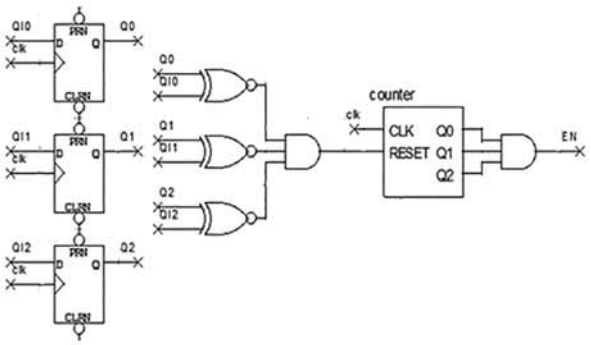


**Figure 8:** Sensor detection and deadband generator logic

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# EMBEDDED SYSTEM DESIGN

**MAURIZIO DI PAOLO EMILIO**, PHD AND TELECOMMUNICATIONS ENGINEER, OUTLINES THE FUNDAMENTALS OF EMBEDDED SYSTEM DESIGN

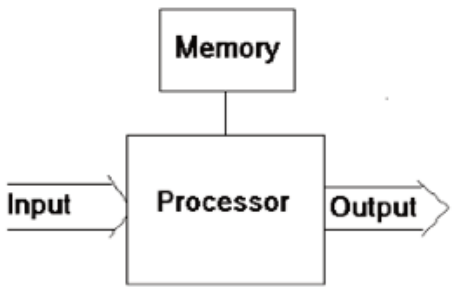


**Figure 1:** Generic block diagram of an embedded system

Computers are used to control a wide range of systems from simple domestic machines, through game controllers and even entire manufacturing plants. Their software must react to events generated by the hardware and, often, issue control signals in response to these events. The software in these systems is embedded in the system hardware, typically in the read-only memory, and usually responds in real time to events from the system's environment.

## Embedded Systems

An embedded system is a microprocessor-based system built to manage a function or a range of functions. It is closely integrated with the main system and may not interact directly with the environment. A typical embedded system would have:

- A microcontroller to provide the "intelligence";
- Interfacing circuits to connect with the main application;
- Real-time software;
- Dedicated hardware for functions whose implementation in software might be too slow;
- Test and maintenance hardware.

An embedded microcontroller runs a single program that never terminates. There is no (separate) operating system or monitor program – the operating system has to be merged with the application program. Most embedded microcontrollers have to respond in real time.

In practice, all embedded systems are resource-constrained. For example, an 8052-based system has only 256 bytes of RAM.

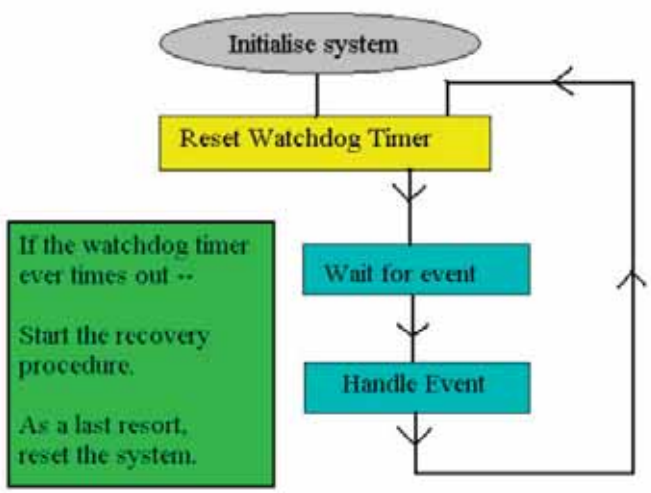


**Figure 2:** Watchdog timer

## Embedded System Design

The design of an embedded system normally consists of the following:

- Task partitioning between hardware and software;
- Hardware design and integration;
- Software development;
- System integration;
- Test strategies.

The design process for embedded systems has to consider – in detail – the design and performance of the system hardware. Part of the design process may involve deciding which system capabilities are to be implemented in software and which in hardware. Low-level decisions on hardware, support software and system timing must be considered early in the process. These may mean that additional software functionality, such as battery and power management, has to be included in the system.

Many tasks can be performed in hardware or in software, such as timing, for example. The choice between hardware and software is driven by considerations of speed, cost, need for flexibility in modifying underlying algorithms, and so on.

Also, hardware is considered to add a 'per unit' cost, whereas software a 'fixed' cost. Typically, only those functions whose speed specifications cannot be met by software solutions are implemented in hardware. Since a microcontroller in an embedded system runs just one program all the time, hardware resources must be matched to the needs of this particular application. Modern technology has made it possible to put the entire electronics, inclusive of sensors, analog circuits, digital circuits etc, on a single chip – System on a Chip or SoC. The degree of integration used will depend on the cost, need for small size, availability of components etc.

Software must provide the algorithms needed for

implementing the applications, and these algorithms often impact the choice of hardware as well, for example whether a DSP processor should be used or not. Most embedded system software need to operate in real time, and watchdog timers may also be needed (see Figures 1 and 2).

## Real-Time Systems

Real-time systems have to guarantee their response to an external event within a specified amount of time, but they don't have to be really fast, just reliably "on time". Soft real-time systems provide a time guarantee, but missing an event is not catastrophic. For example, image decoding in satellite TV reception must be completed within a "frame time".

Open source systems like Linux are becoming extremely popular. In paricular, real-time Linux provides the luxury of development on an advanced system and then migration to the target hardware.

A real-time operating system (RTOS) is an operating system (OS) intended to serve real-time application requests. It must be able to process data as it comes in, typically without buffering delays.

Real-time computing not only depends on the accuracy of the logical result but also on the result's delivery time. So the operating system should have features to support this critical requirement to render it to be termed an RTOS. The RTOS should have predictable behaviour in response to unpredictable external events. Real-time systems in which missing a deadline is catastrophic are called 'hard real-time systems'. Systems that allow deadlines to be missed at times and yet still recover them are called 'soft real-time systems'.

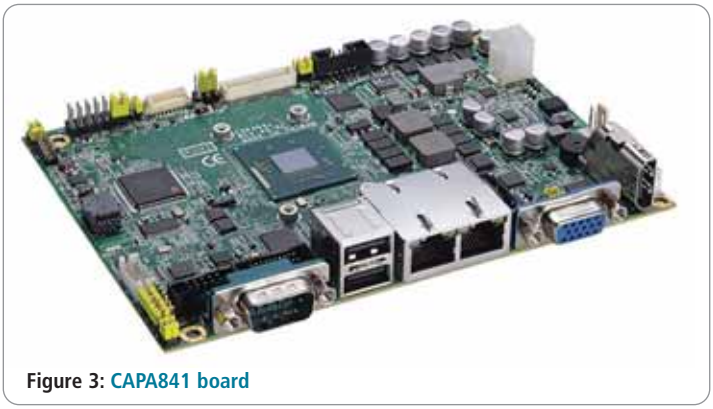

**Figure 3:** CAPA841 board

## Software Architecture

There are several different types of software architecture in common use:

- **Simple control loop:** where the software simply has a

loop. The loop calls subroutines, each of which manages a part of the hardware or software.

- **Interrupt-controlled system:** Some embedded systems are predominantly interrupt-controlled. This means that tasks performed by the system are triggered by different kinds of events. For example, an interrupt could be generated by a timer.
- **Pre-emptive multitasking or multi-threading:** In this type of system, a low-level piece of code switches between tasks or threads based on a timer (connected to an interrupt). This is the level at which the system is generally considered to have an "operating system" kernel.
- **Microkernels and exokernels:** A microkernel is a logical step up from RTOS. The usual arrangement is that the operating system kernel allocates memory and switches the CPU to different threads of execution.

## Power Management

Power management is critical in battery-powered applications. Differences of microamperes can translate into months or years of operating life, which can make or break a product in the marketplace. The single largest factor in power consumption of a microcontroller is the clock frequency, since the power consumed by a microprocessor is directly proportional to its operating speed, so it follows that a device operating at the lowest possible frequency will produce the maximum power savings. The speed chosen depends on the system requirements, most notably the interrupt service time. Temperature can also affect power consumption.

High-speed microcontrollers support four clock management modes: Stop, PMM1 (Power Management Mode 1), PMM2 (Power Management Mode 2) and Idle. They can dynamically switch between these modes, allowing the user to optimize the speed of the device while minimizing power consumption.

PMM1 and PMM2 allow the user to reduce power consumption without sacrificing performance. Although the power management features are an important part of a power-efficient design, a thorough understanding of the microprocessor will allow the system to achieve maximum power savings. The clock speed management modes are designed to be part of a progressive level of power reduction, based on external activity and performance needs. PMM1 and PMM2 provide the lowest level of power consumption whilst still permitting full computational and peripheral operation.

Numerous diverse and conflicting constraints burden the designer of small handheld products. Aside from the usual restrictions on size and weight, these constraints include cost limitations, strict time schedules, battery-life goals measured in weeks instead of hours, and host computers that are (sometimes) overtaxed with the demands of power management.

Because power requirements for handheld applications vary widely with product use, no single "best" power source exists for these applications. A device used intermittently is more concerned with no-load quiescent current than with full-load efficiency, and can operate satisfactorily with alkaline batteries. Mobile phones, however, must contend with high peak loads and frequent use. This mode of operation emphasizes conversion efficiency over quiescent current, so mobile phones are better served with a rechargeable battery.

## Bus Interface

The system bus connects several components of an electronic system, developed to reduce costs and improve modularity. The goal is based on management of a data bus and address bus to determine what and where to send the data; moreover, a control bus determines the operation.

Buses are designed in one of three ways:

- **Point-to-point connection**: a particular bus designed for every transfer.
- **Common bus**, used for all transfers.
- **Multiple bus**: a combination of the previous two methods.

The goal of the bus is to connect the CPU with the memory; it defines the main characteristics of the system. Many CPUs use a set of pins for communicating with memory, but are able to operate at different speeds with different protocols. Others use smart controllers to send the data directly in memory, known as Direct Memory Access (DMA). Most modern systems combine both solutions.

In modern systems, high-speed memory is built directly into the CPU (known as cache), and uses high-performance buses that operate at speeds much greater than memory. Such systems are architecturally similar to multicomputers.

## Future Embedded Systems

Embedded systems created ripples in the scientific world, bringing us closer to autonomous robots for personal use. Embedded systems can be considered as the primary technology of the future. In this market there are two major trends:

- The symbiotic relationship between embedded software vendors and original equipment manufacturers (OEMs).
- The growth and direction of the Embedded Operating System (EOS) market, and the challenges associated with the increasing complexity of embedded applications. ●

## EMBEDDED BOARDS

The 3.5" and 5.25" boards are the most compact form-factors for embedded single-board computers (SBCs). NEXCOM and Axiomtek, for example, offer the compact industrial-grade 3.5" and 5.25" boards with fanless design, low power consumption and rich I/O to support a wide range of demands in embedded applications.

The CAPA841 is equipped with the newest 22nm Intel Atom processor E3800 family, codenamed Bay Trail. This SoC incorporates up to four cores and supports system memory DDR3L-1066/1333 SO-DIMM maximum up to 8GB.

EBC 355 series of 3.5" boards is also based on the multi-core SoC Intel Atom processor E3800 family. The series operates at a wide temperature range with low power consumption, and features USB 3.0 ports and Intel Gen 7 graphics with multi-display support.

NEXCOM's EBC 355 3.5" boards support maximum memory of 8GB DDR3L SDRAM and offer four USB 3.0 ports along with three display outputs for VGA, HDMI and LVDS to provide the flexibility for a range of peripherals and dual displays. These boards provide reliable operation within an operating temperature range of -20degC to 60degC. The EBC 355 series is ideal for battery-powered portable devices, multimedia HMI panels, outdoor systems installed in harsh environments, home automation and thin clients among others.

# DISTRIBUTORS MUST PROVIDE SUITABLE DESIGN TOOLS

By Mark Burr-Lonnon, VP Europe and Asia, Mouser Electronics

Distributors are in the logistics game. We provide customers with an easy point of contact to source what they need and manufacturers with a channel to get their parts to market. Increasing, over a number of years, manufacturers have relied on distribution to service all but the very largest customers, leaving most customers little option but to rely solely on various different distributors, not only for the products themselves, but also support.

The statement above applies to most things – even food and everyday items. But it so happens that we specialise in the electronic components sector. While other sectors no doubt pose different challenges, electronic components require very careful design-in, and an increasingly-sophisticated range of soft and hardware development tools. So distributors are now required to broaden the range of services they offer.

Our model at Mouser Electronics, Inc. means that this approach is even more necessary. Mouser primarily services design engineers. Our goal is to enable design engineers to try out new semiconductor technologies which will differentiate their end equipment by delivering extra performance and increased functionality. Semiconductor vendors have vied with each other to support their microprocessors, microcontrollers, DSPs, FPGAs etc. This is because they know that if a designer can get to market simply and quickly without huge investment in expensive tools that will only work with one device family they stand a very good chance of securing the design slot. At Mouser, we understand that designers need the full technology 'ecosystem' – device itself, software development system, development board, design ideas and documentation – so that they literally 'have the tools to do their job'.

Amongst the many leading franchises this is necessary for are TI, Maxim, Analog Devices, Altera, Microchip, Freescale...the list goes on and on.

As well as offering hard and software tools from its partner suppliers, Mouser has created its own online tools to specifically suit the needs of design engineers looking to source the newest products and technologies, significantly simplifying and shortening the design cycle while ensuring that customers benefit from latest component advances. As well as providing detailed design information, the company has developed its unique BOM tool and added a Search Accelerator, speeding the complex process of building BOMs and ensuring that the most appropriate component choices are made.

Mouser's intelligent BOM tool at **www.mouser.com/bomtool** enables users to set preferences and maintain their own formatting, and is the first to feature built-in Part Resolution Intelligence, enabling users to quickly find parts without full part numbers. BOMs can be uploaded to the tool as a simple parts list or in the customer's original Excel format. www.mouser.com/bomtool is the only online BOM tool that can quote up to five columns of customer specified quantities; it is also the only online tool that can include competitor part numbers in the part search and can auto-select columns based on customer header information. It is able to search for alternative parts and provide detailed parts' status information – price, stock, leadtime, RoHS compliance. BOMs can be saved for future reference.

Mouser's new Search Accelerator at **www.mouser.com/accelerator** turns any web browser into a parts finder by enabling the user to search for any part number or keyword from any website then check availability on www.mouser.com without leaving the current page. This significantly speeds up the process of finding new parts. More, the Search Accelerator can now be used with the near-ubiquitous Microsoft® Office platform enabling component information to be obtained from popular software programs. Simply highlight any part number or keyword in an Outlook email message or Excel spreadsheet and click 'Search Mouser' to instantly preview search results and product details.

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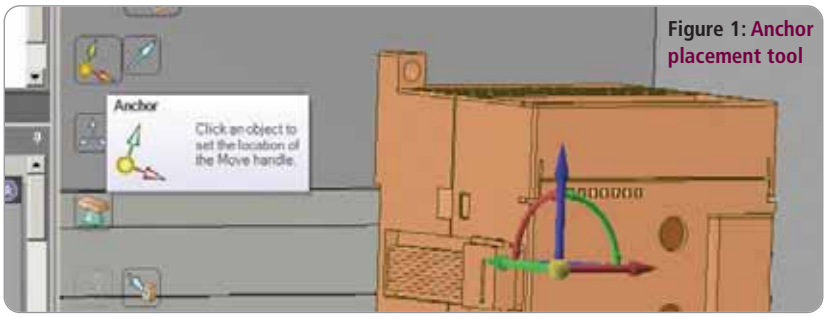



Figure 1: Anchor placement tool

# BRAVE NEW WORLD IN 3D SOLID MODELLING

**DAVID PIKE**, APPLICATIONS ENGINEER AT RS COMPONENTS, DISCUSSES 3D DESIGN AND SOME OF THE BASIC DIFFERENCES BETWEEN FEATURE-BASED MODELLING AND DIRECT MODELLING, AND HOW THE NEW 3D MODELLING TOOL DESIGNSPARK MECHANICAL MIGHT OFFER NEW POSSIBILITIES

The market for advanced software to create models for designs and products in 3D really came into existence in the 1980s. Historically, feature-based or history-based 3D CAD tools have dominated the market. In the early days it was not inevitable that the methodology would prevail, but its success has largely been attributed to the limits of processing power delivered by computers of the time.

Due to the lack of number-crunching performance, feature-based modelling held the advantage over alternative methodologies such as direct modelling. Essentially, it was based on a clever trick to make solid modelling viable on hardware of the 1980s.

Feature-based modelling broke down the design into a list of individual parameter-driven steps or features, which acted as instructions to create the shape of the part and enabled the hardware to create and work with models in something like real time, or at least near it.

Certainly the process worked well enough for designs comprising simple parts and assemblies, but as computers delivered increasing performance, the models became more complex and additional concepts were developed to link the features together. These included constraints and parent-child relationships, which basically describe the relationship between the individual features or steps, held in the tool's 'history tree'. However, it meant that if a specific feature needed to be changed, then it was necessary to retrace the steps right back to the definition of that particular feature.

Feature-based modelling also required the creation of interfile dependencies and, eventually, the development of data-management tools to enable concurrent working of design teams.

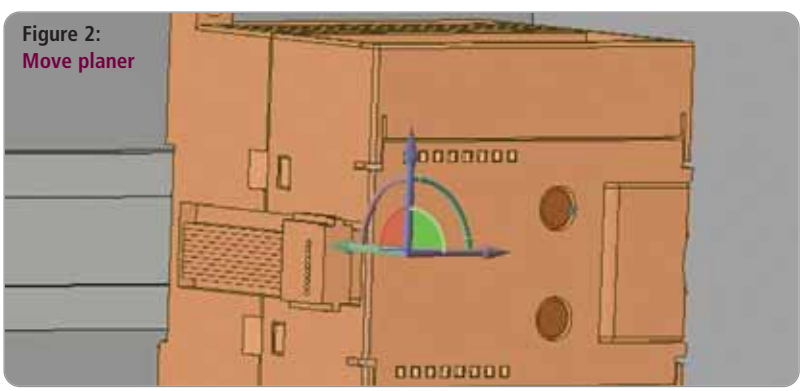


Figure 2: Move planer

## Barriers to Entry

Equally, whilst the 3D software was powerful (but generally expensive), only the experts in CAD could use it. It is estimated that approximately 20 million users around the world, including electronics and mechanical engineers, would benefit from using 3D design, yet there only around one million active 3D CAD licenses in total across the major CAD software vendors. Many who could have benefitted from 3D design have not been given access to this mysterious and impenetrable knowledge, most likely for reasons of cost, both in terms of tool price and also the time it takes to become skilled and fully productive with the tools. Both of these factors have become major barriers to entry for users looking to reap the benefits of 3D design.

The latest tools from leading CAD vendors are in the range of $5,000 to $30,000 per license, and usually come with high-priced annual maintenance fees. As mentioned earlier, the second impediment is the significant learning curve sometimes associated with traditional 3D modelling. Entry-level users may take anywhere between 6 and 18 months before they become

fully productive with an advanced 3D tool. Often, this leads to CAD designs being outsourced to a CAD specialist company, which may introduce bottlenecks in product development with the processing of even simple changes in the design taking many weeks.

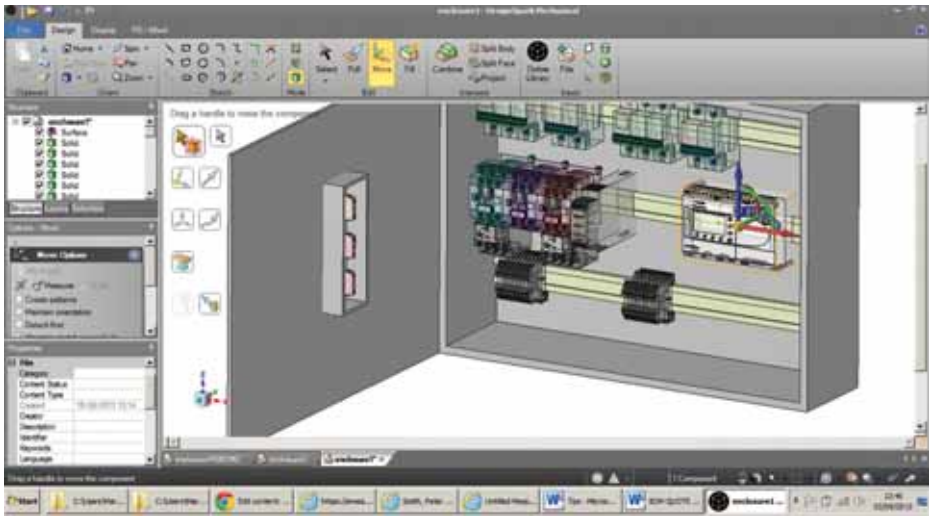


Figure 3: Capture or an enclosure

## Direct Modelling

Today computers are around 100,000 times more powerful than their venerable ancestors of the 1980s. And because of this, direct modelling – which allows a user to draw 3D shapes as easily as they might draw with pen and paper – is making a serious claim as an alternative or, in many cases, a complementary 3D design tool.

Direct modelling offers a large advantage to non-CAD specialists in that it is generally more intuitive and very easy to learn. Essentially, it is all about geometry; there is no feature history and no need to manage any of the associated complexity such as constraints or parent-child relationships. It works at the base geometry level and dynamically changes any requested modifications into geometry to explore ideas and product concepts in 3D. In many respects it is very similar to SketchUp, where a user can push and pull on geometry and make new designs extremely quickly.

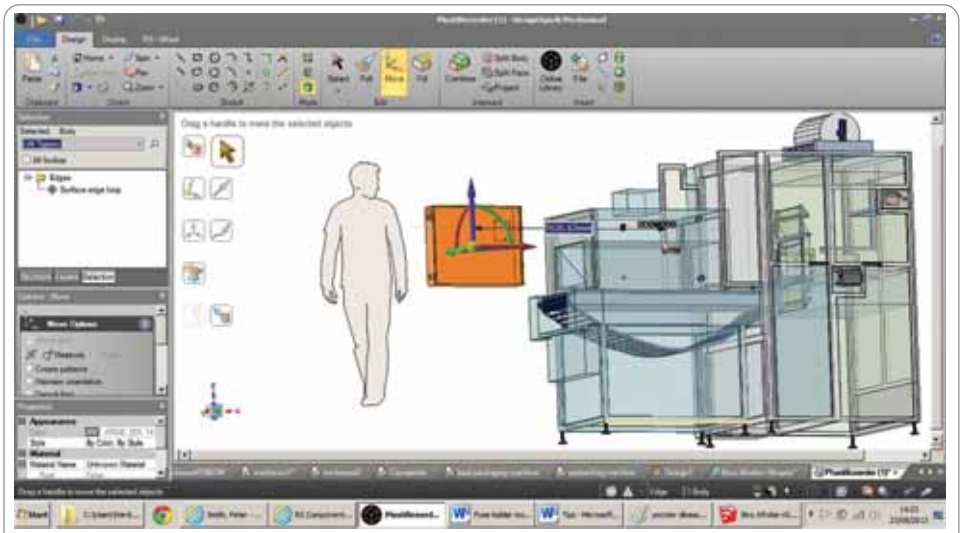


Figure 4: Plasticiser with panel being attached and ergonome

Direct modelling eliminates many of the problems associated with traditional feature-based tools, as engineers who may not use CAD on a regular basis easily can make changes to models without having to fully understand all the 'constraints' of a feature-based model. For example, with direct modelling the engineer can make iterations to the design directly from the last one, adding and removing from the design without any snags.

> It is estimated that approximately 20 million users around the world, including electronics and mechanical engineers, would benefit from using 3D design

However, it is also very true that some applications will still require feature-based modelling if, for example, it is the end goal to create customized variants of an extremely complex assembly of parts with critical and well-understood relationships and requirements. However, this approach can be inefficient for significantly smaller designs; direct modelling is quicker and easier for a growing number of applications.

## Direct Modelling Advanages

Another advantage offered by direct modelling is greater interoperability, whereas proprietary feature-based systems have incompatible data formats. Historically, competing 3D CAD vendors have had very different ideas about the operation of features and relationships within their respective tools. This meant the creation of proprietary software packages that were not compatibile, leading to interoperability problems becoming a significant challenge for CAD users and the supply chain. In the past, this has meant that everyone in the supply chain had to use the same tools, as there is always some loss of information when translating data from one CAD format to another. Employing advanced direct modelling tools such as SpaceClaim Engineer, for example, users in simulation or manufacturing departments can simply edit the actual CAD geometry via STEP files, the most common intermediate data translation format for CAD systems.

Another important advantage of direct modelling is that it allows very quick iteration on concepts, whereas traditional CAD can often be a cumbersome approach, when conceptualizing new ideas in response to RFQs (request for quotation) for example.

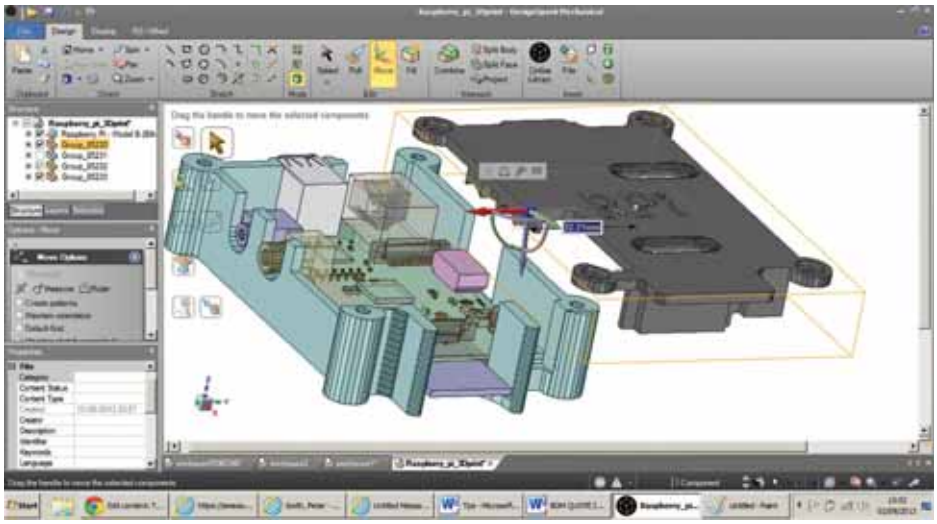


Figure 5: Raspberry Pi closer

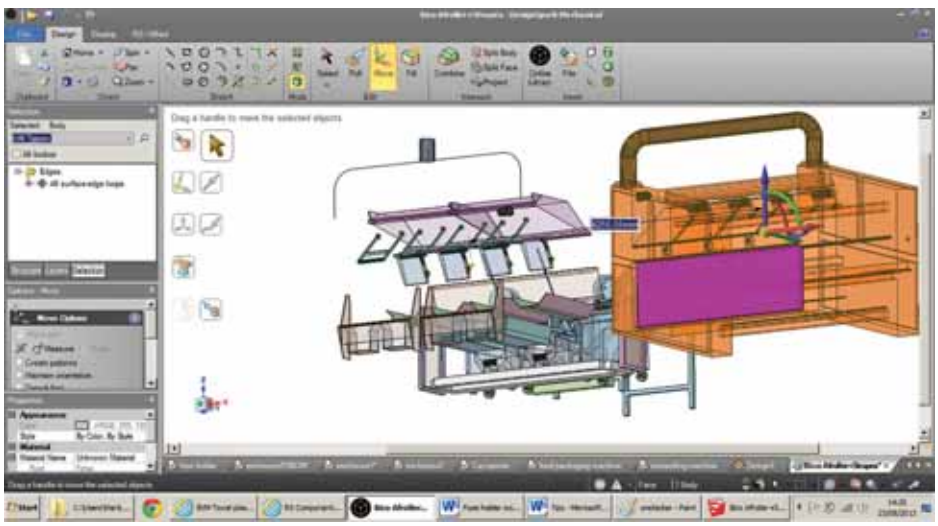


Figure 6: An uncoiler is assembled

## DesignSpark Mechanical

While there is no doubt that traditional feature- or history-based CAD tools have a continuing and important role to play in the development of electronics and mechanical design, direct modelling is making a substantial case for use in product development, especially in concept design and prototype manufacturing, but also in other areas.

RS and Allied have recognised this important trend and launched the DesignSpark Mechanical 3D solid modelling and assembly tool. Developed in conjunction with SpaceClaim and primarily based on the company's direct modelling SpaceClaim Engineer 3D design tool, DesignSpark Mechanical is available for download, free of charge.

DesignSpark Mechanical offers major benefits to industrial designers and electronics design engineers among many others, such as sales, marketing and production, who can now easily contribute and collaborate at the early stages of product development. As it is intuitive and easy to use, anyone can become fully conversant with the software within days or even hours. Basic designs can be achieved quickly via software's four basic tools: Pull, Move, Fill and Combine and, unlike traditional feature-based tools, the software makes use of familiar 'copy and paste' keyboard shortcuts, allowing exceptionally easy reuse of geometry in different designs.

DesignSpark Mechanical exports 3D designs in the STL file format to enable rapid prototyping builds and computer-aided manufacturing, in addition to providing the ability to quickly obtain Bill-of-Materials (BOM) quotes via the RS and Allied websites. The tool can also import circuit layout files in IDF format from any PCB design tool, including the award-winning DesignSpark PCB software from the two companies.

## 3D Models

However, it is not just the choice of 3D design tool that is important. An absolutely crucial piece in the jigsaw for the electronics or electromechanical engineer is a product or component model library. Some three years ago, RS and Allied provided engineers with access to an extensive library of 2D and 3D models downloadable free of charge as part of its initiative with DesignSpark, building up a community of developers to share open-source designs and ideas.

The ModelSource component library contains over 80,000 component schematics and PCB footprints of semiconductors, passives and electromechanical components from leading manufacturers. ModelSource also offers over 38,000 3D models from over 55 manufacturers, covering key technologies including electronics, electromechanical, mechanical, pneumatics and automation and control.

The 3D CAD models are also available in many proprietary file formats from leading CAD vendors. Key manufacturers represented in the 3D element of the library include Molex, 3M, TE Connectivity, Harting and FCI in the general electronics market, and Siemens, Schneider and SMC in the automation and control applications. ●

## MORE INFORMATION

**DesignSpark Mechanical is available for free download via the RS, Allied and DesignSpark websites. Support for the tool is also available via the DesignSpark community at www.designspark.com, which also hosts resources for DesignSpark PCB and the ModelSource library.**

# EMC Concepts

**IAN DARNEY** PRESENTS THIS NEW SERIES OF ARTICLES ON CIRCUIT MODELLING FOR ELECTROMAGNETIC COMPATIBILITY

This series of articles will demonstrate that electromagnetic compatibility (EMC) is as amenable to the design process as any other design requirement. Key to the approach is the use of circuit models to simulate and analyse all the interference-coupling mechanisms. Such an approach results in a dramatic simplification of the mathematics.

This instalment introduces the underlying concepts, with future articles covering lumped-parameter models, transmission lines and antennae, bench testing, transients and design guidelines.

## Simplifying Assumptions

The mechanisms involved in the coupling of interference are governed by the laws of physics, defined by the formulae of electromagnetic theory. These laws also control the functional behaviour of electronic systems, analysed by the much simpler mathematics of circuit theory.

Given these facts, it is reasonable to describe circuit theory as a development and simplification of electromagnetic theory. However, the simplifications inherent in the present-day usage of circuit theory that make it capable of analysing the behaviour of extremely complex electronic systems also render it ineffective in any analysis of interference coupling.

The keyword in the previous sentence is 'usage'. If the simplifying assumptions can be identified and modified, then circuit theory can also be used to analyse interference.

The most significant of these assumptions is the concept of the 'equipotential ground', which manifests itself in the use of the ubiquitous 'earth' or 'ground' symbols found scattered around present-day circuit diagrams. It is assumed that every point identified by such a symbol is held firmly at zero voltage. The simulation tool SPICE, for example, has become totally dependent on this concept.

Another assumption is that the conducting link between two nodes on a circuit diagram has zero impedance.

> *A basic assumption when using circuit theory is that action and reaction are instantaneous throughout the system. They are not!*

## The Signal Link

If it is recognised that every conductor in a system possesses the properties of inductance, capacitance and resistance, then it follows that transient current in any conductor will create a voltage along that conductor. A voltage will exist between any two points designated as being at ground potential. The effect of this can be minimised by assigning a 'return' conductor to return the current delivered by the 'sending' conductor back to the voltage source.

There will be two paths between sender and receiver for the return current, as illustrated by Figure 1. Coupling between the signal loop and the ground loop is inevitable, no matter how the terminations are configured.

A circuit model which simulates the coupling of interference between these two loops is illustrated by Figure 2.

**Figure 1:** Basic signal link

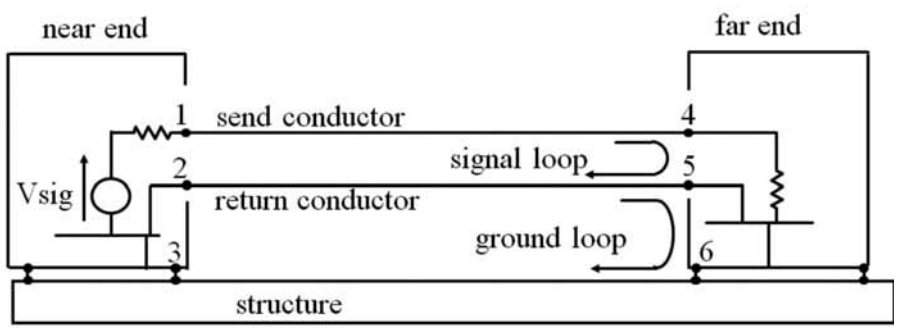
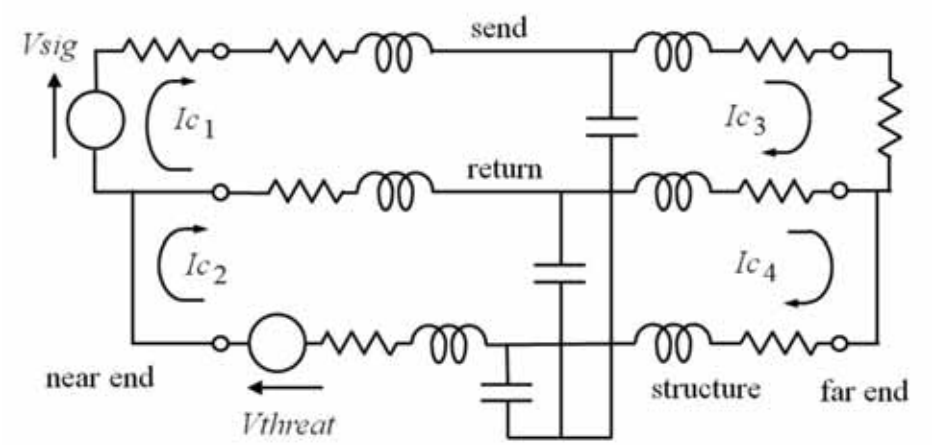


**Figure 2: Circuit model of signal link**




Each conductor is represented by a T-network of inductors, resistors and a single capacitor. The task of assigning numerical values to the L, C and R components of the model will be dealt with in my article on lumped parameters, later in the series.

If the only path available for the return current between the two units of equipment is the structure, or the 'earth' conductors of the power supplies, then there is no point in trying to analyse EMC.

## The Circuit Diagram As A Model

Before the advent of the desk computer, one method of predicting the behaviour of the servo system of a rocket launcher was to relate the currents and voltages generated by an analogue computer to the mechanical properties of the system under review. A simple illustration of this relationship is provided by Figure 3.

A simple damping system is shown in Figure 3a. If an extra mass is dropped on the weight, then the system will oscillate.

Figure 3: Use of a circuit model to simulate a mechanical system: (a) Damping system; (b) Circuit model

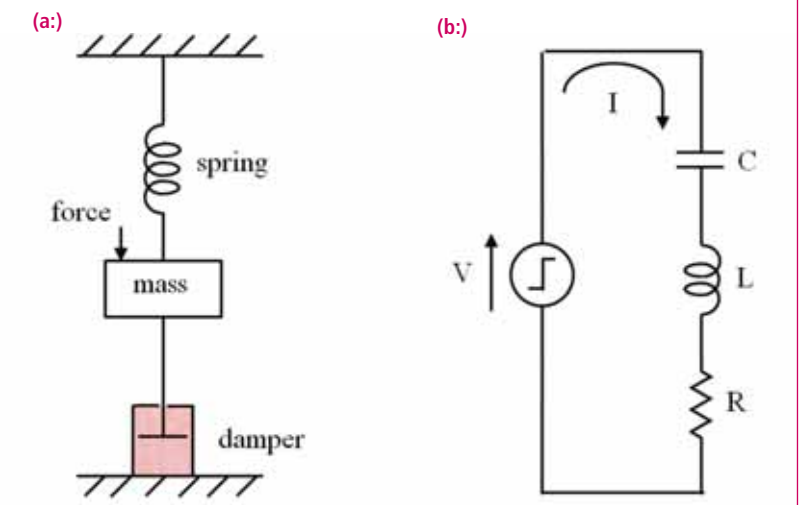



Figure 4: Distributed-parameter model of signal link conductors

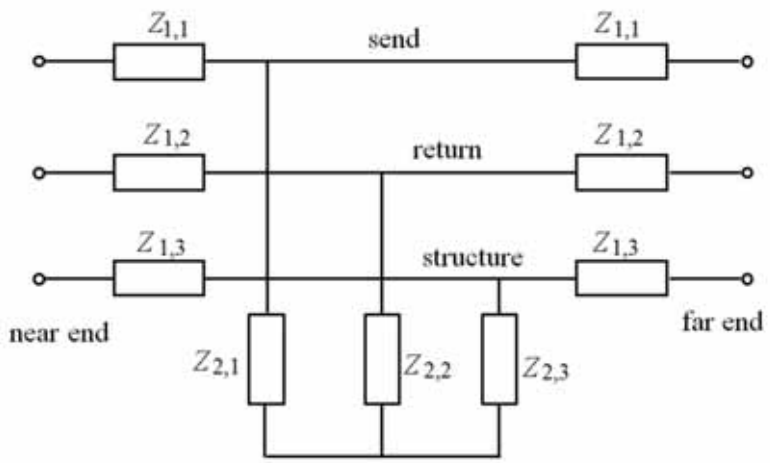
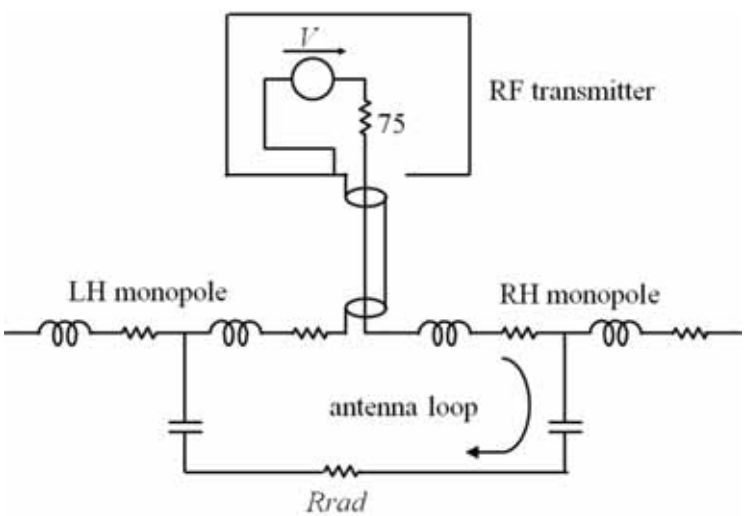



Figure 5: Lumped-parameter model of dipole antenna




The equation of motion is essentially the same as that of the LCR circuit of Figure 3b, where the parameters of force, displacement, velocity, mass and damping factor are replaced by voltage, charge, current, inductance and resistance.

The circuit model can be regarded as a pictorial representation of a set of equations. In concept, this is the same as treating it as the unknown variable in mathematical problems.

## Developing the Model

A basic assumption when using circuit theory is that action and reaction are instantaneous throughout the system. They are not! The velocity of propagation of current and voltage is finite. Transmission line theory allows for this by deriving a pair of hybrid equations that relate current and voltage at the sending end to current and voltage at the receiving end of the line. This derivation can be developed further to define a pair of loop equations that can be manipulated using the rules of circuit theory.

The lumped-parameter model of Figure 2 can be replaced by the distributed-parameter model of Figure 4. These two figures are so named because the first assumes that inductance, capacitance and resistance are discrete components, whilst the second allows for the fact that these three parameters are distributed along the length of the cable. The transformation formulae are discussed in the article on transmission lines and antennae later in the series.

## The Radiation Resistor

The theory of the dipole antenna identifies the concept of the radiation resistance. This parameter is probably new to circuit designers, but is well understood by students of electromagnetic theory. It is not a component in the sense that it can be purchased from a supplier. It is a mathematical constant derived from the analysis of the power density of the electromagnetic field over a spherical surface enclosing a transmitting antenna. When a dipole is providing maximum radiated power output, the load presented to the transmitter is purely resistive. This leads to the resistance *Rrad* in the model of Figure 5.

The reactive components act as a series tuned circuit. At resonance the only components limiting the current delivered to the environment are the resistors. Although the model is defined in terms of lumped parameters, it is analysed in terms of distributed parameters.

## The Virtual Conductor

Since the model of Figure 5 represents each monopole as a T-network, it is a simple step in the reasoning to speculate that if a twin-conductor cable was to replace one of the monopoles, with the structure acting as the other, the result would be the model shown in Figure 6.

Since the assembly of components representing the environment of each monopole is shown as a T-network and since every conductor of the signal link is also configured as a T-network, it is natural to identify this assembly as a virtual conductor. Again, the lumped parameters are changed into distributed parameters during the analysis.

For susceptibility analysis, the threat voltage *Vthreat* can be calculated by relating it to the electric field of the threat environment.

To analyse emission, it is assumed that the threat voltage is zero. A voltage source *Vsig* at the near end of the signal link will generate a current *Irad* in the antenna loop. The maximum field strength H at a radius r due to *Irad* can then be calculated.

## Bench Testing

Having established a method of modelling any signal link, the way is open for correlation to be established between the performance of the actual hardware and the simulation provided by the model.

Figure 7 illustrates a bench test setup that can be used to measure susceptibility. The clamp-on transformer injects a common-mode voltage into the cable; channel 1 of the oscilloscope monitors this voltage. Simultaneously, channel 2 monitors the effect of this voltage on the function of EUT1.

Figure 8 illustrates a setup used to measure conducted emission. In this test, the voltage delivered to the sending end of the signal link is derived from the signal generator and monitored by channel 1; channel 2 monitors the amplitude of the common-mode current.

In both tests, the designer can monitor the input and output simultaneously. With formal testing, engineers at the test house do not have that option.

The ability to carry out bench tests and create a circuit model of the interference coupling parameters means it is possible to predict the outcome of formal EMC testing and implement corrective measures before submitting the manufactured equipment to the test house. ●

**Figure 6:** General circuit model of exposed cable and structure

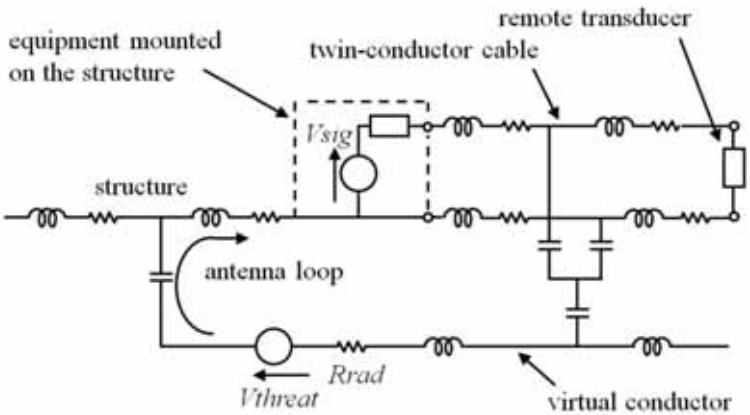



**Figure 7:** Bench test of conducted susceptibility

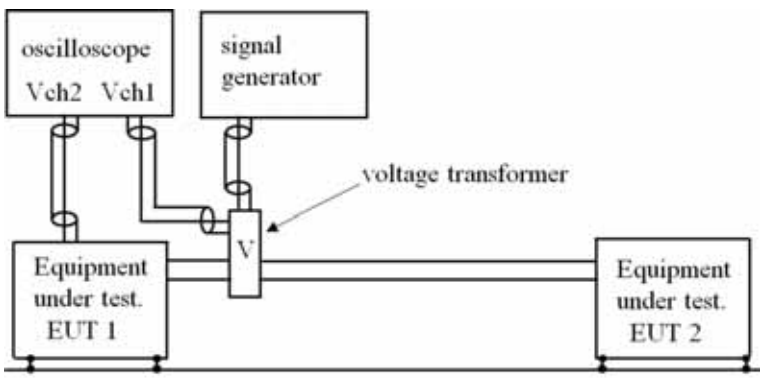
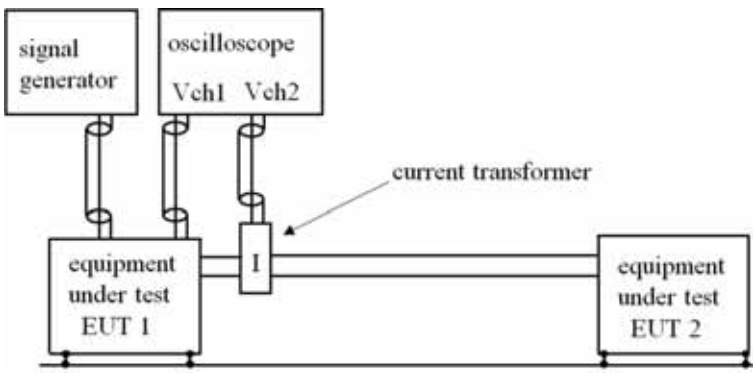



**Figure 8:** Bench test of conducted emission




**WIN A BOOK!**

Ian Darney's *'Circuit Modeling for Electromagnetic Compatibility'* book was recently published by SciTech, an imprint of the IET. A summary of its contents can be found at **www.designemc.info**.

We have a copy of it to give away, so to be in with a chance, please write to the Editor at svetlanaj@sjpbusinessmedia.com, providing your name, and postal and email addresses.

The winner will be drawn at random after the series ends later in the *year*.

# Microelectronics: Differential Amplifiers

**MAURIZIO DI PAOLO EMILIO**, PHD IN PHYSICS AND A TELECOMMUNICATIONS ENGINEER, PRESENTS THIS SERIES OF ARTICLES ON THE FUNDAMENTALS OF MICROELECTRONICS

Microelectronics has changed our lives, with mobile phones, digital cameras, laptop computers and other devices becoming an integral part. In this series I will analyze the principal circuits that are at the heart of many electronic systems and offer a practical and theoretical approach to some of them.

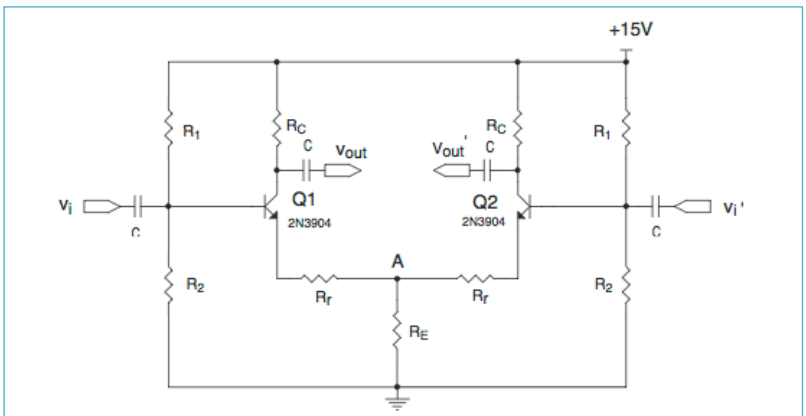



**Figure 1:** Schematic of a differential amplifier

## Differential Amplifiers

The main part of analog integrated circuit (IC) design is the differential pair or differential amplifier configuration, introduced to eliminate all or part of the problems of amplifiers with direct coupling. The goal is to create amplifiers characterized by an acceptable signal-to-noise ratio (SNR), even in the presence of external/internal disturbances generated by thermal variations due to the aging of electronics components.

One example of this design is the input stage of an op-amp and its emitter-coupled logic (ECL). This technology was invented in 1940s for use in vacuum tubes; the basic differential-amplifier configuration was later implemented with discrete bipolar transistors. However, the configuration became most useful with the invention of the modern transistor/MOS technologies.

## Main Features

The main features of differential amplifiers are:

1) High input resistance, so small voltage signals can be amplified without losses;
2) Temperature drift is minimal;
3) Two input terminals, for inverting and non-inverting inputs.
4) It amplifies the difference between two input signals.

The differential amplifier works only on dual power supplies, requiring both +Vcc and -Vcc voltages simultaneously. However, the same circuit connected to a single power supply becomes unstable and the circuit does not amplify properly.

The differential amplifier (Figure 1) provides a number of advantages, making it one of the most useful circuit configurations, particularly as an input stage in high gain and DC amplifiers. A differential amplifier is a special-purpose amplifier designed to measure differential signals, also known as subtractor.

In the figure the CMRR (common-mode rejection ratio) can be calculated with the following equation:

$$A_d = \frac{R_c}{2(R_r + r_{tr})} \; ; \; A_c = \frac{R_c}{2R_E + R_r + r_{tr}} \; ; \; CMRR = \frac{2R_E + R_r + r_{tr}}{2(R_r + r_{tr})}$$

where $r_{tr}$ is the transresistance, usually indicated also as $r_e$.

The 741 (a common op-amp chip) has a CMRR of 90dB, which is reasonable in most cases. A value of 70dB may be

Figure 2: CMRR vs frequency in the Analog Devices AMP03 amplifier

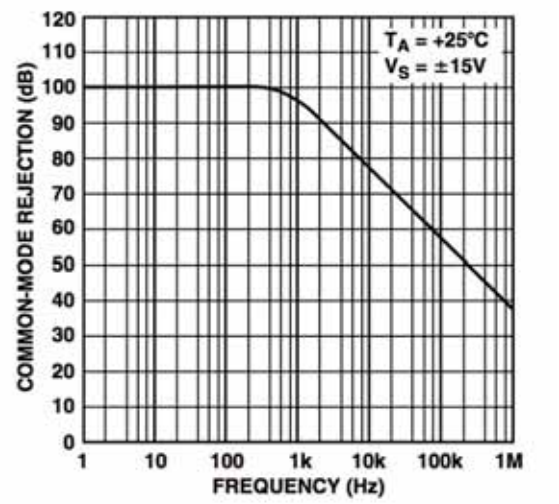



Figure 3: Differential and single-ended amplifiers

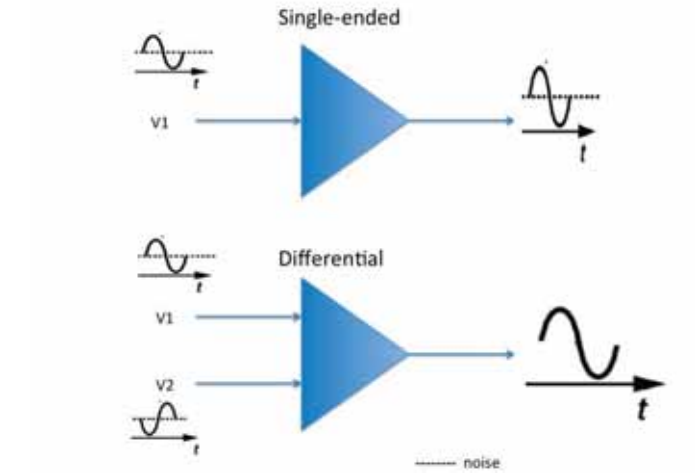
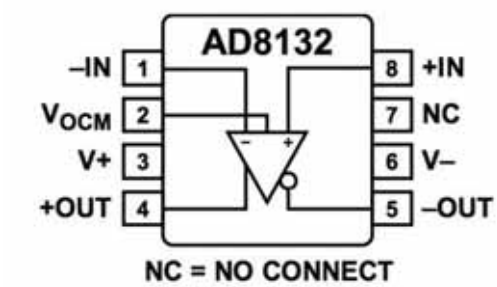



Figure 4: Analog Devices AD8132




adequate for applications insensitive to the effects on amplifier output; some high-end devices may use op-amps with a CMRR of 120dB or more. CMRR relates to the ability of the op-amp to reject a common-mode input voltage. This is very important because common-mode signals are frequently encountered in op-amp applications (Figure 2).

## Differential Amplifier Applications

Differential signals (Figure 3) are made up of pairs of balanced signals around a reference point. In this way differential amplifiers are less susceptible to noise and interference.

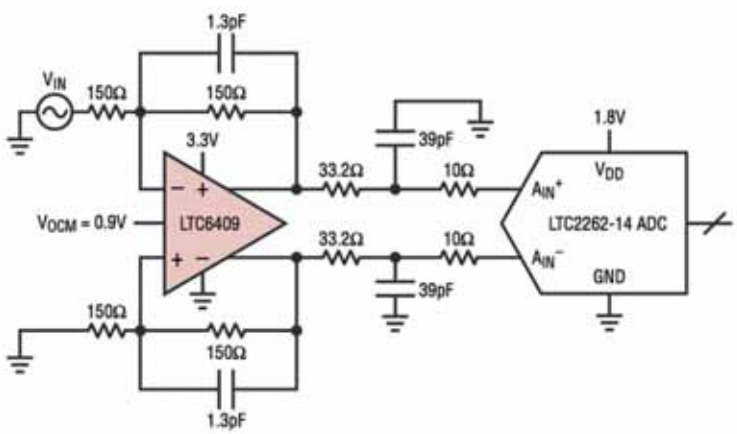
Common application of differential amplifiers is in the control of motors or servos, as well as in signal amplification. In discrete electronics, a common arrangement for implementing a differential amplifier is the long-tailed pair, typically found as a differential element in most op-amp integrated circuits. A long-tailed pair can be used as an analog multiplier with a differential voltage as one input and biasing current as another.

There are many differential amplifier ICs on the market today. The AD8132 (Figure 4) from Analog Devices (ADI) is a low-cost differential (or single-ended) amplifier with one resistor for setting the gain. The AD8132 is a major improvement on op-amps, especially for driving differential input ADCs or signals over long lines.

The AD8132 can be used for differential signal processing (gain and filtering) throughout a signal chain, significantly simplifying the conversion between differential- and single-ended components.

Linear Technology provides many other differential amplifiers for different applications. For example, its LTC6409 (Figure 5) offers very high speed and low distortion, and is stable in a differential gain of 1. It is available in 3mm × 2mm 10-pin leadless QFN package and operates in the temperature range of -40°C to 125°C. ●

Figure 5: Example of an application using Linear Technology's LTC6409 (from datasheet)



**THIS SERIES PRESENTS SOME SIMPLE ARDUINO PROJECTS. ARDUINO IS AN OPEN-SOURCE ELECTRONICS PROTOTYPING PLATFORM, BASED ON FLEXIBLE, EASY-TO-USE HARDWARE AND SOFTWARE**

# How to Measure Distance

BY **JOHN NUSSEY**

Two sensors for measuring distance with the Arduino are extremely popular: the infrared proximity sensor and the ultrasonic range finder. They work in similar ways and achieve pretty much the same thing, but it's important to pick the right sensor for the environment you're in.

An infrared proximity sensor has a light source and a sensor. The light source bounces infrared light off objects and back to the sensor, and the time it takes the light to return is measured to indicate how far away an object is.

An ultrasonic range finder fires high-frequency sound waves and listens for the echo when they hit a solid surface. By measuring the time it takes a signal to bounce back, the ultrasonic range finder can determine the distance travelled.

Infrared proximity sensors are not as accurate and have a much shorter range than ultrasonic range finders.

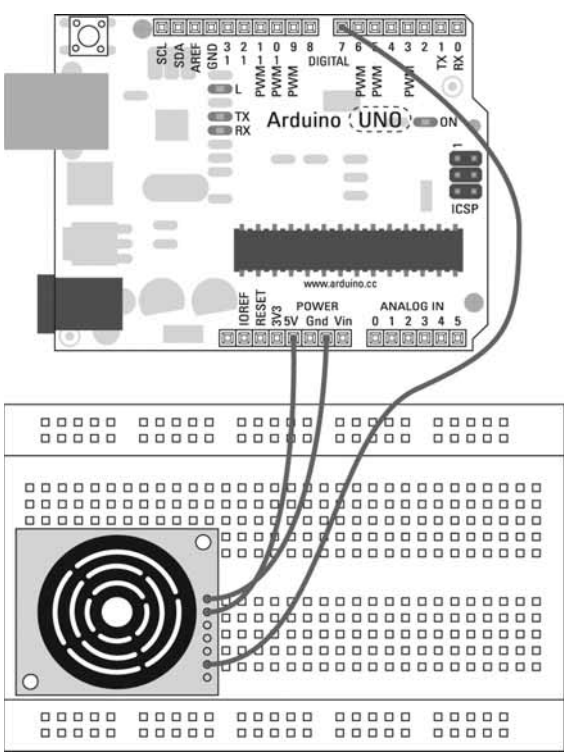



**Figure 1:** An LV-EZ0 circuit layout

Consider the following during planning:

- **Complexity**: Both of these sensors are designed to be extremely easy to integrate with Arduino projects. In the real world, they're used for similar electronics applications, such as proximity meters on the back of cars that beep as they approach a curb. Their main complexity, however, is housing them effectively. Infrared proximity sensors such as those made by Shape have useful screw-holes on the outside of the sensor's body. MaxBotix makes ultrasonic range finders that do not have these mounts, but their cylindrical shape makes them simple to mount on a surface by drilling a hole through.
- **Cost:** Infrared proximity sensors cost about $15 (£10) and have a range of up to 59 inches. Ultrasonic range finders have a far greater detection range and accuracy, and cost between $27 (£18) for a sensor that reads up to 254 inches (645cm) and $100 (£65) for a more weather-resistant model that reads up to 301 inches (765cm).
- **Where:** A common application for these sensors is monitoring presence of a person or an object in a particular area, especially when a pressure pad would be too obvious or easy to avoid, or when a PIR sensor would measure too widely. Using a proximity sensor lets you know when someone is in a straight line from that sensor, making it a very useful tool.

When using ultrasonic range finders, you can also choose how wide or narrow a beam you want. A large, teardrop-shaped capture-area sensor is perfect for detecting large objects moving in a general direction, whereas narrow beams are great for precision measurement.

IR proximity sensors are fine for dark environments but perform terribly in direct sunlight.

## Implementing The MaxSonar Sketch

In this example, the emphasis is on learning how to measure precise distances using a MaxBotix LV-EZ0. The EZ0, EZ1, EZ2, EZ3 and EZ4 all work in the same way, but each has a slightly narrower beam, so choose the appropriate one for your project.

The range finder needs some minor assembly. To use it in your circuit, you need to either solder it on header pins for use on a breadboard, or lengths of wire.

There are three ways to connect this range finder: by using analog, pulse-width or serial communication. We have chosen the pulse-width communication for this example, explaining how to

take a measurement and convert it to distance. The analog output can be read straight into the analog input pins but provides less accurate results than pulse width. This example does not cover serial communication.

The list of components for the project includes:

- An Arduino Uno;
- An LV-EZo Ultrasonic Range Finder;
- Jumper wires.

Complete the circuit from the layout and circuit diagrams. The connections for the range finder are clearly marked on the underside of the PCB. The 5V and GND connections provide power for the sensor and should be connected to the 5V and GND supplies on your Arduino (see Figure 1).

The PW connection is the pulse-width signal that will be read by pin 7 on Arduino. Make sure the distance sensor is affixed to some sort of base pointed in the direction you want to measure (see Figure 2).

## MaxSonar Code

You can find the MaxSonar code by Bruce Allen in the Arduino playground, along with some additional notes and functions. Create a new sketch, copy or type the code into it, and save it with a memorable name, such as myMaxSonar for example.

```
//Feel free to use this code.
//Please be respectful by acknowledging the author in the code if you use or modify it.
//Author: Bruce Allen
//Date: 23/07/09
//Digital pin 7 for reading in the pulse width from the MaxSonar device.
//This variable is a constant because the pin will not change throughout execution of this code.
const int pwPin = 7;
//variables needed to store values
long pulse, inches, cm;
void setup() {
 //This opens up a serial connection to shoot the results back to the PC console
 Serial.begin(9600);
}
void loop() {
 pinMode(pwPin, INPUT);
 //Used to read in the pulse that is being sent by the MaxSonar device.
 //Pulse Width representation with a scale factor of 147 us per Inch.
 pulse = pulseIn(pwPin, HIGH);
 //147uS per inch
 inches = pulse/147;
 //change inches to centimetres
 cm = inches * 2.54;
 Serial.print(inches);
 Serial.print("in, ");
 Serial.print(cm);
 Serial.print("cm");
 Serial.println();
 delay(500);
}
```

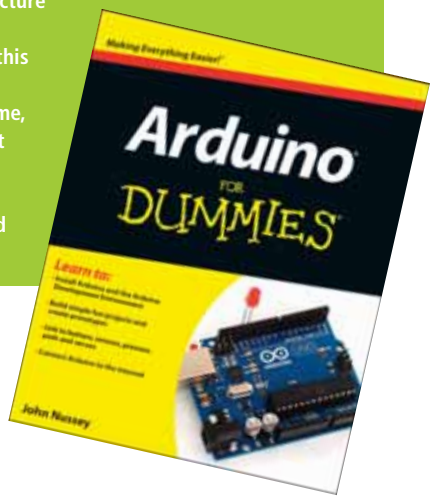
## WIN THE 'ARDUINO FOR DUMMIES' BOOK BY JOHN NUSSEY

John Nussey is a creative technologist based in London. He advocates the Arduino prototyping platform and teaches interaction design and prototyping at the Goldsmiths College and the Bartlett School of Architecture among others.

We have a couple of copies of this book to give away.

To enter please supply your name, address and email to the Editor at svetlanaj@sjpbusinessmedia.com

The winner will be drawn at random and announced at the end of the series.




Press the Compile button to check your code. The compiler highlights any grammatical errors, turning them red when they are discovered. If the sketch compiles correctly, click Upload to send the sketch to your board. When it completes the uploading, open the serial monitor and you should see the distance measured in inches and centimeters. If the value is fluctuating, try using an object with a bigger surface.

This sketch allows you to accurately measure distance in a straight line. Test this with a tape measure and make adjustments to the code if you find discrepancies. ●

*More on this and other Arduino projects can be found in the 'Arduino For Dummies' book by John Nussey.*

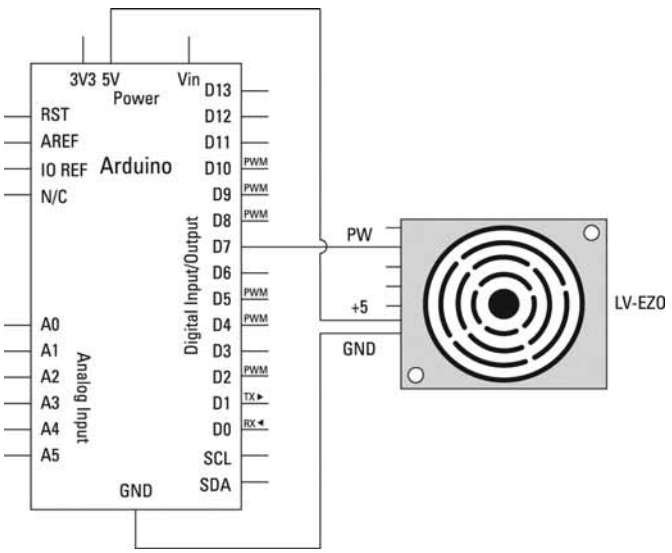



**Figure 2:** An LV-EZO circuit diagram

# Embedded World 2014

## 25-27 February
## Nürnberg, Germany

**Embedded World And Electronic Displays 2014**

From 25-27 February, two of the world's best-known events on embedded systems will take place in Nürnberg, Germany, as part of the embedded world Exhibition & Conference: Embedded World And Electronic Displays. The embedded community will be able to meet and network over three days at these events and hear the latest information in the conference sessions.

The embedded world event is expected to grow again this year. "The [embedded] industry has a remarkable dynamic. Based on the present level, we will be able to greet 15% new exhibitors in 2014," said Alexander Mattausch, Exhibition Director of embedded world. "The event is the top worldwide platform for the industry to exchange ideas and source information at a high level – the two conferences with their groundbreaking themes make a valuable contribution."

**Embedded World Conference 2014**

The embedded world conference runs in parallel with the exhibition and offers many presentations and an extensive programme of practical workshops. The conference committee of top experts has assessed many of the papers submitted and assembled a first-class conference programme intended primarily for embedded hardware and software developers.

This year, the conference will focus on the three areas: smart systems, smart software and smart connections. In addition, each day there will be ten parallel sessions and workshops covering these themes.

Part of the smart connections focus will be various wireless communication technologies, and in particular RFID and M2M. In the smart software sessions focus will fall on embedded Linux design methods, but also model-based software development in general, software design in high-level languages, simulation, verification and debugging, RTOS, Android, Java and more.

The system concept at the conference goes beyond just hardware. Modern multicore modules will be a major topic at the conference, also addressing questions such as ultra-low energy consumption, FPGA-based system design and building secure systems, including firewall systems that cannot be hacked into or attacked. Embedded security is more important than ever nowadays, and the conference organizers have devoted a lot of time to this subject.

More information about the embedded world conference 2014 programme and registration are available at www.embedded-world.eu.

**Electronic Displays Conference 2014**

Alongside the electronic displays exhibition will be the electronic displays conference with highlights including latest display trends, technologies and applications, and future markets. The programme includes practical lectures on HMI, touchscreens, interfaces, automotive displays, 3D systems and display measurement, among other subjects.

"The programme for the electronics display conference has grown continuously for years. This year we will be able to offer even more top-class presentations by international experts. I am delighted about this as it impressively shows the great importance of the conference for the industry," says Professor Karlheinz Blankenbach, Pforzheim University of Applied Sciences, Chairman of the Conference Committee.

As with previous years, there is a special highlight for students: the "German Flat Display Forum (DFF) Award" will be presented to the best bachelor or master's thesis on the topic of electronic displays.

More information about the electronic displays conference 2014 programme and registration can be found at **www.electronic-displays.de.**

**Information And Free Online Registration**

The latest lists of exhibitors and products, floor plans, detailed conference programmes, travel tips and lots more information on embedded world 2014 are available at **www.embedded-world.de.**

## Swissbit at embedded world
### Hall 1, Stand 520

Swissbit AG will be presenting its S-40 and S-40u series of SD and MICRO SD memory cards with autonomous data maintenance that require no intervention by host or application. This enables the memory cards to offer much longer data retention than conventional SD or MICRO SD cards.

Another highlight at the show will be the recently launched X-55 series. Compared to standard MLC SSDs, Swissbit's EM-MLC 2.5" SATA SSD drives achieve endurance values up to ten times higher while maintaining consistent data retention, in line with the JEDEC standard. The sophisticated diagnosis and monitoring features as well as deletion technology such as Secure Erase make the X-55 series ideal for cost-sensitive industrial applications that nevertheless have tough requirements.


Swissbit's portfolio encompasses industrial DRAM and flash memory solutions in all commonly used technologies and form factors. The DRAM modules are produced as chip-on-board and SMT versions and are available as SDRAM, DDR, DDR2 and DDR3.

**www.swissbit.com**

## IQD at embedded world
### Hall 4, Stand 650

Portable instrumentation equipment and communications systems (fixed and mobile) frequently require a high stability oscillator but don't have either the physical space for or power to drive an Oven Controlled Crystal Oscillator (OCXO). IQD's latest TCXO launching at embedded world 2014 provides a practical alternative and is designed specifically for such applications.

Housed in an industry standard 7 x 5mm ceramic package, the new IQXT-200 series offers a class leading frequency stability down to ±0.28ppm across a wide frequency range from 1.25MHz up to 200MHz. Operating over the standard industrial temperature range from -40 to 85 degrees C, users can select variants to operate off a 3.0V, 3.3V or 5.0V power supply with the current drawn being typically less than 15mA. A wide range of outputs can be specified including LVTTL, HCMOS, Clipped Sine Wave or Sine Wave into 50-Ohms.

**www.iqdfrequencyproducts.com**



## Cadence at embedded world
### Hall 4, Stand 116

At embedded world 2014, Cadence Design Systems will demonstrate the latest solutions for developing infotainment systems, early software, and integration and verification of embedded systems. The company will present and demonstrate solutions from analogue/mixed-signal simulation to complex system configuration and hardware/software co-development.

Visitors to the Cadence booth can learn about the latest enhancements to the Cadence System Development Suite, whose four connected platforms enable concurrent hardware/software design and verification to accelerate system integration, validation and bring-up.

In addition, there will be system-verification demonstrations on the subjects of Palladium XP II, virtual system platforms, rapid prototyping platforms, mixed-signal verification and implementation using the encounter platforms, automotive Ethernet design IP, and PCB and IC package design and analysis using the Allegro platform.

**www.cadence.com**

## Toshiba at embedded world
### Hall 4, Stand 548

At Embedded World 2014, Toshiba Electronics Europe (TEE) will be showcasing technologies from across its wide range of standard and custom semiconductor solutions. Among the featured demonstrations is a "Digital Kiosk" that combines TransferJet, NFC and Qi wireless charging technology to show an example use case in which rich digital content, including HD video, can be purchased and downloaded swiftly to mobile devices, such as smartphones. Other sections of the stand will highlight solutions that help to accelerate application development in areas including automotive, industrial, multimedia, telecoms, smart communities, networking, home appliances and consumer devices.

Toshiba's Digital Kiosk is a fully finished concept system that shows how various emerging wireless technologies can function together to deliver new services. The single formed plastic unit comprises an LCD screen with platter for smartphone charging or wireless connection, and status LEDs. To operate, the user taps a kiosk app icon on a smartphone, previews and then buys the available video content.

**www.toshiba-components.com**


## Mouser Electronics at embedded world
### Hall 4A, Stand 300

Mouser Electronics has entered into an agreement with Axiomtek to supply their extensive offering of Single Board Computers, industrial motherboards and embedded systems. As a leading member of the Intel Intelligent Systems Alliance (ISA), Axiomtek is focused on bringing intelligent systems and solutions to embedded systems engineers worldwide. Axiomtek delivers a reliable and flexible family of embedded computing products and platforms, and is devoted to producing state of the art solutions for a broad industrial customer base.

To find out more visit uk.mouser.com/axiomtek.

Mouser Electronics will be at embedded world 2014 in Hall 4A, Stand 300.

**www.mouser.com**

## congatec at embedded world
### Hall 1, Stand 358

congatec AG announces the immediate availability of the conga-QA3 Qseven module based on the Intel Atom processor E3845. All modules are fitted with ceramic capacitors making them ideal for industrial mobile applications in harsh environments. New features include an ample L2 cache, which can be shared by multiple cores, and a much faster Intel HD graphics unit compared with the previous generation, turning new applications into visual experiences.

The modules support Intel Advanced Encryption Standard New Instructions (Intel AES-NI) set, which is more relevant than ever in practical application. This allows developers to offload particularly compute-intensive packaging and encryption routines of the well-known cryptographic algorithm AES (Advanced Encryption Standard) into hardware, thereby enabling high performance encryption without putting a significant burden on the CPU cores.

The conga-QA3 comes in five different Intel Atom processor-based versions (formerly codenamed "Bay Trail") for high scalability.

**www.congatec.com**

# Omron Long Life Anti-Tamper Switch for Smart Meters, Safety And Security Systems

Omron Electronic Components Europe has launched a new sub miniature switch for tamper detection in smart meters, security and safety equipment and other systems.

The new Omron D2FS ultra sub miniature switch has been specifically engineered to activate reliably even after exceptionally long periods of non-use, making it ideal for the detection of attempted sabotage. According to Omron, anti-tamper systems may not be actuated for ten or more years, but should still operate reliably if the system is attacked after this period. These mechanisms are essential to preserve the integrity of the system, preventing meter fraud, unauthorised override of safety systems and compromise of security systems.

Omron developed the D2FS as a switch solution specifically for this type of application, requiring very high reliability with a low switching frequency. In creating the D2FS, Omron's switch designers used a highly innovative construction, with just a single-leaf movable spring to realize the component at a reasonable cost. The D2FS range includes versions with pin plunger and hinge lever actuation, with self-clinching, straight, right-angled or left-angled PCB terminals.

Omron Electronic Components Europe is a supplier of electromechanical PCB relays and other components such as micro switches, MOSFET relays, DIP switches, photomicrosensors and connectors. Omron has a strong portfolio of innovative technologies including MEMS sensors for pressure, flow and thermal measurement applications, as well as vibration and tilt sensors.

Omron Electronic Components Europe has eight regional offices strongly supports its customers in Western and Eastern Europe, Russia and the CIS, and a network of local offices and partnerships with specialist, local regional and global distributors.

Omron Electronic Components Europe is a subsidiary of the Omron Corporation, manufacturer of high-quality, high-technology electrical and electronic control equipment and components.

**http://components.omron.eu**

## YOKOGAWA LAUNCHES THE WORLD'S FIRST PRECISION POWER SCOPE

Yokogawa has combined its world-leading expertise in power measurement and its long heritage in oscilloscope design to create the world's first Precision Power Scope: the PX8000.

The PX8000 brings oscilloscope-style time-based measurement to the world of power measurement. It can capture voltage and current waveforms precisely, opening up applications and solutions for a huge variety of emerging power measurement problems.

The new instrument has 12-bit resolution with 100MS/s sampling and 20MHz bandwidth. This means that the PX8000 can be used for accurate measurement of inverter pulse shapes, which can then be used to fine-tune inverter efficiency. A choice of input modules covers voltage, current and sensor measurements at voltages up to 1000V RMS and currents up to 5A RMS (higher values are possible with external current sensors), with basic accuracy down to ±0.1%.

To evaluate three-phase electrical systems, at least three power measurement inputs are required and yet the PX8000 has four.

**www.tmi.yokogawa.com/px8000**

## ELECTRONICS COMPONENT MANUFACTURER REAPS BENEFIT OF PRODUCTION MANAGEMENT SOFTWARE

A successful company in the design and manufacture of fibre optic assemblies had traditionally relied on manual manufacturing management and administration procedures to check and track bills of materials, quotations, stock, work in progress, deliveries and invoicing. Like many electronic component manufacturers, the company had a number of different product platforms and a vast number of configurable assemblies, including many customised versions. This customisation had led to even more complex production procedures and the company recognised the need to find a solution for the associated administration of orders.

Datatrack was selected as the most appropriate and proven system and once configured to work with the company's manufacturing principles, all production procedures, particularly the creation of bills of materials and assemblies, are now being managed automatically by Datatrack.

Datatrack's system is used widely in the electronics industry including in sub-contract engineering, where batch production suppliers can face similar administration problems.

**www.psldatatrack.com**

## Unipolar Hall-Effect Switch Offers Unique Self-Diagnostic Capability

The new A1160 from Allegro MicroSystems Europe is a unipolar Hall-effect switch with built-in diagnostic capabilities that provide a unique solution to the monitoring of device performance and the self-diagnosis of incorrect device operation.

The new device is the only Hall sensor IC capable of verifying proper electrical performance and magnetic sensing: a critical feature for safety applications that must adhere to Automotive Safety Integrity Level standards or for those applications requiring two sensors for redundancy.


The key to the self-diagnostic capability of the A1160 is an integrated coil surrounding the Hall sensing element. During normal operation, the A1160 functions as a typical unipolar switch (with the output turning on in the presence of a south-pole magnetic field and turning off when the field is removed), but when the diagnostics pin is pulled high it enters the diagnostics mode.

This patented feature allows current to pass through the integrated coils, generating magnetic field.

**www.allegromicro.com**

## AVX Offers The Lowest Profile 0603 And 0805 MLO Diplexers

AVX Corporation offers the lowest profile 0603 and 0805 multilayer organic (MLO) diplexers available in the global market. Compared to equivalent low-temperature co-fired ceramic (LTCC) products, AVX's 0603 and 0805 MLO diplexers exhibit superior attenuation, low insertion losses, low parasitics, high heat dissipation and excellent solderability. Ideally suited for band switching in dual and multiband systems, such as WiFi and WiMax (WLAN/BT); mobile telecommuni-cations, including 3G and 4G LTE (WCDMA, CDMA and GSM); and GPS, the 0603 and 0805 MLO diplexers measure a scant 0.42mm (0.017") and 0.55mm (0.021") in height, respectively.

Based on AVX's patented multilayer organic high density interconnect technology, the 0603 and 0805 MLO diplexers employ high dielectric constant and low loss materials to realize high Q passive printed elements, such as inductors and capacitors in multilayer stack-ups. Expansion-matched to PCBs, the devices also provide improved reliability compared to ceramic and silicon components.

**www.avx.com**

## GECKO CONNECTORS WILL BE USED IN THE QB50 NETWORK OF MINIATURE CUBESAT SATELLITES

Harwin, a hi-rel connector and SMT board hardware manufacturer, announced that its Gecko family of high-performance connectors will be used on CubeSat miniature satellites being designed by Surrey Space Centre as part of the international QB50 programme led by the von Karman Institute, Belgium.

The QB50 program will study in situ the temporal and spatial variations of a number of parameters in the lower thermosphere using a network of around 40 double CubeSats Carrying identical sensors. QB50 will also study the re-entry process by measuring and comparing actual trajectories and orbital lifetimes during re-entry against predicted data. A third part of the programme will see about 10 double or triple CubeSats used for In-Orbit Demonstration (IOD) of technologies including miniature sensors and the Gossamer-1 solar sail.

Harwin's low profile Gecko connectors are designed to offer high performance in a miniature package with 1.25mm pin spacing.

**www.harwin.co.uk**

## FIRST DEMONSTRATION OF QUALCOMM QUICK CHARGE 2.0 SMARTPHONE CHARGER REFERENCE DESIGN


Power Integrations introduces the first reference design for a Qualcomm Quick Charge 2.0-enabled charger power supply. Launched earlier this year, the Quick Charge 2.0 protocol from Qualcomm enables users to charge mobile devices, such as tablets and cellphone handsets, up to 75% faster than when using conventional USB charging technology.

Power Integrations has developed the ChiPhy family of AC-DC wall-charger interface ICs which, when combined with the company's AC-DC switcher ICs, incorporates all of the necessary elements to add rapid charging functionality to AC-DC wall chargers. The CHY100 IC detects commands from a Quick Charge 2.0-enabled device, and adjusts the output voltage of the AC-DC wall charger to deliver increased power to the device's battery through a standard USB cable. When plugged into a five-volt USB-powered device without Quick Charge 2.0 capability, CHY100 IC automatically disables the higher-voltage capability to ensure safe operation and backwards compatibility with older hardware.

**www.powerint.com**

## NEW AP4034 FAMILY OF POWER MOSFETS FOR DC-DC CONVERTER APPLICATIONS

Advanced Power Electronics Corp (USA) has introduced a new family of 30V N-channel enhancement-mode power MOSFETs – called the AP4034. It is available in several packages to offer flexibility and meet differing cost/performance points. All AP4034 MOSFETs provide fast switching and feature a low typical gate-charge of 15nC for good switching performance.

With the best thermal performance of the three, AP4034GMT-HF-3 MOSFETs benefit from a low maximum on-resistance of 8mΩ and a drain-source current rating of 44.3A. The devices come in a PMPAK5x6 package with an integrated thermal pad and a standard SO-8 footprint compatible with other enhanced 5 x 6mm packages. The AP4034GM-HF-3 is in a standard SO-8 package, which is widely used for commercial and industrial surface-mount applications, and offers a maximum on-resistance of 9mΩ and drain-source current rating is 13A.

AP4034GYT-HF-3 MOSFETs have maximum on-resistance of 9mΩ, with a drain-source current rating of 15.5A but with improved thermal performance and smaller 3 x 3mm footprint.

**www.a-powerusa.com**

MOUSER ELECTRONICS

## Intel 20nm High Performance Solid-State Drives Now Available At Mouser

Mouser Electronics now stocks Intel's high performance solid state drives (SSDs), offering improved performance, increased reliability and lower operating costs over conventional hard drives.

Intel's SSDs are a high performance hard drive alternative for boosting laptop and desktop PCs to the next level in performance and reliability. They are 50% faster, 60% more durable and use 20% less power compared to conventional computer hard drives.

Improved performance, reliability and battery life are only the start of the benefits of Intel SSDs. The 530 Series SSDs target consumer desktops and laptops, provide a small form-factor, low cost of operation and low idle power. These SSDs continue to evolve as new consumer platforms emerge, not just for traditional desktops and laptops but also for Ultrabooks, tablets and tomorrow's small form-factor mobile systems.

Intel's DC S3500 Series SSDs, target data centers and combine consistently fast read/write performance with the strong data protection of leading edge 20nm Flash memory technology.

**www.mouser.com**

## TE's Micro-MaTch Connectors Are One Of The Smallest 1.27mm Connector Systems Available

TTI Inc now stocks TE Connectivity's Micro-MaTch connectors. With its contact spacing of 1.27mm, the connector family fully complies with the electronic packaging requirements of today and the future. The system offers a range of board and wire connectors, enabling a variety of wire-to-board and board-to-board interconnections.

The Micro-MaTch contact concept is essentially different from other systems available. By its design, the traditional failure mode in tin-plated connections, fretting corrosion, is prevented. Due to an additional positioning spring in the female part, relative movements caused by vibrations/thermal expansion between male and female contacts are absorbed. By preventing movements on the contact spot, a gas tight connection can be guaranteed under all circumstances.

The contact spring is located in the board connector and not in the cable connector, which is usually the case. The counterpart, incorporated in the cable connector, is a simple pin, either with an insulation displacement section or a kinked solder leg.

**www.ttieurope.com**

# 10 PORT & 20 PORT USB CHARGING & SYNC HUBS

**Powersolve professional USB charging & sync hubs are ideal for schools, businesses or in fact any application requiring multiple connection to USB devices, for either charging or data transfer**


Features

- Charges and syncs up to 10 devices (PSUSB-10CH), or 20 devices (PSUSB-20CH)
- Charge current 2A for 10 port hub and 1.1A for 20 port hub
- Supports high speed 480 Mbps, full speed 12 Mbps and low speed 1.5 Mbps operation
- Compatible with all USB compliant devices
- 10 or 20 USB 2.0 downstream ports, depending on model
- Over current detection and protection and surge and ESD protection
- 3 x 10 port devices can be connected in cascade to give up to an optimum of 30 USB ports
- 2 x 20 port devices can be connected in cascade to give up to an optimum of 40 USB ports
- Supports Windows 98SE/ME/2000/XP/Vista/7/8/ and Mac OS 8.6/9.X/10.X and higher

## 10 Port 60 Watt USB Charger (charging only)


**Features**

- Universal 90-264VAC Input
- IEC320 C8 2 pin AC Input Connector (UK power cord included)
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- Will charge most devices powered by standard USB 5VDC chargers
- EMC to EN55022'B', CISPR22 'B' & FCC 'B'
- Full International Safety Approvals & CE marked
- Compact Desk Top Enclosure
- Meets ROHS requirements

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