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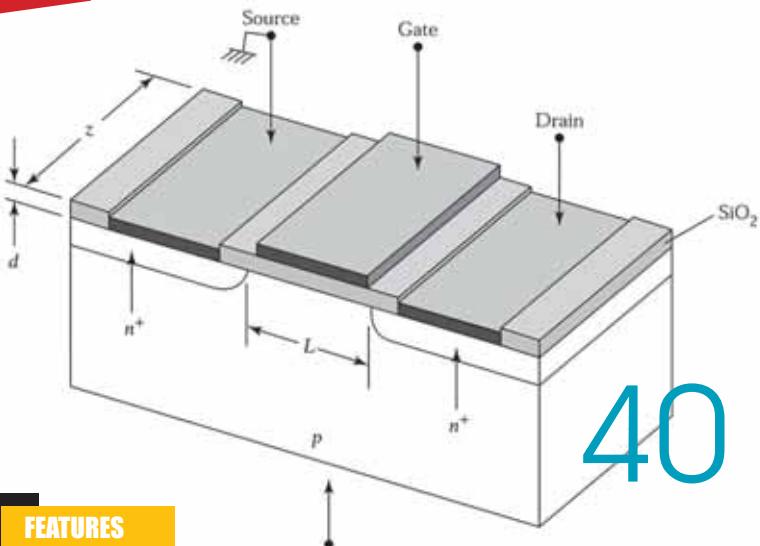
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COMBO SENSORS WILL SHAPE A \$2BN MARKET

French firm Yole Développement has analysed the impact of 6- and 9-axis combo solutions on the market and found that 2012 was seen by many as a turning point for consumer combo sensors, with high volume adoption in many platforms, including the Samsung Galaxy S smartphone. Since then many developments have occurred and the market acceptance of combo solutions has been extremely quick, not only for 6-axis devices (adopted in a growing number of platforms) but also for 6-axis e-compass (shipments are reaching new records every month). In addition, 9-axis solutions are being introduced to the market and innovative creations will follow, integrating pressure sensing, processing units and RF capabilities among others.

The combo sensor market was estimated at \$446m in 2013, representing 21% of the global inertial consumer market. By 2018 it is expected to grow by an impressive 66%, to \$1.97bn. "While smartphones and tablets are now driving volume increases and adoption of combo [solutions], the picture should be different in 2018," said Laurent Robin, Activity Leader, Inertial MEMS Devices & Technologies at Yole Développement. "The next market wave should come from wearable electronics, where the long-term market potential is huge. While combo sensors will take a significant portion of total market share, opportunities will remain for discrete sensors: from accelerometers used in basic activity trackers to gyroscopes for camera module stabilization."

In the early days, inertial combo sensors had to surmount certain challenges before being widely adopted. Sometimes they were said to be inaccurate or to create constraints for placement on the board (for magnetic field detection a tiny magnetometer die is often preferred to a larger combo package). Footprint reduction was the only argument in favour of combo sensors in the past. However, recently significant improvements have been made with most of the past yield issues resolved, leading to lower unit prices. In addition, combo solutions facilitate both qualification and testing at integrator level, and development of sensor fusion.

There has been much hype over the years regarding sensor fusion



“

The next market wave for combo sensors should come from wearable electronics, where the long-term market potential is huge

developments, but we have just started to see commercial implementations. The first commercial products with sensor fusion are already on the market, such as sensor hubs in the latest smartphones and tablets from Samsung, and more recently by Apple, with the M7 processor in iPhone 5S. In addition, GPS chipsets with indoor navigation capability relying on MEMS sensors are now available from CSR, Qualcomm and Broadcom.

Four Players Share 75% Of The Market

STMicroelectronics (ST) is the global leader in the inertial consumer sensor market with 42% market share. Only InvenSense and Bosch Sensortec are able to compete with it today.

It is key to be able to control the different technologies or to establish the right partnerships to sell a large range of combo solutions. ST started selling its own magnetometer in 2013, while Bosch has been very active in launching new product lines since 2012. InvenSense has partnered with Melexis as an alternative source to AKM for the magnetometer die in 9-axis solutions.

The unit price is sharply dropping, in 2013 selling under \$1 in large volumes. To stay in the race, the three leaders will need to continue with technical innovations: monolithic integration of 6- to 9-axis, use of TSV, chip scale packaging and active capping, among others.

Other companies, including Kionix, Freescale, Alps Electric, Fairchild and Maxim are eyeing this market, getting ready to address it with new business models.

In the sensor fusion ecosystem, we are seeing the first signs of consolidation as collaborations along the value chain are being set up (Qualcomm with Cisco Systems, Aruba acquisition of Meridian, Apple acquisition of WiFiSLAM etc.).

Laurent Robin is in charge of the MEMS & Sensors market research at Yole Développement with focus on inertial sensors & RF MEMS related technologies. Contact leroy@yole.fr for more information on this subject

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BLUETOOTH-ENABLED JEWELLERY HITS THE SHOPS

CSR is the latest in a line of companies launching 'wearable' electronics. The UK-based company used its latest Bluetooth Smart solution – the CSR1012 – to develop a range of Bluetooth-connected jewellery, which will alert users to new notifications on their smartphone or other connected devices. On the aesthetic side, the Bluetooth-enabled necklaces and bracelets will also be able to change brightness and colour too.

"Many of the wearable technology devices hitting the shelves today offer great features but don't take into consideration that consumers want beautiful, cutting-edge devices that

complement their personal style," says Paul Williamson, Director of Low Power Wireless at CSR. "If wearable technology is to reach its potential it needs to appeal to more than just technology lovers. Devices like these connected pendants will help wearable tech go mass-market."

CSR's innovative Bluetooth Smart platform has been engineered specifically for the wearable-technology market. It allows the jewellery to connect to smartphones using a fraction of the power of standard Bluetooth by connecting directly to a small lithium battery. It's also designed to enable a small form-factor, to

fit into various wearable accessories.

Those wearing the jewellery can be alerted to new notifications from their iPhone. This is because the CSR microprocessor within the necklaces supports the Apple Notification Center Service (ANCS), a new feature released in iOS 7 which allows peripheral devices to access all notifications generated on an iOS device over a Bluetooth connection. CSR will also be demonstrating Android applications that enable the user to set the colour and patterns of the jewellery.

"Although these prototypes have been designed to alert users to notifications on their smartphones, they could be used for many other things," concludes Williamson. "Developers could use the same printed circuit board (PCB) to design more aesthetically pleasing activity monitors. They could even integrate scent capsules to allow users to release a spray of their favourite fragrance at certain times. We wanted to give our customers a glimpse of what they could do with this technology. The possibilities for truly wearable technology devices are endless and we're looking forward to seeing what they develop with it in the future."

CSR recently asked consumers of their views on wearable technology and found that 72% believe it's important for wearable technology devices to look good and 67% require that they fit with their personal style.



Wearable communications electronics is now being integrated into jewellery

AGILENT TECHNOLOGIES REVEALS NAME OF ELECTRONIC MEASUREMENT SPIN-OFF COMPANY

Agilent Technologies is going to spin off its test and measurement (T&M) business into a standalone company called Keysight Technologies later this year. "The name Keysight conveys the ability to see what others cannot, offering critical or key insights to

understand and unlock the changing technology landscape," said Chris Rennie, Keysight Technologies UK Managing Director designate. "The new company's tagline, 'unlocking measurement insights for 75 years', commemorates the 1939 birth of the original Hewlett-Packard company, from which Keysight originated."

Agilent's \$2.9bn T&M business is recognized worldwide as one of the key suppliers of T&M equipment and services. The new company will include the entire portfolio of Agilent electronic measurement products focusing on

the communications, industrial, computers, semiconductors and aerospace and defence market sectors.

The splitting up process will begin in August, and complete in early November 2014. Keysight's headquarters will be in Santa Rosa, California, and the company will have approximately 9,500 employees in 30 countries.

The rest of the Agilent business, currently worth \$3.9bn, including pharma/biotech, chemical, energy and molecular diagnostics among others, will retain the Agilent name and pursue its own course.



Unlocking Measurement Insights for 75 Years

THE FUTURE OF REFRIGERATION LOOKS COOL

Scientists at the National Physical Laboratory (NPL) and Imperial College are working to make inefficient methods of refrigeration and air conditioning a thing of the past, leading to a complete overhaul of the refrigeration industry.

A new project sets out to provide a more economical, energy-efficient and environmentally-friendly cooling alternative based on the electrocaloric effect, a phenomenon in which a material changes temperature under applied electric field.

Current domestic refrigeration relies on a continuous cycle of compression and expansion of chemicals – known as vapour compression. Freon gas, for example, can be cooled and condensed into a liquid, which then absorbs heat from the refrigeration area, causing it to re-evaporate, where it begins the cycle again. However, these chemicals can be harmful to the environment when disposed of, or if they leak. They have a fairly low efficiency, requiring high energy input to create adequate cooling. They also require bulky apparatus, making them unsuitable for smaller applications, such as cooling electronics.

Thermoelectric and magnetic cooling technologies have been put forward as environmentally-friendly alternatives to vapour compression. However, these technologies struggle to compete with vapour-compression due to intrinsically low energy-efficiency (maximum 10%), and the need for large and expensive magnets to generate the magnetic fields needed to run magnetic coolers.

"An electrocaloric cooler could potentially deliver higher efficiency than vapour compression – as the creation of an electric field requires less energy than the compression process to create the same level of cooling," explained Maciej Rokosz, PhD student at NPL and Imperial. "It could also offer reduced size and weight, making it viable for applications like cooling electronics."

The team believe they will see the first electrocaloric refrigerator operating in room temperature surroundings within the next three years.



Tatiana Correia is one of Imperial College research team working on the electrocaloric cooler

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PROTECTION STRATEGIES FOR POWERING LOW VOLTAGE DIGITAL LOGIC

By Willie Chan, Senior Product Marketing Engineer and Jason Sekanina, Design Engineer
Power µModule Products, Linear Technology Corp.

T

Intermediate bus voltages of 24V~28V nominal are commonplace in industrial, aerospace and defense systems where series-connected batteries may be a backup power source and 12V bus architectures tend to be impractical due to distribution losses. The widening voltage gap between the system bus and the power inputs of digital processors present design challenges relating to power delivery, safety and solution size. If a single-stage non-isolated step-down DC/DC converter is used, it must operate with extremely accurate PFM/PWM timing. Input surge events put further stress on the DC/DC converter, presenting another overvoltage risk to the load. Erroneous or counterfeit capacitors introduced in manufacturing may cause output voltage excursions exceeding the load's ratings, potentially causing the FPGA, ASIC or microprocessor to ignite. Determining root cause can be challenging and costly to repair. Such failures can result in significant downtime and cause great harm to reputation, thereby impacting future opportunities and revenue stream.

Therefore, an overvoltage protection strategy must be given careful consideration to minimize cost and inconvenience to customers. Traditional overvoltage protection schemes involving a fuse are inadequate for protecting modern digital processors, particularly when the upstream voltage rail is 24V or 28V nominal. A new solution has been created, combining a 38V-rated, 10A DC/DC switching regulator with circuitry to defend against many faults, including output overvoltage. Power and protection for today's most advanced digital logic devices are now available in one compact device.

Protection Strategy Planning

Any protection strategy should consider how the system would respond to and recover from an overvoltage condition. Is the possibility of smoke or fire resulting from an overvoltage fault acceptable? Would efforts to determine root cause and implement corrective actions be hampered by damage resulting from an overvoltage fault? If a local operator were to power-cycle (reboot) a compromised system, would even greater harm come to the system, further hindering recovery efforts? What is the process and time required to determine the cause of the fault and resume normal system operation? Which protection circuit architecture is most appropriate for my load?

Review of the Traditional Protection Circuit

A traditional overvoltage protection scheme consists of a fuse, silicon controlled rectifier (SCR), and Zener diode. This circuit (Figure 1) protects the load in the following manner. If the input supply voltage exceeds the Zener breakdown voltage, the SCR

activates, drawing sufficient current to blow open the upstream fuse. It is relatively simple and inexpensive, however drawbacks of this approach include accuracy of the Zener diode breakdown voltage, SCR gate trigger threshold variation, varying response time of the SCR and fuse and the level of effort required to recover from a fault. If the voltage rail under consideration powers the digital core, the SCR's protection capability is limited since the forward drop at high currents is comparable to or above the core voltage of the latest digital processors. Because of these drawbacks, the traditional overvoltage protection scheme is not suitable for high voltage to low voltage DC/DC conversion powering loads valued in the hundreds if not thousands dollars.

A New Innovation Combining Power & Protection Circuits

A better solution would be to accurately detect an imminent overvoltage condition and respond by quickly disconnecting the input supply while discharging excess voltage at the load with a low impedance path. This is now possible with the extensive protection features included within the LTM4641 step-down µModule® regulator. At its core is a 38V-rated, 10A step-down regulator with the inductor, control IC, power switches and compensation all contained in one surface mount package. However, to add a level of protection for high value loads such as ASICs, FPGAs and microprocessors, extensive monitoring and protection circuitry is included. The LTM4641 constantly watches for input undervoltage, input overvoltage, overtemperature and output overvoltage and overcurrent conditions and acts appropriately to protect the load. To avoid false or premature execution of the protection features, each of these monitored parameters has built-in glitch immunity and user adjustable trigger thresholds—with the exception of overcurrent protection, which is implemented by reliable cycle-by-cycle current-mode control. In the case of an output overvoltage condition, the LTM4641 reacts within 500ns of fault detection (Figure 2).

Not only does the internal architecture of the LTM4641 allow it to respond nimbly and reliably, it can even automatically reset and rearm itself after fault conditions have subsided. A differential sense amplifier is employed to regulate the voltage at the load's power terminals, minimizing errors stemming from common-mode noise and PCB trace voltage drops between the LTM4641 and the load. The DC voltage at the load is regulated to better than $\pm 1.5\%$ accuracy over line, load and temperature. This accurate output voltage measurement is also fed to the fast output overvoltage comparator, which triggers the LTM4641's protection features.

When an overvoltage condition is detected, the µModule regulator rapidly takes multiple courses of action, simultaneously. An external MOSFET (MSP in Figure 3) disconnects the input

supply, removing the high voltage path from the regulator and the high-value load. Another external MOSFET (MCB in Figure 3) implements a low impedance crowbar function, quickly discharging the load's bypass capacitors (C in Figure 3). The DC/DC step-down regulator within the LTM4641 enters a latched-off shutdown state and issues a fault signal indicated by the HYST pin which can be used by the system to initiate a well managed shutdown sequence and/or system reset. A dedicated voltage reference independent of the control loop's reference voltage is used to detect fault conditions. This provides resilience against a single-point failure, should the control loop's reference happen to fail.

The improvement in protection offered by the LTM4641 over the traditional fuse/SCR protection scheme is further bolstered by how the system recovers from a fault. In the traditional overvoltage protection scheme, a fuse is relied upon to separate the power supply from the high value load. Therefore, in order to resume normal operation after a fault has occurred, someone must physically be present to remove and replace the fuse. In contrast, the LTM4641 can resume normal operation quickly once the fault condition has cleared either by toggling a logic level control pin or by configuring the LTM4641 for autonomous restart after a user specified timeout period expires. No components need to be physically replaced, which is a critical requirement for systems with high uptime requirements—especially those operating in remote locations. If fault conditions reappear after the LTM4641 resumes operation, the aforementioned protections immediately engage to protect the load.

Input Surge Protection

In some cases, output overvoltage protection alone is insufficient, and input overvoltage protection is desired. The LTM4641's protection circuitry can monitor the input voltage and activate its protection features, should a user-configured voltage threshold be exceeded. If the anticipated maximum input voltage exceeds the 38V rating of the module, input surge protection can be extended up to 80V with the LTM4641 still fully operational by adding an external high voltage LDO, which keeps control and protection circuitry alive.

Conclusion

With market requirements for higher system performance and uptime coupled with the tremendous expense of the latest digital processors, engineers must evaluate protection strategies, particularly when a distributed power bus in range of 12V-28V or those with surges are involved. The latest-generation and often very costly FPGAs, ASICs, and microprocessors have supply voltages with a maximum voltage SOA limit as low as 3% - 10% of the intermediate voltage rail, which makes them extremely susceptible to damage. Such faults might be caused by timing errors in the switching regulator, an input voltage surge or improper components introduced during manufacturing. The reaction and recovery time of today's overvoltage protection schemes must be faster and more precise than a traditional fuse/SCR circuit. The

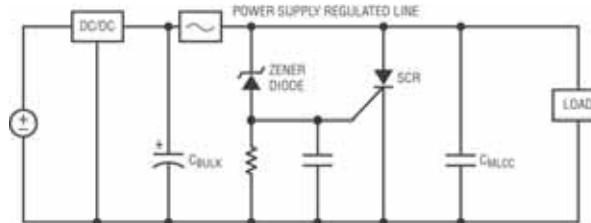


Figure 1: Traditional overvoltage protection circuit consisting of a fuse, SCR and Zener diode. While inexpensive, this circuit's accuracy and response time is insufficient to reliably protect the latest digital circuits, particularly when the upstream supply rail is an intermediate voltage bus. Moreover, even the simplest recovery from an overvoltage fault is invasive and time consuming.

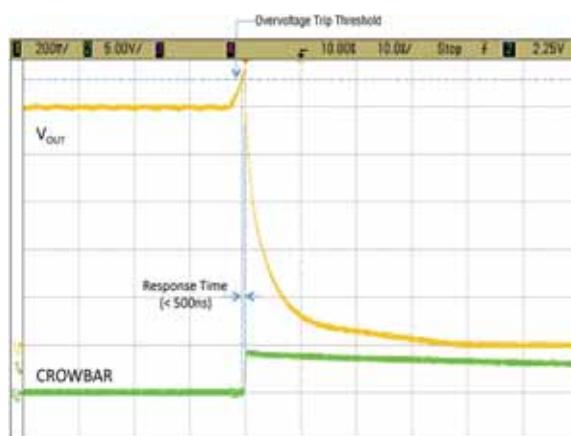


Figure 2: The LTM4641 protects the load from voltage stress by responding to an overvoltage condition within 500ns of fault detection. (VIN = 38V, VOUT = 1.0V, adjustable overvoltage trip threshold set at +5%)

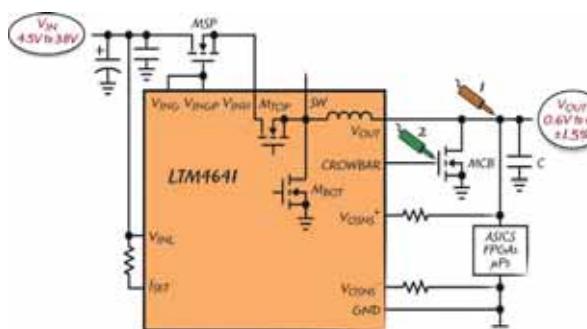


Figure 3: LTM4641 output overvoltage protection plan. The two probe icons correspond with the waveforms in Figure 2.

Watch the LTM4641's protection in real time at
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LTM4641, combining an efficient 10A DC/DC step-down regulator with a fast and accurate output overvoltage protection circuit in one surface mount package, meets these demanding requirements and forms an integral part of a protection strategy for the latest mission-critical systems.

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Over the last decade how often has a statement like that graced the pages of the technical press?... (usually with a discrete mention somewhere in the text that the author is employed by one or other major silicon vendors.)

As an RF engineer working in the low-power radio industry such statements have been the bane of my existence – not because they are true, but because every time they pop up every non-technical manager decides that *this time* they are true. There is partial truth at best, but whilst some applications may fit silicon radios, others require conventional “real component” circuit approaches, and it definitely does not mean that whatever that statement might be advocating as a solution will solve all current (or future) problems.

Sadly, pushed on by these non-technical managers (who are typically several layers up and removed from everyday engineering), the RF engineering staff then enjoy an additional, pointless, increment to their workload, by having to minutely justify the actual methods they need to use to realise an actual product that meets actual specifications, against an incessant, uninformed critic's chorus singing variations of “Why don't you just use a *chip*?”

The thing is, sometimes there is a morsel of sense to this. High-integration RF silicon is not a panacea to every radio-engineering solution, but it has, over the last decade, become a great deal more sophisticated. It is no longer reasonable to condemn every single-chip radio device as noisy, unstable, low spec, hard to use and expensive. While all of those pejoratives have been well-earned by older designs, the current generation of integrated devices has reached a level of performance that even a “traditional” engineer cannot ignore.

Specifically, I'm referring to phase-noise performance. We now have parts from two or three different suppliers that have

local oscillator phase-noise approaching levels previously only attainable with (admittedly simple) discrete VCO plus PLL approaches (around -110dBc/Hz at $\pm 12.5\text{kHz}$ offset). This is significant. It doesn't

really matter if the parts in question are intended to be used as receivers or transmitters, it's the achievable level of performance that is crucial.

This is the point at which the local oscillator phase-noise is no longer the only (or major) defining factor in receiver adjacent-channel selectivity performance. A 60dB spec is quite easily met with a local oscillator of this type, which in turn makes it possible to build chip-based narrowband radios with performance levels as good as typical older discrete designs. (Some previous generation single-chip radios I have seen for “high performance narrowband” usage have offered selectivity performance levels as low as 25-30dB).

So is every industrial telemetry radio now going to be a single chip?

Unfortunately not! While there has been a truly impressive improvement in one crucial specification, the overall implementation of a typical single-chip radio still has a few hidden pitfalls:

- The remainder of the (on-chip) receive path won't always live up to the (new) local oscillator performance. The low IF or direct conversion systems found on most chips are frequently lacking in image performance, filter stop-band and large signal handling, and they often have very time-consuming calibration sequences before they achieve anything close to their datasheet performance.
- The baseband interface is usually “digital only” and frequently requires the transmit datastream to be synchronous with a (device supplied) clock. This is a serious issue if an analogue path is needed (in audio applications, for example) or if the new radio needs to work with existing (legacy) data structures.



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- Operating frequency bands are limited. Many devices cover, for example, 433 and 868MHz, but what if the specific customer requirement is for a 230MHz band military application, or low VHF, or a 700MHz licensed band? You cannot "just re-tune" an integrated device in the way that you can with a discrete component design.
- The user-programming interfaces of the newer generations of RF silicon devices are becoming more and more complex. While this isn't a problem at the evaluation stage, where a PC-based "driver" and a sophisticated suite of demonstration boards can be brought to bear, it can make the actual real-product implementation learning curve (where processing power, memory and pin count can be at a premium) unacceptably steep.

Maybe the preceding list of issues looks unduly pessimistic, but it isn't. Five years ago it would have been four pages long. Current generation RF silicon has reached a remarkable level of performance and has become a tool that allows a skillful engineer to implement solutions to problems in ways not previously imaginable, but we have not yet reached some imaginary plateau of perfection. There is a lot that integrated devices cannot do as well as conventional circuits, but I do not for a moment imagine that the upward path of development has stopped.

I, for one, am looking forward to seeing what the next five years will bring. ●

A LONG SHOPPING LIST?

If on the off chance an RF silicon designer might happen to be reading this piece, then this particular engineer has quite a long shopping list of useful functions he'd like to see in chip form. How about starting with a low noise local oscillator, plus a good (high IP3) mixer, all integrated with a simple-to-drive user interface, in a straightforward package that even an unsophisticated assembly subcontractor can place? I can think of a good few uses for something like that.

Housed in a low-profile U-channel the UP series delivers from 150W to 400W (UP350 = 300W, UP500 = 400W) with free air convection, (UP350 = 350W, UP500 = 500W with fan cooling). Built using 105°C electrolytic capacitors for a long service life, these units are designed for a range of telecom and industrial applications requiring low maintenance and noise. All models have universal ac input, and are available with a single output voltage of 12, 15, 24 or 48Vdc. Safeguards include: short-circuit protection; over-voltage protection; overload protection and over-temperature protection. The 350W and 500W units also feature: active inrush current limiting; remote voltage sensing; remote inhibit function; power OK signal.

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CHRISTIAN KUECK, STRATEGIC MARKETING MANAGER FOR POWER MANAGEMENT PRODUCTS AT LINEAR TECHNOLOGY, EXPLAINS HOW TO MAKE THE OPTIMAL CHOICES IN PC BOARD LAYOUT FOR SOLID POWER-SUPPLY DESIGNS

PCB layout determines the success or failure of every power-supply project; it sets functional, electromagnetic interference (EMI) and thermal behaviour. Switching power-supply layout is not black magic, but is often overlooked until too late in the design process.

Fortunately, physics is on your side. Functional and EMI requirements must be met and, in the world of trade-offs in power-supply-unit layout, what is good for functional stability is good for EMI. Good layout from the beginning does not add to cost, but can save significant resources in EMI filters, mechanical shielding, EMI test time and PC board runs.

Some twelve years ago one of my customers used a switch-mode power supply (SMPS) in a car radio for the first time and his colleagues said that it could not be done. But, after a

few things in the input filtering and layout were ironed out, everything worked fine. Later, another customer successfully used a dual step-down switching regulator (LT1940 1MHz), which operated in the middle of the AM band of his car radio-receiver design. No additional metal shielding was required for the power supply unit (PSU); it was only an issue of placement and layout.

Power Supply Topologies

The most basic of non-isolated topologies is the buck regulator, where EMI starts off from high di/dt loops. The supply wire, as well as the load wire, should not have high AC current, so we will approach our analysis from the input capacitor's (C_{IN}) standpoint, which should source all relevant AC currents to the output capacitor, C_{OUT} , where any AC current ends.

Figure 1 shows that during the on cycle with S1 closed and S2 open, the AC current follows the red loop; and during the off cycle, with S1 open and S2 closed, the AC current follows

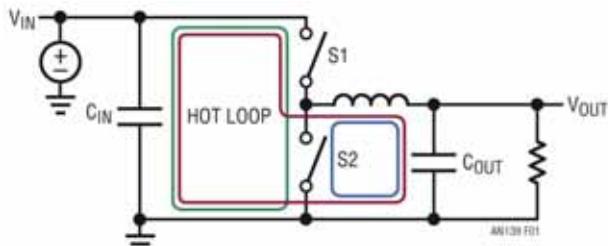


Figure 1: During the on cycle with S1 closed and S2 open, AC current follows the red loop

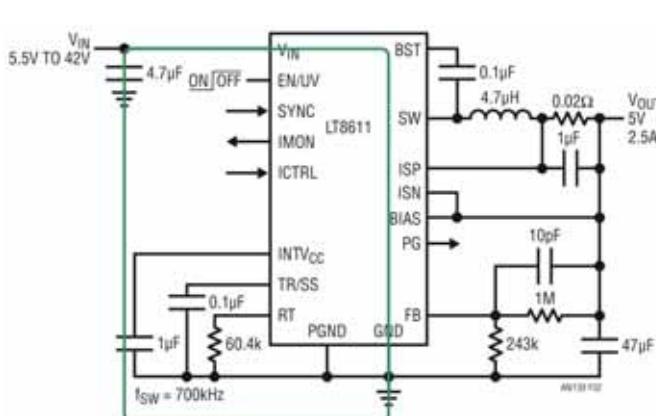


Figure 2: As shown by the schematic in Figure 2, the hot loop is not easy to spot for layout purposes

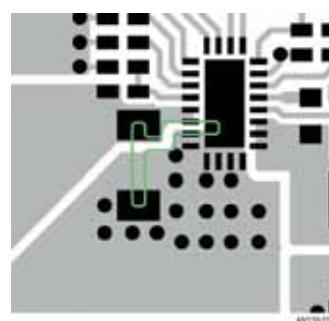


Figure 3: The layout of an LT8611 buck converter demo board (DC1750A)

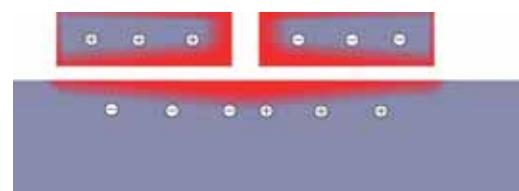


Figure 4: Current density in the cross cut of the hot loop

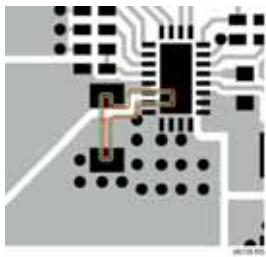


Figure 5: The green top layer hot loop magnetic AC field produces eddy currents in the plane

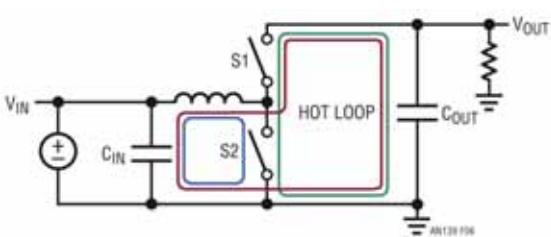


Figure 6: The hot loop is identified as the difference between the blue loop if S1 is closed and the red loop with S1 open and S2 closed

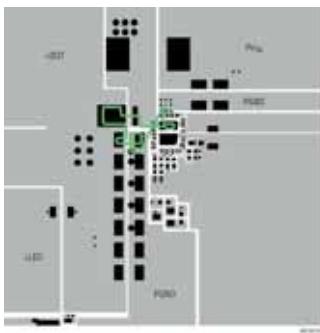


Figure 7: The hot loop of the LT3956 LED driver boost controller is shown in green

the blue loop. Both currents have a trapeze waveforms. Some designers have difficulty grasping that the loop producing the highest EMI is neither the red nor the blue one, but that fully-switched AC current flows only in the green loop, switched from zero to I_{PEAK} and back to zero. Since the green loop has the highest AC and EMI energy, we refer to it as the hot loop.

In order to reduce EMI and improve functionality, we need to reduce the radiating effect of the green loop as much as possible. If we could reduce the PC board area of the green loop to zero and use an ideal input capacitor with zero impedance, the problem will be solved, but we are limited to the real world, so the task is to find the optimal compromise.

ELECTROMAGNETIC FIELD IMPEDANCE

Far field impedance is about $377\Omega = 120\pi$ or $29,9792458 \times 4 \times \pi\Omega$ for the vacuum velocity of light. Any electromagnetic wave far enough from its source (rule of thumb $> \text{wavelength}/2 \times \pi$) has a 377Ω relationship between its magnetic and electric field. Closer to the source, it can be a perfectly matched antenna, which transforms its input power source to the right 377Ω electromagnetic field; or there is significant mismatch and the antenna acts mainly as a magnetic field source or an electric field source.

The magnetic field source has an impedance of 377Ω , while the electric field source's impedance is higher than 377Ω . The graph in Figure 30 shows that, regardless if it starts as an electric or a magnetic field source, the electromagnetic field balances itself to its far field impedance at a distance of:

$$\frac{\lambda}{2 \cdot \pi}$$

Non-isolated switch mode power supply (SMPS) units have primarily magnetic field sources since the impedances of the EMI-relevant loops with high di/dt are much lower than 377Ω , unless they are very low current, high-voltage power supplies. So minimizing the AC magnetic fields on any non-isolated power supply will be the key to success.

Any isolated power supply unit will have AC loops with lower than 377Ω , where the same magnetic field minimization as with non-isolated PSUs will be required. However, due to the very nature of isolation, we need higher impedances across the isolation barrier.

At the isolation barrier, which is mostly a transformer, we try for megohms of isolation. On the isolation barrier, the electric AC field dominates and requires a different strategy. Here we try to get as low capacitive field coupling as possible. So we try for as much distance as possible and to minimize the size of any conductors, i.e. copper.

Managing The Hot Loop

Let's take a look at the layout of the LT8611 buck converter (Figure 3). The LT8611 has both switches internally, so we only need to think of the input capacitor's connection.

From the schematic in Figure 2 it can be seen that the hot loop is not easy to spot for layout purposes; the green line is the hot loop in the top layer. AC current flows through the input capacitor and switches.

Figure 3 shows the DC1750A LT8611 demo board. The current density in the cross-cut of the hot loop looks like Figure 4.

How much does a copper short-circuit loop or plane under the hot loop improve the functional and EMI behaviour of a circuit? The result of an experiment with a 10cm x 10cm rectangular loop at 27MHz is shown in Table 1, where the improvement made by using a solid copper-plane under the hot loop topside traces can be seen. The inductance of a single-layer loop of 187nH gets down to 13nH with only 0.13mm insulation between the plane and loop traces.

DIPOLE ANTENNA EFFECT OF THE HOT LOOP

When analyzing what the hot loop does, magnetic dipole antennas give a good clue.

The AC current flows around an area and creates the magnetic field part of a normal dipole antenna (Figure 31).

Magnetic antennas with loop diameters \ll have very low radiation resistance, ranging from micro-ohms to milli-ohms.

$$R_R = 320\pi^4 \left[\frac{NF}{\lambda} \right]^2$$

R_R = Radiation resistance in Ω

F = Area of magnetic loop

N = Number of turns (= 1 in most layouts)

λ = Wavelength

with $\lambda = \frac{c}{f}$ and $N = 1$ for all practical layout loops

$$R_R = \frac{320\pi^4 N^2}{\lambda^2}$$

c = Speed of light ≈ 300000 km/s

f = Frequency

The radiation resistance is low ($m\Omega$) for typical dimensions of a PC-board power supply unit. Increasing the radiation resistance improves the matching and increases emitted radiation proportional to the radiation resistance. The parameter we can influence the most with layout is the area of the magnetic loop.

The emitted radiation is proportional to the square of this area.

d (mm)	f (MHz)	C (pF)	L (nH)	FACTOR OVER 0.12mm	
18.4	400	187	Single-Layer Open Loop	14.4	
21.2	400	141	Inner Copper Short-Circuit Loop	10.85	
1.5	38.9	400	42	Solid Plate 3.23	
1.5	34.7	400	53	Rectangular Loop No Overlap	4.08
0.5	52.1	400	23	Thin Rectangular	1.77
0.27	55	400	21		1.61
0.12	69	400	13	Paper	

Table 1: Indication of improvement provided by a solid copper plane under the hot loop topside traces

A solid plane on the next layer in a multilayer board (four layers or more) will have over 3x less inductance than a normal 1.5mm²-layer board with a solid bottom plane, and over 14x

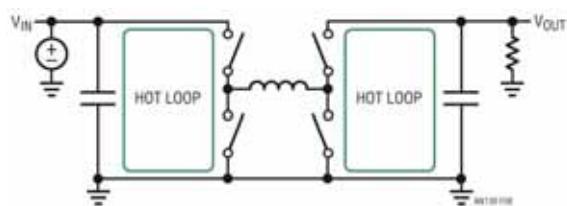


Figure 8: The single inductor 4-switch buck-boost consists of a buck circuit followed by a boost circuit

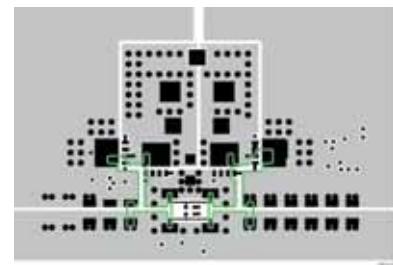


Figure 9: The LTC3780 DC1046A demo board shows an elegant solution splitting the sense resistor into two parallel ones

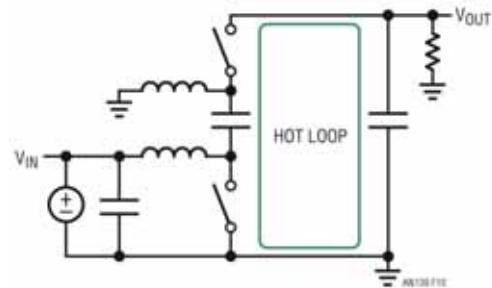


Figure 10: Drawing of a SEPIC circuit shows its hot loop. Instead of an active MOSFET for the top switch, a diode is often used

less than a single-layer board. A solid plane with minimum distance to the hot loop is one of the most effective ways to reduce EMI.

Where does the current flow in the plane? The green top-layer hot loop magnetic AC field produces eddy currents in the plane (Figure 5). Those eddy currents produce a mirror AC magnetic field, which is opposite the hot loop field (red trace). The two magnetic fields will cancel out. This works better the closer the mirror current is to the hot loop. Current is a round trip in the top layer. The most likely current path in the shield is the same round trip directly under the top layer. Both currents are almost the same. Since the plane current needs to be as high as the top trace current, it will produce as much voltage across the plane as necessary to sustain the current; to the outside it will show up as GND bounce.

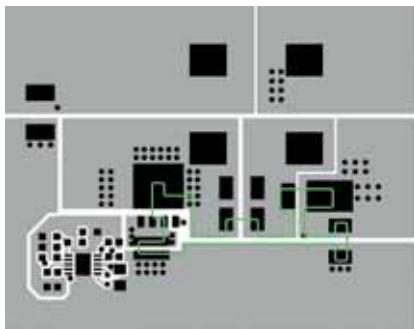


Figure 11: The LT3757 DC1341A shows a good SEPIC layout. The green hot loop area is minimized and there is a solid GND plane on the next layer

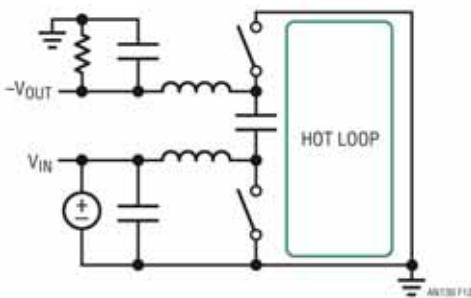


Figure 12: The inverting topology is very similar to SEPIC, only the signal has been directed through the top switch and top inductor

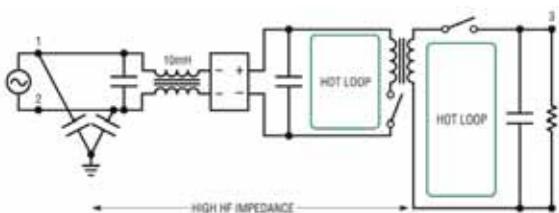


Figure 13: Flyback uses separate windings on a transformer with only magnetic coupling between the primary and secondary windings

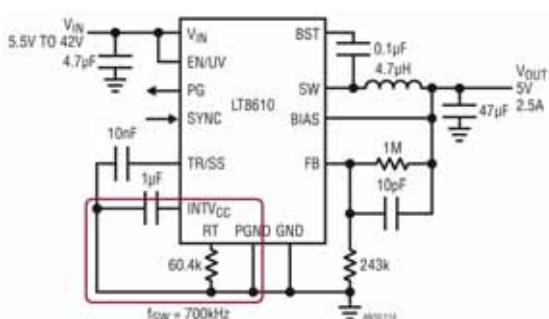


Figure 14: Other ICs use a separate voltage for the drive circuit, often referred to as INTVCC

Best Loops

From an EMI perspective small hot loops are best. A power supply IC with integrated sync switches, optimized pin-out and careful internal switch control will outperform on EMI a non-sync power-supply IC with external Schottky diode. Both will outperform a controller solution with external MOSFETs.

The boost circuit can be viewed in continuous mode as a buck circuit operating backwards. The hot loop is identified as the difference between the blue loop if S2 is closed and the red loop (Figure 6) with S2 open and S1 closed.

The hot loop of the LT3956 LED driver boost controller is shown in green (Figure 7). The second layer is a solid GND plane. The main EMI emitter is the magnetic antenna the hot loop creates. The area of the hot loop and its inductance are tightly related. If you are comfortable thinking in inductance, try to decrease it as much as you can. If you are more comfortable in antenna design, reduce the effective area of the magnetic antenna. For near-field purposes, inductance and magnetic antenna effectiveness are essentially the same.

The single inductor 4-switch buck-boost (Figure 8) consists of a buck circuit followed by a boost circuit. The

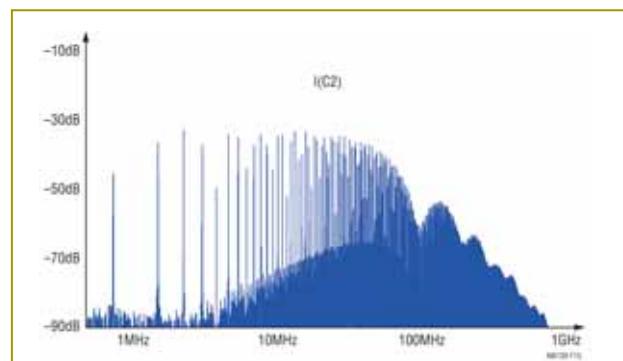


Figure 15: An FFT of the current in the INTVCC decoupling capacitor (C2 in Figure 17)

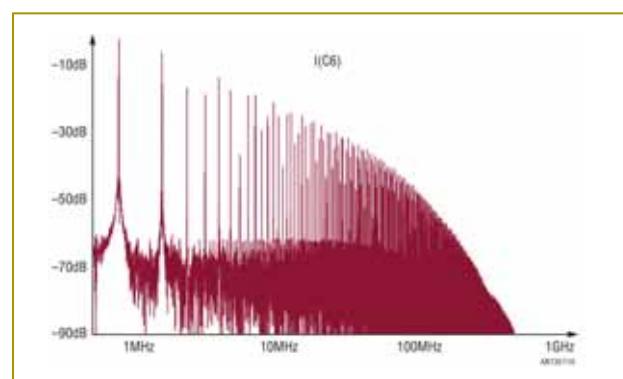


Figure 16: An FFT of the current in the input capacitor (C6 in Figure 17)

SKIN EFFECT

To understand the effect of shielding, we need to dig a bit into the electromagnetic properties of the materials used. Electric current, whether or not it is tied to a conductor, will always flow on the path of least impedance. For higher frequencies this will be the path of least inductance. This means the current will also flow on the path of its lowest losses. Electric conduction material minimizes any internal magnetic AC fields by creating eddy currents that oppose AC fields internal to the conducting material. Viewed from the outside, this looks like skin effect, because the current density is forced to the outside of the conductor.

For the first model example, assume that the current, I , flows uniformly through a cylinder. This is a typical case for DC current. If the current is DC, then it will look like that in Figure 32. Since I is constant, the resulting H is constant and I_w is zero. If I has an AC component, which means there is di/dt , then the resulting magnetic field H changes. The changing magnetic field H creates induction voltage and, since we are inside a conductor, the induction voltage creates an induced current I_w , often referred to as eddy current. Eddy currents will create losses. If we assume that nature minimizes these losses, the only way to minimize this is to change the original uniform current distribution and let all current flow only at the surface of the cylinder. Now the magnetic field H is only at the surface of the cylinder. This way the eddy currents I_w are moved to the outside and the return path is cut off, omitting most of the eddy currents and its losses.

Figure 33 shows forces that move the current density to the outside of a conductor, called skin effect. The wall thickness of a pipe, which would give the same resistance at DC as a solid wire at AC, is called skin depth (Figure 34). Since the forces moving the current density to the outside are a result of the induction law, skin depth decreases with rising frequency. Skin depth also decreases with rising conductivity and when magnetic permeability increases.

For another example, assume we have a pipe wall conducting all the current on its surface, as shown in the large diameter in Figure 35. Total inductance of a given length of this wire (1 meter or 1 foot, whatever is most suitable) is the complete volume integral of its magnetic field up to infinity or whatever physical size you assume for the universe.

Now we shrink the pipe diameter to the smaller inner one shown in Figure 35. The magnetic field is still the same as the old larger pipe to infinity. However, we now have an additional magnetic field volume between the new small pipe and the larger pipe diameter, so the total integral of the magnetic field is now larger. This shows that the inductance is larger for a thinner conductor of a given length, or we can assume that the inductance increases as more of the current moves from the outer wall to the centre of the wire. If we apply a voltage over both ends of the wire, the resulting current distribution is determined by the impedance.

Since the inductance in the centre is higher, most current

density moves to the surface. The most extreme case of skin effect in conductors with zero resistance is superconductors. There, quantum effects prevent all current from being bound to an outer layer of zero thickness. The thickness where most current is concentrated on superconductors is called London depth.

A graph of skin depth over frequency for some materials is shown in Figure 36. We see that copper on typical PC-board material is affected by skin effect starting in the 5MHz to 50MHz range, and that even highly doped silicon at the thickness typically used on ICs is only affected in the terahertz region. Copper (Cu) and gold (Au) are close together. Material with high magnetic permeability (Fe-Ni) has low skin depth even at audio frequencies. For this reason it is used to shield audio transformers.

AC current through a good conductor will push current density to the outside. The current will flow where the impedance, dominated by inductance, is lowest. With regard to the impact of skin effect on layout and components, we can derive simple guidelines. Better is short and thick or wide. Reverse geometry capacitors have lower ESL because they are shorter and thicker.

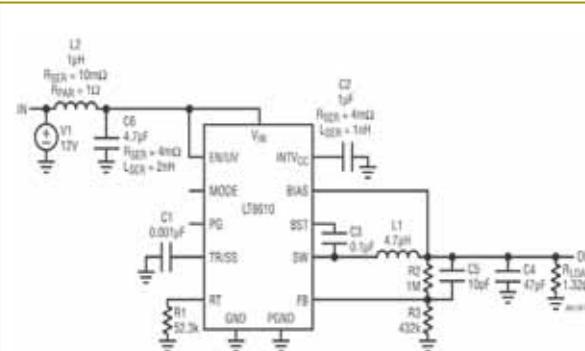


Figure 17: The LT8610 LTspice circuit. L2, with a high loss of $R_{PAR} = 1\Omega$ is used to decouple the zero impedance LTspice voltage source, V1, from the input capacitor, C6

layout will often be complicated by a common GND current shunt which belongs to both hot loops. The LTC3780 DC1046A demo board (Figure 9) shows an elegant solution, splitting the sense resistor into two parallel ones.

A drawing of a SEPIC (single-ended primary inductive converter) circuit, see Figure 10, shows its hot loop. Instead of an active MOSFET for the top switch, a diode is often used. The LT3757 DC1341A (Figure 11) shows a good SEPIC layout. The green hot-loop area is minimized, with a solid GND plane on the next layer.

The inverting topology (Figure 12) is very similar to SEPIC, with the signal now moving through the top switch

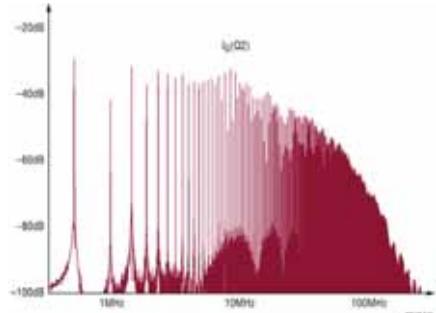


Figure 18: The FFT of the gate current into Q2 of Figure 19

PROXIMITY EFFECT

If we have opposite direction current, the same forces will attract the currents to each other (Figure 37). This is called proximity effect.

In a PC board trace on a single layer board, the high frequency current density will look like that in Figure 38. If we add a solid plane in a second layer eddy currents will be generated in the plane, creating in total a mirror image of the current in the top trace, as shown in Figure 39.

On multilayer boards, a plane will shield the AC currents (see Figure 40).

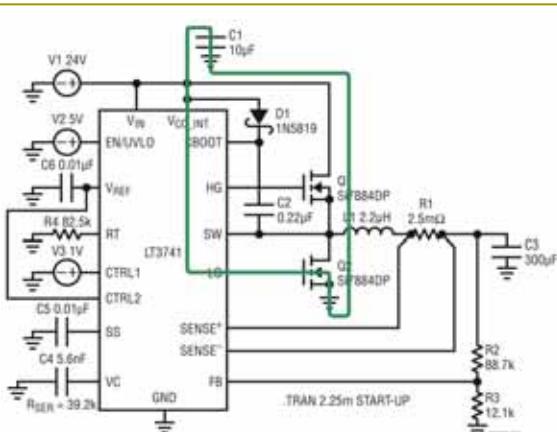


Figure 19: The green loop shows the current path for the bottom gate current. It is supplied from C1

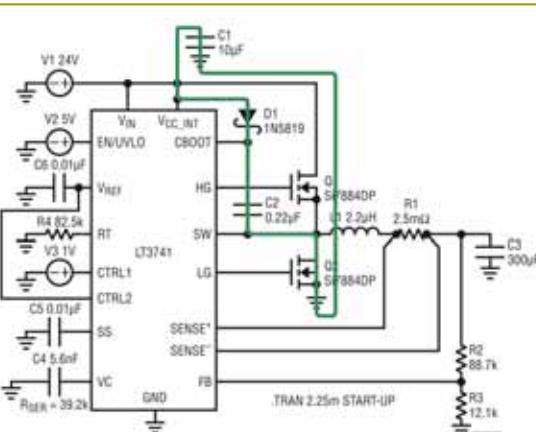


Figure 21: The green loop shows the recharge of the boost capacitor

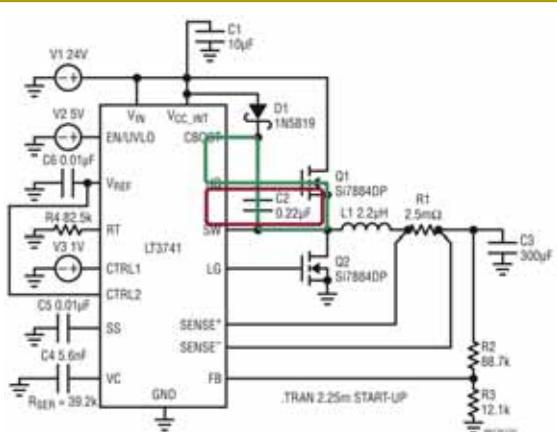


Figure 20: The red and green loop show the top gate drive current loops

and top inductor. The layout is very similar and the demo boards can typically be modified from SEPIC to inverting, provided the IC can also regulate on negative feedback voltage like the LT3581, LT3757, etc.

Flyback (Figure 13) uses separate windings on a

transformer and there is only magnetic coupling between the primary and secondary windings. The current in the primary winding goes to zero at a relative high di/dt ; only the energy stored in the leakage inductance and capacitance between windings and the switch node slows that down. The primary and other transformer windings can be seen as fully switched current. We get two hot loops as in the buck-boost case (Figure 8). To reduce EMI, in addition to close V_{IN} decoupling for differential mode EMI, common mode chokes are used for the likely dominant common mode EMI in Figure 13's topology.

Other AC Loops

The hot loop with the main switching energy is the major source of RF energy. However, for operation of the IC and the circuit, other AC carrying loops are required. All circuits need a supply for the main switch driver. In case of the buck, it is often decoupled with the same V_{IN} capacitor as the hot loop. Other ICs use a separate voltage for the drive circuit, often referred to as $INTV_{CC}$ (Figure 14).

Make the $INTV_{CC}$ capacitor PGND and GND loop as small as possible, shielded by a solid plane in the next layer.

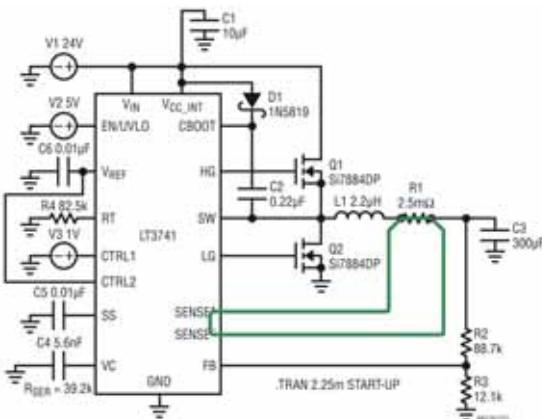


Figure 22: The sense amplifier looks with high bandwidth at SENSE+ and SENSE- on the small shunt voltage over R1 to terminate the top switch on cycle

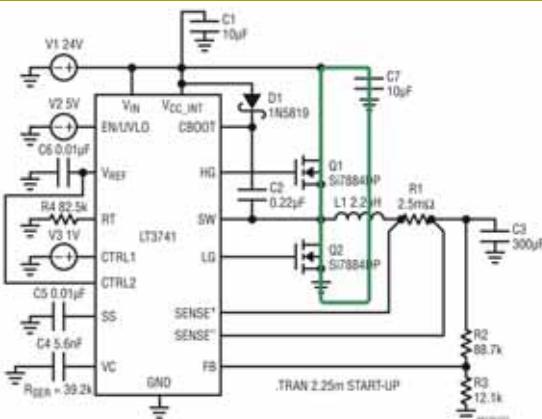


Figure 23: The main hot loop consists of the external MOSFETs Q1 and Q2 and the closest low impedance decoupling capacitor C7

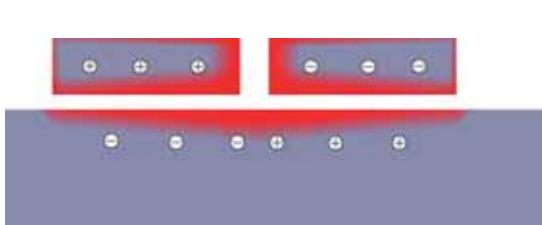


Figure 24: Eddy currents in the shield material need to create an AC magnetic field opposite to the original AC current behind the wall

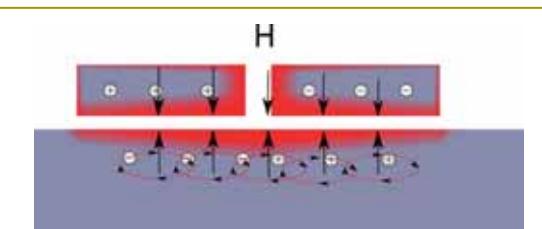


Figure 25: The eddy currents in the shield will only be enough to cancel any magnetic AC field to the outside of the box or, in this case, in the direction shown at the lower portion

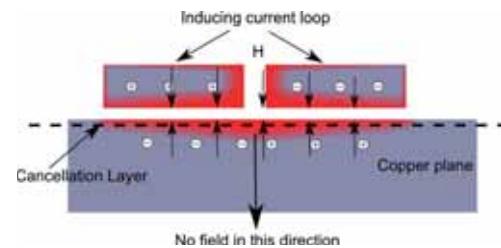


Figure 26: Currents will cancel any magnetic field inside the copper shield and outside in the direction away from the inducing current, within the limits of the skin and proximity effects

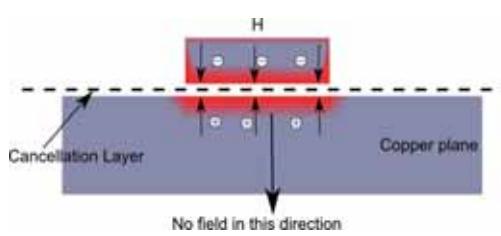


Figure 27: If the current returns through the plane, the situation is somewhat different. Now the current in the plane is not only passively induced, but is the active return flow

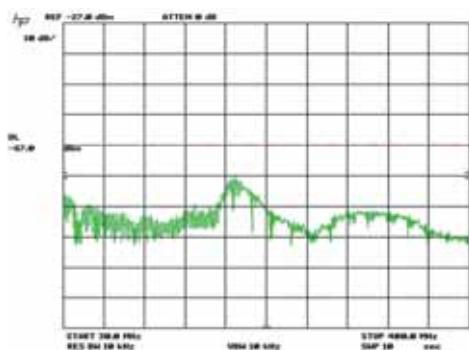


Figure 28: An LT8611 with some input filtering with a ferrite bead and 4.7uF ceramics line conducted from 30MHz to 400MHz. The display line of -67dBm corresponds to 40dBuV

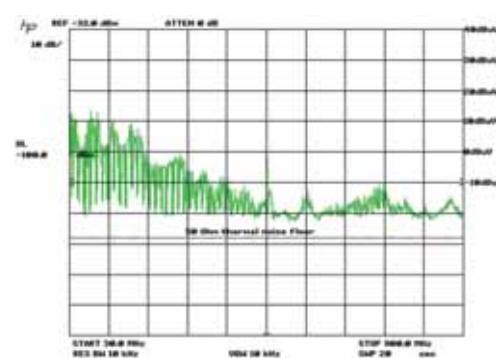


Figure 29: An LT8610 power supply 13V in, 5V out at 1A out, line conducted up to 900MHz

EMI energy is on the order of 20dB lower than in the main hot loop. Any excessive inductance in the INTV_{cc} loop will deteriorate IC performance. Figure 15 is an FFT of the current in the INTV_{cc} decoupling capacitor (C2 in Figure 17). Figure 16 shows an FFT of the current in the input capacitor (C6 in Figure 17). C6's RF energy is over 20dB higher than in the INTV_{cc} loop.

Figure 17 shows an LT8610 LTspice circuit. L2, with a high loss of $R_{PAR} = 1\Omega$, is used to decouple the zero impedance LTspice voltage source, V1, from the input capacitor, C6.

Note that LTspice switch-mode regulator models are developed to simulate the functionality of the IC, so use great caution to extrapolate RF behaviour because the models do not account for the internal or external lump devices or board layout. Nevertheless, LTspice is a great tool to get an approximation of very difficult to measure effects.

EMI MEASUREMENTS

Most power supplies are relatively small, compared to the wavelength of the relevant EMI frequencies they produce and are measured against. In prudently designed power supplies most of the energy is below 500MHz. EMI standards must be general and apply to equipment of variable size. Those can be in the order of the wavelength of interest. So they call for line conducted measurements up to 30MHz and radiated measurements above 30MHz. However, reliable radiated measurements require large anechoic chambers; hourly prices are high and availability scarce. Free field is too noisy, requires a large and difficult setup and is weather dependent.

For power supply optimization work, a reasonable approach is to make line-conducted pre-compliance measurements up to the end of the spectrum required for radiated measurements. Since the power supply dimensions are still small against the wavelength of interest, we can assume that most energy will find its way through the V_{IN} and V_{OUT} wires, where we can measure them line conducted.

The set-up is quite simple. We need a LISN (line impedance stabilizer network) or AN (artificial network), an input supply, a load and a measurement receiver. The purpose of the LISN (AN) is to isolate the voltage source V1 from the power supply (or DUT device under test) V_{IN} (V_{DUT+} , V_{DUT-}).

Figure 41 shows an example of a non-symmetric LISN often used in automotive equipment. Such a simple circuit can be made with L1 as air coil, or an inductor with losses can be used. Some standards specify different core types in series and a special winding scheme. However, the main purpose is to create a wideband high impedance against 50Ω for L1.

Other than the wire length inside for C1, R1 and the V_{OUT_HF} and L1 impedance, nothing limits the usable upper frequency range. So buy one or build your own. Resonances of L1 can be

External Switch Drive Signals

After the main hot-loop and the INTV_{cc} decoupling loop, the next EMI trouble sources are often external switch drive signals. Even modern MOSFETs have single-to-dual-digit-nanofarad effective input capacitance. Their drivers often have drive currents in the single amp range, with rise and fall times of just a few nanoseconds.

Figure 18 is the FFT of the gate current into Q2 of Figure 19. The green loop (Figure 19) shows the current path for the bottom gate, supplied from C1. Make sure this loop is small. The Q2-source GND to C1 GND connection is most easily accomplished with a solid GND area in the layer under the component layer.

The red and green loops (Figure 20) show the top gate drive-current loops. They are supplied from the boost capacitor, C2, and the return is the SW connection to the controller IC. Keep the red loop small and place the traces

damped with a resistor over a part of L1 windings. Any dedicated EMI receiver can be used, but a spectrum analyzer will usually do for pre-compliance work. Make sure you use the AC-coupled input, since it provides a second barrier against blowing up your expensive mixer inside the analyzer.

From the EMI lab experts, you can expect a lengthy discussion about the required detection method from the relevant EMI standard, including peak, quasi peak, average with relative accurate time constants required for them. You can shortcut this discussion when your power supply operates at fixed frequency in the load area of interest.

At fixed frequency, only harmonics with a distance of the switching frequency can be created, a frequency comb. If the switching frequency is above the required resolution bandwidth (mostly 9kHz up to 30MHz and 120kHz above 30MHz), peak, quasi peak and average methods will yield the same results, so you can use whatever your receiver provides. Some standards allow for the 9kHz to use a 10kHz bandwidth and for 120kHz 100kHz. The error for a fixed frequency switching PSU, which operates well above 100kHz, is not relevant for our pre-compliance task.

If your system includes a processor it can produce currents with large fluctuations with frequency contents well within the above resolution bandwidth.

Then you need to refrain to the filter method your standard requires. If you see components that are a fraction of the switching frequency or cannot be divided by integers to the switching frequency, check the switch node with an oscilloscope. In the time domain, you will likely see pulse skipping or subharmonic oscillation. Check the source for this behaviour before proceeding further.

Do not forget to unhook your scope probe because you get different results with the additional introduced probe antenna if you do EMI measurements with a probe attached.

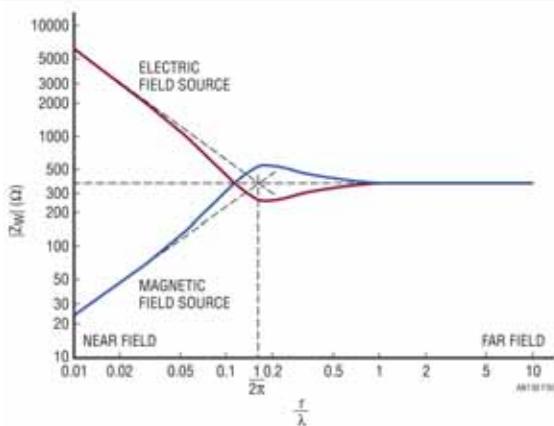


Figure 30: The graph shows that, regardless if it starts as an electric or a magnetic field source, the electromagnetic field balances itself to its far-field impedance

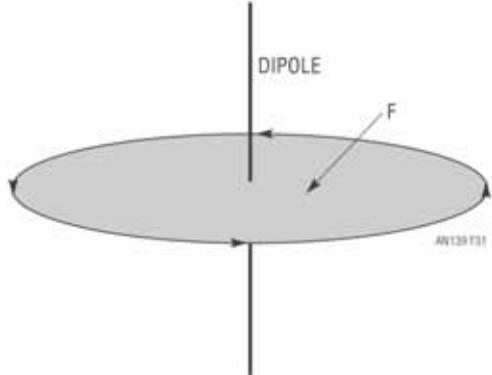


Figure 31: The AC current flows around an area and creates the magnetic field part of a normal dipole antenna

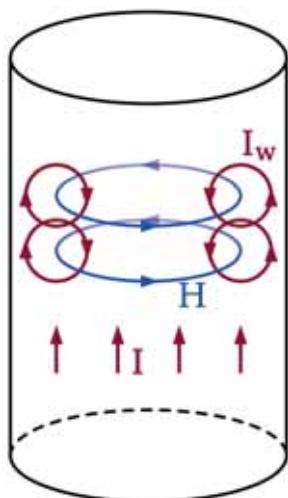


Figure 32: If the current is DC, then it will look like that shown here

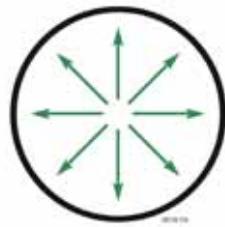


Figure 33: Forces that move the current density to the outside of a conductor are called skin effect

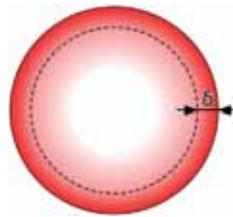


Figure 34: The wall thickness of a pipe, which would give the same resistance at DC as a solid wire at AC, is called skin depth

parallel with only a small gap. If C2 is placed close to the controller IC, the green loop will also become small.

The green loop of Figure 21 shows the recharge of the boost capacitor. If you have already made the above loops small and have placed D1 relatively close, this loop is also small.

Passive antennas, including magnetic antennas or loops, operate reciprocally; their transmit and receive characteristics are the same. The sense amplifier in Figure 22 looks with high bandwidth at SENSE+ and SENSE- on the small shunt voltage through R1 to terminate the top switch on-cycle. Even sub-millivolt noise will result in duty-cycle jitter.

Coupling to any of the former transmitting loops should be minimal. First, this loop area needs to be small as well, so make the gap between the SENSE+ and SENSE- line minimal. Then place the loop traces on the other side of a shielding plane from the high current loops mentioned earlier. If enough layers are available, the SENSE+ and SENSE- lines can be on top of each other if there are not significant magnetic AC fields parallel to the PC board layers. If SENSE+ and SENSE- filtering is used, place the filter close to the controller IC, since R1 is always low impedance and the sense inputs are higher impedance.

The main hot loop in Figure 23 consists of the external MOSFETs Q1 and Q2 and the closest low impedance decoupling capacitor C7. This is the loop with the highest RF energy in a controller solution.

The Way Shielding Works

DC magnetic fields go through air, FR4 epoxy dielectric and copper almost undisturbed. AC magnetic fields are impacted only by the induced currents in a conductor, usually copper or tin, etc. So, absent from ferromagnetic material, we can focus on currents as the only source to alter or attenuate AC magnetic fields in a typical PC board environment.

We know from experiments that complete conductive enclosures have a very high attenuation – easily over 100dB – over a very broad frequency range. To enable high frequency (HF) measurements cookie boxes (widely used in the R&D community to shield sensitive circuitry) are a popular example. You can buy them in rectangular form to easily fit PC boards and HF connectors like BNC, N etc. For practical purposes, HF magnetic fields do not escape closed conductive boxes, as long as the wall is thicker than skin depth (see box).

If we blow up the conductive enclosure like a balloon, large enough that it becomes a flat wall between us and the AC current, the eddy currents in the shield material need to create an AC magnetic field, the opposite of the original AC current behind the wall (Figure 24). The eddy currents in the shield will only be enough to cancel any magnetic AC field to the outside of the box or, in this case, in the direction shown at the lower portion of Figure 25.

Shield Effectiveness

If the board copper plane was non-conductive, it would be transparent to any magnetic field like a sheet of paper. The current in the copper is the only influence on the magnetic field. The energy available for eddy currents is induced in the shield. Such currents will cancel any magnetic field inside the copper shield and outside in the direction away from the inducing current, within the limits of the skin and proximity effects (Figure 26).

The cancellation layer is the layer that cancels the magnetic field from the inducing currents (i.e. from the hot loop) and induced currents in the shield, so it is sort of midway between the AC currents in opposite directions.

The position of the cancellation layer can be estimated by rule of thumb and may help visualize how the remaining AC fields will look. The closer the cancellation layer is to the induced current layer, the better the cancellation. Inductance is the integral of the magnetic field – the same magnetic field that forms the near-field RF antenna. All of these effects are reduced when the cancellation layer is placed closer to the inducing current loop.

If the current returns through the plane, the situation is somewhat different (see Figure 27). Now the current in the plane is not only passively induced, but is the active return flow; it is forced to be same as the current in the top trace. The benefit is that the cancellation is now closer to the inducing trace, in this case halfway between the top layer

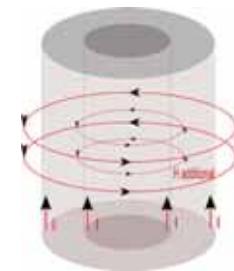


Figure 35: A pipe wall conducting all the current on its surface (the large diameter in the figure)

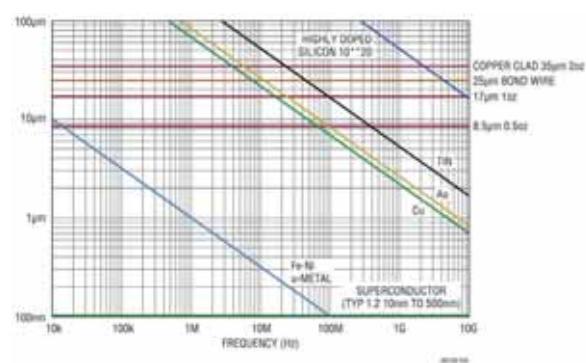


Figure 36: Skin depth over frequency for some materials

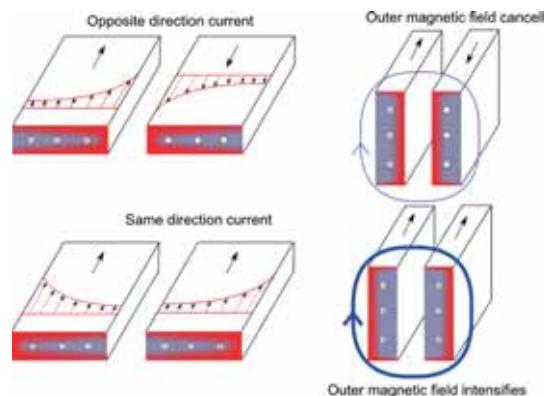


Figure 37: With opposite direction currents, the same forces attract them to each other

current and the returning current in the plane. Because the cancellation layer is now half the distance to the inducing current, it is safe to say that the magnetic field is now lower by at least a factor of two compared to the above situation with passive shielding only.

If possible, let the return current flow in the closest layer. Make its dielectric (isolation) as thin as practically possible. It is better to have the return current flow in the closest trace to the inducing current with minimum dielectric distance. That's what solid GND planes do by default.



Figure 38: High-frequency current density in a PC board trace on a single layer board

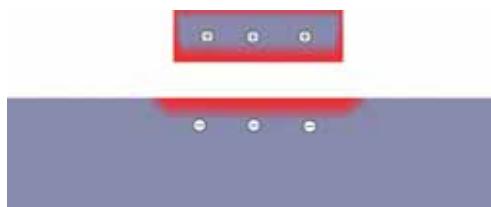


Figure 39: Adding a solid plane in a second layer, eddy currents will be generated in the plane, creating in total a mirror image of the current in the top trace

Standard multilayer boards often have much thinner outer layer dielectrics to help reduce EMI.

Line Conducted EMI Measurements

Figure 28 is an LT8611 with some input filtering with a ferrite bead and $4.7\mu\text{F}$ ceramics line conducted from 30MHz to 400MHz. The display line of -67dBm corresponds to 40dBuV.

Figure 29 shows an LT8610 power supply 13V in, 5V out at 1A out, line conducted up to 900MHz. In Figure 29 an additional wideband amplifier (LNA) in the HF signal chain with 35dB gain is used. So the -100dBm spectrum analyzer display line corresponds to -135dBm, which is the thermal noise floor of a 50Ω system with 10kHz bandwidth at room temperature. The main HF energy needed to be filtered out of the LT8610/LT8611 is below 400MHz. +10dBuV corresponds to $3.16\mu\text{VRMS}$.

First check the layer stack. Use a PC board of four layers, or more if possible. The second layer from top is typically only about $200\mu\text{m}$ distance, and a shield will cancel the hot loop much better than any shield over 1mm away in a dual-layer board.

In the hot-loop shield, the same current as in the top trace hot-loop runs as eddy current. Keep the layer-2 shield solid. Place vias away from the hot loop for connections to GND planes you want to keep quiet. The hot-loop shield cancellation currents create HF voltage across the loop, and you do not want to couple it with vias in areas you need quiet. This current decays with distance, but often remains a problem.

The challenge for filtering the input and, if required, the

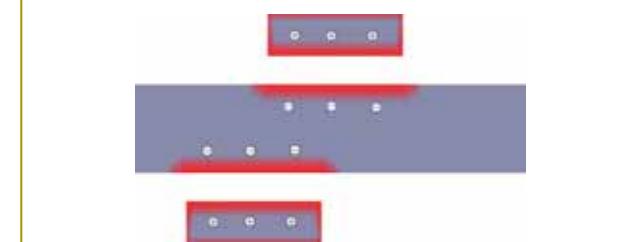


Figure 40: On multilayer boards, a plane will shield the AC currents

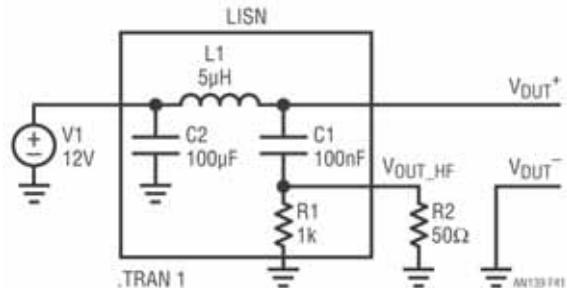


Figure 41: Non-symmetric LISN often used in automotive equipment

output is mainly in finding an area that is quiet enough. An effective way is to make a complete GND ring around the power supply unit (PSU) connected with vias. Filter capacitor GND return should be at the location where the V_{IN} current crosses the ring. There should still be filtering inductance in the direction of the hot loop. That can be a ferrite bead or an inductor. Beware of magnetic coupling between filter inductors and the main inductor; the transformer action can jeopardize your attenuation. Place filter inductors at a distance from the main inductor. Use short ceramic capacitors, i.e. 0402, or reverse geometry capacitors because the block capacitors need low equivalent-series-inductance (ESL), which mainly dictates their impedance. Shorter and thicker ones have lower ESL (see box).

Characteristic impedance of the strip lines you create with your V_{IN} traces is only a few ohms. The ESL of your block capacitors should be as low as possible. Use reverse geometry capacitors or a stack of 0402s closest to the filter point and larger cases close by. Any trace length significantly increases the few hundred pH inductance of your small block capacitors. Ensure the routing path of the V_{IN} and the return trace go through the filter capacitor pads; this avoids additional trace inductance.

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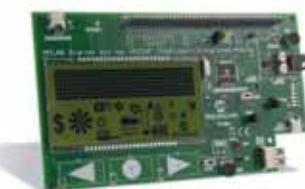
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NOVEL DESIGN OF INTERNAL POWER SUPPLY FOR HIGH-VOLTAGE DC-DC CONVERTER

LING-FENG SHI AND LING-YAN XU OF XIDIAN UNIVERSITY IN CHINA PRESENT A NOVEL, INTERNAL, POWER SUPPLY STRUCTURE FOR HIGH-VOLTAGE POWER MANAGEMENT IC TO SOLVE SUPPLY ISSUES LINKED TO THE INTERNAL LOW-VOLTAGE MODULE.

S

witching integrated DC-DC converters have become the solution of choice for power management in automotive electronics due to the advantages they offer, including high efficiency. However, new challenges are facing the converter design, brought on by the requirements for wide input voltages and load range in automotive, telecommunication and industrial systems, as well as battery-powered handheld devices. Both high and low power is needed for a general high-voltage DC-DC converter.

The high-input-power supplies energy to the internal high-side driver and other high-voltage modules, while the low internal-power supplies the internal low-voltage module. Therefore, a low-voltage internal power-supply is required to be generated from the high-voltage input inside the chip.

In order to overcome this problem, we suggest an internal power-supply structure for high-voltage buck DC-DC converters, which consists of a pre-bias and soft reference generating circuit, multiplex differential input linear regulator and a power grouping isolation circuit. The pre-bias and soft reference generating circuit provides bias current and soft reference voltage for the linear voltage regulator. After the 1.2V zero temperature coefficient voltage produced by a bandgap reference circuit is established, a soft reference voltage will automatically switch to a 1.2V reference voltage to make the linear regulator generate a precise internal power supply of 5V. By lifting V_{GS} (gate-source voltage), the power grouping isolation circuit produces four non-interfering analog, digital, power and bootstrap internal power supplies.

Power Supply System Analysis

The block diagram of a pulse width modulation (PWM) peak-current mode high-voltage buck DC-DC is shown in Figure 1. The circuit part enclosed with the dashed line is the chip's internal circuit, while the rest is the peripheral circuit. Analog circuits such as the error amplifier (EA) and PWM comparator need constant supply voltage under normal working conditions. Power modules like the low-side driver require relatively large transient currents, while the logic and other digital modules will make the supply voltage of hundreds of millivolts dithering. Therefore, several different internal power supplies are needed to power the different modules, and with good isolation too, to reduce mutual interference.

The internal regulator in Figure 1 is the power supply module of interest in this article, which produces four internal power supply lines V_{CCA} , V_{CCD} , V_{CCP} and V_{CCB} , to provide voltage to the analog, digital and power parts and bootstrap capacitor respectively. Since the capacitance is usually in the nF ballpark, the charging current will be relatively large. Therefore, another internal power supply is required.

Internal Power Supply Design

Figure 2 shows the pre-bias and soft reference voltage generating circuit. The MOS (Metal-Oxide Semiconductor) symbol with a slash at the drain represents the high-voltage MOS transistor. The bias circuit is a typical circuit generating bias current independent of the power supply voltage. A cascode structure is used in MP_1 - MP_4 , MN_1 - MN_4 to improve the Power Supply Reject Ratio (PSRR) and reduce the effect of channel length modulation on the bias current.

Assuming that MN_1 and MN_2 have the same width to length ratio (W/L) and the number of MN_1 is twice that of MN_2 , and assuming that the gate potentials of MN_1 and MN_2 are the same, Equation 1 can then be obtained:

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox} W/L}} + V_{THN} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K W/L}} + V_{THN} + I_{out} R_1 \quad (1)$$

where μ_n and C_{ox} are process parameters, V_{THN} represents the threshold voltage of the NMOS and I_{out} represents the bias current generated by the circuit. Ignoring the body effect, Equation 2 can then be obtained:

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox} W/L}} \left(1 - \frac{1}{\sqrt{K}} \right) = I_{out} R_1 \quad (2)$$

Therefore:

$$I_{out} = \frac{2}{\mu_n C_{ox} W/L} \times \frac{1}{R_1^2} \left(1 - \frac{1}{\sqrt{K}} \right)^2 \quad (3)$$

So, after the bias circuit establishes a stable working point, the bias current essentially becomes independent from the supply voltage.

The start-up circuit consists of MP_5 - MP_9 and MN_6 , where MN_6 is a high-voltage NMOS transistor. The current leakage of NMOS causes the gate potential of MP_6 to decrease, which in turn raises the gate potential of MN_4 , unbalancing the bias circuit and generating bias current. After generating the bias current, MP_5 lifts the gate potential of MP_6 by current mirror, shutting off MP_6 will complete the start-up process, consuming little static current.

The soft-reference provides voltage to the linear regulator to generate a rough V_{CCA} before the 1.2V bandgap reference voltage is established. After that the soft reference will automatically switch to the bandgap reference

voltage to generate a precise internal power supply of 5V through the application of a multiple differential-input linear regulator. Soft reference voltage is generated by the current I_{S00} flowing through MN7.

$$V_{Soft} = \sqrt{\frac{2I_{Soft}}{\mu_N C_{ox} (W/L)_{MN7}}} + V_{THN} \quad (4)$$

The required V_{Soft} voltage can be obtained by adjusting the value of the current I_{Soft} .

The Linear Regulator and Power Grouping Isolation Circuit

The multiple-differential-input linear regulator generates a precise power supply voltage of 5V through negative feedback. On the basis of this voltage, four groups of non-interfering internal power supply with different load ability are obtained by the method of lifting the V_{GS} grouping isolation.

The multiple-differential-input linear regulator and power grouping isolation circuit are shown in Figure 3. The dashed line shows the linear regulator circuit, with outside it is the grouping isolation circuit corresponding to each internal power supply.

The current I_{BLAS} generated by the pre-bias circuit provides bias current for the linear regulator. Before the precise reference voltage V_{BG} is generated by the bandgap circuit, the reference voltage is provided by V_{Soft} after which it automatically switches to the V_{BG} voltage through the structure of multiple differential pairs made of MP₁-MP₃. Thus a stable and accurate voltage V_{OUT} can be obtained by a negative-feedback structure controlling the conduction state of MN₄. The value of V_{OUT} can be expressed as Equation 5:

$$V_{OUT} = V_{BG} \left(1 + \frac{R_{FB2}}{R_{FB1}} \right) \quad (5)$$

The required output voltage value can be obtained by setting different values for R_{FB1} and R_{FB2} . As the input voltage can change from 3V to 24V, the device with high drain-voltage is used for the pass transistor and cascode mirror transistor. In our design, the buck of MP_1 , MP_2 and MP_3 is connected to the source of MP_8 . Due to the body effect, the threshold voltage of the multiple-differential-input pair transistors will increase, which ensures MP_1 , MP_2 and MP_3 work better in the saturation region.

The linear regulator amplifies in two stages. One of these stage's structures and open-loop DC (Direct Current) gain can be expressed:

$$A_{openloop} = g_{m(MN_1)} r_{o(MN_1)} g_{m(MN_2)} r_{o(MN_2)} \frac{g_{m(MN_1)}(R_{FB1} + R_{FB2})}{1 + g_{m(MN_1)}(R_{FB1} + R_{FB2})} \quad (6)$$

where $g_{m(MP3)}$, $g_{m(MN3)}$ and $g_{m(MN5)}$ represent the transconductances of MP₃, MN₃ and MN₅ respectively; and $r_{o(MN1)}$ and $r_{o(MN3)}$ represent the output impedances of MN₁ and MN₃ respectively.

The $PSRR$ of the linear regulator is expressed as:

$$PSRR = \frac{1}{\beta A_{out_pc}} \quad (7)$$

where β is the feedback factor and $A_{OL,DC}$ the DC gain of the open loop. By improving the open-loop's gain, the *PSRR* of the regulator can be increased, enhancing the rejection effect on the power supply's variances. The dominant

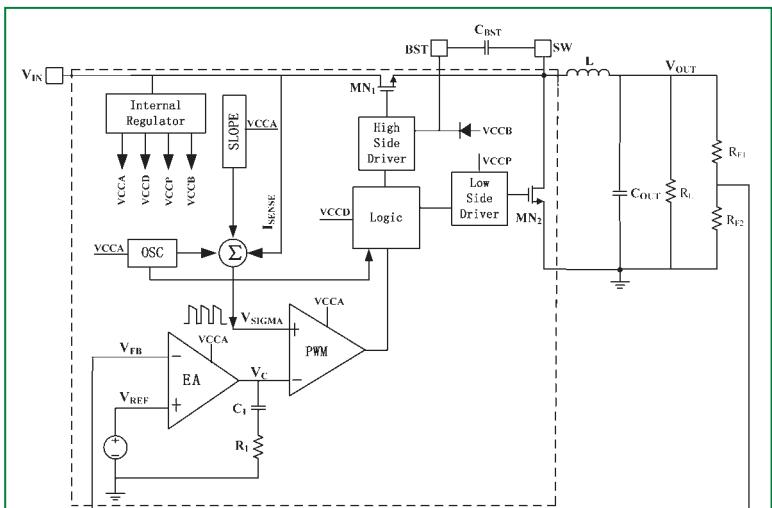


Figure 1: High-voltage buck DC-DC system frame

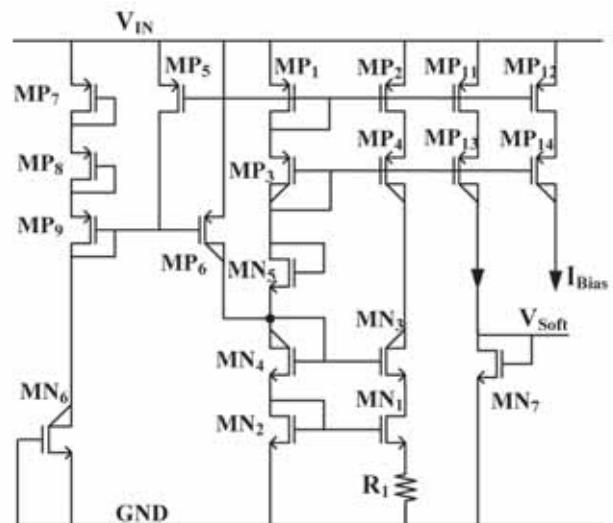


Figure 2: Pre-bias and soft reference-voltage-generating circuit

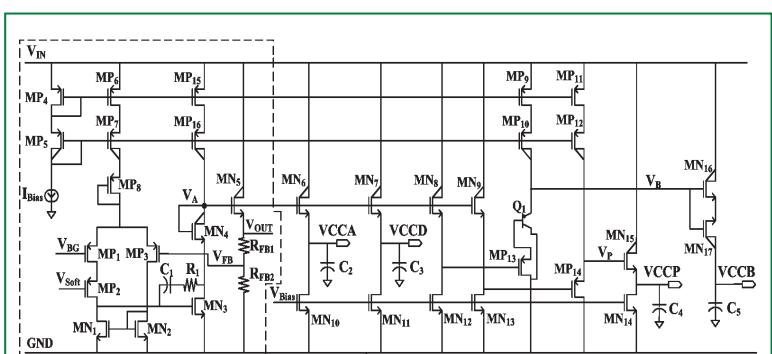


Figure 3: Multiplex differential input linear regulator and power grouping isolation circuit diagram

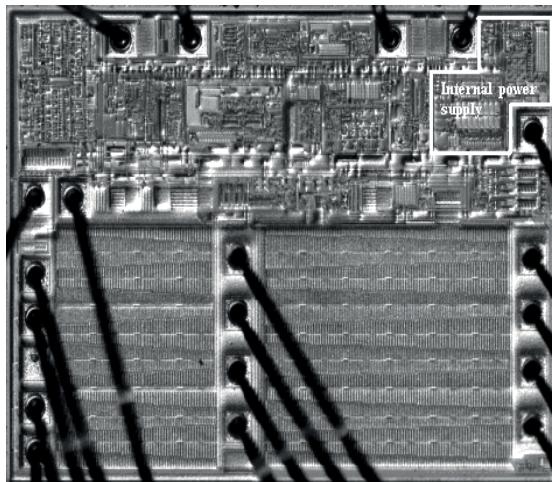


Figure 4: Micrograph of the high-voltage buck DC-DC converter

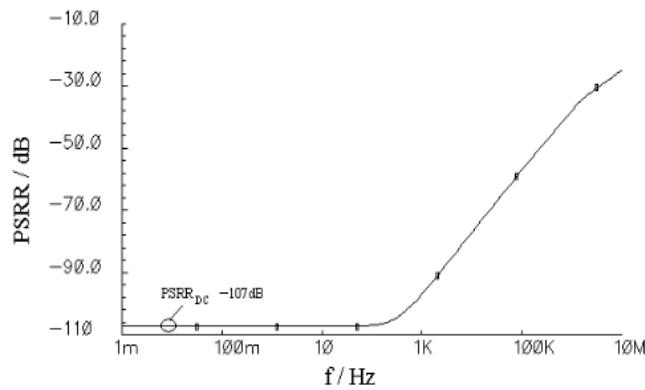


Figure 5: PSRR curve of multiplex differential input linear regulator

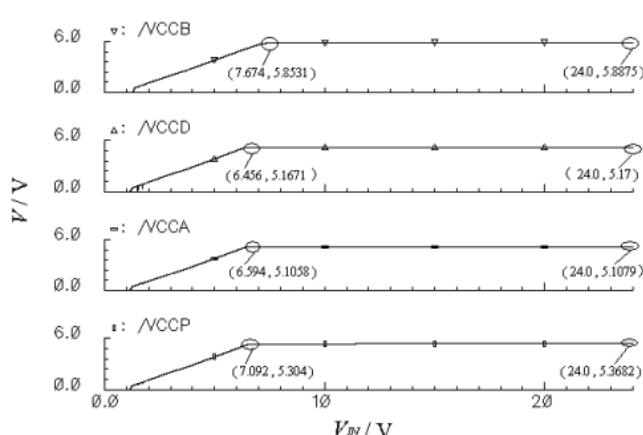


Figure 6: The curve of the internal power supply voltage that changes with the input voltage

pole at the gate of MN_3 has a value $f_o = 1/(2\pi r_{o(MN2)}g_{m(MN3)}f_{o(MN3)}C_1)$. C_1 is the Miller capacitor, which can force the dominant pole at low frequencies. A resistor R_1 is used to inhibit the bad influence caused by the Miller compensation. Loop gain of the regulator is up to 105dB and the phase margin is 82°.

Power Grouping Isolation Circuit

As different internal power supplies can interfere with each other, it is essential to group and isolate them. Here we lifted V_{GS} separately to obtain good isolation. It can be seen in Figure 3 that $VCCA$ and $VCCD$ are obtained by raising the V_{OUT} voltage by MN_5 , and then reducing the value of $V_{GS(MN6)}$ and $V_{GS(MN7)}$ through MN_6 and MN_7 respectively:

$$VCCA = V_{OUT} + V_{GS(MN_5)} - V_{GS(MN_6)} \quad (8)$$

$$VCCD = V_{OUT} + V_{GS(MN_7)} - V_{GS(MN_8)} \quad (9)$$

When the load current of $VCCA$ and $VCCD$ are relatively small, $V_{GS(MN5)}$ and $V_{GS(MN7)}$ can be considered to be approximately equal. Thus, the voltage of $VCCA$ and $VCCD$ will be almost the same as V_{OUT} . As the load currents of $VCCP$ and $VCCB$ are relatively large, additional isolation is needed. Similarly, with the method of lifting V_{GS} , Equations 10 and 11 are obtained respectively:

$$VCCP = V_{OUT} + V_{GS(MN_9)} - V_{GS(MN_8)} + V_{GS(MP_{14})} - V_{GS(MN_{15})} \quad (10)$$

$$VCCB = V_{OUT} + V_{GS(MN_9)} - V_{GS(MN_8)} + V_{GS(MP_{15})} + V_{RE(Q)} - V_{GS(MN_{17})} \quad (11)$$

When the load current is small and flowing through MN_{10} - MN_{15} , MP_{9} - MP_{10} , $VCCP$ will be approximately equal to V_{OUT} and $VCCB$ will be equal to $V_{OUT} + V_{RE(Q)}$. When the load current is relatively large, $VCCP$ and $VCCB$ do not change with the load current variation because of MN_{15} and MN_{17} 's large width-to-length ratios. V_{OUT} is typically set at 5V, making $VCCB$ larger than 5V by $V_{RE(Q)}$, which will improve the gate-source voltage and reduce the on-resistance of the upper-side power transistor, which improves the efficiency of the DC-DC converter.

MN_{17} is an inverted high-voltage NMOS transistor. The $VCCB$ voltage will be elevated to the value of $VCCB + V_{IN}$ once the upper-side power transistor is open, preventing an anti-sink current flowing from the $VCCB$ terminal to the input power through the parasitic drain-body diode by the inverted high-voltage NMOS transistor.

Simulation and Test Results

Using a 0.5μm 30V CDMOS process, the internal power supply structure presented in this article has been successfully applied in a high-voltage buck DC-DC converter. The circuit and layout design of the chip were achieved using Cadence and Hspice software and it's already taped out. Figure 4 shows the micrograph of this chip, with the section in the white box being the internal power supply circuit presented here.

The PSRR curve of the multiple differential-input linear regulator of the power supply is shown in Figure 5. The PSRR is up to -107dB, indicating the strength of the linear regulator's inhibiting effect on power changes.

The normal operating voltage range of this DC-DC converter is 4.5V to 24V. Figure 6 shows how the output voltage of each internal power supply changes when the input power supply ranges from 0V to 24V, and that the analog power $VCCA$, digital power $VCCD$, driver power $VCCP$ and bootstrap power $VCCB$ can start up normally.

After the internal power supply voltage is established at a set point, the analog power $VCCA$, digital power $VCCD$, driver power $VCCP$ and bootstrap power $VCCB$ only change 2.06mV, 2.87mV and 40.15mV respectively, in accordance with the varying input voltage V_{IN} . So, it can be seen that the internal power supply requiring high accuracy, such as $VCCA$ and $VCCB$, almost does not change with V_{IN} , and the power supply's output voltage consuming power such as $VCCP$ and $VCCB$ slightly increases with increments in the input voltage, but this is within the normal work tolerances of the chip.

Since the load transient variation of the driver supply may be quite large when the chip works normally, it can be seen that its amplitude varies around 350mV when the input voltage V_{IN} is 12V, and the load current changes in the range of 1~10mA in 100ns (see Figure 7). However, the variations in the analog $VCCA$, digital $VCCD$ and bootstrap $VCCB$ are lower than 1mV, which indicates that the transition variation of one internal power-supply has almost no effect on the others. It shows that the suggested circuit provides good isolation and interference shielding.

Figures 8 and 9 show the test waveforms of the chip in normal operation conditions, while the input voltage V_{IN} is 12V and 24V respectively. The output voltage V_{OUT} is 3.3V and load current I_L is 2A. It can be seen that the DC-DC converter works well in case of both lower and higher input voltages, which also reflects the excellent characteristics of the internal power-supply's circuit. ●

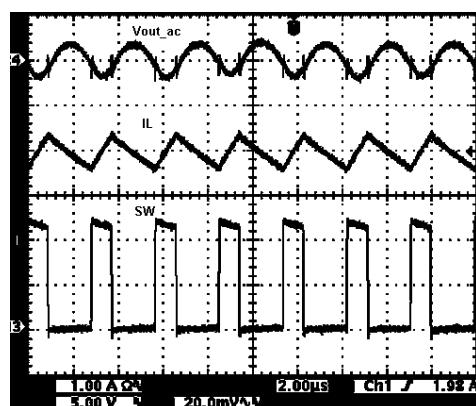


Figure 8: Working waveforms of the chip when $V_{IN} = 12V$, $V_{OUT} = 3.3V$, $I_L = 2A$

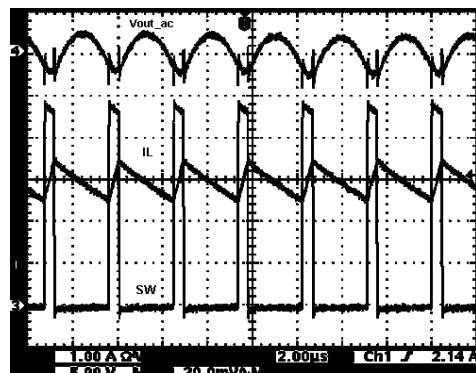


Figure 9: Working waveforms of the chip when $V_{IN} = 24V$, $V_{OUT} = 3.3V$, $I_L = 2A$

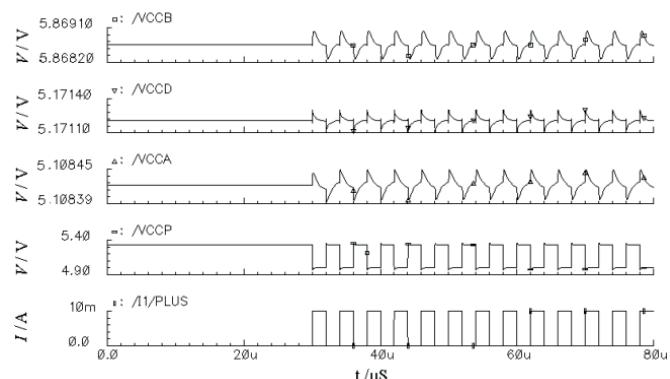


Figure 7: The curve of each internal power output voltage's variation when the load of the driver power changes transiently

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LOW-POWER LED LIGHTING APPLICATIONS: A POWER-MANAGEMENT TECHNIQUE

EZANA HAILE, PRINCIPAL APPLICATIONS ENGINEER AT MICROCHIP TECHNOLOGY'S ANALOG & INTERFACE PRODUCTS DIVISION GIVES A PRACTICAL APPROACH TO EFFICIENTLY AND COST-EFFECTIVELY LIGHTING AND DIMMING A BANK OF LEDs

When a set of LEDs is controlled, LED luminosity versus electrical power is a key specification in determining the quality of visible light. In low-power applications, illuminating an entire set of LEDs simultaneously to achieve the maximum luminous level may not be possible, due to the limited current source. The power dissipation per LED must be managed efficiently, to produce optimum luminosity from the low-power source. This requires a power-management technique where, in a set of LEDs, only one bank of LEDs is powered for a given time. This time interval is managed to achieve the required luminous intensity, without visually detecting the alternating banks of LEDs.

Application Specific

In order to determine the number of LEDs for a given

time interval, the available power and the luminous intensity must be determined for the application. The LED datasheet must be carefully reviewed for luminous intensity versus forward-current characteristics, to select LEDs that meet the required intensity level. Once the number of LEDs needed to achieve the required level of luminosity from the application is determined, then the number of LEDs that can be powered at a given time-interval is determined by taking the ratio of the total current required for the LEDs and available current, as follows:

$$\text{# of LEDs in a bank} = \frac{\text{Total Required Current for LEDs}}{\text{Total Available Source Current}}$$

Additionally, the frequency at which the bank of LEDs is turned ON/OFF must be tuned. The ON time is long enough

for full illumination of a bank, and the OFF time is limited by the time it takes before the bank of LEDs start to visibly dim. The OFF time limits the number of additional LED banks that can be controlled in the application while the first set is in the OFF state. Therefore, the OFF time limits the number of banks that can be controlled with time-interval management.

A low-cost implementation of this technique requires a clock source, digital flip-flops to control banks of LEDs and an OR gate to detect a start condition with a simple On/Off switch. Figure 1 shows a block diagram of a D flip-flop configuration to control four banks of LEDs.

Initially, the flip-flop is in a no-change state and requires a start pulse. The duration of the start pulse must be at least once clock-cycle, so that it can be detected by the first flip-flop at the rising edge of the clock cycle. The duration of the start signal must

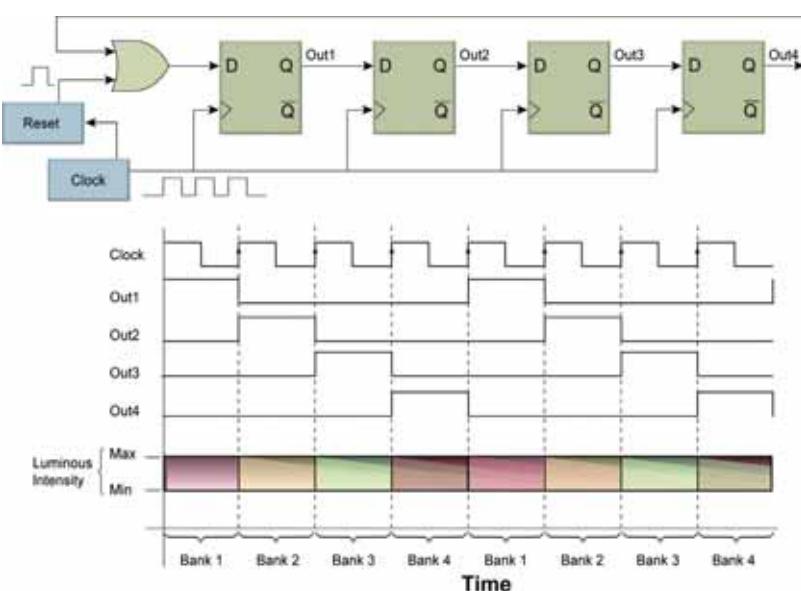


Figure 1: LED lighting time-interval using a flip-flop circuit

be momentary – it cannot be longer than one clock cycle, otherwise the first two flip-flop outputs will be set at the same time and, since the source current is limited, the lighting application will not function properly. Therefore, with this configuration at the rising edge of every clock cycle, a bank of LEDs is fully illuminated. However, to the human eye it appears as though all LEDs are fully turned on simultaneously.

The limitation of this implementation is that it is monotonic and does not provide design flexibility. It only has an on or off state. For some applications, such as LCD backlights, this circuit may be adequate. However, if dimming or pattern generation is needed, a microcontroller (MCU) based circuit provides the greatest flexibility with minimum impact to the total cost of the solution. The circuit is also simpler to build, with fewer components. The MCU controls each bank of LEDs and it can also detect user inputs for dimming control and pattern selection.

A Cost-Effective Example

One example of a cost-effective implementation is to use a low-cost and low pin-count 8-bit microcontroller, such as Microchip's PIC10F or PIC12F family, with an I/O port expander such as Microchip's MCP23018. I/O expanders can also be useful for driving LEDs, when the lighting circuit is remotely located with respect to the MCU.

I/O port expanders are devices that are used to expand the I/O ports of a microcontroller. In this application, the MCU controls the I/O expander ports via the I²C protocol, to drive the LEDs on or off. The MCU's I/O pins can be used to detect user inputs via a push-button switch, or by utilizing the built-in analog-to-digital converter (ADC) to detect a potentiometer level for dim control.

I/O expanders are available with open-drain or push-pull output configurations. With today's microcontrollers operating at 3.3V or lower, an open-drain-output I/O expander lends itself well to this application. The advantage of using an open-drain-output I/O expander is that it permits the LEDs to operate at 5V or higher, while the microcontroller and the I/O expander are powered at a lower voltage. The MCP23018 is a 16-bit I/O port expander with an open-drain output and an I²C interface. Figure 2 shows a circuit diagram for an open-drain-output I/O expander pulled up to a voltage higher than the MCU's supply voltage.

In this case, when the I/O port is set low, then the voltage at the I/O expander port is 0V and current

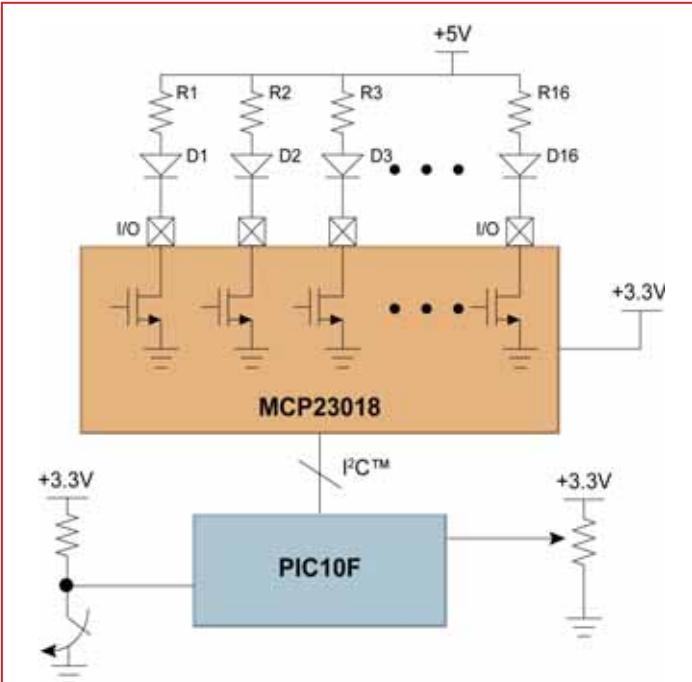


Figure 2: Low-cost, microcontroller-based lighting solution using I/O port expander

flows, which forward biases and turns on the LED. The LED-biasing resistor, which also functions as a pull-up resistor for the open-drain output, limits the current to the LED for the required luminous intensity.

When the I/O-expander output port is set high, the open-drain output is off or high impedance and the voltage at the I/O expander port is pulled up to 5V by the pull-up resistor. This is an off state for the LED, because current will not flow.

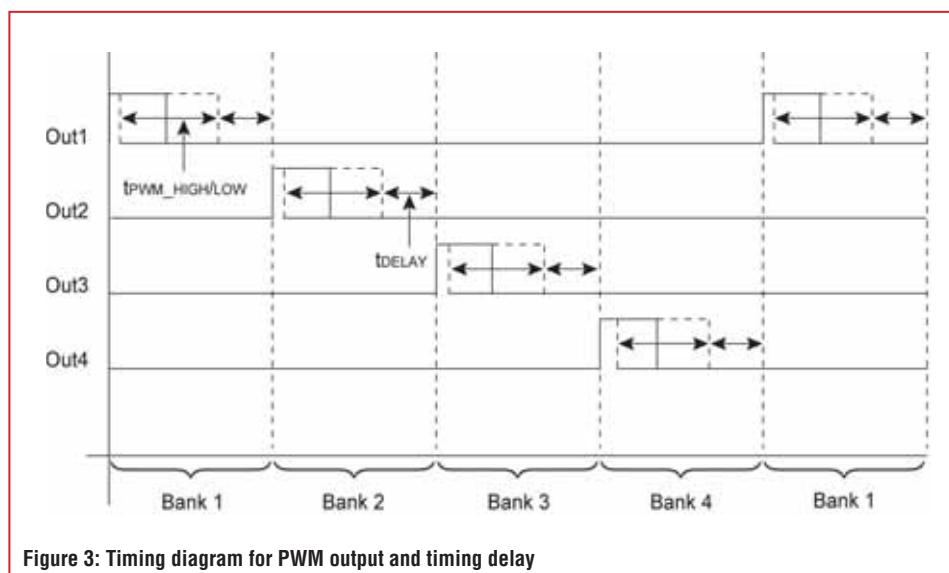
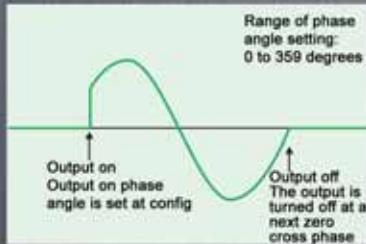


Figure 3: Timing diagram for PWM output and timing delay

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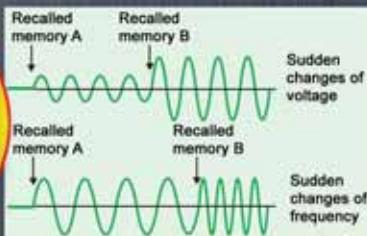
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0 ~ 650V 0 ~ 3.5A

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PWX1500MH

PWX1500H

Output Range

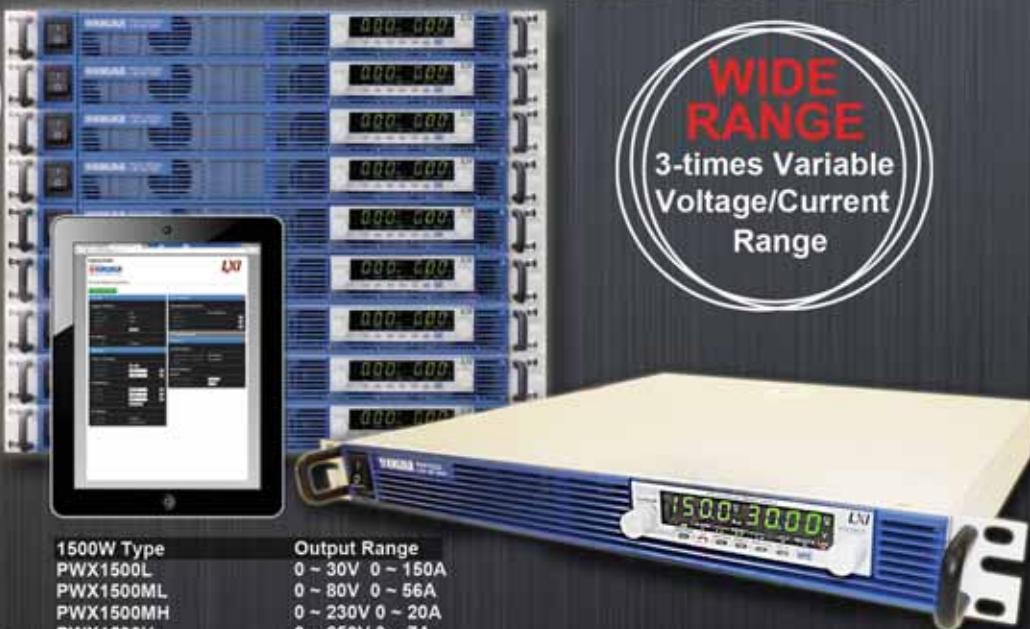
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Another advantage to an open-drain output configuration is that when the port is configured as high impedance, it takes longer for the LED to turn off due parasitic capacitance. This enables the next bank of LEDs to turn on for slightly longer duration, when compared to similar applications with push-pull output.

The MCP23018's 16 I/O ports can drive up to 16 LEDs. The I/O expander's output drive capability also limits the amount of current that can be sunk into the I/O port when the LED is fully turned on. The I/O port's low-level voltage is specified as 0.6V maximum at 8.5mA of current. If the current is higher than 8.5mA, then the low-level voltage will exponentially increase and the absolute maximum current is specified as 25mA.

For example, if the source current is limited to 5V/50 mA, and if approximately 2mA is budgeted for the microcontroller, the I/O expander and the resistors for user-input detection, then the rest of the available current can be dedicated for LED lighting. If the luminous intensity of the LED at approximately 10mA is adequate, then four LEDs can be controlled per bank. And, the current-limiting resistor value will be approximately 440Ω.

The timing shown in Figure 1 can be replicated using a relatively short MCU instruction code. For example, referring to the Pseudo Code 1, the main subroutine can be an infinite while-loop. At the MCU timer intervals (Timero) an interrupt service routine sends an I²C command to the I/O expander to turn on only one bank of LEDs. The interrupt service routine counts or keeps track of the LED bank status, such as the bank that is currently turned on, and the corresponding I/O expander port configuration as high or low. Initially or after the MCU resets, on the first Timero interrupt, bank 1 is turned on; on the second interrupt, bank 1 is off and bank 2 is on. Then, on the third interrupt, bank 2 is off and bank 3 is on. Finally, on the fourth interrupt, bank 3 is off and bank 4 is on and the bank counter variable is cleared. On the next interrupt, the cycle repeats by turning on bank 1 and turning off bank 4. Other variables, such as Command_byte, Address_pointer_bank1n2 and Address_pointer_bank3n4 are constants defined in the header file. With such an implementation, the circuit outputs the required luminous intensity and it appears that all LEDs are turned on simultaneously from the available power-source.

LED Pattern Generation and Dimming Control

With a microcontroller-based application, interesting lighting patterns can be easily generated. The I/O port expander's output states are loaded from 2 bytes of RAM variables, labelled as Bank1n2_pattern and Bank3n4_pattern. The nibble of each byte corresponds to each bank. A predefined look-up table contains various patterns of 1s and 0s for each bank. An 'IF THEN' statement is added to the MCU code (the main subroutine's infinite while-loop) to continuously monitor

```
void main(Void){
    initialize(); //Initialize the PICmicro peripherals including Timer0, and I/O expander peripherals
    bank_counter = 0; //Clear the bank counter variable
    while(1){ //Infinite while loop
    }
    Void Interrupt int_service(void){
        TurnOffAll_LEDs(); //subroutine to turn off all previously lit LEDs
        I2C_start(); //I2C protocol - start signal subroutine
        I2C_send(Command_byte); //I2C protocol - send byte subroutine

        If(bank_counter == bank1){ //bank1 is a constant defined as 0
            I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
            I2C_send('0000 1111'); //I2C protocol - send bank status (bank 1 on and bank 2 off)
            bank_counter = bank_counter + 1;
        }
        If(bank_counter == bank2){ //bank1 is a constant defined as 1
            I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
            I2C_send('1111 0000'); //I2C protocol - send bank status (bank 2 on and bank 1 off)
            bank_counter = bank_counter + 1;
        }
        If(bank_counter == bank3){ //bank1 is a constant defined as 2
            I2C_send(Address_pointer_bank3n4); //Send peripheral register address pointer
            I2C_send('0000 1111'); //I2C protocol - send bank status (bank 3 on and bank 4 off)
            bank_counter = bank_counter + 1;
        }
        If(bank_counter == bank4){ //bank1 is a constant defined as 3
            I2C_send(Address_pointer_bank3n4); //Send peripheral register address pointer
            I2C_send('1111 0000'); //I2C protocol - send bank status (bank 4 on and bank 3 off)
            bank_counter = 0;
        }
        I2C_stop(); //I2C protocol - stop signal subroutine
    }
}
```

Pseudo Code 1: Microcontroller interrupt service routine code

```
*
*
*
If(bank_counter == bank1){ //bank1 is a constant defined as 0
    I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
    Bank1n2_pattern = ~Bank1n2_pattern; //complement the variable using ~
    I2C_send((Bank1n2_pattern | '0000 1111)); //I2C protocol - send bank status
                                                //use OR '|' to set bank 1 on and bank 2 off
    bank_counter = bank_counter + 1;
}
*
*
*
```

Pseudo Code 2: Pattern generation

```
*
*
*
Void Interrupt int_service(void){
    TurnOffAll_LEDs(); //subroutine to turn off all previously lit LEDs
    If(Delay_ON == ON){ //ON is a constant defined as 1
        Update_Timer0_Counter(Timer0delay_interval); //subroutine to update Timer0
                                                //Timer0delay_interval is a constant to set the minimum delay
        Delay_Counter = Delay_Counter - 1; //count down the number of interrupts for delay
        If(Delay_Counter == 0){
            Delay_ON = OFF; //Clear the delay flag for the next interrupt
            Delay_Counter = Get_Delay_Counter(); //subroutine to detect user input
                                                //and set the delay counter variable
        }
        else{
            Delay_ON = ON; //leave delay flag ON
            Return; //exit the interrupt service routine
        }
    }
    I2C_start(); //I2C protocol start signal subroutine
    I2C_send(Command_byte); //I2C protocol - send byte subroutine

    If(bank_counter == bank1){ //bank1 is a constant defined as 0
        I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
        Bank1n2_pattern = ~Bank1n2_pattern; //complement the variable using ~
        I2C_send((Bank1n2_pattern | '0000 1111)); //I2C protocol - send bank status
                                                //use OR '|' to set bank 1 on and bank 2 off
        bank_counter = bank_counter + 1;
        Delay_ON = ON; //turn on the delay flag
    }
}
*
```

Pseudo Code 3: Delay code implementation to view the lighting pattern

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HP	5361B	Pulse/Microwave Counter – 26.5GHZ	£1,500	MARCONI	6210	Reflection Analyser for 6200 Test Sets	£1,500
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HP	54600B	Oscilloscope – 100MHZ 20MS/S from	£195	MARCONI	TF2167	RF Amplifier – 50KHZ-80MHZ 10W	£125
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HP	8560A	Spectrum Analyser synthesised – 50HZ -2.9GHZ	£2,100	R&S	SMT06	Signal Generator – 5KHZ-6GHZ	£4,000
HP	8560E	Spectrum Analyser synthesised – 30HZ-2.9GHZ	£2,500	R&S	SW085	Polyscope – 0.1-1300MHZ	£250
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the push-button switch on/off state. When the push-button is momentarily pressed, a pattern from the look-up table is loaded in the two bytes of RAM, labelled as Bank1n2_pattern and Bank3n4_pattern. When the Timero interrupt occurs, the new pattern is sent to the I/O expander and the LEDs are lit according to the pattern. The main subroutine cycles through the look-up table, as the push-button switch continues to be momentarily pressed by the user. To display an alternating light, simply

11 In low-power applications, LEDs can be controlled by managing the time interval for each bank of LEDs, for efficient illumination

send the complement of the previous pattern. For example, if the bank1 pattern is '0101' then the complement is '1010,' as shown in Pseudo Code 2, which is a snippet from Pseudo Code 1.

However, a delay must be added to visually inspect the alternating patterns. The delay is added in the interrupt subroutine, before the bank on/off 'IF THEN' statements. To do so, add a Delay_ON flag, so that on the following interrupt, only a delay counter is decremented to count down the number of interrupts for delay. The delay value can also be a user-selected value using a potentiometer, where the centre tab is connected to the MCU's on-chip ADC input. The ADC's digital data is scaled from minimum to maximum delay by simply detecting the top four bits, which provide 16 levels. A finer ratio can be set by detecting the top five bits, or 32 levels. The maximum delay is the slowest the LEDs can blink and, with minimum delay, it appears that all LEDs are fully turned on. The timing diagram in Figure 3 shows the delay position, t_{DELAY} .

The dim control uses pulse-width modulation (PWM) to control the duration for the time-interval of each bank. In this case, the Timero interrupt duration will have two values, one for high duration and another one for low duration, proportional to the PWM percent ratio. The ratio is set using a thumb-wheel potentiometer and the centre tab is connected to the ADC input. The resolution level can be adjusted by selecting the top 4 or 5 bits from the ADC.

The Timero counter position is adjusted ratiometrically, with the scaled ADC data (where the 100% PWM is equal to the maximum counter position) fully lit, and 0% minimum or lowest dim level. Pseudo Code 4 shows the PWM scaling equation for 16 levels, and Figure 3 shows the timing diagram for the PWM duration, $t_{\text{PWM_LOW}}$ and $t_{\text{PWM_HIGH}}$. In this case, the interrupt service routine has to update the Timero counter positions for the next interrupt. It also has to detect whether the duration is for PWM high or low time. Therefore, in addition to detecting the LED bank states, a few instructions must be added to detect the potentiometer level for dim control and ratiometrically scale the Timero counter position with the PWM_High and PWM_low values shown in Pseudo

code 4. Pseudo Code 5 shows the code for adjusting the PWM; an 'IF THEN' statement is used to detect the PWM state.

This methodology can also be implemented on a mid-range 8-bit microcontroller with additional program memory, such as Microchip's PIC16F family. The upgrade enables the main subroutine to handle sophisticated lighting patterns, such as chase lights. The MCU's Timer1 module can be utilized to vary the duration where the two RAM bytes are updated for the chase pattern.

Efficiently Driving LEDs

In summary, while there are many ways to efficiently drive the banks of LEDs used in LCD backlights or lighting-pattern applications, designers are always looking for novel ways to cut costs without compromising performance.

In low-power applications, LEDs can be controlled by managing the time interval for each bank of LEDs, for efficient illumination. In addition, low pin-count microcontrollers and I/O port expanders provide a low-cost alternative for lighting solutions with great design flexibility. ●

```
Void get_PWM_ratio(void) {
    Double PotScale;           //local variable to store ADC output scale
    Double PWM_Percentage;    //local variable to store PWM change percentage

    PotScale = (ADRESH)/16 + 1; //Scale ADC output high byte
    PWM_Percentage = 1/16 * PotScale; //Scale the output from 0 to 1, equivalent to 100%
    PWM_High = Frequency_counter * PWM_Percentage; //set PWM high Timer0 value
    PWM_Low = Frequency_counter * (1 - PWM_Percentage); //set PWM low Timer0 value
    //PWM_High and PWM_Low are global variables,
    //and Frequency_counter is a constant Timer0 value to set frequency.
}
```

Pseudo Code 4: Subroutine to calculate PWM ratio

```
*
*
*
If(bank_counter == bank1){ // bank1 is a constant defined as 0
    If(PWM_High_Low_flag == OFF){ //check PWM status flag
        get_PWM_ratio(); //Detect user input for PWM ratio
        Timer0_counter = 65535 - PWM_High; //set Timer0 counter variable
        Update_Timer0_Counter(Timer0_counter); //subroutine to update Timer0
        I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
        Bank1n2_pattern = ~Bank1n2_pattern; //complement the variable using '~'
        I2C_send(Bank1n2_pattern | '0000 1111'); //I2C protocol - send bank status
        //use OR '|' to set bank 1 on and bank 2 off
        PWM_High_Low_flag = ON; //Set flag
        Delay_ON = OFF;
    }
    else{
        Timer0_counter = 65535 - PWM_Low; //set Timer0 counter variable
        Update_Timer0_Counter(Timer0_counter); //subroutine to update Timer0
        I2C_send(Address_pointer_bank1n2); //Send peripheral register address pointer
        I2C_send('1111 1111'); //I2C protocol - turnoff all LEDs
        bank_counter = bank_counter + 1;
        PWM_High_Low_flag = OFF; //Clear flag
        Delay_ON = ON;
    }
}
*
```

Pseudo Code 5: Code flow for PWM ratio setting

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Recent years have certainly seen rapid development in testing and sample analysis; further advancements have also been made in medical diagnosis technology. Part of this progress can be attributed to improvements in rechargeable lithium-ion batteries, which have allowed medical devices to cross the chasm into the portable and wearable sector.

Doctors, emergency services and patients have benefitted, with countless lives being saved or improved, but a recent consumer trend has raised concerns. Our pocket pal, the mobile phone, has experienced even faster product

development lifecycles, with new iterations available every six to ten months. The increased dependency on our smartphones has resulted in a wave of portable medical devices that can connect directly to the phone, with apps offering on-the-spot diagnosis. Heart rate and blood pressure monitors are already extensively used in tandem with mobile phones and tablets. More complex devices for patients with chronic diseases, such as glucose meters for diabetics, pulse oximetry and kidney infection machines, as well as ultrasound wands and smart fitness monitors, have all flooded the market.

Vital Reliability

At first, this seems like a great innovation; on deeper inspection, however, problems arise. In isolation, the emergence of new technologies empowers consumers with increased transparency in health monitoring. In reality, the convergence of professional portable equipment used by doctors and cheap consumer devices used by anyone poses the possibility of an unregulated self-diagnosis society. We could see potentially unsafe and unreliable devices being used to self-diagnose and self-treat. Any trend in the consumer market would, inevitably, have a competitive knock-on effect on professional use, and the proliferation of sub-par devices could put lives at risk.

At the heart of the issue lies the power supply. On a typical day, a paramedic may report for a 24-hour shift, ensure the equipment is charged and ready to use before undertaking emergency calls. Throughout the day, a device may be turned on and off several times and withstand the bumps and knocks present in a high-pressured environment.

The consequences of a battery failing during medical use could, quite literally,



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An essential component of portable medical technologies is the power source which usually comes in the form of a battery. This must be as small and light as possible, so as not to impede the user's daily activities

be life threatening. A failing lithium-ion battery may not be immediately noticeable but may become unreliable over time as overcharging and overheating could lead to a risk of failure or even combustion. This is relatively common in poorly tested, often consumer-focused batteries, but extremely unlikely in professionally-designed smart batteries.

Joint Solution

In contrast to the short product-life-cycles of smartphones, medical devices can be expected to endure periods of up to a decade without re-development. The stark reality is that cell technology used in such devices will become obsolete long before the product is discontinued. If we are to eliminate the medical risk, it is essential that battery solutions are designed into the product at the conceptual stages, rather than being relegated as an afterthought.

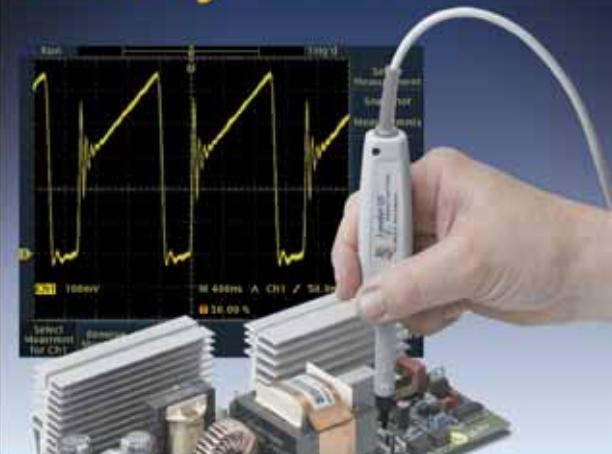
The rise of portable medical devices also raises concerns within regulatory circles. There are strict testing requirements for lithium-ion batteries to ensure that they remain safe whilst being transported, stored, charged, discharged and even when electrically or mechanically abused.

Smartphone use isn't going away, and portable medical use is becoming an increasingly serious proposition, so why inhibit either? Rather, use the benefits of both and minimise the burdens and shortcomings of each.

An effective solution in which the two areas can co-exist, is using the smartphone to complement the medical technology; this could be to log and share data over the – improving – cellular networks. Similarly, smartphones could be used as a secondary monitor to give additional information and utilise their increasingly powerful processors to perform non-vital diagnoses, supporting medical staff.

So the next time your doctor starts using a mobile phone in an emergency – don't panic! They are most likely checking your vitals and not your Facebook page. ●

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ZIGBEE AT THE HEART OF MODERN WIRELESS NETWORKS

IVAN SKORYK FROM DURBAN UNIVERSITY OF TECHNOLOGY (DUT) DESCRIBES THE ZIGBEE STANDARD AND ITS USE IN A VARIETY OF APPLICATIONS

There are many ways to organize a wireless network nowadays. One way is to use ZigBee, which offers an extensive coverage range, as each node in the network can work as a relay. This technology shows a number of advantages compared to other wireless technologies, such as Bluetooth and WiFi for example, making it highly suitable for a wide range of applications.

ZigBee

The ZigBee technology is based on the IEEE 802.15.4 standard. It operates in the industrial, scientific and medical (ISM) radio bands: 868MHz, 915MHz and 2.4GHz. Its transmission data rate can vary from 20kb/s up to 250kb/s, depending on the frequency band. The standard can also be used in wireless personal area networks (WPANs) and wireless local area networks (WLANs). The wireless space occupied by ZigBee in the IEEE 802 map, along with other IEEE standards, is shown in Figure 1.

ZigBee is a short-range wireless standard, using low transmission power, which in turn has an effect on the longevity of the devices' battery life. The standard specifies a nominal transmitter output power of -3dBm (0.5mW), with the upper limit controlled by the regulatory agencies of the region in which it is used. A single ZigBee node with transmitting power of -3dBm is able to provide communication of 10-100m, depending on the environment, antenna and operating frequency band.

Due to the nature of the ZigBee technology, even the basic IEEE 802.15.4 transmitter can be used to create sophisticated multi-node networks with flexible functions. Depending on the data latency requirements, a ZigBee network can use dozens of nodes, providing a (cumulative) coverage range of hundreds to thousands of meters.

Network Organization

ZigBee allows three different types of networks configurations: star, cluster tree and mesh (see Figure 2).

The flexibility of network building with ZigBee allows individual client devices to conserve battery in certain applications.

The star networks are most common, as they are convenient for relatively small physical environments which require a central node to be used as a personal area network (PAN) coordinator. The PAN coordinator controls and distributes data traffic for the entire network, driving all full-function- and reduced-function devices or nodes.

For larger physical environments, the cluster tree is a good way

to aggregate multiple basic-star networks into one larger network; however, such a network still requires a PAN coordinator node.

Some applications will make best use of the mesh structure, which provides alternate route flexibility and the capability for the network to heal itself when intermediate nodes are removed or RF paths change. In a mesh network the PAN coordinator node works not only as a router but a synchronizer across widely dispersed networks, to preserve battery lives of the networked devices.

Figure 1: The IEEE 802 wireless-space map

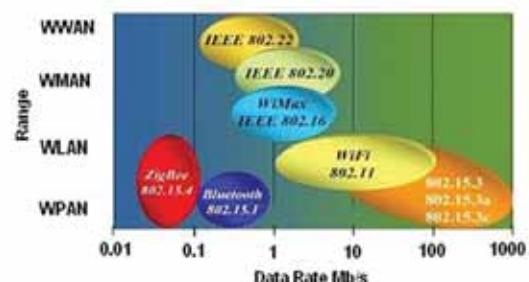


Figure 2: Three common configurations of a ZigBee network

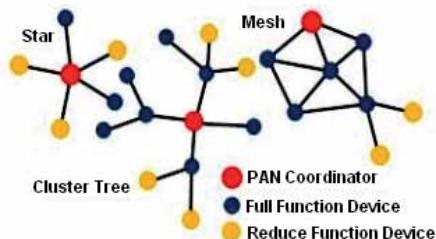
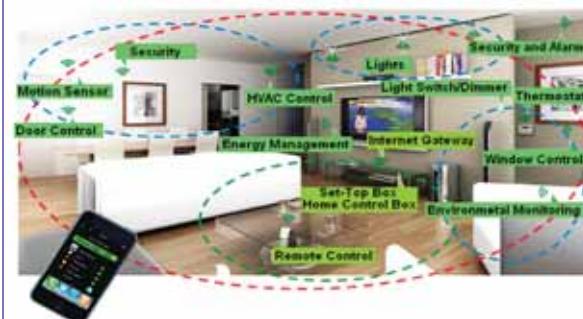


Figure 3: ZigBee in home automation



Applications

The ZigBee technology can find many applications, including:

- Remote equipment monitoring;
- Active RFID or asset tracking and telemetry;
- Security systems;
- Wireless audio;
- Industrial sensors and control;
- Home automation (Figure 3);
- Commercial and industrial automation;
- Medical equipment;
- Automotive networks.

As seen in the Figure 3, a room equipped with the ZigBee mesh network enjoys control of all the devices within it and it doesn't require a designer to implement any special remote control systems to run it. The most convenient feature of ZigBee is that it can be driven by any modern media device that supports this standard.

Radio Frequency Unit

Today, a lot of manufacturers produce fully assembled radio-frequency (RF) ZigBee modules with an embedded microcontroller unit (MCU) placed on tiny printed circuit boards (PCBs), see Figure 4. Such RF modules can be equipped with an onboard printed antenna loop for relatively short communication ranges, or an antenna connector to allow use of an external antenna for a longer communication range.

In case of insufficient functionalities or capabilities of the RF module's embedded MCU, an external auxiliary microcontroller unit can be connected for added functionality.

Figure 4: ZigBee RF modules



Benefits

Benefits of using ZigBee include:

- Reliable, self-healing and secure data transmission;
- Fully interoperable with other modern standards;
- The support of a large number of nodes and different network configurations;
- Easy to deploy and use;
- Long battery life;
- Low cost;
- Can be used globally;
- It uses plug-and-play RF modules without needing technical assistance.

These benefits make ZigBee an ideal technology for building wireless networks for many applications and environments. Its low cost and short project-development times make it highly suitable for various custom applications. Its low power usage extends battery life, which is especially important for portable or mobile devices. ●



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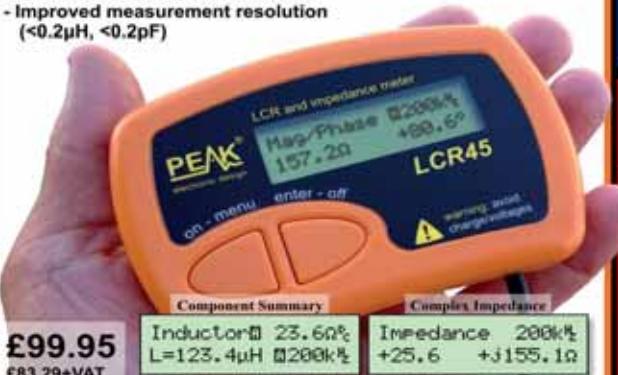
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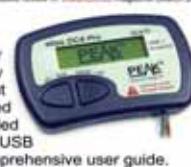


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How to Detect Movement with the Arduino

BY JOHN NUSSEY

A

passive infrared (PIR) sensor is used to detect movement and as such it is commonly found in commercial buildings and some homes. It registers heat given off by people, animals and other heat sources, similar to the sensor found in digital cameras. Most commonly it is used for motion detection in burglar alarms, where instead of detecting motion, it detects changes in temperature.

PIR Sensor Project

For this project you can buy the sensor, which will most likely come with a basic, ping-pong-ball style lens and a bare circuit board. There is always the option to take apart a PIR burglar alarm, which will be pre-packaged with a lens and sensor.

During the planning stages, the following aspects will need to be considered:

- **Complexity:** It can be tricky to hack an existing PIR sensor made for a specific system. As it needs to communicate with that system, it has clearly marked connections on the back.

One of the benefits of using an existing sensor is that it is pre-packaged, which reduces the amount of time needed to put the components together. Pre-packaged systems are designed

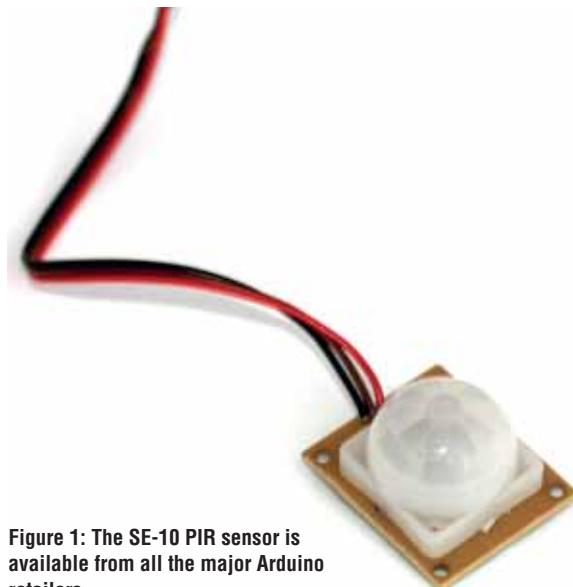


Figure 1: The SE-10 PIR sensor is available from all the major Arduino retailers

for easy installation and allow manual calibration. Using a PIR sensor that is not pre-packaged should be a lot more straightforward hardware- and software-wise but might require careful thought concerning the housing. Some PIR sensors have their own on-board logic and operate like a switch, going HIGH when movement occurs. This kind of sensor needs calibration to identify change from the norm.

- **Cost:** A household PIR sensor costs between \$15 and \$45 (£10 and £30). The main expense is the housing, usually designed to be discreet or look suitably high-tech. Bare PIR sensors cost a fraction of the price at around \$10 (£6.50), but need a suitable housing to be of any real use.

- **Where:** Many premises allow to neatly fit the sensor against a wall, or it may be mounted on a mini tripod for direction. These tripods may come with a suction-cup for fixing it to slippery surfaces such as glass.

At this stage, the PIR sensor will only need power. They calibrate themselves based on what they can see and then send a HIGH or LOW value when they detect change. This makes them extremely easy to program because you are dealing with the same signals as with a push-button.

PIR Sensor Example

In this example, we are using the SE-10 (see Figure 1), a PIR sensor available from all the major Arduino retailers. This particular device has three wires: red, brown and black. The red wire is the power source and should be connected to 5V. Oddly, the black wire is the signal wire and not the ground. Brown should be wired to ground and black to pin 2.

The signal pin is known as open-collector and initially needs to be pulled HIGH. To do so, you use a 10k resistor to connect it to 5V as well. The signal pin, therefore, reads HIGH when no motion occurs and is pulled to LOW when there is motion.

You will need:

- An Arduino Uno;
- Breadboard;
- An SE-10 PIR motion sensor;
- A 10k ohm resistor;
- Jumper wires.

Lay out the circuit as in the layout and circuit diagrams.

Complete the circuit and choose File → Examples → 01.Basics →

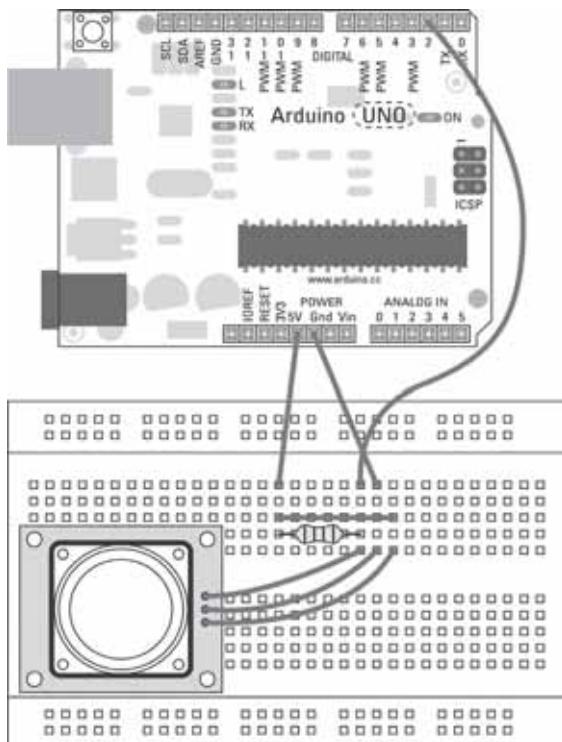


Figure 2: Layout diagram for the project

DigitalReadSerial from the Arduino menu to load the sketch.

This sketch is intended for a push-button but follows the same principles. If you want to make the sketch more specific, you can save it with a more appropriate name and variable names.

```
/*
DigitalReadSerial
Reads a digital input on pin 2, prints the result to the serial
monitor
This example code is in the public domain.
*/
// digital pin 2 has a pushbutton attached to it. Give it a name:
int pushButton = 2;
// the setup routine runs once when you press reset:
void setup() {
  // initialize serial communication at 9600 bits per second:
  Serial.begin(9600);
  // make the pushbutton's pin an input:
  pinMode(pushButton, INPUT);
}
// the loop routine runs over and over again forever:
void loop() {
  // read the input pin:
  int buttonState = digitalRead(pushButton);
  // print out the state of the button:
  Serial.println(buttonState);
  delay(1); // delay in between reads for stability
}
```

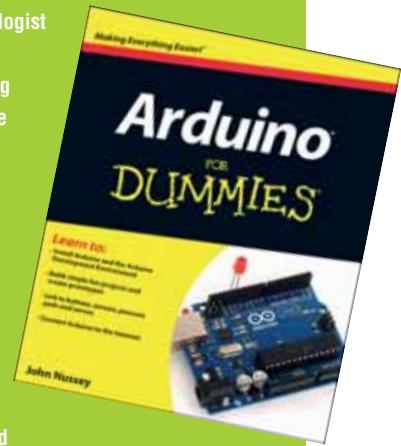
Press the Compile button to check your code. Doing so highlights any grammatical errors and turns them red when they are discovered. If the sketch compiles correctly, click Upload to send it to the board. When it has finished uploading, affix the PIR

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John Nussey is a creative technologist based in London. He teaches interaction design and prototyping at the Goldsmiths College and the Bartlett School of Architecture among others.

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sensor to a surface that is free of movement, and open the serial monitor, which will reset the sketch; the sensor then calibrates itself in the first 1 to 2 seconds. When movement is detected, the button's state-value changes from 1 (no movement) to 0 (movement).

If nothing happens, double-check your wiring:

- Make sure the correct pin number is being used;
- Check the connections on the breadboard. If the jumper wires or components are not connected using the correct rows in the breadboard, they will not work;
- Try restarting the PIR sensor by disconnecting and reconnecting the GND wire, and be sure that it does not move during or after calibration.

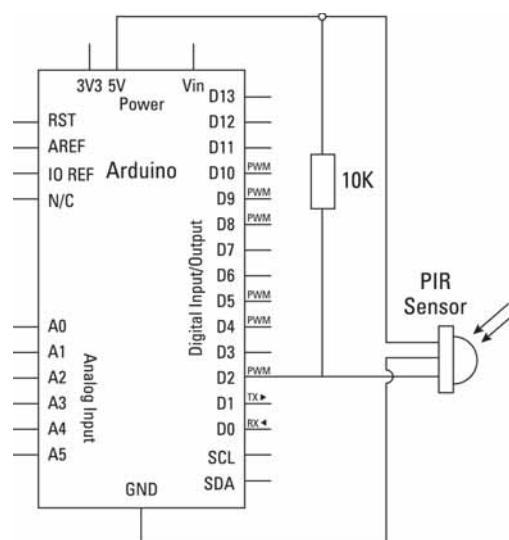


Figure 3: Arduino board connections to the PIR sensor



Microelectronics: The MOS Transistor

MAURIZIO DI PAOLO EMILIO, PHD IN PHYSICS AND A TELECOMMUNICATIONS ENGINEER, PRESENTS THIS SERIES OF ARTICLES ON THE FUNDAMENTALS OF MICROELECTRONICS

Today's microelectronics systems are dominated by MOSFETs (metal oxide semiconductor field effect transistors). A typical MOSFET structure is shown in Figure 1: on a substrate of monocrystalline p-type semiconductor, two junctions are made of type n+ semiconductor, with terminals called drain (D) and source (S). The area between them is made of a 0.01 μ m (or less) silicon dioxide layer – an excellent insulator. As the third terminal, or gate, is isolated from the silicon substrate, the gate current is zero.

Applying a positive voltage between gate and source causes electrons to flow, forming a conductive channel. In these conditions if $V_{ds} > 0$ is applied, current will flow between drain and source, which is controlled by the voltage between the gate and source.

The electrical characteristics of the MOSFET depend on its gate length (L) and gate width (W) and parameters such as oxide thickness and doping of the semiconductors (degree, material). Typical values are $L = 0.1\text{--}2\mu\text{m}$, $W = 0.5\text{--}500\mu\text{m}$, with a range of gate oxide thickness of 3–50nm.

Transistor Types

There are four types of MOS transistors: two n-channel based and two p-channel based. N-channel MOSFETs or nMOS, are

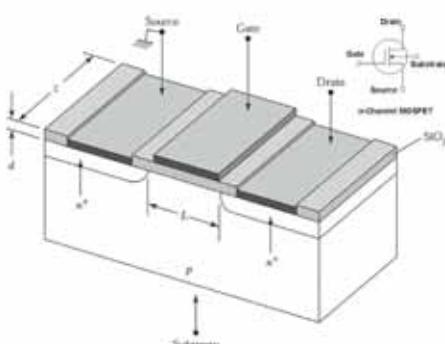


Figure 1: The inside outline (general) and symbol of a MOSFET

formed on a p-type substrate:

- nMOS enrichment (enhancement) or normally off;
- nMOS depletion (depletion) or normally on.

The p-channel MOSFET (pMOS) is formed on an n-type substrate:

- pMOS enrichment (enhancement) or normally off;
- pMOS depletion (depletion) or normally on.

In most MOSFET applications, input signal is the gate (G) voltage V_g and output is the drain (D) current I_d . The ability of the MOSFET to amplify signals is given by the output/input ratio, or transconductance $g_m = dI/dV_{gs}$.

Figure 2 shows the $I_d - V_{ds}$ characteristic curve, with three main regions of operation:

- **Cutoff:** in this case it is necessary to induce the channel with $V_{gs} \geq V_t$ (V_t being the threshold voltage) of the nMOS.
- **Triode:** the channel must be induced and have V_{ds} low enough to keep it continuous: $V_{gd} > V_t$.
- **Saturation:** in this mode the channel is induced by $V_{gs} \geq V_t$ to ensure that the channel is pinched off at the drain end, $V_{gd} \leq V_t$. Figure 3 shows the plot of I_d versus V_{gs} for an enhancement-type nMOS device in saturation.

In saturation mode, this device as an ideal current source (Figure 4); however, the output resistance (r_o) should be considered.

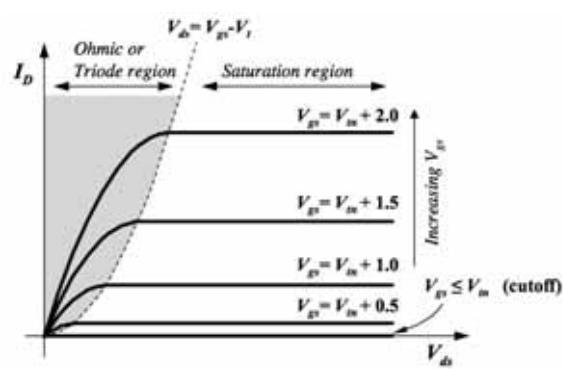


Figure 2: Characteristic curve $I_d - V_{ds}$

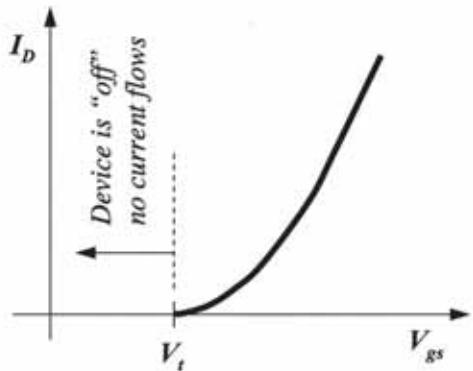
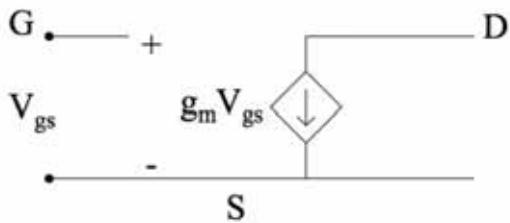
Figure 3: Saturation, I_d vs V_{gs} 

Figure 4: MOSFET model (ideal)

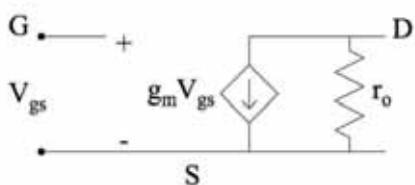


Figure 5: MOSFET model (not ideal)

Conductances

Whilst the transconductance g_m gives drain current variations dependent on the variations of V_{gs} , there is another fundamental MOSFET parameter called output conductance, which is variation of the drain current I_{ds} due to variations of V_{ds} . The output conductance assumes a much greater importance, result of

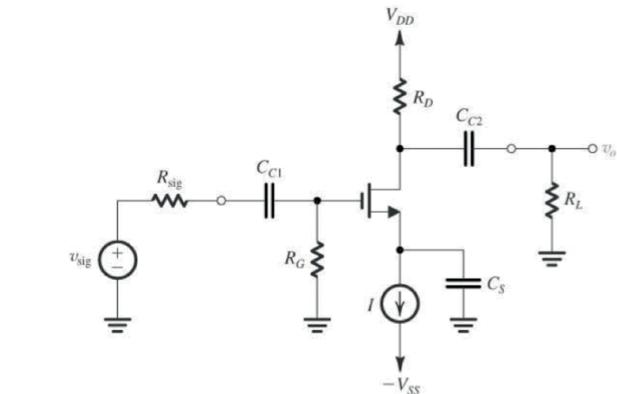


Figure 6: Common source amplifier

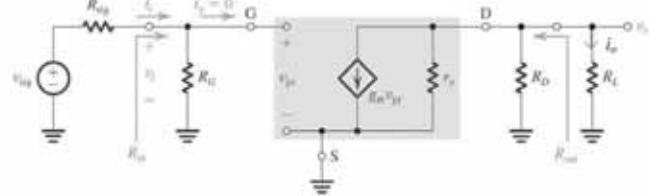


Figure 7: Common source amplifier (model)

an effect called “channel length modulation” due to V_{ds} , which is a shortening of the length of the inverted channel region.

$$I_{ds} = k(V_{gs} - V_t)2(1 + V_{ds}/\lambda)$$

It is obvious that there's a linear dependence of I_{ds} on V_{ds} in accordance with λ , which is the channel length's modulation parameter. Parameter k is the transconductance factor proportional to the MOSFET's geometry.

Application Example

One typical MOSFET application is the common source amplifier seen in Figures 6 and 7. The input signal is applied to the gate through the coupling capacitor C_1 . The output signal of the outline in Figure 6 (voltage on R_L) is on the drain pin of the MOSFET and connected to the load through C_2 . Capacitors C_1 , C_2 and C_s are coupling capacitors and can be considered short circuits for the signals in the centre-band frequencies; the source pin (S) is therefore connected to ground for all analog input signals. Resistors R_1 , R_2 , R_D and R_s form a bias network.



Lumped Parameter Models

IAN DARNEY PRESENTS THIS SERIES OF ARTICLES ON CIRCUIT MODELLING FOR ELECTROMAGNETIC COMPATIBILITY

T

his is the second article in this series on 'Circuit Modelling for Electromagnetic Compatibility' (EMC). The first article introduced the concepts involved in the approach, including that of the Triple-T circuit model. This instalment shows how values can be assigned to the components of that model. They are described as 'lumped parameters' to distinguish them from the 'distributed parameters' of transmission-line theory. Future articles will focus on transmission line and antennae models, bench testing, transient models and design guidelines.

Primitive Equations

The starting point in the process of building a circuit model is to consider the magnetic field surrounding a section of wiring harness.

In Figure 1 all three currents are defined as flowing from left to right.

The end-to-end voltage along each conductor is a function of the rate of change of current in that conductor and the rate of change of current in the other two conductors. This leads to the Primitive Equations:

$$\begin{aligned} Vp_1 &= Zp_{1,1} \cdot Ip_1 + Zp_{1,2} \cdot Ip_2 + Zp_{1,3} \cdot Ip_3 \\ Vp_2 &= Zp_{2,1} \cdot Ip_1 + Zp_{2,2} \cdot Ip_2 + Zp_{2,3} \cdot Ip_3 \\ Vp_3 &= Zp_{3,1} \cdot Ip_1 + Zp_{3,2} \cdot Ip_2 + Zp_{3,3} \cdot Ip_3 \end{aligned} \quad (1)$$

$$\text{where: } Zp_{i,j} = j \cdot \omega \cdot Lp_{i,j} \quad (2)$$

$$\text{and: } Lp_{i,j} = \frac{\mu_0 \cdot \mu_r \cdot l}{2 \cdot \pi} \cdot \ln \left(\frac{l}{r_{i,j}} \right) \quad (3)$$

$r_{i,j}$ is the radial separation between the centres of conductors i and j , $r_{i,j}$ is the radius of conductor i , μ_0 is the permeability of free space, μ_r is the average permeability of the immediate environment, l is the length of the section, ω is the frequency, in radians per second. The letter p has been included in the definition of the electrical parameters because there are different 'types' of parameter and it is necessary in any computation to be able to distinguish one type from another. Since Equation 3 is the simplest possible definition of an entity that has the 'dimension' of inductance, Lp can be described as a 'primitive'.

Equation 1 relates the energy of the magnetic field in the vicinity of the assembly to the voltage developed along the length. Primitive inductance is one of the basic building blocks of all circuit models.

Loop Equations

Since electronic systems are concerned with the voltages between adjacent terminals, rather than the distribution of energy along conductors, the next step is to derive a pair of Loop Equations. Figure 2 defines the relationship between loop currents and primitive currents, and between loop voltages and primitive voltages.

$$\begin{aligned} Ip_1 &= Iloop_1 \\ Ip_2 &= Iloop_2 - Iloop_1 \\ Ip_3 &= -Iloop_2 \end{aligned} \quad (4)$$

and:

$$\begin{aligned} Vloop_1 &= Vp_1 - Vp_2 \\ Vloop_2 &= Vp_2 - Vp_3 \end{aligned} \quad (5)$$

Substituting primitive currents for loop currents in Equation 1 and using Equation 5 leads to the Loop Equations:

$$\begin{aligned} Vloop_1 &= Zloop_{1,1} \cdot Iloop_1 + Zloop_{1,2} \cdot Iloop_2 \\ Vloop_2 &= Zloop_{2,1} \cdot Iloop_1 + Zloop_{2,2} \cdot Iloop_2 \end{aligned} \quad (6)$$

where:

$$\begin{aligned} Zloop_{1,1} &= Zp_{1,1} - Zp_{1,2} - Zp_{2,1} + Zp_{2,2} \\ Zloop_{1,2} &= Zp_{1,2} - Zp_{1,3} - Zp_{2,2} + Zp_{2,3} \\ Zloop_{2,1} &= Zp_{2,1} - Zp_{2,2} - Zp_{3,1} + Zp_{3,2} \\ Zloop_{2,2} &= Zp_{2,2} - Zp_{2,3} - Zp_{3,2} + Zp_{3,3} \end{aligned} \quad (7)$$

Since:

$$r_{i,j} = r_{j,i}, \quad Lp_{i,j} = Lp_{j,i}, \quad Zp_{i,j} = Zp_{j,i}, \quad \text{and} \quad Zloop_{1,2} = Zloop_{2,1}$$

The important fact about the loop equations is that they have been derived from Electromagnetic Theory.

Circuit Equations

Figure 3 is a model that yields a similar pair of equations. Mesh analysis gives:

$$\begin{aligned} Vc_1 &= (Zc_1 + Zc_2) \cdot Ic_1 - Zc_2 \cdot Ic_2 \\ Vc_2 &= -Zc_2 \cdot Ic_1 + (Zc_2 + Zc_3) \cdot Ic_2 \end{aligned} \quad (8)$$

$$\text{where: } Zc_k = j \cdot \omega \cdot Lc_k \quad (9)$$

and the integer k identifies the circuit branch.

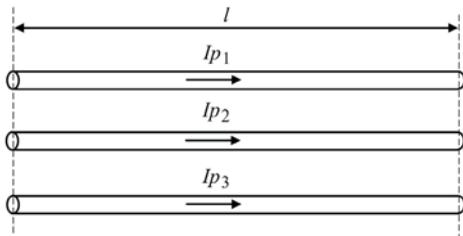
Correlation

Defining circuit impedances in terms of loop impedances:

$$\begin{aligned} Zc_1 &= Zloop_{1,1} + Zloop_{1,2} \\ Zc_2 &= -Zloop_{1,2} \\ Zc_3 &= Zloop_{2,2} + Zloop_{1,2} \end{aligned} \quad (10)$$

Using Equation 7 to substitute for the loop impedances enables the circuit impedances to be related directly to the primitives:

Figure 1: Primitive currents in a section of three-conductor cable



$$\begin{aligned} Zc_1 &= Zp_{1,1} - Zp_{2,1} - Zp_{1,3} + Zp_{2,3} \\ Zc_2 &= Zp_{2,2} - Zp_{1,2} - Zp_{2,3} + Zp_{1,3} \\ Zc_3 &= Zp_{3,3} - Zp_{3,1} - Zp_{2,3} + Zp_{2,1} \end{aligned} \quad (11)$$

Using Equations 9 and 2 to relate circuit inductors to primitive inductances and Equation 3 to relate primitive inductances to radii and length gives:

$$\begin{aligned} Lc_1 &= \frac{\mu_0 \cdot \mu_r \cdot l}{2 \cdot \pi} \cdot \ln \left(\frac{r_{1,2} \cdot r_{1,3}}{r_{1,1} \cdot r_{2,3}} \right) \\ Lc_2 &= \frac{\mu_0 \cdot \mu_r \cdot l}{2 \cdot \pi} \cdot \ln \left(\frac{r_{1,2} \cdot r_{2,3}}{r_{2,2} \cdot r_{1,3}} \right) \\ Lc_3 &= \frac{\mu_0 \cdot \mu_r \cdot l}{2 \cdot \pi} \cdot \ln \left(\frac{r_{1,3} \cdot r_{2,3}}{r_{3,3} \cdot r_{1,2}} \right) \end{aligned} \quad (12)$$

Capacitance

If the rate of change of current in the three conductors of Figure 1 is very low and magnetic effects are ignored, then the voltage on the surface of each conductor can be related to the charge it carries as well as to the charges on the other two conductors. Electric field effects predominate. Even so, Equation 1 continues to define the relationships. But this time, the primitive impedances are capacitive. That is:

$$Zp_{i,j} = \frac{1}{j \cdot \omega \cdot Cp_{i,j}} \quad (13)$$

where:

$$Cp_{i,j} = \frac{2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_r \cdot l}{\ln \left(\frac{l}{r_{i,j}} \right)} \quad (14)$$

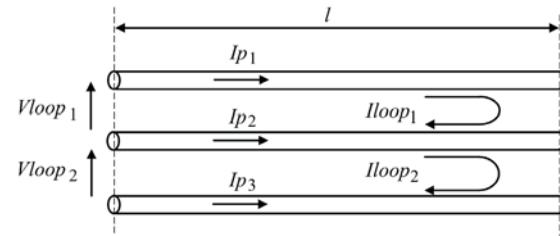
ϵ_0 is the permittivity of free space and ϵ_r is the average value of the relative permittivity of the insulation.

The relevant circuit model is that shown by Figure 4, where the impedance of each branch is:

$$Zc_k = \frac{1}{j \cdot \omega \cdot Cc_k} \quad (15)$$

Using Equation 15 to substitute for the circuit impedances on the left hand side of Equations 11 and 13 to substitute for the primitive impedances on the right-hand side allows the components of Figure 4 to be defined in terms of the primitive capacitors. Using Equation 14 enables the circuit capacitors to be defined in terms of the geometry of the assembly:

Figure 2: Loop currents and voltages



$$\begin{aligned} Cc_1 &= \frac{2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_r \cdot l}{\ln \left(\frac{r_{1,2} \cdot r_{1,3}}{r_{1,1} \cdot r_{2,3}} \right)} \\ Cc_2 &= \frac{2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_r \cdot l}{\ln \left(\frac{r_{1,2} \cdot r_{2,3}}{r_{2,2} \cdot r_{1,3}} \right)} \\ Cc_3 &= \frac{2 \cdot \pi \cdot \epsilon_0 \cdot \epsilon_r \cdot l}{\ln \left(\frac{r_{1,3} \cdot r_{2,3}}{r_{3,3} \cdot r_{1,2}} \right)} \end{aligned} \quad (16)$$

The voltage at the node at the junction of the three capacitors is zero because each primitive capacitor is defined in terms of the work done in bringing unit charge from a point in the far distance to the conductor surface. At any far distant point, the energy level is zero.

General Circuit Model

Combining Figure 3 and 4 and adding resistors to simulate conductor resistance gives Figure 5. This model can simulate electromagnetic field coupling, since it caters for interaction between the magnetic field and the electric field.

The voltage at the star point remains at zero because the magnetic field strength at any point in the far distance is zero.

The Twin Theories

The reasoning in the previous section helps to identify the key relationship between Electromagnetic Theory and Circuit Theory.

The mathematics of the former involves divs, dels and curls, the relationships between rectangular, circular and spherical coordinate systems, and the concept of time-varying electromagnetic fields. Electromagnetic Theory has been developed as a result of a multitude of measurements and many analyses of the data gathered. It shows that currents and voltages anywhere in the system affect currents and voltages everywhere else in the system.

Circuit Theory invokes a totally different set of concepts. The system is depicted as a network of nodes and branches, and the voltage across each branch is defined as a unique function of the current flowing in that branch. This results in a dramatic simplification in the mathematics, but at the expense of a lack of fidelity in the simulations.

The derivation process for the general circuit model can be summarised in the form of a series of steps:

1. Define the geometry of the assembly.
2. Define a set of Primitive Equations.
3. Define the loop currents and voltages in terms of the primitives.
4. Define a set of Loop Equations.
5. Define the loop inductors and loop capacitors in terms of the primitives.
6. Create a circuit model that can replicate these equations.
7. Derive the Circuit Equations.
8. Relate the circuit components to the loop inductors and capacitors.

Figure 3: Circuit model of magnetic field coupling

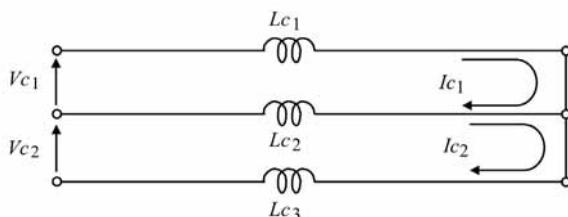


Figure 4: Circuit model of electric field coupling

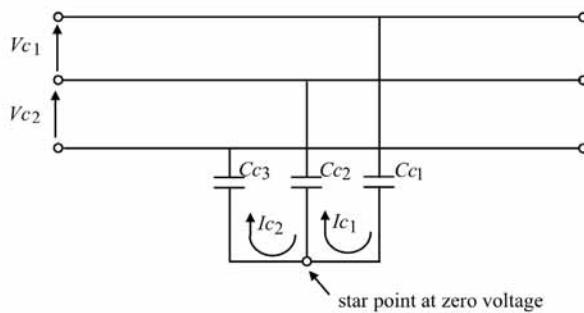


Figure 5: General circuit model of electromagnetic field coupling

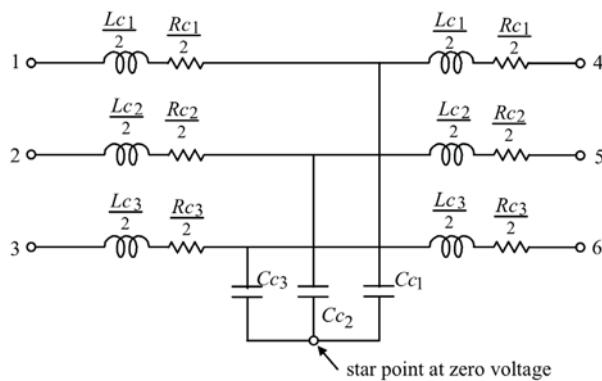
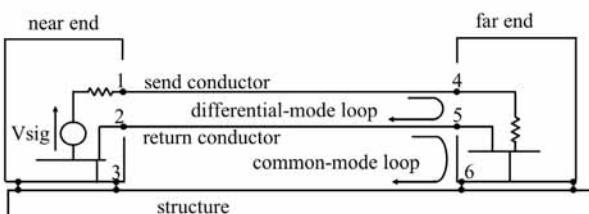


Figure 6: The Signal link



9. Relate the circuit components to the primitive parameters.
10. Define the circuit components in terms of the geometry of the assembly.

The key feature of the above process is that step 6 does not follow naturally from step 5. Lateral thinking is needed. The purpose of the circuit model is to create a set of mesh equations that correlate precisely with those of the loop equations. Mesh equations are derived from Circuit Theory. Loop equations are derived from the relationships of Electromagnetic Theory.

The circuit model can be treated in the same way as the unknown variable in mathematical problems. It enables the equations of Electromagnetic Theory to be solved using the analytical tools of Circuit Theory. This concept is fundamental to the analysis of interference coupling.

Types of Parameter

The process used to create the Triple-T network is based on the textbook method of deriving formulae for the phase inductance and phase capacitance of a three-phase power line. A review of the derivation process reveals that there are three different types of parameter: primitive, loop and circuit.

A Primitive parameter is one which relates the current in a conductor to the energy level of the electromagnetic field associated with that current. The conductor is treated as an antenna.

Loop parameters are derived from primitive parameters and are used in equations which relate loop voltages to loop currents. Since the voltages always appear between adjacent terminals, loop parameters can be measured directly by electronic test equipment.

Circuit parameters are those which appear in circuit diagrams and circuit analyses.

The technique can be used to derive formulae for the circuit components of other configurations such as that between two conductors routed over a ground plane, or coupling via the screen of a co-axial cable. It can be developed to create a circuit model of any cable cross-section. Chapters two and three of the book 'Circuit Modeling for Electromagnetic Compatibility' show how.



The Circuit Model can be treated in the same way as the unknown variable in mathematical problems

Bench Testing

The general circuit model of Figure 5 can be used to simulate any signal link of the form illustrated by Figure 6. Although it is useful to be able to calculate parameter values using knowledge of the geometry of the assembly, it is not essential. Test equipment can provide more accurate measurements for complex assemblies.

During the prototype phase of any new electronic design, the option is available for the designer to carry out bench tests. It is possible to open circuit or short circuit any pair of the terminals identified as 4, 5 and 6. An LCR meter can be connected at the near end. A set of measurements can be defined. Performing these measurements will provide sufficient data to assign numerical values to all the circuit components.

The fourth article in the series will describe bench testing in more detail and will identify a much simpler method of assigning component values to the general circuit model.

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N

ational Electronics Week returns to NEC, Birmingham, this year between 8-10th of April, and as before it will be co-located with other industry events to offer visitors the opportunity to see the best of UK's capabilities at one time in one place.

The show will return to a three-day format to run in line with the neighbouring events and to encourage a greater number of global exhibitors and visitors, providing a platform for international pavilions.

IPC Hand Soldering Competition

This year IPC will host a hand-soldering competition, offering cash prizes from £100-£300. The first place winner will also earn the chance to compete at the IPC World Championship at IPC APEX EXPO 2015, San Diego, US.

Hand soldering of high-density printed boards demands highly skilled operators to ensure a zero-defect soldering process, and this contest – IPC's first competition at National Electronics Week – recognizes the best skills in hand-soldering complex printed board assemblies. Over three days, participants will compete to build a functional electronics assembly within a 45-minute time limit. Assemblies will be judged in accordance with IPC-A-610E Class 3 criteria, the speed at which the assembly was produced and its overall electrical functionality. IPC-A-610 Master Instructors will serve as the judges.

"Many companies take pride in how many IPC certified specialists they have on staff, and this event is a fun and friendly way to give them an opportunity to let their staff shine," said David Bergman, IPC vice president of international relations.

Hand-soldering competition entries will be accepted until



March 25, 2014, and the number of entrants is limited, so participation is on a first come, first served basis. Interested participants can submit their entry at www.ipc.org/hsc-new-uk.

Embedded Masterclass

In addition, National Electronics Week will also be the platform for the Embedded Masterclass, which focuses on designing systems around FPGAs with integrated ARM processors. Altera's Stefano Zammattio will explain how bringing the two technologies together on one die has enabled integration to a level not possible with discrete device packages.

"This brings higher performance and capabilities not possible before, and as such developers have little experience of the issues that can arise," said Zammattio.

The presentations will also explain how to move from designing with a single-core processor to one using two or more cores. Zammattio will cover designing with dual-core processors, notably AMP and real-time systems, and give guidance on how to design high-performance SoC FPGA systems.

The National Electronics Week exhibition will have a specific Embedded Zone that will include industry leaders. The seminar and workshop theatres will be integrated into this area, giving delegates plenty of time to engage with suppliers, view demos and discuss industry issues in one location.

UMR's Embedded Masterclass, a dedicated engineering design conference for the embedded community, will take place alongside the National Electronics Week exhibition.

Student Zone

National Electronics Week's organisers also welcome students and academics to the show, to engage with key companies in the electronics sector, attend free seminars and technical conferences and see live features, including production lines and board assembly.

For further information about National Electronics Week, the content and sponsorship, contact: Claire Saunders, Event Director, NEW Events, Email: Claire@neweventsLtd.com or Jayne Foster, Conference Manager, UMR Ltd, Email: j.foster@umronline.co.uk or check out this event's website at www.new-expo.co.uk/newuk

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PIC18F65J11-I/PT	1.32	PIC18F4520-I/PT	2.22
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PANASONIC PIR SENSORS

Based on a patented MiPTec manufacturing process, the Panasonic range of miniature PIRs are continuously being expanded in specification to meet customers' needs. Using the ubiquitous TO5 can casing, with an encapsulated Fresnel lens array, the addition of internal high-density embedded circuits eliminates the need for external control circuits. This allows the designer to meet the highest of PIR specification in the minimum of space.

Panasonic's PIRs are available in two distinct ranges: The NaPION range is available in 5M and 12M detection ranges with a choice of white or black lens casings. The choice of analogue and digital outputs allows the range to comprehensively cover



the majority of sensing applications with consideration of the aesthetic properties needed in many domestic configurations.

The PaPIR range is designed for applications where very low quiescent currents or extreme sensitivities are required. Ideal for wireless and battery-operated systems, typical applications include security, occupancy, lighting and remote control use.

www.panasonic-electric-works.co.uk

SCHURTER OFFERS LOW-LOSS AND PRECISE CHIP FUSES

Schurter offers a broad range of high-quality chip fuses, developed specially for low-loss and precise overcurrent protection in secondary circuitry. Six different types, available in chip dimensions from 0402 to 1206, offer compact and effective protection in the event of a fault.

The Schurter chip fuses are available in a number of different current ratings from 50mA to 25A at a rated voltage of up to 125VAC/VDC. Depending on the version and voltage ratings, a breaking capacity of up to 600A is



reached. Thanks to these impressively high values and variety, these chip fuses can be used in a wide range of applications, especially in mobile and battery-operated

devices.

Schurter chip fuses set themselves apart from comparable products through their extremely precise opening times and minimal power dissipation. In addition, their solid construction makes them especially resistant to vibrations and pulse loads.

www.schurter.co.uk

TMD FEATURES ULTRA-HIGH POWER TWT AMPLIFIERS FOR EMC HIRF TESTING AT EMV 2014

A wide range of travelling wave tube (TWT) amplifiers from TMD Technologies will be highlighted at the EMV 2014 exhibition and conference on electromagnetic compatibility (EMC) in Dusseldorf, Germany. TMD's capability extends up to 40kW

for certain special pulsed models, covering the frequency range from 10kHz to 40GHz using suites of solid-state and TWT-based amplifiers.

In particular, TMD has recently launched a range of ultra-high power pulsed TWT amplifiers, optimised for use in high intensity radiated fields (HIRF) EMC testing. Using these instrumentation amplifiers, EMC test laboratories have generated 14,000V/m, easily complying with the latest, most demanding RTCA/DO-160 test requirements.

TMD is a world leader in design innovation in this field, and these compact, lightweight, rack-mounted units benefit from being based on the company's rugged radar amplifiers, sharing the same switched-mode power supply technology.

The company will exhibit on Stand 309 at EMV 2014, which takes place on 11-13 March 2014.

www.tmd.co.uk



PEAK GROUP AND SIMPLICITY AI FEATURE ATE AND MASS INTERCONNECT SYSTEMS

At the PXI Show, The Peak Group is featuring its recently announced partnership with

Simplicity AI to provide integrated test solutions based on National Instruments (NI) industry-standard platforms, along with Peak's test hardware and fixturing technology and Simplicity AI's advanced test and measurement software.

Both companies are NI Alliance Partners. Peak Production Equipment, based in Letchworth, UK, is a proven provider of automated test and measurement solutions, supporting every stage of the assembly process from component testing to highly complex functional solutions. Peak is also the exclusive UK agent for the mass interconnect systems made by Virginia Panel Corporation, which are extensively used as interfaces within the automatic test sector.

Simplicity AI, based in Farnborough, UK, provides a range of advanced technical products and engineering services for test, measurement, control and automation, with a particular emphasis on developing automatic test and measurement software built around industry-standard platforms.

www.thepeakgroup.com

THE PXI SHOW, NEC, BIRMINGHAM, 8-10 APRIL 2014, STAND NUMBER 45



MINIATURE LINEAR HALL-EFFECT SENSOR IC FOR MEDIUM-ACCURACY APPLICATIONS

The new A1304 from Allegro MicroSystems Europe is a linear Hall-effect sensor IC specifically designed for applications that require medium accuracy in a very small package.

The new device is designed for applications in consumer and industrial markets, and supports an industrial temperature range of -40°C to 85°C.

The A1304 is a factory-trimmed one-time programmable 3.3V linear sensor that eliminates the need for customers to program the device to compensate for temperature effects on sensor performance. It has a typical programmable



sensitivity level of 4mV/G ± 6%.

The device's high bandwidth and high-speed chopping scheme minimise quiescent

voltage output drift across the operating temperature range, yielding a low noise analogue output and ultimately enabling higher accuracy.

The A1304 complements Allegro's existing linear Hall-effect sensors by providing a more cost-effective solution for non-automotive markets, with sensitivity and quiescent voltage output temperature coefficient being trimmed at the factory for improved accuracy.

www.allegromicro.com

PEI-GENESIS EUROPE PRESENTED WITH AN AWARD BY AMPHENOL LTD

"PEI-Genesis has done a fantastic job of accelerating sales of our Black Zinc Nickel products, particularly the MIL-DTL-38999 range into a wide selection of interesting market applications," said Steve Roberts, Managing Director of Amphenol Ltd (left) whilst presenting PEI-Genesis's Steve Hutchinson, the company's European Sales Manager (right), with an award for their exceptional first year sales of Black Zinc Nickel connectors.

Until recently Cadmium plating has been the industry preference for aeronautical and defence applications but it is a highly toxic metal now severely restricted under RoHS legislation. Now, Amphenol Ltd is the first UK manufacturer to supply Black Zinc Nickel plated connectors approved to the strict military specification Mil-DTL-38999. The conductive and non-reflective Black Zinc Nickel RoHS compliant finish is approved for 500 hours salt spray endurance and is fast becoming the new defence industry standard, whilst also being highly reliable in commercial and industrial applications.

www.amphenol.co.uk



NEW, VERSATILE 2MM TEST SOCKETS FROM HARWIN ARE LOW PROFILE

Harwin launched a new range of PCB-mounted, easy-access dual-entry test sockets that accept a 2mm pin. These low-profile devices measure only 5.16mm max above the board when mounted and feature gold-plated contacts to ensure excellent electrical performance.

Devices feature a flat upper surface to enable automated pick-and-place assembly. Both SMT and PTH devices are available: surface-mount versions are supplied on tape-and-reel packaging for automated production or loose for prototyping; throughhole styles are available in three different colours to enable colour-coding of functions. Devices are rated at 5A, 1500V. They have a contact resistance of $5\text{m}\Omega$ (max) and an operating temperature of -40degC to $+105\text{degC}$.



Key applications include high-current test points and wire-to-board connections used in a wide range of market segments such as power supplies, instrumentation, traffic signalling, energy and healthcare.

Devices are immediately available from stock, on low MOQs to enable prototyping and pre-production design.

www.harwin.co.uk

NEW COHERENT POLYMER FIBRE FROM OMC TRANSMITS HI-RES REMOTE IMAGES

OMC has released a new coherent polymer fibre which enables high resolution remote imaging. The bundle consists of thousands of individual polymer fibre cores arranged coherently at each end so the image incident on one fibre face is visible on the other face.

The fibre is designed to provide a lower cost solution to remote imaging in applications where the extremely small diameters of coherent glass fibre (such as those used to image inside blood vessels) are not required. The resolution is very high, making the fibre suitable not only for high resolution imaging, but also high precision sensing, remote vision, passive surveillance and imaging in inaccessible areas.

The high tensile strength coherent polymer fibre consists of over 7000 individual pixels for high resolution imaging. Cable diameters of 2.0mm and 2.5mm are available now and the cores are protected by a robust outer protection layer.

www.omc-uk.com



ST NUCLEO DEVELOPMENT BOARDS FROM MOUSER GET TO THE HEART OF DEVELOPMENT

Mouser Electronics is now stocking the new Nucleo Development Boards from STMicroelectronics (ST). These development boards are suitable for the development of any ST's STM32 product families featuring ARM Cortex M0, Cortex M3 and Cortex M4 microcontrollers, and are compatible with a wide range of expansion boards.

The new Nucleo boards offer many advanced features not found in other microcontroller development ecosystems. Besides the usual assortment of push buttons, LEDs and a USB debug interface, they have two unique sets of expansion headers. The first set of expansion headers is standard on all Nucleo boards; they sit on the outside edges of the board and allow easy access to all peripherals of the target microcontroller during test and development.

The second set of expansion headers are nestled inside the first set and are Arduino shield compatible. They support the use of Arduino Uno v3 expansion boards, called "Arduino shields", allowing ST's Nucleo boards expanded access to dozens of Arduino-compatible expansion boards.

www.mouser.com



AVX EXPANDS ITS AWARD-WINNING 9296 SINGLE POKE-HOME WTB CONTACT SERIES

AVX has expanded its award-winning 9296 Single Poke-Home Wire-to-Board (WTB) contact series with the addition of an extremely low profile (1.7mm) single-position contact. Recently recognized with an Electronic Products Product



of the Year Award for design innovation, price and performance, the 9296 series contacts enable simple, reliable and solder-less termination of power, signal and ground wires in a broad range of harsh industrial applications, whilst exhibiting full connector performance without the added expense of an insulator and its associated assembly costs. Featuring a unique closed box design with dual opposing high spring-force contacts that provide excellent wire retention in rugged environments, 9296 series contacts are now available with 1.7mm, 2mm, 3mm and 4mm profiles.

Integrating several key features within the stamping to facilitate SMT pickup, wire guidance, high force retention and easy twist-and-pull wire removal, 9296 series WTB contacts have upper and lower tines that guide stripped wires down the centre of the contact zone.

www.avx.com

SONDREL APPOINTS NEW EUROPEAN SALES MANAGER

Sondrel, a system-to-silicon IC design consultancy, has appointed Massimo Cecchetti as its European Sales Manager. Sondrel enjoyed a successful 2013 and this new post is one of a number created across the globe as the company doubled its worldwide workforce during last year.

Massimo has twenty years' experience in the semiconductor industry; he was involved in setting up the Italian office of TMA – later Avant! – acquired by Synopsys, and held positions at Infiniscale, Pulsic Ltd and Credence Systems. He was a consultant to many European EDA companies but also in the renewable energy sector.



"We're delighted that Massimo has joined us to spearhead our sales operation in Europe," said Graham Curren, Sondrel's CEO. "The outlook for European business is strong and Massimo's experience and respected reputation in the industry will enable us to expand our customer base in central and southern Europe and win repeat business in the region."

www.sondrel.com

GaN SYSTEMS APPOINTS TONY ASTLEY AS DIRECTOR EUROPEAN OPERATIONS

GaN Systems, a developer of gallium nitride power switching semiconductors, has announced the appointment of Tony Astley as Director of European Operations, with immediate effect. Astley will have

overall responsibility for all aspects of GaN Systems' business in Europe, the Middle East and Africa and will further develop its presence in the region, which represents about 20% of the world's total market for power device sales.

GaN Systems' cost-effective, high power gallium nitride transistors feature its proprietary Island Technology and overcome the limitations of today's silicon-based semiconductors, bringing significantly better performance and efficiency to power conversion applications such as alternative energy products and electric and hybrid vehicles. EMEA is a world leader in industrial and automotive technologies and Astley's role will encompass broad-based customers across the region as well as large OEMs in the industrial, power and automotive sectors.

"We're very excited to have Tony on board to drive growth in a key region," said Girvan Patterson, GaN Systems's CEO.

www.gansystems.com

NEW SWISSBIT SD AND MICRO SD MEMORY CARDS OFFER EXTREMELY LONG DATA RETENTION

Swissbit presents its new S-40 and S-40u Series SD and Micro SD memory cards for TCO-optimised applications. These are the first SD and Micro SD cards on the market to feature autonomous data refresh that requires no intervention by the host or application. Thanks to intelligent algorithms,



the memory cards deliver up to one hundred times longer data retention than conventional SD memory cards.

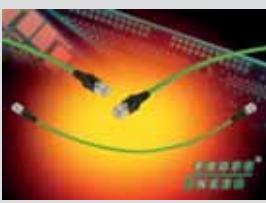
S-40 (SD) and S-40u (Micro SD) memory cards are equipped with

intelligent read disturb management (RDM) alongside an autonomous, performance-neutral background auto-refresh process. This type of data-care management significantly improves data reliability and balances out the increasing limitations of MLC NAND flash during long operation time and extensive use in the field. Data transfer rates reach up to 11MB/s for write and up to 24MB/s for read operations, putting them into SD3.0 speed class 6.

www.swissbit.com

GIGABIT CABLING COMPONENTS FOR PROFINET APPLICATIONS

Harting has introduced a range of Gigabit cabling components designed to extend the scope of industrial PROFINET applications into the Gigabit Ethernet range. Until now, PROFINET solutions have been based on Fast Ethernet operating at 100Mbit/s, but the new Harting products, which include all the familiar Fast Ethernet RJ45 PROFINET cabling



components, will allow future PROFINET applications to work in conjunction with a Gigabit Ethernet platform.

PROFINET systems based on these products will offer more variety and performance as well as being faster. They will also give users the option of incorporating standard Gigabit devices into PROFINET solutions, with the cabling containing eight wires instead of four.

For RJ45 wiring, Harting has defined the so-called modularity principle in a company standard which guarantees the mechanical compatibility of the RJ45 connector with the various IP65/67 housings such as the Han 3A or PushPull V.14 (AIDA interface).

www.harting.com

APACER'S CFAST 2.0 MEMORY CARD BRINGS PERFORMANCE TO HIGHER LEVEL

Since the release of CFast 2.0 specifications, Apacer has actively invested in its R&D and successfully launched the industry-leading CFast 2.0 memory card with SATA 3.0 (6Gb/s) high-speed transmission interface – CFast 2. Featuring a 2-channel bidirectional structure, Apacer's CFast 2 brings its performance to a higher level by adopting Toggle DDR 2.0 NAND Flash. With a sequential speed up to 310/240 MB/s, the CFast 2 doubles the speed of its predecessor. Apacer's CFast 2 features 40-bit ECC (Error Correcting Code), as well as supports Wear Levelling Technology and S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) that can detect the health status of



the memory card so as to significantly boost the reliability of the product. DEVSLP (Device Sleep) power mode is also supported, which enables the memory card to switch into a lower power state.

Both solutions are resilient to temperature variation, vibration and shock in harsh environment, with standard dimensions of 42.8mm x 36.4mm x 3.6mm.

www.apacer.com

ENVIRONMENTAL SENSING FOR A SMARTER LIFE

Sensirion will present its latest humidity and temperature sensor SHTW1 at the Mobile World Congress 2014. Using chip-scale packaging and combining

minimal size with maximum performance and low energy-consumption, the device is



particularly suitable for the wearable and mobile markets. It is based on CMOSens Technology, which integrates the sensor component and the evaluation circuit on a single semiconductor chip.

Sensirion is one of the first companies to use wafer-level chip-scale packaging in humidity and temperature sensors. This means SHTW1's package is no larger than the CMOSens Chip itself (1.3 x 0.7 x 0.5mm), yet the SHTW1 has the same functionality as conventional digital humidity and temperature sensors.

The operating voltage of 1.8V and power consumption of just 2pW at 1 measurement per second provide an optimal basis for using the sensor in small, mobile devices. SHTW1 measures relative humidity across a range of 0% to 100% RH, with a typical accuracy of ±3% RH.

www.sensirion.com

ENHANCED OXLEY BA9 LED LAMPS FROM AERCO

Now available from Aerco is a new version of the popular Oxley BA9 LED bulbs that incorporates the latest surface-mount technology to improve performance and expand capability.



Designed as a fit-and-forget replacement for traditional filament panel lamps, these enhanced lamps achieve the required intensity levels while avoiding the 'hot spot' issues and the inconsistencies in light spread inherent in discrete flat-topped LEDs. In addition to increased intensity, they provide enhanced colour uniformity, even illumination, sealing to IP66 and increased reliability, particularly at the higher end of the voltage range. Also, a reduction in overall length simplifies assembly and widens the range of potential applications.

Available in white, warm white, yellow, blue, green and red, the bulbs have a cut-out diameter of 9.8mm and a voltage range of 12 to 60VAC.

www.aerco.co.uk

SIC CELEBRATE 50 YEARS OF MANUFACTURING EXCELLENCE

Started in 1964 and originally called Swansea Industrial Components, the company supplied electrical assemblies into the white goods and gaming markets, but as it continued to improve and diversify its manufacturing capabilities it expanded into new sectors and product applications.

Today SIC serves over 450 customers across 24 sectors including aerospace and automotive among others. Its consistent expansion has allowed the company to become a full manufacturing partner to its customers, offering an 188,000ft² UK-based manufacturing facility with 150 staff.

SIC remains a family-owned business, which has helped it maintain a clear identity and future direction in the pursuit of manufacturing excellence.

"Manufacturing excellence permeates everything we do, from making sure we maintain our ISO9001/ISO14001 quality and environmental standards, to offering customers delivery systems that best match their production schedule and fundamentally ensuring that every project we take on and every product we manufacture is done so with the highest levels of excellence," said Operations Director Anthony Roberts.

www.sic ltd.com



CAD CONNECTED



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www.labcenter.com

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