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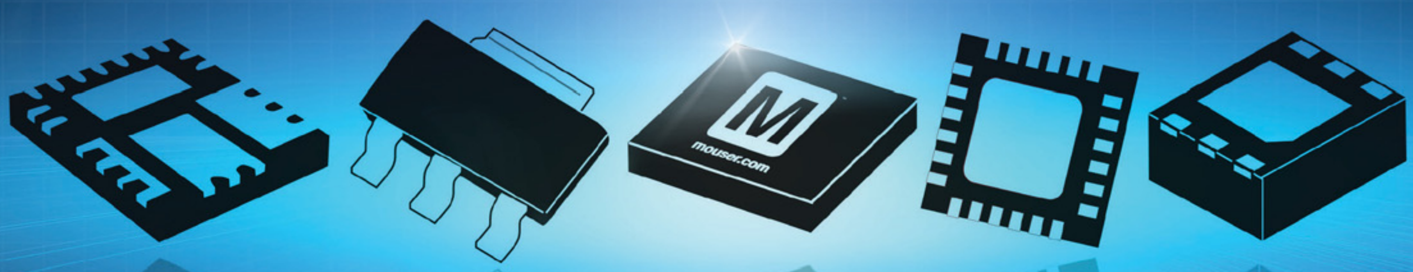
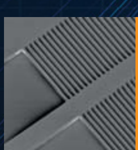
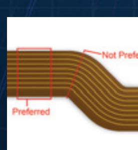


POWER MANAGEMENT
in Noise-Sensitive Applications



News
Novel mid-IR waveguide structure for sensing applications



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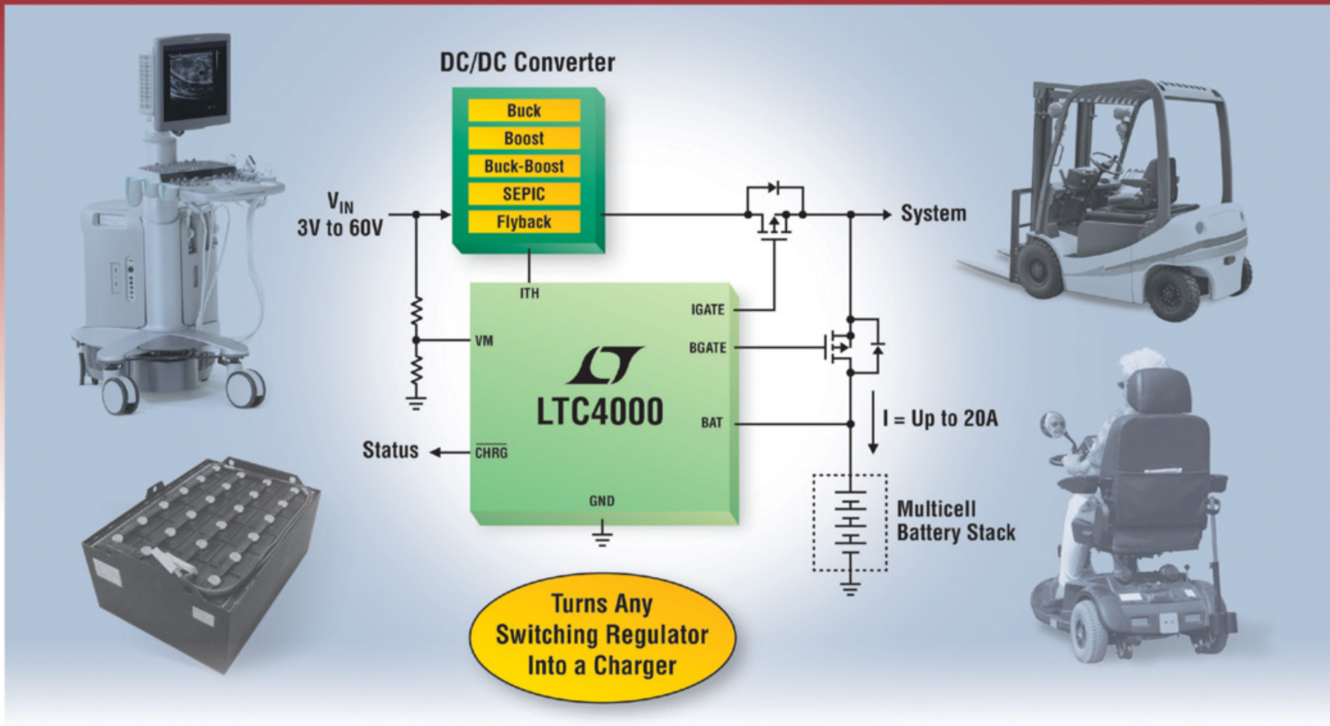
FEATURES

New Concept in BIG Battery Charging



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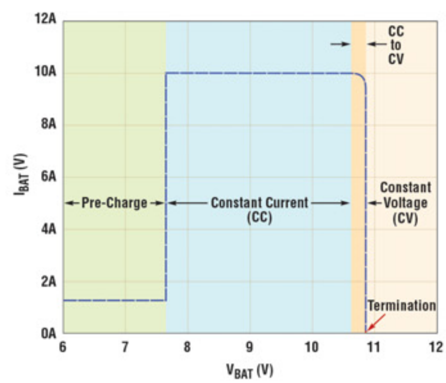
Charge Current Profile vs V_{BAT}



V_{FLOAT} = 10.8V

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TECHNOLOGY MOVES TO SMART PARKING APPLICATIONS

> Results gained from trials so far help explain the stages and multidimensional factors needed to successfully deploy smart parking projects

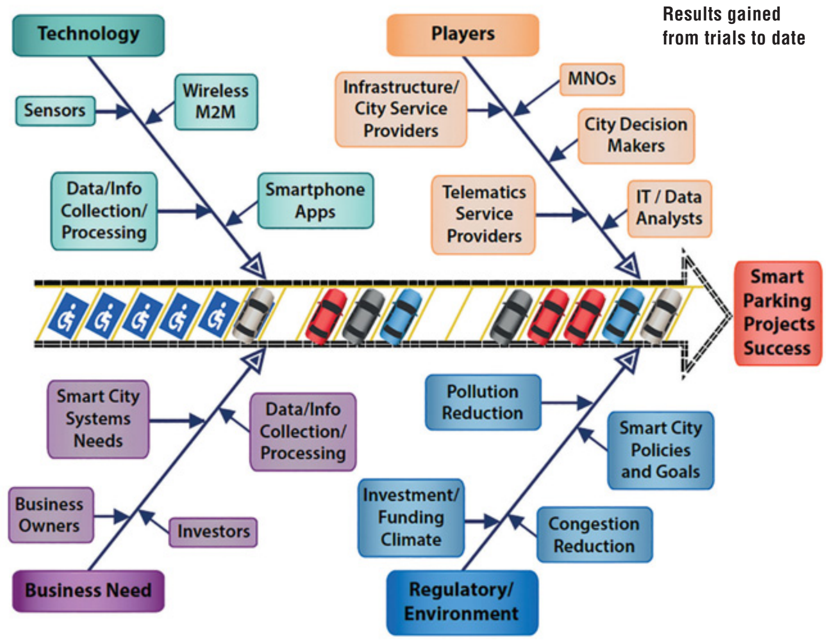
Smart parking could relieve congestion, reduce driver frustration, improve health and give a vital boost to the future of our cities, says Dr Therese Cory, the principal author of a new report published by Beecham Research.

"Road systems provide the vital arteries for commercial and business activities but parking has become a major problem in all cities," said Dr Cory. "Early smart parking apps may appear to be a novelty, but they are just the start. Alleviating parking congestion could deliver major benefits by helping to eliminate time wastage, cut petrol consumption and reduce harmful exhaust emissions. We can learn from these relatively circumscribed smart parking initiatives how to shape future, larger scale smart-city projects to drive further productivity and prosperity."

Cities are centres for business, government and culture, attracting high numbers of workers and visitors. But today, the use of modern communications and information technology is enabling city authorities to explore new ways to make their cities work better. There are already a number of ongoing smart parking trials in major cities, including Birmingham in the UK and Moscow in Russia, which rely on road-mounted sensors in busy shopping or tourist centres to guide traffic. Drivers use smartphone apps to access data collected from these sensors and analyzed in central IT systems to produce a map of free spaces. In the near future, automotive manufacturers will make this feature available on their in-car telematics displays.

This also opens opportunities for a broad range of companies who will be needed to deliver smart parking solutions, including sensor manufacturers, wireless network designers, mobile operators and IT system developers, integrators and analysts. They will be expected not only to provide solutions but help surmount challenges, such as fine-tuning the Machine-to-Machine (M2M) value chain to work well at the lowest cost. In addition, smart parking will enable small companies with state-of-the-art technologies to engage with large traditional bodies such as city departments and public service providers, where specialized expertise are often needed to enable these partners to work together.

Results gained from trials so far (see diagram below) help explain the disciplines and multidimensional factors needed to successfully deploy smart parking projects.



For more information on smart parking for smarter cities, go to http://www.beechamresearch.com/download.aspx?id=37, with the latest report by Beecham Research, a technology market research, analysis and consulting firm based in Cambridge, UK

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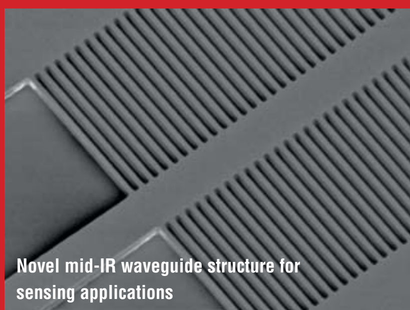
CAN GERMANIUM REPLACE SILICON IN THE MID-INFRARED GROUP IV PHOTONICS?

A new research project led by the University of Southampton is trying to establish if germanium, a group IV semiconductor, can be used as the material of choice in mid-infrared (mid-IR) photonics circuits and sensors.

Mid-IR group IV photonics have a number of important application areas, such as chemical and biological sensing, environmental and hazardous substance monitoring, medicine, telecommunications, astronomy, defence and security. So far, research in mid-IR group IV photonics has focused on silicon-based devices for shorter wavelengths due to its availability, low cost, maturity of fabrication processes, possibility for photonics-electronics integration and good transparency. However, the transparency of silicon only extends up to eight micrometres (μm) and as such it is not very suitable as a core material for the mid-IR fingerprint band (8-14μm). The Mid-Infrared GeRmAnium phoTonIcs fOr seNsing (MIGRATION) project will investigate germanium as an alternative platform to silicon to future-proof emerging technologies in this field. Significantly, compared to silicon, germanium offers a number of other advantages in terms of device development, including higher non-linear coefficients, better carrier mobility and the potential to produce active devices based on germanium-based alloys.



Novel mid-IR waveguide structure for sensing applications

One of the main outcomes of the project will be to identify high-quality germanium substrates that rival the performance of the well-established silicon-on-insulator wafers. This framework will then be used to demonstrate a library of devices such as waveguides, couplers, filters, amplifiers and modulators that will form the building blocks of integrated on-chip circuits, systems and sensors over an extended wavelength regime.

This interdisciplinary project is funded by the Engineering and Physical Sciences Research Council (EPSRC).

ANALOG DEVICES BREAKS THROUGH THE DIGITAL POWER BARRIER

High-performance semiconductors developer Analog Devices (ADI) has introduced its ADP1055 advanced digital power controller with PMBus interface for high-density, isolated DC-to-DC power supply system applications. The ADP1055 combines ADI's high-resolution, high-speed A/D converter sensing technology with proprietary non-linear transfer functionality to achieve high-bandwidth performance and transient response equivalent to traditional analog switching controllers.

The ADP1055 is a versatile digital controller with six PWM (pulse-width modulation) logic outputs that can be programmed with a GUI (graphic user interface) via the PMBus interface. The device makes possible high energy-efficiency topologies including full bridge with precision drive timing and control of secondary synchronous rectifiers. The controller's GPIO (general-purpose I/O) can be configured for active clamp, secondary, energy-efficient snubbing. Energy efficiency is further optimized by using adaptive dead-time compensation to improve efficiency over the load range. Programmable light-load-mode operation combined with low device-power-consumption (< 150mW) reduces system stand-by losses.

The ADP1055 provides accurate analog and digital fault signalling via the PMBus and configurable GPIO. The device also records the first instance of each fault and provides a 'black box' fault-history recording capability, ideal for analyzing system failure mechanisms and reliability.

The ADP1055 digital power controller's GUI enables customers to design and store settings in the high-reliability, internal EEPROM memory.

The digital power controller is available in a 5mm x 5mm LFCSP package.

Analog Devices (ADI) introduces ADP1055, an advanced digital power controller with PMBus interface

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POWER MANAGEMENT IN NOISE-SENSITIVE APPLICATIONS

By Landa Culbertson, Mouser Electronics

A careful, systematic approach is required when designing the power distribution system in noise-sensitive applications like broadcasting. Not only must one consider parameters like input voltage, output voltage, and current, but also how to handle PSU noise to eliminate effects on the system's video and audio signal integrity.

Choose Linear Regulators with Low-Noise and High PSRR Characteristics

Whenever possible, choose linear regulators to directly power the signal conditioning and signal processing components. All voltage regulators introduce noise into the system, but linear regulators inherently produce less noise than switching devices. Linear regulators can also offer good power supply ripple rejection (PSRR), also known as audio-susceptibility. A high PSRR specification at the switching frequency of any switch mode power supply fed into the linear regulator input will help attenuate that switching noise so that it does not get introduced to the signal chain and cause interference issues. This technique is called post-regulation.

Keep in mind that PSRR falls off eventually to 0-dB at higher frequencies. Most switch mode power supplies operate in the 100kHz to 2MHz range, so this is not an issue as it relates to the linear regulator's ability to attenuate the fundamental switching frequency. However, additional filtering may be required to dampen noise at high frequencies.

The task of choosing a linear regulator can be overwhelming considering the plethora of devices in the market, amid a myriad of manufacturers. Texas Instruments alone, after their merger with National Semiconductor, now offers over 1300 linear regulators. Mercifully, some companies provide online parametric search tools that allow one to narrow selections based on output noise as well as PSRR.

Table 1 highlights some linear regulators with exceptional noise specifications.

Unfortunately, it is not practical to use only linear regulators in every situation, as they are not very efficient at power conversion, and thus can get hot. Calculate the power dissipation in the application using Pdiss=(Vin – Vout)*Iload , and compare the wattage against the thermal rating of the package. If it looks like there are going to be heat issues, opt for more thermally enhanced packages like QFN, or it may be time to consider a switching converter instead. Generally speaking, this is the case if the load circuit continuously draws much above 1A. However, there are 1.5-A, 2-A, and 3-A rated linear regulators commonly available.

Switching DC/DC Converters Offer High Efficiency

Selecting a switching DC/DC converter is an even more daunting task. There are multiple topologies and trade-offs to consider, not to mention a multitude of suppliers. In any case, when faced with a noise sensitive application, implement a switching DC/DC converter with low output voltage ripple, say, less than 30 mVpp. Follow up the switcher with a linear regulator for post-regulation if a more quiet power supply is desired.

One feature to look for in a switching regulator intended for a broadcasting application is high switching frequency. Besides the benefits of smaller package and better transient response, high switching frequency avoids the frequency bands where noise can be disruptive, including the AM broadcast band.

Another desirable feature is switching frequency synchronization. In a system with multiple converters, similar, but not matching switching frequencies can produce a disturbance called beat frequency

Table 1:

Supplier	Device	V_{in} (V)	V_{out} (V)	I_{out} (A)	Output Noise	PSRR
Intersil	ISL78302A (Dual)	2.3 to 6.5	1.2 to 3.3	0.3	30 µVRMS	90-dB @ 1kHz
Intersil	ISL80111	1 to 3.6	0.8 to 3.3	1	100 µVRMS	70-dB @ 1kHz
ON Semi	NCV8570B	2.5 to 5.5	1.8V, 2.8V, 3.0V, 3.3V	0.2	10 µVRMS	82-dB @ 1kHz
ON Semi	NCP565	2.5 to 9	0.9 to 7.7	1.5	28 µVRMS	75-dB @ 1kHz
TI	LP5907	2.2 to 5.5	1.2 to 4.5	0.25	10 µVRMS	82-dB @ 1kHz
TI	TPS7A4700	3 to 36	1.4 to 20.5	1	4.17 µVRMS	78-dB @ 1kHz
TI	TPS7A8101	2.2 to 6.5	0.8 to 6	1	23.5 µVRMS	80-dB @ 1kHz

Table 2:

Supplier	Device	V_{in} (V)	V_{out} (min) (V)	I_{out}	Output Voltage Ripple (mVpp)	Switching Frequency	Freq Synch	Power Seq	Soft Start	Power Good
Intersil	ISL8206M Power module	1 to 20	0.6	6	8	600 kHz	No	No	Yes	No
On Semi	NCP1592 Switcher with integrated FETs	3 to 6	0.891	6	10	280 kHz to 700 kHz	Yes	No	Yes	Yes
TI	TPS54620 Switcher with integrated FETs	4.5 to 17	0.8	6	33 (per EVM)	200 kHz to 1.6 MHz	Yes	Yes	Yes	Yes
TI	TPS84621 Power module	2.95 to 14.5	0.6	6	30	250 kHz to 780 kHz	Yes	Yes	Yes	Yes

phenomenon. The ability to synchronize the switching frequencies of the regulators prevents the formation of beat frequencies. In addition, it helps keep the EMI generated within the system to a predictable set of frequencies.

Also consider that today's designs are implementing FPGAs and DSPs that are pushing the limits of technology, with some unintended consequences. A given device may need power sequencing, soft-start, or power-good indication to operate properly. Modern power management solutions integrate these capabilities.

Table 2 lists switching dc/dc step-down converters with desirable features for broadcasting applications.

Conclusion

Power supply noise reduction is a complex subject and part of a good power distribution system design is in choosing the right voltage regulators. However, keep in mind that there are other important factors that are beyond the scope of this article, including proper bypassing, decoupling, damping, PCB layout, and much more. Thankfully, there are many great resources for additional information on these topics including www.mouser.com

For more information on technologies and applications, visit uk.mouser.com/applications

What Does "Quality" Actually Mean?

MYK DORMER IS A SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD **WWW.RADIOMETRIX.COM**

Of all the subjects discussed in engineering management circles, the much argued-over area of "quality" is the one subject I never thought I would write about. Too much has already been said about it already. Whole books have been written about it, and it still varies between a barely understood buzzword and something close to an article of faith – depending on the author or company in question.

Even the use of the word is complicated. We talk about good and bad quality quite plainly, but then muddy the waters when we implement quality processes or strive for a "quality" product as if "good quality" and "quality" were synonymous.

> No process, instruction, order or procedure is worth the paper it is written on unless the people doing the work are capable, skilled, motivated and happy

In a very inexact, woolly sort of sense, there seems to be a general understanding in engineering today: rather than quantifying the value or innovative nature of an actual product or item, "quality" refers to the manufacturing and, in some cases, the design processes being predictable, traceable and offering good yields. It's a measure of how nebulous the word is, that in the preceding sentence, I was almost unable to avoid using the word to describe itself. Perhaps it would help to define what it isn't:

- **Quality isn't just a process.** There is no corpus of rigid guidelines that can be distilled down into a set of rules, regulations, documents and tests that, if followed with blind obedience, will yield the desired result.
- **Quality isn't a medicine for sick companies:** If the basic engineering underlying a company's products is poor, no amount of diligence and rigour in the manufacturing or administrative processes will save it. There is no point in a 100% yield if the product in question is second rate.
- **Quality isn't a religion.** It isn't something to "believe in" and you can't convert to it. Wanting quality will not, by the act of wanting, realize it, and tens of thousands of written or spoken words will not summon it up.

Lack of attention to quality on the other hand, is much easier to diagnose. There are some very clear markers:

- **Inconsistency:** The rate of defects in delivered batches varies at random. Products from one batch might perform flawlessly; a second batch might have a high proportion of failures, or all the units received might have slightly different parameters.
- **Unpredictability:** Delivery times, quoted prices and levels of support vary without apparent cause, and communication with the company does not always elicit a consistently rapid and professional response.
- **Untraceability:** It is never possible to track down the actual reason for a unit's failure. Either a different explanation is given every time, or no clear reason is evident. At every level the documentation tends to be sparse and/or incomplete.

These indicators suggest an absence of quality but (saving the hardest bit until last) it is not so easy to define what makes for (good) quality:

In my embarrassingly simplistic opinion, it is people. No process, instruction, order or procedure is worth the paper it is written on unless the people doing the work are capable, skilled, motivated and happy. Even without exacting guidelines, complex instructions or step-by-step management, a competent team with good morale, working together, will achieve good quality simply by co-operation. Faults at any stage will be reported up and down the hierarchy because the reporter cares about what they are doing, and co-workers are prepared to listen.

How to recruit skilled staff and maintain their good morale are far, far harder questions, and must wait for another day. ●

AC POWER SUPPLIES

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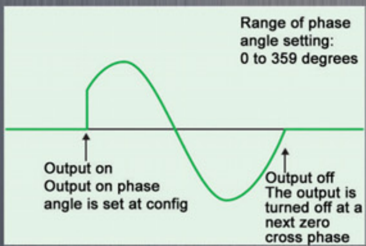
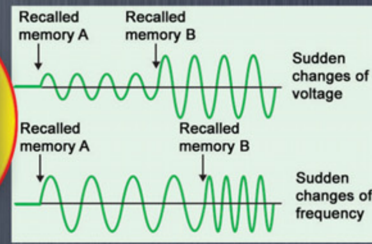


Memory Function



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Safety-critical industries tend to embrace software test processes such as unit and integration testing, code coverage analysis, regression testing and continuous test as best practices. While it is widely known that test is essential for developing quality software, many organizations not in the safety-critical industries consider exhaustive software testing to be too time-consuming and costly to implement. By letting "the perfect be the enemy of the good", business-critical applications are facing increasing software quality problems. Since complete testing is critical to developing good quality software, the good news is that organizations can gradually implement a structured software-test process and achieve benefits right away, not years down the road.

"Code coverage analysis during system testing provides an instant metric of its completeness

Step 1: Using code coverage to understand the current state of testing

Since system testing is practiced by nearly everyone, it makes sense to optimize it first. Code coverage analysis during system testing provides an instant metric of its completeness. In order to maximize efficiency, a code coverage tool should be able to perform the following actions:

- Identify which lines of code are being executed and which are not. Using the example in Figure 1, the source lines are colour-coded: the lines that have been executed are in green and those that are not in red.
- Provide a way to understand the cause of particular lines being covered. There are different ways to do this: displaying a back-trace of the covered line to the test case(s) that executed that line of code (as shown in Figure 2), or tracking the execution flow and "replaying" that flow after testing is complete.
- The tool should be able to capture coverage directly on the same hardware where the final application will be deployed,

```
2 6     *      switch(Order.Entree)
               {
2 7     (T)       case NO_ENTREE :
2 8     *            break;
2 9     (T)       case TIKKA :
2 10    *            Table_Data.Check_Total = Table_Data.Check_Total + 14.0;
2 11    *            break;
2 12    (T)       case JIROU :
2 13    *            Table_Data.Check_Total = Table_Data.Check_Total + 10.0;
2 14    *            break;
2 15    ( )       case ROTI :
2 16                 Table_Data.Check_Total = Table_Data.Check_Total + 18.0;
2 17                 break;
2 18    (T)       case MIANTIAO :
2 19    *            Table_Data.Check_Total = Table_Data.Check_Total + 12.0;
2 20    *            break;
               }
2 22    *      Update_Table_Record(Table, Table_Data);
```

Figure 1: A code coverage tool shows which lines of code are being executed, and which ones are not

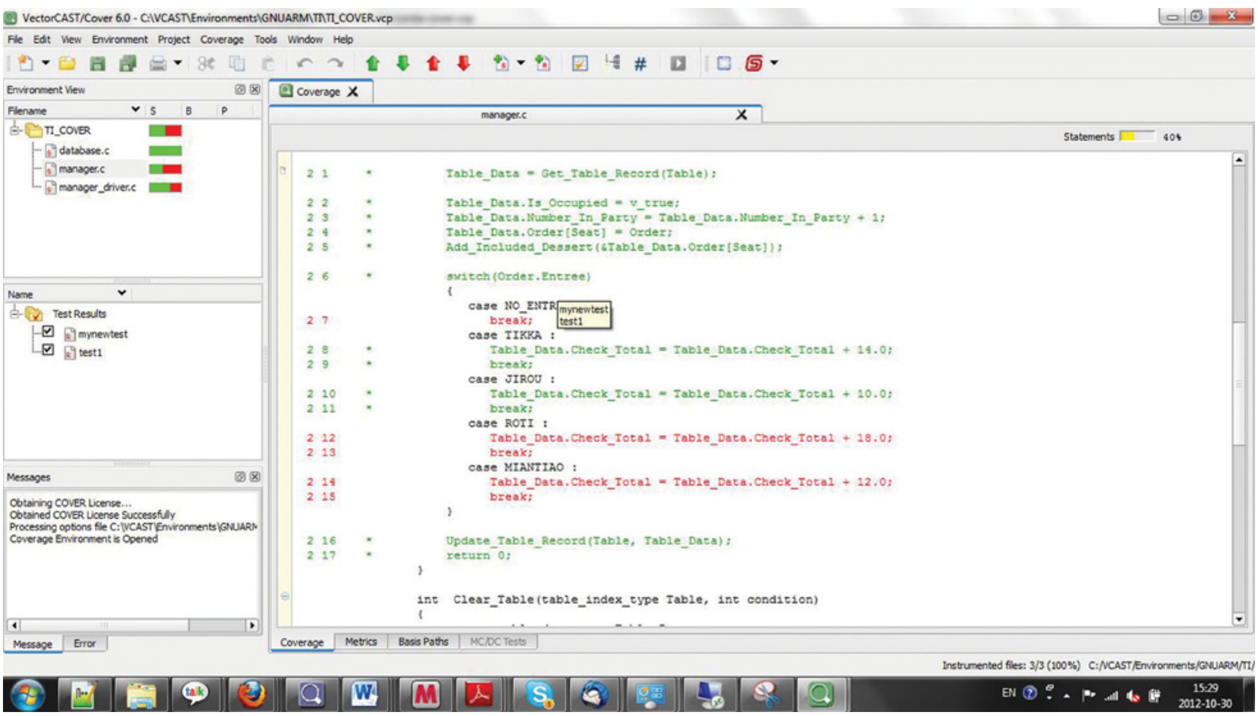

Figure 2: The test tool should clearly show how coverage was generated

and if necessary dump its output through different peripheral interfaces.

- Finally, the tool should be easy to integrate into the build cycle of the application using a command line interface.

Code coverage will give an accurate report of the thoroughness of the existing testing environment. The effort required to set up code coverage at the system-testing level is minimal and it integrates nicely into activities that are already being performed. Although it is unlikely that existing tests provide 100% code-coverage, you might be shocked to discover that only 60% to 70% of the application is being tested. By analyzing the reports however, it may not require much additional effort to achieve 80% – a reasonable goal for system testing.

Step 2: Extending code coverage with module testing

Once you have the code coverage during system testing and have analyzed the results, the next goal might be to test the remaining portions of the application using a module-testing technique. The goal here is simply to ensure that all lines of code are executed at least once, not to prove the code is correct. There are two paths to achieve this result:

- Import the code coverage generated during system testing and generate new module-level test cases manually to cover lines that remain untested.
- Auto-generate test cases to achieve code coverage quickly. For instance, some tools allow basic path analysis to auto-generate test cases that may provide very high levels of code coverage.

One advantage of auto-test case generation is that it will also provide an overview of the code's robustness at a unit level. For instance, if a minimal value causes a crash or some corruption, it may mean that additional defensive code should be implemented. These methods can be adopted in tandem, by first augmenting coverage with auto-generated test cases and then finalizing the code coverage by hand-building a test case to provide the remaining coverage.

Step 3: Testing individual modules correctness

Once a project has been set up so that each line of code is tested at least once, additional efforts can guarantee a high level of software quality by testing individual units and modules for correctness. A unit-test tool is the ideal choice for this type of test, permitting the user to specify input and expected values for parameters, global variables, even variables being used in the middle of functions when these functions are stubbed. Focusing on test correctness may yield interesting discoveries, since an issue may not take down the system immediately, but cause issues later if allowed to remain in the code.

This can be accomplished by taking the unit tests created for coverage in the previous step and adding expected results data to the test cases, which the tool will use to assess


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the pass/fail status of the test and therefore the correctness of the code.

Step 4: Automated regression testing over the project lifecycle

All the activities described so far have focused on a specific code base, which is a snapshot of a project at a given point in time. As every developer knows, code does not sit still – fortunately, solutions exist that make code changes a non-issue. One method is to use a system-test code coverage tool that is integrated in the build setup to quickly repeat the system testing. Another way is to have a tool that keeps track of everything: unit, integration, module and system testing environment tests, and reruns them automatically as needed.

A quality unit test tool would be able to reuse as much as possible of specific test cases, or subsequent baselines, even when the number of global variables changes or the range of possible values varies. Such a capability should also enable different users to collaborate in real time on the same project so the library of test cases can grow at a quicker pace.

Step 5: Empowering the development team

Once a library of test cases is established and the engineering team has become adept at generating test cases at either a unit or module level, it may prove advantageous to use the tool to test their code before it is committed to the source management system. Unit test tools make for a great "sanity check", because they quickly build a test harness around the code and stub dependencies, and they let developers run tests before the code is committed to the code management system.

It is possible to quickly run locally only the test cases impacted by a source code change, before the modified code is ever committed, keeping errors out of the committed code in the first place.

Gradual Testing

Implementing a gradual code-testing process offers many benefits, specifically the flexibility to adopt an incremental test approach that meets the needs of business, resources and budgets. In addition, it avoids disruptive changes to existing development processes and testing cycles in favour of a measured approach that builds on what has already been done and even improves upon it.

As shown in each of the five steps, the added benefits of testing automation are easily exploited as engineers become more acquainted with testing tools and concepts, ensuring that the code gets a much more complete review for limited additional effort. These efforts increase predictability and decrease the number of difficult – not to mention stressful – debugging sessions due to costly errors that made it to a late stage of development – or worse, when in the field.

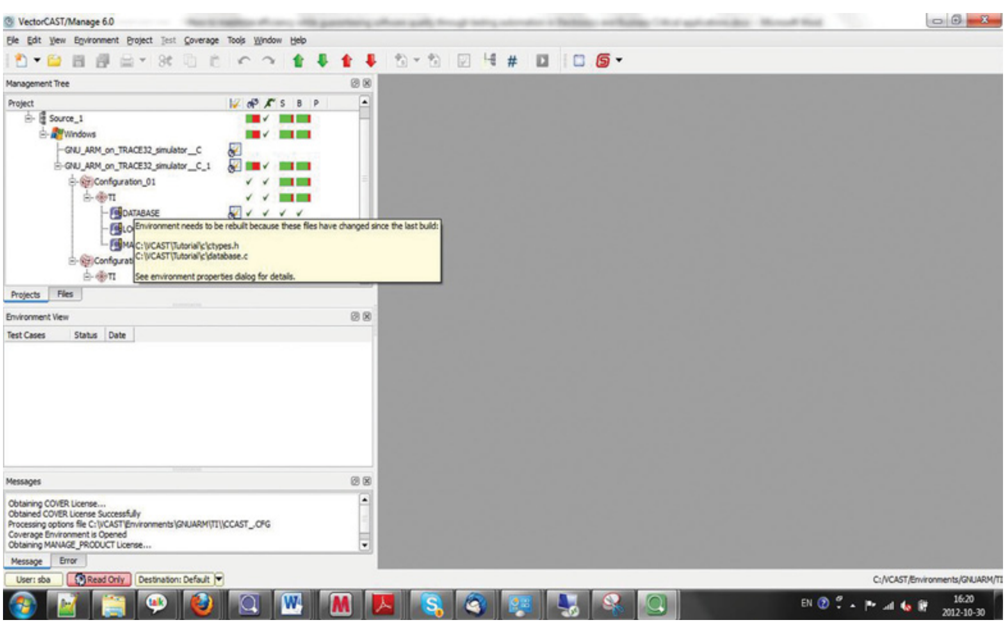

Figure 3: Integrating change-based testing into the test process provides a way to find regression errors early in the development cycle

HARDWARE IMPLEMENTATION OF A FAST FLOATING-POINT ADDER FOR EMBEDDED SYSTEMS

ONURSAL CETIN FROM SAKARYA UNIVERSITY, **EMRE OLMEZ** AND **FEYZULLAH TEMURTAS** FROM BOZOK UNIVERSITY AND **ETEM KOKLUKAYA** FROM GAZI UNIVERSITY, ALL IN TURKEY, PRESENT A DESIGN FOR AN IEEE SINGLE PRECISION FLOATING POINT ADDER AS ENTIRELY COMBINATIONAL LOGIC TO REDUCE LATENCY. THE DESIGN REQUIRES A LARGE AMOUNT OF HARDWARE, BUT THE RESULT REQUIRES ONLY A SINGLE CLOCK-CYCLE

Floating-point addition is frequently used for high precision calculations. Due to its complexity, it is hard to implement on adaptive hardware. However, FPGAs (Field Programmable Gate Arrays) are suitable platforms to implement complex digital computations such as floating point additions that require a large number of logic gates.

Various applications of floating-point adders in FPGAs are presented in the literature. Pipelining techniques and parallel structure are used to implement a floating-point adder and an area reduction is then achieved [1].

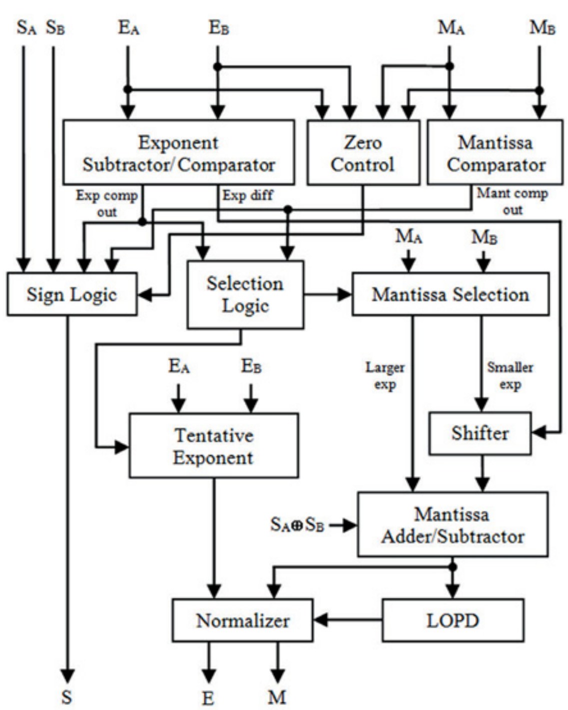

Figure 1: Architecture of a fast floating point adder

Akkas presented the implementation of double precision, quadruple precision, dual-mode double precision and dual-mode quadruple precision adders in VHDL [2]. Reference [3] presents a dual-mode quadruple precision floating point adder design that uses conventional floating point addition algorithm. In Reference [4], delay due to leading zero detection is eliminated by predicting the number of leading zeros without waiting for the result from the mantissa adder. The multi-path floating-point adder/subtractor with separate operations is presented in Reference [5].

Krueger and Seidel designed an on-line floating-point adder, fully compliant with the IEEE standard [6]. High performance, low latency floating-point adder construction methods are described in a Virtex-4 board [7].

In this article, an entirely combinational logic design of an IEEE single-precision floating point adder is implemented in a single FPGA by using the Quartus II software.

Single Precision Floating-Point Number

According to the IEEE 754 standard, the 32-bit (single precision) floating-point number is composed of three parts: sign S (1 bit), exponent E (8 bits) and mantissa M (23 bits) [8]. The most significant bit is the sign bit; 0 indicates a positive number and 1 indicates a negative number.

The next eight bits denote the exponent part of the number. A bias value is added to the actual exponent in order to represent both negative and positive exponents. The last 23 bits represent the mantissa of the number. The leading bit of the mantissa is a hidden 1 that does not need to be represented explicitly.

System Model

The architecture of the fast floating-point adder is shown in Figure 1. Two 32-bit floating-point operands A and B are presented to the system as input. Exponent parts of the operands are compared and subtracted by the Exponent Subtractor-Comparator to produce exponent difference and comparison results.

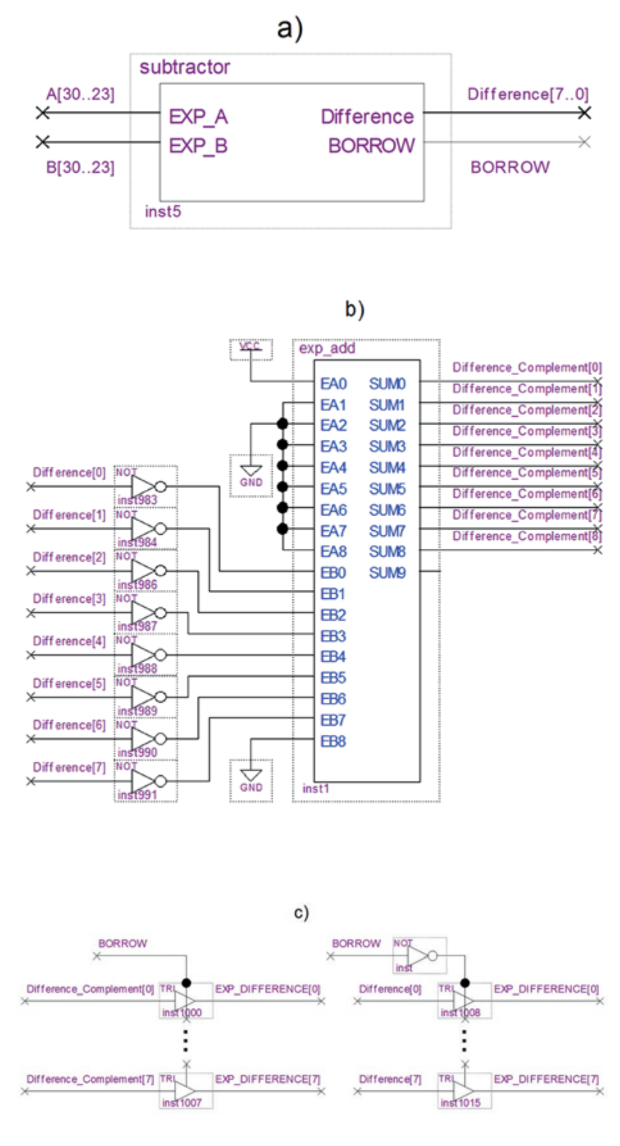

Figure 2: Exponent difference selection: (a) 8-bit subtractor; (b) 2's complement circuit; (c) tri state buffers

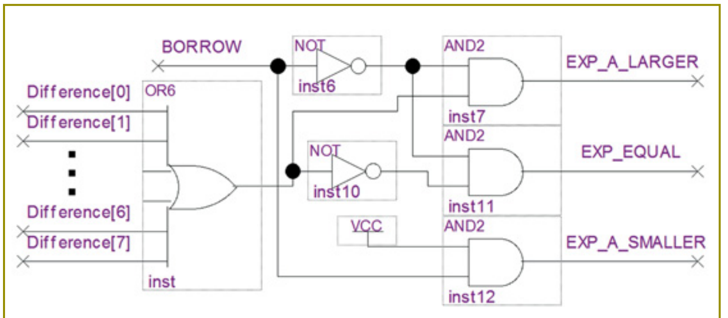

Figure 3: Logic circuit design of the comparator part for exponents

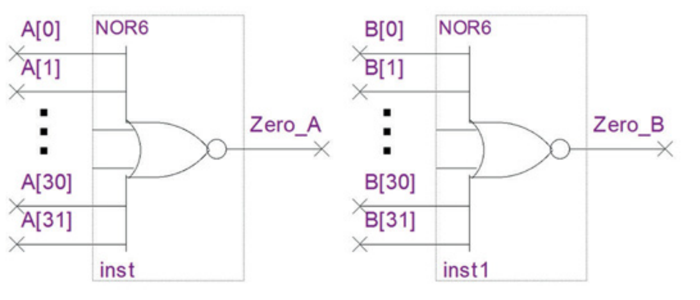

Figure 4: Zero control logic

The exponent and mantissa parts of the operands are given to the Zero Control unit to check if the operands are zero. The Mantissa Comparator subtracts one mantissa from the other mantissa and gives a comparison result. The Sign bit is determined by the Sign Logic, depending on the exponent comparator output, mantissa comparator output, zero control logic output and sign bits of the operands.

Selection Logic is used to produce a control bit to determine a larger mantissa, smaller mantissa and a tentative exponent by using an exponent comparator output and mantissa comparator output. A Shifter is designed by using a tri-state buffer series instead of shift registers, thus a clock pulse is not required for shifting.

A smaller mantissa is shifted by the Shifter and transferred to the Mantissa Adder-Subtractor. This unit is divided into two separate circuits as a 24-bit adder and 24-bit subtractor for parallel processing. An addition or subtraction result is selected by a tri-state buffer series. A Leading One Position Detector is used to locate the position of the most significant one of the 25-bit data given by the Mantissa Adder-Subtractor. A normalizer unit is designed to normalize the mantissa and to update the exponent appropriately.

Exponent Subtractor-Comparator

A subtractor-comparator unit is implemented to determine the larger exponent and to compute the exponent difference, and for this purpose, an 8-bit subtractor is designed as a fundamental part.

The exponent difference is calculated by the subtractor. The subtraction result or its complement is transferred to the output by using two separate tri-state buffer series according to the borrow bit of the exponent difference. If an exponent of A (EA) is greater than or equal to an exponent of B (EB), the subtractor produces 0 as borrow and the difference is directly transferred to the output. Where EB is greater than EA, the subtractor produces 1 as borrow and the 2's complement of the exponent difference is transferred to the output. In Figure 2, (a) shows the 8-bit subtractor, (b) shows the 2's complement circuit that consists of NOT gates and an adder, and (c) shows the tri-state buffer series which selects the subtraction result or its 2's complement.

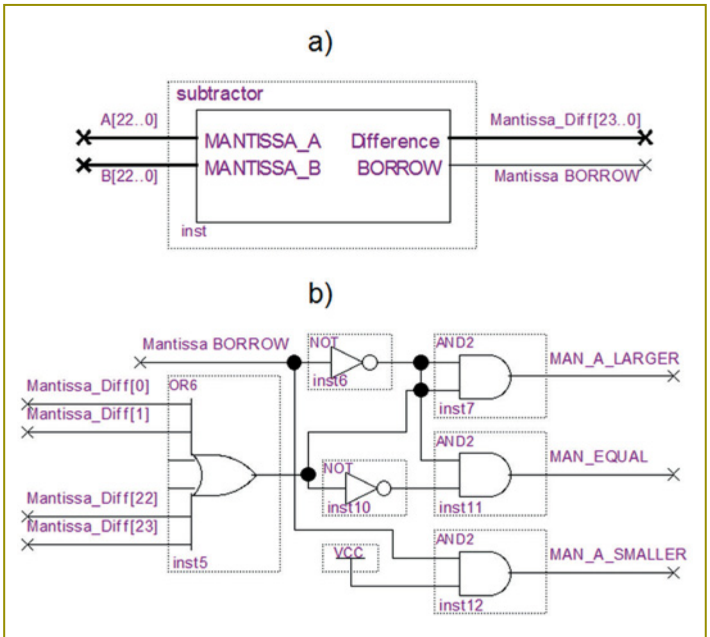

Figure 5: Mantissa comparator: (a) 24-bit subtractor; (b) comparison logic

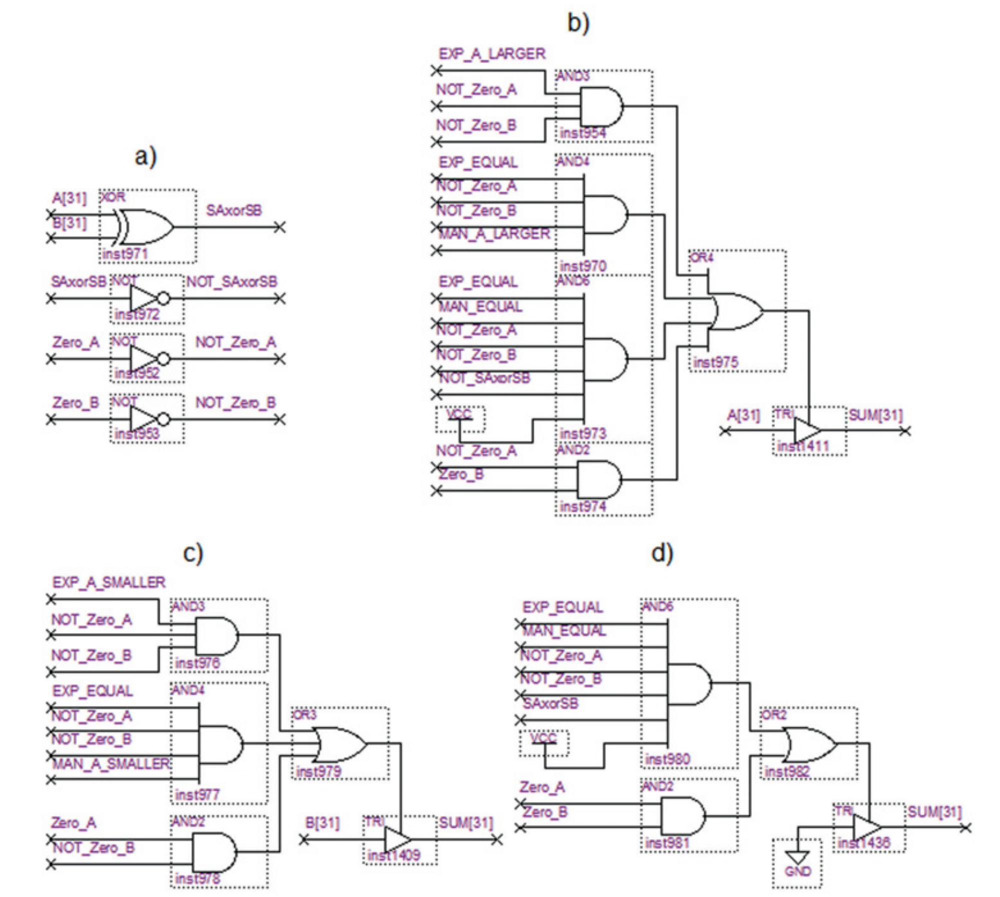

Figure 6: Sign logic

The exponent subtractor-comparator unit generates two types of outputs as difference and comparison. Its comparator output is based on the value of input A being greater than, smaller than or equal to the value of input B, depending on the exponent difference and borrow bits. The logic circuit design of the comparator part is shown in Figure 3.

> “ The adder is designed as an entirely combinational logic that performs addition and subtraction operations in parallel

Zero Control Logic

The zero control logic is made up of NOR gates to check if the operands are zero. If one of them is zero, the other one is transferred to the output directly. If both are zero, the output is set to zero. As seen in Figure 4, each of the circuits produces the output 1 when all inputs are zero but produce 0 otherwise.

Mantissa Comparator

Another combinational logic circuit is the mantissa comparator circuit. A mantissa comparator consists of 24-bit subtractor and comparison logic made of AND, OR and NOT gates. Before comparison, the hidden bit of the mantissas must be made explicit. According to the IEEE standard, if the exponent and mantissa field are equal to 0 the hidden bit is set to 0, otherwise the hidden bit is set to 1.

In Figure 5, (a) shows a 24-bit subtractor and (b) shows the comparison logic. The 24-bit subtractor subtracts one mantissa from the other and gives outputs as difference and borrow bits. The comparator circuit takes the mantissa difference and borrow bit as input and gives the comparison results.

Sign Logic

The sign logic consists of AND gates, OR gates and tri-state buffers to determine the sign bit of the floating-point adder result. In Figure 6, (a) shows the control bits, (b) shows the selection of sign bit for operand A; (c) shows the selection of sign bit for operand B; and (d) shows the selection of zero as sign bit.

According to Figure 6, one of the sign bits A[31], B[31] or 0 is transferred to the output, depending on the exponent comparator output, mantissa comparator output, zero control logic output and sign bits of the operands.

Selection Logic and Mantissa Selection

The selection logic that includes AND, OR and NOT gates is used to produce a control bit named SEL_LOG. For this purpose, the logic circuit takes an exponent comparator output and mantissa comparator output as input to produce SEL_LOG. The selection logic is given in Figure 7.

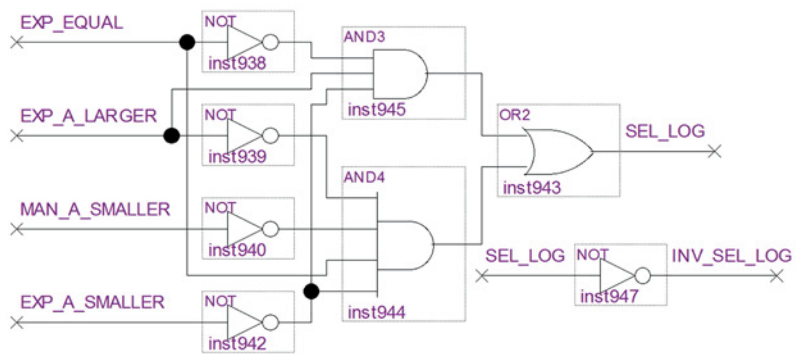

Figure 7: Logic circuit of selection logic

A larger mantissa, smaller mantissa and larger exponent as tentative exponents of the result are determined by using a tri-state buffer series depending on SEL_LOG. In Figure 8, (a) shows a smaller mantissa selection logic; (b) shows a larger mantissa selection logic; and (c) shows tentative exponent selection logic.

Shifter

Here we designed a clock-independent and low-latency shifting system instead of using conventional shift registers. The shifter consists of an 8 x 256 decoder and a tri-state buffer series. The 8 x 256 decoder is a combinational circuit that converts an 8-bit exponent difference to 256 output lines. The outputs of the decoder from 24 to 256 are combined using OR gates, and a single value is obtained. Thus, the output number of the decoder is reduced to 25 (SHIFT_SEL[0] to SHIFT_SEL[24]). The block diagram of the combinational circuit is shown in Figure 9.

The mantissa of the smaller operand is shifted right by the exponent difference amount. The mantissa can be shifted maximum 24 times. If the exponent difference is greater than 24, the shifted mantissa is set to 0. For this purpose, 25 tri-state buffer series are implemented and the shifted values of the mantissa given to the tri-state buffers separately. As seen in Figure 10, for the right shifting operation, the left-most bit (high-order bit) is replaced by a zero bit and the right-most bit (low-order bit) is discarded at each tri-state buffer series. The figure shows the operation performed on 24 bits. According to the decoder output, only one of the tri-state buffer series is activated, thus shifted data is determined (Shifted_Man[0] to Shifted_Man[23]) and transferred to the Mantissa Adder-Subtractor (MAS).

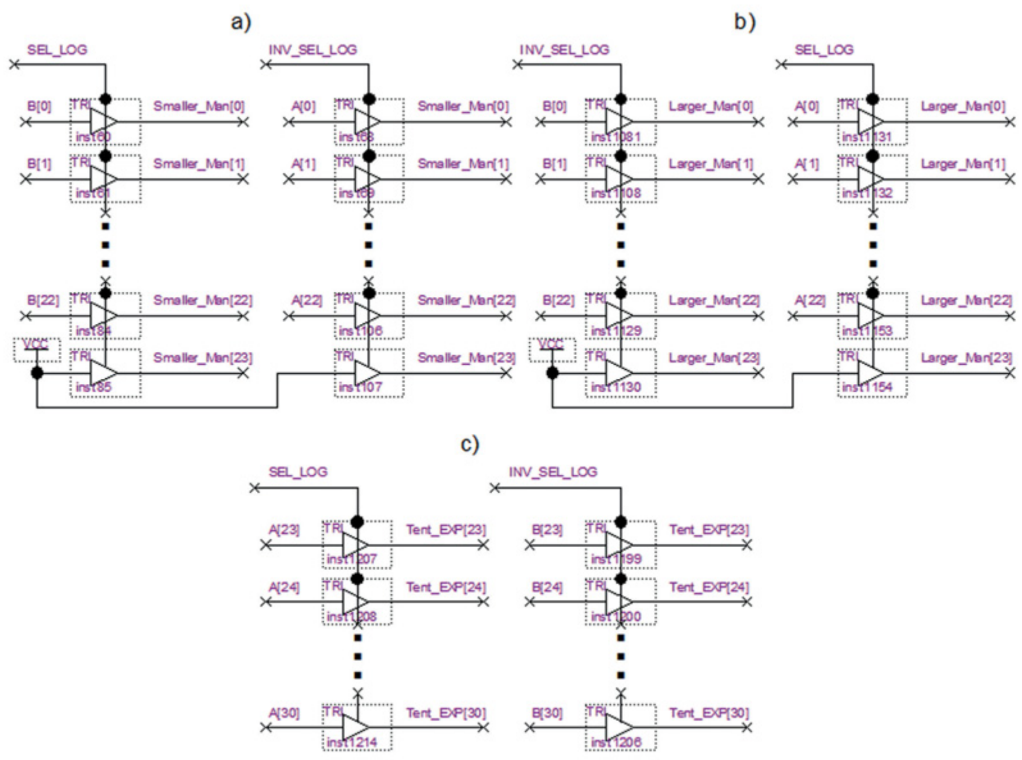

Figure 8: (a) Smaller mantissa selection logic; (b) Larger mantissa selection logic; (c) Tentative exponent selection logic

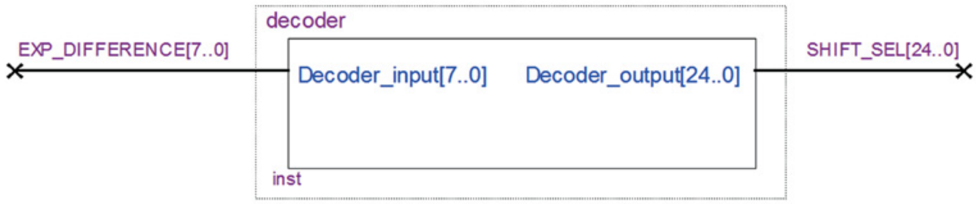

Figure 9: Decoder

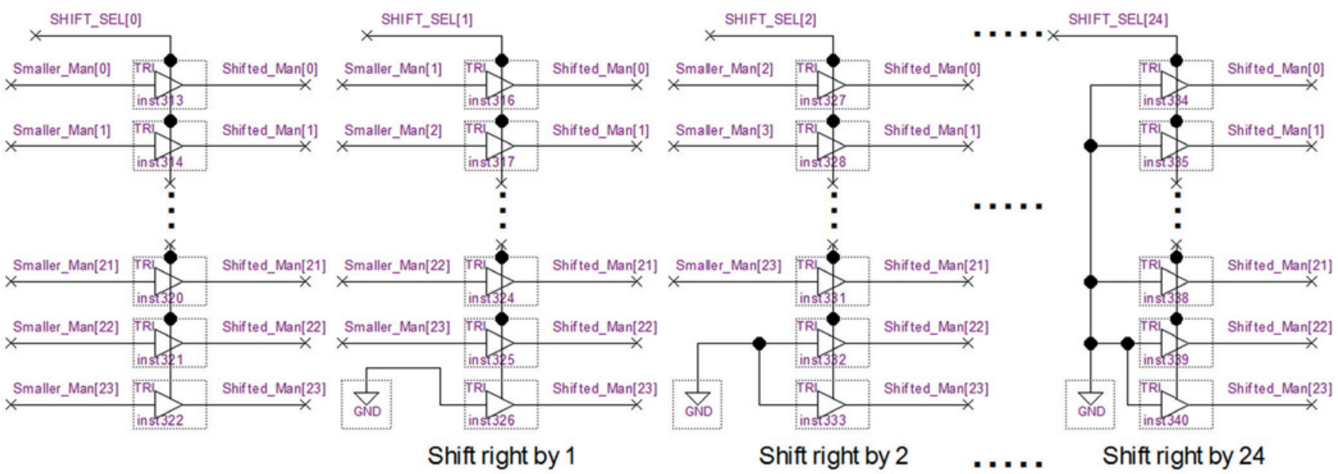

Figure 10: Shifted mantissa selection

Mantissa Adder-Subtractor

The MAS is divided into two separate circuits for parallel processing. For this purpose, a 24-bit adder and 24-bit subtractor are designed as seen in Figure 11. The larger mantissa and shifted mantissa are given as input to both the adder and subtractor. An addition or subtraction result is selected by the tri-state buffer series depending on the signs of the input operands. The addition result is chosen when the XOR operation of sign bits is 0, otherwise the subtraction result is chosen. The unit forms 25-bit (MAS[0] to MAS[24]) result (including carry out or borrow out) for the Leading One Position Detector (LOPD) and Normalizer, respectively.

Leading One Position Detector

An LOPD is used to locate the position of the most significant one of 25-bit data given from MAS. LOPD consists of AND gates, NOT gates and a 25-bit adder as seen in Figure 12. The MAS result is given in reverse order as input to the NOT gates; afterward the data is incremented one by using a 25-bit adder. In the last stage of the LOPD, a logical AND operation is performed on two inputs: the output of the 25-bit adder and the input data of the LOPD. As a result, 25-bit data containing all zeros – except the leading one position – is generated.

Normalizer

In order to normalize the mantissa and update the exponent appropriately, a Normalizer unit is used. It consists of a Mantissa Shifter (MS) and an Exponent Adjustment Logic (EAL). The LOPD result is used as selection bits for MS, which includes 25 series of tri-state buffers.

The logic circuit design of the MS is shown in Figure 13. Shifted values of the result of MAS and the exponent increment/decrement values (1 for increment, 0 to 23 for decrement) are given to the tri-state buffers, respectively. One of the tri-state buffer series is activated according to the selection bit, thus a mantissa of the result is determined and an exponent increment/decrement value is transferred to the EAL.

> “Because of using tri-state buffer series, a clock pulse is not required for shifting operation and thus the result is generated at only a single-cycle period

The EAL consists of an 8-bit adder, 8-bit subtractor and a selection logic that includes three tri-state buffer series. Addition and subtraction operations are performed separately to reduce latency. The exponent of the larger operand is incremented by an 8-bit adder if the MAS result presents a carry, and decremented by the subtractor

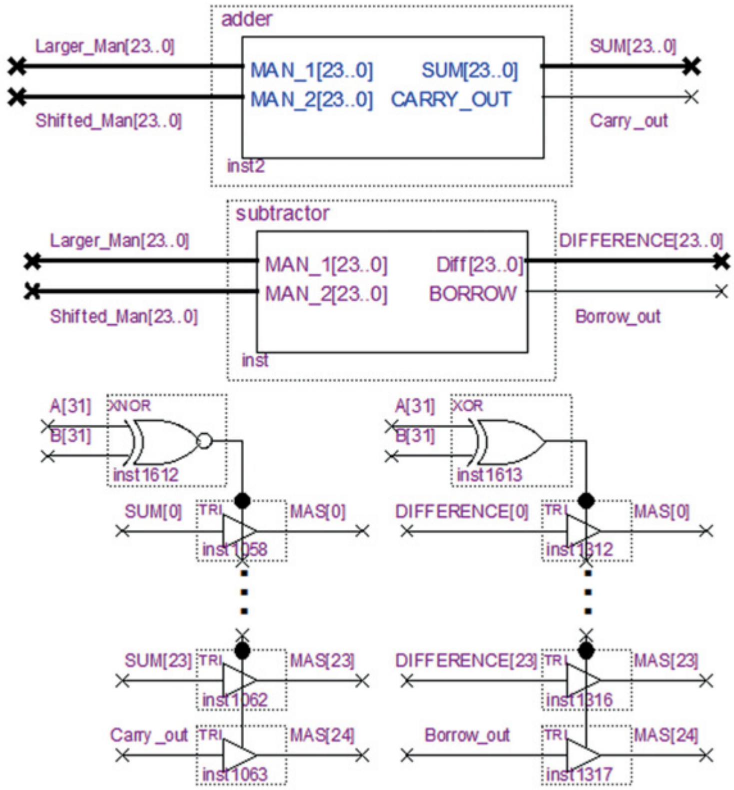

Figure 11: Mantissa adder-subtractor

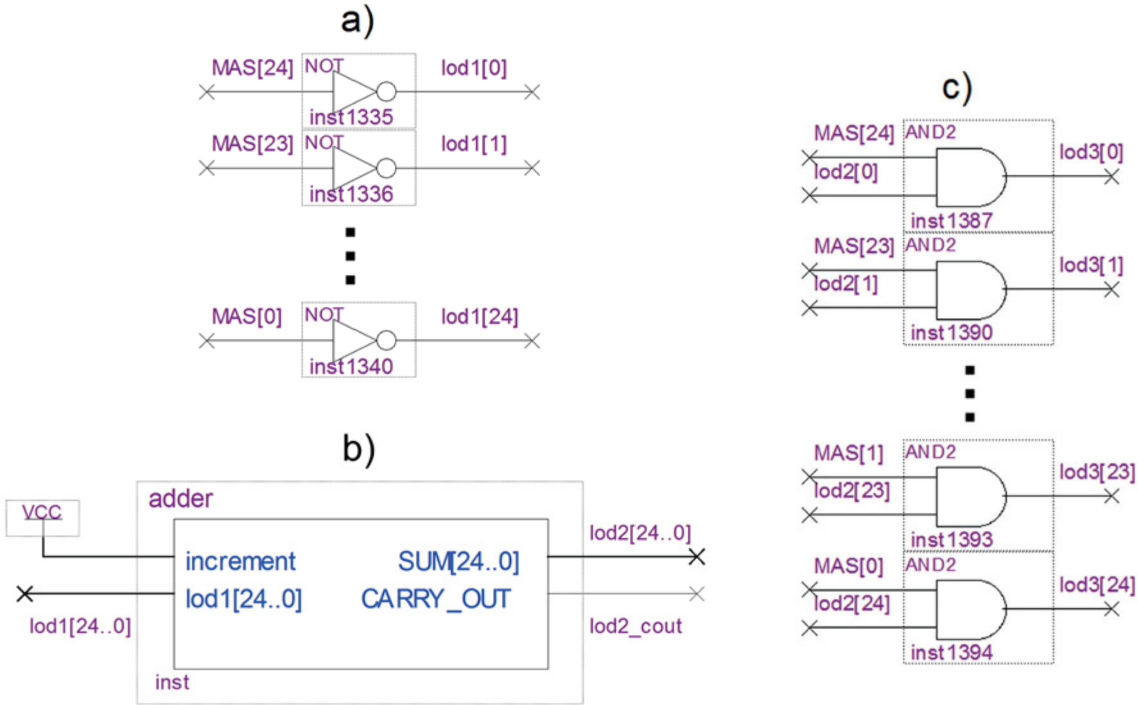

Figure 12: Leading one position detector

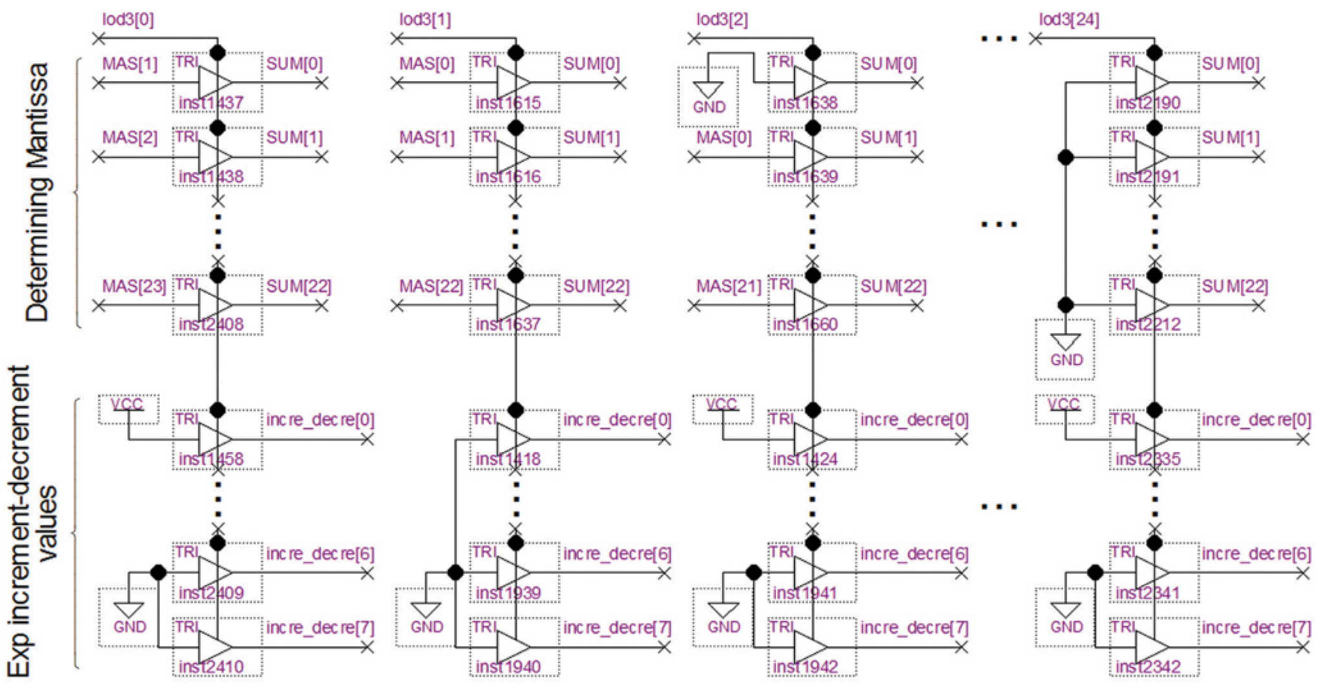

Figure 13: Determining the mantissa and exponent increment/decrement value

if the MAS result presents a cancellation of its most significant bits. If both operands are zero, the exponent is set to zero; thus the exponent is updated by EAL.

Result and Conclusion

This article presents a hardware design of a fast floating-point adder that's fully compliant with the IEEE single-precision floating-point standard. The adder is designed as entirely combinational logic that performs addition and subtraction operations in parallel. The addition and subtraction results are internally linked to inputs of the tri-state buffer series which selects one of the results depending on the signs of the input operands. In addition, tri-state buffer series are used for shifting operations instead of shift registers for reducing latency. Because the use of tri-state buffer series, a clock pulse is not required for shifting and thus the result is generated in only a single clock-cycle.

The embedded floating-point adder consists of 864 logic elements, which takes up a large portion of the FPGA, but the proposed design is suitable for 32-bit additions at the cost of gate delays only. ●

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ADDING FLEXIBILITY TO THE FINAL DESIGN

LIMITATIONS OF SOLID SUBSTRATES ARE NOW LARGELY A THING OF THE PAST, AS EQUIPMENT MAKERS DISCOVER THE ADVANTAGES OF FLEXIBLE BOARD DESIGN. BY **BENJAMIN JORDAN**, SENIOR MANAGER FOR CONTENT MARKETING STRATEGY AT ALTIUM

The continued transition toward smaller and lighter devices seen in the consumer sector is crossing over into parts of the industry where typically larger and more power-hungry end-systems are the norm. Expectations are for functionality and performance to continue to increase, whilst sizes decrease or at least remain the same, leading to even tougher challenges for product developers. Components have continued to shrink in size in tune with Moore's Law, so the substrate for those components, or printed circuit boards (PCBs), have also had to evolve to meet those expectations. In some instances however, access, not size, may be the most important requirement in design.

For ease of manufacture, designing an end product may nowadays be aided by less mainstream but increasingly viable PCB approaches, one of which is the rigid-flex PCB technology.

The Best of Both Worlds

A rigid-flex PCB combines conventional rigid (FR4) substrates with flexible (film) materials in a single assembly that can be used to mount components and replace wiring looms or other discrete interconnects. This can make assemblies easier to manufacture and more reliable, whilst opening up a wider array of design options.

Although the manufacturing process may be more complex than that of traditional rigid PCBs, many PCB manufacturers now support rigid-flex PCBs. If the OEM and PCB manufacturer communicate from an early stage of the rigid-flex PCB's design, it can be of low complexity and yet provide a host of benefits in the final assembly phase. The flexibility of the final PCB is application-dependent, so if the aim is purely to provide simpler final assembly, there is no need for extensive flexibility; however if the aim is to support hinged movements that will require many operations, the design considerations should reflect this.

For some applications, such as those that require only a small amount of movement during assembly, it may be possible to use conventional materials. A rigid PCB gets most of its rigidity from the epoxy applied to the fibreglass that forms its inner layer. By not applying the epoxy, a PCB may actually offer the level of flexibility required by some assembly situations. However, when considering rigid-flex PCBs it is more applicable to assume the requirements will extend beyond a basic level of movement and thus it becomes necessary to consider the way most flexible PCBs would be made.

Drawing Parallels

The most common materials used for flexible circuits are Polyester (PET) and Polyimide (PI). Of the two, PI is the optimum; it offers flexibility and durability, as well as extreme heat tolerance, making it suitable for manufacturing processes that require multiple reflow cycles. To this layer, another one must be applied to insulate the conductive tracks and protect them from damage such as corrosion. This layer, which acts much like a solder mask layer on a rigid PCB, is often also formed from either PET or PI, and is called 'coverlay'.

In some applications, such as where flexibility is needed,

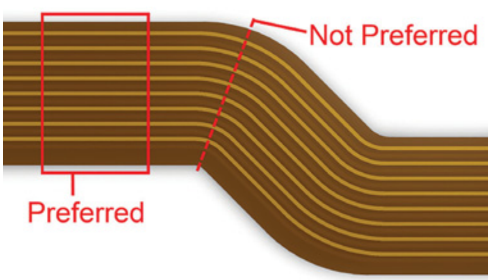


Figure 1: Preferred bend locations

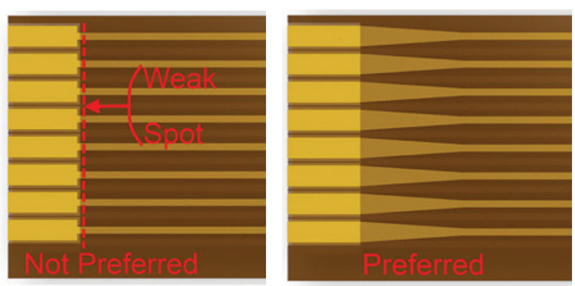


Figure 2: Trace width change and pad entries can cause weak spots

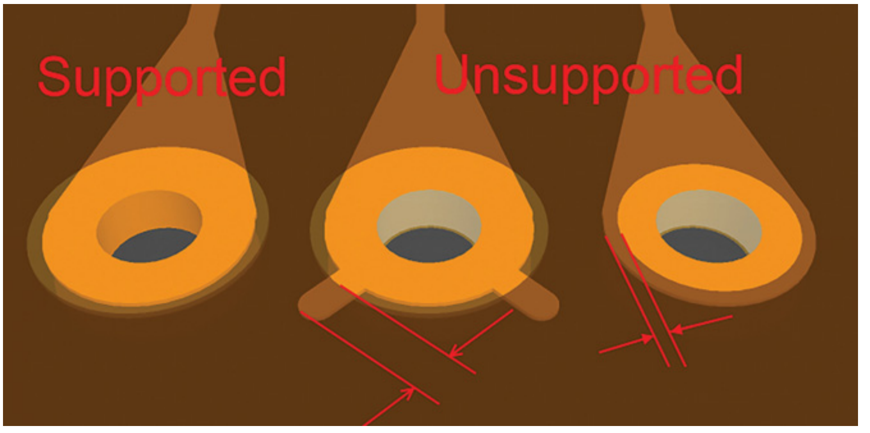


Figure 3: Supporting through-hole pads in flex with plating, anchoring stubs, and reduced coverlay access openings

purely to aid final assembly, the conductor used may be more conventional than expected. Traditional laminated copper foil, electro-deposited, can be used, often in high-current applications. However, if the application requires significant flexibility and/or repeated movement, the traditional approach may not be viable. Copper in this form is subject to fatigue, so to overcome this it may be advisable to use rolled annealed copper film. The process of annealing the copper removes stress in the Z axis, exactly what's needed in a flexible circuit.

Because the surface of annealed copper doesn't create a reliable bond to PI or other films using heat and pressure alone, it is necessary to employ a specially developed adhesive when using annealed copper. However, it is becoming more common to use copper plating or deposition directly on the PI film, removing the need for an adhesive and thereby retaining greater flexibility in the end assembly. This can be achieved through depositing a 'seed' layer of copper (often by vapour deposition, such as sputtering) to provide a base on which copper may be chemically deposited. Vias in the resultant one- or two-layer flexible PCB can then be drilled, plated and etched in much the same way they would in a conventional two-sided rigid PCB process.

One of the final stages in the manufacturing process is to combine the flexible circuit with a rigid PCB, to create a laminated stack-up. This can result in a PCB assembly comprised of multiple rigid and flexible parts, although no two flexible parts would be abutted. It is often advisable to apply a bead of epoxy or other adhesive where the rigid PCB meets the flexible circuit, to provide greater cohesion.

Design Considerations

There are several aspects of flexible PCB circuit design that, while not immediately obvious, may impact negatively on a first-time design. For example, 45-degree and 90-degree angles are used extensively in rigid PCB design, but should be avoided

Layer Type	Base Type	Description
Coverlay	solder_mask	Clearances of a coverlay layer
Covercoat	solder_mask	Clearances of a covercoat layer
Punch	route	Pattern for die-punching of the flex circuit
Stiffener	mask	Shapes and locations of stiffeners to be adhered
Bend Area	mask	Labelling of areas that will be bent while in use
PSA	mask	Pressure Sensitive Adhesive shapes and locations
Area	document	An area definition (Rigid, Flex, or arbitrary)
Exposed Area	document	An exposed area of an inner layer and its associated coverlay (could also be used for embedded components)
Signal Flex	signal	A signal layer for a flex circuit
Power Ground Flex	pg	A power of ground layer for a flex circuit
Mixed Flex	mixed	Mixed layer for a flex circuit
Plating mask	mask	A mask for defining which areas within a layer should be masked off from plating process
Immersion Mask	mask	A mask for defining which areas within a layer should be masked off for immersion gold

Table 1: Subset of Layer Types in ODB++ (v7.0 and later) used for GenFlex
(Source: ODB++ v7.0 Specification)

Layer	Name	Material	Thickness	Constant	Flexible	Rigid
1	Top Paste					
2	Top Overlay					
3	Top Solder	Coverlay (PI)	0.50mil	4		
4	Top Layer	Copper	1.40mil			
5	PIBase	Polyimide	1.40mil	4.8		
6	Dielectric 1	FR-4	12.00mil	4.2		
7	Bottom Layer	Copper	1.40mil			
8	Bottom Solder	Coverlay (PI)	0.50mil	4		
9	Bottom Overlay					
10	Bottom Paste					

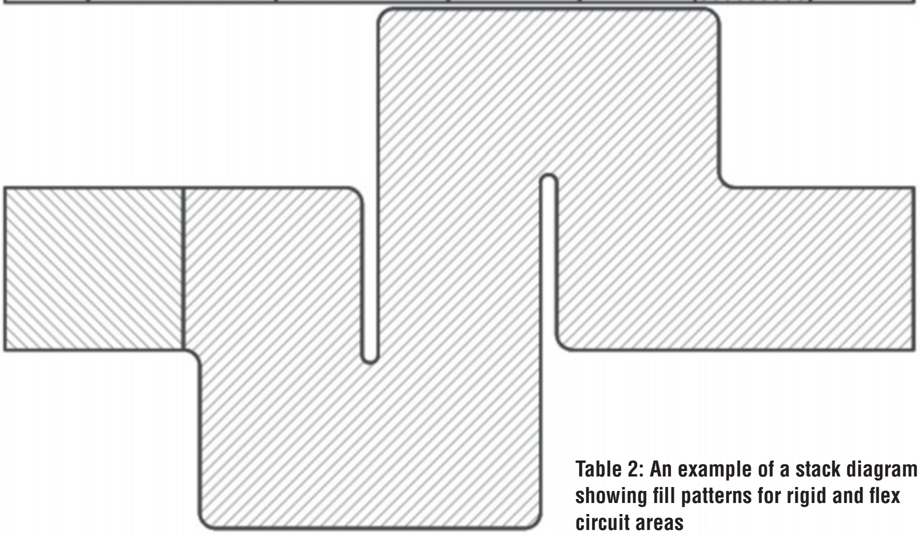


Table 2: An example of a stack diagram showing fill patterns for rigid and flex circuit areas

on flexible substrates. Where a change in direction is unavoidable, arced corner mode should be used to reduce mechanical stress during bending (see Figure 1).

Another important aspect to bear in mind is to avoid introducing possible weak spots in the tracks, such as the transition between significantly different track widths – particularly if they are used at a point where flexing occurs. Instead, a taper using a teardrop profile is preferable.

It may seem inadvisable but sometimes it is necessary to carry power and ground planes across flexible PCB spans; "inadvisable" because it would seem intuitive that the extra conductive material is more likely to fracture or suffer fatigue when flexed. Fortunately there is a solution for this, in the form of hexagonal polygons (see Figure 2).

Support for exposed copper (such as pads and vias) is also advised, as they are more likely to become detached through repeated flexing. While vias are inherently supported by the plate-through, pads and SMT pads may require support by ensuring the coverlay overlaps their edges (at least on two sides, in the case of square pads, see Figure 3).

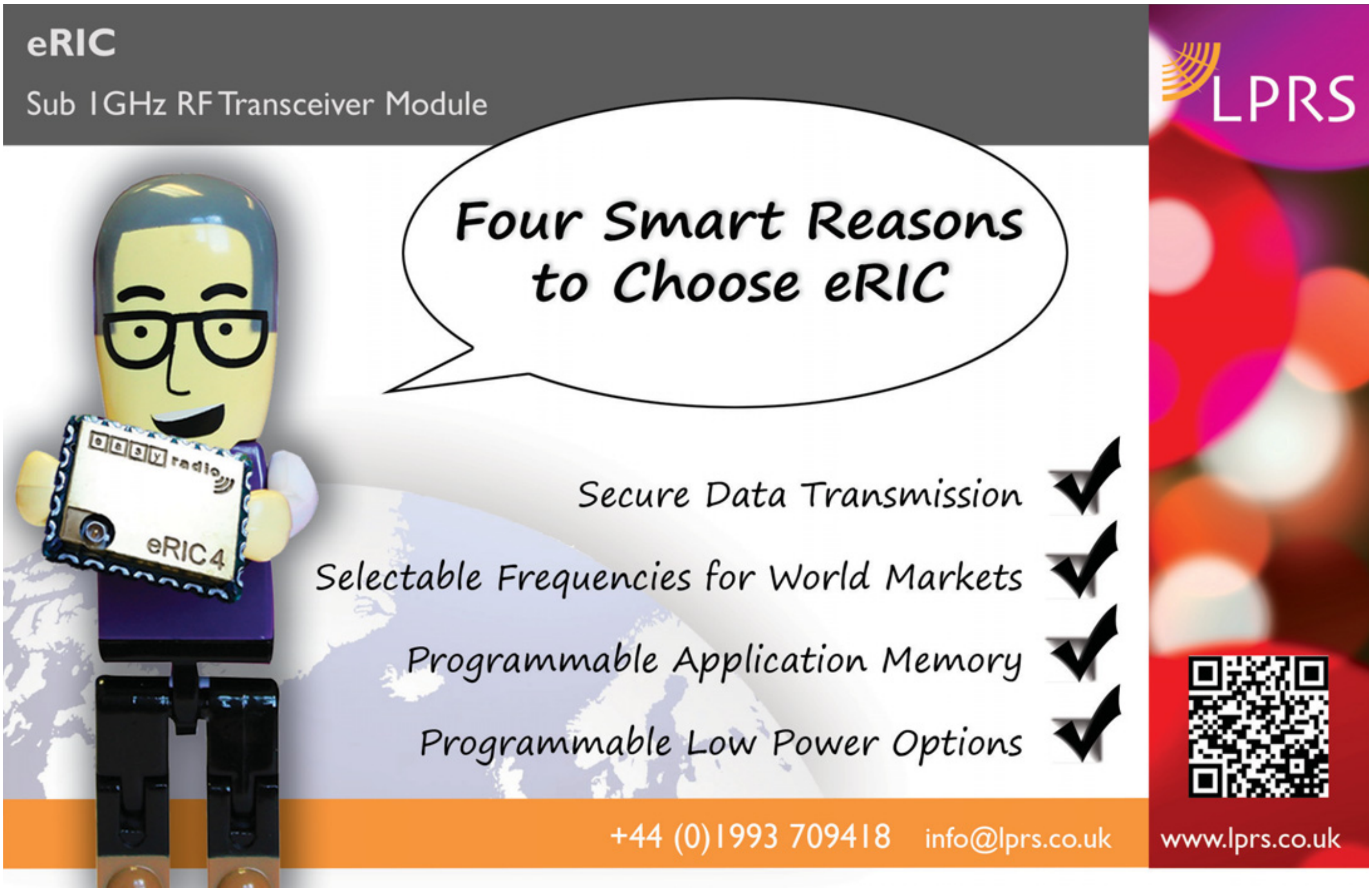
By understanding the requirements of the application it becomes simpler to choose the right rigid-flex PCB solution to meet those requirements, and many PCB design tools will now support the concept. For instance, as Table 1 shows, a rigid-flex PCB may require the definition of 10 layers, even when only two of them are used to carry conductors in both the rigid and flexible sections of the PCB.

Detailing this information in a design is only part of the process; it then needs to be conveyed to the PCB manufacturers, so a common set of design parameters can be agreed upon to which both parties adhere. In this case, the suggested solution is to adopt IPC-2223B, the Sectional Design Standard for Flexible PCBs. Furthermore, while many manufacturers still accept (and perhaps prefer) files in the Gerber format, it is now advised that its successor ODB++ be used; specifically ODB++ Version 7.0 (or later), which uses layer types that support the documentation of flexible circuits. Table 2 shows the subset of layer types defined in ODB++ V7.0 as used in GenFlex (a dedicated CAM solution for flex and rigid-flex PCB manufacturing).

Enabling Innovation

The use of flexible PCBs can enable innovation, as well as provide a more cost-effective and reliable solution to interconnect, while offering greater flexibility in the final assembly. For all these reasons, flexible and rigid-flex PCBs are now being used in a wider range of applications. Moving and movable parts are becoming more common in various devices, supported in part by developments in the design and manufacture of rigid-flex PCBs.

By appreciating the capabilities and limitations of this manufacturing process, it is now feasible for any OEM to employ rigid-flex PCB design, but selecting the right design partner at every stage is crucial to a successful outcome. ●



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MAKING WIRELESS SENSORS AS ACCESSIBLE AS WEB SERVERS

ROSS YU, PRODUCT MARKETING MANAGER, AND **THOMAS WATTEYNE**, SENIOR NETWORKING DESIGN ENGINEER, BOTH AT THE DUST NETWORKS PRODUCT GROUP, NOW PART OF LINEAR TECHNOLOGY, EXPLORE THE EFFORTS THAT GO INTO FULLY STANDARDIZED, INTEROPERABLE IP-BASED WIRELESS SENSOR NETWORKS WITH A LEVEL OF RELIABILITY NORMALLY ASSOCIATED WITH WIRES

The Internet of Things (IoT) revolution is upon us, and by the year 2020 there will be over 30 billion connected devices and systems in the world. With the world's population increasing and resources becoming more precious, this interconnection promises to supply real-world data to drive higher efficiencies and streamline business practices.

> "To further enable wide-scale deployment of sensors, IP standards efforts are underway, with the goal of making small wireless sensors as easy to access as web servers

With the wide acceptance of Internet Protocol (IP), it is becoming easier to process data and make meaningful use of information. Fortune 500 companies provide enterprise-level database solutions for data storage and software tools to streamline business processes, such as asset tracking, process control systems and building management systems (see Figure 1). Smart phones and tablets provide people with useful and actionable information, such as live parking information or real-time equipment-health monitoring to inform maintenance schedules. And while there are wireless sensors in place today, there is a hunger for more sensor data to measure and optimize processes that have not been previously measured.

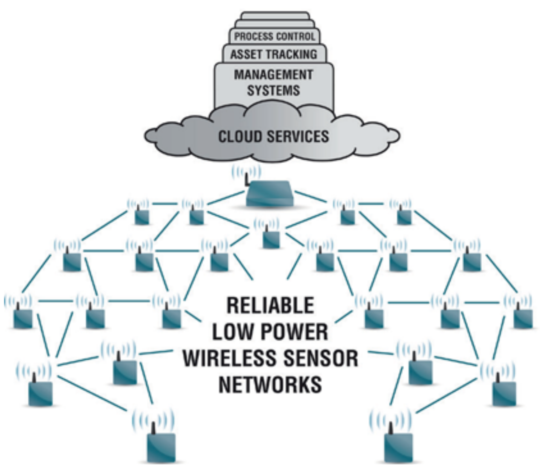


Figure 1: Making IP-enabled wireless sensors reliable and low power will enable wide-spread usage

To further enable wide-scale deployment of sensors, IP standards efforts are underway, with the goal of making small wireless sensors as easy to access as web servers. These efforts are the confluence of two driving forces: the proven low-power, highly reliable performance of time-synchronized mesh networks, and the ongoing IP standards efforts for seamless integration into the Internet. Together, these forces will drive relatively small, low-power sensors that communicate reliably and are IP-enabled.

Wireless Sensor Network Challenges

Since wireless is unreliable by nature, it is important to understand the sources of unreliability to be able to account for them in communication systems. In low-power wireless networks, the main sources of unreliability are external interference and multi-path fading. Interference occurs when an external signal, such as WiFi for example, temporarily prevents two radios from communicating. This requires them to re-transmit, so they end up consuming more power.

Multipath fading happens when a wireless signal bounces off objects in the vicinity of the transmitter and the various echoes destructively interfere at the receiver's antenna. This phenomenon is a function of the device's position, the frequency used and the surrounding environment. Because the surrounding environment of any wireless system changes over time, any single RF frequency channel can experience problems over the operational life of a wireless system.

However, multipath fading is frequency-dependent, so while one frequency may be experiencing a problem, there will be several other RF frequency channels that work well. Because of interference and multipath fading, the key to building a reliable wireless system is to employ channel and path diversity without sacrificing low-power operation. Such a system was pioneered by Dust Networks (now part of Linear Technology) with its time-synchronized, channel-hopping mesh networking.

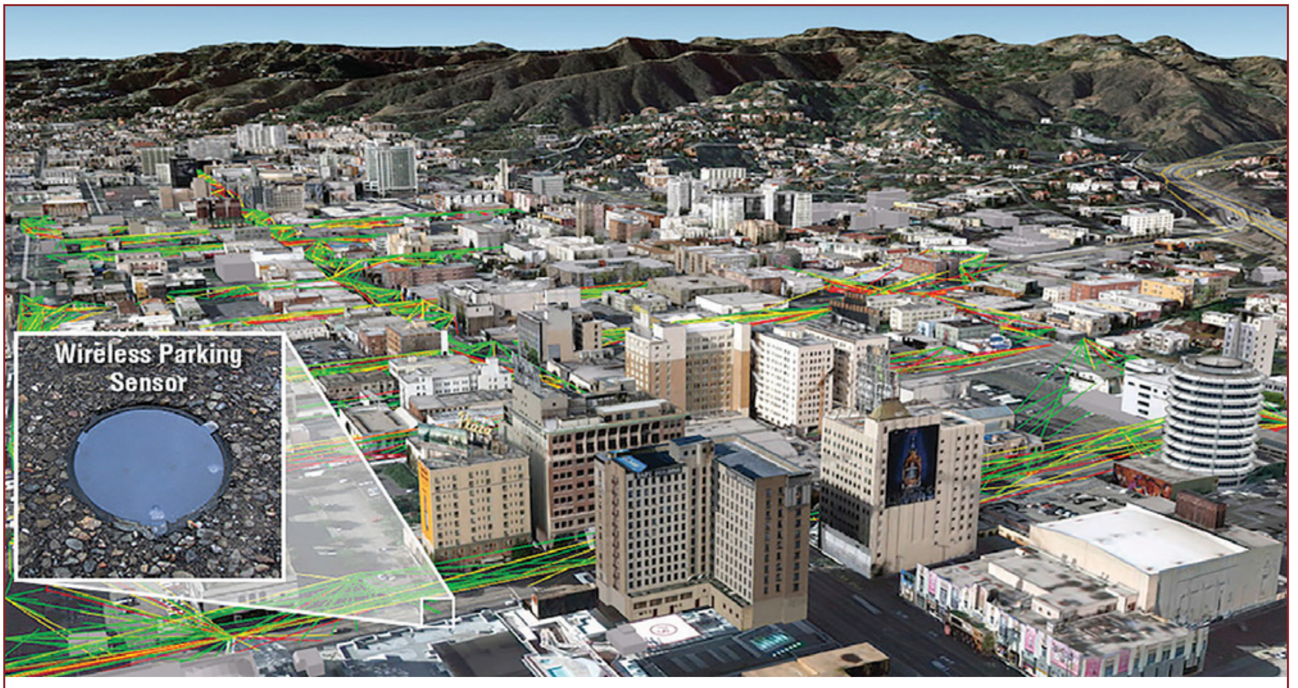


Figure 2: Streetline Networks has deployed time-synchronized channel-hopping networks to improve parking in such cities as Hollywood

Time-Synchronized Channel-Hopping Mesh Networks

In a time-synchronized channel-hopping mesh network, all wireless nodes across a multi-hop network are synchronized to within a few tens of microseconds and time is sliced into time slots. Communication is orchestrated by a schedule which indicates to each node what to do (transmit, receive, sleep) in each time slot. Because they are synchronized, each node switches on its radio only when communicating, thereby significantly reducing its duty cycle (< 1% is commonplace) and increasing battery life. Furthermore, since the schedule is flexible, the network is always available to the application, unlike other "sleepy" network architectures that completely shut down the network for extended periods of time.

Each packet sent between two nodes is done so on a frequency calculated using a pseudo-random hopping pattern. The resulting frequency diversity is an effective way of combating interference and multipath fading. Time-synchronized mesh networks enable a decade of battery life and > 99.999% end-to-end reliability.

Time-Synchronized Mesh Networking Successes

Time-synchronized channel-hopping mesh networks have already been widely deployed for several years. Dust Networks introduced its first SmartMesh system in 2004 and the industrial process industry was one of the earliest adopters.

Industrial applications have some of the harshest operating environments, yet have the most stringent demand for data integrity, which when assured, significantly improves efficiency, productivity and safety of industrial plants. Because traditional wired industrial sensors are expensive to install, only a small fraction of potential measurement points in a plant are traditionally instrumented. While this creates significant demand for wireless in industrial applications, traditional point-to-point wireless systems lack the required reliability and are difficult to install, limiting their use to small, isolated applications.

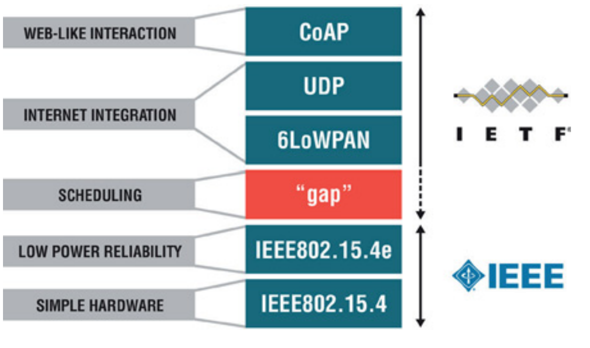


Figure 3: IP protocol stack for low-power, reliable wireless sensor networks

With the introduction of time-synchronized mesh networks, low-power wireless systems that deliver the reliability normally associated with wired systems became a reality. Its standardization into the industrial standard, IEC62591, also known as WirelessHART, established interoperability within the industrial process market. Most of the major industrial manufacturers, such as Emerson Process, Siemens, ABB, Endress & Hauser, Pepperl & Fuchs and Phoenix Contact are shipping

Figure 4: Small TSCH-based wireless nodes, such as the LTP5901-IPM from Linear Technology, deliver 5-10 years of battery life with data reliability > 99.999%

WirelessHART products. Today, SmartMesh networks have been widely accepted, with 30,000 networks deployed in over 120 countries around the world, to improve safety and efficiency in a variety of locations, ranging from steel mills and refineries to remote oil fields and offshore platforms to food and beverage plants.

Beyond the industrial process industry, SmartMesh systems have been successfully deployed in data centres and commercial buildings to optimize air-conditioning costs. Streetline Networks is a smart parking provider that monitors the real-time availability of urban parking spaces (see Figure 2). Vehicle detectors are installed beneath parking spaces, embedded in the roads. This brings challenges, since the antenna for the sensor device is located underground and then covered by a metal

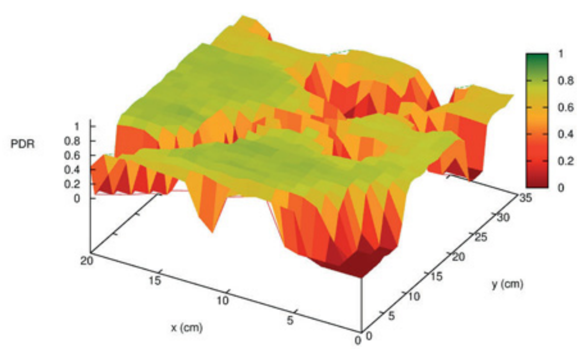


Figure 5: Multipath fading causes the quality of a link to vary dramatically, even when moving the receiver by only a couple of centimeters

vehicle when the space is occupied. Applications such as these, previously thought impossible or impractical, are being deployed with time synchronized channel-hopping mesh networks.

A Standards-Based World

Standards play an important role in networking technology, with end-users advocating development of standards-based solutions. Knowing that a technology has been developed and approved by a major standardization organization inspires confidence. And while WirelessHART/IEC62591 is the standard in industrial process, beyond that market Internet Protocol (IP) is the communications standard.

All devices connected to the Internet use IP to communicate with each another. Each device acquires an IP address, which unambiguously identifies it on the Internet. Data packets exchanges contain an IP header, a series of bytes that encode the addresses of the device that created the packet, and the destination device. Many other protocols are needed to form a protocol stack (TCP, HTTP, etc), but the IP protocol is the common denominator. Allowing low-power mesh networking devices to connect to the Internet using the IP protocol represented a major contribution toward development of IoT.

> “Most of the major industrial manufacturers, such as Emerson Process, Siemens, ABB, Endress & Hauser, Pepperl & Fuchs and Phoenix Contact are shipping WirelessHART products

Several standardization bodies have developed standards for IoT (see Figure 3). The challenge is to enable full Internet integration, while incorporating the proven principles of time-synchronized channel-hopping mesh networking. Within the Internet Engineering Task Force (IETF) – the standardization body behind most protocols used in today's Internet – the CoRE working group has defined the Constrained Application Protocol (CoAP) application layer protocol. CoAP runs on top of the UDP protocol and is easily translated to HTTP for web-like interaction with wireless sensor nodes. The 6LoWPAN working group has defined an IP adaptation layer that compresses an IP packet's large headers into small wireless frames or data packets, allowing sensor nodes to be individually addressable by IP addresses. While these upper layers enable web-like interaction and Internet integration, it is the protocol layers beneath them that determine the quality of the wireless sensor network communications.

The IEEE802.15.4 Standard Evolution

The standards developed by the IETF typically run on radio chips which comply with the IEEE802.15.4 standard. IEEE802.15.4 provides a healthy trade-off between data rate (250kbps), range (tens to hundreds of meters), power consumption (5mA to 20mA when transmitting or receiving) and packet size (up to 127 bytes). This trade-off makes IEEE802.15.4 a good fit for low-power mesh technology and has therefore become the de facto link technology for those networks.

In 2012, the IEEE published a new medium access standard to run on IEEE802.15.4-compliant radios, known as IEEE802.15.4e. Its Time Slotted Channel Hopping (TSCH) mode incorporates principles from Dust Networks's time-synchronized mesh protocol to enable precise time-slotted synchronization and RF channel hopping.

While IEEE802.15.4e defines the mechanism for two nodes to establish a synchronized data packet transfer, it does not define how each node is assigned a schedule. The communication schedule affords a TSCH network the flexibility to match the communication needs of the nodes in the network (Figure 4). For example, a network can be configured for small networks with low data rates and extremely low power consumption, as is common in remote environmental monitoring. The same network can be configured as a large network, optimized for faster data throughput. In addition, an automatically assigned yet flexible schedule enables a TSCH network to adapt to the surrounding environment. Specifically, network functions such as self-healing, routing optimization and load balancing are enabled by scheduling and are critical to delivering high performance over the life of a network. Solutions for building and assigning the TSCH schedule can be developed, but until standards are established, such solutions will not be interoperable over the air.

This is, however, changing with a new standardization activity inside the IETF, known as Deterministic IPv6 over IEEE802.15.4e Time Slotted Channel Hopping (6TSCH). Co-chaired by Linear Technology and Cisco Systems, this activity will define the missing communication protocols to allow the TSCH schedule to be managed by a scheduling entity.

By closing this remaining gap in the IP protocol stack, 6TSCH will enable fully standardized, interoperable IP-based wireless sensor networks that deliver the level of reliability normally associated with wires. Web developers will be able to request real-time sensor data by making web requests to the IP address of a sensor, and the underlying wireless sensor network will support such communications with data reliability of over 99.999% .

By making sensors as easily accessed as web servers, wireless sensor networks will feed real-world information to the Internet of Things. ●

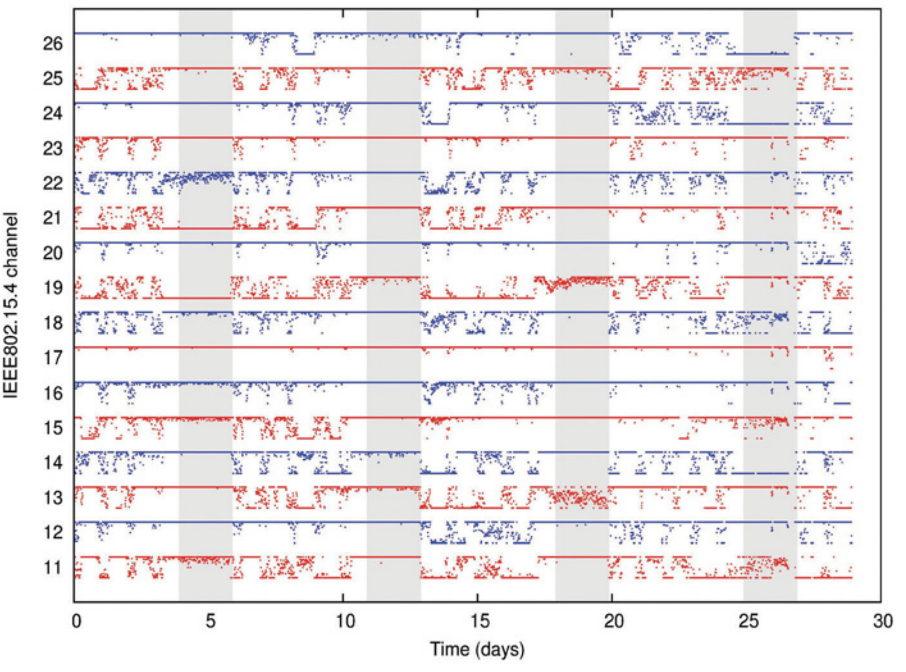


Figure 6: The packet delivery ratio of a wireless link evolves over time

THE EFFECT OF MULTIPATH FADING ON WIRELESS COMMUNICATIONS

Because of interference and multipath fading, the key to building a reliable wireless system is to exploit channel and path diversity. Multipath fading depends on the position and nature of every object in the environment, and is unpredictable in any practical setup. One good property is that the topography depicted in Figure 5 changes with the frequency: if a packet is not received because of multipath fading, retransmitting on a different frequency has a high probability of success.

Because objects in the environment are not static, i.e. cars drive by and doors are opened and closed, the effect of multipath changes over time. Figure 6 shows the packet delivery ratio on a single wireless path between two industrial sensors over the course of 26 days, and for each of the 16 channels used by the system. There are weekly cycles where workdays and weekends are clearly visible. At any given time, some channels are good (high delivery), others bad, and still others highly varying. Channel 17, while generally good, has at least one period of zero delivery. Each path in the network shows qualitatively similar behaviour, but unique channel performance, and there is never any one channel that is viable everywhere in the network.

SMART HOME SCHEME USING A SMARTPHONE AS A REMOTE CONTROL

BY **SHAOPENG GUAN, DAIPING JIA** AND **WENYAN SUN** FROM THE SHANDONG INSTITUTE OF BUSINESS AND TECHNOLOGY IN CHINA

A smart home management scheme is an integrated system incorporating home security, network service and home automation, and other home-related systems. It combines computer, communication and control (3C) technologies to offer a multitude of intelligent features. Its basic objective is to connect diverse household appliances, home security devices, and home computing and entertainment systems through wired and/or wireless means for centralized management and control.

Core Components

The home gateway is the core component of the smart home management system and it manages the conversion of various communication protocols and information sharing between different nodes, and the data exchange with any external communication networks. It also acts as a firewall, checking the legality of instructions transmitted through the network.

Here we present the smart home scheme shown in Figure 1, with home appliances connected using the ZigBee wireless network. All facilities are linked to external Internet through the home gateway. Based on this scheme, we also designed a remote control system based on the smartphone.

At present, the most popular short-range wireless communication technologies are infrared (IrDA), Bluetooth, WiFi (IEEE802.11a, b, g, n) and ZigBee; see their working frequency ranges, power and data speeds compared in Table 1. They all have different advantages and disadvantages.

ZigBee Connectivity

ZigBee is a short-range, low-power and low-cost wireless communication technology, with physical and MAC layers in accordance with the IEEE 802.15.4 standard. The ZigBee technology focuses on low-speed transmission applications between 10kbps and 250kbps and is mainly used for automatic control and short-distance remote control applications, therefore we have chosen it to be our connecting mode.

The ZigBee protocol is fairly simple and compact, see Figure 2. The functions and roles of its layers are as follows:

- **Physical layer.** This layer defines the interface between the physical radio channel and the MAC layer, and it provides the data and management services of the physical layer. The functions of the physical layer include activation of ZigBee, energy detection of the current channel, service quality of the receiving link, selection of the channel frequency and data transmission and reception.
- **Medium Access Control (MAC) layer.** Functions of this layer include generation and synchronization of the beacon frame, association and disassociation of devices, media access through the Collision Avoidance Carrier Sense Multiple Access (CSMA/CD) technology and making a reliable MAC communication link. Because the MAC layer adopts the CSMA/CA technology, all nodes share the same wireless channel.
- **Network layer.** This layer is the core of the ZigBee protocol. Its main functions include the joining or leaving of nodes, routing queries, data transmissions and so on.
- **Application layer**. This layer provides some necessary functions and service interfaces to the network layer. Another important feature of this layer is that users can define their own application objects.

ZigBee provides the network platform for internal control of the smart home. However, limited by the scope of the ZigBee network, the user won't know the state of the home appliance nor manage to control it once outside its domain. That's why the home network should be connected by an external network. As the smartphone is so widely used, we recommend a smartphone-based remote control for the smart home scheme. The overall system architecture of the scheme is shown in Figure 3.

Technology	Frequency (GHz)	Speed (Mpbs)	Power (mW)	Node number	Application
IrDA	3.5×103	1.521/4/16	10	2	Close remote
Bluetooth	2.4	1/2/3	100	7	Personal network
802.11g	2.4	54	100	255	WLAN
ZigBee	ISM band	0.02/0.04/0.25	3	65535	Home network, WSN

Table 1: Comparisons of four wireless communication technologies

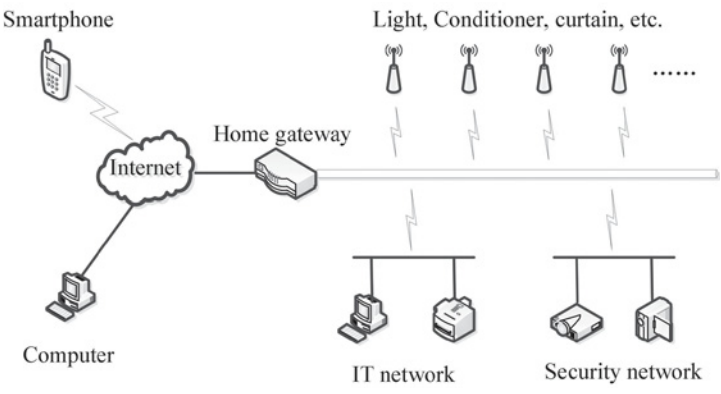


Figure 1: Topology of the smart home

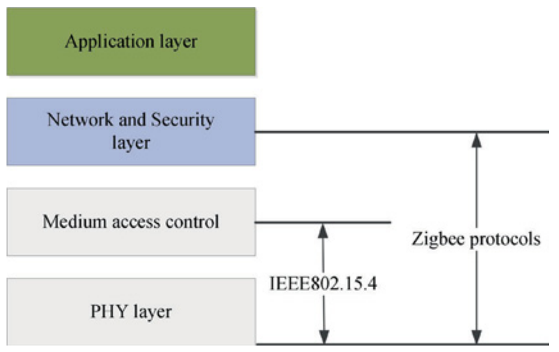


Figure 2: The ZigBee protocol

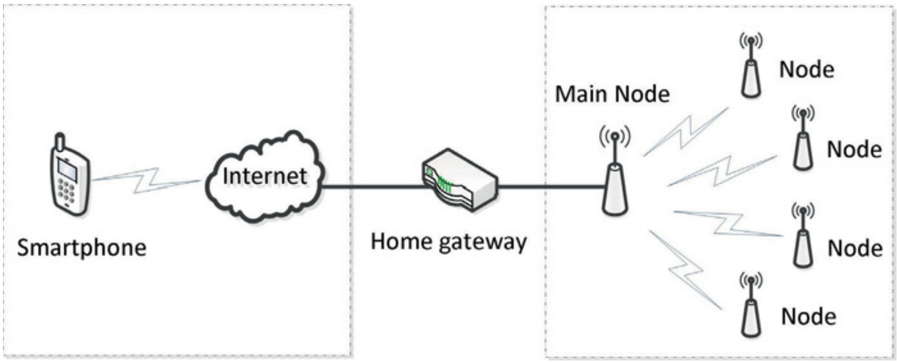


Figure 3: System architecture of the smartphone-based remote control for a smart home scheme

Home Appliance Nodes

The home appliance node consists of three parts: the RF module, the arithmetic and control module, and the sensing and execution module. The RF module is the communication interface of the node; it takes charge of the connection with the other nodes and the transmitting and receiving of wireless data and instructions.

The sensing and execution module is responsible for detecting any illegal invasion, unexpected disasters, but also the data acquisition and control of the home appliances. This detailed control process is performed by the arithmetic and control module.

Instructions are sent by the smartphone; we've developed a Java-based control system for an Android smartphone. The system provides a friendly operation interface and consists of four functional modules as shown in Figure 4. A temperature control module is used to enquire the home ambient temperature and graphically present the results to the user, for adjustments if necessary.

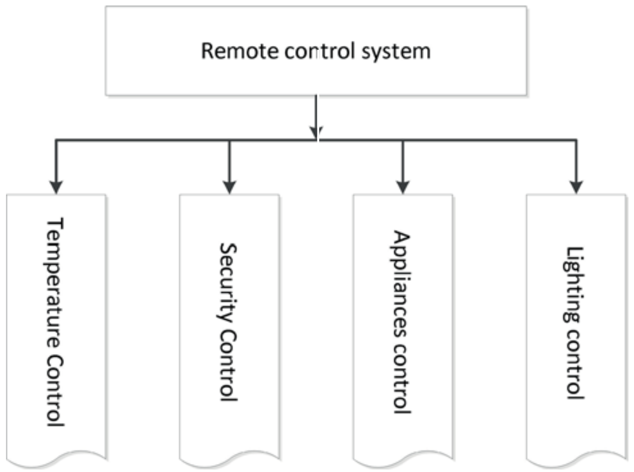


Figure 4: Functional modules of the remote control system

The security control module takes charge of monitoring the home via the Internet, and checking and controlling the status of the alarm, which it can activate if the home is in danger. The appliance control and lighting modules are responsible for checking and controlling the status of the home appliances and lighting respectively.

We have adopted the CC2430 ZigBee modules as home nodes and have conducted experiments to verify our system. ●

ELECTRONIC AID SYSTEM FOR THE VISUALLY IMPAIRED

BY A TEAM* FROM THE AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY AND THE JAGIELLONIAN UNIVERSITY IN KRAKOW, POLAND (SEE BOX)

Electronic systems and devices are part of almost every aspect of our life, so it is not surprising that a vast spectrum of scientists and engineers work together to develop systems to extend a person's life and make it easier. This includes not only high-priced systems for hospitals and rehabilitation centres, but also electronic aid and monitoring systems for everyday use, such as hearing aids, pacemakers, insulin pumps, glucometers and others.

One type of device focuses on helping disabled people live a normal everyday life. In many developed countries, electronic aid device research is supported and funded by governmental organizations. Additionally, there are many rehabilitation programs that financially support disabled people in purchasing electronic aid devices.

The MOBIAN Project

There are nearly 300 million visually impaired people worldwide, about 90% live in the developing countries. Although there have been cases of successful vision restoration through surgery, for the time being blind people have to rely on white canes, and that's why so many research projects all over the world focus on designing electronic aids for the visually impaired.

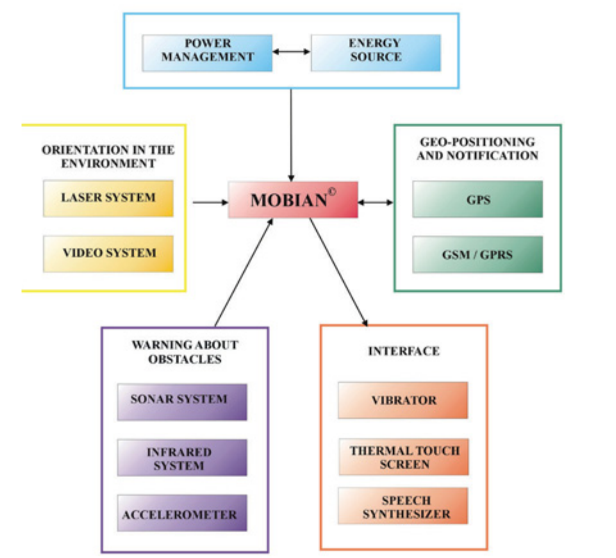


Figure 1: Block diagram of the MOBIAN device

AGH University of Science and Technology engineers, together with students and teachers from the Special Educational Centre for Blind and Visual Impaired People in Krakow, Poland, are working on the MOBIAN project. Its general goal is to design and implement a mobile safety system to help blind users avoid dangerous objects and situations.

Many visually-impaired people suffer daily from accidents, most of which can be avoided if only more information from the surroundings was relayed to them in some way. Even small holes and bumps on the pavement can pose major problems.

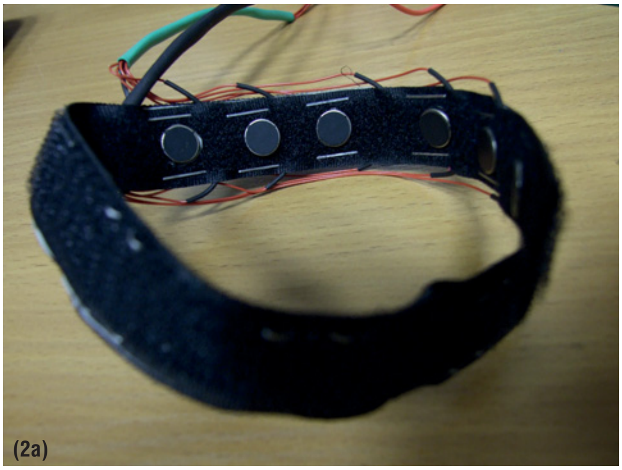
> "Designing electronic aids for the visually impaired is more challenging than some regular consumer devices

People with unimpaired vision gather most of their environmental information visually, the reason most consumer devices have displays. Even though visually-impaired people have sensitive hearing and a sense of touch, it is not enough to compensate for their lack of vision. So the MOBIAN system uses various sensors to gather information from the nearest surroundings. A camera module, in conjunction with a laser range finder, is useful for detecting objects, as well as faces, signs, shop ads (text/symbols) and so on.

To avoid walking into hazards, the MOBIAN system is equipped with a low-power infrared range finder that's directed toward the ground. Also, an additional multichannel ultrasonic range finder was added to detect large obstacles that are hard to recognize with a laser range finder, such as glass doors.

Since the system ought to detect very small potholes, even ones that are only 5cm deep, some sort of a stabilization system was needed. When a blind person walks, the system's sensors are constantly in motion in all three axes. Thanks to sensor fusion of an accelerometer, gyroscope and adaptive filtering, the system is able to correct the readouts of the ranges, stabilize the data and reliably detect small potholes. Additionally, GPS-based localization was implemented to inform users of points-of-information (POI) specific to blind people, such as an audible zebra-crossing.

The MOBIAN system is also equipped with a GSM/GPRS modem, so that a user in distress or lost can call someone, with data being sent through the GPRS communications channel, offering the system's position and a video feed. Since GPS localization is mostly available



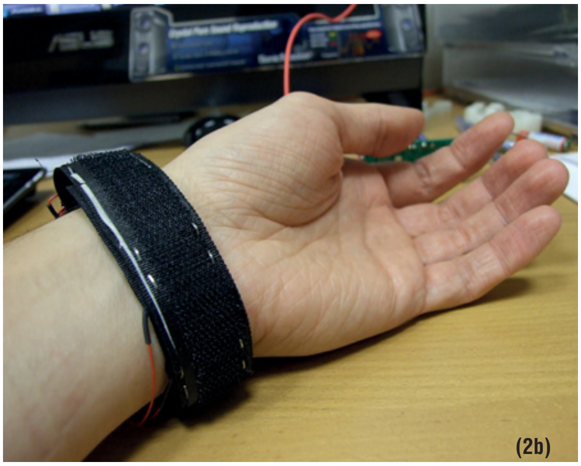


Figure 2: Figure 2a and b: Six-point vibrating bracelet – a novel interface for the visually impaired

outdoors, when a GPS fix cannot be established and yet the localization functionality is needed, GSM-based localization is turned on. With a known correlation between GSM base-stations and their geo positioning – which is stored on the server – MCUs can gather data from the GSM modem and establish which base-stations are within range. With this data and signal strength approximation, the blind user's location can be established via triangulation. This will lead to large localization errors – in cities tens or hundreds of meters, and in the countryside even more; but when a GPS signal is not available and the user is in distress or possibly unconscious, narrowing the search area is extremely important.

Interfaces

The natural way to pass information from system to user is with voice commands. However, blind people strongly depend on their hearing sense when they are outside. They navigate with the help of what they hear; sounds are emitted by objects or echoes of their white cane on the pavement. Therefore, we developed a different method of signalling – the multipoint vibrating bracelet. For this to function properly, an electronic driver was designed to control each vibrating channel with PWM.

Tests confirmed that the optimal number of vibrating points is six, as initially those testing the system found it hard to recognize one vibrating point from another when there were a larger number.

To accomplish diverse communication and obstacle differentiation, we had to implement a vibrating scheme. By incorporating PWM vibrating strength, frequency and also different groups of points vibrating at the same time, various commands can be sent to the user, to be informed of the types of obstacles detected by the system's various sensors, the distance to them (in meters or steps), the nearest POI, and so on.

During the tests it was also determined that the vibration bracelet could be used separately from the safety device for other applications: a doorbell indicator for deaf people for example, as an indicator cooperating with smartphones, medicine timer and others.

Another innovative interface that has been used in the MOBIAN project is the Thermal Touchscreen. Designed almost a decade ago, this matrix consists of very small Peltier modules, that – when correctly controlled – can display thermal images and Braille text. Successful tests at the Special Educational Centre for Blind and Visual Impaired People in Krakow showed that both text and simple symbols can be recognized in matter of seconds.

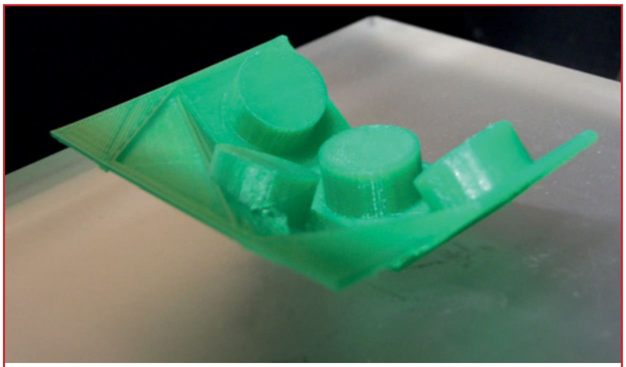


Figure 3: Part of device's plastic cover for the Mobian device – a prototype created with a 3D printer

Using both vibrating and thermal indicators the system can communicate and pass important information and warnings to the user without compromising their sound perception.

The Development Process

Designing electronic aids for the visually impaired is more challenging than some regular consumer devices. Usually, many mainstream-accepted solutions are not suitable for these aids. For instance, one cannot use graphical displays or simple LEDs for information in some devices intended for blind people. Engineers have to search for different, innovative solutions to meet these users' specific needs and every functionality and possible solution has to be discussed at length.

Another important issue is the power consumption of the device, whose battery should be fully usable for at least a full day, since essentially it is a mobile device. The system power management was taken into consideration. Some parts of the system should be turned on only when the user needs them, whilst others which are responsible for the user's safety should be operational at all times.

While working on the embedded software, an energy debugging technique was used to detect unnecessary current consumption and a way to minimize it. Also, for convenience the battery can be charged simply via any USB port.

From the first device test, we have noticed that blind users like to get familiar with the whole device by touching it and surprisingly they did not like the casing, which was a standard box-shaped ABS. We identified an acceptable, customized casing with the help of a 3D printer; creating a variety of casing prototypes in a short time, relatively cheaply.

Device Tests

Apart from standard mechanical, electrical and functional tests of the device, such as its maximum- and minimum-distance sensor range, stabilization reliability, current consumption and so on, other usefulness tests of the device were conducted at all stages of development.

Many tests were performed, indoor and out: in rooms, corridors, stairs, etc. Various obstacles were placed in the testing path, from boxes and chairs, to road signs, furniture, bumps and road holes, as well as moving people. In most cases all the objects were detected and the users were informed of their distance through the vibrating bracelet. In the beginning only one vibration point was used, but later all six points were implemented. Testers quickly accepted this multipoint vibrating bracelet as a new, intuitive interface.

Tests showed that the MOBIAN device can be used as a mobility safety system, where objects tagged as dangerous for blind people can be detected and sufficient information about them obtained via the available interfaces to avoid them. ●

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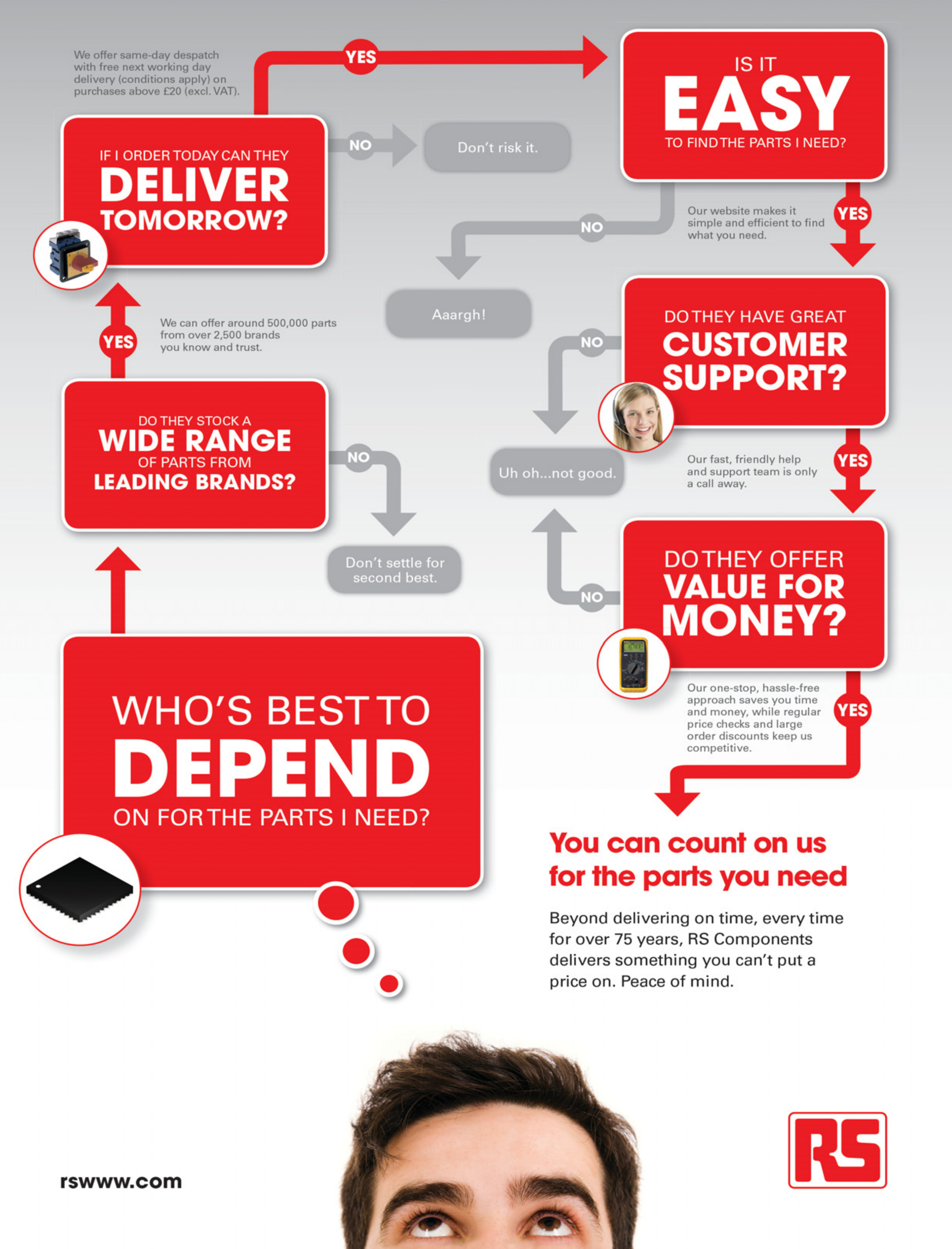

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Don't settle for second best.
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IF I ORDER TODAY CAN THEY DELIVER TOMORROW?
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How to Add and Test the LCD Display for An Arduino Clock Project

BY **BROCK CRAFT**

Once you've programmed and tested the beating heart of an Arduino clock, you need a way to display the time without using the serial monitor. This is where the LCD display comes in. It is fairly inexpensive and uses the very common Hitachi HD44780 driver. These LCD modules are easily recognized because they have 16 pins in a single row and a parallel interface.

Because of this, the Arduino uses several digital pins to make the display work. This process is somewhat complicated but, luckily, there is an Arduino library for it already that makes it very easy to send text to the screen without worrying about the low-level commands that would otherwise be needed.

A 4-bit mode should be used to display text, which needs only seven Arduino digital pins to control the display. Power for the LCD and the backlight is also needed. Controlling the contrast of the display is by using the potentiometer.

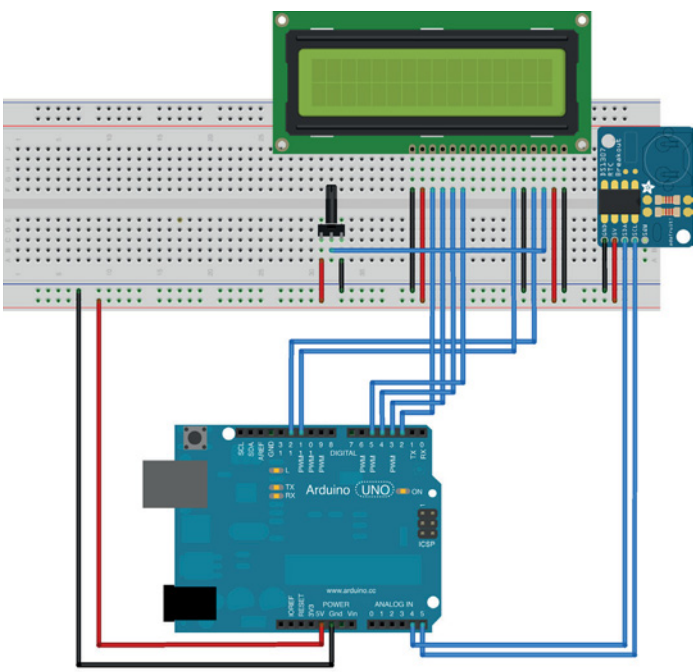


Figure 1: Arduino board connections for this project

Connections

Here's how to make the connections:

- Add the LCD display and potentiometer to the breadboard.
- Connect the power and ground pins on the LCD, which are Pins 15 and 16, respectively.
- Connect the ground and power for the LCD's backlight, which are Pins 1 and 2, respectively.
- Connect the control pins for the LCD to the digital pins on Arduino.
- Then connect the potentiometer, which controls the display's contrast.

The centre pin of the potentiometer connects to Pin 14 of the LCD display and the other two pins of the potentiometer are connected to power and ground.

Now that you have connected the LCD, it's time to make it do something interesting. First upload code to make sure the LCD is working properly (see the book for further details). You can copy the code for the clock all at once, but consider adding it in sections, as described here. That makes it easy to troubleshoot problems and test the clock in stages, as you build it.

The following code should be added into the integrated development environment (IDE), or downloaded from the companion website and uploaded to Arduino:

```
// Chapter 7: Arduino Alarm Clock
// An alarm clock that uses the Adafruit Industries DS1307
RTC Breakout board
// and a 16x2 Parallel LCD Display
#include <Wire.h> // I2C Wire Library for
communicating with the DS1307 RTC
#include “RTClib.h” // Date and time functions for the
DS1307 RTC connected
#include <LiquidCrystal.h> // Display functions for the
LCD Display
RTC_DS1307 rtc; // Create a realtime clock called rtc
LiquidCrystal lcd(12, 11, 5, 4, 3, 2); // Create an LCD called
lcd
void setup () {
 Wire.begin(); // Enables the communication for the LCD
 rtc.begin(); // Enables the RTC
 lcd.begin(16, 2); // Enables the LCD
```

```
 lcd.print(" It's Alive!"); // Print a message, centered, to the
LCD to confirm it's working
 delay(500); // Wait a moment so we can read it
 lcd.clear(); // Clear the LCD
}
void loop(){
}
```

When this code is uploaded, the message "It's Alive!" displays on the LCD for a half-a-second. If you don't see anything, or if the display shows garbled characters, something has been wrongly connected, which should be corrected back at the wiring table.

The first three lines of this code include libraries used for the clock, the first of which contains the I2C library that enables communication with the RTC module. I2C is a communication link between integrated circuits, in this case Arduino and the Dallas DS1307 chip. It's also useful for communicating with many other peripherals, such as GPS modules. The useful thing about I2C is that it requires only two pins, plus power and ground. This library makes communication pretty easy with most I2C devices.

16x2 LCD Display Pin	Arduino Digital Pin
1 (to GND rail on breadboard)	
2 (to +5V rail on breadboard)	
3	2
4	3
5	4
6	5
7 (no connection)	
8 (no connection)	
9 (no connection)	
10 (no connection)	
11	11
12 (to GND rail on breadboard)	
13	12
14 (to potentiometer middle pin)	
15 (to +5V rail on breadboard)	
16 (to GND rail on breadboard)	

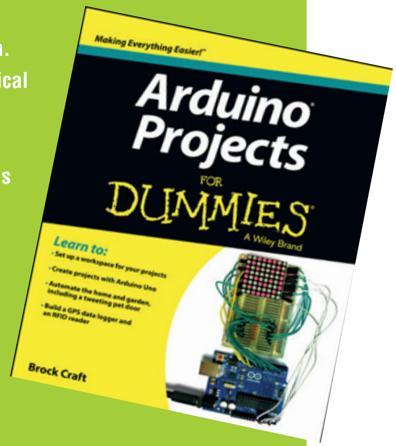
Table 1: Arduino board connections

WIN THE 'ARDUINO PROJECTS FOR DUMMIES' BOOK

Brock Craft is a Lecturer in the Department of Computing at Goldsmiths, University of London. He drew extensively on his practical experience with Arduino to write 'Arduino Projects For Dummies'. We have a couple of copies of this book to give away.

To enter please supply your name, address and email to the Editor at svetlanaj@sjpbusinessmedia.com

The winner will be drawn at random and announced at the end of the series.



The next library is the RTCLib. It's a version of a library written by JeeLab and modified by Adafruit Industries for communicating with the RTC module. It's used for getting the time from the RTC module using the I2C library to negotiate that communication.

The last library is the LCD display library, which handles parallel communication with the display. Unlike the RTC library which is added manually, it's included as a standard library in the Arduino software distribution.

Communication

After including the libraries, the code creates two objects: a clock object called rtc and a LiquidCrystal object called lcd. This object has parameters that determine which digital pins the Arduino uses to communicate with the LCD.

After creating those objects, the setup() function gets things going. The I2C, RTCLib and the lcd all have to be enabled, which is done by the begin() function. The lcd.begin() function takes two parameters, the number of columns and the number of rows, which on the display are 16 and 2. After this has been set, messages may be written to the screen simply by using the lcd.print() function:

```
lcd.print(" It's Alive!")
```

There are two spaces at the beginning of this text, which centres the 11-character message within the 16-character space on the top line. You normally control the position of text with the setCursor() function, but it's not needed here – one less instruction to put into setup().

After a brief delay, so you can see that it has been printed to the screen, the lcd.clear() function wipes all the text, ready to go for the main loop(). ●

More on this project, as well as other Arduino-related projects, can be found in the book 'Arduino Projects For Dummies' by Brock Craft.

Current Mirrors

MAURIZIO DI PAOLO EMILIO, PHD IN PHYSICS AND A TELECOMMUNICATIONS ENGINEER, PRESENTS THIS SERIES OF ARTICLES ON THE FUNDAMENTALS OF MICROELECTRONICS

Current mirrors replicate the input current of a current sink or current source in an output current, which may be identical or a scaled version. They are used to provide bias currents and active loads to circuits. Apart from some special circumstances, a current mirror (Figures 1 and 2) is one of the basic building-blocks of the operational amplifier; it is a circuit designed to keep the output current constant, regardless of loading. This type of topology may, therefore, be used to create current generators.

The main requirements a current mirror must meet are:

- Output current independent of the output voltage.
- Wide range of output voltages at which the mirror works properly.
- Low input voltage.

The range of voltages within which the mirror works is called the 'compliance range', and the voltage marking the behaviour in the active/linear region is called the 'compliance voltage'. There are also a number of secondary performance issues with mirrors, such as temperature stability.

An Ideal Current Mirror

A current mirror is usually and simply approximated by an ideal current source. However, an ideal current source is unrealistic for several reasons:

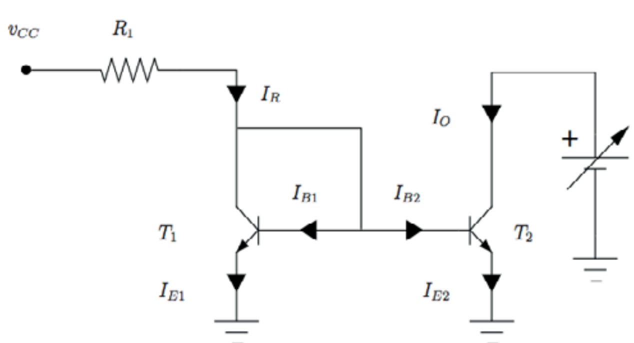


Figure 1: Current mirror with a BJT

- It has an infinite AC impedance, whereas a practical mirror has a finite impedance;
- It provides the same current regardless of voltage, that is, there are no compliance range requirements;
- It has no frequency limitations, whilst a real mirror has limitations due to the parasitic capacitances of the transistors;
- The ideal source has no sensitivity to real-world effects like noise, power-supply voltage variations and component tolerances.

The main part of the current mirror is a transistor – a bipolar junction transistor (BJT) or a MOSFET. Transistors in a current mirror must all be maintained at the same temperature for precise operation.

There are different types of current mirrors:

- Simple current mirror (BJT and MOSFET);
- Base-current-corrected simple current mirror;
- Widlar current source;
- Wilson current mirror (BJT and MOSFET);
- Cascoded current mirror (BJT and MOSFET).

All these circuits have a compliance voltage that is the minimum output voltage required to maintain correct circuit operation: the BJT should be in the active/linear region and the MOSFET should be in the active/saturation region.

Current Mirror BJT/MOS

Current mirror circuits are usually designed with a BJT, such as an NPN transistor, where a positively doped (P-doped) semiconductor base is sandwiched between two negatively doped (N-doped) layers of silicon. These transistors are specifically designed to amplify or switch current flow.

In some current mirror design specifications, the NPN transistor works as an inverting current amplifier, which reverses the current direction, or it can regulate a varying pulse current through amplification to create output mirror properties.

One of the reasons BJTs are used in current mirrors is that the base-emitter (or PN part) of the transistor functions reliably like a diode. Diodes regulate both the amount of

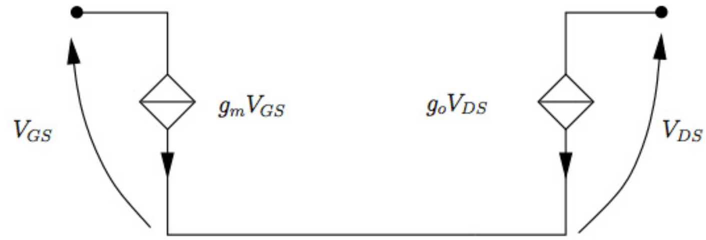


Figure 2: Current mirror with a a MOSFET (model)

current that passes and the forward voltage drop for that current.

The basic current mirror can also be implemented using MOSFETs (Figure 3). In Figure 3, M1 is operating in the saturation or active mode, and so is M2. In this setup, the output current I_{OUT} is directly related to I_{REF}.

The drain current of a MOSFET ID is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by a relationship derived from the functionality of the MOSFET. In the case of transistor M1, $I_D = I_{REF}$.

Reference current I_{REF} is a known current and can be provided by a resistor or by a “threshold-referenced” or “self-biased” current source to ensure that it is constant and independent of voltage supply variations. ●

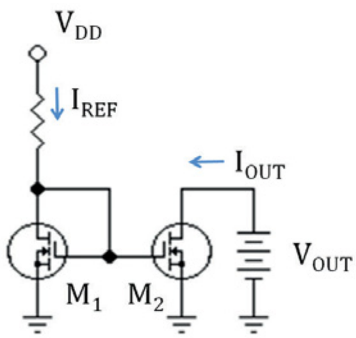


Figure 3: Current mirror with a MOSFET

IAN DARNEY PRESENTS A SERIES OF ARTICLES ON CIRCUIT MODELLING FOR ELECTROMAGNETIC COMPATIBILITY

Transients

This is the fifth article in the series *'Circuit Modelling for Electromagnetic Compatibility'*. The first three described a systematic method of deriving circuit models from the relationships of Electromagnetic Theory. The fourth showed how bench testing with an oscilloscope and a signal generator can be used to define a representative model of the signal link-under-review. This article shows how time-step analysis can be used to simulate transient performance.

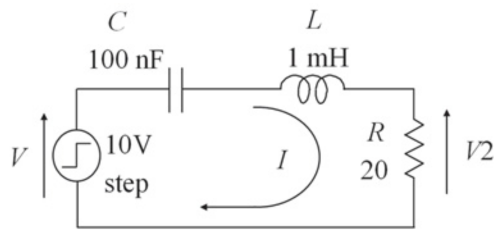


Figure 1: Series RLC circuit

```
L := 1·10^-3    C := 100·10^-9
V := 10    R := 20    dt := 10^-6
N := 101    i := 2..N
t_i := (i − 1)·dt·10^6
V2 := | I ← 0
      | Q ← 0
      | for i ∈ 2..N
      |   | dI ← (dt/L)·(V − R·I − Q/C)
      |   | I ← I + dI
      |   | Q ← Q + I·dt
      |   | V2_i ← I·R
      | V2
```

Figure 2: Mathcad worksheet

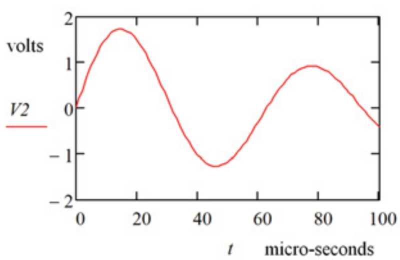


Figure 3: Waveform of voltage V2 of Figure 1

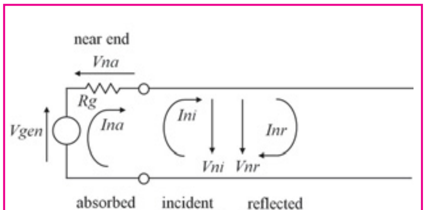


Figure 4: Voltages and currents at the near end of the line

Basics

Time-step analysis is similar to the iterative method used in mathematics to solve non-linear equations. The essential difference is that each calculation defines the condition of the system at a later time. If the time steps are sufficiently small, then the variation in the amplitude of the current can be assumed to be linear. Two factors are involved in each set of calculations:

- The state of the system immediately prior to the calculation.
- Incremental changes to the applied voltages.

The basic equations are the simplest possible. The voltages across an inductor, resistor and capacitor are:

$$V = L\cdot\frac{dI}{dt} \tag{1}$$

$$V = R\cdot I \tag{2}$$

$$V = \frac{Q}{C} \tag{3}$$

$$Q = \int I\cdot dt \tag{4}$$

where Q is the stored charge on the capacitor.

Series LCR Circuit

For the circuit shown in Figure 1, the total voltage at any time, t, is the sum of the instantaneous voltages across each component. This gives the loop equation:

$$V = L\cdot\frac{dI}{dt} + R\cdot I + \frac{Q}{C} \tag{5}$$

If the time increment dt is finite, this equation can be re-arranged as:

$$dI = \frac{dt}{L}\cdot\left[V - R\cdot I - \frac{Q}{C}\right] \tag{6}$$

At the end of time dt, the current increases to:

$$I = I + dI \tag{7}$$

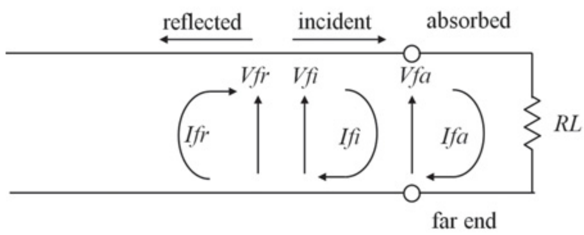


Figure 5: Voltages and currents at the far end of the line

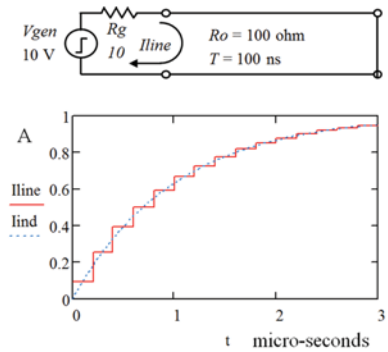


Figure 6: Response of short-circuited line

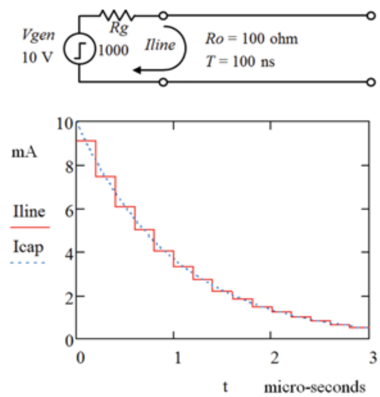


Figure 7: Response of open-circuited line

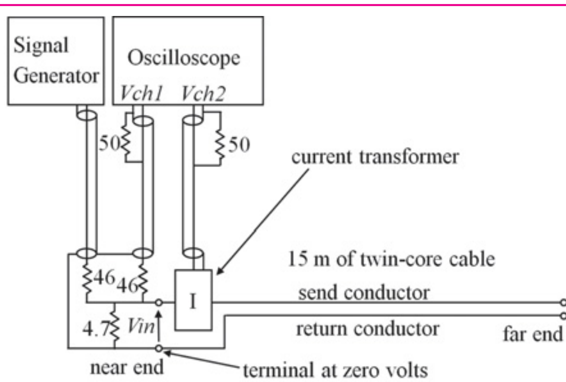


Figure 8: Setup used to measure transient characteristics of the line

and the charge Q becomes:

$$Q = Q + I \cdot dt \qquad (8)$$

This set of equations can be used to write an iterative program to calculate the variation of voltage $V2$ with time, as illustrated by the Mathcad worksheet of Figure 2. The response is shown in Figure 3.

Delay-Line Model

Transmission-line theory invokes the concept of electromagnetic waves travelling forwards and backwards along a path, bounded by a pair of parallel conductors. For this to happen, the current and voltage transients must travel at the same velocity as the waves they create. At each termination, some of the incident energy is absorbed and some reflected. To analyse this action, it is necessary to introduce the concept of partial voltages and currents.

At the near end, at any instant:

$$Vni + Vnr + Vgen = Vna \qquad (9)$$

$$Ini + Inr = Ina \qquad (10)$$

$$Vni = Ro \cdot Ini \qquad (11)$$

$$Vnr = -Ro \cdot Inr \qquad (12)$$

$$Vna = Rg \cdot Ina \qquad (13)$$

where Ro is the surge resistance of the line.

Subtracting (12) from (11) yields:

$$Vni - Vnr = Ro \cdot (Ini + Inr) = Ro \cdot Ina \qquad (14)$$

Using (13) to substitute for Vna in (9):

$$Vni + Vnr = Rg \cdot Ina - Vgen \qquad (15)$$

Adding (14) and (15) gives:

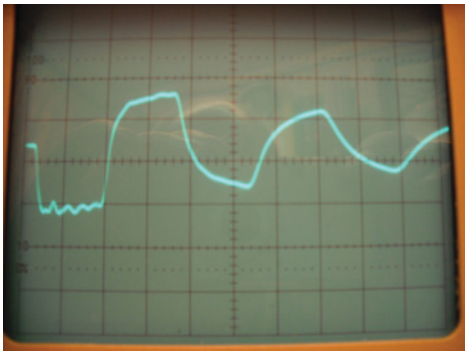


Figure 9: Waveform monitored by channel 2 of the scope (100ns/div, 10mV/div)

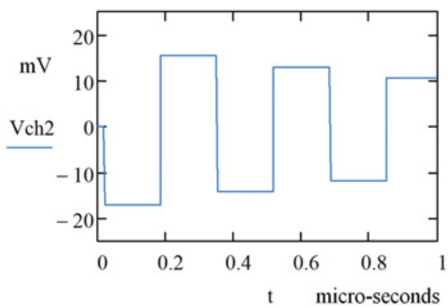


Figure 10: Expected waveform at channel 2

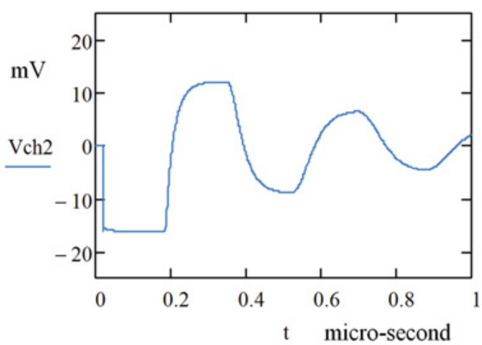


Figure 11: Response of modified model

$$2 \cdot Vni = (Rg + Ro) \cdot Ina - Vgen \qquad (16)$$

Re-arranging (16) and using (11) to substitute for *Vni*:

$$Ina = \frac{2 \cdot Ro \cdot Ini + Vgen}{Ro + Rg} \qquad (17)$$

At each instant, the incident current *Ini* and voltage *Vgen* are known, so *Ina* can be calculated. Once this is done, *Inr* can be calculated from (10).

If it is assumed that the surge resistance *Ro* is 100 ohm, $Rg = 0$, initially $Ini = 0$ and a step voltage of 1V is applied to the line, then a step voltage of 1V and a step current of 10mA will propagate in synchronism up the line. This can be simulated by inserting a value of 10mA into computer memory programmed to act as a 100-element shift register. After 100 time intervals, the current step arrives at the far end. Figure 5 defines the partial currents and voltages at this instant.

The current absorbed at the far end can be calculated using:

$$Ifa = \frac{2 \cdot Ro \cdot Ifi}{Ro + RL} \qquad (18)$$

and the reflected current can be derived from:

$$Ifr = Ifa - Ifi \qquad (19)$$

This set of equations allows the program to be adapted to simulate the presence of inductors and capacitors at each interface.

Transmission Line Properties

Any twin-conductor line can be characterised by two parameters: the time it takes a pulse to propagate from one end to the other, *T*, and the surge resistance, *Ro*. Using the delay-line model, the response of a short-circuited line can be simulated. The red waveform of Figure 6 illustrates the

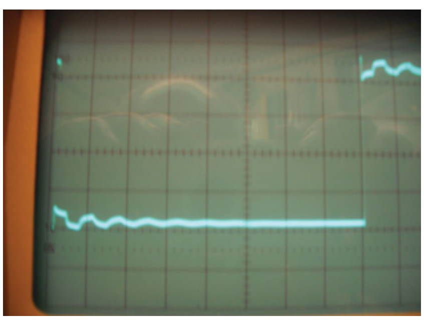


Figure 12: Waveform of voltage monitored by channel 1 (500ns/div, 0.1V/div)

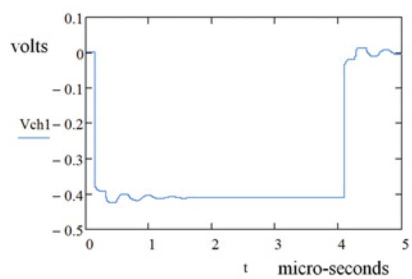


Figure 13: Simulated waveform of voltage at channel 1

response of a short-circuited line when a 10V step is applied via a 10-ohm resistor. The blue curve simulates the current in a 10 micro-H inductor. The value of this inductance was derived from T and Ro, using:

$$L = T \cdot Ro = 10 \text{ micro-H} \qquad (20)$$

If the terminations of this line are open-circuited and the source resistance increased to 1000 ohm, then the current delivered to the line would be as shown by the red stepped-waveform of Figure 7. The blue curve defines the current in a 1nF capacitor in series with 1kohm. The value of the capacitor was calculated using:

$$C = \frac{T}{Ro} = 1 \text{ nF} \qquad (21)$$

This means that the inductance and capacitance of the line can be derived from transient measurements. Similarly, the values of T and Ro can be derived from measurements of L and C.

Bench Testing

Figure 8 depicts the setup used to check the validity of the delay-line model. Since the near end was terminated with a 4.7-ohm resistor and the far end was open-circuited, this setup guaranteed that there would be many reflections of a step pulse applied to the near end. The input was a square wave, with sufficient time after each step to allow the system to settle down before the next step.

Figure 9 shows the waveform of the differential-mode current, as monitored by channel 2 of the oscilloscope. This is the response to the negative-going edges of the input waveform.

Figure 10 shows the waveform which would have been expected if the line had been lossless. The step pulse travels up the line to the far end, where the voltage doubles and the current changes sign. This reflected current propagates back to the near end, which is almost a short circuit. Here, the amplitude of the current almost doubles. Then the step propagates back to the far end.

Modelling The Current Waveform

During the period between the first and second transitions, the actual response behaves essentially as predicted. The oscillations on the flat portion of the curve are probably due to reflections coming back from the ground conductors of the test equipment. The elapsed time between the first negative-going step and the first rising edge gives a measure of the time taken for the transient to propagate to the far end and return; 166ns. This gives a value for T of 83ns. The amplitudes of the input voltage Vin and delivered current Ina are derived from the measured values of $Vch1$ and $Vch2$.

During the time taken for the step to complete the first round trip, both Vni and Ini are zero. So, $Ina = Inr$, enabling Ro to be measured using:

$$Ro = \frac{Vin}{Ina} = 100 \text{ ohm} \qquad (22)$$

The pulse arriving back at the sending end is not at all as was predicted. It has the same sort of waveform as an R-C network. The step function then morphs into a sine wave.

It was reasoned that the voltage step was radiating current out into the environment as it travelled down towards the far end. So the delay-line model was modified to simulate this effect. The response of the modified model is shown in Figure 11. This is much closer to the actual response and indicates that most of the losses are due to current radiating out of the conductors into the environment.

Modelling The Voltage Waveform

A much more interesting observation comes from an analysis of Figure 12, the waveform of the voltage applied to the terminals at the near end of the line. The sweep time of the oscilloscope has been reduced to show the positive as well as the negative steps.

The waveform of Figure 12 shows that the current delivered to the line has a loading effect on the source resistance. When the difference in the sweep times is taken into account,s it can be seen that the ripple waveform added to the applied voltage is very similar to that of the current waveform.

The modified circuit model used to simulate the current in the line was also used to simulate the waveform of voltage across the source resistance, see Figure 13.

Deductions

In the setup of Figure 8, the return conductor is connected to the earthed terminals of the test equipment. It is held at zero volts. No current can be delivered to the line via this terminal. This means that current delivered to the line flows from the earthed conductors of the test equipment, through the 4.7-ohm resistor, into the near end of the send conductor.

During the time zero to T, current flows from the send conductor into the return conductor. When the voltage step reaches the far end, the charge on the return conductor is such that its voltage is equal in magnitude, but opposite in sign, to the voltage on the send conductor. During the time T to $2 \cdot T$, current flows from the return conductor back into the send conductor, in the same direction as the delivered current; thereafter, current is flowing in both directions along the line. The analysis has also shown that losses in the line are mostly due to current departing into the environment in the form of electromagnetic radiation. ●

MICROCHIP ANNOUNCES A NEW PARALLEL FLASH MEMORY DEVICE

Microchip has announced the SST38VF6401B – a new parallel flash memory device. It is a 4M x16 CMOS Advanced Multi-Purpose Flash Plus (Advanced MPF+) device manufactured with Microchip's high-performance CMOS SuperFlash technology, a split-gate cell design and thick-oxide tunnelling injector for better reliability and manufacturability. This device conforms to JEDEC standard pin assignments for x16 memories.

With an operating voltage range from 2.7V to 3.6V, fast read and program times, and advanced protection features, this parallel Flash memory excels in a variety of applications. The memory is partitioned into uniform 32kWord and non-uniform 8kWord blocks, offering flexible erase capabilities and seamless partitioning for program code and data.

The SST38VF6401B parallel Flash memory offers high performance with flexible read and write options, including random read access time of 70ns; page read access time of 25ns; erasing sectors and blocks as fast as 18ms; erasing the entire Flash memory chip in 40ms; and a word-programming time of 7µs among other features.

www.microchip.com

INDUSTRIAL MINI I/O CONNECTOR PORTFOLIO NOW WITH FIELD-INSTALLABLE VERSION

TE Connectivity (TE) announced the extension of its Industrial Mini I/O connector portfolio with a field-installable version, which provides innovative and time-saving wire-termination, alongside being a space-saving and reliable I/O solution for industrial environments.

TE's Industrial Mini I/O solution is only one quarter the size of the conventional RJ45 plug and, as a result, provides space saving and the flexibility to use limited space on the PCB more effectively. Designed with two points of contact, this connector is built for the stringent demands of an industrial and high-vibration environment, enabling increased productivity through a reliable connection. With its innovative piercing termination, the Mini I/O field -installable version decreases the time needed to terminate the wires through soldering and, with an easy to use hand tool, the field assembly is now possible in virtually any environment.

www.te.com

NEW ARBITRARY WAVEFORM GENERATORS FEATURING DEEP MEMORY AND SIGNAL FIDELITY

Rigol Technologies EU introduces the DG1000Z series arbitrary waveform generators, the latest development in its family of fast, easy-to-use and ultra-modern test instruments.

Rigol's DG1000Z series helps engineers accomplish a wide range of testing applications by combining many functions in one easy-to-use instrument. Functions include arbitrary waveform generator, function generator, pulse generator, harmonic generator and analog/digital modulator.

The DG1000Z series also incorporates Rigol's Direct Digital Synthesizer (DDS) technology, ensuring that signals are delivered with stability, precision, purity and low distortion. These arbitrary waveform generators with innovative SiFi (Signal Fidelity) can generate arbitrary waveforms point by point, restore signal distortionless and allow precisely adjustable sample rates and low jitter (200ps).

The arbitrary waveform memory is available with 8Mpts (standard) and 16Mpts (optional). Two full functional channels can be used as two independent generators offering ±1ppm frequency stability and -125dBc/Hz phase noise. The instruments have a built-in 8 orders harmonics generator and 7 digits/s full-function frequency counter.

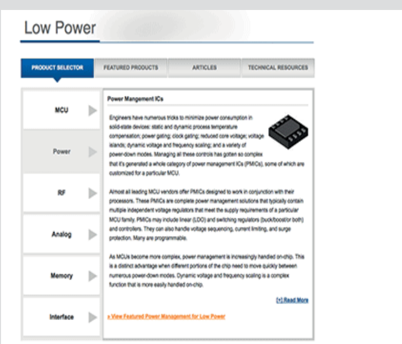
www.rigol.eu

MOUSER ANNOUNCES NEW, LOW POWER TECHNOLOGY SITE

Mouser Electronics has introduced a new Low Power Technology Site. The site offers component selection guidelines and circuit design techniques for any developer seeking to achieve the best low-power design possible, along with advice on some of the advantages and tradeoffs resulting from these techniques.

The new Low Power Technology Site available on Mouser.com has several sections designed to help developers create low-power projects. The Product Selector section is divided into different component categories and covers microcontrollers, power management ICs, RF devices, analog components, memory ICs and interface chips among others.

To learn more about low power design, visit: **http://www.mouser.com/applications/low_power/**



DUAL SYNCHRONOUS LOW-VOLTAGE BUCK REGULATOR IC COMBINES FLEXIBILITY AND ROBUSTNESS

New from Allegro MicroSystems Europe is the A8651, a dual synchronous low-voltage buck regulator IC that combines flexibility, robustness and automotive (AEC-Q100) qualification for use in multiple output systems with a 2.5V to 5.5V system rail.

The new device is a dual 2A, low input voltage synchronous regulator with an adjustable-frequency integrated high-side P-channel MOSFET and a low-side N-channel MOSFET. It incorporates current-mode control to provide simple compensation as well as excellent loop stability.

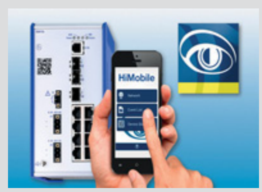
The A8651 uses external compensation to optimise the transient response without sacrificing stability. It regulates input voltages from 2.5V to 5.5V down to output voltages as low as 0.8V, and is able to supply up to 2A of load current per regulator.

Key features include an externally adjustable and synchronisable switching frequency, an externally set soft-start-time to minimise inrush currents, independent "enable" inputs and independent open-drain fault indication outputs with 7.5ms delay.

www.allegromicro.com

BELDEN IMPROVES NETWORK AVAILABILITY THROUGH MOBILE MONITORING

Belden has announcesd HiMobile, a new app from its Hirschmann product portfolio. Running on smart phones or tablets, this app improves network availability by allowing users to access status information about switches from almost anywhere. This enables administrators to respond immediately to error messages even without a PC. To avoid typing errors on the smaller keypads used on these devices, IP addresses can also be entered by scanning a QR code affixed to the switches. A further alternative is to select network devices from lists.



HiMobile is particularly suitable for applications that depend on seamless processes and reliable data communication. Possible application scenarios include machinery for the food and beverage industry, material handling systems, printing presses and robotics. The app can be used to improve network availability in the oil and gas sector or in power generation from wind power and solar energy just as effectively as in road and rail transport or at airports or ports.

www.belden.com

EZ-BOARDWARE RFI SHIELD CANS DELIVER COST-EFFECTIVE RFI/EMI SCREENING

Harwin has expanded its popular EZ-BoardWare portfolio of surface mount PCB hardware components with EZ-RFI shield cans which, when used with the company's EZ BoardWare RFI shield can clips, provide excellent RFI and EMI protection to sensitive circuitry at PCB level.

Because the cans are mounted by simply pushing them into the surface mount clips, installation costs are minimised as there is no secondary processing required. Cans can be easily removed for inspection, repair or rework without any damage to the PCB. The clips ensure secure can retention, resistant to shock and vibration.

New E-Z RFI shield cans feature a mechanically-robust, simple, five-sided box design that saves cost when compared to fence and cover styles. Cans are nickel-silver plated to ensure good screening and are available in a range of sizes to suit various applications.

The E-Z RFI shield cans are beneficial for many markets, including radio systems, wireless equipment and consumer electronics among others.

www.harwin.co.uk

NEW *LYTSWITCH-2* ISOLATED LED-DRIVER ICs DELIVER GREATER ACCURACY

Power Integrations announced its LYTSwitch-2 family of isolated LED drivers, which delivers up to 12W of accurately-controlled output power, and substantially reduces component count, resulting in simpler, smaller and more reliable LED lighting designs.

LYTSwitch-2 LED-driver ICs use primary-side control, resulting in cost-effective, single-sided PCBs with low component count. In addition, driver isolation allows the LEDs to be affixed directly to a metal heat-sink, avoiding the added expense of an electrically isolating enclosure that is often required for non-isolated drivers. Accurate constant-current (CC) output tolerance across temperature (better than ±5% at both low-line and high-line voltages) reduces the need to over-design systems in order to meet requirements such as the US ENERGY STAR minimum-lumens-delivered specification. Designs using LYTSwitch-2 ICs are also highly efficient – up to 90% in typical applications.

LYTSwitch-2 ICs protect the LED load from surges in line voltage, increasing bulb lifetime in regions where the mains voltage is subject to frequent peaks.

www.powerint.com

TTI INC STOCKS BOURNS'S WIDE PORTFOLIO OF TRIMMING POTENTIOMETERS

Bourns's surface-mount, through-hole, sealed and open Trimpot trimming potentiometers can now be ordered from TTI Inc. The components are ideal for a variety of circuit adjustments in all types of electronic equipment. The many available physical configurations and the ability to withstand today's manufacturing environment offers the designer flexibility in selecting the best trimmer for any application.

Bourns's Trimpot trimming potentiometers are easy to adjust and offer a reliable and stable output over time. The components are available in top, bottom, side, front and back adjust styles and come in sizes ranging from 2mm up to 30mm.

Packaged in tube, bulk, embossed tape, ammo pack, and tape and reel format, they are compatible with pick-and-place equipment. RoHS compliant, halogen-free, as well as Mil-spec versions are available.

TTI in Europe strives to be the distributor of choice by introducing new product technologies and by stocking broad and deep inventory across its franchise base.

www.ttieurope.com

NEW DUAL N-CHANNEL ENHANCEMENT-MODE MOSFET FOR BATTERY APPLICATIONS

Advanced Power Electronics Corp (USA), a Taiwanese manufacturer of MOS power semiconductors for DC-DC power conversion applications, has announced a new dual N-channel enhancement-mode power MOSFET for battery applications.

The AP9922AGEO-HF-3 device supports 1.8V gate drive and features a low on-resistance of 18mΩ, a drain-source breakdown voltage of 20V and a continuous drain current of 6A. RoHS-compliant and halogen-free, the device is available in the small and thin TSSOP-8 package.

Advanced Power Electronics Corporation (APEC) was established in Taiwan in 1998, as a supplier of MOS power discretes, IGBTs and Power ICs, which enable cost-effective efficient solutions for new and existing power applications. The company's wide range of solutions targets the computing, consumer electronics, display, communications and industrial segments among others.

www.a-powerusa.com

POLYPROPYLENE FILM CAPACITORS FOR POWER SUPPLY, DC AND PULSE APPLICATIONS

AVX Corporation has released its new FM Series medium power film capacitors. Non-inductively wound with dry, metallized polypropylene film dielectric and encapsulated in a flame-retardant plastic case sealed with self-extinguishing, thermosetting epoxy resin and featuring RoHS-compliant double metallized polyester film electrodes in series construction, the FM Series capacitors exhibit high reliability at high current stress, high dv/dt capability, high moisture resistance, high capacitance stability, low losses, self-healing properties and long useful lifetimes.

Rated for capacitance values spanning 0.01µF to 0.47µF, voltages spanning 250V to 2000V, and operating temperatures spanning -40°C to +105°C, the new FM Series capacitors are designed for high frequency and high pulse rise-time circuits, high-voltage power supplies, switch mode power supplies (SMPS), power converters, snubbers and electronic lighting ballasts, such as compact florescent lamps and LEDs.

The capacitors are available in 17 case sizes (A-S), 14 voltages (250-2000V), three capacitance tolerances (±5%, ±10%, and ±20%), and two lead lengths (3.5mm and 22mm).

www.avx.com

OMC LAUNCHED A NEW POLYMER-FIBRE MICROSITE

OMC, one of Europe's longest-established specialist manufacturers of optoelectronics and a pioneer in industrial fibre optic transmission, has launched a new microsite – www.polymerfibre.co.uk – dedicated to explaining the advantages of polymer fibre and making it simple for customers to buy exactly what they need.

OMC has led industry in the use of polymer PMMA fibre for many years, supplying fibre to the majority of UK and European users directly and through distribution. As OMC manufactures standard and bespoke polymer and glass fibre cable assemblies for a wide range of industries and applications, the company is well-positioned to offer impartial advice on which solution is the best fit for any particular requirement.

As well as explaining all about polymer fibre and OMC's significant product range, a key feature of the site is that customers can buy polymer fibre online directly from OMC, achieving the most competitive pricing possible.

www.omc-uk.com

IOT LOW POWER CONSUMPTION INTEGRATED WIRELESS CONTROLLER FROM LPRS

LPRS, a manufacturer of short-range wireless devices, now offers Internet of Things (IoT) system builders with a system-on-chip fully integrated wireless controller suitable for remote, battery-powered sensor systems, which can offer current consumption as low as 32µA.

The low cost, high-security easyRadio Integrated Controller (eRIC) offers designers seven power-saving modes of operation to ensure maximum battery life of remote sensors. The LPRS eRIC transceiver power-saving modes provide control of the duty cycle of the receiver so that the ‘ON’ time can be set to 12.5%, 6.25%, 3.1% , 1.56%, 0.78%, 0.39% and 0.2% with corresponding levels of power saving from its “always on” current of 16mA. The transmitter may then be independently set to the same duty cycle as the receiver or longer as required for transfer of data. Up to 250Byte data-packets are supported throughout all operating modes and up to 500kbs over air data rates are available.

www.lprs.co.uk

WÜRTH ELEKTRONIK’S MAGI^{3}C-VDRM MODULES ARE EXCLUSIVE TO RS COMPONENTS

RS Components (RS) has announced exclusive availability of a new series of innovative PCB-mount variable step-down regulator module ICs from Würth Elektronik. The award-winning MagI^{3}C-VDRM modules comprise a fully integrated and low-EMI-noise current-mode DC/DC power supply that includes the switching power stage, passive components and control circuitry in a single low-profile and small-outline package, saving valuable design-in time for engineers and reducing time-to-market.

Providing high efficiencies and accurate regulated output voltage, the series offers a wide input voltage range from 6 to 42V DC, output voltages from 0.8 to 24V, and maximum output currents from 1 to 5A, as well as built-in compensation circuitry and soft-start functionality for smooth and safe power-up. Delivering stable and low-ripple voltages for components such as microprocessors, DSPs, FPGAs and MCUs and I/O interface applications, typical uses for the MagI^{3}C-VDRM series are Point of Load (POL) DC/DC conversion in system power supplies and in server and datacom/telecom applications among other markets.

www.rs-components.com

NEW 50MA VERSION OF USFF FAMILY: LOW POWER LOSS AND PRECISE-ACTING FUSE

SCHURTER is expanding its extensive range of surface-mount chip fuses with a unique model: the new 50mA fuse in the USFF family sets itself apart from standard commercial products through a lower voltage loss and an exact opening time. The USFF 1206 thus offers the safe solution for the optimal operation of sensitive electronic systems where such performance is critical.

With the new 50mA version of the USFF 1206, SCHURTER is offering a true market innovation. The wire-bonding technology used in the USFF 1206 allows stable, reliable operation at ambient temperatures from -55°C to 90°C, making it ideal for protection of applications with sensors, ICs and batteries.

The new fuse is particularly well suited for the protection of smart metering systems.

www.schurter.co.uk

FIRST CONGATEC MINI-ITX MOTHERBOARD

Congatec has extended its successful board-level product range with the first industrial Mini-ITX motherboard. The new embedded motherboards will meet the same standards and quality as the established Computer-On-Modules from congatec. Additional services include 7+ years availability, global technical support, extended manuals, specifications and customized design services.

The conga-IGX Mini ITX board is based on AMD Embedded G-Series SOC technology and integrates the next-generation computing power of the “Jaguar” based processor and high performance AMD Radeon graphics cores in a compact package. The integrated AMD Radeon graphics feature the Universal Video Decoder 4.2 for seamless processing of BluRays with HDCP (1080p), MPEG-2, HD and DivX (MPEG-4) videos.

Users benefit from outstanding multimedia performance, an excellent performance-per-watt ratio and flexible task allocation on the CPU and GPU. Thanks to these features, the new conga-IGX board is an ideal solution for cost-sensitive visualization and control applications.

www.congatec.com

NEW TCVCXO DELIVERS ±0.14PPM STABILITY IN A 5 X 3.2MM PACKAGE

IQD’s new IQXT-210 series TCVCXO offers frequency stabilities to ±0.14ppm over the full industrial temperature range of -40 to 85 degrees C. This new model is approaching OCXO performance levels, in a miniature 8-pad 5 x 3.2mm package.

Powered from a 3.3V supply the IQXT-210 has a typical current draw of only 12mA, dependent on the frequency, which can be specified between 10MHz to 50MHz.

There are 11 standard frequencies initially offered, including 12.8MHz, 19.2MHz and 26.0MHz. Output can be specified as either HCMOS, 15pF load or Clipped Sine, into 10k Ohms load. The oscillator can be specified to include various pulling range options, from ±5ppm to ±10ppm and also ±10ppm to ±15ppm, enabling the frequency to be adjusted by a fixed amount for various applications. It also allows for the oscillator to be used remotely.

The IQXT-210 is primarily designed for low power consumption applications.

www.iqdfrequencyproducts.com

AMPHENOL’S LATEST 38999 HIGH POWER CONNECTOR HIGHLIGHTED AT DVD 2014

At the defence event DVD this year, Amphenol Ltd will be highlighting its latest circular and rectangular power connectors developed for applications with high power capability and comprehensive safety requirements plus full RoHS compliance (stand SP46). Designed to meet various specifications, these connectors allow reliable performance even at high current and voltage ratings, whilst different housing materials offer a choice of aluminium for a high strength-to-weight ratio or stainless steel and aluminium bronze for their corrosion resistance. Furthermore, the use of RADSOK contacts creates an electrical interface that exceeds typical interconnect requirements via a hyperbolic socket contact construction which distributes normal forces over a high percentage of the mating surface to ensure a smooth and even engagement force with exceptionally high performance under vibration. The Rhino 38999 Series High Power Connector will be highlighted at the show.

Also exhibited will be standard and customised filter connectors including products for EMC and EMP protection.

www.amphenol.co.uk

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