February 2015
Volume 121
Issue 1946
£5.20
www.electronicsworld.co.uk

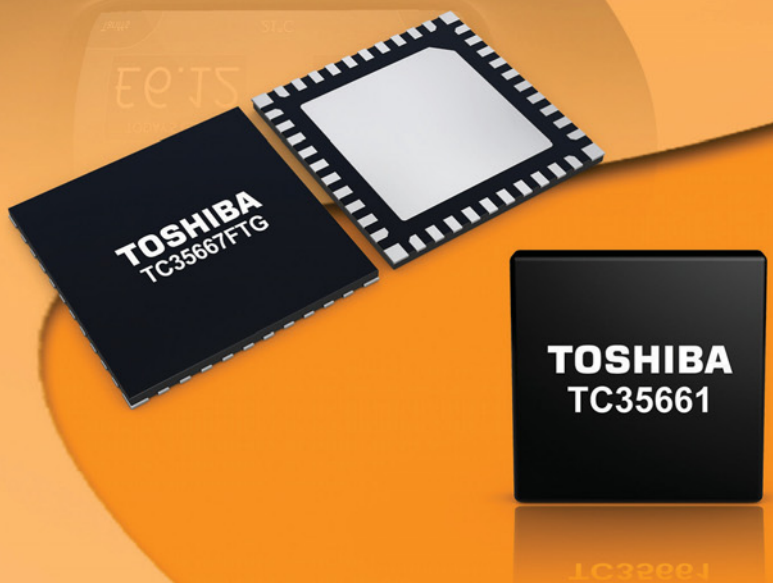
Electronics WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Bluetooth® SMART

Communications in a Low Energy Internet of Things

By Toshiba Electronics Europe



SPECIAL REPORT:

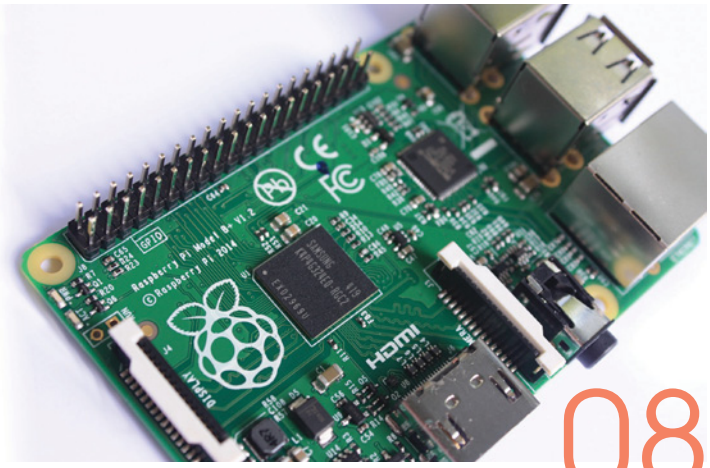
- Oscillators
- Current conveyors
- Analog design

Technology
Bringing the hospital home

Feature Series:
RF design

Products
Latest connectors and other components


Digi-Key CORPORATION
Login
Register | Why Register?
United Kingdom | 0800 587 0991
GBP | Change Country
Search
Online Ordering
Order Status
Newest Products
Product Index
Supplier Index
Catalogue
Resources
TechZone
TechXchange Community
Supply Chain HQ
Need Help?
BOM MANAGER
Access Over 975,000 In-Stock Components!
GO
NEW FEATURES
Enhancing YOUR Digi-Key Experience
FREE SHIPPING
WORLD'S LARGEST SELECTION
of electronic components AVAILABLE for immediate shipment!
POWER TRIPLE LOCK
For improved power and signal applications
• Connector position assurance
• Terminal position assurance
• Audible click
LEARN MORE
THE WORLD'S LARGEST SELECTION OF ELECTRONIC COMPONENTS
Available for Immediate Shipment!®
FREE SHIPPING
ON ORDERS OVER £50!*
DIGIKEY.COM
0800 587 0991 • 0800 904 7786
DIGIKEY.CO.UK
Digi-Key CORPORATION
1,000,000+ PRODUCTS IN STOCK | 650+ INDUSTRY-LEADING SUPPLIERS
*A shipping charge of £12.00 will be billed on all orders of less than £50.00. All orders are shipped via UPS for delivery within 1-3 days (dependent on final destination). No handling fees. All prices are in British pound sterling and include duties. If excessive weight or unique circumstances require deviation from this charge, customers will be contacted prior to shipping order. Digi-Key is an authorized distributor for all supplier partners. New product added daily. © 2015 Digi-Key Corporation, 701 Brooks Ave. South, Thief River Falls, MN 56701, USA
Elektra 2014
Distributor of the Year



08

Cover supplied by TOSHIBA ELECTRONICS EUROPE
More on pages 14-15

REGULARS

44

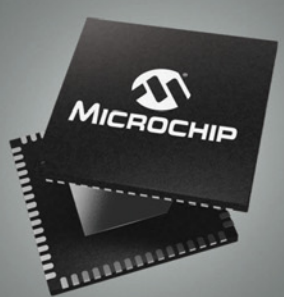
FEATURES

Intelligent Design

Starts with Intelligent Analog PIC® Microcontrollers

INTELLIGENT
ANALOG

Analog design is difficult and consumes precious development time. Microchip's intelligent PIC® MCUs integrate analog functions such as high performance Analog-to-Digital Converters, Digital-to-Analog Converters and Op Amps providing simple-to-use interfaces that ease analog design. A single-chip solution enables reduced system noise and provides higher throughput, while dramatically reducing design time and cost.



Applications

- Environmental quality sensors
- Portable medical equipment
- Industrial equipment
- Power conversion
- Efficient motor control
- Lighting
- Power measurement and monitoring
- Energy harvesting equipment
- Solar inverters

microchip DIRECT
www.microchipdirect.com

MICROCHIP

microchip.com/intelligentanalog

THE HIDDEN VALUE IN FORGOTTEN INVENTORY

> An effective asset recovery partnership can quickly demonstrate its value to a business through space- and money-savings and breathe new life into forgotten inventory

What do you do with returned electronic devices that are no longer needed? Not sure? Nothing? Place them in a warehouse and worry about them at a later date?

If the answer is "Yes" to any of these questions then you are certainly not alone. There are always other activities in organizations that creep in and take higher priority. This is normal. It is not unusual for us to encounter businesses that have stacks of devices containing hard disk drives (HDD) in storage, such as laptops or set-top boxes. These devices may have reached the end of their lease period or have been swapped as part of an upgrade process. Typically the volumes of such inventories can be unclear and will be left untouched, becoming your forgotten inventory.

Such inventory will often have reached the end of its depreciation curve but managers can be loath to destine it to scrap as it does not seem right or especially green in an increasingly environmentally-conscious society. Even with no book value left, it does not mean it's not costing money. Money is spent on space, electricity and other resources, as such products gather dust. So what can be done?

Periodically, organizations may choose to scrap or recycle such inventory and there is nothing fundamentally wrong with this; however, it may add to the organization's costs. Another option is to speak with a reputable company with expert knowledge and experience with asset recovery. Asset recovery will investigate the potential value of the forgotten inventory and companies may receive cash in return, turning cost into profit.

With growing pressure on businesses to increase revenues and cut costs, asset recovery is one way to support this overarching business objective. Specialist HDD asset recovery companies test HDDs for functionality and performance, and resell them into secondary markets. Reputable asset-recovery companies would also ensure that HDDs have any data properly deleted to recognized industry standards such as Infosec 5. Doing this professionally results in quality refurbished HDDs being sold into the market, which attracts higher prices yet still remains great value for the markets in which they are sold and used. The other parts of such forgotten inventory are then recycled responsibly.

Value is also generated through environmentally-responsible disposition, data-deletion assurance as well as the simplicity of performing such transactions knowing that a professional asset-recovery service will take care of everything. Above all, organizations get to extend the lifecycle of electronic products.

There are three fundamental considerations for implementing an asset-recovery programme to harvest HDDs and the revenues within:

- **Select the right partner** – Making the right choice of partner is critical. You should satisfy yourself that they operate responsible processes and to standards. They need to be a company you can trust for a professional service at a fair price.
- **Check the processes** – Satisfy yourself that product is handled and processed the right way to generate the best yields and therefore the best value for you. A proven testing, soft-repair and data-deletion solution to recognized industry standards offers peace of mind that your brand integrity remains intact.
- **Responsible recycling** – any part of your products that cannot have their lifecycles extended need to be processed and recycled responsibly through controlled processes. This is an important factor in supporting your organization's environmental and corporate social responsibility objectives.

Returned electronic devices needn't become a burden to the business. An effective asset-recovery partnership can quickly demonstrate its value to a business through space- and money-savings. Importantly, it can breathe new life into forgotten inventory and enable new revenue streams for your organization.

Sven Boddington is Vice President of Global Marketing and Client Solutions at Teleplan (www.teleplan.com)

EDITOR: Svetlana Josifovska
Tel: +44 (0)1732 883392
Email: svetlanaj@sjpbusinessmedia.com

SALES: Sunny Nehru
Tel: +44 (0)20 7933 8974
Email: sunnyn@sjpbusinessmedia.com

DESIGN: Tania King
PUBLISHER: Justyn Gidley

ISSN: 1365-4675

PRINTER: Buxton Press Ltd

SUBSCRIPTIONS:
Subscription rates:
1 year: £62 (UK);
£89 (worldwide)
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com

SJP business media

2nd Floor,
52-54 Gracechurch Street,
London, EC3A 0EH

Follow us on Twitter
@electrowo

Join us on LinkedIn

HEALTH INNOVATION VILLAGE IN FINLAND TO HELP STARTUPS SPEED UP TECH SOLUTIONS

GE Healthcare officially opened its first health tech startup campus in Finland, called the Health Innovation Village, at its headquarters in Helsinki. The campus already boasts 20 health tech startups operating in the fields of wireless technologies, sensors, apps and cloud services.

Health-related solutions are the largest and most important Finnish export sector; some 47% of Finnish hi-tech exports are for the health sector. As such, the Village was created to foster an ecosystem for health tech startups to flourish in.

GE has a history of working with startups through GE Ventures, as the company strongly believes collaboration feeds innovation.

"The health sector needs speedy clinically-relevant and affordable innovations. We believe the magic formula is the combination of large global corporations and agile startups, co-located. We wanted to bring them closer, because innovations are created when people meet. Living close to startups, exchanging ideas and eventually working together on innovative projects is fresh thinking. Eventually, this benefits our customers, too," said Didier Deltort, Managing Director of GE Finland.

The Health Innovation Village includes startups covering technology innovations that feed into many aspects of the health sector, such as comfort for premature babies, monitoring, maintaining fitness and other challenges as part of larger programmes, including designing smart baby clothes and bringing the hospital home.

The newly set up Health Innovation Village will help with sensor-laden smart clothing for babies, such as this from Finish company Beibamboo

INTEL AND IBM OUTLINE 14NM FINFET STRATEGIES

Intel, which began using FinFET transistors commercially in its Ivy Bridge and Haswell processors at the 22nm process node, has disclosed some of the innovations behind its second generation of FinFET technology, at the IEEE International Electron Devices Meeting (IEDM) in San Francisco last December.

Made on a standard bulk silicon substrate, the new Broadwell 14nm technology is in production as part of Intel's latest family of microprocessors.

Among the features Intel discussed were a novel doping technique to prevent current leakage under the fins and maintain very low doped fins, resulting in improvement in variation; two levels of air-gap-insulated interconnects at ultra-narrow 80 and 160nm minimum pitches, yielding a 17% reduction in capacitance delays; eight layers of 52nm pitch interconnects embedded in low-k dielectrics; an embedded 140Mb SRAM memory with a tiny cell size of 0.0588μm^2; and saturated drive currents significantly higher than for Intel's 22nm first-generation FinFETs (improvements of 15% and 41% for NMOS and PMOS transistors, respectively). The transistors operate from a supply voltage of only 0.7V.

Researchers also discussed how aggressive design rules enabled the production of very high aspect-ratio rectangular fins (8nm wide and 42nm high) at unprecedented levels of uniformity.

IBM, meanwhile, described a very different approach to 14nm FinFET transistors. The IBM devices are made not from a standard bulk silicon substrate but from an insulating substrate known as SOI (silicon on insulator). Although a more expensive material, SOI simplifies manufacturing in terms of device isolation. These devices are more than 35% faster than IBM's 22nm planar (i.e. standard, non-FinFET) transistors, with an operating voltage of just 0.8V.

The IBM technology features what may be the smallest, densest embedded DRAM memory ever demonstrated with a cell size of just 0.0174μm^2 for high-speed performance in a fully integrated process flow. IBM also designed an elegant way to make the technology suitable for both low-power and high-speed applications, using a unique dual-workfunction process that optimizes the threshold voltages of both NMOS and PMOS transistors without any mobility degradation in the channel.

Because the technology is envisioned for use in system-on-a-chip (SoC) applications ranging from video game consoles to enterprise-level corporate data centres, the IBM design also features a record 15 levels of copper interconnect to give circuit designers more freedom that ever before to distribute power and clock signals efficiently across an entire SoC chip, which may be as large as 600mm^2.

FinFETs

The development of increasingly sophisticated and energy-efficient CMOS technology for mobile, client and cloud computing depends on a continuing stream of advances in the process technologies with which the complex integrated circuits are built. Among the most promising chip technologies are transistors called FinFETs, which have attracted significant R&D investment and are already used in commercial products. However, the technology is complex and the path forward isn't settled.

All modern transistors have a channel to conduct electricity and one or more gates to turn the current on and off. FinFETs have long, thin fin-like channels (hence the name) surrounded by multiple gates. This design leads to greater performance and enhanced energy efficiency.

RADIOMETRIX

www.radiometrix.com

500mW UHF High Performance Radio Modem

The M48-458-SFX2 presents the M48 modem IC combined with the SFX2 radio module & suitable interface circuits, power supplies, connectors to provide a complete RS232 multi-chanel radio modem interface.

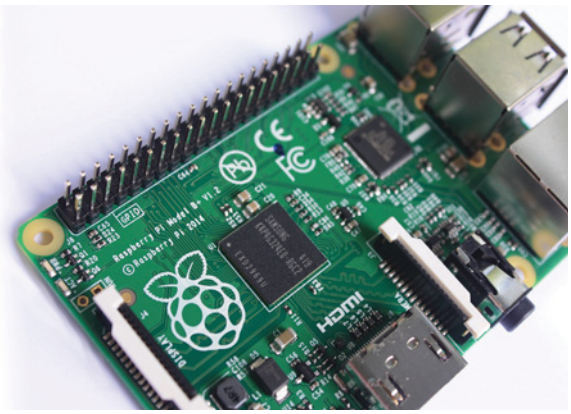
Usable range over 5km.

VISIT http://www.radiometrix.com/m48-458-sfx2

REAL RADIOS FOR REAL APPLICATIONS

THIS SERIES PRESENTS THE RASPBERRY PI SINGLE-BOARD COMPUTER, ITS FEATURES AND BENEFITS, AND HOW TO USE IT IN VARIOUS ELECTRONICS PROJECTS

Downloading The Raspberry Pi's Operating System



BY **SEAN MCMANUS**

Before anything can be done with the Raspberry Pi, it needs an operating system, which enables it to use the computer's basic functions, manage files and run applications, such as word processing or web browsing. Those applications use the operating system as an intermediary to talk to the hardware and they won't work without it.

The operating system used on the Raspberry Pi is GNU/Linux, or just Linux for short.

Creating A NOOBS Card

The easiest way to get started with the Raspberry Pi is to use the NOOBS (New-Out-Of-Box Software). Don't underestimate the power of this software, especially if you're a more experienced user: NOOBS is easy to copy to the SD or MicroSD card and provides a simple menu for installing a number of different operating systems, including different versions of Linux, RISC OS and XBMC media centre software. There are cards with NOOBS already on them, which might be the quickest way to get started.

However, it is useful to know how to create your own NOOBS card: It means you can get started with a new card in about 20 minutes, since a specific operating system can be downloaded from the Raspberry Pi website and easily installed on the SD or MicroSD card.

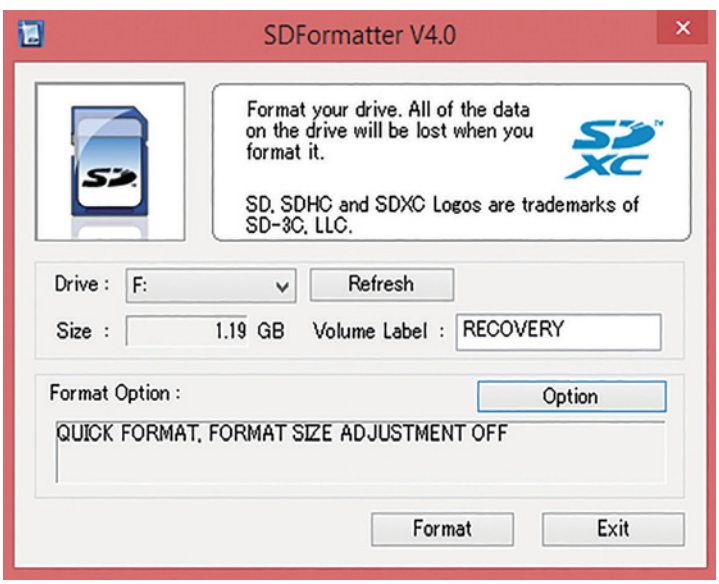


Figure 1: SDFormatter, used to format the SD or MicroSD card on Windows

Downloading NOOBS

On the 'www.raspberrypi.org/downloads/' website there are two versions of NOOBS. I recommend NOOBS Lite because it offers a wide range of operating systems and media centre software. It requires a network connection on the Raspberry Pi, so it's not appropriate for Model A.

The other version is the offline and network install NOOBS, which includes everything needed for the Raspbian Linux operating system in one file that can be copied on to an SD card. This version doesn't need an Internet connection on the Raspberry Pi.

Formatting The SD Card

For best results, you'll need to format your SD or MicroSD card. You can use a program available from the SD Association called SDFormatter on Mac and Windows, found it at www.sdcard.org/downloads/formatter_4/.

If using Linux, use GParted to format your card.

Our recommended approach for flashing an SD card using a Linux-based computer does not require any additional software. We're using Ubuntu, the most

popular desktop distribution, so you might see some variations if you prefer a different distribution.

These are the steps:

1. The utility called GParted is used to set up the SD card on Ubuntu. It needs to be run with root permissions, so start it by issuing a command from the terminal. Enter the following: sudo gparted.

   You can open a terminal window through Dash Home in Ubuntu, or the applications menu in your distribution, or use a keyboard shortcut (Ctrl+Alt+T in Ubuntu). Figure 2 shows GParted running on the desktop.
2. Click at the top right to choose the SD card.

   Take particular care here. Choosing the wrong disk can seriously damage your hard drive. We know this is our SD card because it shows a capacity of 7.4GB and our hard drive has a capacity of 500GB.
3. The main window shows the partitions on your card.

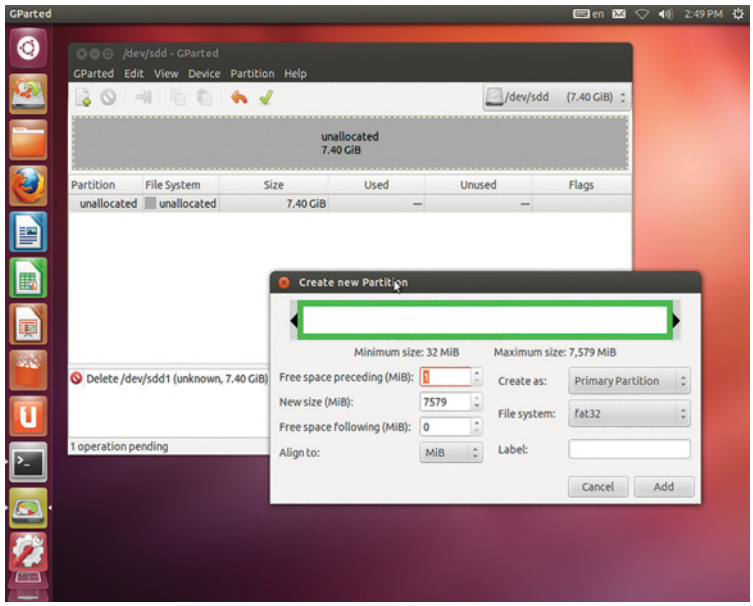


Figure 2: GParted, running on the Ubuntu desktop

   You want to delete them, so click them in turn and then click the delete icon on the toolbar.

   The delete icon looks like a No Entry sign, or the international No symbol. This won't take effect yet: You queue up the actions you want to carry out and then trigger them all when finished. (If you can't set a partition to delete because it has a key icon beside it, right-click the partition and choose Unmount in the menu that appears.)
4. Click the unallocated partition and click the Add Partition button. It's on the toolbar as a picture of a blank page with a plus sign on it.
5. The pop-up window appears, seen in the foreground in Figure 2. Click the menu to change the file system to FAT32. Click the Add button. Again, this doesn't take effect immediately.
6. Click the tick (or check mark) button on the toolbar to carry out the actions you've queued up, which remove the existing partitions and add a single new FAT32 partition.

Copying NOOBS to your SD or MicroSD card

With a formatted SD or MicroSD card and a zip file for NOOBS downloaded from the Raspberry Pi website, it's just a matter of simply copying the files to the card, enabling you to set up the Raspberry Pi. ●

This is an edited extract from Raspberry Pi for Dummies, 2nd Edition, by Sean McManus, published by Wiley, December 2014

Driving Mobile Displays

LUCIO DI JASIO, ELECTRONICS ENGINEER AND TECHNICAL AUTHOR, PRESENTS THIS SERIES ON EMBEDDED USER INTERFACE DESIGN ON A BUDGET

The undisputed centrepiece of every user interface design is the display. While cell phones and smart phones in particular have increased the expectations of our customers in terms of resolution and colour depth, there is one positive side-effect I can ascribe to their (smart phone) market success: TFT display prices have dropped over the last few years. It has been a typical consumer market dynamic: volumes going through the roof, prices plummeting and generation after generation of new display modules coming to the market at a breakneck pace.

For us, at the fringes of this market, it's a blessing and a curse. A blessing because the technology has progressed so fast and the value/price ratio has improved steadily. A curse because in a consumer market there is no expectation of product longevity. Every new generation of displays takes over the market from the previous generation after a short time (often 12 to 18 months), and manufacturers competing fiercely for few margin points come and go (bankrupt) just as fast. Most embedded control applications simply cannot keep up with such a market. Customers expect a product to be available and maintained for a decade at least.

HX8347 or IL9341?

Mikromedia boards can offer a great example of the contrast between these two worlds moving at such different speeds. Almost all components on those boards are available through the normal distribution channels and have a reasonable life expectancy for all embedded control purposes, except the TFT display module.

When originally conceived, Mikroelektronika certainly negotiated with its suppliers a good volume of those 3.2" display modules (see the MultiInno MI0283QT2 module in Figure 1) counting on the sum volume of all different Mikromedia models, a dozen today with 8-, 16- and several 32-bit architectures, considering their high production volumes. And yet, less than two years after launch, faced with the impossibility to procure any more of the originally chosen brand and model, it had to succumb and switch to a different part number (MI0283QT9A).

By the nature of the consumer market, the new display was identical as perceived by the final user, if not better in colour fidelity and contrast. But to the developer it was/is a very different object. Despite only the last digit difference in the part number (QT2 vs QT9A), the new modules feature a different display controller chip IL9341 (instead of the previous HX8347), which forced a rewrite of the protocol used to communicate with the main microcontroller.

Fortunately, the Microchip Library for Applications's (MLA's) well thought-out modular approach to the design of the graphics libraries reduces the complexity of responding to such disruptive market forces. Supporting a new display module can be as easy as linking in a single, new, source file and changing a single line of code:

```
#define GFX_USE_DISPLAY_CONTROLLER_IL9341
```

> The most important file is certainly the HardwareProfile (.h). This is used by all MLA libraries and provides the very first abstraction layer from the details of the specific board/application layout

Hardware Profile

The MLA, like any good application library, provides its great flexibility thanks to the diligent use of a number of configuration files. Understanding their roles and inter-relationships is key to a solid design and its longevity.

The most important of such files is certainly the HardwareProfile (.h), used by all MLA libraries, which provides the very first abstraction layer from the details

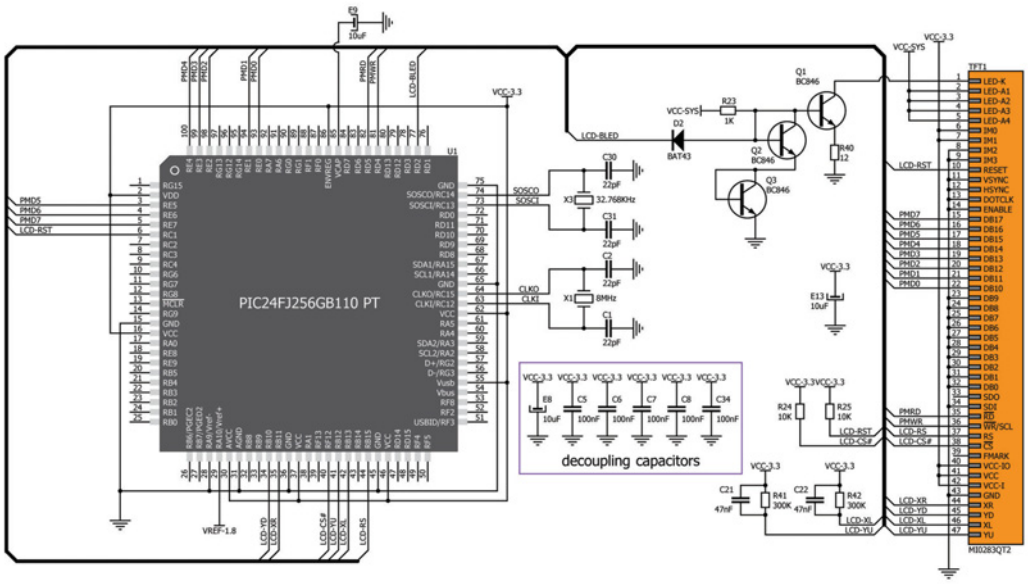


Figure 1: The Mikromedia PIC24 schematic, a detail of the display module connections

of the specific board/application layout. Here is where pins are assigned to peripheral devices. Analog and digital input/outputs are assigned to resources so the individual library modules can adapt to the specific design details of our applications. The file's contents, mostly macro definitions, are grouped in sections for ease of reference and maintenance. The display section, for example, will contain details about the (parallel) nature of the interface to the display controller used, the touch controller type and the allocation of the analog and digital input/output pins used.

You can immediately match the symbol definitions in the listing of Figure 3 with the schematic detail shown in Figure 4 to understand how the HardwareProfile abstraction works.

For any given Mikromedia board there needs to be only one common hardware profile that, once tested and trusted, can then be re-used for all subsequent applications.

Configuration Files

There are then a number of configuration files, one for each library module. The graphics library, has its GraphicsConfig(.h), the MDD File System library has its FSconfig(.h) and so on. They do contain mostly macros and symbol definitions too, but their role is that of adapting each library to specific application at hand. For example, the Graphics library configuration file (GraphicConfig.h) might contain "switches" to enable the use of particular font and bitmap resources, a selection of widgets and even more granular options for rendering gradients and/or partial bitmaps.

Configuration files are not as much concerned with the hardware setup as with optimal use of program space. A well-crafted configuration file can provide the optimal balance between performance and features required by an application and the amount of code space the library will absorb.

Each project/application can have a set of unique configuration files (one for each library used), although the hardware profile remains common to all other applications for the same board.

```
...
/*********************************************************************/
#define FONTDEFAULT             TerminalFont
#define USE_FONT_FLASH                  // fonts located in internal flash
//#define USE_FONT_EXTERNAL             // fonts located in external memory
//#define USE_ANTIALIASED_FONTS  // disable anti-aliased fonts

/*********************************************************************/
#define USE_BITMAP_FLASH            // bitmaps located in internal flash
//#define USE_BITMAP_EXTERNAL           // bitmaps located in external memory
...
```

Figure 2: Segment of a GraphicConfig.h file

```
...
/*********************************************************************
 * IOs for the Display Controller
 *********************************************************************/
...
// Definitions for RS pin
#define DisplayCmdDataConfig()  _TRISB15 = 0
#define DisplaySetCommand()     _LATB15 = 0
#define DisplaySetData()        _LATB15 = 1

// Definitions for CS pin
#define DisplayConfig()         _TRISF12 = 0
#define DisplayEnable()         _LATF12 = 0
#define DisplayDisable()        _LATF12 = 1
...
```

Figure 3: Segment of the HardwareProfile.h file for the Mikromedia PIC24

The Path To Harmony

Over the last decade, the MLA has proved incredibly valuable by defining a unified software platform, serving all Microchip processors with 8-, 16- and even 32-bit architectures (more than 1,000 at last count), featuring hundreds of demo projects and targeting a couple dozen different demo boards. This has been possible because of the careful separation between hardware profiles and library configuration files.

In the last couple of years though, a team of mostly 32-bit application engineers has decided to break free from "the group" and sprint ahead with a new and improved software

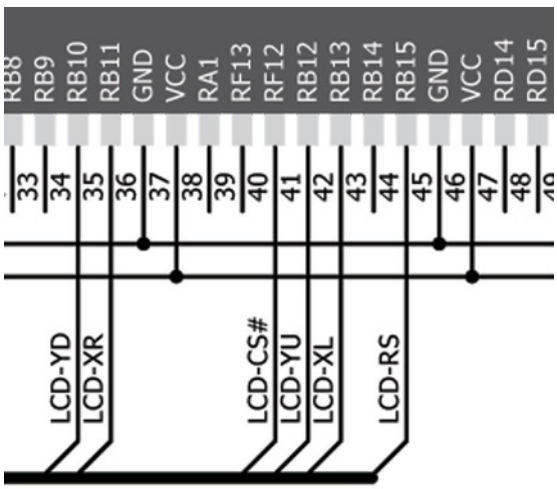


Figure 4: Detail of the RS and CS pin connections to the microcontroller ports, among others

USER INTERFACE DESIGN FOR EMBEDDED APPLICATIONS

Lucio Di Jasio is EMEA Business Development Manager at Microchip Technology. He has been covering various technical and marketing roles within the company's 8, 16 and 32-bit divisions for the past 18 years. Lucio has published several books on programming for embedded control applications, and we have three copies of his book '*Graphics, Touch, Sound and USB, User Interface Design for Embedded Applications*' to give away at the end of the series. If you want to be in with a chance, please write to the Editor at svetlanaj@sjpbusinessmedia.com mentioning the book in the heading.

architecture, designed for maximum performance on 32-bit microcontrollers. This has become known as the "Harmony" project.

As in a bicycle race, "the group" is now teaming up to catch the "fugitives" and reconcile their work and many innovations by creating a new MLA and rebranding the original library as "legacy MLA". This has perhaps confused some users who wondered about the destiny of the MLA and its relationship to the Harmony project.

First of all, there is nothing wrong with legacy MLA. In fact my last book (*"Graphics, Touch, Sound and USB. User Interface Design for Embedded Applications" Lulu.com – ISBN: 978-1-304-60654-9*) is based entirely on its original design, and its (MLA) sources will be available for many years to come. If anything, legacy MLA (and the December 2013 release in particular) represents the most stable version available to date.

The new MLA is instead a fast-moving target. It is adopting the new naming conventions used in Harmony and most of the new folder structure that comes with it, in the hope to provide an easy migration path between the two libraries.

At the same time, the authors are trying to avoid architectural detail that might penalize non-32-bit microcontrollers.

After all, the intent remains the same, one development Platform with capital 'P'.

Coming Up

In the following articles in this series I will continue to explore the "legacy" MLA design and its use to simplify and expedite the design of embedded user interface applications. ●

Two Loops?

MYK DORMER IS A SENIOR RF DESIGN ENGINEER AT RADIOMETRIX LTD **WWW.RADIOMETRIX.COM**

The PLL frequency synthesizer is by now one of the more iconic and familiar radio frequency sub-systems. Its ability to provide a stable, low noise, programmable frequency source puts it at the core of many of low-power wireless transmitters and receivers, where previously a crystal would give only fixed-frequency operation. It has made possible simple multichannel devices, and has made frequency-agile and frequency-hopping techniques widespread.

Unfortunately, as with all things, there are compromises and limitations. Once the obvious limits of VCO tuning range and digital circuit speeds have been understood, the fundamental tradeoff at the core of every frequency synthesizer will be loop bandwidth versus phase noise and frequency resolution.

> Lacking the elegant simplicity of single-loop designs, multiple-loop synthesizers do allow contradictory design requirements, such as low noise and vibration resistance, to be combined in the same system

In the simplest case, a PLL frequency synthesizer is a phase comparator controlling a VCO via the lowpass "loop filter" that defines bandwidth and settling time. The VCO output is passed through a variable ratio divider – "N counter" – back to one of the phase-comparator inputs; the other receives the "reference" – or "step" – frequency, divided down from a stable, fixed source.

In this simple case the VCO will "lock" to a frequency equal to N multiplied by the reference frequency. For 25kHz channel steps starting at 200MHz, ref = 25kHz and N = 8000 (and 8001, and 8002, and so on). So, you then set the loop filter bandwidth to give you the settling time you need and everything is just fine, or is it?

Not quite. The interesting problems start with that loop filter. It needs to be at the same time as wide as possible – for fastest lock-in time, and to allow the loop to cancel out mechanical vibration in the VCO – while also being as narrow as possible, to reduce reference-frequency breakthrough from the phase comparator and roll off the phase comparator output noise, as amplified by the loop ratio.

In simple "integer divider" PLLs these tradeoffs limit the choice of both loop bandwidth and frequency resolution: it is challenging to design a loop with adequate phase noise for narrowband use, a frequency step well below 25kHz and under 25ms lock time ... in doing so, the resultant loop bandwidth will be reduced below the point that the loop cancels VCO microphony.

There are a number of techniques used to overcome this tradeoff, for faster loops with lower noise and finer resolution. Current "RF system on silicon" approaches favour fractional-N techniques, whereby (using considerable amounts of complex logic) the division ratio of the loop divider is no longer an integer. This then allows the reference frequency to be increased, permitting a wider loop bandwidth while retaining fine resolution.

If you are designing off-chip, however, there is an older technique worth some research: the multiple loop synthesizer. Typically found in older signal generators, this technique sidesteps the compromises by using more than one loop. Here is an example:

Taking the same design requirement as before, we set up a (main) loop with a 1MHz reference but mix the 200MHz VCO output with a 50MHz signal from a second synthesizer loop before it reaches the divider as a (now) 150MHz signal.

Main loop divide ratio is 150, permitting a much wider bandwidth. The secondary loop uses a 500MHz VCO and a 250kHz reference frequency with a divider ratio of 2000 (still permitting a more relaxed loop filter). The 50MHz fed to the main loop mixer is the secondary VCO output divided by ten. Fine 25kHz steps are produced by changing the secondary loop by one (250kHz divided by ten), while if necessary, incrementing the main loop divider will provide coarse 1MHz steps.

Lacking the elegant simplicity of single-loop designs, multiple-loop synthesizers (of which my example is only one of many possible forms) do allow contradictory design requirements, such as low noise and vibration resistance, to be combined in the same system. ●

COMMUNICATIONS IN A LOW ENERGY INTERNET OF THINGS

By Heiner Tendyck, Principal Engineer for Solution Marketing and Strategic Business Planning at Toshiba Electronics Europe

Cut the Wires; Now Lower the Power

The Internet of Things (IoT) is developing quickly, creating an 'always on' interconnected world that requires low-cost, highly integrated smart devices capable of seamless intercommunication and low-power operation. Bluetooth® is proving a valuable solution in the IoT development scene thanks to advantages that range from certified interoperability to low design risk and rapid time-to-market. The emergence of Bluetooth Low Energy (BLE) has further strengthened the role that this technology can play in driving IoT designs forward.

Bluetooth Low Energy, now branded Bluetooth Smart by the Bluetooth SIG, satisfies important requirements for IoT connectivity. It combines advantages such as long communication range, ubiquity and low implementation costs, which are synonymous with Classic Bluetooth, yet has significantly lower power consumption thereby enabling applications to run for longer from a small and lightweight battery such as a coin cell. The Bluetooth SIG notes that analyst firms all over the world recognise Bluetooth Smart as a key enabler of the Internet of Things.

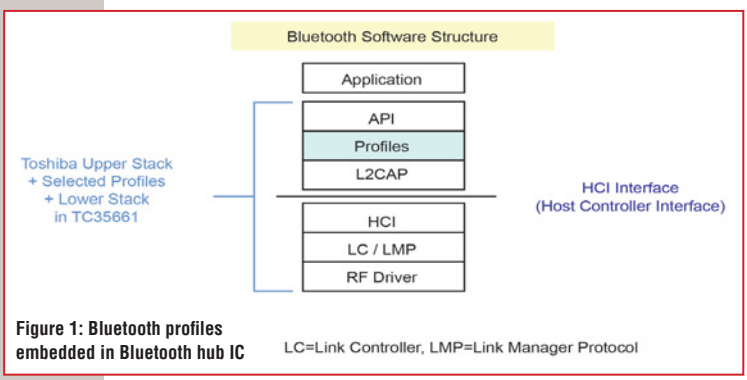


Figure 1: Bluetooth profiles embedded in Bluetooth hub IC

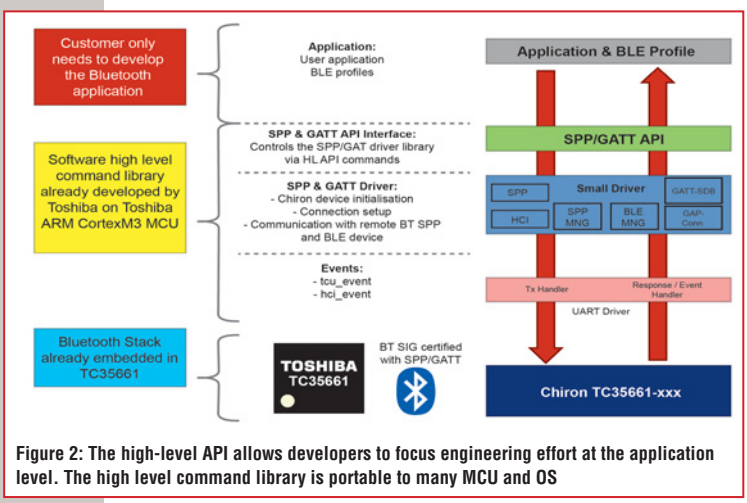


Figure 2: The high-level API allows developers to focus engineering effort at the application level. The high level command library is portable to many MCU and OS

Bluetooth Smart can be used in a number of ways to connect the "fingers" of the IoT to the Internet. Bluetooth Smart IoT devices such as sensors, for example, can communicate with Bluetooth Smart Ready smartphones, or PC dongles. Native support for Bluetooth Smart is already provided in popular desktop and mobile operating systems, such as Windows® 8, iOS, OSX and Android. The Bluetooth-enabled smartphone, often labelled Bluetooth Smart Ready, is widely recognised as a key part of the IoT-human interface. BT SIG makes sure that such labelled phones comply to the standard and are interoperable to other BLE nodes.

The extremely low power consumption intrinsic to Bluetooth Smart now opens up many new opportunities to create different types of hubs for use in homes, in-car, in industrial scenarios, or in medical applications. Home automation is expected to be the fastest growing market for Bluetooth Smart technology over the coming years, and is likely to encourage integration of Bluetooth Smart technology into gateways such as routers or set-top boxes thereby enabling continuous remote monitoring and control of various nodes around the house. These may include door locks, ambient-light sensors, thermostats, switches and other devices to be controlled by a simple mobile or home gateway.

The maximum specified transmit power of +4dBm is enough to give Bluetooth Smart devices a communication range of up to 50 metres. This gives designers great flexibility to take advantage of Bluetooth for industrial sensing, such as collecting data from machines installed on a factory floor or from equipment such as autonomous vehicles used to monitor conditions in environments that are inaccessible or dangerous to human health. End users in industry may connect to Bluetooth-enabled equipment using a range of devices including Bluetooth-enabled PCs, smartphones, or dedicated sensor hubs.

Bluetooth Smart also has numerous potential automotive applications. These include low-power remote controls as well as improved keyless entry systems as well as many connected applications around the vehicle such as monitoring the driver's health and ability to control the vehicle.

Bluetooth Smart is a good fit with the IoT applications that have been envisaged so far, as these often need to send short bursts of data at infrequent intervals. A Bluetooth Smart device can wake from deep sleep, send data, and return to deep sleep in three milliseconds. The same cycle can take up to 20 milliseconds in Bluetooth Classic. BLE also enables connection set up within 100msec, compared to several seconds in BT classic. Smaller packet size and fewer RF channels also contribute to savings in power consumption compared to Classic Bluetooth. The over-the-air data rate of 200-300kbps provides plenty of speed to transmit IoT messages quickly allowing the application to return rapidly to deep sleep.

Building Bluetooth Low-Energy Applications

A Bluetooth device may be expected to connect with Classic Bluetooth as well as Bluetooth Smart devices ("Dual Mode"). This type of device is known as Smart Ready, and has built-in support for both standards. A dual-mode IC such as Toshiba's TC35661 Bluetooth Dual Mode single-chip LSI is suitable for this type of application.

The TC35661 has a low-power architecture and is fabricated using a power-efficient 65nm RFCMOS process. It can operate with a serial connection to a host MCU (in Dual Mode) or in stand-alone mode (single profile mode). In single profile mode, the upper stack including API, selected profiles and L2CAP as well as the HCI, Link Controller (LC), Link Manager Protocol (LMP) and RF drivers are embedded on the TC35661, as illustrated in figure 1. In this case the embedded stack and protocols are pre-certified, which enables developers to avoid the cost and time overheads associated with Bluetooth certification process.

Running in Dual Mode the device is managed by an external host processor across a serial UART interface and the embedded API. Toshiba offers driver software for these external hosts featuring high-level abstracted APIs e.g. for SPP or BLE GATT to enable dual mode functionality and take care of device initialisation, connection setup and communication with remote devices. Figure 2 illustrates how this high-level API helps to minimize development effort.

Bluetooth Smart-Compliant Integration

The Toshiba TC35667 is an ARM-based Bluetooth Smart Compliant IC created for use in Bluetooth Smart hubs or Bluetooth Smart devices such as sensors capable of connecting to a Smart or Smart ready hub. It integrates a complete Bluetooth 4.0 (BLE) modem and RF block, and has ultra low-power consumption with peak current 5.9mA (typical) in transmit mode, and deep-sleep power consumption of 0.1µA typical. The Generic Attributes (GATT) profile and Generic Access Profile (GAP) that allow Bluetooth devices to accomplish basic interactions smoothly are built-in. The user application can reside in the 32KByte programming area in the external EEPROM and are bootloaded from there.

The GATT profile supports Bluetooth Smart central and peripheral modes, allowing the TC35667 to interact with a host microcontroller when used in a hub application, or to perform in standalone mode when used as a device such as a sensor. Figures 3 and 4 show how the device can be used in standalone mode with minimal external components, or combined with a host microcontroller in a hub application.

Starter kits are available to help accelerate development of new Bluetooth Smart and Smart Ready applications, including IoT applications, using the TC35661 or TC35667.

Custom Profile Support

As the Internet of Things continues to evolve, new applications are expected to emerge that will require new profiles. A variety of BT SIG BLE profiles suitable for industrial, medical and automotive applications are already specified by the Bluetooth SIG and can be provided by Toshiba, including the Blood Pressure Profile, Heart-Rate Profile, Thermometer, Location and Navigation Profile and Proximity Profile. Toshiba has also created a proprietary SPP over BLE Profile which is not part of the BT SIG BLE profile set. Toshiba's high-level

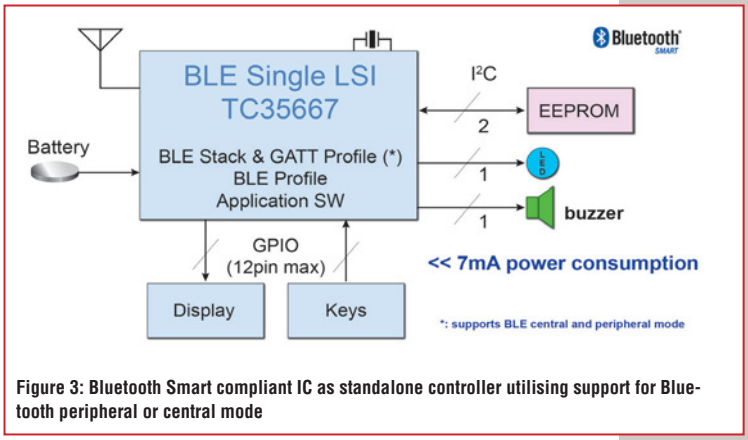


Figure 3: Bluetooth Smart compliant IC as standalone controller utilising support for Bluetooth peripheral or central mode

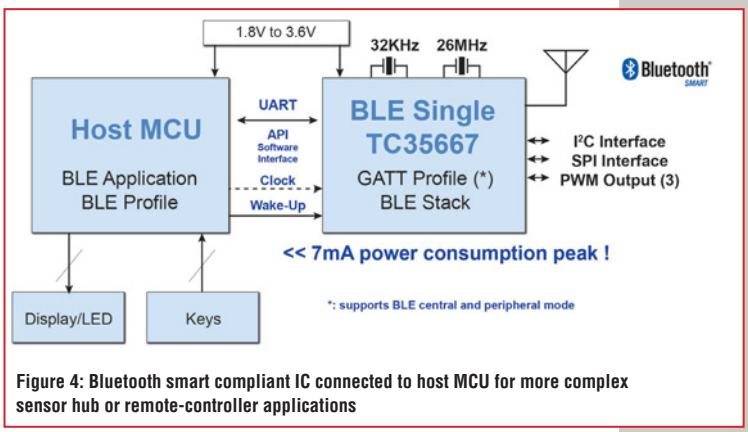


Figure 4: Bluetooth smart compliant IC connected to host MCU for more complex sensor hub or remote-controller applications

API not only helps implementing existing profiles but also simplifies development of new proprietary profiles thereby maximizing flexibility to create more advanced IoT applications in the future and differentiate against other system solutions.

The Future: Enhancing Usability

The Bluetooth Smart Compliant IC functionality can be further extended to help simplify the set-up of IoT applications by integrating circuitry to operate a low-power NFC (Near-Field Communication) tag. Adding NFC functionality enables devices to be paired simply by touching. Devices can also take advantage of the NFC link to exchange small quantities of data, reducing system power consumption further below BLE level. Toshiba is currently finalising an NFC-Forum compliant Bluetooth/NFC Combo IC, which is pin-compatible with the TC35667 single-Bluetooth IC and includes features ensuring low power consumption, rapid wake-up from standby, and smooth handovers between NFC and Bluetooth communication.

Conclusion

By offering low power consumption, low cost and convenient ease of use, the Bluetooth Smart standard has quickly become recognized as a major enabling technology of the Internet of Things. IoT applications and markets are evolving quickly, and engineers need a combination of ultra low-power ICs and software and development support to ease integration, accelerate design and provide the flexibility to adapt and customise for the future.

www.toshiba.com

SPICE DIFFERENTIATION

IN THIS ARTICLE **MIKE ENGELHARDT**, MANAGER OF SIMULATION DEVELOPMENT AT LINEAR TECHNOLOGY, GIVES US HIS VIEW ON WHY LTSPICE YIELDS BETTER RESULTS IN ANALOG DESIGN THAN OTHER SPICE IMPLEMENTATIONS

Analog design engineers lean heavily on simulation to predict circuit performance. The value of a simulator depends on how well it can predict physical reality and how quickly it can produce results. Discrepancy between simulated and real performance can send a product into costly iterative debugging cycles.

SPICE is used for analog circuit simulation because it can compute the full large-signal behaviour of arbitrary circuits. Three numerical methods used in SPICE account for its success in analog circuit simulation:

- Newton iteration to find the solution of circuits with nonlinear elements;
- Sparse matrix methods to corral huge matrices into the address space of a practical computer;
- Implicit integration to integrate the differential equations that arise from circuit reactances.

The ability of a SPICE simulator to reliably produce correct results depends on how well these methods are implemented.

Newton Iteration

Newton iteration involves expanding each nonlinear circuit device's I-V curve as a Taylor series but keeping only the first two terms and solving the resultant system of simultaneous linear equations. If the solution of the linear system is indeed the very point about which the Taylor series was expanded, then, because the Taylor approximation is exact at that point and accurate near it, the solution of this linear system is in fact the correct solution to the original nonlinear circuit; otherwise the solution of the linear system is used as an iteration step, with the original nonlinear circuit re-expanded as a new Taylor series about this solution, again keeping only the first two terms; and then solving the resultant system of simultaneous linear equations.

The process repeats until a proof that the correct solution has been found is successful. Success of the convergence of Newton iteration results in finding a numerical proof that the correct solution of your circuit was found.

Robustness of Newton iteration depends on: (1) having all circuit element I-V curves continuous in value and slope; and (2) all non-linear elements being bypassed with capacitance so the previous time-step solution is a good starting point for the Newton iteration of the current time point. Conditions (1) and (2) are met by any physical circuit, but SPICE programs usually don't get this right because the semiconducting devices in Berkeley SPICE have discontinuities and these implementation errors have spilled over to pay-for SPICE implementations. These discontinuities do not occur in LTspice. To illustrate, Figure 1 shows the I-V curve of a diode in PSpice versus LTspice. The netlist used in each case is:

```
* I-V discontinuity in PSpice Diode
V1 N001 0 0
D1 N001 0 D
.dc V1 -.3 -.2 2u
.probe
.model D D(Is=10n)
.end
```

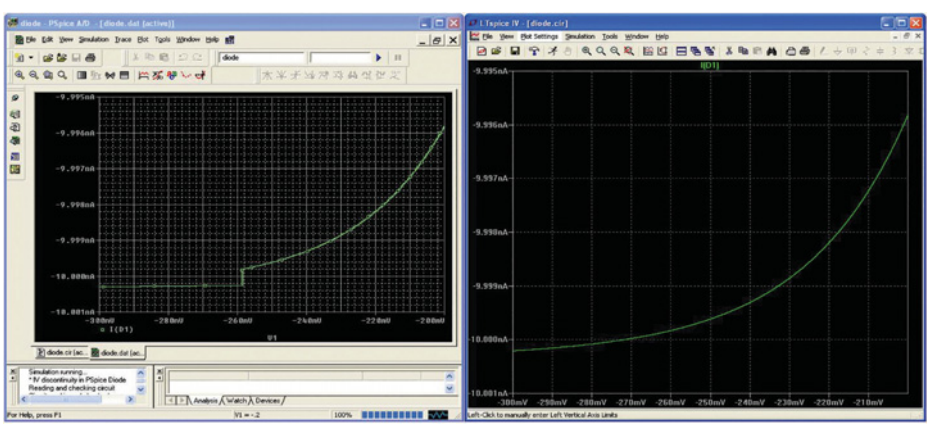


Figure 1: Discontinuity in PSpice (left) diode I-V curve versus continuous diode I-V curve in LTspice (right). Discontinuities negatively impact a simulator's ability to solve non-linear circuits

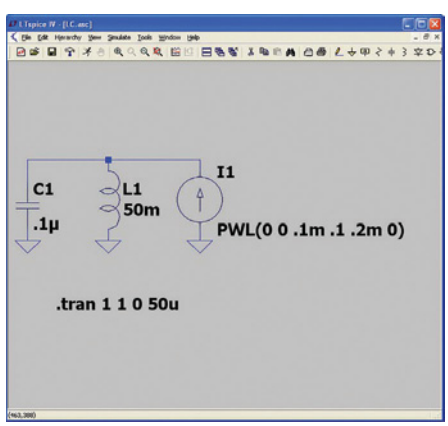


Figure 2: Simple circuit with solution known by inspection

The PSpice diode I-V curve is discontinuous in both value and slope. Such discontinuities exist in most semiconducting devices in PSpice but in none of the semiconducting devices in LTspice.

Sparse Matrix Methods

The Taylor series is multidimensional – one dimension for each unknown voltage node in the circuit. For an analog IC this can be 100,000 distinct voltage nodes, leading to a conductivity matrix of 100,000 by 100,000, or 80 billion bytes for double precision matrix coefficients. Even today's 64-bit processors don't bond out enough address lines to access that much memory. Fortunately, almost every coefficient is zero, so they don't need to be stored. Sparse matrix methods keep track of only the non-zero elements, which allows a huge matrix to be solved in a comparatively tiny address space.

The sparsity of the matrix arises from the physical nature of practical circuits. Most nodes are only connected to a few other nodes. For example, even if you write the conductivity matrix of a circuit that looks like a fishnet grid of resistors, the matrix is almost diagonal because each node is resistively connected only to adjacent nodes. Practical circuits aren't as dense with connections as fishnets are with knots. The sparsity of a large analog circuit is in the parts-per-million range. This sparsity is what allows the matrix to be solved in a present-day computer. Newton iteration of analog circuits is not possible without sparse matrix methods.

The greatest similarity across SPICE implementations is in these sparse matrix methods. All SPICE programs use LU (Lower Upper) factorization. Most SPICE implementations use a sparse matrix library derived from the code distributed with the academic Berkeley SPICE code, but some, usually marketed as a fast SPICE, try to improve on it by using an enhanced sparse matrix library such as SuperLU; the sparser the matrix, the more closely it can be written as a diagonal, i.e. solved, matrix. Since analog circuit matrices are so sparse, improving LU factorization with SuperLU does not give as much speed advantage as one might hope.

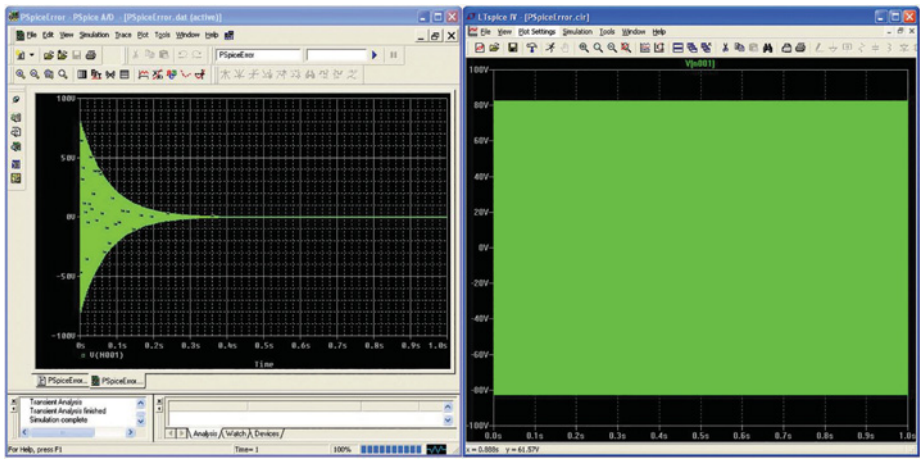


Figure 3: PSpice (left), utilizing modified Gear numerical integration, incorrectly artificially dampens ringing in the circuit of Figure 2. LTspice (right) produces the correct result

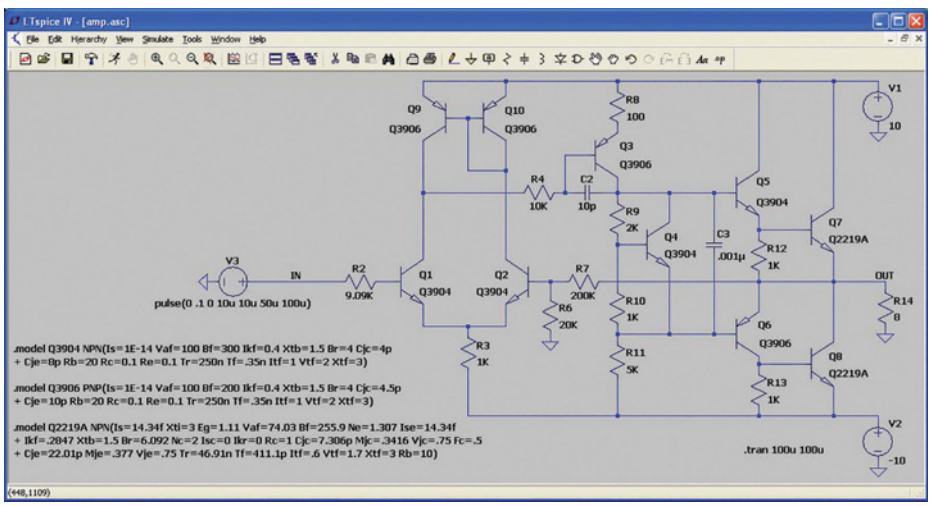


Figure 4: Unstable power amplifier

A better approach is to simply get the processor to do the math at the theoretical FLOP (floating-point operation) limit of the underlying hardware. The issue here is that it takes longer to get the numerical data to the FPU (floating-point unit) than it does to actually perform the FLOP.

The FPU pipeline usually runs empty. Ultimately, this is a consequence of the fact that all operating systems use dynamic memory allocation. At the time the simulator is written and compiled, the memory location storing the matrix data isn't known. At run-time the simulator requests memory with function call malloc(), which returns an address where the simulator is allowed to safely store matrix data. Since it isn't possible to give each matrix element its own name, arrays are used. This means the simulator asks for fewer but larger pieces of memory, and the individual coefficients are indexed off the base address returned by malloc().

Resolving this address at run-time and fetching the data pointed to by that address into the FPU takes longer than executing the FLOP itself. Eliminating the unknowns of a matrix involves mostly

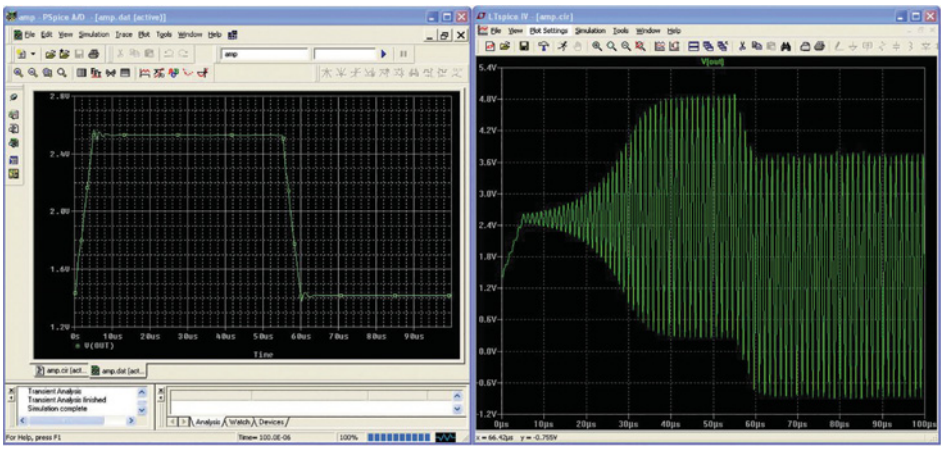


Figure 5: Simulated output from an unstable power amplifier in the face of a large signal transient. PSpice (left) incorrectly indicates the circuit as stable, while LTspice (right) correctly reveals the instability

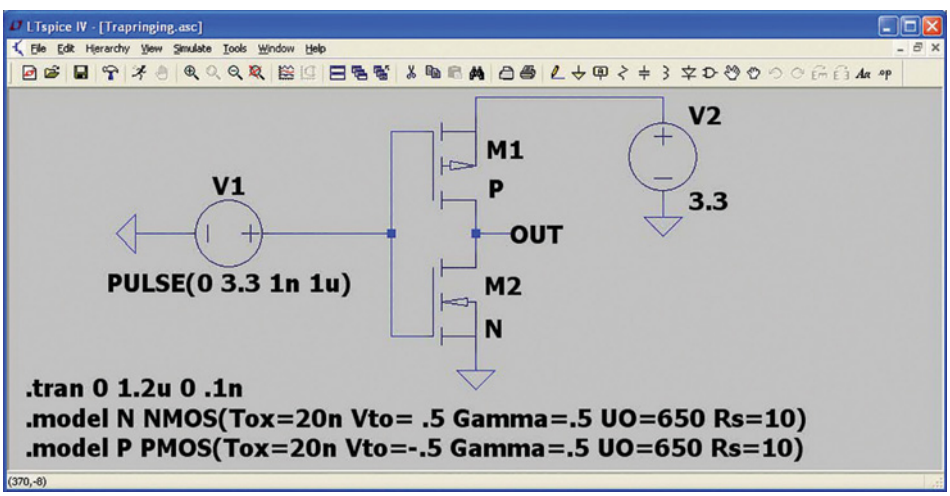


Figure 6: Circuit prone to trap ringing

addition, subtraction and multiplication, instructions costing only three latent clock cycles. There are also some divisions which cost much more than three clocks, but there's only one division per unknown to be eliminated. Fetching data that is only known by the address of the address of the base address of which one indexes takes much longer than three clock cycles.

Ideally, the addresses of the data required for a calculation would be known ahead of calculation time so that data can be efficiently fetched and the FPU doesn't have to wait for it.

LTspice eliminates the overhead in getting the data to the FPU with self-authoring assembly language source written at run-time, after matrix memory has been allocated and the addresses returned from malloc() are known. This late-authored code can resolve concrete matrix element addresses in line with the code so data can be efficiently loaded, allowing the FPU to operate with the pipeline full, once the code is assembled and linked with LTspice's built-in assembler and linker. LTspice is unique in implementing a self-authoring, self-assembling and self-linking sparse matrix solver. The method performs remarkably better than any other technique.

Implicit Integration

Analog circuit simulation requires numerical integration of differential equations to track the behaviour of the capacitances and inductances. This is where the largest differences between one SPICE implementation and another are mostly seen: the method(s) available for integrating differential equations.

Numerical integration involves error. Analog circuit simulation entails integrating the behaviour of many time constants. The nature of integrating differential equations that have solutions that look like exp(-const*time) is that the errors will in fact add up to infinity, unless a numerical method called implicit integration is used. On this, literature points out the numerical solution is not singular if a small enough time-step is guaranteed, but in practice, an approach with explicit integration and limited time-step size doesn't work unless you can numerically integrate with infinite precision. The error doesn't add up to infinity because of round-off error but because of approximating the derivative with sampled finite differences. There are no successful general analog circuit simulators that use explicit integration. Without implicit integration, transient analysis would not be possible in SPICE.

SPICE uses second-order integration. Most SPICE implementations follow Berkeley SPICE and provide two forms of second-order implicit integration: Gear and trapezoidal (trap). (SPICE occasionally drops to first-order integration; e.g. if an event with a known discontinuous first-order time derivative occurs, such as at the transition between two straight-line segments of a piecewise linear or pulse function of an independent voltage or current source, most SPICE implementations drop to first-order integration for that circuit's reactances at the transition. The first-order version of Gear and trap are both backward Euler.)

Trap integration is both faster and more accurate than Gear, but trap integration can give rise to a numerical artifact where the integrated discrete time-step solution oscillates between time

steps about the true continuous-time behaviour, which can cause the user to be suspicious of the correctness of the simulator, even though each trapezoid contains the correct integrated area.

Trap ringing has been feared to be so unacceptable to analog circuit designers that trap integration has been eliminated from one commercial SPICE implementation, PSpice, leaving the slower and less accurate Gear integration as the only available option. Some users are predisposed to be suspicious of SPICE because of popular literature denigrating the value of SPICE simulation. However, Gear integration doesn't just dampen numerical ringing, it dampens all ringing, even physical ringing, making it possible for a circuit that malfunctions in real life due to an oscillation to simulate as perfectly stable and functional because the instability was damped out of numerical existence. This has lead to disastrous situations where an IC design is simulated in PSpice, laid out and fabricated only to find that the circuit doesn't function due to an instability that PSpice's Gear integration missed. A mask revision cycle – at considerable expense in time and treasure – is required to remove the instability to try to achieve initial functionality.

In principle, Gear integration error could be reduced by having the IC designer stipulate a small maximum time step, but this is not a viable solution because: (1) small time-steps slow simulation speed to a crawl; and (2) there's no way to ensure that the time step is small enough anyway.

PSpice's documentation states that it uses a modified Gear method and it does indeed seem better at picking a small enough time step to reduce the error than the Gear integration implementation in Berkeley SPICE.

But, PSpice's method often fails. It's easy to compose a trivial circuit and see the PSpice numerically-integrated result deviate dramatically from the true solution than can be found by inspection. Consider Figure 2, which shows a parallel tank circuit with a parallel piecewise linear current source. The current source asserts a spike of current over the first 0.2ms and is zero thereafter. The solution should be that the tank circuit resonance is excited by the spike of current and thereafter ring at constant amplitude.

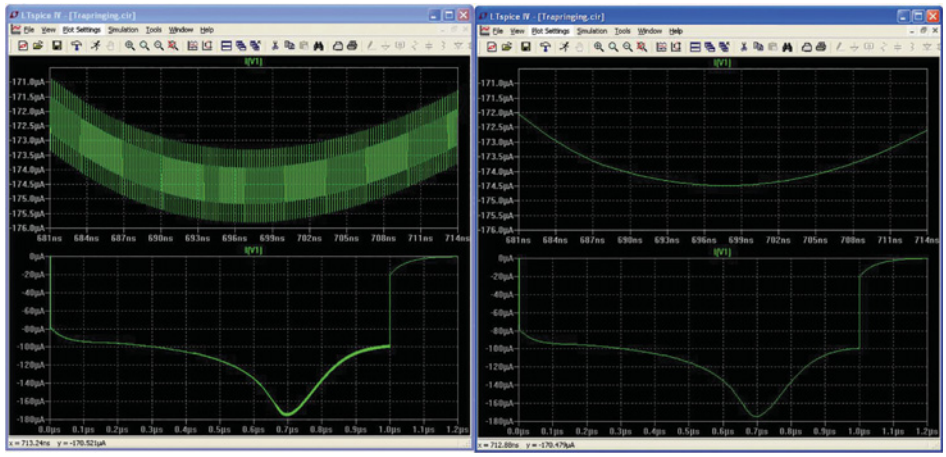


Figure 7: Trap verses LTspice modified trap integration applied to the circuit in Figure 6. Conventional trap integration (left) exhibits trap ringing while the ringing is eliminated with LTspice modified trap (right)

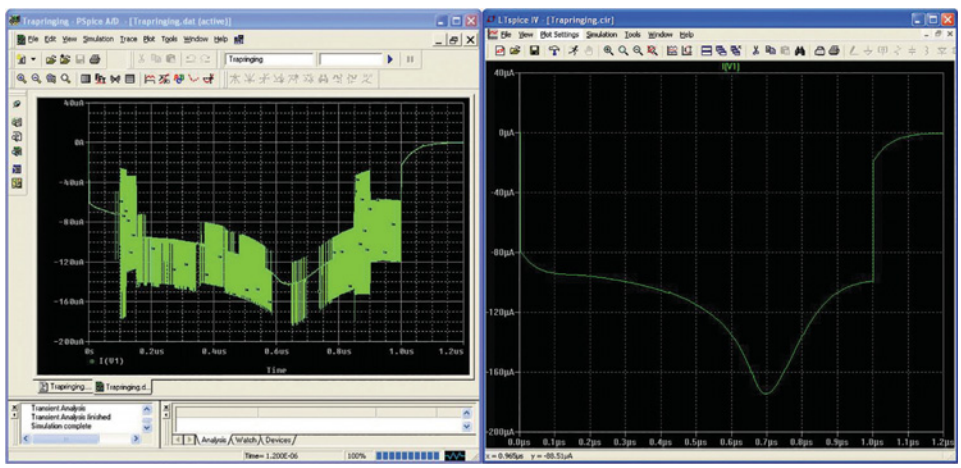


Figure 8: The trap ringing example circuit of Figure 6 run in PSpice (left) does not exhibit trap ringing, but produces other artifacts most likely due to an error in the implementation of the Yang-Chatterjee charge model. LTspice (right) produces the correct result

The netlist of the circuit is given by:

```
* Gear (PSpice) integration error
L1 N001 0 50m
I1 0 N001 PWL(0 0 .1m .1 .2m 0)
C1 N001 0 .1u
.tran 1 1 0 50u
.probe
.end
```

Figure 3 shows that PSpice's modified Gear integration artificially dampens the ringing, whereas LTspice immediately yields the correct solution. The error in PSpice can be reduced by stipulating a smaller maximum time-step (fourth number in the .tran statement). This should be a simple circuit for PSpice's modified Gear to figure out. However, a circuit with many different time constants is basically impossible for PSpice to solve reliably without the engineer manually inspecting how the "solution" converges as one stipulates ever smaller maximum time steps.

Figure 2 shows clearly that PSpice Gear

integration doesn't correctly integrate the two reactances of a trivial circuit with only one node. The nature of the error of Gear integration is to make circuits look more stable in simulation than they actually are in real life. To put the consequences of this error into the perspective of a practical example, Figure 4 shows an audio power amplifier that isn't stable because compensation capacitor C2 is too small. PSpice incorrectly simulates this circuit as stable, whereas LTspice gives the correct result. The netlist used in each case is:

```
* Unstable Power Amplifier
Q5 N001 N006 N007 0 Q3904
Q7 N001 N007 OUT 0 Q2219A
Q8 OUT N013 N014 0 Q2219A
Q6 N013 N012 OUT 0 Q3906
V1 N001 0 10
V2 N014 0 -10
R11 N012 N014 5K
R14 OUT 0 8
R9 N006 N008 2K
R10 N008 N012 1K
Q4 N006 N008 N012 0 Q3904
Q1 N005 N009 N011 0 Q3904
Q2 N002 N010 N011 0 Q3904
R3 N011 N014 1K
Q3 N006 N004 N003 0 Q3906
R6 N010 0 20K
R7 OUT N010 200K
V3 IN 0 pulse(0 .1 0 5u 5u 50u 100u)
R8 N001 N003 100
R4 N004 N005 10K
C2 N006 N004 10p
R13 N013 N014 1K
R12 N007 OUT 1K
C3 N006 N012 .001u
Q9 N005 N002 N001 0 Q3906
Q10 N002 N002 N001 0 Q3906
R2 IN N009 9.09K
.tran 100u 100u
.model Q3904 NPN(Is=1E-14 Vaf=100
Bf=300 Ikf=0.4 Xtb=1.5
+ Br=4 Cjc=4p Cje=8p Rb=20 Rc=0.1
Re=0.1 Tr=250n Tf=.35n
+ Itf=1 Vtf=2 Xtf=3)
.model Q3906 PNP(Is=1E-14 Vaf=100
Bf=200 Ikf=0.4 Xtb=1.5
+ Br=4 Cjc=4.5p Cje=10p Rb=20 Rc=0.1
Re=0.1 Tr=250n
+ Tf=.35n Itf=1 Vtf=2 Xtf=3)
.model Q2219A NPN(Is=14.34f Xti=3
Eg=1.11 Vaf=74.03
+ Bf=255.9 Ne=1.307 Ise=14.34f
Ikf=.2847 Xtb=1.5
+ Br=6.092 Nc=2 Isc=0 Ikr=0 Rc=1
Cjc=7.306p Mjc=.3416
+ Vjc=.75 Fc=.5 Cje=22.01p Mje=.377
Vje=.75 Tr=46.91n
+ Tf=411.1p Itf=.6 Vtf=1.7 Xtf=3 Rb=10)
.probe
.end
```

Figure 5 compares PSpice's erroneously stable result (left) with the correct, oscillating result from LTspice (right). The simulation is a large signal transient. If a small enough time-step is stipulated in the PSpice simulation, you can force it to approach the correct LTspice solution, suggesting that while PSpice is interpreting the device equations of the transistors correctly, it just isn't accurately integrating the differential equations.

What is needed is a method with the speed and accuracy of trap but without the ringing artifact.

Another approach is to use a de-tuned version of trap integration so it will damp trap ringing but only introduce a hopefully acceptably small error in the true circuit behaviour. It is actually possible – but not recommended – to de-tune LTspice's trap integration with the undocumented option called trapdamp, by adding the SPICE directive .options trapdamp=.01 to your schematic. You might be able to find a value of trapdamp that duplicates the integration behaviour of HSPICE. Nevertheless, I do not recommend using this option because it dampens real circuit behaviour and isn't necessary in LTspice, which uses a better method of eliminating trap ringing.

Speed And Accuracy Without Ringing

LTspice uses an integration method modified trap that has the speed and accuracy of trap but without the ringing artifact. Modified trap is a method I invented some years ago and made widely available first in LTspice. To the best of my knowledge, it is the best means to integrate the differential equations of an analog circuit and is not duplicated in any other SPICE program. It is the only method I recommend for circuit design. LTspice does also support the use of the other known methods, trap and Gear, but simply so that a user can duplicate the erroneous results from other SPICE simulators to verify that the models are interpreted the same, and only the integration method is different.

Modified trap was used by LTspice to produce Figure 3. Note that there is no change in ringing amplitude even after thousands of cycles. This demonstrates that LTspice modified trap does not introduce artificial numerical damping. Modified trap is also used by LTspice to produce Figure 5, where LTspice correctly exposes the amplifier's instability.

To demonstrate the ability of LTspice modified trap to eliminate trap ringing, we need a circuit that is prone to trap ringing. Trap ringing is initiated when discrete time-step second-order integration has trouble representing the exact continuous-time circuit behaviour. It can be reduced or eliminated with judicious use of time-step and integration-order control.

Since LTspice has been the most popular SPICE program for the last 10 years, it has seen a lot of circuits and there is a lot of knowledge accrued in libraries for the solver to avoid trap ringing, so one has to work a little harder to find a counter-example.

Figure 6 shows a circuit that causes trap ringing due to the highly nonlinear capacitance of the gates of an unusually dimensioned MOSFET inverter. Trap ringing is visible in the gate current drive, I(V1).

Figure 7 compares trap integration to LTspice modified trap. The top plot shows a zoomed in region of the bottom plot to clearly show the ringing. If you would like to reproduce this result in LTspice, go to the SPICE pane of the control panel and select trapezoidal integration instead of the default, modified trap. The netlist for this simulation is:

```
* Trap Ringing Example
V2 N001 0 3.3
V1 N002 0 PULSE(0 3.3 1n 1u)
M1 OUT N002 N001 N001 P
M2 OUT N002 0 0 N
.tran 0 1.2u 0 .1n
.model N NMOS(Tox=20n Vto= .5
Gamma=.5 UO=650 Rs=10)
.model P PMOS(Tox=20n Vto=-.5
Gamma=.5 UO=650 Rs=10)
.probe
.end
```

Note that most SPICE programs won't run this deck as intended because they use the Meyer capacitance model for this type of MOSFET. Because the Meyer capacitance model doesn't conserve charge and is inaccurate for short channels, it fell into obsolescence in the 1990s.

Both LTspice and PSpice have replaced the Meyer capacitance model with the Yang-Chatterjee charge model. Since both simulators use the same updated charge storage equations, they should give the same results. But when we compare the PSpice simulation to LTspice, as shown in Figure 8, PSpice shows remarkably erroneous results. The oscillations visible in the PSpice simulation, though, are not trap ringing because the oscillation isn't from time-step to time-step and PSpice doesn't use trap. This artifact is almost certainly due to an error in differentiating the Yang-Chatterjee charge equations to capacitances in the PSpice Yang-Chatterjee charge model implementation.

Solving Circuit Behaviour

LTspice was not the first SPICE implementation, nor is it the only free SPICE, but it is the best and most widely used SPICE implementation.

Newton iteration, sparse matrix methods and implicit integration are the core numerical methods of SPICE. The simulator's robustness, speed and integrity hinge on how well these methods are implemented. In the end, a SPICE simulator needs to earn designers' confidence in correctly solving circuit behaviour. This is impossible if the solver doesn't perform the core numerical methods correctly. LTspice performs these methods correctly and better than any other SPICE implementation. ●

LTSPICE

LTspice is downloaded four times per minute and is the topic of the largest users' group of any simulator. Using distribution and use-figures of other SPICE implementations based on private communication with representatives from the respective companies that sell those other SPICE programs, LTspice is distributed and used three orders of magnitude more than any other SPICE program.

QUADRATURE VOLTAGE CONTROLLED OSCILLATOR FOR L-BAND WIRELESS APPLICATIONS

JINGRU SUN AND **CHUNHUA WANG** DISCUSS A NEW SINGLE-CURRENT DIFFERENCING QUADRATURE VOLTAGE CONTROLLED OSCILLATOR FOR L-BAND WIRELESS APPLICATIONS, BASED ON A TRANSCONDUCTANCE AMPLIFIER AND 0.18-MICRON RF CMOS TECHNOLOGY

The current-mode approach has become popular in analog integrated circuit design due to its advantages such as wider dynamic range and bandwidth and lower power consumption over its voltage-mode counterparts and various active current mode blocks, including Compound Current Conveyors (CCII), Operational Transconductance Amplifiers (OTA), Current Differencing Buffered Amplifiers (CDBA) and Current Differencing Transconductance Amplifiers (CDTA).

The current-mode method is actually a modular design method. Current-mode quadrature oscillators (QOs) consist of two integrator loop quadrature oscillators (second-order QO) and three or more integrator loop quadrature oscillators (ring QO). All these QOs are completely inductorless, and the current-mode theory of designing oscillators is well established. However, the frequency limit of these existing current-mode QOs is very low (no more than 100MHz), so they can't meet the demands of modern communication systems.

Choices

Several RF ring oscillators exist, using connected phase delay stages forming a loop, but they can't provide quadrature sinusoidal output waveforms. Actually, in current-mode circuit design, we call the phase delay stage for lossy integrator or first-order lowpass filter. Not only the first-order lowpass filter, but also the first-order allpass, highpass and bandpass filters can realize the phase delay stages, and these blocks are easy to deal with thanks to the modular current-mode design method. This approach will also make the RF oscillators' design easier and more convenient.

The current-mode modular design method is particularly tempting in designing quadrature second-order and ring RF oscillators. A 1.45GHz Quadrature Voltage-Controlled Oscillator (QVCO) for L-band (1-2GHz) applications using single CDTA is discussed here to explain the convenience of applying the current-mode method to RF oscillator design. This QVCO works at 1.45GHz, and the tuning range is about 145MHz by changing the bias voltage.

The QVCO consists of a CDTA, a resistor and two capacitors and, because there is no need for inductance, its chip area is only about 0.26 × 0.35mm² including the test pads.

Circuit Description

Figure 1 is the symbol and ideal model of CDTA. Equation 1 presents the terminal relations of CDTA:

$$\begin{aligned} v_p &= v_n = 0 \\ i_z &= i_p - i_n \\ i_x &= g_m v_z = g_m Z_z i_z \end{aligned} \qquad (1)$$

Figure 2 is the CMOS CDTA used for this article. In order to use

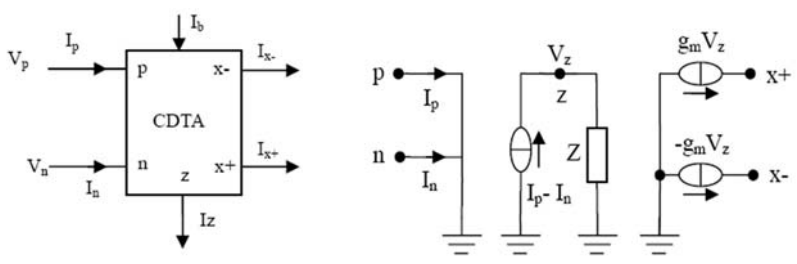


Figure 1: Symbol and ideal model for CDTA

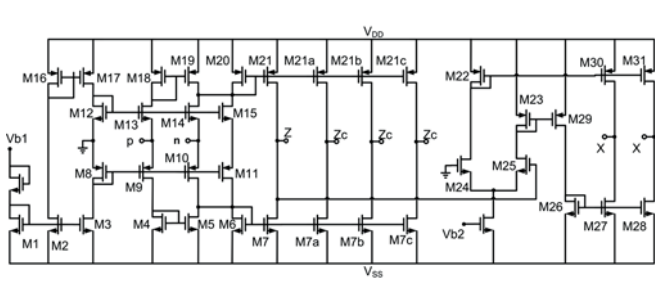


Figure 2: Figure 2 CMOS-based CDTA in this work

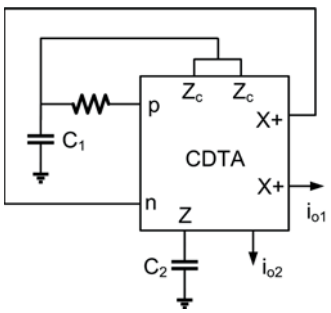


Figure 3: Proposed current-mode QVCO

the current from terminal Z, an auxiliary Z_c terminal is added in Figure 2 to copy the current.

The proposed single CDTA-based QVCO, which consists of three passive elements and only one CDTA, is shown in Figure 3. Using Equation 1, it is easy to get the characteristic equation of the QVCO in Figure 3, and it can be expressed as:

$$s^2 + \left(\frac{g_m}{C_2} - \frac{1}{R_1 C_1}\right)s + \frac{g_m}{R_1 C_1 C_2} = 0 \qquad (2)$$

From Equation 2, the condition of oscillation (CO) and frequency of oscillation (FO) of the two QOs can be expressed as:

$$\frac{g_m}{C_2} = \frac{1}{R_1 C_1} \qquad (3)$$

$$\omega_o = \sqrt{\frac{g_m}{R_1 C_1 C_2}} \qquad (4)$$

From Figure 3, the current transfer function between i_{o1} and i_{o2} is:

$$\frac{i_{o1}(s)}{i_{o2}(s)} = \frac{g_m}{sC_2} = \frac{i_{o1}(j\omega)}{i_{o2}(j\omega)} = \frac{g_m}{\omega C_2} e^{-j90^0} \qquad (5)$$

From Equation 5 we can determine that the phase difference between i_{o1} and i_{o2} is 900, and the two outputs are quadrature.

Post-Layout Simulation Results

The suggested QVCO is realized using Cadence IC Design Tools 5.1.41 Spectre RF simulator with standard 0.18µm RF CMOS technology. The chip layout design strictly obeys the Chartered Design Rule (YI-093-DR001_Rev1V_1.8V-3.3V) and Chartered Spice Model spec (yi093dr001_1v_00_20090731a), and is designed as symmetrically as possible to minimize mismatch in the signal paths.

In the post-layout simulation, the supply voltage is ±1.8V, the bias voltages V_b = 1.2V and V_{ctrl} = -0.63V, the capacitors are C_1 = 2.5pF, C_2 = 1pF, and the resistor is R_1 = 20kΩ.

Figure 4 is the transient response of V_{o1} and V_{o2} during the initial state with 50Ω load resistors; it is clear that the starting time of the QVCO is about 25ns. Figure 5 shows the quadrature outputs of V_{o1} and V_{o2} from 32-36ns. From the markers M_0 and M_1, we can see that the period of the QVCO is about 0.69ns, and

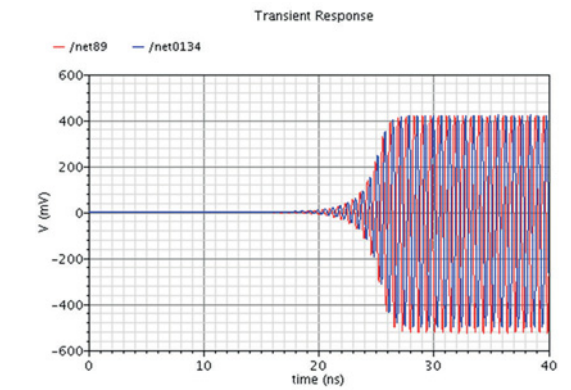


Figure 4: The transient response of V_{o1} and V_{o2} during initial state

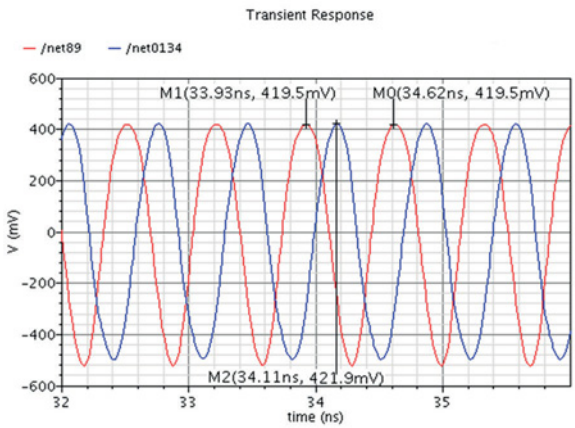


Figure 5: Figure 5 The quadrature outputs of V_{o1} and V_{o2} with 50Ω load resistors

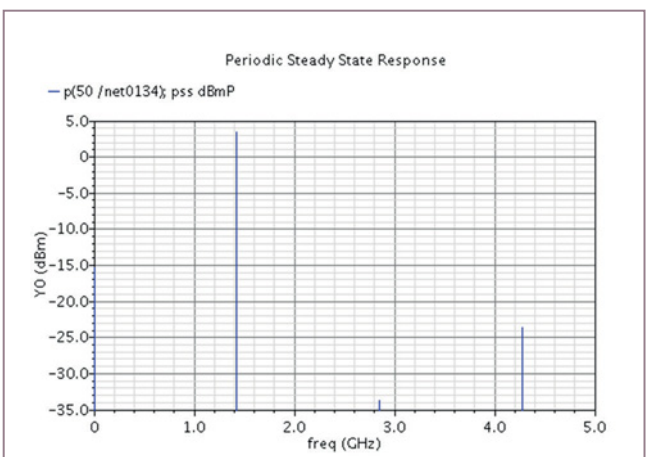


Figure 6: The harmonic balance simulation result of V_{o2}

the frequency is about 1.45GHz.

From the markers M_1 and M_2, it can be determined that the phase difference between V_{o1} and V_{o2} is about 93°, and V_{o1} and V_{o2} are almost quadrature.

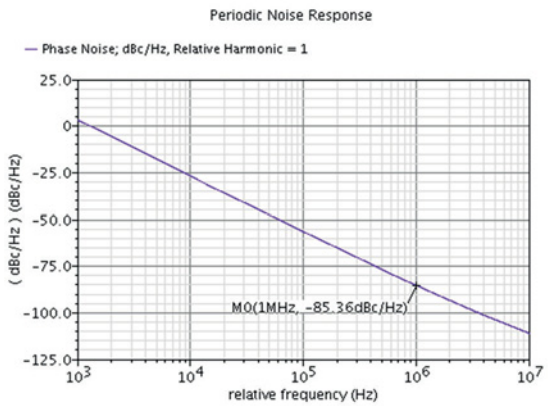


Figure 7: The phase noise of the QVCO

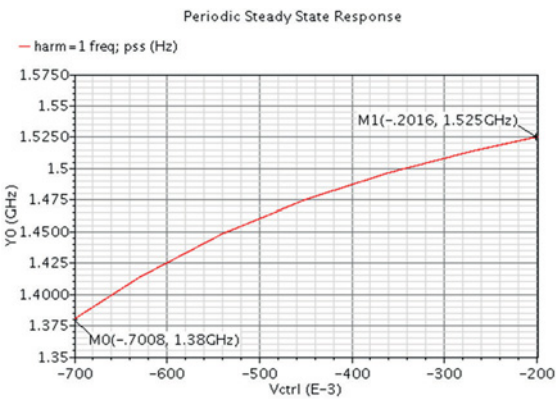


Figure 8: The output frequency versus the control voltage of the QVCO

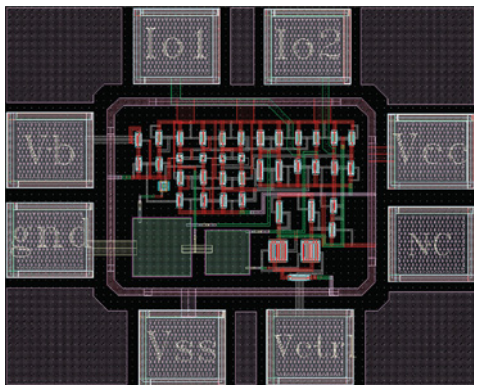


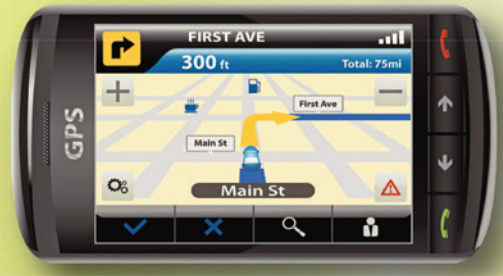
Figure 9: The layout diagram of the QVCO (0.26-0.35mm²)

Figure 6 is the harmonic balance post-layout simulation result of V_{o2}. It is noted here that the output power of V_{o2} is concentrated at 1.45GHz, and the output power of the other harmonic signals are relatively small. Figure 7 is the phase noise of the QVCO. The phase noise of the QVCO at 1MHz offset is -85.36dBc/Hz when the carrier is 1.45GHz.

Figure 8 is the output frequency versus the control voltage of the QVCO. From this figure it is clear that the output frequency tuning range of the QVCO is about 145MHz when the control voltage changes from -0.7V to -0.2V.

The layout of the proposed QVCO is shown in Figure 9. ●

If you take one of these out with you!



You might need one of these!

Model PAG14AH4 portable rechargeable lithium polymer USB standby battery charger keeps all your mobile electronic devices fully charged wherever you are! Get up to 7 or 8x the standby and talk time for typical mobile smart phone and a full charge or two for a tablet PC!

Features

- **Powerful 14,400mAh lithium polymer battery**
- **Dual 5V USB outputs can charge any mobile device that uses USB charging technology**
- **Micro USB charging input can be recharged using your standard mobile or tablet USB charger or any USB charging outlet**
- **Simple operation touch pad controls with LED charge indicator**
- **Lightweight and very compact design measures only 125 x 74 x 23mm and weighs 304 grams**

Fantastic gift for those who have everything!

Buy with confidence from Powersolve the power professionals with over 27 years experience in power! All products carry full 1 year no quibble replacement warranty!

Many other models and special offers available online.

POWER SOLVE

Buy online at **www.powersolvemobile.com** or telephone **01635-521858** and talk to one of our technical sales people who can suggest the right product for your mobile electronic device

INDUCTORLESS, LOW-VOLTAGE, LOW-POWER, LOW-COST, QUADRATURE OSCILLATOR

MINGLIN MA, ZHIJUN LI, YUAN CHEN, CHENGWEI LI AND **LIXIANG ZHOU** FROM XIANGTAN UNIVERSITY AND **XIANGLIANG JIN** FROM HUNAN ENGINEERING LABORATORY FOR MICROELECTRONICS, OPTOELECTRONICS AND SYSTEM-ON-A-CHIP IN CHINA PRESENT A QUADRATURE OSCILLATOR THAT CONSISTS OF TWO LC NEGATIVE OSCILLATORS BASED ON AN ACTIVE INDUCTOR

Wireless and mobile communications are the fastest growing microelectronics applications, with enormous impact on solution makers. Driven by the insatiable demand for lower cost, lower power and higher data rates in wireless and mobile communications systems, there is a growing demand for CMOS wireless System-on-a-Chip (SoC) solutions. This trend has motivated the evolution of and research on low-voltage, low-cost RFIC designs.

CMOS quadrature oscillators are used widely in modern digital communication systems; they are the essential circuit blocks in fully-integrated CMOS image-rejection, direct conversion, or low-IF receiver and transmitter systems.

Quadrature Oscillator Design Process

The design process of a quadrature oscillator is as follows: (1) choosing an LC-resonator; (2) combining this resonator with active transistors to form differential oscillators; (3) using two differential oscillators and passive or active coupling devices to ensure the two oscillators run in quadrature phase.

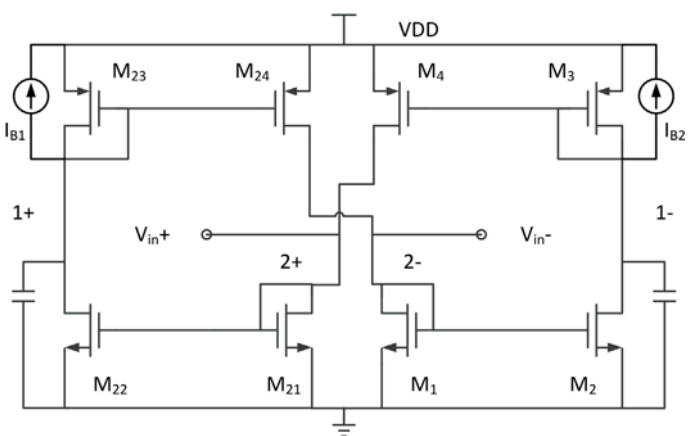


Figure 1: The suggested floating active inductor with low voltage supply

Traditional oscillators use passive inductors. To lower costs we've selected an active inductor, which sadly is not low in voltage. So here we suggest a low-voltage floating active-inductor with a two-layer transistor structure. The coupling devices include an inductor, transformer, capacitor, diode, varactor and a resistor. Considering the aspects of phase noise, voltage supply and power dissipation, the two differential oscillators are coupled by capacitors through the back gates (or body terminals) of the cross-coupled nMOS transistors.

Circuit Design

Figure 1 shows the proposed floating active inductor with low voltage supply. It consists of four current mirrors. Current mirror 1 (M1,2) and current mirror 2 (M3,4) comprise the negative feedback to port 2+, whereas current mirror 3 (M21,22) and current mirror 4 (M23,24) comprise the negative feedback to port 2-. G_{m1} and G_{m2} are the transconductances of the differential transconductors 1 (M2 and M22) and 2 (M4 and M24), The current sources (I_{B1}, I_{B2}) are used to decrease the power this active inductor needs.

Consider the equivalent network of the proposed floating active inductor shown in Figure 2. We assume that the transconductances of the transconductors are constant. Writing KCL at nodes 2+, 2-, 1+ and 1- yields:

$$(V_2^+ - V_2^-)g_{m1} = (V_1^- - V_1^+)\left(\frac{sC_1 + G_{o1}}{2}\right) \quad (1)$$

$$I_{in} = (V_1^- - V_1^+)g_{m2} + (V_2^+ - V_2^-)\left(\frac{sC_2 + G_{o2}}{2}\right) \quad (2)$$

The admittance looking into port 2 of the equivalent network (see Figure 3) can be obtained from:

$$Y = \frac{I_{in}}{(V_2^+ - V_2^-)} = \left(\frac{sC_2 + G_{o2}}{2}\right) + \frac{2g_{m1}g_{m2}}{sC_1 + G_{o1}} \quad (3)$$

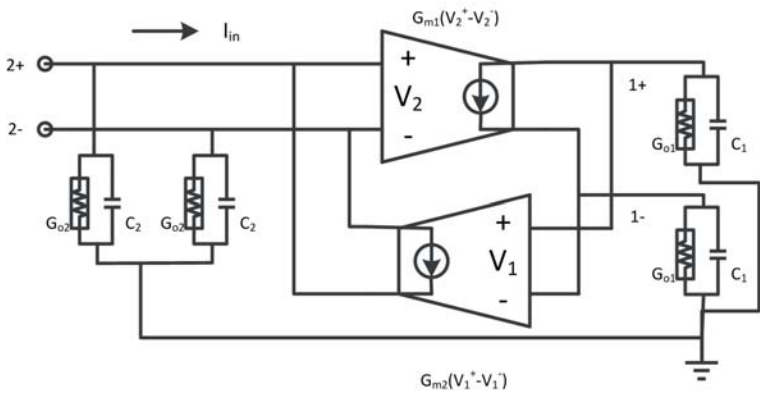


Figure 2: Equivalent network of the suggested floating active inductor

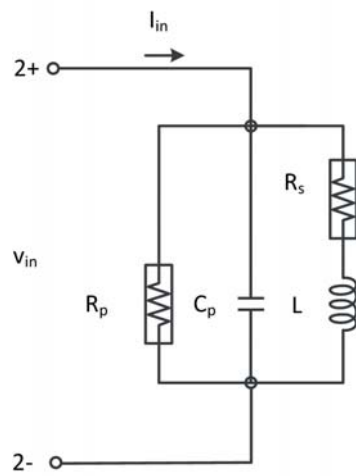


Figure 3: The admittance at port 2

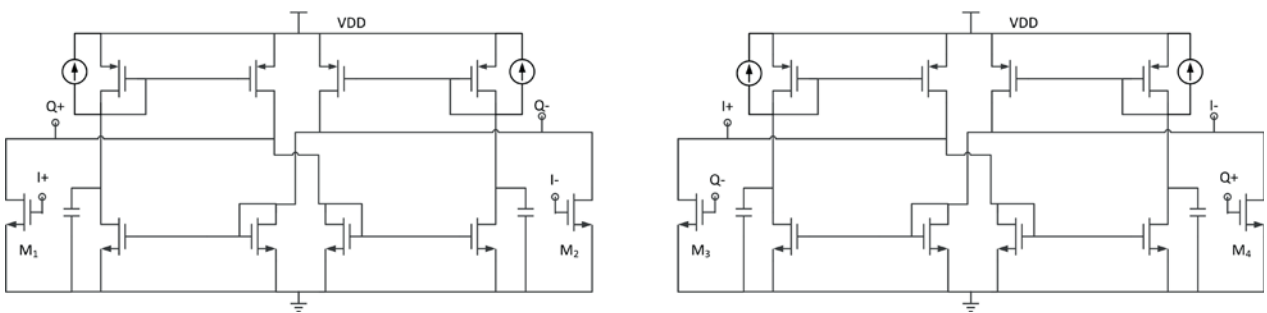


Figure 4: The proposed quadrature oscillator using a low-voltage floating active inductor

Equation 3 can be represented by the RLC network shown in Figure 3, with its parameters given by:

$$R_p = \frac{2}{Go_2}$$

$$C_p = C_2/2$$

$$R_s = \frac{Go_1/2}{g_{m1}g_{m2}} \qquad (4)$$

$$L = \frac{C_1/2}{g_{m1}g_{m2}}$$

Figure 4 shows the suggested quadrature oscillator circuit with two differential LC negative oscillators combined into one quadrature oscillator. In this quadrature oscillator, there are two floating active inductors and two cross-coupled pairs (M1,2 and M3,4), just like the quadrature-VCO using Wu's active inductors.

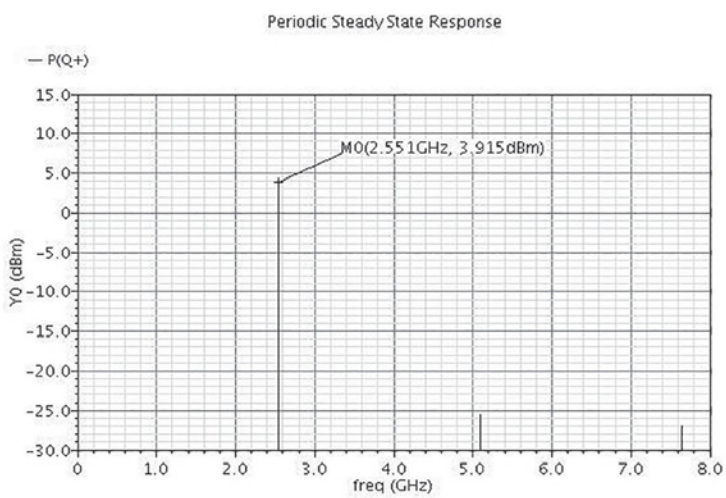


Figure 5: Simulated frequency spectrum of the quadrature oscillator

Ref.	Tech.(μm)	Vdd(V)/ PDC(mW)	PN (dBc/Hz)	Coulpling method	inductor
[3]	0.18	1.8/30.5	-100	transistor	active
[4]	0.18	1.45/8.7	-124.58	inductor	passive
[5]	0.18	0.7/5.18	-124.9	transformer	passive
[6]	0.18	0.8/7.4	-122.91	capacitor	passive
[7]	0.18	1.8/3	-120	capacitor	passive
[8]	0.18	0.54/1.78	-114	diode	passive
Our work	0.18	1.2/12	-112	transistor	active

Table 1: Comparison of CMOS quadrature oscillators performances

Simulated Results

The quadrature oscillator has been designed and simulated in 0.18μm 1P6M CMOS technology. The circuit simulation was carried out by the simulation tool Specter-RF.

The power consumption of the quadrature oscillator is 12mW at the supply voltage of 1.2V. Figure 5 shows the simulated frequency spectrum of the quadrature oscillator; the output power is 3.915dBm.

Figure 6 shows the simulated phase noise at the oscillation frequency of 2.551GHz. The phase noise is -112dBc/Hz at 1MHz offset frequency.

Figure 7 shows the simulated time-domain output waveforms of the four quadrature outputs, while Table 1 compares quadrature oscillator performances.

The simulated results prove that a quadrature oscillator using low-voltage, low-power floating active inductors is useful for RF circuit design. ●

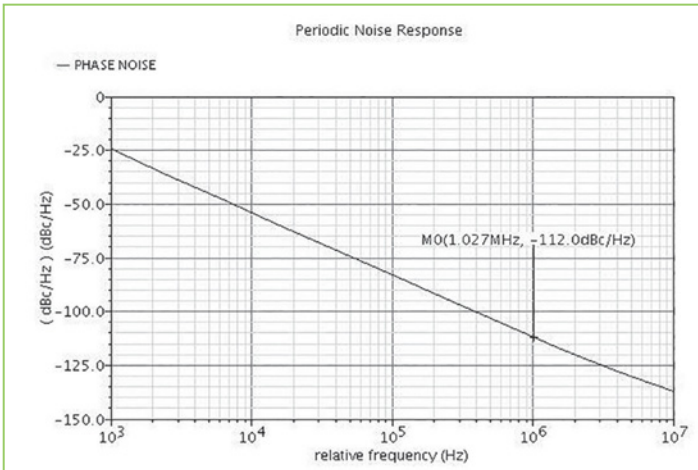


Figure 6: Simulated phase noise at oscillation frequency of 2.551GHz

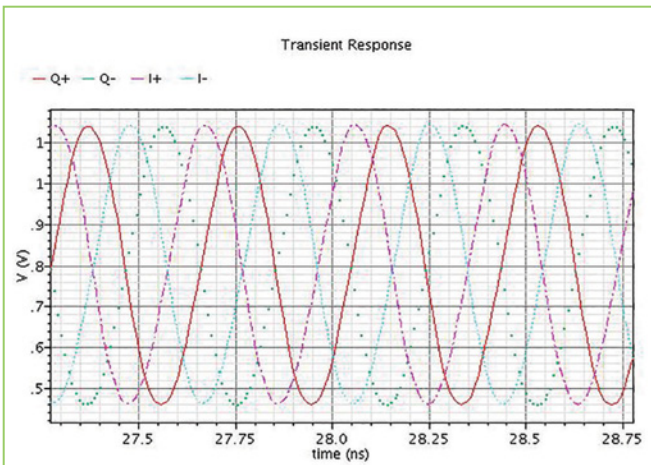
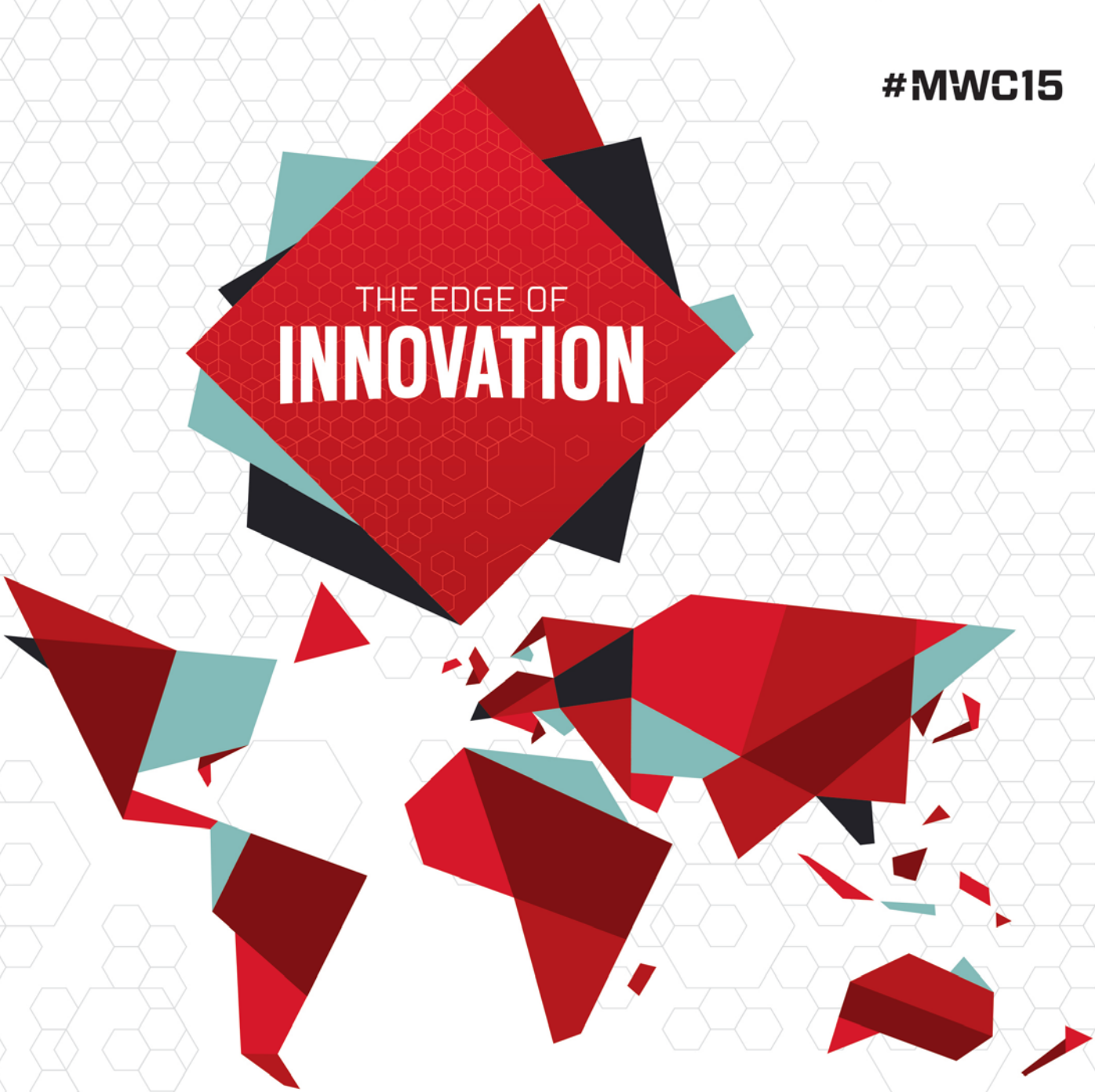


Figure 7: Simulated time-domain output waveforms of the four outputs

#MWC15



GSMA MOBILE™ WORLD CONGRESS

BARCELONA 2-5 MAR 2015

The mobile communications revolution is driving the world's major technology breakthroughs. From wearable devices to connected cars and homes, mobile technology is at the heart of worldwide innovation. As an industry, we are connecting billions of men and women to the transformative power of the Internet and mobilising every device that we use in our daily lives. The 2015 GSMA Mobile World Congress will convene industry leaders, visionaries and innovators to explore the trends that will shape mobile in the years ahead. We'll see you in Barcelona at **The Edge of Innovation.**

WWW.MOBILEWORLDCONGRESS.COM

AN EVENT OF
MOBILE WORLD CAPITAL™ BARCELONA

NEW, HIGH-PERFORMANCE, SECOND-GENERATION, CURRENT-CONTROLLED CURRENT CONVEYOR

HAIRONG LIN AND **CHUNHUA WANG** FROM THE COLLEGE OF INFORMATION SCIENCE AND ENGINEERING AT HUNAN UNIVERSITY, CHINA, PROPOSE A NEW MULTIPHASE SINUSOIDAL OSCILLATOR BASED ON CURRENT-CONTROLLED CURRENT DIFFERENCING UNITS

It is well known that multiphase sinusoidal oscillators (MSOs) are widely applied in many fields, such as power electronics, communication systems, instrumentation control, signal processing and measurement systems.

Most MSOs are based on either voltage-mode or current-mode active building blocks. Voltage-mode MSOs use operational transconductance amplifiers (OTAs), current conveyors (CCIIs), current feedback operational amplifiers (CFOAs) and current differencing buffered amplifiers (CDBAs), among others. Sadly, most of these oscillator configurations suffer from one or more disadvantages:

(a) Over-use of active and passive elements;
(b) Using floating passive components;
(c) Complex topology;
(d) Lack of electronic adjustability;
(e) Realizing only odd or even number of phases.

More recently, current-mode MSOs have received widespread attention, since they offer higher slew rate, greater linearity, lower power consumption and wider signalling bandwidth.

In 2003, a novel active device – the current differencing trasconductance amplifier (CDTA) – was developed. Its input and output signals are of the current-mode type, and CDTA has become one of the most frequently used active elements of recent analog signal processing designs.

MSOs using CDTAs or current-controlled CDTAs (CCCDTAs), offer low input and high output impedances and independent control of the oscillation frequency and condition through bias currents or external passive elements. However, from an integration point of view, the complexity of the active device has a direct impact on chip area and power, since each CDTA or CCCDTA requires a CDU or CCDU and an OTA. Such construction greatly increases chip area and power consumption.

In view of such disadvantages, there are MSO circuits based on current differencing units (CDUs) and current backward transconductance amplifiers (CBTAs) that offer improved chip complexity, area and power consumption. However, their drawbacks include the need for a passive floating resistor and a capacitor for each phase, and electronic fine-tuning is not possible.

We propose a new current-mode (CM) and voltage-mode (VM) MSO circuit by using all-pass filters (APF) employing fundamental CCDUs.

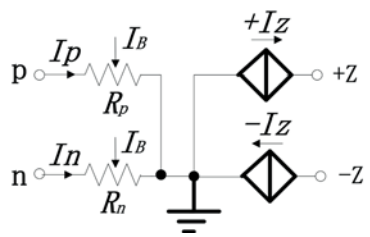


Figure 1: CCDU equivalent circuit

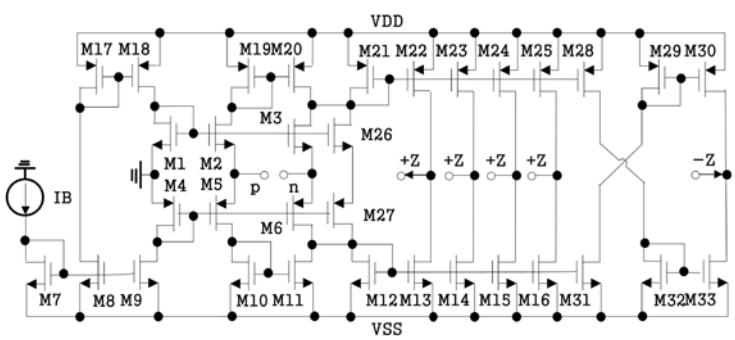


Figure 2: Possible CMOS implementation of a CCDU

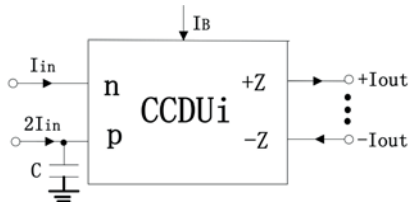


Figure 3: CCDU-based first-order allpass section

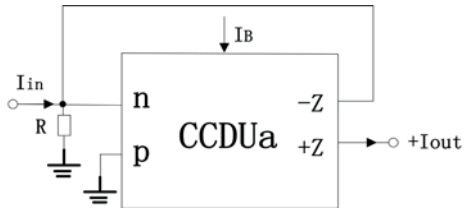


Figure 4: CCDU-based inverting amplifier

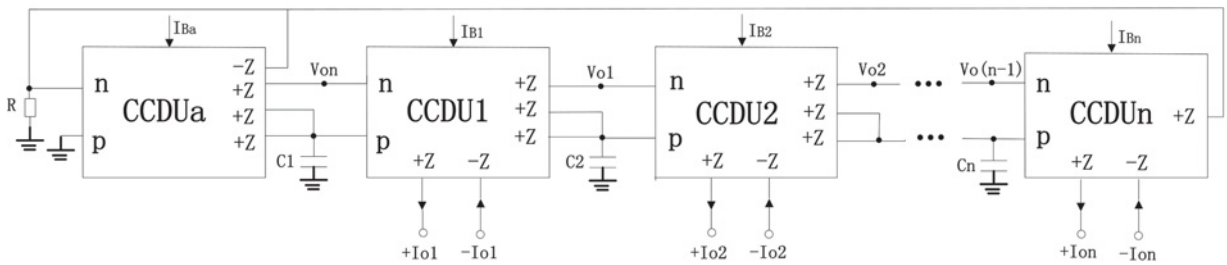


Figure 5: Proposed current-mode and voltage-mode MSO circuit

CCDUs

Compared to CDUs, CCDUs have the obvious characteristic that input resistances R_p and R_n at the p and n input terminals can be controlled by the bias current I_B. Usually, these parasitic resistances are equal.

The circuit representation and the equivalent circuit of the CCDU are shown in Figures 1a and 1b. The terminal relation of the CCDU can be described by the following matrix equation:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 \\ 0 & R_n & 0 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ 0 \end{bmatrix} \quad (1)$$

According to Equation 1 and the equivalent circuit of Figure 1b, current flowing out of the terminal +z ($+I_z$) is the difference between the input currents through terminals p and n ($I_p - I_n$). The proposed device provides current I_z in both directions, equal in magnitude.

Although there are several techniques to realize the CCDU, one possible low-voltage CMOS implementation is shown in Figure 2. Assuming transistors (M1-M6) and (M26-M27) are operated in the saturation region, the input resistances of p and n terminals can be characterized by the following equations:

$$R_p = \frac{1}{g_{m3} + g_{m6}} \quad (2)$$

$$R_n = \frac{1}{g_{m2} + g_{m5}} \quad (3)$$

where g_{mi} is the transconductance parameter of transistor M_i.

If transistors M1-M6 and M26-M27 are identical, the p and n resistances can be approximated by using:

$$R_p \cong R_n \cong \frac{1}{\sqrt{8\mu C_{ox}(W/L)I_B}} \quad (4)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the effective channel width and length.

From Equation 4, the parasitic resistances R_p and R_n can be controlled by adjusting the bias current I_B of the CCDU.

Circuit Description

In general, an MSO can be realized using various topologies, such as lossy integrators, high-pass filters, all-pass filters and so on. Here we present an MSO using a resistorless current-mode first-order all-pass filter (APF) topology, with positive and negative outputs, employing only one CCDU and one grounded capacitor; see Figure 3. Using Equation 1, we can get the current transfer function of the circuit in Figure 3:

$$\frac{I_{out}}{I_{in}} = \frac{\frac{1}{R_{pi}C} - S}{\frac{1}{R_{pi}C} + S} \quad (5)$$

Here, R_{pi} is the input resistance of the CCDUi at the p terminal. From Figure 3 it can be seen that the CCDU-based

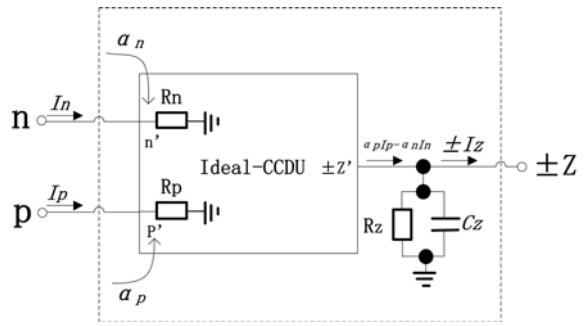


Figure 6: Model of a non-ideal CCDU

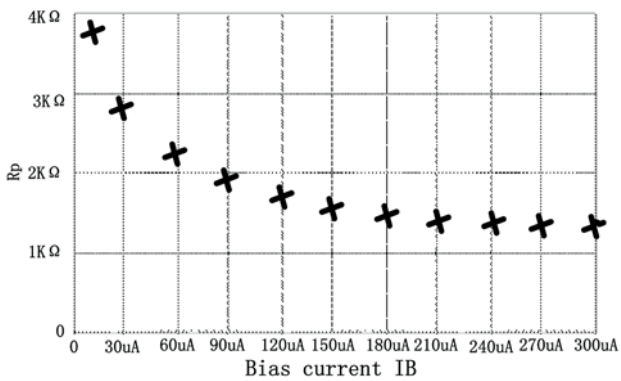


Figure 7: Variability of the resistance R_p as a function of bias current I_B

circuit does not require any external passive resistors. The phase shift (ϕ) of this section is written as:

$$\phi = -2\tan^{-1}\left(\omega R_{pi} C\right) \quad (6)$$

In the ideal case, ϕ with ω change from 0^o to -180^o and from zero (DC) to infinity. By applying Equation 6 the shifted phase value can be tuned electronically by adjusting the bias current I_{Bi}.

CCDU-Based Inverting Amplifier

A tunable current inverting amplifier using only one CCDU and one grounded resistor is shown in Figure 4; the current gain (K) of this circuit is:

$$K = \frac{I_{out}}{I_{in}} = -\frac{R}{R_{na}} \quad (7)$$

where R_{na} is the input resistance of CCDUa at terminal n, and where the amplifier gain K can be controlled electronically by tuning the bias current I_{Ba}.

The dual-mode multiphase sinusoidal oscillator (MSO) based on the CCDU is shown in Figure 5. The system includes n cascaded CCDU-based all-pass sections (see Figure 3).

The output current I_{on} of the nth stage is fed back to the input of the first stage through the current inverting amplifier in Figure 4, which reduces the oscillator topology complexity considerably. It is important that the proposed circuit realizes n current and voltage output signals simultaneously. Assuming that $R_{p1} = R_{p2} = \circ = R_{pn} = R_p\left(I_{B1} = I_{B2} = \circ = I_{Bn} = I_B\right)$ and $C_1 = C_2 = \circ = C_n = C$, the loop gain $L(S)$ of the proposed structure in Figure 5 can be calculated by:

$$L(S) = K\left(\frac{1/R_pC - S}{1/R_pC + S}\right)^n = -\frac{R}{R_{na}}\left(\frac{1/R_pC - S}{1/R_pC + S}\right)^n \quad (8)$$

According to the Barkhausen criterion (which helps determine when a linear electronic circuit will oscillate), the condition for the proposed MSO circuit of Figure 5 to oscillate at frequency $\omega(=2\pi f)$ is that:

$$L(j\omega) = -\frac{R}{R_{na}}\left(\frac{1/R_pC - j\omega}{1/R_pC + j\omega}\right)^n = 1 \quad (9)$$

and:

$$\phi = \frac{\pi}{n} \quad (10)$$

where $n \geq 2$. Equation 10 shows that there are n outputs I_{oi} and $V_{oi}\left(i = 1,2,\circ, n\right)$, each shifted in phase by $180^o/n$, so the oscillation condition (OC) and frequency (OF) can be determined as:

$$\text{OC:} \quad \frac{R}{R_{na}} = 1 \quad (11)$$

and

$$\text{OF:} \quad \omega = \left(\frac{1}{CR_p}\right)\tan\left(\frac{\pi}{2n}\right) \quad (12)$$

Further, by substituting Equation 4 into Equations 11 and 12, the following can be determined:

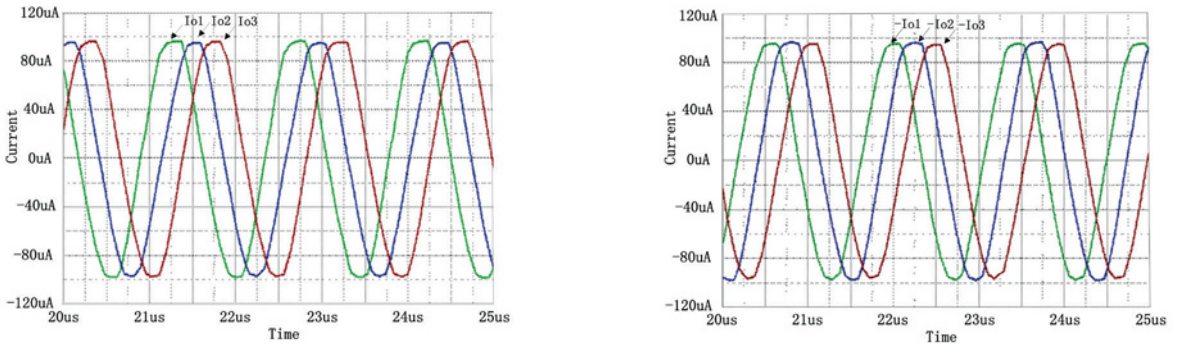


Figure 8: Simulated output currents of the proposed MSO

OC:
$$R = \frac{1}{\sqrt{8\mu C_{ox}(W/L)I_{Ba}}} \quad (13)$$

and

OF:
$$\omega = \left(\frac{\sqrt{8\mu C_{ox}(W/L)I_B}}{C}\right)\tan\left(\frac{\pi}{2n}\right) \quad (14)$$

From Equations 13 and 14 can be seen that ω can be tuned electronically by the bias current I_B without affecting the condition of oscillation, which can also be changed through varying the bias current I_{Ba} without influencing ω. Therefore, the circuit provides the attractive feature of independent current control of frequency and condition of oscillations. Additionally, by using an inverted version of the CCDU's output current, the 2n-phase outputs $(-I_{o1}, -I_{o2}, \cdots, -I_{on})$ are also obtained from the same topology.

Non-Ideal Case

For a non-ideal case, the CCDU in Figure 1a is modelled by the circuit in Figure 6. As can be seen, there are parasitic resistance R_z and parasitic capacitances C_z at terminal z, with its current described in the form of:

$$I_z = \alpha_p I_p - \alpha_n I_n \quad (15)$$

where α_p and α_n are current transfer values, which can deviate from their ideal values (1) depending on the internal circuit construction. R_p and R_n are the parasitic resistances of the terminals p and n. So, taking into account the non-ideal CCDU characteristics and its parasitic elements, the modified current transfer functions of Figures 3 and 4 can be rewritten as:

$$\frac{I_{out}}{I_{in}} = \alpha_n \frac{1 - s\left(\frac{\alpha_n C R_p}{\alpha_p}\right)}{\frac{\alpha_n}{\alpha_p} + s\left(\frac{\alpha_n C R_p}{\alpha_p}\right)} \quad (16)$$

and

$$\frac{I_{out}}{I_{in}} = -\frac{\alpha_n R}{R_{na}(1 + sC_z) + R\left(1 - \alpha_n + \frac{R_{na}}{R_z}\right)} \quad (17)$$

Using Equations 16 and 17 with $C_z >> C, R_{na} >> R_z$, the modified ω and oscillation condition can be determined with the following equations:

OC:
$$R = \frac{1}{(2\alpha_n - 1)\sqrt{8\mu C_{ox}(W/L)I_{Ba}}} \quad (18)$$

OF:
$$\omega = \left(\frac{\alpha_p\sqrt{8\mu C_{ox}(W/L)I_B}}{\alpha_n C}\right)\tan\left(\frac{\pi}{2n}\right) \quad (19)$$

It should be mentioned here that the oscillation condition is mainly affected by the current transfer error α_n of the CCDU. However, the effect of these errors can easily be accommodated by changing the bias current (I_{Ba}). Also, it can be seen that ω is slightly different from the ideal case by a factor of α_p/α_n. To compensate for this effect, the bias current I_B can be adjusted slightly.

The ω-sensitivity analysis with respect to the parameters of the active and passive elements used can be determined as:

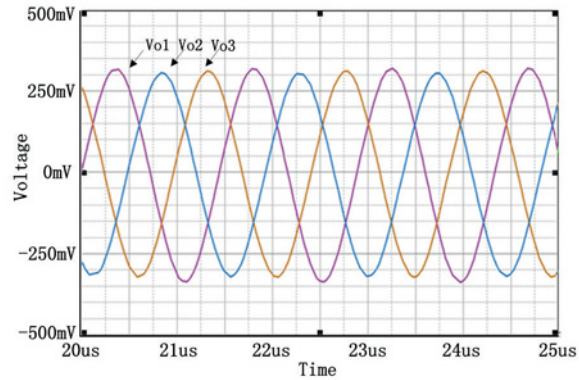


Figure 9: Simulated output voltages of the proposed MSO

$$S_{\alpha_p}^{\omega} = -S_{\alpha_n}^{\omega} = -S_{R_p}^{\omega} = 1, S_C^{\omega} = 1 \qquad (20)$$

Thus, the proposed topology enjoys low sensitivity to active and passive element variations.

Simulation Results

The behaviour of the MSO topology in Figure 5 has been studied through simulations performed by employing PSPICE software. The CCDU in Figure 2 was simulated using TSMC's 0.25um CMOS technology. The dimensions of the CMOS transistors are listed in Table 1.

The CCDU circuit is supplied with symmetrical voltages VDD = -VSS = 1.5V. Using PSPICE simulations, variations of resistance (R_p) with bias current I_B are shown in Figure 7.

Resistance R_p can be controlled by changing the CCDU bias current I_B within a wide current range.

In order to prove the performance of the proposed circuit, a six-phase (n = 3) oscillator was designed. Here, the external bias currents are $I_{B1} = I_{B2} = I_{B3} = I_B = 40uA(R_p = 2.62K\Omega)$ and $I_{Ba} = 35uA(R_{na} = 3.60K\Omega)$, the grounded capacitors are $C_1 = C_2 = C_3 = C = 52pF$ and the external resistor $R = 3.63K\Omega$.

The output waveforms and frequency spectra obtained from the proposed MSO topology of Figure 5 are shown in Figures 8, 9 and 10. Figures 8 and 9 show the current and voltage output signals of each stage in the six-phase oscillator, respectively. It is evident that the amplitudes of all output signals are equal.

The corresponding frequency spectrum of the output signals for n = 3 is shown in Figure 10. The oscillation frequency is measured as 672.24kHz by the simulation, which is close to the calculated value of 674.77kHz. From the simulation results, it is noted that the phase difference of $I_{o2}, I_{o3}, -I_{o1}, -I_{o2}, and -I_{o3}$ compared to I_{o1} were obtained by using $61^o, 119^o, 180^o, 242^o$ and 300^o, very close to the theoretical values.

The variability of the oscillation frequency (f_o) as a function of the bias current (I_B) is seen in Figure 11, showing that the circuit exhibits a large tuning range. Although there is a difference between the theoretical and simulation values in the high-bias-current region, this error can be decreased by modifying the value of the external capacitors.

All the properties presented here for this circuit make the proposed topology highly suitable for use in both current mode and voltage-mode analog signal processing. ●

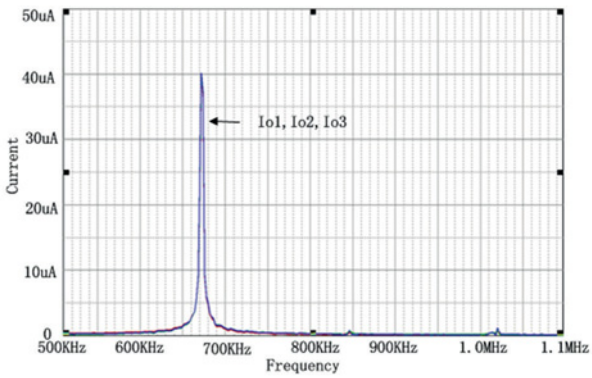


Figure 10: Simulated frequency spectrums for I_{o1}, I_{o2} and I_{o3}

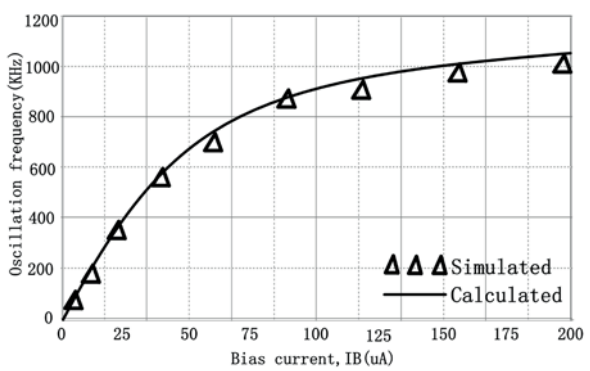


Figure 11: Variations of the frequency (f_o) with bias currents I_B

COMS TRANSISTORS	W(um)/L(um)
M1-M3,M26	2/0.5
M4-M6,M27	7/0.5
M7-M16,M31-M33	5/0.5
M17-M25,M28-M30	15/0.5

Table 1: Dimensions of the CMOS transistors

A NOVEL GRID MULTI-SCROLL CHAOTIC OSCILLATOR

YUAN LIN AND **CHUNHUA WANG** FROM THE COLLEGE OF INFORMATION SCIENCE AND ENGINEERING AT HUNAN UNIVERSITY IN CHINA PRESENT A NEW GRID MULTI-SCROLL CHAOTIC OSCILLATOR CIRCUIT EMPLOYING SECOND GENERATION CURRENT CONVEYORS

Chaotic signals have proven very useful in a wide number of applications including secure communications, signal encryption, medical applications, neural networks and even music generation. Due to the increase in chaotic signal applications, there's a growing demand for electronic chaotic signal generators that are simple and easy to construct, with an extended frequency range and that are suitable for low-voltage integrated circuit design.

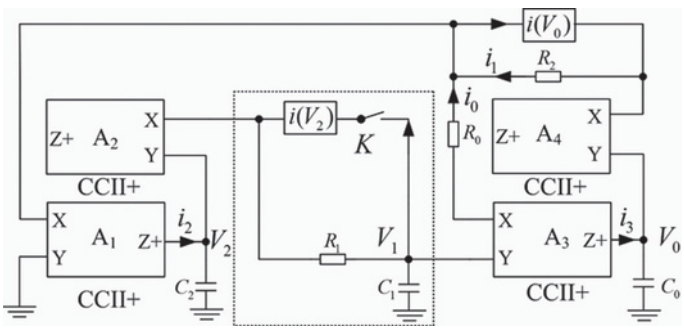


Figure 1: Suggested grid multi-scroll chaotic circuit

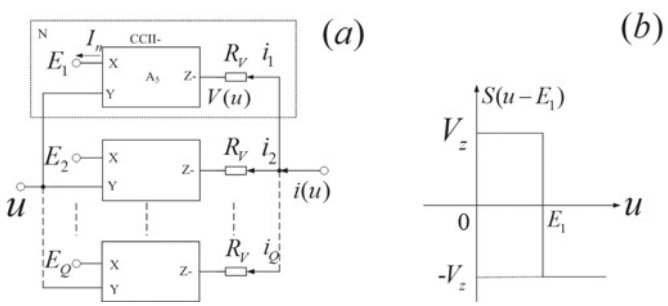


Figure 2: The SNFS circuit and shifted voltage: (a) The voltage SNFS circuit structure; (b) Shifted voltage stair function $S(u-E_1)$

There are many ways to generate chaotic electronic oscillations: using conventional op-amps, operational transconductance amplifiers (OTAs), current feedback operational amplifiers (CFOAs), second generation current conveyors (CCIIs) or special integrated circuits. Since CCII-based implementations offer better performance than op-amp based implementations in terms of accuracy and bandwidth, researchers have focused on CCIIs in the implementation of chaotic oscillators to improve high-frequency performance.

Single- and double-scroll chaotic oscillators have already been designed with CCIIs, but multi-scroll attractors (in the mathematical field of dynamic systems, an attractor is a set of numerical properties toward which a system tends to evolve, for a wide variety of starting conditions) are preferred over the double-scroll attractors. Hasan et al built 5-scroll chaotic oscillators with CCIIs, based on fifth-order nonlinear equations. Sanchez-Lopez et al realized one direction (1D) 3- and 4-scroll chaotic attractors based on a generalized Jerk circuit using the Analog Devices AD844 as CCII and voltage follower, with the chaotic frequency spectrum centred at 43kHz.

Here, we suggest a novel grid multi-scroll chaotic circuit that includes only CCIIs as active devices: two current integrators and voltage followers employing CCII+, and passive RC integrator and nonlinear elements employing CCII- to realize current saturated nonlinear function series (SNFS). The proposed chaotic circuit is mathematically modelled, using third-order nonlinear differential equations. The chaotic behaviour of the proposed circuit is verified in both numerical simulations and PSPICE simulation, using a model of the TMSC 0.18µm technology at 1.5V to illustrate the feasibility of the design for low-voltage applications. The result shows that the simple chaotic circuit can generate more scroll chaotic attractors in one direction. The operating frequency is increased, with the chaotic frequency spectrum centred approximately on 3MHz.

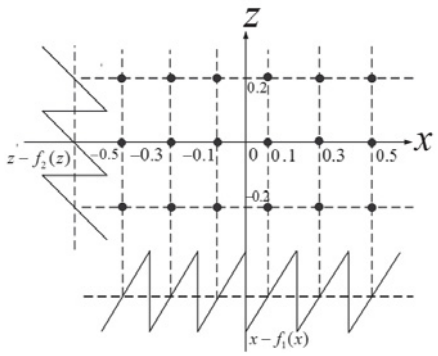


Figure 3: The equilibrium points of grid multi-scroll chaotic attractors distributed in x-z phase

Grid Multi-Scroll Chaotic Oscillators

Figure 1 shows the proposed new grid multi-scroll chaotic circuit. It includes two current integrators A1 and A3 and voltage followers based on CCII+, a passive RC integrator and two current SNFS components realized with CCII-. The circuit is mathematically modelled through circuit analysis. The parasitic effects of concern in a CCII are the small input resistance R_x of the inverting terminal and the capacitance of the compensating terminal C (appearing in parallel with C_i (i = 0, 2)).

The contribution of R_x is negligible as it is dominated by the series resistance R_i (i = 0, 2) if R_x is small. On the other hand, the values of C_i (i = 0, 2), should be larger to neglect the effect of C at high frequencies. The circuit is described by the following equations:

$$\begin{cases} \dot{V}_0 = \dfrac{V_1}{R_0 C_0} \\ \dot{V}_1 = -\dfrac{V_1}{R_1 C_1} + \dfrac{V_2}{R_1 C_1} - \dfrac{i(V_2)}{C_1} \\ \dot{V}_2 = -\dfrac{V_0}{R_2 C_2} + \dfrac{i(V_0)}{C_2} - \dfrac{V_1}{R_0 C_2} \end{cases} \quad (1)$$

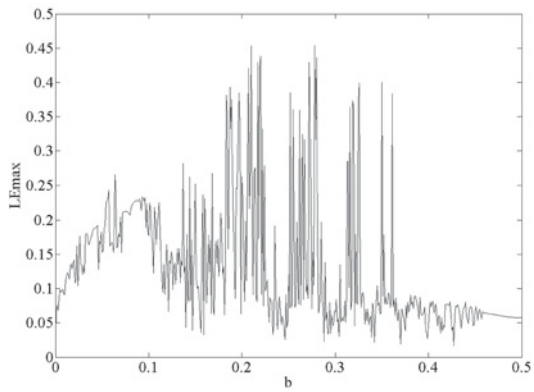


Figure 4: Maximum LE spectrum of parameter b

which is a set of third-order nonlinear differential equations in voltages (V_0, V_1 and V_2) and nonlinear component output current ($i(V_0), i(V_2)$) form. It can also generate only one-direction multi-scroll when K is off, corresponding to $i(V_2) = 0$.

The current SNFS can be synthesized by using CCII-, as shown in Figure 2a. Taking $i(V_0)$ for example, the voltage gain of virtual box N in Figure 2a is given by $V_z = -A_z I_n = -A_z \dfrac{(u - E_1)}{R_x}$, where Z is the open-loop transimpedance gain of CCII-, and R_x the resistance of the CCII inverting input terminal X.

Assume that the saturation voltage of all CCIIs is $\pm|V_{sat}|$ under the specific supply voltage, then the output voltage of A_5 is:

$$V(u) = S(u - E_1) = -|V_{sat}|\,\mathrm{sign}(u - E_1) \quad (2)$$

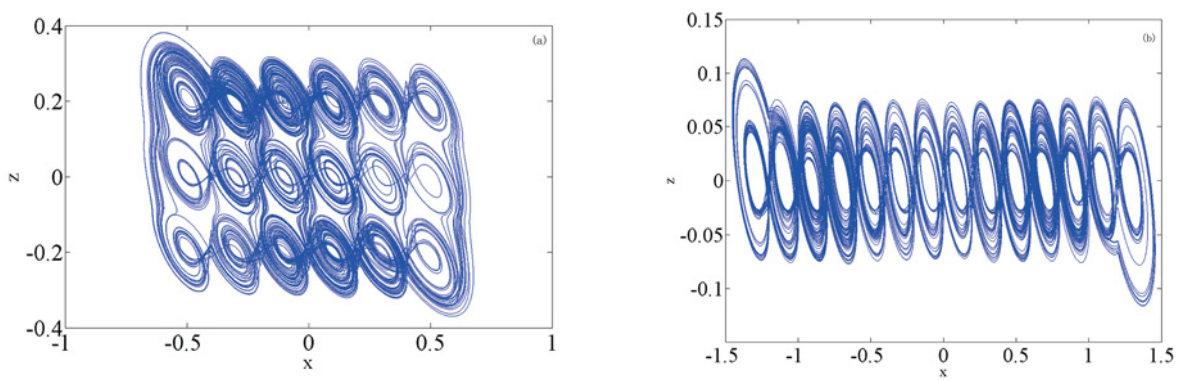


Figure 5: Multi-scroll chaotic attractors in $x-z$ phase: (a) 6×3-scroll; (b) 14-scroll

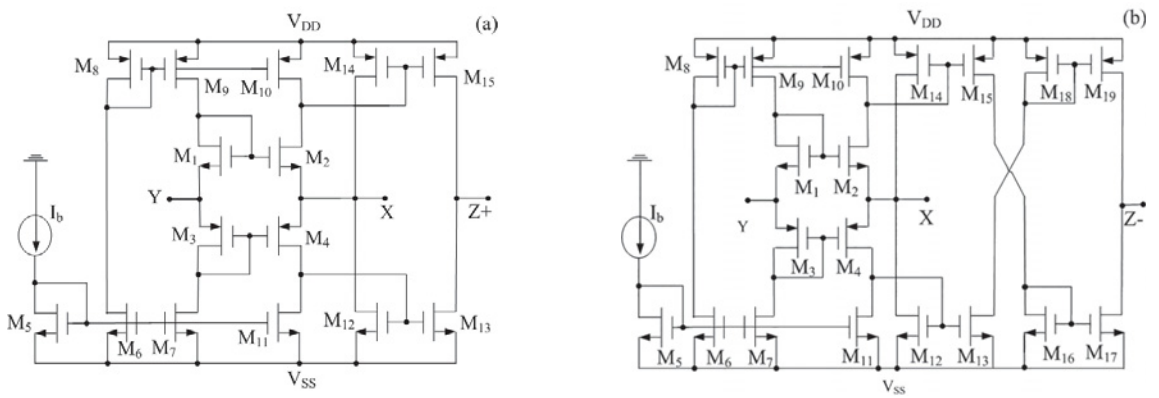


Figure 6: CMOS structure of CCII: (a) CCII+; (b) CCII-

Figure 2b shows the shifted voltage stair nonlinear function $S(u-E_1)$, where E_1 is the turning point and also the turning point of the SNF. We can obtain:

$$i_1 = \frac{0-V(u)}{R_v} = \frac{|V_{sat}|\,sign(u-E_1)}{R_v} \tag{3}$$

By connecting several basic cells in parallel as shown in Figure 2a, the current SNFS can be described as:

$$i(u) = \sum_{j=1}^{Q} i_j = \sum_{j=1}^{Q} \frac{|V_{sat}|\,sign(u-E_j)}{R_v} \tag{4}$$

Analysis And Numerical Simulations

Setting $x=V_0$, $y=V_1$, $z=V_2$, $t=R_0C_0\tau$, $dt=R_0C_0d\tau$, $a=R_0C_0/(R_0C_0)$, $b=R_0C_0/(R_1C_1)$, $c=R_0C_0/(R_2C_2)$ and $d=R_0C_0/(R_0C_2)$, the set of equations given in (1) can be written in the following dimensionless form:

$$\begin{cases} \dot{x} = \mathrm{a}\cdot y \\ \dot{y} = b\cdot(-y+z-f(z)) \\ \dot{z} = -c\cdot(x-f(x)) - d\cdot y \end{cases} \tag{5}$$

Referring to Equations 1-5, we get: $f(x)=R_2\cdot i(V_0)$, $f(z)=R_1\cdot i(V_2)$, which are SNFS as nonlinear controllers to stretch and fold the trajectories of the system repeatedly. Then:

$$f_1(u) = A\cdot\xi\sum_{j=-M}^{M} sgn[u+2j\xi] \tag{6}$$

for $2M+2$-even scrolls or:

$$f_2(u) = A\cdot\xi\sum_{\substack{j=-N\\ j\neq 0}}^{N} sgn[u+\xi(2j-\frac{|j|}{j})] \tag{7}$$

for $2N+1$-odd scrolls, where $u\in\{x,z\}$, M and N are two integers, $\xi=E_1=V_{sat}/R_v$. Various grid multi-scroll chaotic attractors can be created in the set of equations (5) considering the SNFS as below:

$f(x)\in\{f_1(x),f_2(x)\}$ and $f(z)\in\{f_1(z),f_2(z)\}$ for some suitable parameters a, b, c, d. We set $R_0=R_1=R_2=1K\Omega$, $C_0=\frac{1}{2}C_1=\frac{1}{4}C_2=25pF$, then $a=1$, $b=0.5$, $c=0.25$, $d=0.5$.

Dissipation

For system (5), $\nabla V=\partial f_1/\partial x+\partial f_2/\partial y+\partial f_3/\partial z=-b<0$. Therefore, system (5) is dissipative.

Letting $\dot{x}=0$, $\dot{y}=0$, $\dot{z}=0$ in system (5) with Equation 6 or 7, equilibrium points are obtained by:

$$\begin{cases} y=0 \\ z\text{-}f(z)=0 \\ x-f(x)=0 \end{cases} \tag{8}$$

As for $(2M+2)\times(2N+1)$ scrolls, based on Equations 6-8 we get:

$$\begin{cases} y=0 \\ z=2n\xi & n=(0,\pm1,\pm2,\mathrm{L}\ ,\pm N) \\ x=(2m+1)\xi & m=(0,\pm1,\pm2,\mathrm{L}\ ,\pm M) \end{cases} \tag{9}$$

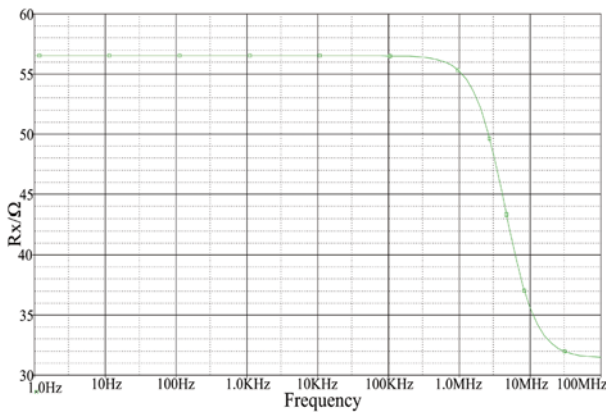


Figure 7: PSPICE simulation of R_x in CCII+

For example, if M = 2; N = 1, the equilibrium points of 6×3 scrolls chaotic attractors are located on the x-z plane as shown in Figure 3.

Obviously, system (5) has 18 equilibria points, with eigenvalues $\lambda_1 = -0.9196, \lambda_{2,3} = 0.2098 \pm 0.3031i$, called saddle points of index 2, because the two complex conjugate eigenvalues have positive real parts. System (5) has the potential to create 6×3 scroll chaotic attractor for the parameters.

Maximum Lyapunov Exponent

To further prove the existence of chaos in system (5), take 6×3 scrolls chaotic attractors generated by SNFS for example. To accurately calculate the Lyapunov exponent (LE) of system (5), the continuous differentiable function $\tanh(K(u \pm n\xi))$ should be adopted to approximate the sign function $\mathrm{sgn}(u \pm n\xi)$.

The LE spectrum is also obtained as shown in Figure 4, where the existence of positive LE implies the chaotic nature of the system. Here, $f_1(x)$ and $f_2(z)$ are used for generating chaotic attractor with $(2M+2)\times(2N+1)$ scrolls. For $\xi = 0.1$, $M = 2$, $N = 1$, the numerical simulation result of 6×3 scrolls chaotic attractors is depicted in Figure 5a. The results demonstrate that system (5) can create 6×3-scroll chaotic attractor for the parameters. In turn, $f_1(x)$ and $f_1(z)$ are designed to generate chaotic attractor with $(2M+2)\times(2M+2)$ scrolls. Similarly, $(2N+1)\times(2M+2)$ and $(2N+1)\times(2N+1)$ scrolls chaotic attractors can be created by $f_2(x)$, $f_1(z)$ and $f_2(x), f_2(z)$, respectively. When K is off, $f_1(x)$ and $f_2(x)$ are used for generating a 1D chaotic attractor with $(2M+2)$ and $(2N+1)$ scrolls, respectively. For example, letting $\xi = 0.1$, $N = 6$, the numerical simulation result of 14 scrolls chaotic attractors created by $f_2(x)$ is depicted in Figure 5b.

PSPICE Simulations

The contrivable CCII+ and CCII- are shown at transistor level in Figure 6. The oscillator was simulated with the PSPICE software using a real circuit at transistor level, using TMSC 0.18μm CMOS technology models. The supply voltage was ±1.5V with $I_b = 100\mu A$.

In the designed CCII+, the parasitic resistance R_x of the inverting terminal can be simulated by PSPICE, as shown in Figure 7. The value of R_x is about 56Ω; the contribution of R_x is negligible because it is dominated by the series resistance $R_i = 1K\Omega (i = 0,1,2)$.

Taking $R_0 = R_1 = R_2 = 1k\Omega$, C_0=25pF, C_1=50pF, C_2=100pF, experimental results show the output saturated voltage $\pm|V_{sat}|$ is about $\pm 1.5V$. Tables 1 and 2 show the current SNFS $i(V_0)$ and $i(V_2)$ parameter values for achieving 16 scrolls and 6×3 scrolls, respectively.

The PSPICE simulation results of 1D 16 scrolls chaotic attractors are shown in Figure 8. The proposed multi-scroll chaotic oscillator circuit employing CCIIs can generate more scroll chaotic attractors compared with the existing literature able to physically realized 1D 14 scroll chaotic attractors at the most.

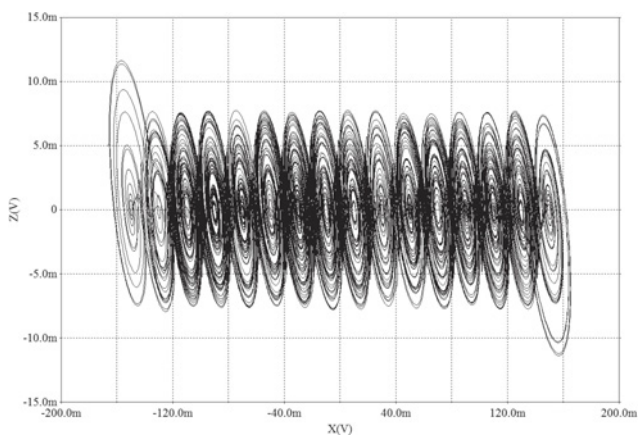


Figure 8: PSPICE simulation of 16-scroll attractor

SNSF	E_1	E_2	E_3	E_4	E_5	R_v
$i(V_0)$	$0mV$	$-20mV$	$20mV$	$-40mV$	$40mV$	$150k\Omega$
$i(V_2)$	$-10mV$	$10mV$	×	×	×	$150k\Omega$

Table 1: SNFS parameters for 16 scrolls

SNSF	E_1	E_2/E_3	E_4/E_5	E_6/E_7	E_8/E_9	E_{10}/E_{11}	E_{12}/E_{13}	E_{14}/E_{15}	R_v
$i(V_0)$	0V	$20mV$ / $-20mV$	$40mV$ / $-40mV$	$60mV$ / $-60mV$	$80mV$ / $-80mV$	$100mV$ / $-100mV$	$120mV$ / $-120mV$	$140mV$ / $-140mV$	$150k\Omega$

Table 2: SNFS parameters for 6×3 scrolls

Similarly, the results of 6×3 scrolls chaotic attractor are shown in Figure 9.

In general, there is a trade-off between the number of scrolls and the frequency of operation, as well the frequency behaviour of the cells used to design the SNFS. The 16-scroll scroll chaotic frequency spectrum is shown in Figure 10; the chaotic frequency spectrum is centred approximately at 3MHz. Moreover, higher frequencies can be achieved by designing the CCIIs with CMOS technology.

The numerical simulations of the derived models and PSPICE results verify that the proposed chaotic electronic oscillator can generate more scroll chaotic attractors with higher frequency and low voltage, which is very important for designing secure chaotic communications systems. ●

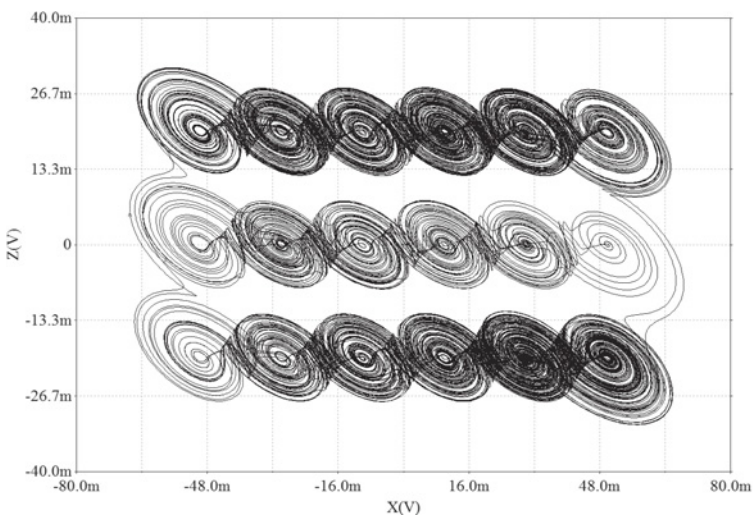


Figure 9: PSPICE simulation of 6×3-scroll chaotic attractor

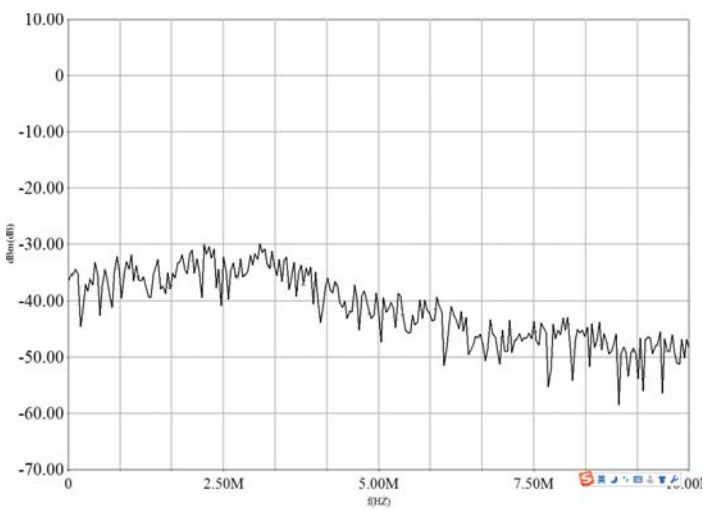


Figure 10: PSPICE simulation of 16-scroll attractor frequency spectrum

INTEGRATED TEMPERATURE AND RELATIVE HUMIDITY SENSORS

IN WIRELESS ENVIRONMENTAL CONTROL AND MONITORING APPLICATIONS

IN THIS SERIES, PROFESSOR DOGAN IBRAHIM OF THE NEAR EAST UNIVERSITY IN CYPRUS PRESENTS SEVERAL DIFFERENT TYPES OF RF SYSTEMS FOR EMBEDDED APPLICATIONS. IN THIS ARTICLE HE DESCRIBES THE USE OF INTEGRATED TEMPERATURE AND HUMIDITY SENSORS EASILY CONNECTED WITH A MICROCONTROLLER-BASED WIRELESS SYSTEM

Environmental sensors are used in many areas, including weather forecasting, air quality monitoring, ecological research, agriculture, wildlife monitoring and so on. Some of the sensor types used in environmental monitoring and control are temperature, humidity, pH, acoustic, solar radiation, light level, wind speed and direction, atmospheric pressure, rain, and chemical compounds in air and water (see Table 1 of the most common sensors).

The output signal of some sensors is digital, with the data usually sent in serial format either in standard RS232, SPI or I2C bus protocols. Some sensors provide analog output voltage, so an A/D converter must be used to convert the signal into digital format before it's processed. Others, however, provide more than one type of output, as is the case with the integrated sensors SHT11 and RHT03 listed in Table 1.

In environmental data collection applications, a network of mobile sensor stations is usually established with each station sending its own data at pre-assigned times to a central processing unit. The mobile sensor stations are identified by unique identity codes, or by using GPS to send their geographical co-ordinates and other data.

In this article we will discuss the use of the popular RHT03 integrated temperature and humidity sensor chip in embedded systems.

Example System

Figure 1 shows the block diagram of an example telemetry system. Here, the transmitting side consists of the RHT03 sensor chip, the Start USB for PIC development kit (www.mikroe.com) and the TXL02 transmitting modem (www.radiometrix.com). The start USB for PIC kit (Figure 2) is a PIC microcontroller-based development board with an onboard PIC18F2550 microcontroller, operating with an 8MHz crystal.

The microcontroller is shipped pre-loaded with a Bootloader program so it can be directly programmed via the mini-USB port on the board from a PC using a host bootloader applications program. The development board provides access to the microcontroller I/O pins through edge connectors.

The receiving side consists of RXL02 receiving modem, a processor and a display. In practice, the processor could be a microcontroller, a PC, Raspberry Pi, or any other digital computer.

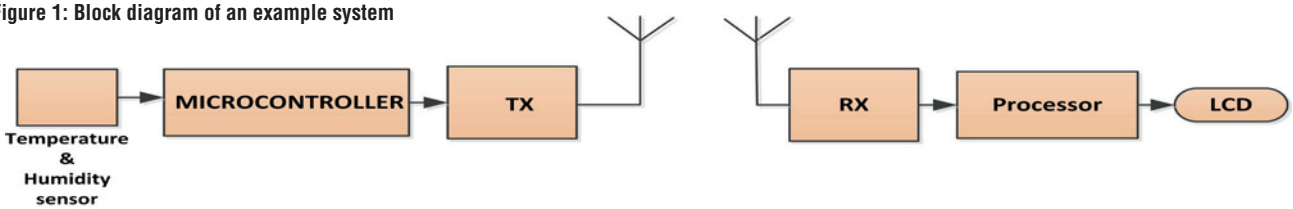
The RHT03 is a 4-pin capacitive-type temperature and humidity sensor chip (Figure 3), interfaced with the microcontroller using only one wire. The sensor operates with 3.6-5.5V and can measure temperature in the range -40°C to +80°C with accuracy of ±0.5°C.

Relative humidity can be measured in the range 0-100% with accuracy of ±2%. The sensor consumes only 1-1.5mA during normal operation and 4-50µA in standby.

Figure 4 shows the RHT03 timing diagram. Operation of the device is based on the MaxDetect 1-wire bus by MaxDetect Technology.

At first the MCU data pin is configured as an output, and data transmission starts after the MCU lowers this pin for a minimum of 18ms. The MCU then pulls the pin high for the next 20-40µs before configuring the data pin as an input.

Figure 1: Block diagram of an example system



The sensor responds to the MCU by pulling its data line low for 80µs. Next, the data line is pulled high by the sensor for another 80µs, enabling it to receive the temperature and humidity data. Data transfer begins with the sensor lowering the data line for 50µs and then sending the data bit by pulling the line high. The duration of logic 0 and logic 1 are 25-40µs and 70µs respectively. The required delays and timing can be met by using the timer interrupt facilities of microcontrollers, although built-in delay functions can also be used.

Data is returned by the sensor as 40 bits (5 bytes). First two bytes represent the humidity data; the next two represent 16-bit temperature data with the MSB denoting the sign. The last byte is the checksum, which is equal to the sum of the first four bytes of data received from the sensor. User programs should check the checksum byte to make sure that correct data has been received.

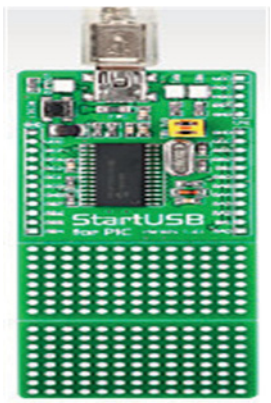


Figure 2: Start USB for PIC kit

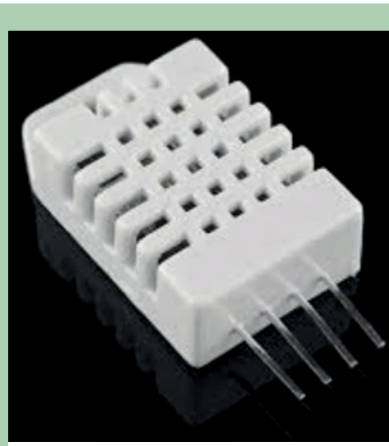


Figure 3: RHT03 temperature and humidity sensor

The TXL2/RXL2 Modem Pair

Many different types of wireless modems can be used in embedded systems. In this project the Radiometrix TXL2/RXL2 modem pair is used (Figure 5). These are UHF, multi-channel, 9600-baud, simplex radio modems requiring just an external antenna for their operation.

Unencrypted serial raw ASCII data is sent by the transmitter module. The TXL2/RXL2 can operate on one of five different channels and offers up to 8 unique addresses.

The TXL2 provides +10dBm (10mW) power to a 50Ω antenna. Operation of the device is extremely simple because it requires only the TXD input pin to be driven with serial user data. Since this pin is inverted, it can be connected directly to a microcontroller UART output pin.

The RXL2 has sensitivity of -107dBm and adjacent-channel rejection of 60dB. Received serial data is available at the RXD output, which is normally connected to a UART to capture the data.

Figure 6 shows the circuit diagram of the transmitter hardware (the receiver hardware is not shown here due to its complexity and because it depends on the type of processor used). Notice that it is recommended that the RHT03 data line be pulled high with a 4.7K resistor.

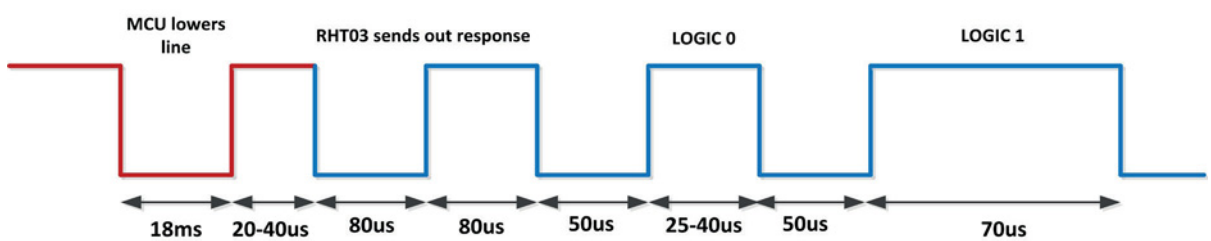


Figure 4: RHT03 sensor timing diagram. The red line is the MCU output; the blue line is the sensor output

Figure 5: The TXL2/RXL2 modem pair

Figure 6: Circuit diagram of the transmitter hardware

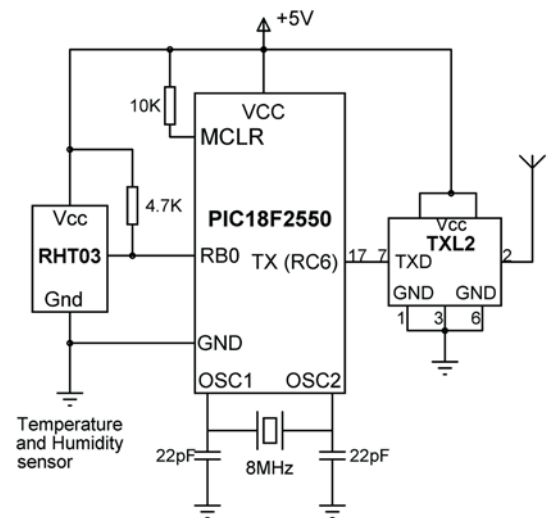


Figure 7: Operation of the transmitter program

```
BEGIN
        Configure microcontroller I/O ports
        Configure UART
        DO FOREVER
                Send Start pulse to RHT03
                Read RHT03 response
                Read temperature and humidity data
                Send to UART transmit buffer
                Wait 1 minute
        ENDDO
END
```

Figure 8: Operation of the receiver program

```
BEGIN
        Configure I/O ports
        Configure UART
        Initialize LCD
        DO FOREVER
                Read temperature and humidity from RXL02
                Display data on LCD
                ENDIF
        ENDDO
END
```

Sensor	Used for measuring	Output
LM35	Temperature	Analog
DS1820	Temperature	Digital
SHT11	Temperature + Humidity	Digital
RHT03	Temperature + Humidity	Digital
MPX10	Barometric Pressure	Analog
KP125	Barometric Pressure	Analog
MG811	Carbon dioxide	Analog
MQ-6	LPG	Analog
MQ-7	Carbon monixide	Analog
MQ131	Ozone	Analog
MQ-4	Methane	Analog
MQ-8	Hydrogen	Analog
MQ135	Air quality	Analog
MAX44007	Light sensor	Digital

Table 1: Some popular environmental sensors

The Software

The test system's software is based on the mikroC Pro for PIC language. This is a popular microcontroller programming language developed by mikroElektronika. Programs are normally developed and compiled on a PC, and loaded to the target microcontroller through a bootloader program.

Figure 7 shows the operation of the transmitter program, which executes in an endless loop. The program reads the temperature and humidity data from the sensor each minute and sends the data to the TXL2 in serial format using the mikroC built-in UART functions.

Operation of the receiver program is shown in Figure 8. The program also operates in an endless loop; the temperature and humidity data are received via the RXL02 receiver and displayed on an LCD.

The actual microcontroller program listing is shown in Figure 9 (again, the receiver software is not shown). At the beginning of the program, the interface to the RHT03 sensor and the TXL02 modem are defined. The main program initialises the UART to 9600 baud, and enters an endless loop. Inside this loop function RHT03_Start() is called to send a start pulse to the sensor. The sensor response is read using the RHT03_Read_Response() function. Function Read_RHT03() reads the temperature and humidity data from the sensor. The data is then sent to the TXL02 modem using the built-in UART function UART1_Write_Text(). ●

Figure 9: Transmitter program

```
sbit RHT03_Data at RB0_bit;
sbit RHT03_Data_Dir at TRISB0_bit;
unsigned int humidity, temperature;

unsigned short i,RHT03_Byte1, RHT03_Byte2, RHT03_Byte3, RHT03_Byte4;
unsigned char Check, Checksum;

void RHT03_Start()
{
RHT03_Data_Dir = 0;             // Configure as output
RHT03_Data = 0;                 // RHT03 data LOW
Delay_Ms(25);                   // 25ms LOW
RHT03_Data = 1;                 // RHT03 HIGH
Delay_us(30);                   // HIGH for 30us
RHT03_Data_Dir = 1;             // Configure as input
}

void RHT03_Read_Response()
{
while(RHT03_Data);              // Wait until data goes LOW
while(!RHT03_Data);             // Wait until data goes HIGH
while(RHT03_Data);              // Wait until data goes LOW
}

unsigned short Read_RHT03()
{
unsigned short num;
num = 0;
RHT03_Data_Dir = 1;             // Configure as input
for(i=0; i<8; i++)              // Do for all bits
{
while(!RHT03_Data);
Delay_us(50);                   // Wait 50us before data
if(RHT03_Data) num |= 1 << (7-i);
while(RHT03_Data);
}
return num;
}

void main()
{
        unsigned chat TxtHumidity[7], TxtTemperature[7];
        ADCON1=0x0F;                                    // Configure ports as digital
        UART1_Init(9600);                               // Initialise UART
        TRISB=1;
        Delay_Ms(2000);                                 // Wait 2 secs to stabilise RHT03

        while(1)                                        // Do Forever
        {
                RHT03_Start();                          // Send START pulse
                RHT03_Read_Response();                  // Wait for response
                RHT03_Byte1 = Read_RHT03();             // Read humidity upper byte
                RHT03_Byte2 = Read_RHT03();             // Read humidity lower byte
                RHT03_Byte3 = Read_RHT03();             // Read temperature upper byte
                RHT03_Byte4 = Read_RHT03();             // Read temperature lower byte
                Checksum = Read_RHT03();                // Read checksum

                Check = (RHT03_Byte1 + RHT03_Byte2 + RHT03_Byte3 + RHT03_Byte4);
                if (Check == Checksum)
                {
                        humidity = (RHT03_Byte1 << 8) | RHT03_Byte2;
                        temperature = ((RHT03_Byte3 & 0b01111111) << 8) | RHT03_Byte4;
                        if(RHT03_Byte3 & 0b10000000)temperature *= -1;
                        IntToStr(humidity, TxtHumidity);                // Convert to text
                        IntToStr(temperature, TxtTemperature);          // Convert to text
                        UART1_Write_Text(TxtHumidity);                  // Send humidity
                        UART1_Write_Text(TxtTemperature);               // Send temperature
                }
                Delay_ms(60000);                                        // Wait 1 minute
        }
```

4 YEARS FROM NOW

Hall 8, Fira Montjuïc
02-04 March 2015

4yfn@mobileworldcongress.com

4YFN | An event of MOBILE WORLD CAPITAL BARCELONA | GSMA MOBILE WORLD CONGRESS

Back for a second year, 4 Years From Now is an international programme presented by Mobile World Congress Barcelona and GSMA that brings together the best mobile start-ups and entrepreneurs with investors, accelerators, incubators and corporations from the mobile ecosystem.

For three days during Mobile World Congress, 4YFN will host inspiring talks, interactive workshops, cutting-edge exhibition and unique networking opportunities for 5,000+ attendees from 70 countries. 4YFN will feature:

- 150+ SPEAKERS
- 44 SESSIONS
- 40 WORKSHOPS
- 3,600 SQM OF EXHIBITION SPACE

4YFN PROGRAMME

Each day the programme will cover a different topic, lead by globally known experts in the field of entrepreneurship and innovation. Among them the following:

Monday, 02 March – Disrupted by Mobile
Designing for Touch
Context Matters
Hyper-local Services
Big Data
New Business Models
Privacy and Cybersecurity

Tuesday, 03 March – The Internet of Things
Connected Home
Quantified Self
Wearables
Rapid Prototyping
3D Printing
Product Design

Wednesday, 04 March – Digital Media
Content Strategy
Storytelling
Transmedia
New Entertainment
Alternative Education Models
Cross-Platform Perfection

SPEAKERS

The goal of 4YFN is to provide some of the most fascinating speakers in the mobile ecosystem to share their ideas on a variety of topics, including:

Mike Butcher, Editor At Large, TechCrunch
Weili Dai, President and Co-Founder, Marvell Technology Group
Dale Dougherty, Founder and Executive Chairman,Maker Media
Maelle Gavet, CEO, Ozon Holdings
Jimmy Maymann, CEO, The Huffington Post
François Moreau, CEO, Viaccess-Orca
Yossi Vardi, Chairman, 4YFN
Martin Varsavsky, CEO, FON
Be sure to check back often for updates. For complete details visit: **4yfn.com**

HOW TO PARTICIPATE

There are several different ways to participate:

ATTEND

4YFN takes place at Fira Montjuïc during Mobile World Congress and is open to all Congress attendees. Your MWC pass includes access to this three-day programme. There is a FREE shuttle to get you between Fira Gran Via and Fira Montjuïc so you can move between the two events without the expense of a taxi. For more details visit the **4yfn.com** website.

SPONSOR OR PARTNER

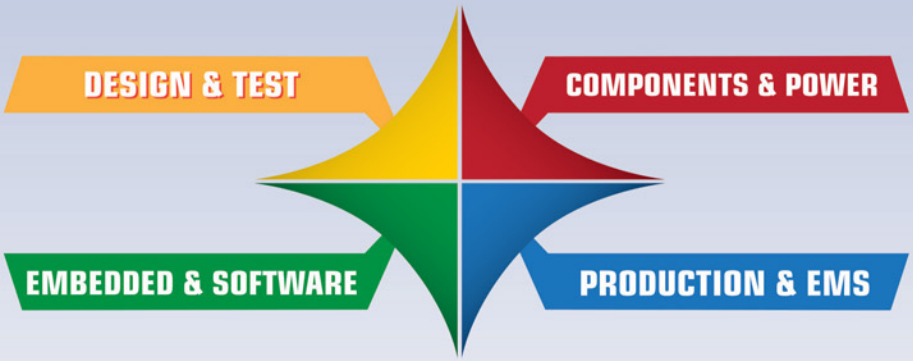
There are multiple opportunities to show your support of innovation and extend your presence to multiple MWC venues. Consider partnering as a Global, Track or Main Partner. More information on these sponsor and partner opportunities are available on the **4yfn.com** website.

EXHIBIT

There are a variety of exhibition packages to show your company, products or services to a highly relevant international audience. These packages offer a way to generate new contacts and build relationships with startups, investors, corporations and media. Packages offer everything from space only to enhanced solutions that include a booth and presence at MWC.

For additional information on exhibition opportunities, go to the **4yfn.com** website or send an email to: 4yfn@mobileworldcongress.com

FOUR INDUSTRY SECTOR EVENTS UNDER ONE ROOF



NATIONAL ELECTRONICS WEEK

Birmingham NEC - The Pavilion Hall
21st - 22nd April 2015

- PXI Show
- Test & Measurement Masterclass
- ECSN Technical Seminars
- Embedded Masterclass
- NPL & Smart Group Printing & Assembly Automatic Optical Inspection Experience
- Hand Soldering Competition

Book your stand space now! Call 01483 420 229

Don't miss the UK's most comprehensive electronics event

- Meet with suppliers, manufacturers and distributors
- Find out about the latest news and innovations in the industry
- Meet face to face with your contacts to secure the best business deals
- Meet new companies and experience their products first hand
- Get involved in the technical content and seminar program

Exhibitors include:

TECHNOLOGY, europlacer, HumiSeal, ELITE7, LCL ELECTRONICS, UNITEMP, PACE, O'DELL REWORK, Lighthouse, FLAIR, SAMSUNG TECHWIN, exception, esd, evolvi, TEKeurope, Cupio, MAC-PANEL, hitex DEVELOPMENT TOOLS, ISMOsys, JTAG TECHNOLOGIES, LPKF, TE, GEYER, Medi, TDK·Lambda, HCD, ECODAC, ROHDE&SCHWARZ, PEAKGROUP, pickering, DKL METALS LTD, BAE SYSTEMS INSPIRED WORK, ART, briton ems

Find out more:

www.new-expo.co.uk/newuk

Call 01483 420 229 or email info@new-expo.co.uk

Or keep in touch by following

twitter.com/NEW_expo facebook.com/NationalElectronicsWeek linkedin.com/groups/National-Electronics-Week-2684878

RS EXPANDS PORTFOLIO WITH INNOVATIVE ELECTRIC PAINT AND TOUCH BOARD

RS Components (RS) has entered into a distribution partnership with London technology company Bare Conductive over Bare Conductive's Electric Paint and Arduino-based Touch Board products, suitable for professional engineers and hobbyists alike.

Electric Paint is electrically-conductive, non-toxic, solvent-free and water-soluble paint, suitable for use as a liquid wire, a cold-soldering medium, or even a conductive adhesive.

The Touch Board microcontroller board integrates a capacitive touch chip, MP3 player, SD Card slot, Li-Po battery charger. There are 12 electrodes that can be connected directly to conductors, such as Electric Paint pads, to trigger sounds via the MP3 player or other functions such as wireless communication or motor control added using an Arduino expansion shield.

uk.rs-online.com

GESTIC CONTROLLER ENABLES ONE-STEP 3D GESTURE RECOGNITION DESIGN-IN

Microchip has announced the second member of its award-winning and patented GestIC family - the MGC3030 3D gesture controller. It features simplified user-interface options focused on gesture detection, enabling true one-step design-in of 3D gesture recognition in consumer and embedded devices. Housed in an easy-to-manufacture SSOP28 package, the MGC3030 expands the use of highly sought-after 3D gesture control features to high-volume cost-sensitive applications such as toys, audio and lighting.

The simplicity of gesture-detection integration offered by the MGC3030 is also achieved through Microchip's free, downloadable AUREA Graphical User Interface (GUI) and easily configurable general-purpose IO ports that even allow for host MCU/processor-free usage. The MGC3030's on-chip 32-bit digital signal processor executes real-time gesture processing, eliminating the need for external cameras or controllers for host processing and allowing a faster and more natural user interaction with devices.

www.microchip.com

NEW BUCK REGULATOR ADDED TO AUTOMOTIVE-GRADE REGULATOR ICs

The new A8590 buck regulator from Allegro MicroSystems Europe is the latest addition to the company's industry-leading family of automotive-grade AEC-Q100 qualified regulator ICs.

The device has been designed to provide the power-supply requirements of next-generation car audio and infotainment systems, and provides all the control and protection circuitry for a 3A regulator, which withstands the rigours of a wide automotive battery input voltage range. The A8590 can also be used in cluster and centre stack applications and in advanced driving assistance systems.

The A8590 employs pulse frequency modulation to draw less than 50µA from a 12V input while supplying a 3.3V/40µA output. After start-up, the A8590 operates down to an input voltage (falling) of at least 3.6V and maintains ±1% output voltage accuracy.

www.allegromicro.com

COMPREHENSIVE EMC FILTER SERVICE FROM AERCO

As part of its expanding value added service, Aerco's agreement with Oxley components division allows the Horsham-based electronics component distributor to offer a comprehensive EMC service that helps customers solve complex EMC design issues thus removing the risk of susceptibility of systems to electromagnetic interference. This is a common problem faced by many design engineers and as part of the service Aerco stocks standard EMC products such as discrete and multi-line EMI filters, ceramic planar capacitor arrays and arrays of discrete filters available in threaded, solder, press fit and surface-mount styles. Custom designed versions to suit specific requirements are also supplied.

Aerco and Oxley are able to offer valuable advice and provide a comprehensive design-in service for filtering solutions.

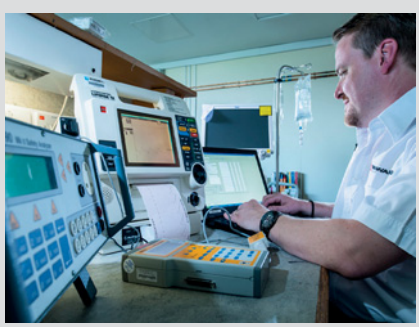
www.aerco.co.uk

CALIBRATIONHOUSE SERVICE EXPANSION

Calibrationhouse, a specialist UKAS accredited calibration service for electrical and electronic test and measurement equipment has expanded its operations to meet growing demand. The company invested in extended workshop facilities and new test technology, as well as recruited additional service and calibration engineers at its County Durham headquarters.

Calibrationhouse now has new test, measurement and analysis equipment including infrared thermometry and thermal imaging cameras, luminance (lux) meters, specialist audiology equipment and different types of medical electronic equipment. In addition, its team of highly trained and qualified engineers will provide specialist UKAS calibration services at customer premises.

www.calibrationhouse.com



ELECTROTESTEXPO 2015 PCB TEST EXHIBITION AND SEMINAR

Now enjoying its sixth consecutive year of free-to-attend events, ElectroTestExpo will commence its unique combination of drop-in tabletop exhibition and seminar on 25th March at one of the UK's most unique attractions – the National Space Centre in Leicester.

There will be a programme of short talks by industry experts, covering a range of topics in an easily accessible, relaxed environment. Among the confirmed exhibitors are Tektronix, AmFax, JTAG Technologies, Aeroflex (Cobham Wireless), TestWorks, Prism Sound, Aster, Test Solutions Limited (TSL), MAC Panel, Pico Technology, TTi and Pickering Interfaces.

The event is open to all electronic engineering professionals but numbers are limited so register early at: **www.electrotestexpo.co.uk**

NEW, LOW-PROFILE POLYMER CAPACITOR BY PANASONIC

Panasonic Automotive and Industrial Systems has introduced a new low-profile version of its SP-Cap range of speciality conductive polymer aluminium capacitors. Measuring just 0.9mm above the PCB, the devices (LR & SR series) are rated from 2V to 6.3V, with capacitance values of 68-220µF. Capacitance tolerance is ±20% (120Hz/+20degC).

"Thanks to their ultra-low ESR values, polymer capacitors have a low impedance near their resonance point, which reduces AC ripple in power circuits," said Melanie Raimann, European Product Manager for Polymer Capacitors at Panasonic. "Polymer capacitors suffer no capacitance drifts due to temperature changes and DC bias, so they remain stable over time."

Panasonic has also upgraded the ripple current rating of the SP-Cap range, which can now handle up to 10.2Arms at 45degC, two and a half times higher than previous devices. Devices are also now available with a higher 20V working range and some of them now feature an extended life to 2000 hours.

A catalogue detailing all Panasonic's new SP-Cap polymer aluminium capacitors can be downloaded free from:

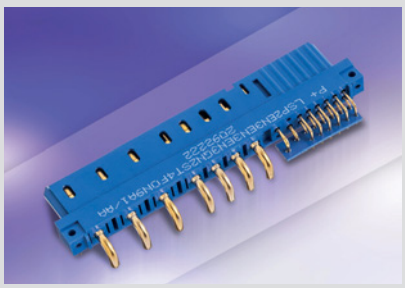
http://industrial.panasonic.com/jp/i/29880/SPC_E/SPC_E.pdf

SCORPION POWER/SIGNAL CONNECTORS FOR HI-REL APPLICATIONS

The Positronic's Scorpion modular signal power connector family, including the low profile version, is now available at Astute Electronics. Positronic uses modular tooling that enables the quick turnaround of a very large number of customer-specified contact variants up to 100mm long, yet the moulding process yields a one-piece insulator.

Power options include 60, 40 and 30A contacts, or 55 and 12A in the low 8.2mm profile version. Contact resistance is as low as 1 milliohm for standard conductivity contacts and 0.7 milliohms for high conductivity contacts. 3A signal contacts are available, and blank module options enable creepage and clearance specification to be made. Contact terminations include board-to-board, board-to-cable, cable-to-cable and panel mount options.

www.astute.co.uk



AWS ELECTRONICS DEDICATED TO TS 16949 AUTOMOTIVE QUALITY ACCREDITATION

AWS, one of Europe's leading specialist contract electronics manufacturers, has won new orders in the extremely competitive European Automotive sector, working directly for a large global Automotive Tier 1 company. The project has required significant investment in new equipment and a new production hall dedicated to automotive projects. With the order, AWS will now seek full accreditation to the ISO/TS 16949 technical specification. This sets out the quality system requirements for the design/development, production, installation and servicing of automotive related products.

The new processes and equipment is being set up and AWS is initially operating under a 'letter of conformity' with stage audits during 2015 as per the normal process steps to TS 16949 full accreditation.

"With the investment we have made, both in the UK at our facility in Slovakia, we are well-placed to support the automotive market. Our plants are within easy reach of at least three major car makers," said AWS CEO Paul Deehan. "We are seeing a lot of reshoring work – contract work coming back to Europe from South East Asia. Our Slovakia investment means that we can be cost-competitive."

www.awselectronicsgroup.com

LOW POWER VOICE DETECTION AND RECOGNITION SOLUTIONS FOR MOBILE DEVICES

Lattice Semiconductor is now offering human voice detection and command recognition IP for smartphones and other handhelds for the growing Internet of Things (IoT) category of devices. These IPs are implemented in the iCE40 family of mobile FPGAs, enabling manufacturers to improve the user experience of their mobile devices with new voice activation capabilities and by maximizing battery life by minimizing false wake-up triggers to the processor.

"Accurate and reliable voice detection and command recognition is important for today's smartphones and other mobile devices, but sound processing with a power hungry processor quickly drains batteries when random sounds are misinterpreted as human speech," said Joy Wrigley, Product Line Manager, Lattice Semiconductor. "Further, user experience is diminished when devices do not properly capture commands. "

The rapidly expanding number of IoT devices is projected to reach 26 billion by 2020, according to the analyst firm Gartner. Lattice's new solutions are ideal for a growing number of these IoT devices, which must minimize power consumption while maximizing sensor reliability and performance.

www.latticesemi.com

SMALLEST AND THINNEST FUSED UNDERTAB HIGH CV TANTALUM SMD CHIP CAPACITORS

AVX Corporation has released a new series of fused high CV tantalum SMD chip capacitors with undertab terminations. The new F98-AS1 Series capacitors feature a proprietary lead-frameless structure with precise dimensions and low stress packaging, an internal thin-film fuse that protects against short circuits, and well-established undertab termination technology that enables high volumetric efficiency and high PCB assembly density.

Currently available in a 0805 (2012 metric) S case with four ratings (22F/10V, 33F/10V, 10F/16V, and 1F/35V) and a 0.9mm maximum height, the F98-AS1 Series is the smallest and thinnest SMD fused tantalum product currently available on the market. As such, the series is ideal for use in a wide variety of applications in which safety and size are a primary concern.

www.avx.com

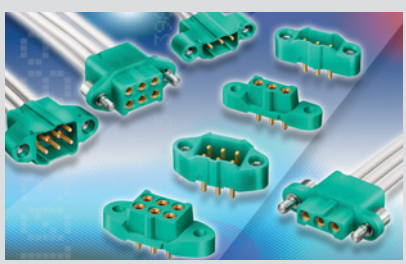
NEW 10A HI-REL POWER CONNECTOR HANDLES UP TO 175DEGC

Harwin has launched a family of high-density power connectors that can handle currents up to 10A. Based on a 3mm pitch, the new M300 connectors are designed for rugged environments and withstand twice the number of operations as older generation products.

The M300 connectors feature a 4-fingered Beryllium Copper female contact which delivers superb electrical and mechanical performance. Devices suit 18-22AWG applications and are designed for use in temperatures of between -65 and +175degC, rated for 1000 operations. They pass shock (EIA-364-27: 100g 6ms No Discontinuity >1µs and vibration (EIA-364-28 10g No Discontinuity >1µs) testing. Jackscrews are available for extra security.

Other features include keyway polarisation and identification of the #1 position, and the connector bodies are moulded in environmentally-friendly material.

www.harwin.co.uk



EMBEDDED OFFICE EXTENDS THE RANGE OF ITS CERTIFICATION KITS

Embedded Office, a company for embedded systems that specialises in safety-critical applications, has extended the range of its Cert-Kits for a series of new microcontrollers. The range now also supports ARM 9, C166, C166SV2, Cortex A9, Cortex M3, Cortex M4F, Cortex R4F, PPC e200 and PPC e500. In addition to the certificate and the documentation for the certification, the Cert-Kits also comprise an executable system along with a complete validation software solution.

The system supplied in the Cert-Kits serves primarily for verifying whether the pre-certified source code of the real-time kernel has been transferred correctly from the customer and has generated the real-time kernel with the correct configuration. To this end, the validation software generates a report on the respective evaluation board, which serves as the documentation for this step.

www.embedded-office.de

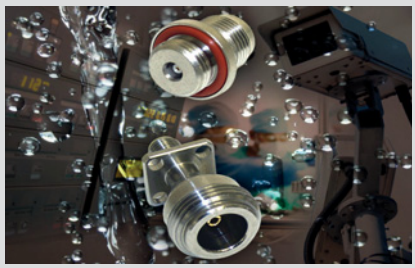
INTELLICONNECT EXTENDS PISCES RANGE OF WATERPROOF CONNECTORS

Intelliconnect (Europe) Ltd has extended its Pisces range of IP68 waterproof connectors to include additional connector and cable termination options. The range now includes SMA, TNC and N Type cable plug options which may be connected to a wide variety of cables including many LMR, RG, Semi-Rigid and Semi-Flexible cable types.

These product enhancements extend the range of potential applications for Pisces connectors to include 75-ohm variants for video camera security applications, environmental monitoring ocean buoys, traffic cameras (ANPR), coastguard/HM customs patrol boats, military radios/communication systems, environmental monitoring and water management and vehicle tracking.

In addition, Intelliconnect's standard range includes IP67- and IP68-rated interconnect solutions for harsh environments including N Type, SMC, SMA, TNC, Push-Pull and ABMS (harsh environment MCX).

www.intelliconnect.co.uk



CONFERENCE PROGRAMME ANNOUNCED FOR AVIATION ELECTRONICS EUROPE

Aviation Electronics Europe, which will take place on 25th-26th March 2015 in Munich, Germany, has launched the conference programme for the event, focusing on key industry topic areas, including the Single European Sky initiative.

Following the keynote session, which will see opening addresses from the European Commission and European Aviation Safety Agency, the conference discussions will look at Avionics in SESAR, the progress of the Single European Sky initiative, and the impact of avionics on air traffic management systems, among others.

In addition there will be panel discussions, looking at the Impact of Performance Based Navigation, Standardisation and Certification of software and systems, analysis and implications in compliance of DO-178B/C - ED-12B/C and so on.

www.ae-expo.eu

CONGATEC LAUNCHES COM EXPRESS AND THIN MINI-ITX FOR INDUSTRIAL RELIABILITY

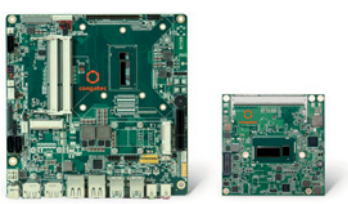
Congatec has expanded its product range with 5th generation Intel Core processor platform up to Intel Core i7-5650U on COM Express Computer-On-Modules and Thin Mini-ITX motherboards. The single-chip processors feature low power consumption of just 15W TDP.

Built on Intel's new 14nm process technology, the 5th generation Intel Core processor is designed to prove excellent graphics and performance, supporting the next generation Congatec's COM Express and Thin-Mini-ITX boards for Internet of Things (IoT) solutions, while maintaining compatibility with previous generations.

New Intel HD Graphics 5500 and 6000 delivers stunning and responsive visuals in 5th generation Intel Core processors, including Ultra HD 4k display and additional codec support. Enhanced security and manageability features help to drive down total cost and risk, protecting data and preventing malware threats.

Embedded World: Hall 1, Booth 358

www.congatec.com



POWER CONNECTOR DELIVERS UP TO 300A AT SINGLE POINT OF CONTACT

Amphenol Industrial Products Group now offers a new, high-current PCB power connector that enables a single-point power delivery of 150A, 200A and 300A in less than one linear inch of a PCB edge.

Amphenol's RadFin power connectors use RADSOK contact technology to meet the increasing power requirements of printed circuit boards and the need for smaller board footprints.

Ideal for use by data centre equipment manufacturers and power supply manufacturers, as well as in energy storage systems, these low-profile power connectors offer flexible power delivery to PCBs enabling a variety of layout choices.

The heat dissipating design of RadFin dramatically helps reduce T-rise with minimal air-flow required.

The space-saving RadFin is offered in right angle mating planes as single-point contact terminals, making them versatile when component placement is crucial.

www.amphenol-industrial.com

T&M INDUSTRY'S FIRST GRAPHICAL SAMPLING DIGITAL MULTIMETER

Keithley Instruments introduced Model DMM7510 7½-Digit Graphical Sampling Multimeter, the first of a new class of digital multimeters that integrates a high accuracy digital multimeter, a digitizer for waveform capture and a capacitive touchscreen user interface.

The Model DMM7510 is designed to give confidence in the accuracy of results, the ability to explore measurements further, and intuitive touchscreen operation. This user interface continues the company's "Touch, Test, Invent" design philosophy that lets users learn faster, work smarter and invent easier.

The Model DMM7510 provides capabilities such as a five-inch touchscreen display for more information displayed simultaneously, lower swipe screen speeds to access often-used features, and the storing of test results in any of the data buffers, displayed in graph, histogram, or numerical/ datasheet form, among others.

www.keithley.com

NEW! PS12MK /PS20MK Series IP67 rated power supplies

Features

- 90-264VAC universal AC input
- Compact dimensions PS12MK 56 x 39 x 26mm and PS20MK 64 x 47 x 28mm
- PS12MK 12 Watts & PS20MK 20 Watts
- Single DC outputs of 5, 9, 12, 15 or 24V
- IP67 fully encapsulated and waterproof
- Fixing holes for wall or chassis mounting
- Input and output connectors optional
- No Load Power Consumption ≤0.3W max
- EN60950 & EN55022 safety & EMC standards
- Ideal for CCTV or LED applications
- Class II safety, no earth connection required

POWER SOLVE

www.powersolve.co.uk
Email: sales@powersolve.co.uk Tel: 44-1635-521858