July 2015
Volume 121
Issue 1951
£5.20

www.electronicsworld.co.uk

Electronics WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Toshiba accelerates the development of sports watch applications

INSIDE:

T&M SUPPLEMENT

Starting on page 45 of this issue

Technology
Skyrmions will be used for the next generation electronic devices

Special Report
Theoretical and practical approach to system design

Products
Latest connectors, intelligent devices and power supplies

TELEDYNE LECROY
Everywhereyoulook™

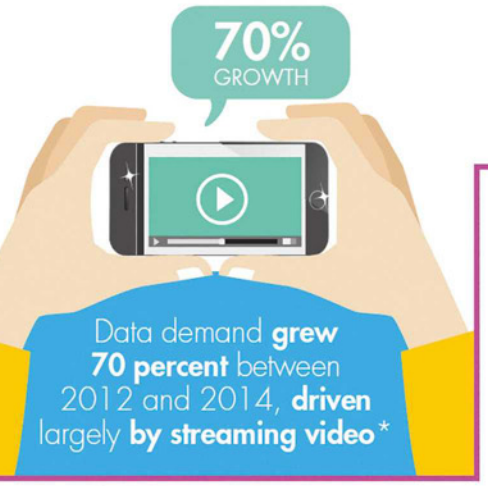
Premium Performance – Economy Price

WaveSurfer 3000

200 MHz – 750 MHz
4 GS/s, 10 Mpts
10.1" Touch Screen

teledynelecroy.com/europe/ws3000

From € 3.140

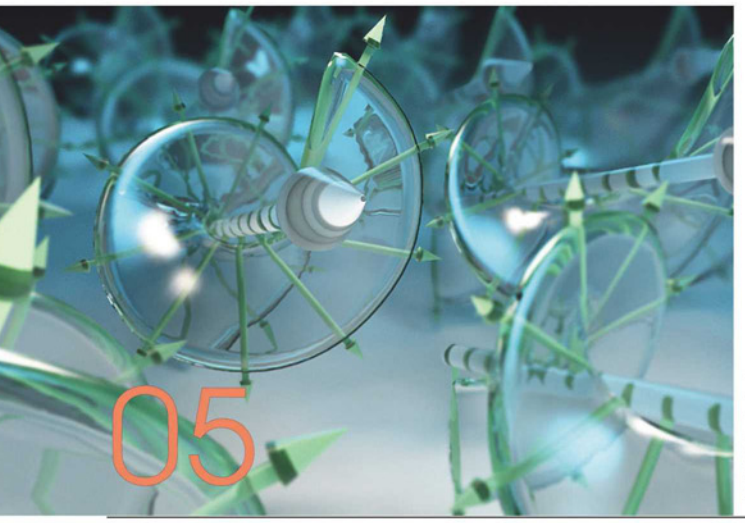


By 2019, **more than half** of all wireless data will be **video***

10

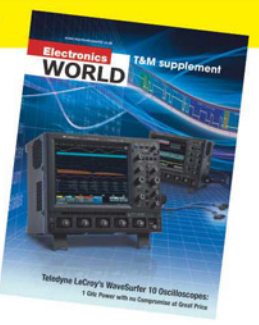
Cover supplied by **TOSHIBA ELECTRONICS EUROPE**
More on pages 16-17

REGULARS



FEATURES

45



The World's Largest Selection of Electronic Components Available for Immediate Shipment!™

We Source What's Inside YOUR DESIGN

FREE SHIPPING ON ORDERS OVER £50!*

0800 587 0991 • 0800 904 7786

DIGIKEY.CO.UK

Digi-Key® ELECTRONICS

1,000,000+ PRODUCTS IN STOCK | 650+ INDUSTRY-LEADING SUPPLIERS | 100% AUTHORIZED DISTRIBUTOR

*A shipping charge of £12.00 will be billed on all orders of less than £50.00. All orders are shipped via UPS for delivery within 1-3 days (dependent on final destination). No handling fees. All prices are in British pound sterling and include duties. If excessive weight or unique circumstances require deviation from this charge, customers will be contacted prior to shipping order. Digi-Key is an authorized distributor for all supplier partners. New product added daily.

ecia MEMBER ecsn member CEDA

TRENDS THAT IMPACT MATERIAL SELECTION FOR LED LIGHTING

LED lighting offers longevity, lower power consumption and design choices. It has been promoted as a greener solution because it creates no mercury waste, is energy efficient and boasts a long life. It has revolutionized the lighting world, becoming the dominant light-form in nearly all commercial and residential applications, and likely to remain so in years to come.

The trends outlined here are important to recognize in LED lighting. They not only drive application development but impact the materials chosen to produce the final product.

The Trends

1. **Swift product cycles.** Innovation has never been quicker. New products enter the market in as little as every six months. Materials suppliers have to be constantly aware of new developments in the industry and ready to respond quickly with new and innovative materials to meet the demands of an evolving market space.
2. **Thinner gauge materials** to reduce material consumption and/or improve flux efficiencies of light sources. For OEMs, maximizing the amount of light output through lenses, covers and optics is a key driver. To accomplish this, thinner gauge lens and covers are used. This requires material suppliers to be innovative and develop materials with the best optical properties (light-transmission/light-diffusion) while also maintaining UL certification and excellent mechanical properties.
3. **Design freedom and lighter-weight parts.** LEDs as small, solid-state, robust light sources offer designers the opportunity to revolutionize the design of light forms. Materials to meet these needs must be easily fabricated by multiple processing methods. Thermoplastic resins such as polycarbonate-based materials offer superior processing and can be moulded into complex shapes and forms at a substantially lighter weight than traditional materials such as glass and metal.
4. **Cost savings.** Lighting OEMs constantly look to reducing production costs. Working closely with the material makers can help them reduce costs – this may involve higher quality raw materials, local sourcing and developing new materials to meet the requirements for a thinner gauge. Local sourcing minimizes shipping costs too.
5. **Greener technology.** LED lighting offers a more environmentally-friendly approach than traditional lighting due to the energy savings of efficient light sources and the absence of harmful substances such as mercury. Polycarbonate-based solutions reduce the amount of material required due to their excellent properties at very thin gauges and, also, thermoplastic materials can be recycled.

Materials

The materials chosen for LED lighting applications impact a producer's ability to achieve key LED benefits. Glass and acrylics have traditionally been used but, today, plastic – specifically polycarbonate – is quickly becoming the preferred material, notably in four main application areas: coverings, housing and enclosures, LED reflectors and heat sinks.

Polycarbonate is unique in that it can balance mechanical properties to exacting requirements, helping achieve the following top priorities:

1. Durability

Because the LED light source (a solid-state semiconductor) is more robust than traditional incandescent options, the materials covering it should be at least as resilient as the light source itself. Polycarbonate is much more impact-resistant and less prone to breakage than other available materials. Often used for riot shields, aircraft canopies and impact resistant panels, polycarbonate has outstanding toughness, even over a wide temperature range.

2. Optical properties

The benchmark of LED light transmittance is the absolute clarity provided by glass; however, optically, an even distribution of visible light is desirable. This means carefully balancing clarity and diffusion: materials must either allow the LED light source to shine directly through a surface for maximum brightness or provide uniform light distribution to create a more diffused effect. Polycarbonate allows for light transmission greater than 90% for transparent grades, and polycarbonate resins containing a light diffusion additive can help achieve excellent light uniformity over the part's entire surface.

3. Design flexibility

LED lighting offers manufacturers creative freedom in product design. Unlike with traditional incandescent lighting, plastics used for housing or covering the LED source can be formed into countless shapes and sizes through injection moulding, injection blow moulding, profile extrusion and sheet extrusion/thermoforming processes. In addition, parts can be down-gauged for weight, energy and cost savings.

4. Ignition resistance

Ignition resistance refers to safety standards based on the plastic's flammability and how the material, at a certain thickness, will burn. Operating at temperatures as high as 80-110°C, these applications, no matter the part, all contain materials that can ignite when in contact with electrical current or heat sources. So it is essential that plastics used in lighting applications contain the proper additives to resist ignition. For ignition resistant applications (UL 94 V-0 and 5VA), polycarbonate is the most cost-effective replacement for glass.

Bill Marshall, account manager at Trinseo Performance Plastics/Consumer Essential Markets, is a 25-year veteran chemist, focusing on the LED lighting industry. Trinseo is a global materials company (www.trinseo.com)

EDITOR: Svetlana Josifovska
Tel: +44 (0)1732 883392
Email: svetlanaj@sjpbusinessmedia.com

SALES: Sunny Nehru
Tel: +44 (0)20 7933 8974
Email: sunnyn@sjpbusinessmedia.com

DESIGN: Tania King
PUBLISHER: Justyn Gidley

ISSN: 1365-4675

PRINTER: Buxton Press Ltd

SUBSCRIPTIONS:
Subscription rates:
1 year: £62 (UK);
£89 (worldwide)
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com

SJP business media
2nd Floor,
52-54 Gracechurch Street,
London, EC3A 0EH

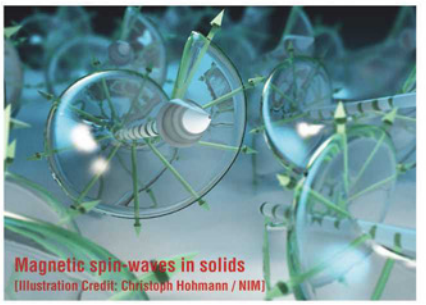
Follow us on Twitter
@electrowo

Join us on LinkedIn

RESEARCHERS LAY THE FOUNDATION FOR FUTURE ELECTRONIC COMPONENTS WITH PURPOSE-DESIGNED PROPERTIES

Magnetic vortex structures, called skyrmions, could in the future store and process information very efficiently and form the basis for high-frequency components, thanks to the efforts of a team of physicists from Technische Universität München (TUM), the University of Cologne (Germany) and the École Polytechnique Fédérale de Lausanne (Switzerland). For the first time, the team has succeeded in characterizing the electromagnetic properties of insulating, semiconducting and conducting skyrmion materials and developed a unified theoretical description of their behaviour.

More than six years ago, physicists at TUM discovered extremely stable magnetic vortex structures in a metallic alloy of manganese and silicon. Since magnetic vortices are microscopic and easy to move, computer components may need 10,000 times less power with this technology than today to store much larger volumes of data. Also, the typical resonance frequencies of the skyrmions are in the microwave range – the frequency



Magnetic spin-waves in solids
[Illustration Credit: Christoph Hohmann / NIM]

range of mobile phones, Wi-Fi and many types of microelectronic remote controls. Thanks to the robustness of the magnetic vortices and their ease of excitability, skyrmion materials could also be the basis for highly-efficient yet very small microwave transmitters and receivers.

"With this theory, we have laid an important foundation for further developments," said Professor Dirk Grundler, Chair of Physics at TUM. "While the wavelength of electromagnetic microwaves typically lies in the range of centimeters, the wavelengths of the magnetic spin waves, so-called magnons, are 10,000 times shorter. In the area of microelectronics, much more compact or even entirely new devices could be developed from magnetic nanomaterials such as the skyrmion materials, with the specific properties we need for functional devices."

In addition to the material itself, its shape also significantly influences the electromagnetic properties of the device. The researchers' newly-developed theory can predict which form produces the best properties for which material.

"Chiral magnetic materials promise a lot of new functionalities with an interesting interplay of electronic and magnetic properties," said Dr Markus Garst from the University of Cologne. "But for all applications, it is essential to predict the possibilities and limitations of various materials. We have come a lot closer to achieving this goal."

The work was funded by the European Research Council (ERC Advanced Grant), the Deutsche Forschungsgemeinschaft (TRR 80, SFB 608 and Nanosystems Initiative Munich, NIM), as well as the TUM Graduate School.

PRIVACY CONCERNS OVER MODERN-DAY DEVICES' SIGNAL RADIATION

Researchers at UK-based security services consultancy Context Information Security have demonstrated how easy it is to monitor and record Bluetooth Low Energy (BLE) signals transmitted by many mobile phones, wearable devices and iBeacons – including the iPhone and some fitness monitors, raising concerns about privacy and confidentiality.

"Many people wearing fitness devices don't realise that they are broadcasting constantly and that these broadcasts can often be attributed to a unique device," said Scott Lester, senior researcher at Context. "Using cheap hardware or a smartphone, it could be possible to identify and locate a particular device that may belong to a celebrity, politician or senior business executive within 100 metres in the open air. This information could be used for social engineering, as part of a planned cyber attack or for physical crime by knowing peoples' movements."

BLE was released in 2010 specifically for a range of new applications that rely on constantly transmitting signals without draining the battery. Like other network protocols BLE relies on identifying devices by their MAC addresses, but whilst most BLE devices have a random MAC address, Context researchers found that in most cases it doesn't change. Sometimes the transmitted packets also contain the device's name, which may be unique, or even give the name of the device's user, such as "Scott Mill's Watch" for example.

The Bluetooth Special Interest Group (SIG) has predicted that "by 2018, more than 90% of Bluetooth-enabled smartphones are expected to be Smart Ready devices", supporting BLE; whilst the number of Bluetooth-enabled cars is also predicted to grow to over 50 million by 2016.

iBeacons, which also transmit BLE packets in order to identify a location, are already used in Apple Stores to tailor notifications to visiting customers, while flight operators BA and Virgin use iBeacons with their boarding pass apps to welcome passengers walking into the lounge.

The current version 4.2 of the Bluetooth Core Specification makes it possible for BLE to implement public key encryption and keep packet sizes down, whilst also supporting different authentication schemes, but this would reduce battery life and increase application complexity.

"While the ability to detect and track devices may not present a serious risk in itself, it certainly has the potential to compromise privacy and could be part of a wider social threat. It is also yet another demonstration of the lack of thought that goes into security when companies are in a rush to get new technology products to market," added Lester.

From 50 MHz to 4 GHz: Powerful oscilloscopes from the T&M expert.

FROST & SULLIVAN 2015 BEST PRACTICES AWARD
Global Oscilloscopes Competitive Strategy Innovation and Leadership Award

Fast operation, easy to use, precise measurements –
That's Rohde&Schwarz oscilloscopes.

R&S®RTO: Analyze faster. See more. (Bandwidths: 600 MHz to 4 GHz)
R&S®RTE: Easy. Powerful. (Bandwidths: 200 MHz to 1 GHz)
R&S®RTM: Turn on. Measure. (Bandwidths: 350 MHz and 500 MHz)
HMO3000: Your everyday scope. (Bandwidths: 300 MHz to 500 MHz)
HMO Compact: Great Value. (Bandwidths: 70 MHz to 200 MHz)
R&S®HMO 1002: Great Value. (Bandwidths: 50 MHz to 100 MHz)

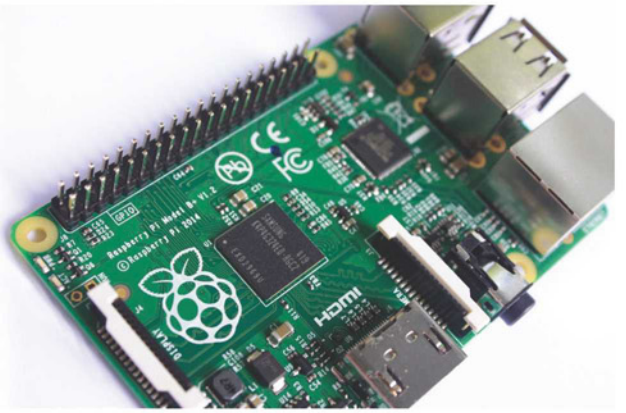
All Rohde&Schwarz oscilloscopes incorporate time domain, logic, protocol and frequency analysis in a single device.

Take the dive at www.scope-of-the-art.com/ad/all

ROHDE&SCHWARZ

THIS SERIES PRESENTS THE RASPBERRY PI SINGLE-BOARD COMPUTER, ITS FEATURES AND BENEFITS, AND HOW TO USE IT FOR VARIOUS PROJECTS

Interfacing With Hardware



BY **ALEX BRADBURY** AND **BEN EVERARD**

Before getting too far into the details of circuitry, let's create a simple circuit. You'll need a breadboard, an LED, a 220-ohm resistor and some way of connecting the GPIOs to the breadboard (either female-male jumpers or a Pi Cobbler). This circuit lets you turn an LED on and off simply with Python, an easy to use and powerful programming language.

LEDs are much more power-efficient than incadescent light bulbs, and don't get too warm when running normally. They have a positive and a negative leg – the base of a typical LED is round with a small flat section on one side, which is normally positioned next to the negative leg.

The series resistor is there to limit the power flowing through the circuit. As a general rule, there should always be at least one resistor of at least 220 ohms in an LED circuit; otherwise, you risk damaging the Pi and other components.

In this circuit, the resistor doesn't have to be 220 ohms; anything between 220 and 470 should be fine (with higher values the LED will be dimmer). Resistors are colour-coded to indicate their values. There are typically four or five bands of colour (most everyday resistors have four) three for the value, and two (silver or gold) for the tolerance.

The resistor and LED should be connected on the breadboard as shown in Figure 1, with the LED's positive leg connected to the resistor.

To make sure the circuit works, connect the wire from the resistor to one of the 3.3V pins on the Raspberry Pi (see Figure 2), whilst the lead coming from the LED should connect to a ground pin. If it's connected properly, the LED will light up.

This, though, is just using the Raspberry Pi as a power source. To be able to control the circuit with Python, you will need an RPi.GPIO module. First make sure you have pip (a software tool to help access modules) installed with the following command (in LXTerminal, not in Python):

sudo apt-get install python3-pip

Then get the library with this command (also in LXTerminal):

sudo pip-3.2 install RPi.GPIO

The GPIO pins access the Raspberry Pi at a low level, and because of this, Python scripts won't run normally. Instead, you will need to run them with superuser permissions. This sounds fancy, but it is just prefixing commands with sudo. So, for example, if you want to run a script in LXTerminal, you need to run:

sudo python3 your-script.py

Alternatively, start a Python shell with:

sudo python3

Or start IDLE 3 with superuser permissions by running the following in LXTerminal:

sudo idle3

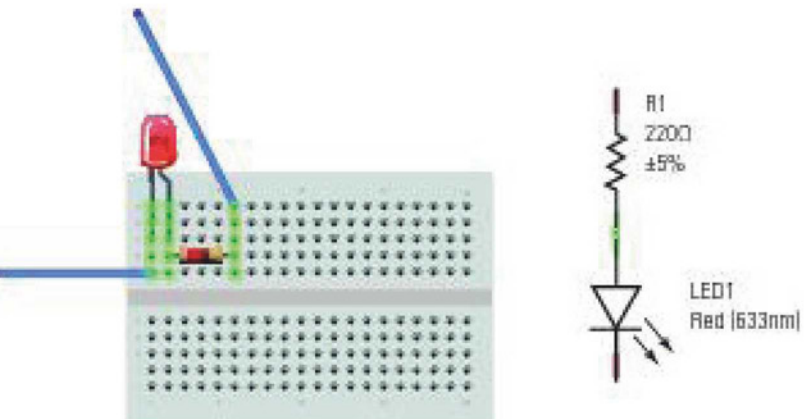


Figure 1: Circuit diagrams: on the left are the connections; on the right, the way they are linked

Once RPi.GPIO is installed, connect the circuit to one of the GPIO pins. Disconnect the pin from 3.3V and connect it to pin 22. Once this is done, open a Python session (don't forget sudo!) and enter the following:

```
>>> import RPi.GPIO as GPIO
>>> GPIO.setmode(GPIO.BCM)
>>> GPIO.setup(22, GPIO.OUT)
>>> GPIO.output(22, True)
>>> GPIO.output(22, False)
>>> GPIO.output(22, True)
>>> GPIO.output(22, False)
```

As you can see, setting the pin to True turns the LED on, while False turns it off. Figure 3 shows the running circuit.

Protecting The Pi

In general, it's very hard to physically damage a computer with programming. You might be able to corrupt some files (although even this is rare) but, generally, no matter how much you mess things up, simply reinstalling the operating system will sort things out. However, when you're adding things to the GPIO, you're sending power directly to the CPU, which can damage it.

The two properties of electricity that can cause problems are voltage and current. With voltage, the rule is simple and important: never connect more than 3.3 volts to a GPIO pin. A lot of hobby electronic components are designed to run at 5V because other processors run at that voltage. However, if you connect these directly to the Pi, the overvoltage can cause irreparable damage to the board. The result is known as "bricking the Pi", because afterward its only use is as a brick.

You'll notice that the Raspberry Pi has two 5V pins. These are only there to power external circuits that don't come back to the Pi. If you need to connect a 5V device to the GPIO ports, you'll need a logic-level converter, which converts 5V signals into 3.3V and vice versa, available for a few pounds.

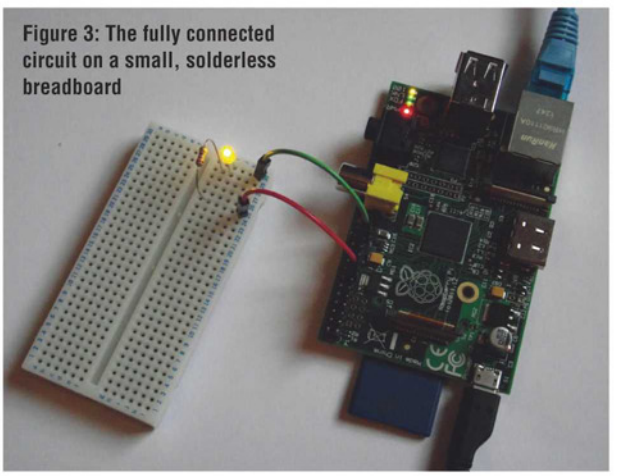


Figure 3: The fully connected circuit on a small, solderless breadboard

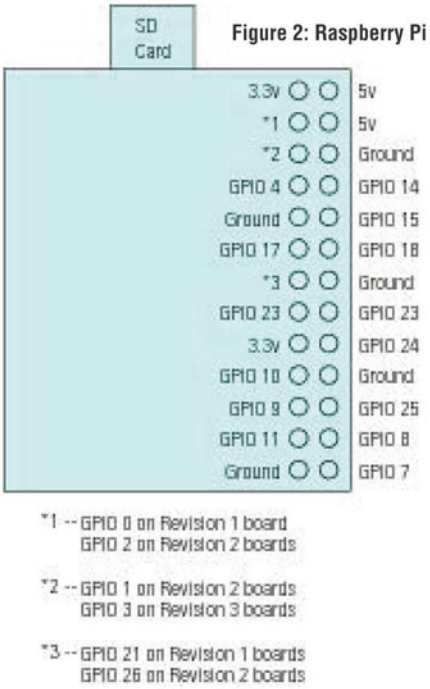


Figure 2: Raspberry Pi pin layout

When using a Raspberry Pi, you must never draw more than 16mA from any one pin, or 50mA from all the GPIO pins combined. That means that you can light up only three LEDs at a time (or use more resistance to decrease the amount of current each one draws). It also means that you should never connect a GPIO pin to a circuit unless there is at least 220 ohms of resistance in it. If you're ever unsure about resistors, always err on the side of caution and use larger values than called for.

Technically, this isn't exactly correct because LEDs are a bit different from many other components.

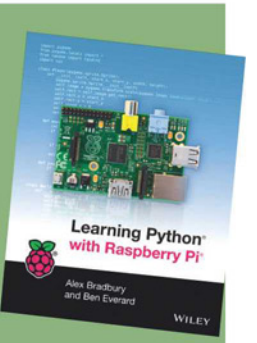
This circuit will draw less power than that. However, unless you understand voltage drop on LEDs, it's best to stick with these guidelines. If you need more current, or just want to protect your Pi in case you accidentally draw more current, use an expansion board with buffered input/output ports such as the PiFace, or alternatively, use a buffer-integrated circuit (IC or chip) to protect the GPIO ports. ●

This column is an edited extract from 'Learning Python With Raspberry Pi' book by Alex Bradbury and Ben Everard

LEARNING PYTHON WITH RASPBERRY PI

'*Learning Python With Raspberry Pi*' book by Alex Bradbury and Ben Everard is published by Wiley as a paperback and an e-book (ISBN: 9781118717059).

We have a couple of copies to give away, so to be in with a chance, write to the Editor at svetlanaj@sjpbusinessmedia.com, specifying the name of the book in the subject field.



The State of LTE

BY **RAY BUTLER**

Since the first Long Term Evolution (LTE) commercial service in 2009, there are now over 400 networks offering commercial LTE service worldwide, according to the industry trade organization 4G Americas. LTE-Advanced, a technology standard that improves the performance of LTE, has been deployed in over 50 markets worldwide. North America led the way with the first broad coverage of LTE commercial networks, and now South Korea and Japan have the highest deployment rates. Wireless operators in many parts of the world have just begun, or are about to begin, rolling out LTE.

In more mature markets, operators are deploying advanced features such as carrier aggregation, voice over LTE (VoLTE) and LTE-Advanced. Carrier aggregation enables operators to combine data bandwidth from different radio frequency (RF) carrier signals for higher peak bandwidth. VoLTE is like voice over IP but is integrated into the LTE standard and provides voice capability over a data-only network; VoLTE enables high-definition voice capability.

The next steps in the LTE evolution will likely be wireless operators deploying more networks, activating new features and adding capacity to existing networks through re-farming spectrum and re-using new spectrum from 2G and 3G wireless services. This capacity growth is enabled through aggregating more carriers in the vacated frequency bands.

> Did you know?... Just 1dB of passive inter-modulation can reduce LTE coverage by up to 11%

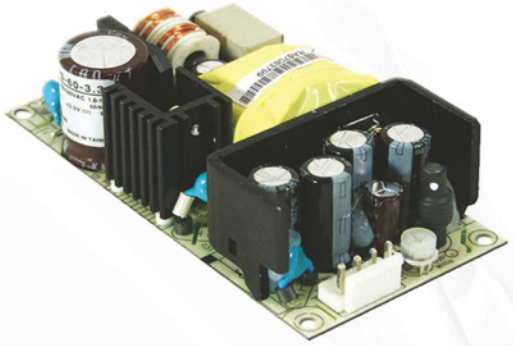
Another key capability being developed is LTE–License Assisted Access (LTE-LAA), which aggregates carriers in existing bands with LTE in unlicensed bands, currently being used by Wi-Fi, in order to supplement the downlink. LTE-LAA will increase data bandwidths when the shared unlicensed spectrum is not in use.

LTE is also a key enabler for the Internet of Things (IoT), which includes any device that can be connected to the Internet. For example, highway safety can be enhanced if cars are connected with each other to warn drivers of impending dangers or poor conditions. Likewise, in the IoT vision the status and management of connected appliances and electronics will be possible in areas of mobile coverage, leading to better efficiency and performance.

In short, LTE is the leading wireless network technology today and for the next several years. ●

Ray Butler is Vice President of Wireless Network Engineering at CommScope
This column is an edited extract from CommScope's new eBook, 'LTE Best Practices'. Over the next few months, different authors of this eBook will contribute comments to this section.

ECOPAC POWER UK LTD



Power Supplies

DIN Rail

Open Frame

Enclosed

External

MEAN WELL

Call: 01844 204420

Email: sales@ecopacpower.co.uk

Website: ecopacpower.co.uk

Universal Serial Bus

LUCIO DI JASIO, ELECTRONICS ENGINEER AND TECHNICAL AUTHOR, PRESENTS THIS SERIES ON EMBEDDED USER-INTERFACE DESIGN ON A BUDGET

For the universal serial bus (USB) it all began around 1995, with the attempt to solve a performance problem of the early graphic desktops (Windows's humble beginnings). At the time, Microsoft and others realised that the interfaces used for floppy disk controllers and the serial ports for connecting modems, printers and pointer devices (ever used a serial mouse?) were all "asynchronous" interfaces, loading the CPU with constraints and severely limiting the PC's performance. (Keep in mind that the Intel 80286/386 processors used in those days were running at or below 33MHz – slower than most modern, entry-level, 8-bit microcontrollers.)

The proposed USB standard made all such peripherals communicate "synchronously" with the host (PC). The real-time constraints were moved onto the devices, relieving the main CPU so to operate on a managed schedule.

Despite the increase in complexity, even the peripheral devices gained from the new standard. There were two big issues in those days: power supply and configuration. The USB physical layer definition now allowed power to any connected device (initially only 100-500mA @5V), and the standard specified very flexible means of automatically configuring each type of peripheral and, in doing so, completely removed the issue from the user experience.

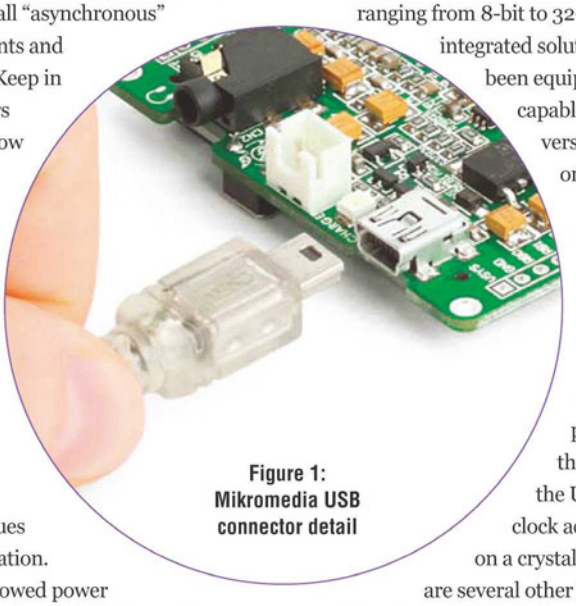


Figure 1: Mikromedia USB connector detail

USB On A PIC

From a microcontroller point of view, a USB interface requires three things:

1. A fast and accurate clock source (48MHz with better than ±0.25% tolerance);
2. A bi-directional transceiver capable of handling the Manchester-encoded differential signalling used by the USB D+ and D- lines;
3. A serial interface engine (SIE) capable of handling (multiple) fast data transfers (up to 12Mbit/s) to and from dedicated RAM buffers.

Luckily, today there is a large selection of PIC microcontrollers ranging from 8-bit to 32-bit that provide a completely integrated solution. All Mikromedia boards have been equipped with one such microcontroller, capable of offering the most widely adopted version of the standard known as USB2.0 or Full Speed.

See Figure 1 for a detail of the Mikromedia USB connector.

The PIC microcontroller on the PIC24 Mikromedia board (PIC24FJ256GB110) offers a very flexible, dedicated PLL circuit, capable of multiplying the main processor's clock signal to obtain the high-speed clock signal needed by the USB SIE. Meeting the stringent USB clock accuracy requirements is dependent on a crystal oscillator in this case; however, there are several other PIC microcontroller models that achieve the same accuracy without using a crystal but rather a new technology known as Active Clock Tuning.

The PIC24 GB110 device also has a USB Full-Speed-capable transceiver and a set of internal pull-up resistors for automatically selecting the desired transmission mode (full speed vs low speed). The transceiver pins can be directly wired to the USB connector, as shown in Figure 2.

Mikromedia boards can also use the power supply (5V) offered by the USB interface to charge a Li-Polymer battery thanks to the onboard dedicated chip, MCP73832 (see Figure 3).

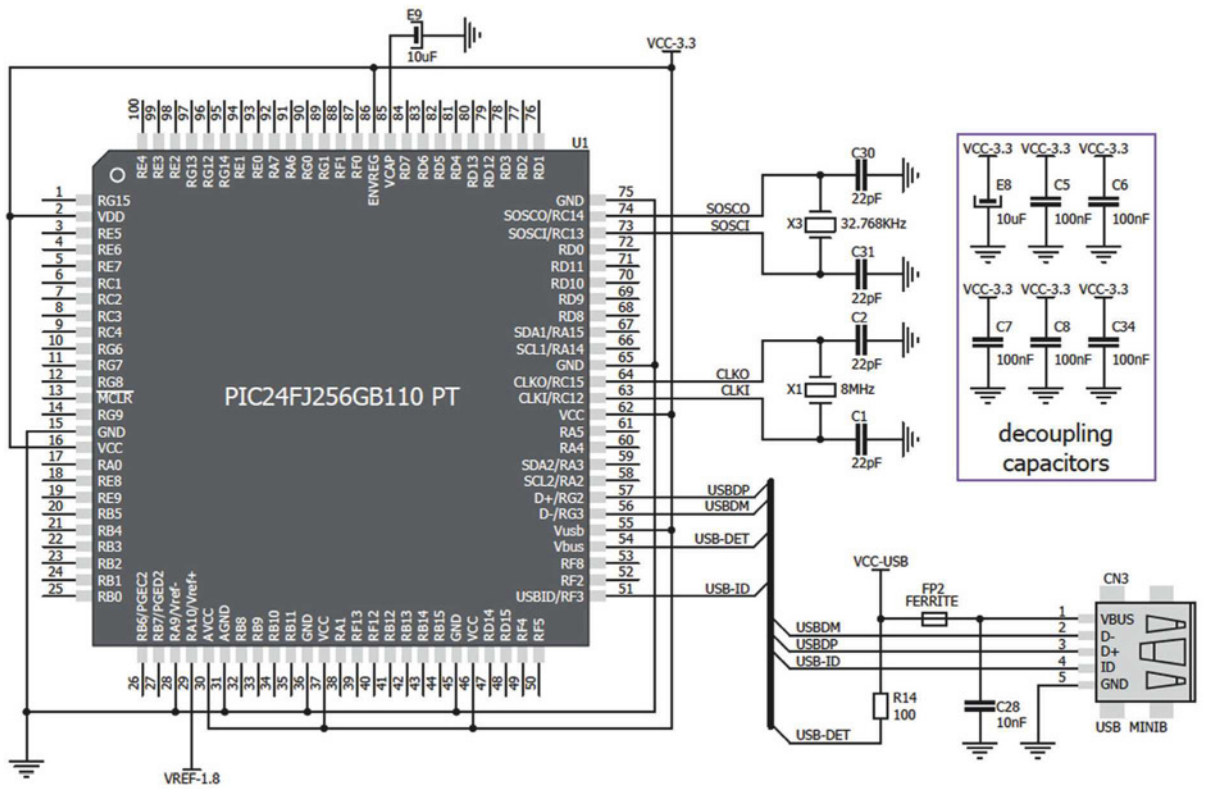


Figure 2: . Schematic detail of a Mikromedia USB module

USB Support

Despite the considerable amount of on-chip hardware support, significant software to configure and use a proper USB application is still needed. The Microchip Library for Applications (MLA) – and specifically the USB library – provide the necessary modules and a very large number of ready-to-use example projects.

If you have read any previous instalments of this series, you will remember that the USB library demands that its own configuration file be added to the project – usb_config.h (see Listing 1 for a segment of the file).

```
//#define USB_POLLING
#define USB_INTERRUPT
//-------------------------------------------------------------------------
---

#define USB_PULLUP_OPTION USB_PULLUP_ENABLE
//#define USB_PULLUP_OPTION USB_PULLUP_
DISABLED
#define USB_TRANSCEIVER_OPTION USB_INTERNAL_
TRANSCEIVER
//#define USB_TRANSCEIVER_OPTION USB_
EXTERNAL_TRANSCEIVER

#define USB_SPEED_OPTION USB_FULL_SPEED
//#define USB_SPEED_OPTION USB_LOW_SPEED
```

Listing 1: usb_config.h (segment), USB configuration options

In best MLA fashion, all options are offered as simple symbol definitions, easily switching on or off individual features. In the Listing 1 segment, you will notice the selections of pull-up resistors, internal transceiver and communication speed options.

Finding A Class

One of the greatest benefits of using USB is the standardization (and automation) of device configuration, but this is contingent to the effective use of the USB "class system". It is of primary importance to be able to associate any given (embedded) application with a specific (optimal) class chosen from the many offered by the standard, such as: human interface device (HID), communication device class (CDC), mass storage device (MSD), and also printer, audio and others.

The selection process can be overwhelming for a beginner, but if we limit our scope to the typical embedded control applications

(excluding the larger categories of consumer products here), a vast majority of cases can be covered with just two classes: HID and CDC. Choosing between the two will then depend on a couple of simple considerations:

- CDC is the best choice when dealing with legacy applications originally designed for a simple serial port (UART). The resulting interface can fit right into the existing (embedded) code structure with minor or no modifications to the application design. Further, on the host (PC) side, there will be no modifications required, as the USB connection will be accessible as a "virtual" serial port (COM:).
- HID is the best choice when defining a new (embedded) control application, as long as the data transfer requirements do not exceed 1Mbit/s. This option offers the greatest freedom in defining the control API and its "grammar", since it is based on the simple exchange of data packets of up to 64 bytes at a time.

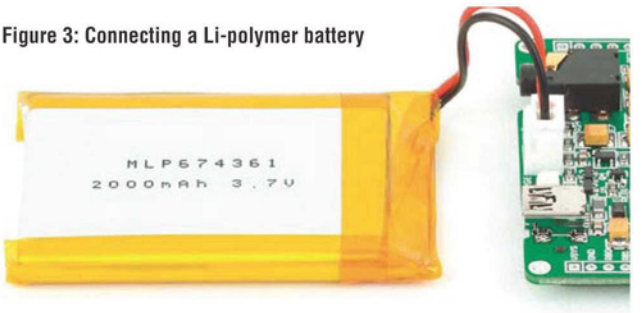
> The solution offered by the proposed USB standard was to make all such peripherals communicate "synchronously" with the host (PC)

To the application developer, the difference between the two classes will translate as setting up the MPLAB X project to use one of two possible USB "descriptor" files – see Listings 2 and 3 for segments extracted for the corresponding usb_descriptors.c file for HID or CDC application. ●

```
/* Device Descriptor */
ROM USB_DEVICE_DESCRIPTOR device_dsc=
{
 0x12, // Size of this descriptor in bytes
 USB_DESCRIPTOR_DEVICE, // DEVICE descriptor type
 0x0200, // USB Spec Release Number in BCD format
 0x00, // Class Code (HID_DEVICE = 0x00)
 0x00, // Subclass code
 0x00, // Protocol code
 USB_EP0_BUFF_SIZE, // Max packet size for EP0, see
usb_config.h
 0x04D8, // MCHP Vendor ID
 0x003F, // Product ID: Custom HID device demo
 0x0002, // Device release number in BCD format
 0x01, // Manufacturer string index
 0x02, // Product string index
 0x00, // Device serial number string index
 0x01 // Number of possible configurations
};
```

Listing 2: *usb_descriptors.c* (segment), USB HID class descriptors

Figure 3: Connecting a Li-polymer battery




```
ROM USB_DEVICE_DESCRIPTOR device_dsc=
{
 0x12, // Size of this descriptor in bytes
 USB_DESCRIPTOR_DEVICE, // DEVICE descriptor type
 0x0200, // USB Spec Release Number in BCD format
 CDC_DEVICE, // Class Code
 0x00, // Subclass code
 0x00, // Protocol code
 USB_EP0_BUFF_SIZE, // Max packet size for EP0, see
usb_config.h
 0x04D8, // MCHP Vendor ID
 0x000A, // Product ID: CDC RS-232 Emulation Demo
 0x0100, // Device release number in BCD format
 0x01, // Manufacturer string index
 0x02, // Product string index
 0x00, // Device serial number string index
 0x01 // Number of possible configurations
};
```

Listing 3: *usb_descriptors.c* (segment), USB CDC class descriptor

USER INTERFACE DESIGN FOR EMBEDDED APPLICATIONS

Lucio Di Jasio is EMEA Business Development Manager at Microchip Technology. He has held various technical and marketing jobs within the company's 8, 16 and 32-bit divisions for the past 18 years.
Lucio has published several books on programming for embedded control applications, and we have three copies of his book *'Graphics, Touch, Sound and USB, User Interface Design for Embedded Applications'* to give away at the end of this series.
If you want to win this book, please send an email to svetlanaj@sjpbusinessmedia.com, mentioning the title in the heading.

Zero Span

BY **MYK DORMER**

The short period during which a transmitter turns on or off is a time fraught with potential troubles. During this "transient switching" period any part of the circuit may go unstable or exhibit unexpected behaviour, and the main frequency source – especially if it is a PLL – may pull off-frequency or unlock entirely. The limits to just how much imperfection is allowable at this point in a radio's operating cycle is strictly defined and limited by the various regulatory specifications. Measuring it can be much more of an open subject.

There are dedicated test-sets and analysers that execute a range of these measurements (usually expressing the results in the same "transient power in adjacent channel" terms as the regulatory specifications define), and advanced examples of the familiar time- or frequency-domain instruments (oscilloscopes and spectrum analyzers) may offer software options that do the same. Unfortunately, while very useful in making a pass/fail check for compliance, knowing there is excessive power in the adjacent channel is very different from knowing what failure mechanism is putting it there.

For that test, you need to directly observe both the RF power envelope over time and the output frequency on a millisecond by millisecond basis.

As I have mentioned before, a compatible receiver outputs this information directly, in terms of its RSSI (envelope) and demodulated AF (frequency) outputs, but these measurements are always compromised by the often slow response time and limited dynamic range of the RSSI and the baseband channel bandwidth of the AF path. Fast effects such as inflections in the RF power ramp or short frequency aberrations in a PLL output can be completely overlooked by such an inherently in-band measurement, while still causing enough mischief to fail the eventual power-off-channel tests.

So what can a practical bench engineer measure with basic lab equipment?

Feeding the transmitter output straight to a spectrum analyzer and toggling the transmitter on and off with a square wave of a few tens of hertz will yield a lot of information:

- Set the sweep frequency of the analyser so it is not a multiple or sub-multiple of the transmitter toggling frequency, activate a "max hold" measurement and leave the instrument to accumulate readings for a few minutes. With a span of a few megahertz, any out-of-channel instabilities or spurii will be visible, as will any peculiarities in the noise floor, often a symptom of LF instability in the PA control loop or bias circuits.

  Reducing the span to about four channels will give a very rough-and-ready idea of the close-in transient power, especially if a comparison can be made (by storing a series of screenshots) with the transmitter in steady state. This adjacent channel close-in measurement gives an idea of the general spread of the carrier energy resulting from the switching operation, and will also reveal any extra loop spurii (typically appearing at multiples of the loop comparison frequency as a consequence of energy from the phase comparator output leaking past the loop filter).

  Asymmetry in the power "skirts" of the transmission usually results from defects in the shape of the RF power ramp (the "envelope"), while generally high off-channel energy results from too-abrupt switching of the RF (badly timed tx/rx antenna switches are a rich source of this trouble), generating what are effectively AM modulation sidebands.
- There is an operating mode in the spectrum analyser that not many use: "zero span". Setting to this mode turns an analyser from a "frequency versus time" instrument into an "RF power versus time" one, with a very fast response and a very wide dynamic range.

  This mode requires some careful tweaking to get the sweep time, resolution bandwidth (as wide as it can be tolerated) and, most particularly, the triggering correct (which varies greatly from analyser to analyser: if all else fails it may be possible to feed the transmitter switching square-wave into an ancillary input on the instrument, often found on the back panel), but once set up will give a far better view of the shape of the RF power ramp than either a receiver's RSSI or any diode detector probe can. Here, you want to see controlled, smooth monotonic shapes. Abrupt transitions, glitches and inflections are definite danger signs.

Of course, identifying the problem is only half the battle, fixing it is a whole different issue. That may well be a (bigger) subject for another day. ●

Myk Dormer is a Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

SPORTS WATCH REFERENCE MODEL ILLUSTRATES POTENTIAL OF SILICON FOR WEARABLES

By Stefan Drouzas, Solution Marketing, Toshiba Electronics Europe

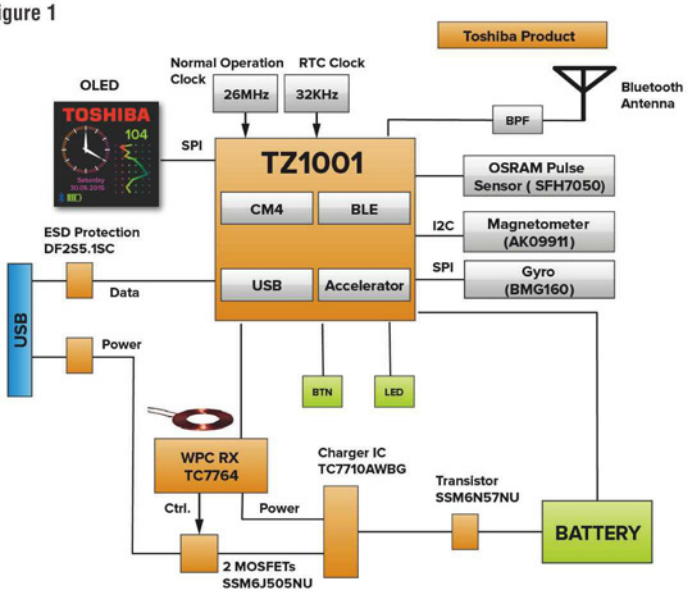
As demand for wearable, connected devices increases, so too does availability of technologies to simplify and speed their design. This is particularly true in the semiconductor arena where there is a growing number of processor technologies targeted at wearable 'internet of things' solutions. The key to delivering functionality alongside the best possible user experience lies in combining these increasingly integrated processors with additional devices and software that are optimised for the target application.

Enabling the Smart Watch Innovators

Among today's most successful wearables is the smart watch. Currently this market is dominated by the sports watch, offering a variety of fitness or 'wellbeing' applications, which demand the ability to monitor a variety of criteria including physical activity, distance travelled, elevation gains and losses and heart rate. And looking at the technologies available to help designers develop such watches can give us insight into how to implement the best possible solution for this type of application.

At the heart of any sports watch application will be a suitable low-power application processor. This processor needs to be integrated with inertial sensors such as MEMS accelerometer, gyroscope and magnetometer, a solution for measuring heart rate, a suitably small yet clear display, and Bluetooth® or other communications for networking with the user's smartphone or other external equipment. All this needs to fit within a form factor that can be worn comfortably on the wrist with a typical wristband sized between 20-25mm. A Micro-USB port for syncing with a PC is also typically needed, as well as circuitry for battery management and charging.

Figure 1



Reference Model Hardware

To demonstrate component selection and hardware/software integration for a smart watch, and to help accelerate development of sport watch applications, Toshiba has created a reference model based on its TZ1001MBG ApP Lite application processor. This processor has a low-power architecture featuring power islands that allow unused parts of the device to be turned off when not in use, making it ideal for wearable and Internet of Things (IoT) applications.

The TZ1001MBG is based on the ARM® Cortex®-M4F core with floating-point unit and DSP extensions for high-speed processing of sensor signals. Requirements for additional discrete components are reduced through the integration of an on-chip MEMS accelerometer, multi-channel 24-bit sigma-delta ADC, Bluetooth Low Energy controller, USB controller, and on-chip Flash memory.

Working with the processor's built-in accelerometer, a MEMS gyroscope and MEMS magnetometer have been integrated into the model via the integrated SPI and I2C interfaces. Together, these sensors enable a comprehensive inertial measurement subsystem capable of motion, gesture and context sensing. This provides the ability to support sports functions such as step counting, as well as user interface functions such as shake-to-tap and screen orientation adjustment.

In addition, the sports watch reference model uses the Osram SFH7050 optical sensor for pulse rate detection. This sensor is arranged to lie on the underside of the watch close to the wearer's skin, and features a green LED emitter and a detector that receives reflected light for making pulse measurements. Green wavelengths have been discovered to be optimum for pulse measurement on the wrist. The sensor also has an infrared emitter for proximity sensing, which enables pulse measurement to start automatically when the wearer puts on the watch.

Wireless charging is convenient and efficient for small mobile devices and wearables, making it a natural choice for the reference model. A number of wireless charging standards have been proposed: Toshiba selected Qi from the Wireless Power Consortium (WPC), which includes Foreign Object Detection and is the standard supported by the Toshiba TC7764WBG wireless power receiver IC. This device is fabricated using a combined CMOS-DMOS wafer process that cuts heat generation while allowing up to 95% power conversion efficiency. Protocol authentication circuit is built in thereby offloading the host microcontroller and simplifying software design.

The main user interaction with the sport watch is via a 128 x 128 pixel 1.5-inch PMOLED colour graphic display. OLED technology facilitates a super-slim display that can be mounted

in the top of the housing, leaving adequate room for the rest of the system electronics.

Figure 2 shows the housing concept and the internal arrangement of the main circuit board, OLED display, pulse sensor, Bluetooth radio, wireless charging circuitry and probing connector.

The reference model also includes the circuit board, which has six copper layers and integral flexible substrates for mounting the optical sensor, Bluetooth antenna and probing connector. The flexible substrate allows convenient assembly, and permits these parts of the design to be positioned for best performance. The optical pulse sensor, for instance, is located in an aperture on the underside of the housing in close proximity to the wearer's wrist.

The watch housing completes the hardware element of the reference model. The housing is a square design, with dimensions that allow the unit to be worn comfortably and provide adequate internal space for the circuit board, battery, display and other components such as buttons.

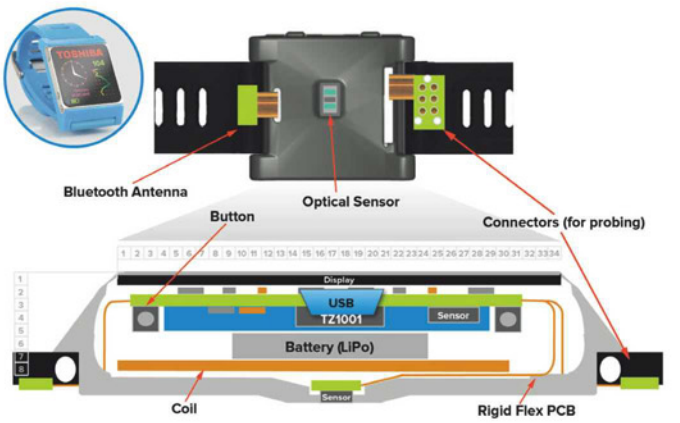


Figure 2

Software Architecture

The sport watch reference model is running on FreeRTOS™, which has features designed to support low-power applications and is available on flexible terms without any requirement for users to publish their source code. Toshiba has ported FreeRTOS to the host TZ1001MBG application processor using its own Board Support Package (BSP).

Above the RTOS, the reference model integrates the Bluetooth Low Energy stack and graphics libraries, as well as the Toshiba Healthcare Solution Development Platform (HcSDP). These support a sample application that performs activity and heart rate monitoring, and also manages Bluetooth communication, wireless charging, power management and user-interface functionality.

Figure 3 shows the software structure and example watch-face display showing pulse monitoring. A sample Android app accompanies the reference model, enabling syncing of the smart sport watch with an Android phone to display current and historic activity data.

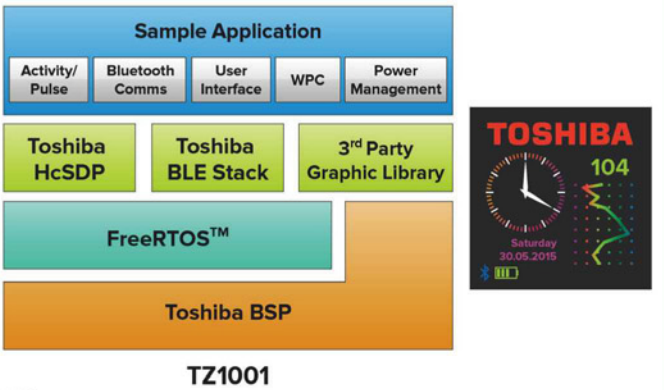


Figure 3

Development Support

The target consumer markets for smart watches and other wearable devices are, by definition, very fast moving. As a result developers need to be able to design, test and implement systems in the shortest possible times. Fundamental to achieving this is the availability of suitable development support. It is no longer enough for silicon vendors and component vendors to simply provide devices – they must, instead, look to create complete ecosystems that speed and simplify implementation and support integration with other hardware and software elements.

In the case of the TZ1001 processor employed in the sports watch reference, for example, Toshiba offers miniature reference boards that allow for pre-design evaluation and rapid development of application prototypes. The RBTZ1001-4MA reference board combines the processor with ADCs, USB ports, coin cell and USB power options, and a variety of external I/Os. This board can be used alongside the forthcoming RBTZ1001-4SH sub-board that is targeted specifically at healthcare applications. Integrated into the latter is a healthcare system reference circuit comprising 8MB SPI Flash memory, charger IC, voltage and current measurement circuitry, two PPG (photoplethysmography) sensors, and ECG electrode circuitry.

Conclusion

Opportunities for new wearable technology products are real and growing. Ideas for new applications will come from creative minds in the healthcare, fitness and other industries, as well as from established technical communities.

Would-be designers from any background need help to choose and integrate the right devices from among the wide variety of low-power ICs currently on offer for wearable and IoT applications. Success here holds the key to delivering an end product that offers the required functionality and delivers an inspiring user experience. A working reference model not only demonstrates how to select suitable hardware and integrate middleware and application software, but also helps accelerate design completion.

Toshiba Electronics
Toshiba Electronics Europe, Hansaallee 181, D-40549 Düsseldorf, Germany
Tel: +49 (0) 211 5296 0
www.toshiba.semicon-storage.com

COMMUNICATIONS SYSTEMS – A DESIGN PRIMER

DUE TO THE COMPLEXITY OF DESIGNING A NEW COMMUNICATIONS SYSTEM, THE USE OF AN EXISTING SYSTEM OR STANDARD IS OFTEN THE MOST SENSIBLE APPROACH TO MINIMISE DEPLOYMENT TIMESCALES, DEVELOPMENT COSTS AND RISK. HOWEVER, A CUSTOM DESIGN CAN LEAD TO BETTER PERFORMANCE AND COST BENEFITS. BY **ANDY DEARN** AND **LIAM DEVLIN** FROM PLEXTEK RF INTEGRATION

Wireless communications systems have progressed a long way in the last 100 years: from radio broadcasting – the first mass market application – to today's ubiquitous smartphones offering an array of applications and communication at ever-increasing data rates. This growth in functionality and complexity was enabled by the advent of the integrated circuit (IC) and the availability of microprocessors, which together led to miniaturisation and low-cost high-volume manufacture.

Modern communications systems proliferate throughout the available spectrum using a wide range of channel bandwidths, modulation schemes and data rates. The main traffic for wireless communications systems is now data rather than voice, and the required data rates are constantly rising.

The optimum implementation choices for a communications system depend on many requirements, including functionality and performance, the available technology, operational conditions and limitations, legislative restrictions, development budgets, unit cost targets and timeframes. The design process is complex, requiring an in-depth understanding of technology, radio systems, digital processing and the ability to accurately simulate the effects of a practical realization at a system level.

Applications And Requirements

Although much global effort is focused on maximizing data throughput to meet the relentless consumer demand for wireless data, there are many other applications. Low-data-rate M2M (machine-to-machine) applications communicate tiny amounts of information infrequently. For example, city authorities can now control street lights using a small two-way radio link, such as that shown in Figure 1, allowing selective dimming late at night to save energy. The street lights also report back the status of the bulbs to schedule maintenance.

Another growth area is high data-rate backhaul links for personal consumer applications. A mobile phone mast will connect to all cellular subscribers in its coverage area, but a link is required to the cellular operator's regional control centre and then onto the established phone network. Wide bandwidth microwave line-of-sight links are often used here, operating with high-order modulation schemes to squeeze more data through each channel.

Satellite systems allow truly global coverage for emergency services in times of disasters, as well as for news reporters and others needing communications beyond the range of the normal cellular services. Satellite receivers are very sensitive; the signal levels are very low by the time they arrive on the ground, and special attention is paid to minimizing their noise figure. The disadvantage is that they are more prone to interference from high-power systems on nearby frequencies.

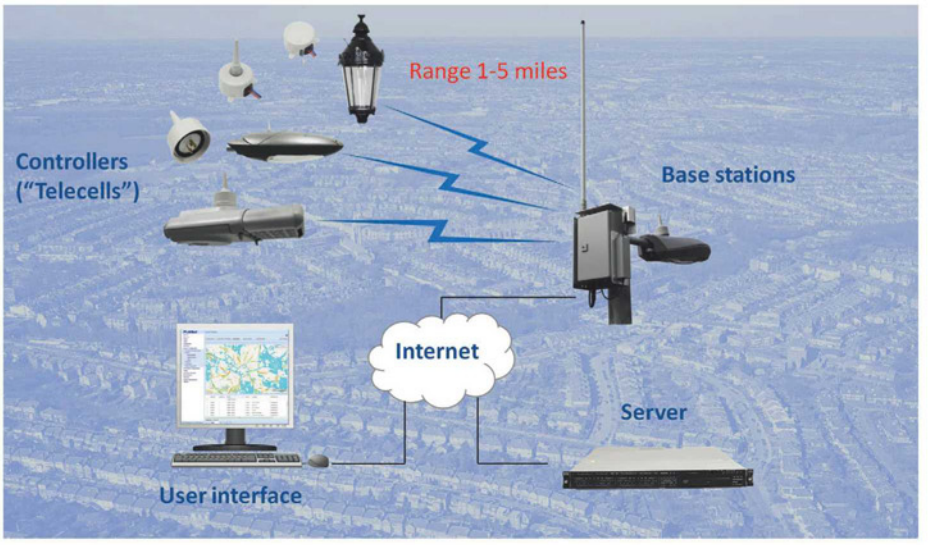


Figure 1: Wireless street lighting control system [courtesy of Telensa]

Modulation Schemes And Data Rates

The one resource all radio applications have in common is a shared radio spectrum. As the number of applications continue to increase, it becomes more important that this is used efficiently. In all cases, the modulation must be appropriate for the

application, as efficient as possible, and constrained to the bounds of the allocated channel.

There are many modulation schemes operating in systems around the world today. So called "high order" modulation schemes are commonly used to obtain high data-transfer rates, but with the disadvantage that they place challenging requirements on the error vector magnitude (EVM), the recovered eye diagram and the control of the symbol detection points.

For illustration, Figure 2 overlays four separate modulation schemes having the same mean power – QPSK, QAM16, QAM32 and QAM64 – on a single constellation diagram, each modulation symbol representing 2, 4, 5 and 6 bits of data respectively. The constellation points of the highest scheme (QAM64) are much closer to each other than are those of the lowest scheme (QPSK), making it the most susceptible to noise and distortion.

> The design process is complex, requiring an in-depth understanding of technology, radio systems, digital processing and the ability to accurately simulate the effects of a practical realization at a system level

The presence of noise in the receive channel sets the fundamental limit on the bit error rate (BER) that can be achieved for a given modulation scheme. The higher the order of modulation used, the higher is the BER for a given signal-to-noise ratio. Distortion within the receiver must also be well contained. Channel filtering, if applied too severely, can distort the modulated waveform, resulting in eye closure, constellation distortion and an increase in BER.

Transmitter imperfections such as amplitude and phase distortion in the RF amplifiers and phase noise of the local oscillator also cause constellation distortion and degrade link BER. Transmitter distortion can cause the signal to self-intermodulate and produce spectral regrowth into adjacent channels. Digital pre-distortion (DPD) techniques are often used to minimize this.

System Simulations

When designing a radio system, sufficient time should be devoted to system simulations to predict performance in terms of EVM, spectral regrowth, constellation and eye distortion and BER sensitivity. This is time-consuming but worthwhile, particularly in cases where ICs are under development. Figure 3 compares the simulated with measured BER of a low-IF demodulator, designed by Plextek RFI and implemented as part of a custom ASIC now in volume production. The close agreement is a testament to the accuracy that can be achieved with careful design and simulation.

Modern cellular systems make use of orthogonal frequency division multiplexing (OFDM) to further increase data throughput. In this case, data to be transmitted is split into a large number of lower data-rate streams and is then modulated onto orthogonally spaced sub-carriers, as shown in Figure 4. The orthogonal spacing ensures that there is no crosstalk between sub-channels and allows

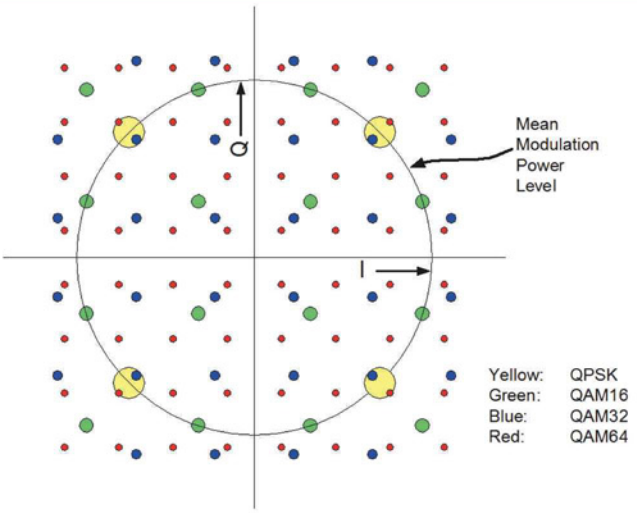


Figure 2: Combined I-Q constellation diagram

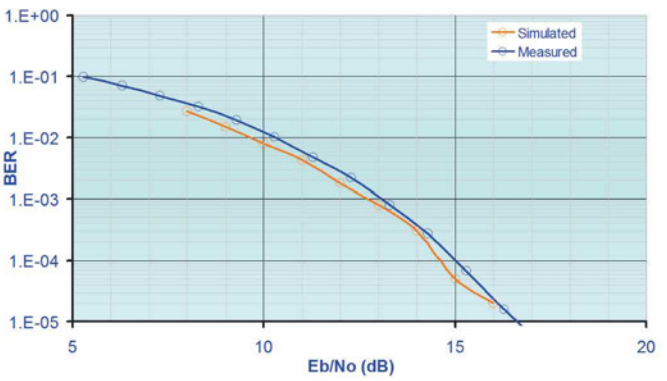


Figure 3: Comparison of simulated to measured BER

a high degree of frequency compaction, giving a very high data-density per unit of transmission bandwidth. The advantage of OFDM over high data-rate single-carrier schemes is its ability to cope with propagation issues, discussed in more detail below.

The use of spatial diversity is also increasingly common in modern mobile devices. This introduces two or more separate transmission paths between the mobile phone and the cellular mast. These MIMO (multiple input multiple output) systems increase further the data throughput. Again, radio system design for these applications involves a lot of detailed simulation of the performance of MIMO OFDM-modulated signals.

Propagation And Link Budgets

In free space, with a single direct line-of-sight path between transmitting and receiving antennas, the path loss follows a simple square law with distance. This is valid for satellite-to-satellite communications, but for terrestrial point-to-point links the formula needs to be modified to include the effects of reflections off the earth, accounting for antenna height and

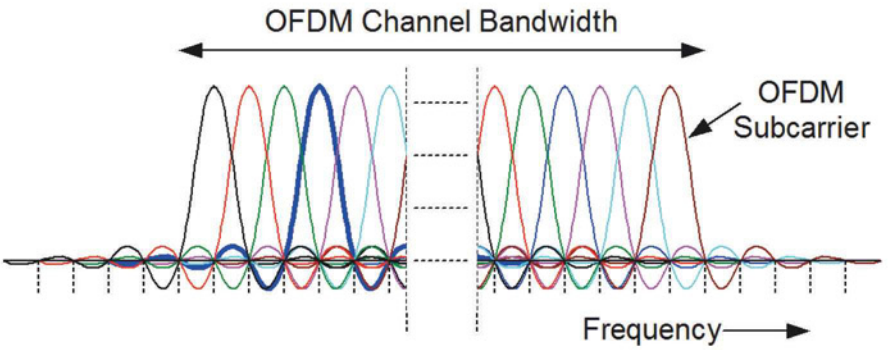


Figure 4: Simplified Image of OFDM

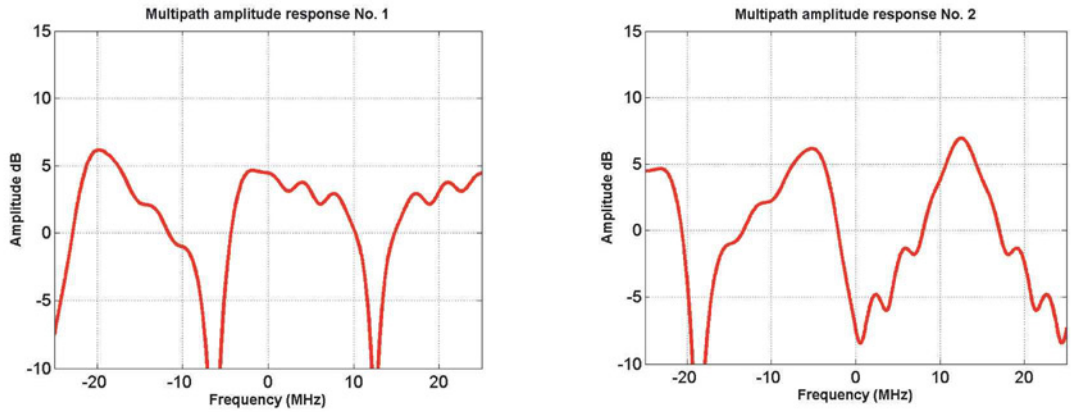


Figure 5: Two instances of the propagation path amplitude response of ITU Indoor Office Channel A

ground reflection coefficient. For non-line-of-sight propagation, additional losses due to reflection, diffraction and scattering caused by obstructions must be included.

At microwave frequencies, loss is also incurred due to rain and atmospheric absorption. A rain fade margin is included in the system design, dependent on the weather conditions of the location and on the required link availability. Atmospheric absorption is dependent on both frequency and altitude, but only really starts to become significant at mm-wave frequencies.

A communications system link budget should be balanced to ensure there is adequate signal power arriving at the receiver for acceptable link quality. The link budget can be improved by increasing transmit power, increasing antenna gain (transmit and/or receive), reducing noise figure, or changing modulation scheme or rate, so that the required signal-to-noise ratio (SNR) is obtained at the receiver.

The impact of multipath propagation on a transmission system can be assessed by undertaking system simulation with an appropriate multipath channel model. Figure 5 shows the channel amplitude response using the ITU Indoor Office Channel A model at two different frequencies. This is a 6-path static model having a 35ns rms delay spread; note that the x-axis is centred about 0Hz and represents the RF carrier centre frequency.

The impact of this channel model on a 5MBd QPSK signal will now be illustrated. Note that the signal bandwidth will occupy the frequency range of ±3.125MHz about the zero Hz centre frequency. As expected, Response 1 has less impact on the signal than Response 2 because its amplitude distortion about 0Hz is much less than that of Response 2; the resulting eye diagram (Figure 6) and constellation plot (Figure 7) show that it will be more difficult to receive the signal with Response 2.

The corruption apparent in Figure 7 is due to inter-symbol interference (ISI), as multiple copies of the transmitted signal arrive at the receiver with slightly different delays. One effective means of combating ISI is to periodically transmit a known sequence of data, allowing the receiver to create an inverse model of the multipath interference and remove (equalize) its effects with a digital filter. With moving users or objects in the local environment, the multipath behaviour of the channel is constantly changing, so the filter needs to be adaptive (continually updated).

The use of OFDM also helps to combat ISI, as each sub-channel propagates independently along narrow subsections of the multipath channel. Each subsection on its own has very little amplitude and phase variation, thus avoiding the need for adaptive

equalization. While the need for equalization may have been removed, some sub-carriers will be transmitted in propagation nulls and lost. The use of appropriate error correction and interleaving of data across sub-carriers can be used to mitigate this effect.

Multiple Access Techniques

To allow multiple users access to the same communications system, a means of separating the different signals must be adopted. This can be by separation in time (time division multiple access – TDMA), in frequency (frequency division multiple access – FDMA), or by applying a unique code (code division multiple access – CDMA). Combinations of these techniques are also used.

Separation in time and/or frequency is also used to separate receive signals from transmit signal, providing full duplex communications. These approaches all have different benefits and the most appropriate technique depends on system requirements.

Operating Frequency and Interfering Signals

The radio frequency spectrum is a global resource, co-ordinated on a worldwide basis by the International Telecommunications Union (ITU). Each country controls access to the frequency spectrum in its jurisdiction by a variety of means. For some parts of the spectrum such as that allocated to private mobile radio systems, the country regulator will set regulatory limits and issue licenses to control interference between users. For other spectrum – such as the cellular bands – there are fewer restrictions and the cellular operators are allowed to self-control their emissions. Still further parts of the spectrum are designated licence-exempt and here there is relatively weak regulatory control of interference levels; an example of this is the industrial, scientific and medical (ISM) bands.

Whatever the operating frequency of the system, there will be strict limits on the allowed emissions at all other frequencies, and this can be a significant design challenge, particularly for spectrum close to the operating band. Unwanted emissions from a transmitter include the generation of excessive harmonic levels or spurious products, adjacent channel leakage of carrier phase noise and spectral regrowth in adjacent channels. Similarly, the radio receiver must include sufficient filtering to reject unwanted signals and operate with sufficient linearity so that intermodulation does not produce interfering signals within the receive band.

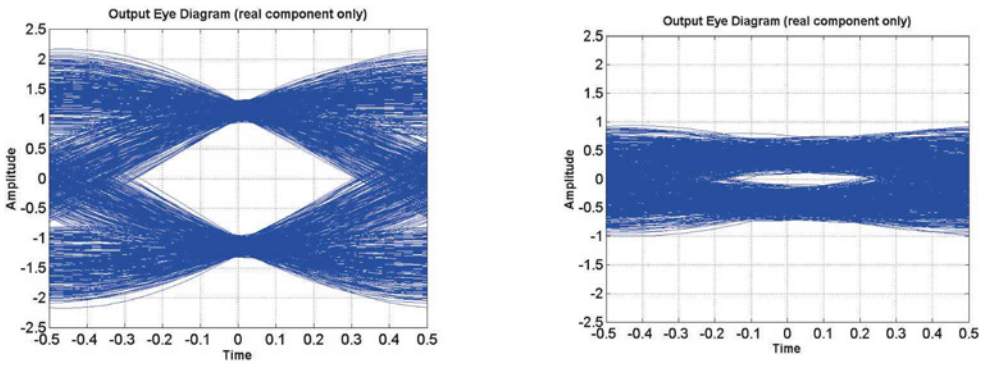


Figure 6: 5MBd QPSK eye diagram: on the left is Response 1 and on the right Response 2

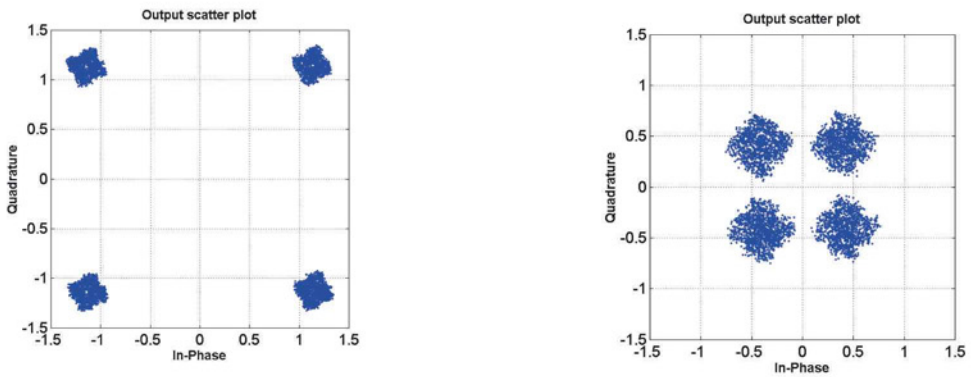


Figure 7: 5MBd QPSK constellation diagram: on the left is Response 1 and on the right Response 2

Radio Architectures

The superheterodyne transceiver architecture goes back to the early days of radio when designs were implemented using discrete components. The receiver mixer converts the signal from the transmission frequency to a standard IF such as 455kHz, 10.7MHz, 21.4MHz or 70MHz, where crystal or ceramic filters provide high-selectivity channel filtering. Similar filtering in the transmitter ensures the transmitted signal only broadcasts in the wanted channel. Filtering at RF is used to reject mixer image responses, protect against blocking signals and reject transmitter harmonics. The predominance of discrete filtering, however, makes this architecture unsuited for integration onto silicon.

The move to full silicon integration over the last twenty or so years has been achieved by adapting transceiver architectures to make use of the advantages of miniaturization whilst steering around the disadvantages. For instance, it is possible to realize integrated channel filters with useful selectivity at low frequencies but not at RF frequencies, so low-IF and zero-IF receiver architectures have been developed to make use of this.

Figure 8 shows a low-IF receiver – direct up-conversion transmitter hybrid architecture, suited to full integration. The received signal is mixed down to a very low frequency IF – close to DC – where polyphase filters make use of the quadrature IF channel to produce a passband response at +IF and a rejected image response at -IF. The level of image rejection achieved depends on the degree of matching in the quadrature channel, and will be finite and will limit the receiver selectivity at this frequency. The low-IF receiver architecture allows the option of including DC blocks to remove DC offsets, which can be problematic in direct conversion receivers.

In the direct up-conversion transmitter, the baseband quadrature modulated signal is mixed up directly to final frequency. Imperfections in the mixers will cause local oscillator leakage and constellation distortion at the output and, to combat this, calibrated corrections are sometimes undertaken.

Depending on the application, further optimization of the architecture may be possible, for example by sharing a common local oscillator or by clever use of dead transmission periods to perform various calibration routines.

Simulating The Communications System

The design and implementation of a new communications system is a complex task and to optimize performance it is wise to undertake extensive modelling. For the RF chain, a cascaded spreadsheet analysis of parameters such as NF, gain, IP3, IP2 and compression used to be the traditional approach – still a valuable tool during the development process. Commercially-available CAD packages have pre-developed blocks that model all stages of the system, including the data, modulation and demodulation, noise and distortion, filtering, channel modeling, frequency conversion, data recovery and error correction. Once established, the model can be adapted as the design moves from concept into realized blocks, either as discrete components or an integrated circuit, and the performance can be continuously checked during this transition.

For fully-integrated designs, the cost of committing to an integrated implementation is high. The options for implementing changes after fabrication are restricted, and the timescales and costs of a second iteration cause nightmares for many project managers. In this instance, simulation of the complete communications system is highly advisable. With adequate care and attention to detail it is possible to accurately simulate system level performance, as shown in Figure 3. ●

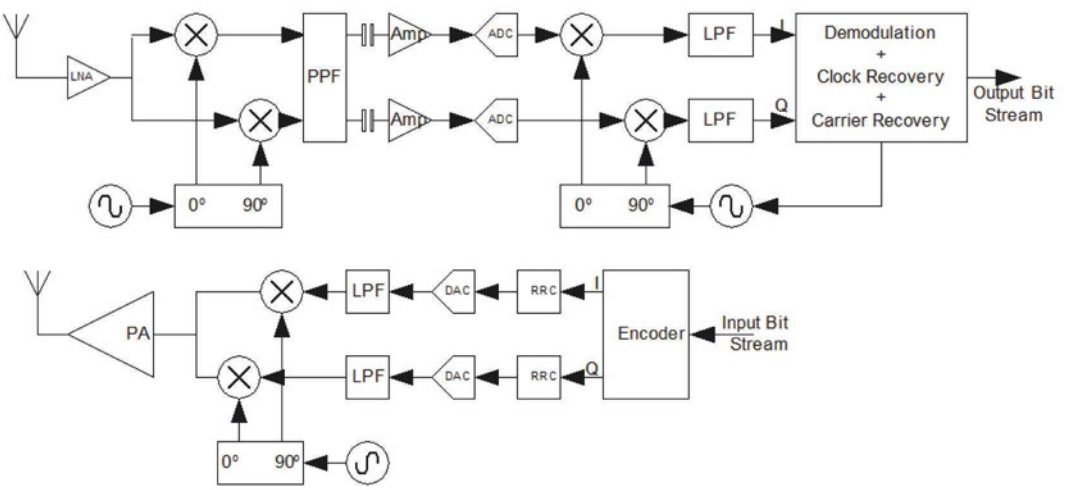


Figure 8: Low-IF receiver – direct up-conversion transmitter hybrid architecture

DESIGN OF A HIGH RESOLUTION TIME TO DIGITAL CONVERTER BASED ON AN INTERPOLATION TECHNIQUE

MAHDI REZVANYVARDOM AND **EBRAHIM FARSHIDI** FROM THE SHAHID CHAMRAN UNIVERSITY OF AHVAZ IN IRAN INVESTIGATE A TIME-TO-DIGITAL CONVERTER THAT EMPLOYS INTERPOLATION AND TIME STRETCHING TECHNIQUES FOR DIGITIZING THE TIME INTERVAL BETWEEN THE RISING EDGES OF TWO INPUT SIGNALS, AS WELL AS INCREASING THE SIGNAL'S RESOLUTION

Time-to-digital converters (TDCs) have been widely used in various industrial applications, such as in on-chip measurement systems, biochemical sensor readouts, frequency synthesis circuits, digital phase lock loops (PLLs), laser range finders, digital storage oscilloscopes and capacitive sensor readouts among others.

In TDCs, the time interval between rising edges of two input signals (start and stop) can be measured digitally, as an analog measurement or a combination of both. With the analog method, a capacitor is charged or discharged by a constant current source at the rising edges of the time interval between signals. The time resolution in this method is excellent but it suffers from poor stability. Also, the linear range of the analog method is not very good and its dynamic range is usually limited.

In the digital method, a synchronous counter counts the clock cycles of a reference oscillator. The linear range of this method is wide, but the time resolution is limited by an uncertainty associated with a ±1 clock cycle. Higher resolution can be achieved by raising the clock frequency, but this adds to power consumption.

One main group of TDCs are delay-line TDCs, which use inverters or buffers to generate quantization levels. As such, their resolution is limited by CMOS gate delay.

To improve time resolution, a Vernier delay-line (VDL) TDC can be adopted, which has sub-gate delay resolution. This, however, has several disadvantages over basic delay-line TDCs, including higher complexity and lower conversion rate. Also, VDL TDCs and delay-line TDCs are sensitive to PVT (process voltage temperature) variations. So to achieve high performance, a high-resolution, high-precision and high-speed TDC is required.

A perfect solution is to use converters based on interpolation and multi-slope pulse stretching techniques for conversion. The interpolation circuits are usually united with the counter-based TDCs to increase the input range to infinity. Compared with similar structures, this approach reduces the active chip area as well as power consumption.

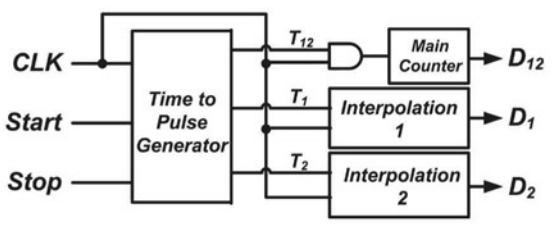


Figure 1: Block diagram of a TDC based on the dual slope time-stretching technique

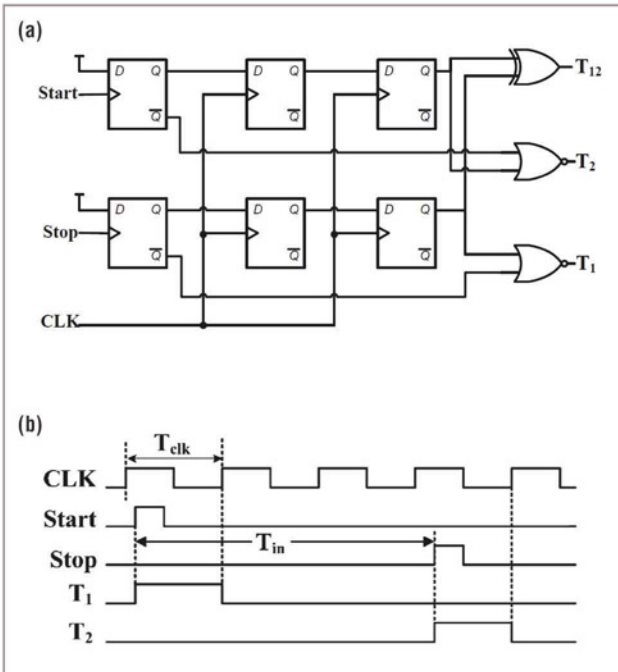


Figure 2: Time splitter: (a) circuit structure; and (b) timing diagrams for a dual slope time-stretcher-based TDC

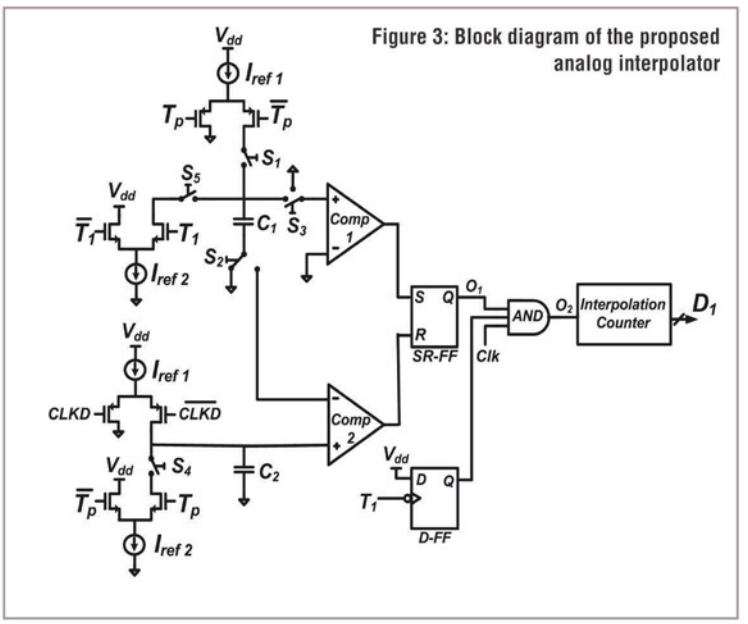


Figure 3: Block diagram of the proposed analog interpolator

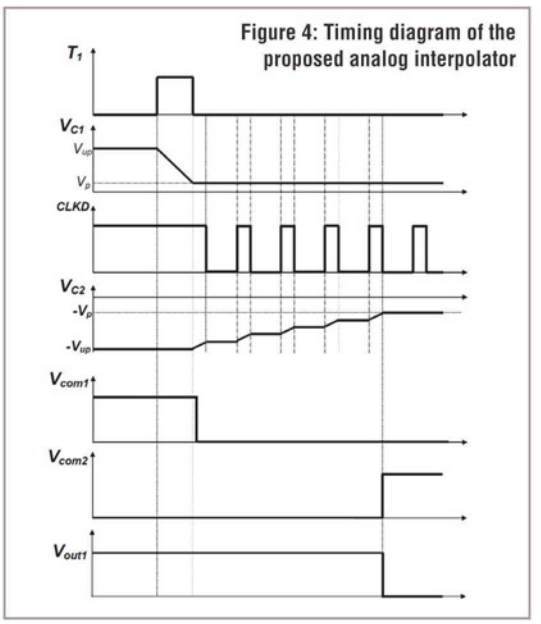


Figure 4: Timing diagram of the proposed analog interpolator

In this article we suggest a TDC based on interpolation, time stretching and dual-slope conversion techniques for digitizing the time interval between two input signals, as well as increasing the resolution. This input time is coarsely measured by the main counter with an accurate reference clock. The fractional portions at the beginning and ending of the input signal are interpolated by two separate time digitizers to improve the time resolution of the TDC.

The main advantages of the proposed converter include eliminating comparator offset voltage, parasitic capacitance, integral nonlinearity (INL) and differential nonlinearity (DNL) errors, whilst offering high accuracy, high time-resolution and low power consumption. Simulation results show that our TDC achieves a resolution of 6.25ps while consuming 185uW with a 1.8V supply. Also, the INL and DNL errors are within +0.06/-0.11 LSB (least significant bit) and +0.2/-0.33 LSB respectively.

The Proposed Converter

The block diagram of a TDC based on the dual-slope-time stretching technique is shown in Figure 1. It is a counter-based TDC that uses an interpolation technique to increase resolution. It consists of a time-to-pulse generator (or time splitter), a coarse counter and two parallel dual-slope time stretchers. The time-to-pulse generator block diagram and its timing diagram are shown in Figure 2.

In the time-to-pulse generator, the time interval between the rising edges of two input signals (T_{in}) is digitized into three separate parts, T_1, T_2 and T_{12}. The main part T_{12} is related to coarse measurements and can be digitized by a main counter with an accurate synchronous reference clock (CLK). Also, the fractional periods T_1 and T_2 are digitized by the analog interpolators with finer resolution than T_{Clk}. Thus, T_{in} is determined by:

$$T_{in} = D_{12} \times T_{Clk} + (D_1 - D_2) \times \frac{T_{Clk}}{2^n} \quad (1)$$

where n and $T_{Clk}/2^n$ are the numbers of bits and LSB, respectively. D_{12} is the digital output of the main counter. Also, D_1 and D_2 are the digital outputs of the analog interpolators 1 and 2 respectively.

The proposed analog interpolator circuit and corresponding timing diagram are shown in Figures 3 and 4. The circuit consists of two comparators, two capacitors with fixed ratio M, two current sources with fixed ratio N, an SR flip-flop, an interpolation counter and several logic gates. In the proposed converter, interpolation is performed based on a dual-slope conversion.

Step 1: Pre-Charging

Initially, capacitors C_1 and C_2 in the analog interpolator circuit are pre-charged to V_{up} and $V_{down} = -V_{up}$, respectively. In this step, switches S_1 and S_4 are turned on while S_5 is turned off. Also, S_2 and S_3 are connected to ground and the comparator input node, respectively. Thus:

$$C_1.V_{up} = I_{ref1}.T_{prch} \quad (2)$$

$$C_2.V_{up} = I_{ref2}.T_{prch} \quad (3)$$

where T_{prch} is the pre-charging time. According to Equations 2 and 3:

$$\frac{C_2}{I_{ref2}} = \frac{C_1}{I_{ref1}} \quad (4)$$

In the proposed converter, $C_2 = M.C_1$ and $I_{ref2} = N.I_{ref1}$, so $M = N$. In this step, the output of comparator 1 is high and the

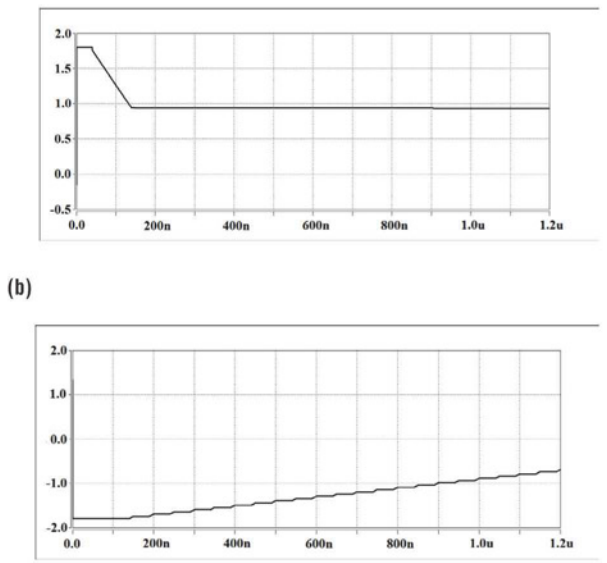


Figure 5: The voltage waveforms of capacitors: (a) C_1; (b) C_2

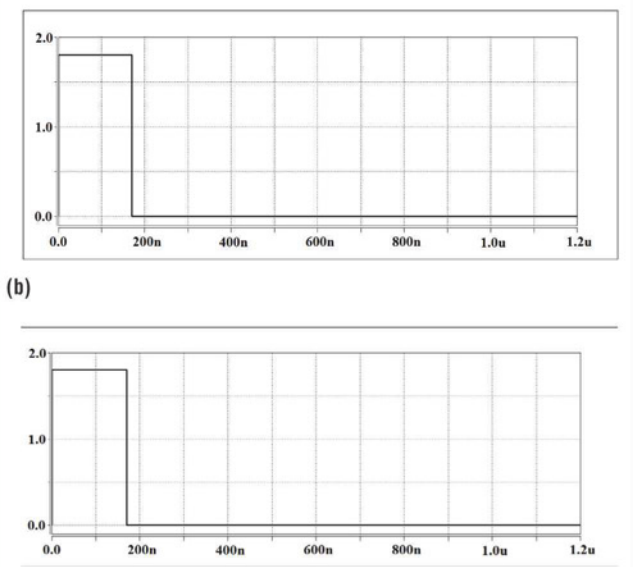


Figure 6: Comparator output waveforms: (a) comparator 1; (b) comparator 2

output of comparator 2 is low, making the output of SR-FF high and enabling the interpolation counter.

Step 2: Discharging

Step 2 starts at the rising edge of T_1. C_1 is discharged linearly by the greater constant current source I_{ref2}. During this step, the voltage on C_2 is saved ($V_{C2} = -V_{up}$), S_1 and S_4 are turned off and S_5 is turned on. Also, S_2 and S_3 are connected to ground and comparator input node, respectively. The outputs of comparators 1 and 2 are 1 and 0, respectively, so the output of the SR-FF is high. This step ends in the falling edge of T_1. Therefore:

$$(V_{up} - V_p).C_1 = I_{ref2}.T_1 \tag{5}$$

where V_p is the voltage of C_1 at the end of step 2.

Step 3: Interpolation And Time Stretching

Step 3 starts at the falling edge of T_1. In this step, S_1, S_4 and S_5 are turned off, and S_2 and S_3 are connected to the input node of comparator 2 and ground, respectively. The voltage across C_1 ($V_{C1} = V_p$) is assigned to the negative input node of comparator 2. As a result, V_{C2} is compared with V_p. During this step, C_2 is charged by I_{ref1}.

At the beginning of C_2 charging, the counter is enabled. The comparators and SR-FF will toggle their outputs to stop the interpolation counter from further counting at the end of the charging phase. While C_2 is charging, the duty ratio of CLKD is set to be greater than 1 to further slow down the charging speed, and the average charging slope will be increased P times. Thus:

$$V_D = \frac{I_{ref1}.T_{CLKD}}{C_2} \tag{6}$$

where V_D is the voltage drop across C_2 for each period of CLKD.

During this step, the outputs of comparators 1 and 2 are 0. Therefore, SR-FF saves its previous state and the interpolation counter continues to count.

Step 3 ends when the output of comparator 2 becomes 1. Next, the output of SR-FF becomes 0, and as a result, the interpolation counter stops.

$$K.\frac{I_{ref1}.T_{CLKD}}{C_2} = \frac{I_{ref2}.T_1}{C_1} \tag{7}$$

$$T_{INT} = M.N.P.T_1 \tag{8}$$

where K is a natural number. Therefore, in the proposed converter the stretch factor becomes (M.N.P) and the LSB width of the TDC improves to $T_{Clk}/(M.N.P)$. The input time interval now measures:

$$T_{in} = D_{12} \cdot T_{Clk} + (D_1 - D_2) \cdot \frac{T_{Clk}}{(M \cdot N \cdot P)} \tag{9}$$

In integrated circuits, due to PVT variations the capacitor ratio must be decreased at the expense of the current ratio increase. Thus, this converter can improve the resolution.

Simulation Of The Proposed Converter

The simulation is performed in TSMC 0.18µm CMOS technology. The proposed converter is implemented by the following elements: a 100MHz reference clock, $C_1 = 1$pF and $C_2 = 8$pF, and constant current sources $I_{ref1} = 10$µA and $I_{ref2} = 40$µA. The duty ratio of CLKD is 20%, so for the simulated converter P = 5.

CLKD is applied at the falling edge of the input time signal. Figure 5 shows the waveforms of the capacitor voltages. C_1 is discharged to V_p by greater constant current source I_{ref1} when T_1 is high. Next, C_2 is charged to V_p by smaller constant current

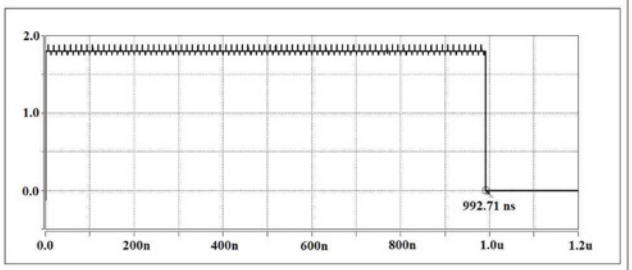


Figure 7: Output waveform of the SR-FF

source I_{ref2} when T_1 is low. V_{C2} reaches V_p once the output of comparator 2 goes high. Interpolation is performed by a second clock reference, CLKD.

Figure 7 shows the output waveforms of the comparators. T_1 is high for 100ns. During this period, the voltage of C_1 (V_{C1}) falls to 0.9V. At the falling edge of T_1, the outputs of comparators 1 and 2 are low. V_{C2} reach to -Vp, once the output of comparator 2 becomes high. This time period for the simulated converter is 992.71ns.

Figure 8 shows the output of SR-FF. When the output of comparator 2 goes high (t = 992.71ns), the output of SR-FF becomes low; therefore, the stretch factor for the converter is 160 and the LSB width of the proposed converter is improved to 6.25ps.

Non-Ideal Effects

DNL and INL

The DNL and INL of the proposed TDC in the linearity performance of the corresponding region are +0.06/-0.11 LSB and +0.2/-0.33 LSB, respectively. Figure 8 shows the measured DNL of the CMOS process corner of technologies with in +0.055/-0.157 LSB. Figure 9 shows the measured INL of the CMOS process corner of technologies +0.051/-0.154 LSB. In general, errors of nonlinearity DNL and INL are less than +0.2/-0.33 LSB and +0.06/157 LSB, respectively.

Comparator offset error

The proposed converter eliminates any error associated with a TDC with offset voltage error, resulting from employing capacitors in parallel with the comparators' input nodes; and as a result, the pulse width of the comparator output is incorrect and the interpolation counter produces erroneous counts. Figure 10 shows the proposed converter with comparator offset voltage and comparator parasitic capacitance errors. In the pre-charge step, $V_{C1} = V_{up} + V_{Offset}$ and $V_{C2} = V_{up}$. In step 2, V_{C1} reaches to V_p. Thus:

$$V_{p,Offset} = V_{up} + V_{Offset} - \frac{I_{ref\,2}.T_1}{C_1} \qquad (10)$$

where $V_{p,Offset}$ is the voltage of C_1 at the end of step 2. During step 3, $V_{C2} = V_p$:

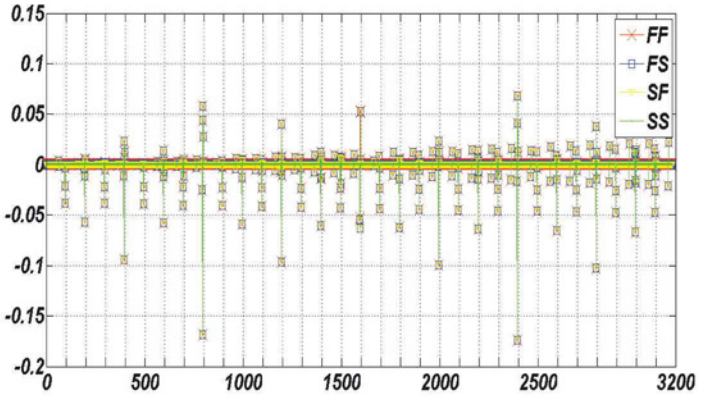


Figure 8: The measured DNL of the proposed converter in the CMOS process corners of technologies

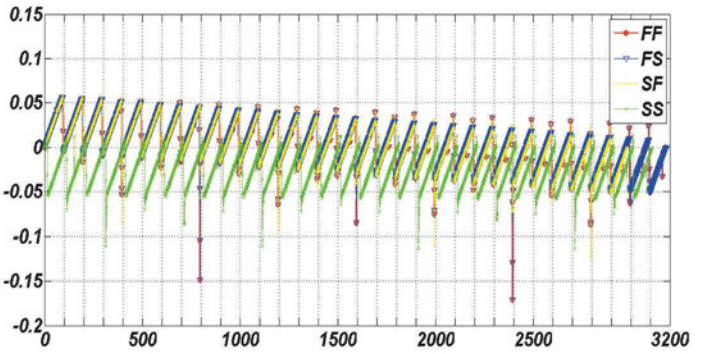


Figure 9: The measured INL of the proposed converter in the CMOS process corners of technologies

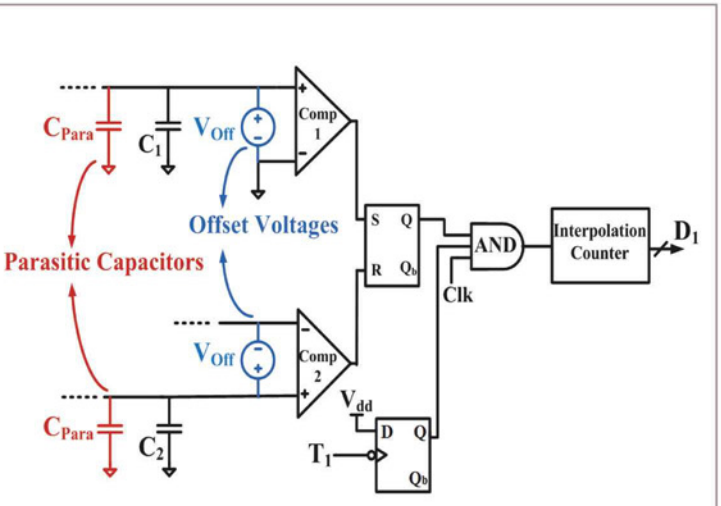
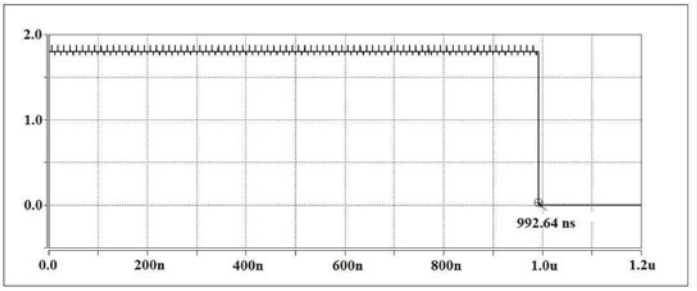
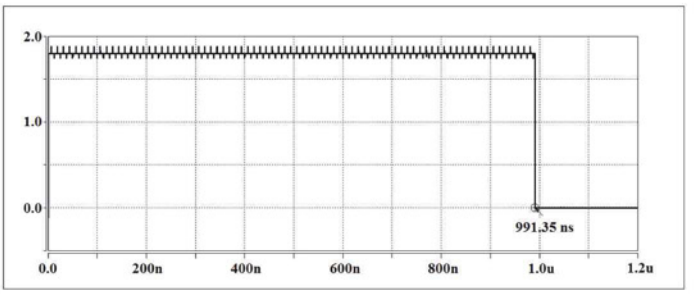


Figure 10: The proposed converter with comparator offset voltage and comparator parasitic capacitance errors

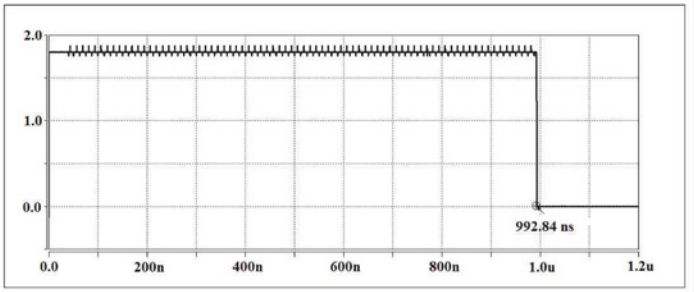
(a)



(b)



(c)



(d)

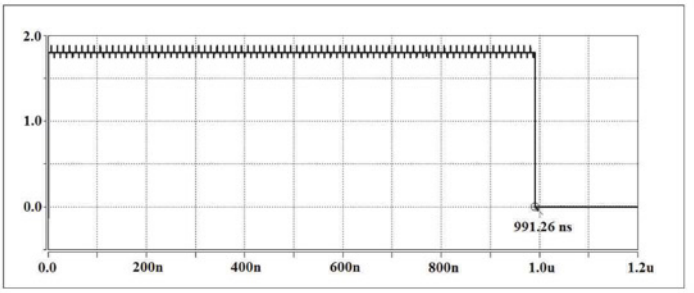


Figure 11: The CMOS process corners of technology: (a) SS; (b) FF; (c) SF; and (d) FS

$$V_{C1} - V_{Offset} = V_{up} + V_{Offset} - \frac{I_{ref2} \cdot T_1}{C_1} - V_{Offset} \quad (11)$$
$$= V_{up} - \frac{I_{ref2} \cdot T_1}{C_1}$$

Comparator parasitic capacitor error

Using capacitors in parallel with the comparators' input nodes can cause comparator parasitic capacitance error, resulting in inaccurate capacitor ratio M and erroneous interpolation counting. Our proposed converter eliminates this error. In the previous TDC, the total charge needed to pre-charge C_2 and C_1 for a dual-slope time stretcher's single cycle of operation can be expressed as:

$$Q_{Precharge,dual} = 2(C_2 + C_{Parasitic} + C_1) \cdot (V_{up} - V_p) \quad (12)$$

whereas in our converter, the total charge needed to pre-charge C_2 and C_1 can be expressed as:

$$Q_{Precharge,proposed} = 2(-C_2 - C_{Parasitic} + C_1 + C_{Parasitic}) \cdot (V_{up} - V_p) \quad (13)$$
$$= 2(C_1 - C_2).(V_{up} - V_p)$$

According to Equation 13, the comparator parasitic capacitor error is removed in the proposed converter operation.

CMOS Process Corners Of Technologies

Figure 11 shows the output of the SR-FF in CMOS process corners of technologies. Figures 11a, b, c and d show the SS, FF, SF and FS corners of technologies, respectively. As can be seen, the errors of the output pulse width in the different CMOS process corners of technologies are negligible and do not affect counter operation. Measurements of the performance of the different TDCs as well as ours are summarized in Table 1.

It can be concluded that this high-resolution TDC, which uses interpolation, time stretching and dual-slope conversion techniques for digitizing time intervals between input signals and increased resolution eliminates comparator offset voltage and parasitic capacitors errors. As such, the converter is highly accurate and suitable for high-accuracy and high-resolution applications. In addition, the converter reduces INL and DNL errors. The time resolution of the proposed converter is 6.25ps.

The proposed TDC was simulated using Hspice in TSMC 0.18µm CMOS technology. Comparison of the theoretical and simulation results confirms the proposed TDC operation. ●

Performance Summery	*Ref [6] (Fabricated)*	*Ref [14] (Fabricated)*	*This Work (Simulated)*
Technology	*0.35uM CMOS*	*0.35uM TSMC*	*0.18uM TSMC*
Supply Voltage	*2.5 V*	*2.5 V*	*1.8 V*
Clock Frequency	*175 MHz*	*80 MHz*	*100 MHz*
INL	*-0.62/+0.79 LSB*	*1.1 LSB*	*-0.11 /+0.06 LSB*
DNL	*-0.68/+0.58 LSB*	*-*	*-0.33/ +0.2 LSB*
Resolution	*357 ps*	*50 ps*	*6.25 ps*
Power Consumption	*1.22 mW*	*0.75 mW*	*185 uW*

Table 1: Dimensions of the CMOS transistors

BASICS OF ANALOG CIRCUIT DESIGN

STOJCE DIMOV ILCEV FROM DURBAN UNIVERSITY OF TECHNOLOGY IN SOUTH AFRICA DESCRIBES THE ANALOG DESIGN PROCESS, WHICH BALANCES IMPORTANT PROPERTIES, DESIRED PERFORMANCE SPECIFICATIONS AND CAPABILITIES

Analog design is part of integrated circuit (IC) design and focuses on signal fidelity, amplification and filtering. The task of analog design, in a nutshell, is to make this complex integrated circuitry perform consistently and most efficiently.

The design process for an analog circuit involves creation of the intial design, the use of software programs to model and verify it, then construction of the system and thorough testing. The process will involve a lot of tweaking with various electronic components, such as placing amplifiers and filters at specific points in the circuit to keep the signals clean, or using matching resistors to cancel out signal variations.

Modern ICs may consist of several hundred million electronic components in the tiniest of areas, a complexity that means that hundreds of rules apply regarding their design specifications, compatible layers and the appropriate tests to measure performance. Further, the manufacturing process is so sensitive that supposedly identical chips may do things differently. If not considered, these variations in an integrated circuit's processors can cause fatal errors during the design process.

The Basics

The electronic parameter resistance (R) can be defined as the characteristic of a material that opposes flow of electrical current through itself. The unit of resistance is the ohm, represented by the Greek letter Ω (Omega). The power value associated with resistance is quantified as the amount of power in watts (W) that a resistor can dissipate as heat without overheating. The current (I) generated by the voltage (V) through the resistor (R) is defined as:

$I = V/R$; where $V = I \times R$ and $R = V/I$

At this point, for a 1 megohm (MΩ) resistance, the current resulting from the application of 10 volts (V) would be 10 microamperes (μA).

Ohm's law is the fundamental equation that describes the above relationship between the voltage, the current flowing in a circuit and the resistance of the circuit; its simple representation is shown in Figure 1. The power dissipated in a load resistance is defined as the product of current and voltage.

Other relationships for power (P) dissipated in R can be easily derived from this by applying Ohm's law using substitutions as follows:

$P = I \times V = V^2/R = I^2 \times R$

To calculate the value of the resistance R, and since $P = V^2/R$, the equation is $R = V^2/P$. So, if R is 100/10, or 10Ω, the 10V applied to 10Ω will yield 10W. Whenever any two of the parameters V, R or P are numerically the same, the third will be the same too.

Voltage And Current Divider Calculations

Many circuits require voltage different from that of the main power source. But rather than have multiple power sources, it is possible to derive other voltages from the main power source by connecting resistors in an appropriate configuration and of different values (see Figure 2).

In electronics, a voltage divider, also known as a potential

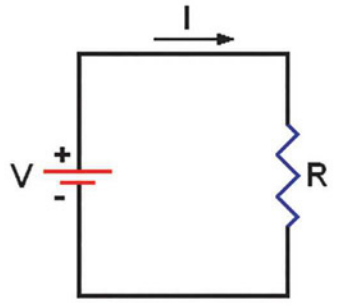


Figure 1: Graphic representation of Ohm's law

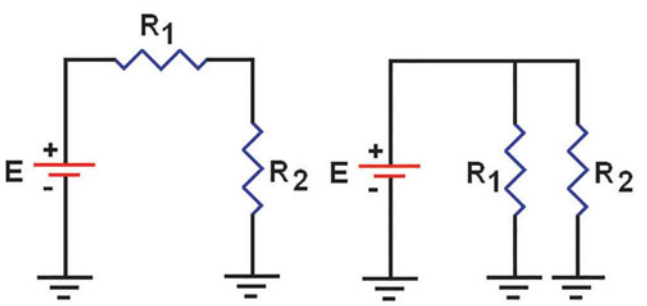


Figure 2: Series and parallel voltage configuration

Figure 3: Example of a capacitor circuit

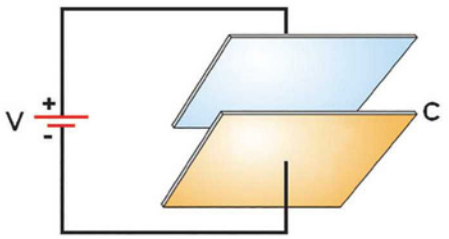
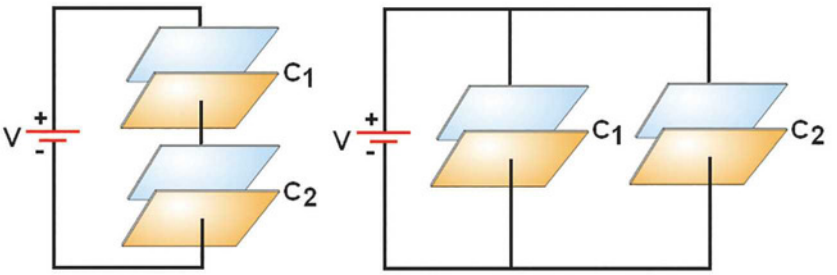


Figure 4: Series and parallel capacitor configurations



divider, is a passive linear circuit that produces an output voltage (V_{out}) that is a fraction of its input voltage (V_{in}). Voltage division results from distributing the input voltage among the components of the divider. A simple example of a voltage divider is two resistors connected in series (Figure 2, left), with the input voltage applied across them and the desired voltage (voltage drop) produced across each resistor.

Resistor voltage dividers are commonly used to create reference voltages, or to reduce the magnitude of a voltage so it can be measured. They may also be used as signal attenuators at low frequencies; thus, for direct current and relatively low frequencies, a voltage divider may be sufficiently accurate if it's made only of resistors, where frequency response over a wide range is required. This can be the case in oscilloscope probes, where a voltage divider may have capacitive elements added to compensate for the load capacitance. In electric power transmission, a capacitive voltage divider is used to measure high voltage.

When two resistors are connected in series, they divide the applied voltage and the same current flows through both of them. The equation used to calculate the resultant voltages is:

$E_1 = R_1 \times I$ (E_1 = voltage drop across R_1); and

$E_2 = R_2 \times I = R_2/I$ (E_2 = voltage drop across R_2);

where:

$R_{EQ} = R_1 + R_2$; $E = E_1 + E_2 = I (R_1 + R_2)$ and $I = E/R_{EQ}$;

where:

$E_2 = R_2/I = R_2 (E / I R_{EQ}) = R_2 [E /(R_1 + R_2)] = E [R_2 /(R1 + R_2)]$

A current divider calculation is performed when two resistors are connected in parallel, with the same voltage across each, shown in Figure 2 on the right. The amount of current flowing through them depends on the resistor values.

In electronics, a current divider is a simple linear circuit that produces an output current that is a fraction of its input current; namely, a current divider circuit which divides its input current into various branches in a certain ratio. A simple arrangement of two or more resistors in parallel can be considered a current divider circuit.

A current divider circuit contains various impedances in parallel. To be specific, if two or more impedances are in parallel, the current that enters the combination will be split between them in inverse proportion to their impedances, according to Ohm's law. It also follows that if the impedances are equal the current is split equally. Thus, a current divider is a simple linear circuit or device which divides the total input current into various paths or loads as fractions of the input current. Figure 2 on the right shows two resistors in parallel, expressed as:

$I = I_1 + I_2 = (E/R_1) + (E/R_2) = E [(1/R_1) + (1/R_2)]$ where:

$E = I_1 \times R_1 = I_2 \times R_2 = I \times R_{EQ}$ and $R_{EQ} = 1/(1/R_1) + (1/R_2) = (R_1 \times R_2)/(R_1 + R_2)$; where R_{EQ} = R equivalent

The digital multimeter (DMM) is the most common measurement device used in automated test systems. It is very simple to use and is often low cost.

Generally, DMMs have built-in conditioning that provides the following properties: (a) high resolution, commonly expressed as "digits of resolution"; (b) multiple measurements (volts, current, resistance, etc); and (c) isolation and high-voltage capabilities.

Capacitance Calculations

Capacitors store energy in form of electrical charge. The amount of charge a capacitor can hold depends on the area of its two plates (as shown in Figure 3) and the distance between them. Large plates close together have a higher capacity to hold charge. The electric field between the plates of a capacitor resists changes in the applied voltage.

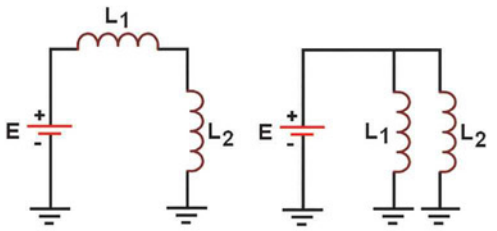


Figure 5: Series and parallel inductor configurations

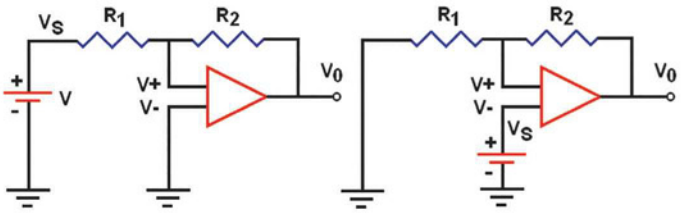


Figure 6: Basic inverting and non-inverting amplifiers

Capacitors decrease their resistance with frequency. They vary in shape and size, but their basic configuration is that their two conductors carry equal but opposite charges. They have many important applications in electronics and electrical engineering, including storing energy, delaying voltage changes when coupled with resistors, filtering out unwanted frequency signals, forming resonant circuits and frequency-dependent and -independent voltage dividers when teamed with resistors.

The formula to calculate capacitance is as follows; the capacitive unit is the farad (F):

$C = Q/V$

where C = capacitance in F, Q = accumulated charge in coulombs (C) and V = voltage difference between the plates.

The limiting factor for capacitor size is the power supply (V). The voltage recharges the capacitor, fully, each supply half-cycle. This will occur when the impedance of the voltage matches that of the primary cap, at the line frequency of 50Hz or 60Hz, for instance. So, maximum capacitor value or impedance can be calculated as Z = V/I; where V = voltage output and I = current output in amperes (A).

Figure 4 (left) shows two capacitors in series. Since the capacitance of a capacitor is inversely proportional to the distance between its plates, the total capacitance (C_T) of any number of capacitances in series can be calculated with:

$C_T = 1/[(1/C_1) + (1/C_2) + (1/C_3)] + \ldots$

The values of capacitance (C) and voltage (V) for two capacitors connected in series are as follows:

$C_1 = Q/V_1$; $C_2 = Q/V_2$; $V_1 = Q/C_1$ and $V_2 = Q/C_2$

The total values of voltage and capacitance equivalent are as follows:

$V = V_1 + V_2 = Q/C_{EQ}$ and $C_{EQ} = 1/[(1/C_1) + (1/C_2)] = C_1 \times C_2/C_1 + C_2$

Figure 4 (right) shows two capacitors in parallel, where each charges to the same applied voltage. Total parallel capacitance equals the sum of the individual capacitances of the capacitors. The amount of charge that can be placed on a capacitor is proportional to the voltage (V) and capacitance (C), pushing the charge onto the positive plate. So, the larger the potential difference (V) between the plates, the larger the charge (Q) on the plates:

$Q_1 = C_1 \times V$; $Q_2 = C_2 \times V$; $Q = Q_1 + Q_2 = V(C_1 + C_2)$
and
$C_{EQ} = C_1 + C_2$; where $C_{EQ} = C_{equivalent}$

Inductance Calculations

Inductance is defined as the amount of voltage drop across an inductor for a given rate of change of current flowing through it. Inductors increase their resistance with frequency. The unit of inductance is the henry (H).

Figure 5 (left) shows two inductors in series; total inductance is the sum of the individual inductances:

$L_1 = L_2 = E \times di/dt$; where $L_T = L_1 + L_2$ and di/dt = instantaneous rate of change of current over time (A/s).

However, in the real world, if we consider a mutual inductance where the magnetic field of each inductor affects the other, then the total inductance can be calculated using $L_T = L_1 + L_2 \pm 2M$; where M = mutual inductance between the two coils.

The instantaneous voltage across the inductor is V = L (di/dt).

Figure 5 (right) shows two inductors in parallel. In such a configuration, their mutual inductance needs to be considered. Also, mutual inductance will be either added or subtracted from the self-inductance of each coil, since the current has two paths to flow through. Total inductance can be calculated using this equation:

$L_T = [(L_1 \times L_2) - M^2]/[(L_1 + L_2) - 2M]$

Modern-day digital multimeters provide universal measurement by offering engineers the 20 most common, automated, test measurements, including voltage, current, capacitance, inductance, temperature and resistance.

Analog Amplifier Circuits

Operational amplifiers (OA) are highly stable, high-gain DC difference amplifier circuits. Since there is no capacitive coupling between their various amplifying stages, they can handle signals from zero frequency (DC) up to a few hundred kHz. Their name is derived from their use in performing mathematical operations on input signals. There are two types of amplifiers: inverting and non-inverting.

1. Inverting amplifier – "inverting" simply reverses the polarity of the input signal, as shown in Figure 6 (left). For example, if the voltage going into the amplifier is positive, it is negative when it comes out. To calculate the output signal voltage and the gain of an inverting amplifier:

$V_o = A (V^+ - V^-)$; $V_S - V_1/R_1 = V - V_o/R_2$
since $V_1 = V - 0$ (virtual ground)

$V_S/R_1 = - V_o/R_2$ and Gain $= V_o/V_S = - R_2/R_1$

2. Non-inverting amplifier, shown in Figure 6 (right) – The gain of the amplifier is determined by the ratio of R_1 and R_2. To calculate the gain of a non-inverting amplifier use:

$V_o \times R_1 = V_S \times R_1 + V_S \times R_2$ and $R_1 (V_o - V_S) = V_S \times R_2$

where:

$V_o/V_S - 1 = R_2/R_1$

Gain $-1 = R_2/R_1$

and Gain $1 = R_2/R_1$ where: Gain $= V_o/V_S$

There are other functions of op-amps: The summing amplifier is a logical extension of the previously described circuit, with two or more inputs. A difference amplifier precisely amplifies the difference of two input signals. The differentiator generates an output signal proportional to the first derivative of the input with respect to time. The integrator generates an output signal proportional to the time integral of the input signal.

Analog RC Filters

1. RC low-pass filter: A common circuit to attenuate high-frequency components in an analog signal is the RC low-pass filter. Figure 7 (A) shows that V_{in} is the applied voltage and the voltage V_{out} across C is the output:

$V_{out} = V_{in} \times R_2/R_1 + R_2$, where $R_1 + R_2 = R_T$

This filter passes low frequency and DC signals to the output, but blocks high frequency signals.

$t = R \times C$ where $F_{adb} = 1/2\pi t$

2. RC high-pass filter: A circuit that attenuates low-frequency components in an analog signal is called an RC high-pass filter, shown in Figure 7 (B). Notice that the circuit is similar to the one above, but V_{out} is now measured across R. The cut-off frequency point (f_C) for a first-order high-pass filter can be found using the same equation as that of the low-pass filter, while the equation for the gain (A_V) and phase shift (φ) is modified slightly to account for the positive phase angle as shown below:

$A_V = V_{out}/V_{in}$; $f_C = 1/4\pi RC$; and $\varphi = \arctan 1/4\pi fRC$ ●

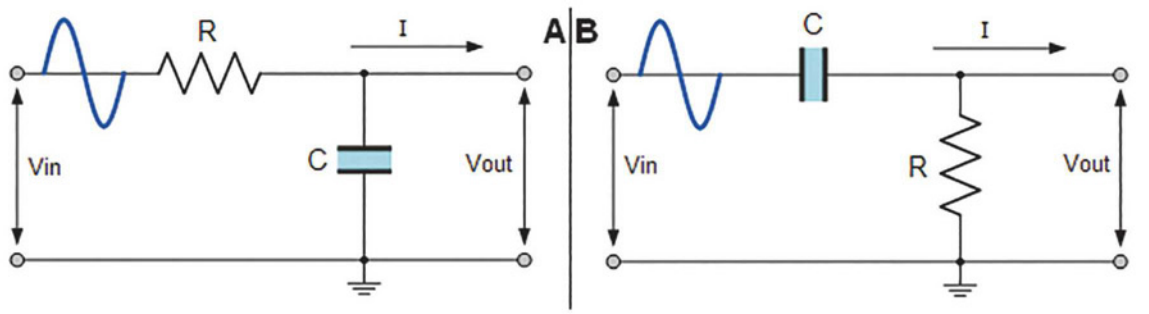


Figure 7: Simple RC low- and high-pass filters

DESIGN AND OPTIMIZATION OF A TELECOMMUNICATION SATELLITE POWER SYSTEM

SELMAN DEMIREL, ERAFETTIN ÖZBEY AND **NEDIM SÖZBIR** FROM SAKARYA UNIVERSITY IN TURKEY AND **DR. ŞENOL GÜLGÖNÜL**, VICE PRESIDENT OF SATELLITE OPERATIONS AT TURKSAT, PRESENT P-SPICE-BASED MODELING OF A POWER SYSTEM FOR COMMUNICATION SATELLITES

Communication satellites have a 15-20-year operational life span, so their design has to be perfect. One of the satellite's most critical systems is the power supply, which includes solar arrays, power regulation units, rechargeable batteries, harness (power distribution) and loads. Each of these parts presents a choice of technologies; for example, for batteries, Ni-H_2 or Li-ion may be used, depending on the satellite's platform. Equally, all these components' behaviour may be nonlinear, for example varying power sources (from 1.5kW up to 21kW), which will require power management, regulation and signal processing. In addition, due to the extended testing periods and high manufacturing costs of communication satellites, analysis, simulation and optimization studies are needed to help model the real system.

Power

As a primary power source, solar arrays generate the electrical energy for the satellite. Rechargeable batteries are used for power storage and as a secondary power source. The energy produced is then regulated and controlled to power the satellite loads. The type of power source to be used depends on the satellite's lifetime: for long missions, it normally consists of solar arrays and batteries, whereas for short missions and small satellites only primary batteries are used.

Power regulation systems (PRS), direct energy transfer (DET) systems or peak power tracker (PPT) systems are typical power system topologies used in satellites. In DET systems the power is sent from the solar arrays to the satellite loads without any power tracking. In PPT systems, for maximum power transfer from the solar arrays, the voltage has to be always monitored and adjusted with a series of linked power trackers. Generally, for small satellites with low power needs, a PPT system could be enough. A DET system is used for satellites with high power requirements, such as communications satellites.

A typical satellite power system is shown in Figure 1.

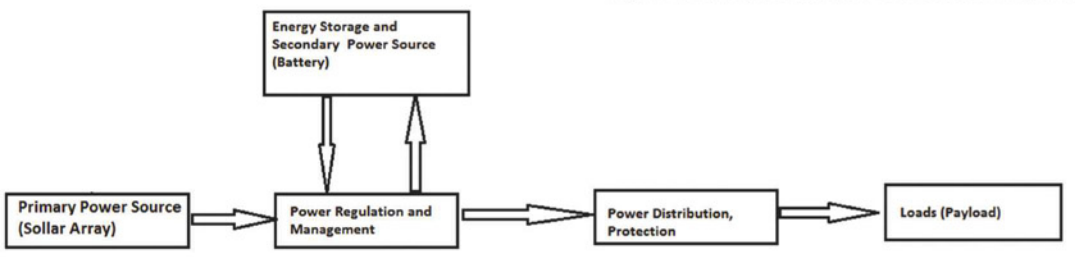
Solar Array Design and Modelling

A solar array (SA) consists of solar cells connected in series. The solar cells can be based on various technologies, but the most commonly used are silicon (Si) and gallium arsenide (GaAs). For their design, solar cell efficiency and cost are the main parameters. Si cells have been used in many satellite missions, as they offer long service lives and are low cost. On the other hand, they have lower efficiency than GaAs, for example. GaAs is considered the more advanced technology, with high efficiency and low mass, but the associated costs are higher. For communication satellites, the main requirements for an SA are small size and low mass, volume and costs. Their design goal is high efficiency with low mass.

Another factor in the SA's design is the satellite's orbital characteristics, since radiation and temperature affect power generation. So to model an SA, electrical characteristics such as I, V and P, need to be taken into account, as well as radiation effects and degradation over time.

When modeling the solar cell, C_o is taken to be approximately 15pF/cm². The capacitance C_p is voltage dependent, so for low voltages C_p = 1.2μF. The equivalent capacitance C_{eq} can be defined in terms of charge or energy stored as follows:

Figure 1: Basic block diagram of the satellite's power system



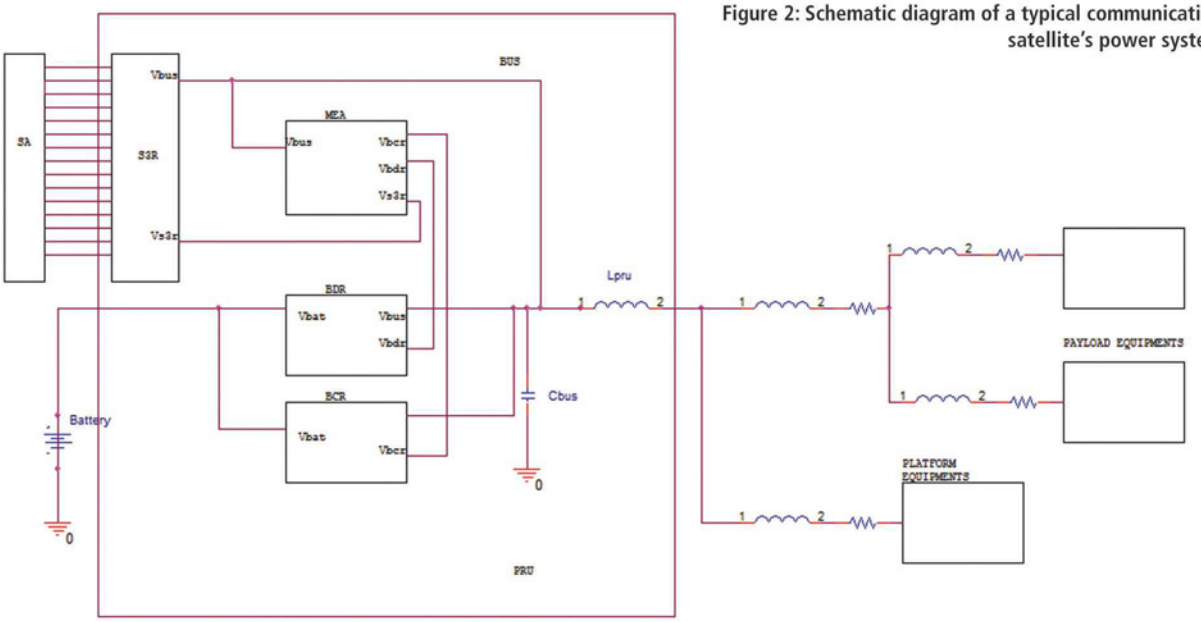


Figure 2: Schematic diagram of a typical communication satellite's power system

Stored energy:

$$E = \frac{1}{2} C_{eq} V_{op}^2 = \int_0^{Vop} C(v)\, d(v) \text{ for } V_{op} = 105V,\ C_{eq} = 2.1\mu F$$

Stored charge:

$$Q = C_{eq} V_{op} = \int_0^{Vop} C(v)\, d(v)$$

$$I(v) = I_{cc}\,(1\text{-}\exp(\text{alpha}*(V\text{-}V_{OC}))$$

In a solar array, solar cells connected in series form strings, and connecting those strings in parallel form the sections (see a section in Figure 4).

If there is a large number of cells (e.g. 256 Si cells per string), and if the negative terminal of the string is connected to a substrate, the equivalent capacitance for the string network is:

$$C_{\infty} = C_0 + \sqrt{(\frac{C_0}{2})^2 + C_0 C_p} = \sqrt{C_0} C_p$$

Normally, disconnection energy dissipation occurs at a section, which may be limited with a sequential switching shunt regulator (S3R). This energy can be calculated as:

$$P_{FET} = RI^2 + fE_{turnoff} \leq 17.5W$$

A turn-on delay occurs when switching from OFF to ON, due to C_{SA}, which can be calculated with $I = C_{sect} V_{op} / I_{SA}$.

P-Spice modeling is used for the SA, as shown in Figure 5.

PRS Design

In power-regulated systems, the SA system's generated power and energy stored in the batteries are regulated. Other satellite designs use unregulated buses, but in high-power applications – like communication satellites – regulated power systems are the norm. Also, depending on the satellite's mission, different regulation topologies can be used, such as regulated S3Rs, sequential switching shunt series regulators (S4R), hybrid systems, regulated maximum power point tracking (MPPT) and so on. For high-power and long-mission-life satellites, S3R regulation topology is preferred. If the satellite mission is shorter than 10 years, depending on the platform used and the power needs, MPPT regulation is a suitable choice.

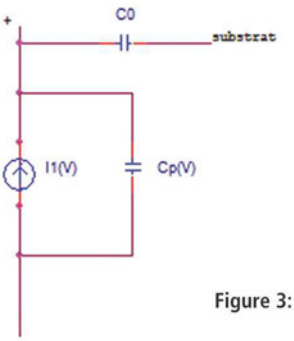


Figure 3: Typical solar cell circuit

In our P-Spice models, we used S3R regulated topology, where initially we compared the SA's power to the bus load's power consumption. When there's enough SA power to supply the bus and battery charge, regulation is performed by the shunts (S3R mode); if there isn't enough power, then the regulation system starts in battery discharge regulator (BDR) mode.

All SA sections are connected to the satellite bus and the batteries will start to discharge. After this point, if the loads need more power, current will flow through the battery charge

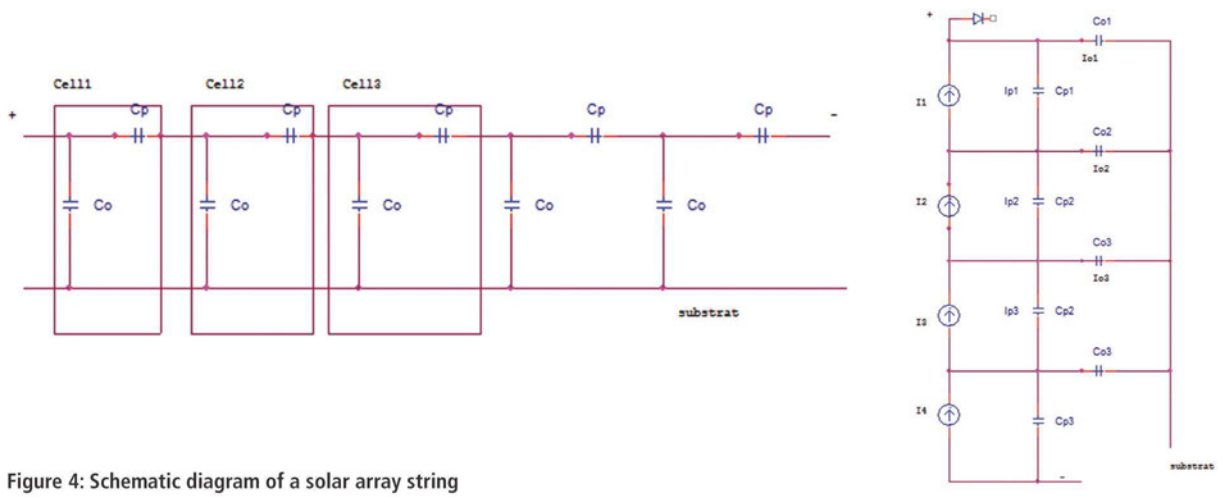


Figure 4: Schematic diagram of a solar array string

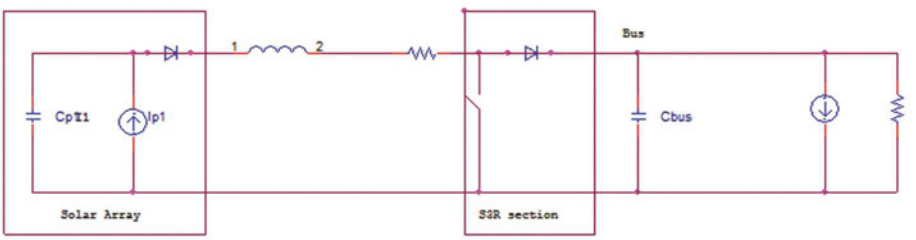


Figure 5: Interface diagram of a solar array section

regulator (BCR) to charge the batteries. After that, if there's any power left, the regulation system goes into S3R mode and closes off some sections.

In Figure 7, the S3R schematic diagram is shown without BDR and BCR modes. In regulation, each regulation source behaves as a constant current generator controlled by the main error amplifier's (MEA's) voltage. The MEA senses the bus's current variations through changes in the bus bar voltage, and then regulates the current from the power sources to exactly balance the bus current. Depending on the current balance, the bus may be controlled by the shunts (S3R domain), the charge regulator (BCR domain) or the discharge regulators (BDR domain). Each domain corresponds to a voltage allocation by the MEA.

In design, satellite power systems are normally developed according to worst-case scenarios. The worst case regarding power regulation is when all power sources supply all power loads; this is called S3R-BDR inter-domain, so the P-Spice modeling has to reflect this approach.

Batteries

In communication satellites, batteries are one of the heaviest parts, so, as a standard design approach, high-efficiency batteries with low mass are used. For long-mission and high-power satellites rechargeable batteries are used, of which the most common are Nickel Hydrogen (Ni-H2) and Lithium-ion (Li-ion). The exact choice of technology depends on the satellite mission, and is based on performance, mass and cost.

Important criteria to compare for various battery technologies are specific energy (Wh/kg), energy density (Wh/l), cycle life and battery DOD (depth of discharge). Li-Ion batteries are considered best due to the advantages they offer over other battery technologies.

Satellite Loads

The payload module consumes the most power in satellites, which comprises a transponder and an antenna. The transponder includes an input test coupler, input filter, receiver, downconverter, input multiplexer, channel amplifier, electrical power conditioner, a travelling wave tube, high-power isolator and an output multiplexer.

See Figure 12 for the P-Spice model of a communication satellite's electrical power system (CSEPS).

Verification of the CSEPS Modeling

The P-Spice model of the satellite electrical power system consists of conducted emission (CE) analyses, with their values compared

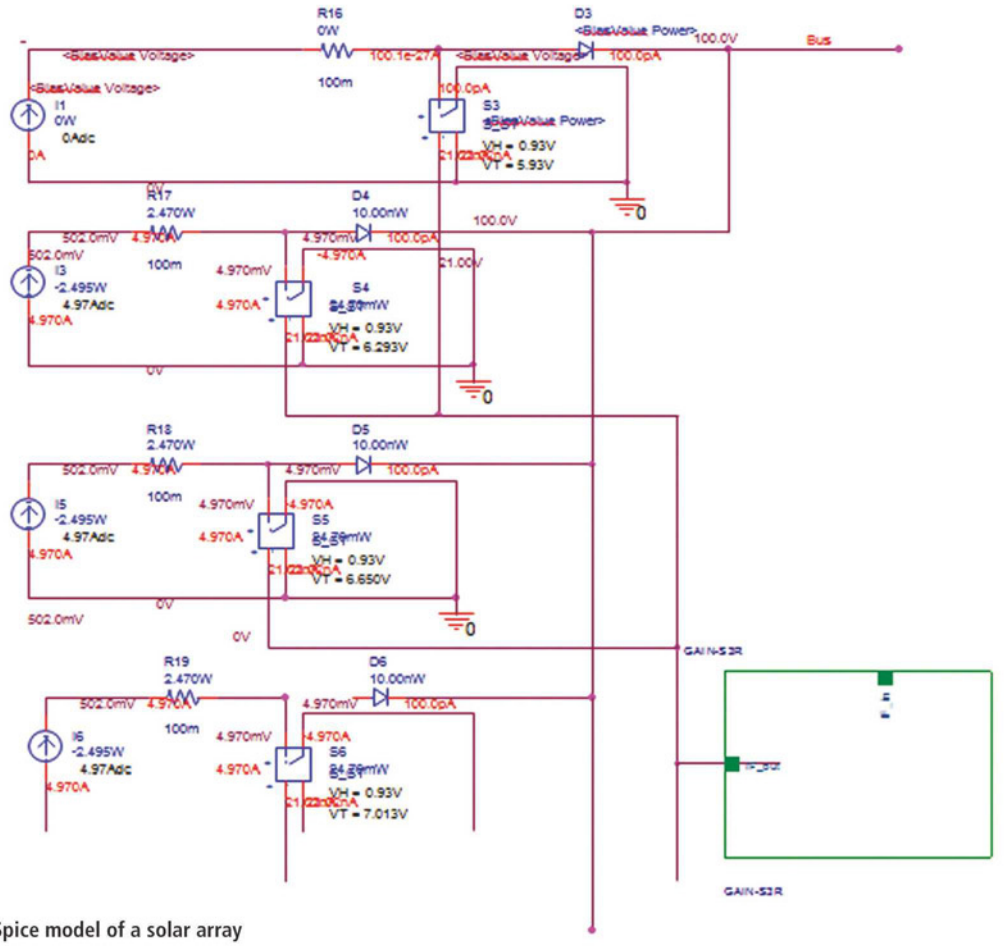


Figure 6: P-Spice model of a solar array

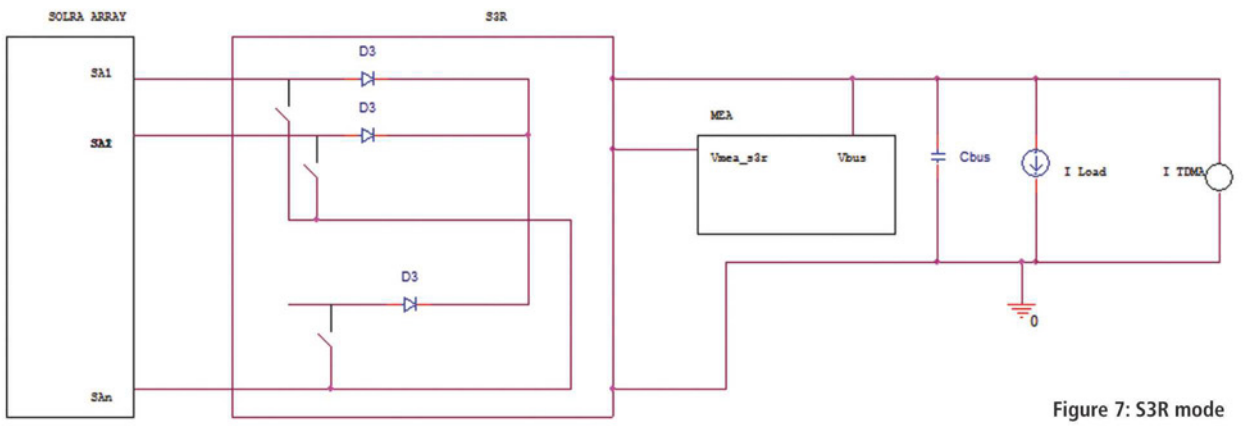


Figure 7: S3R mode

with those of a real-life space orbit-flight satellite. The P-Spice model is designed to include all SA sections, batteries and other equipment with same values as that of the TURKSAT 3A communication satellite for a consistent comparison.

Electromagnetic interference is a result of electric, electronic and other disturbances by another circuit or electric phenomenon outside the system. Interference is not a disturbing signal per se, but it causes problems by coupling, easily affecting a vulnerable system. So the designed system has to be electromagnetically compatible with its environment, i.e. it must function compatibly with other electronic

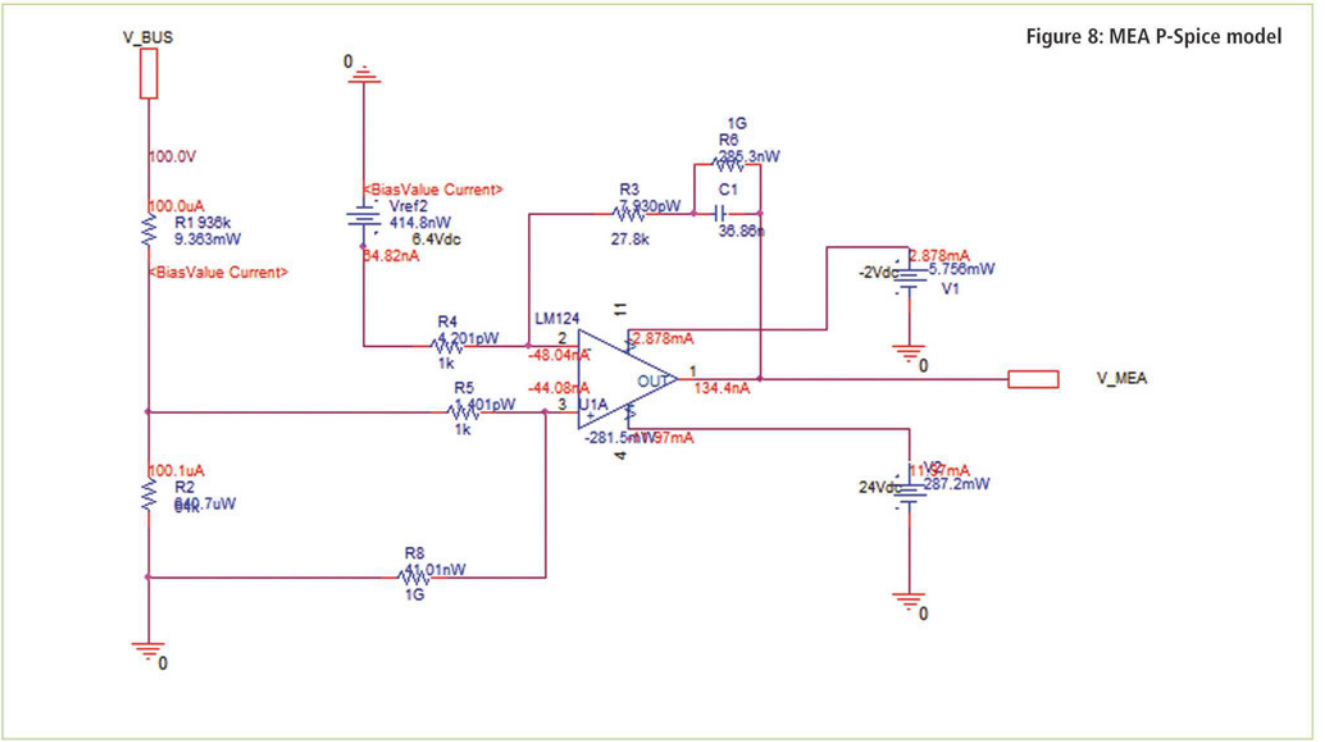


Figure 8: MEA P-Spice model

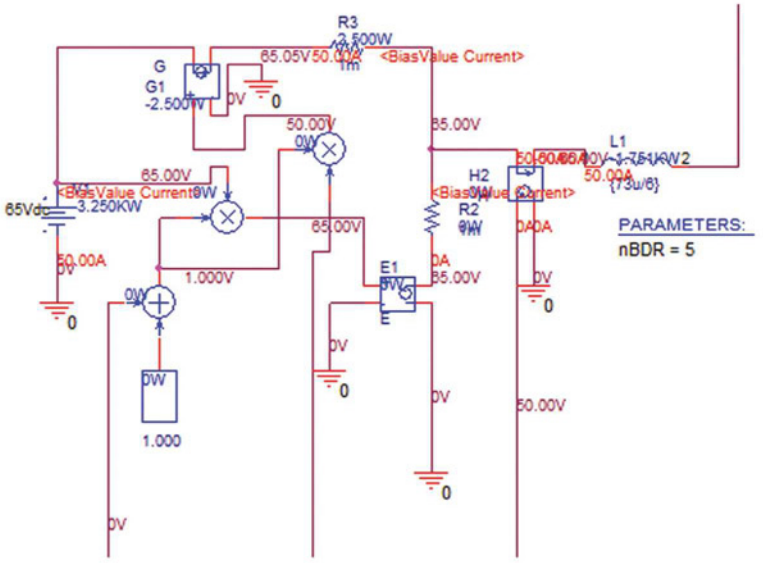


Figure 9: BDR P-Spice model

systems and not produce or be susceptible to interference.

The goal of electromagnetic compatibility (EMC) analyses is to evaluate the conducted emissions on the power bus for worst-case configurations. These conducted emissions (CE) are then compared with the specified conducted susceptibility (CS) of the bus user's equipment.

These analyses prove the coherence between the following specifications:

- Bus users' conducted emissions;
- PRU (power regulation unit) conducted emissions;
- PRU conducted susceptibility;
- Bus users' conducted susceptibility.

CE Parameters

Power-bus users can be sorted into two groups: platform equipment and payload equipment. The nominal contribution of platform equipment to the global conducted emission may be neglected, compared to the payload equipment's contribution. Therefore, in this preliminary analysis, the electric power conditioner (EPC) is assumed to be the sole bus user generating conducted emissions.

These parts of the global system affect the conducted emissions:

- PRU;
- Harness between PRU and the payload distribution unit (PDIU);
- Harness between the PDIU and the EPC;
- EPC input filters connected to the power bus.

PRU Parameters

PRU parameters that influence conducted emissions include:

- Bus capacitance value;
- PRU functioning mode in intra-domain (S3R, discharger regulator (BDR) or BCR) or in inter-domain (S3R/BDR, S3R/BCR or BCR/BDR) transition;
- PRU output impedance (between the regulated point and the output connectors);
- Battery characteristics;

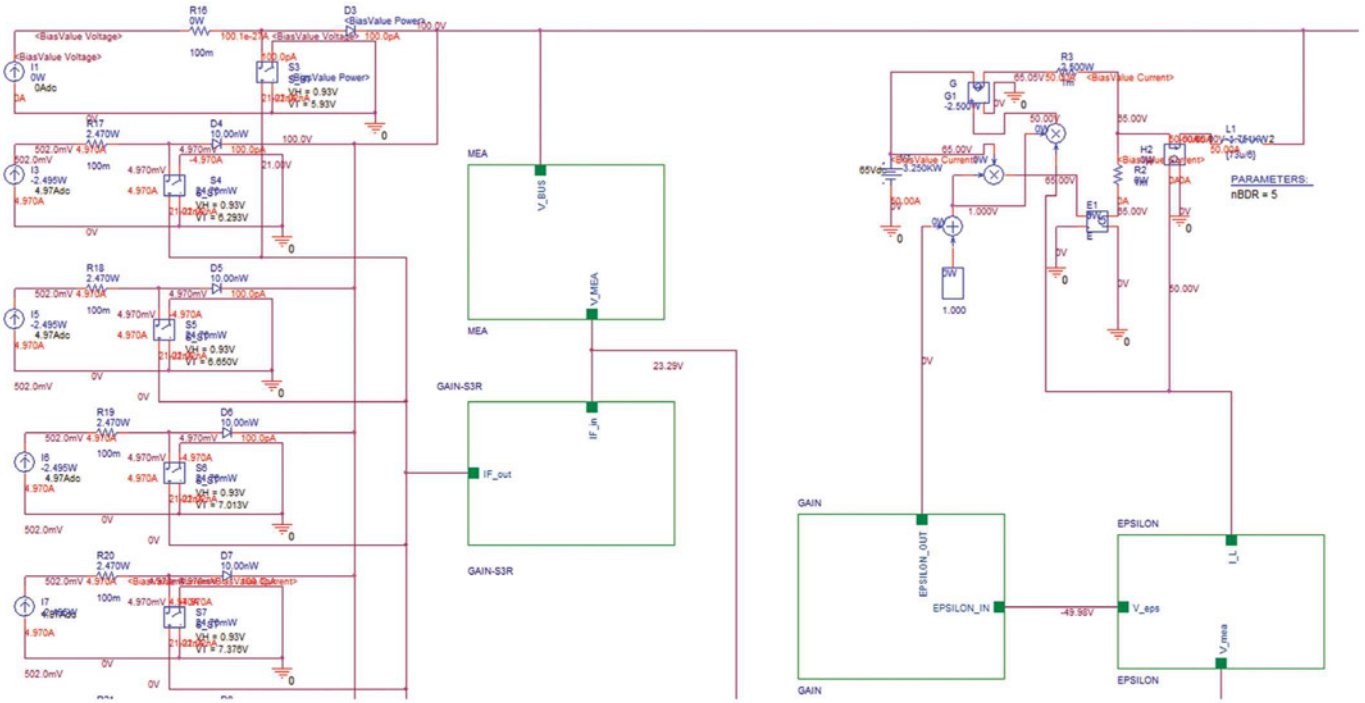


Figure 10: P-Spice model of the power regulation system in S3R-BDR inter-domain

- Solar array characteristics.

Three functioning PRU modes are then analyzed:

- Day regulation (S3R) by solar arrays, taking into account the worst case, which is end-of-life SA current and a S3R section failure.
- Night regulation on BDR, taking into consideration the failure case (one BDR less on each battery).
- Inter-domain S3R-> BDR, with the worst case taking into account an S3R section failure (or the first S3R section).

A PRU P-Spice dynamic model can be used to analyze conducted emissions for different modes. S3R/BCR and BDR/BCR inter-domain transitions have not been analyzed, as the sizing case is the S3R/BDR transition.

Harness Parameters

The EMC aspects depend mainly on the harness inductance values and less so on the resistance. The harness characteristics from PRU to EPC input are:

- between PRU and PDIU harness;
- between PDIU and EPC harness.

EPC And Traveling-Wave-Tube 's Parameters

EPC-conducted emissions are caused mainly by two different phenomena:

- parasitic currents generated by the internal electronics (such as the DC/DC converter);
- currents resulting from pulsed operating mode (TDMA operation) filtered by the EPC input filter.

Full Drive Operation

The DC/DC converter commutating at a frequency higher than 20kHz causes parasitic currents with a spectral domain of a few tenths of kHz. The maximum specified conducted emission for EPC while operating in constant drive is:

- 90dBµA from 30Hz-100kHz;
- - 20dB/decade from 100kHz-10MHz;
- 50dBµA from 10MHz-50MHz.

The maximum specification for equipment with power lower than 100W and other satellite equipment is 10dB less. Calculations are based on the following specifications:

Pulsed Functioning

The TWTs pulsed current is P-Spice-modeled by a rectangular wave-shape current generator at the EPC input filter's output.

The following relation gives the peak-peak amplitude of this current:

$$I_{pp} = (P_{full\ drive} - P_{no\ drive})/V_{input\ EPC} \quad (1)$$

Traveling Wave Tube Amplifiers' Characteristics

The characteristics of the expected TWTAs (linearized channel amplifier (LCAMP) + EPC + TWT) are displayed in Table 1. In TDMA mode, the peak-to-peak current was measured to be 1.78A for Ku band TWTs and 0.81A for C band TWTs.

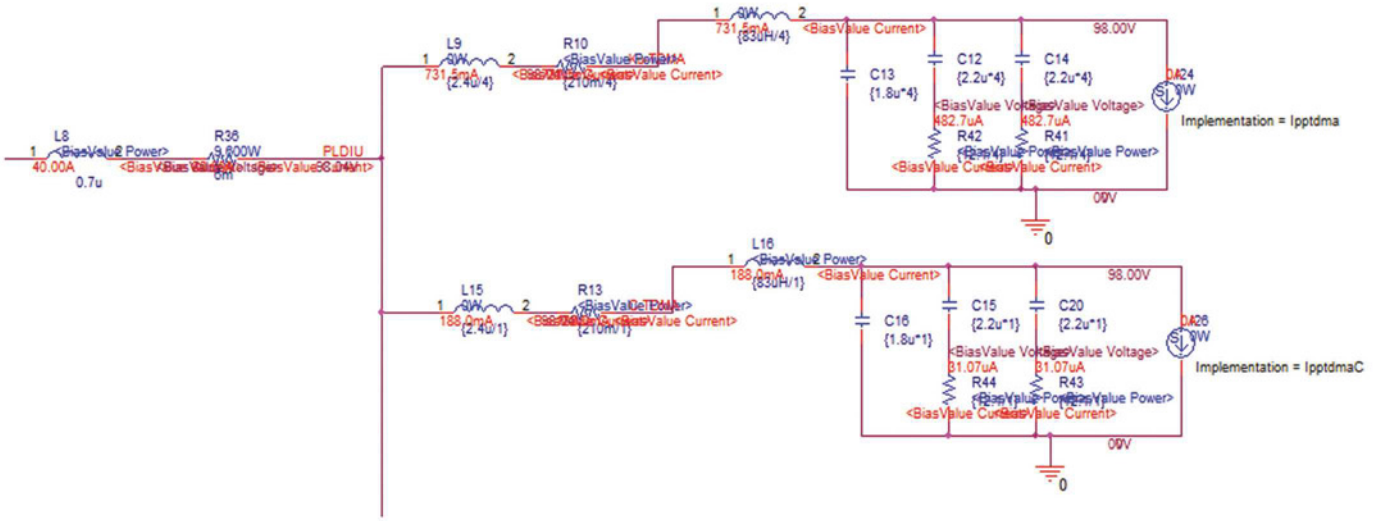


Figure 11: Payload (electrical power conditioner) P-Spice model

Input Filter

The EPC's input filters modify the conducted emissions:

- A transfer function of the EPC filters in TDMA mode modifies the injected current toward the PRU.
- Capacitances of the input filters reduce the bus drop voltage.

Admissible Conducted Susceptibility

In this analysis, the simulations aim to evaluate the following characteristics:

- Injected current by the bus users toward the PRU, which must be compared to the PRU current susceptibility specification;
- Voltage ripple and transients induced at the star point and at the bus users' inputs (self-compatibility), for comparison with bus users' voltage CS specifications.

Equipment Ripple Susceptibility Specification

At equipment input, ripple specification is a sine signal with the following characteristics:

- $2V_{rms}$ from 30Hz-500Hz,
- -20dB/decade from 500Hz-2kHz,
- $0.6V_{rms}$ from 2kHz-50MHz.

Current Susceptibility Limit of the PRU

The PRU conducted susceptibility is shown in Figure 14.

Full Drive Operation

Conducted Emissions Towards PRU

Any contribution from the platform equipment is neglected as their conducted emission (in nominal mode) is 10dB lower than EPC with power higher than 100W. The maximum EPC conducted emissions in constant drive are:

- 90dBµA (32mA) from 30Hz-100kHz;
- -20dB/decade from 100kHz-10MHz;
- 50dBµA (0.32mA) from 10MHz-50MHz.

As conducted emissions of the 20 operational TWTAs are not correlated, the total payload current is calculated by a quadratic summation. The result can be seen in Figure 15 and compared to the PRU conducted susceptibility specification. Minimum CE/CS margin is then 10.2dB in nominal mode.

Bus Users Conducted Emission

Voltage induced at EPC input is calculated using the PRU output and harness impedances:

- Output PCU inductance: 300nH
- PCU/PLDIU : L = 0.7µH, R = 6mΩ
- PLDIU/EPC : L = 2.4µH, R = 210mΩ.

Even without CS, the PRU ripples at (PRU specification) are:

- 0.3V from 30Hz to 1kHz
- - 20dB/decade
- 0.15V from 2kHz to 50MHz.

The PRU ripple is taken into account by a quadratic summation with the inducted voltages. The Bus users' CE/CS margins are displayed in Table 2. The minimum CE/CS margin is 12.4dB.

TDMA Operation

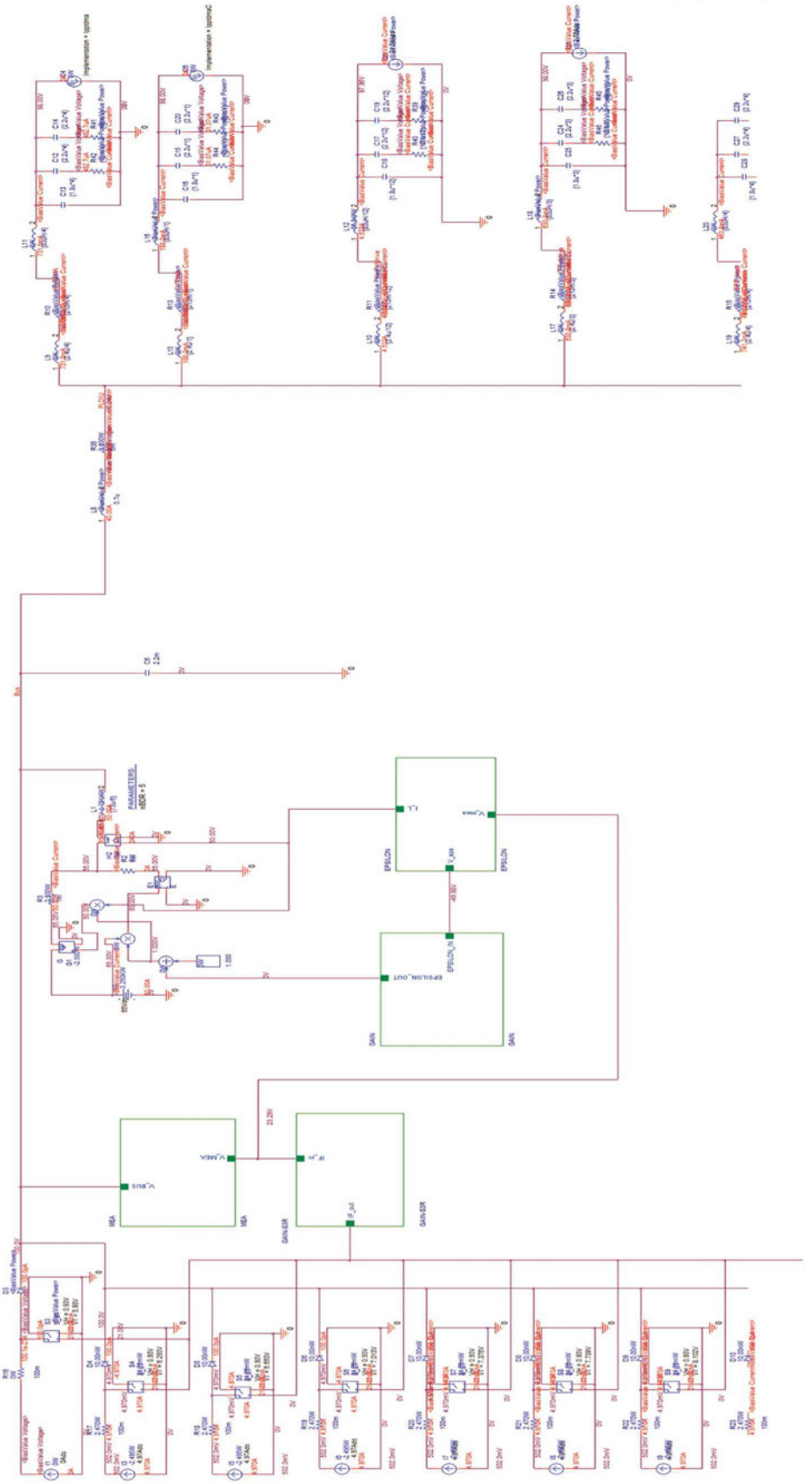
Number of TWTs In Pulsed Functioning

The TDMA requirement is that in synchronous mode:

- 3 Ku band, 1 C band TWTs;
- 4 Ku band TWTs.

TWTs can operate simultaneously in pulsed mode from 'no drive' up to full drive for frequencies lower than 1kHz. The maximum TDMA current is then $7.2A_{pp}$ for the 4 Ku band TWTs on TDMA mode. The PRU conducted susceptibility limits the admissible TDMA current, and as such the number of TWTs operating in pulse mode. The PCU conducted susceptibility is $20A_{pp}$ for square signal at low frequencies. At 500Hz, PCU conducted susceptibility starts to decrease. At 1kHz, the PCU conducted susceptibility is $7.8A_{pp}$ square. TDMA requirements can thus be satisfied for all three configurations. But if the number of TWTs in pulse mode is 4 Ku band, 1 C band or more, the TDMA current would exceed the qualified PCU conducted susceptibility at 1kHz.

Figure 12: P-Spice Modelling of CSEPS



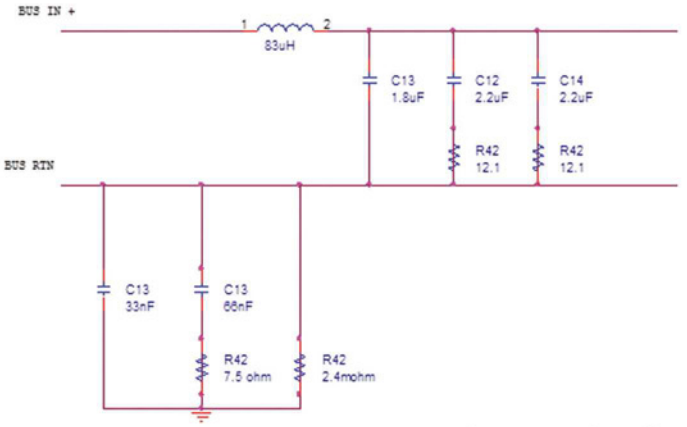


Figure 13: EPC input filter

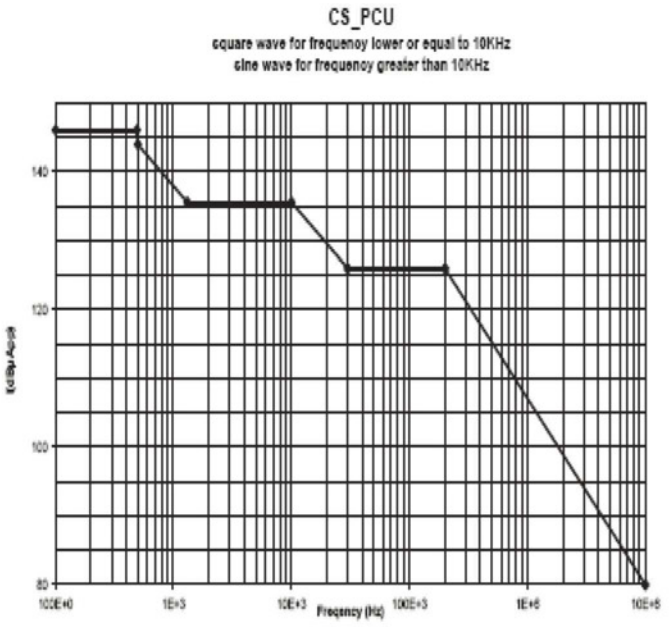


Figure 14: PRU conducted susceptibility

Ripple in TDMA Operation

The PRU P-Spice model evaluates the bus ripple generated in TDMA mode. EPC input filters are added to the PRU P-Spice model as they reduce the bus drop voltage. The PDIU ripple and the input EPC ripple in TDMA mode are evaluated and compared to the bus users' conducted susceptibility. The input voltage of EPC that does not commute is roughly the PDIU voltage.

S3R/BDR Intermode Functioning (Worst Case)

Maximum peak-peak amplitude arises in case of a balanced intermode transient, i.e. when half of the TDMA current is delivered by the BDR and half by the S3R.

Figure 15: Comparison CE Payload and CS-PRU

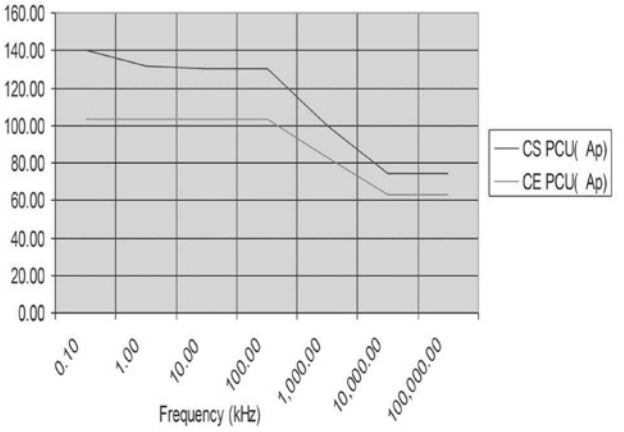


Figure 16: TDMA 6.15 A_{pp} 100Hz S3R-BDR intermode at 3 Ku, 1 C band

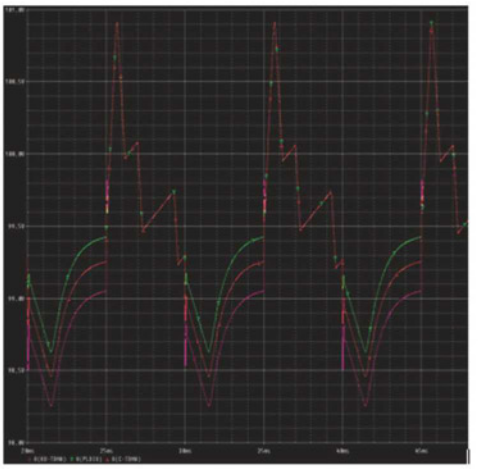


Figure 17: TDMA 7.2A_{pp} 100Hz S3R-BDR intermode at 4 Ku band

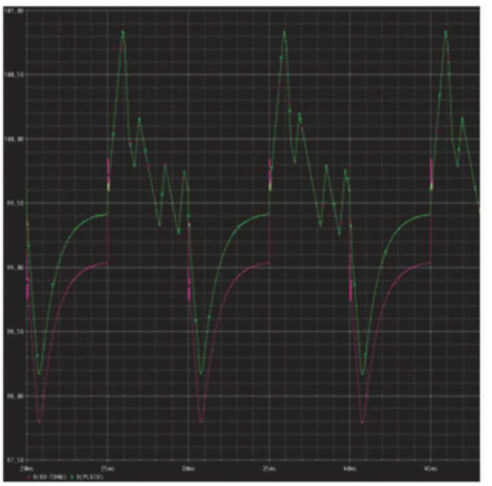
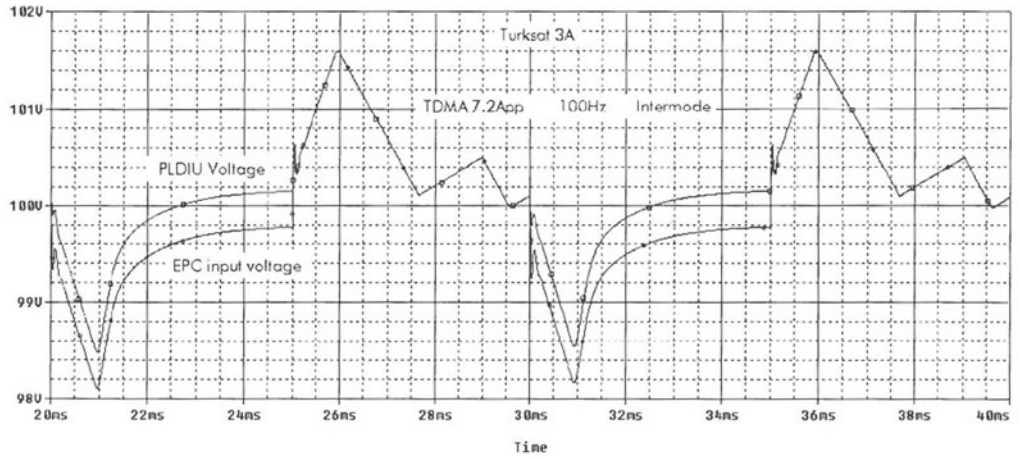


Figure 18: TURKSAT 3A satellite's TDAM 7.2App 100Hz S3R-BDR intermode values



For a constant TDMA current, the higher the frequency, the lower the peak-to-peak ripples. Indeed, for TDMA frequency above 100Hz, the bus voltage is not yet stabilized in its regulation zone where the next current transient occurs. TDMA ripples at 100Hz and 500Hz are presented in Tables 3 and 4.

The CE/CS margin at the equipment's input is 4.3dB in the worst case (intermode with failure). This margin is sufficient as analysis has been realized for the worst case. In consequence, an additional CE/CS margin is not necessary to take into account any calculation/measurement uncertainties. The S3R-BDR intermode at 100Hz for 3 Ku, 1 C Band and 4 Ku Band; configurations are shown in Figures 16 and 17.

TURKSAT 3A's values of TDAM 7.2A_{pp} 100Hz S3R-BDR intermode results are shown in Figure 18.

Summary

A P-Spice model of a communication satellite's electrical power system has been presented in this article. With this model an optimal design has been created that offers cost-effective solutions when considering the big budgets of communications satellites.

The model is then validated with CE analyses and the figures compared with a real-life satellite in orbit, TURKSAT, concluding that:

- In full drive with 20 TWTAs operating, the minimal CE/CS margins are higher than 10dB.
- 4 Ku band TWTs or 3 Ku band + 1 C band TWTs can operate simultaneously in pulsed mode up to 1kHz.
- In worst case, the ripple in TDMA mode is compliant with equipment susceptibility specification.

	Number of installed TWTs	Number of operational TWTs	Full drive (W)	No drive(W)
Ku-band	20	16	198	65
C-band	5	4	90.75	29.8

Table 1: TWTAs' characteristics

Frequency	CE (V_p) Bus users	CS (V_{rms}) Bus users	CE/CS margin (dB)
0.1 kHz	0.30	2	19.5
1 kHz	0.30	1	13.5
5 kHz	0.15	0.6	15.0
20 kHz	0.15	0.6	14.9
50 kHz	0.16	0.6	14.2
200 kHz	0.20	0.6	12.4
1 MHz	0.20	0.6	12.4

Table 2: CE/CS margins

TDMA Frequency	TDMA Current	PFLDIU Ripple	Input EPC Ku ripple	Input EPC C ripple	Equipment CS (spec.)
< 100Hz (50Hz)	6.15A_{pp}	2.53V_{pp}	2.90V_{pp}	2.70V_{pp}	5.6V_{pp}
1 kHz	6.15A_{pp}	0.614V_{pp}	0.986V_{pp}	0.783V_{pp}	2.8V_{pp}

Table 3: Bus ripple in TDMA operation at 3 Ku, 1 C band

TDMA Frequency	TDMA Current	PFLDIU Ripple	Input EPC Ripple	Equipment CS (spec.)
<100 Hz (50 Hz)	7.2A_{pp}	2.67V_{pp}	3.04V_{pp}	5.6V_{pp}
1 kHz	7.2A_{pp}	0.912V_{pp}	0.535V_{pp}	2.8V_{pp}

Table 4: Bus ripple in TDMA operation at 4 Ku band

EUROPEAN MICROWAVE WEEK 2015
PALAIS DES CONGRÈS, PARIS, FRANCE
6 - 11 SEPTEMBER 2015

EuMW 2015
FREEDOM THROUGH MICROWAVES

EUROPEAN MICROWAVE WEEK
PALAIS DES CONGRÈS DE PARIS, FRANCE
6 - 11 SEPTEMBER 2015
www.eumweek.com

EUROPE'S PREMIER MICROWAVE, RF, WIRELESS AND RADAR EVENT

THE CONFERENCES (6 - 11 SEPTEMBER)

- European Microwave Integrated Circuits Conference (EuMIC) 7th – 8th September 2015
- European Microwave Conference (EuMC) 7th –10th September 2015
- European Radar Conference (EuRAD) 9th – 11th September 2015
- Plus Workshops and Short Courses (From 6th September 2015)
- In addition EuMW 2015 will include the 'Defence, Security and Space Forum'

DISCOUNTED CONFERENCE RATES

Discounted rates are available up to and including 6th August 2015.

Register NOW and SAVE!

THE FREE EXHIBITION (8 – 10 SEPTEMBER)

ENTRY TO THE EXHIBITION IS FREE! Register today to gain access to over 300 international exhibitors and take the opportunity of face-to-face interaction with those developing the future of microwave technology.

EuMA European Microwave Association

Official Publication: Microwave Journal

Organised by: horizon house

Supported by: IET The Institution of Engineering and Technology

Co-sponsored by: MTT-S

Co-sponsored by: IEEE

EuMIC 2015
The 10th European Microwave Integrated Circuits Conference
Co-sponsored by:

45TH EUROPEAN MICROWAVE CONFERENCE 2015
The 45th European Microwave Conference
Co-sponsored by:

EuRAD 2015
The 12th European Radar Conference
Co-sponsored by:

Register online now as a delegate or visitor at:

www.eumweek.com

www.electronicsworld.co.uk

Electronics WORLD

T&M supplement

Teledyne LeCroy's WaveSurfer 10 Oscilloscopes:

1 GHz Power with no Compromise at Great Price

eXtreme Low Power MCUs Extend Battery Life

Low Sleep Currents with Flexible Wake-up Sources

- Sleep current down to 9 nA
- Brown-Out Reset down to 45 nA
- Real-Time Clock down to 400 nA

Low Dynamic Currents

- As low as 30 µA/MHz
- Power-efficient execution

Large Portfolio of XLP MCUs

- 8–100 pins, 4–128 KB Flash
- Wide selection of packages, including chip scale packages

Battery-Friendly Features

- Enable battery lifetime > 20 years
- Operate down to 1.8V with self write and analog functions
- Low-power supervisors for safe operation (BOR, WDT)

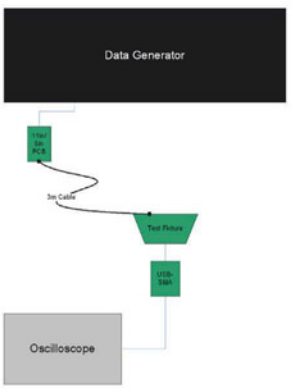
Flexible Peripheral Set

- Integrated USB, LCD, RTC and touch sensing
- Eliminates costly external components

microchip DIRECT
www.microchipdirect.com

MICROCHIP
www.microchip.com/xlp

> CONTENTS



COVER SUPPLIED BY TELEDYNE LECROY – MORE ON P48/49

> TREND

ADVANCEMENTS IN TEST EQUIPMENT WILL CENTRE AROUND LTE AND M2M COMMUNICATIONS

Wireless communication is a focal point for business development, and wireless test equipment users such as network operators and service providers foresee significant opportunities for manufacturers in machine-to-machine (M2M) communication and the long-term evolution (LTE) network infrastructure. Hence, developments in wireless communication test equipment will revolve around LTE and M2M solutions for easy deployment across the live network infrastructure.

Frost & Sullivan recent "*Analysis of End Users' Perspective on the Global Wireless Communication Test Equipment Market*" finds that while North America continues to offer significant opportunities for wireless communication testing and monitoring vendors, the Asia Pacific is fast becoming a hotbed for growth. The study is based on a survey of wireless test equipment customers, including network operators, network equipment manufacturers, contractors and telecom and wireless consulting firms.

"While M2M and the Internet of Things are here to stay, the challenges associated with incorporating them are quite unique and therefore require inventive solutions for testing at every stage of the life cycle," said Frost & Sullivan Measurement and Instrumentation Research Analyst Rohan Joy Thomas. "Respondents rated interoperability as the most significant challenge, one that will be compounded by the proliferation of M2M communications and heterogeneous networks."

Innovative solutions are also necessary to tackle issues stemming from the implementation of small cells, distributed antenna systems, big-data analytics, self-optimising networks (SONs), cloud computing and virtualisation. With end users trying to bridge the gap between network monitoring capabilities and research and development (R&D), solutions that effectively bring field test capabilities closer to the lab environment will gain traction.

"Despite imminent difficulties, respondents noted that they expect a substantial rise in the deployment of SONs, big-data analytics, virtualization, software-defined networks and cloud computing by 2021," added Thomas. "Cloud computing, in particular, will surge ahead as end users look to further optimise IT operations in the global market."

All of these systems will need testing and monitoring equipment and even customization of equipment to end-user requirements to proactively meet demand.

Frost & Sullivan's report "Analysis of End Users' Perspective on the Global Wireless Communication Test Equipment Market" can be bought on https://www.frost.com/mabe

WaveSurfer 10

1 GHz Power with no Compromise at Great Price

Many 1 GHz oscilloscopes are available at attractive entry-point prices, however, they are often limited in sample rate, memory or features. The WaveSurfer 10 provides uncompromised 1 GHz performance with up to 10 GS/s per channel and 32 Mpts of memory.

With the addition of the Advanced Debug Toolkit, the WaveSurfer 10 becomes an unparalleled debug and analysis machine adding 10 GS/s sample rate on 4 channels, 32 Mpts of memory, sequence mode, history mode, 13 additional math functions, and 2 simultaneous math traces.

The WaveSurfer 10 combines the MAUI advanced user interface with powerful waveform processing, in addition to advanced math, measurement and debug tools, to quickly analyze and find the root cause of problems. With a 10.4" touch screen display, high performance hardware, and compact form factor the WaveSurfer 10 is unique among 1 GHz oscilloscopes. MAUI is built for simplicity. Basic waveform viewing and measurement tools as well as advanced math and analysis capabilities are seamlessly integrated in a single user interface. Time saving shortcuts and intuitive dialogs simplify setup and shorten debug time.

ADVANCED TOOLS FOR WAVEFORM ANALYSIS

Save time when working with embedded controllers by adding high-performance mixed signal capability with the WaveSurfer 10. Capture digital signals up to 250 MHz with up to 10 Mpts/Ch memory, 1 GS/s and 18 channels. Quickly and easily isolate specific serial data events with I2C, SPI, UART, RS-232, USB 1.0/1.1/2.0, USB2-HSIC, 10/100Base T ENET, Audio (I2S, LJ, RJ, TDM), MIL-STD-1553, ARINC 429, MIPI D-PHY, DigRF, CAN, CAN FD, LIN, FlexRay, SENT, Manchester, and NRZ trigger and decode options.

LabNotebook is a one-button tool to save and restore waveforms, measurements and settings without navigating multiple menus. Custom reports can be created and easily shared; saved waveforms can be measured and analyzed later both on the oscilloscope or offline using the WaveStudio PC Utility.

WaveStudio is a fast and easy way to analyze acquired waveforms offline. Offline tools include x and y axis cursors for quick measurements and 21 built-in automatic measurements for most precise and accurate results. WaveStudio can also connect to the oscilloscope for direct data transfer to the PC. Data saved with LabNotebook can be shared with others using WaveStudio for easy collaboration.

Built for Simplicity Access shortcuts to analysis tools by touching the waveform – Configure parameters by touching measurement results – Channel, timebase and trigger descriptors provide easy access to controls without navigating menus – Shortcuts to commonly used functions are displayed at the bottom of the channel, math and memory menus.

ADVANCED DEBUG TOOLKIT FOR ADDITIONAL POWER

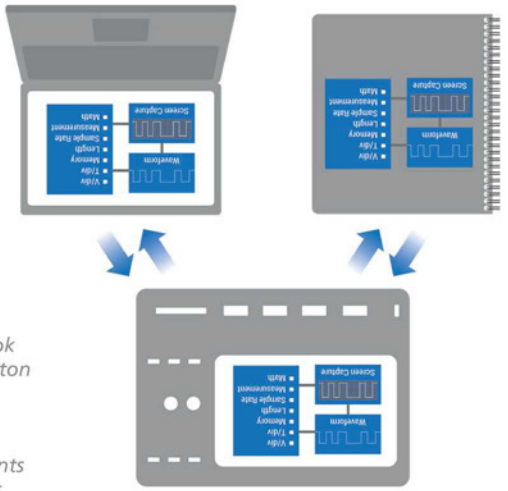
The WaveSurfer 10M includes the Advanced Debug Toolkit software which makes it an unparalleled debug and analysis machine. The high sample rate of 10 GS/s on all 4 channels, 32 Mpts of memory, sequence mode segmented memory, history mode waveform playback, 13 additional math functions, and 2 simultaneous math traces, all included in this powerful debug package, enable the WaveSurfer 10M to perform advanced analysis on long captures with 10x oversampling to find the root cause of problems.

Advanced Waveform Capture with Sequence Mode

Use Sequence mode to store up to 5,000 triggered events as "segments" into memory. This is ideal when capturing many fast pulses in quick succession or when capturing events separated by long time periods. Sequence mode provides timestamps for each acquisition and minimizes dead-time between triggers to less than 1 µs. Combine Sequence mode with advanced triggers to isolate rare events over time and analyze afterwards.

EMBEDDED CONTROLLER DESIGN AND DEBUG

Teledyne LeCroy's versatile WaveSurfer 10 mixed signal oscilloscope combines the powerful



LabNotebook is a one-button tool to save and restore waveforms, measurements and settings

Sequence mode stores up to 5,000 triggered events as "segments" into memory. This is ideal when capturing many fast pulses in quick succession or when capturing events separated by long time periods.

WaveSurfer 10 with the flexibility of digital inputs using the MS-250. In addition, the many triggering and decoding options turn the WaveSurfer 10 into an all-in-one analog, digital, and serial data trigger, acquisition, and debug machine.

High-performance Mixed Signal Capabilities

Embedded controller design and debug involves capturing and viewing a number of different types of signals. These signals are typically a mix of analog, digital, and serial data waveforms from a combination of analog sensors, microcontrollers and peripheral devices. With the ability to capture digital signals with speeds up to 250 MHz and long memory of 10 Mpts/Ch the WaveSurfer 10 provides unmatched mixed signal performance. The WaveSurfer 10 is the ideal tool for testing embedded systems with 8-bit microcontrollers or slower digital signals. With 18 digital inputs each with 250 MHz maximum input frequency and 10 Mpts/Ch memory, the WaveSurfer 10 plus MS 250 is an outstanding value and provides a complete set of tools for embedded system testing.

Extensive Triggering

The WaveSurfer 10 has extensive digital trigger capabilities. Normal oscilloscope triggers will operate on digital inputs. Cross-pattern triggering allows for simple or complex trigger patterns to be setup with any combination of analog and digital channels. Event triggering can be configured to arm on an analog signal and trigger on a digital pattern.

WIDE RANGE OF SERIAL TRIGGER AND DECODE SOLUTIONS

Debugging serial data busses can be confusing and time consuming. The serial data and decode options for WaveSurfer 10 provide time saving tools for serial bus debug and validation.

The serial data trigger will quickly isolate events on a bus eliminating the need to set manual triggers and hoping to catch the right information. Trigger conditions can be entered in binary or hexadecimal formats and conditional trigger capabilities even allow triggering on a range of different events. Protocol decoding is shown directly on the waveform with an intuitive, color-coded overlay and presented in binary, hex or ASCII. Decoding on the WaveSurfer 10 is fast even with long memory. Zooming in to the waveform shows precise byte by byte decoding. To further simplify the debug process all decoded data can be displayed in a table below the waveform grid. Selecting an entry in the table with the touch screen will display just that event. Additionally, built-in search functionality will find specific decoded values.

SPECTRUM AND POWER ANALYZER

Simple Frequency Domain Analysis

Get better insight to the frequency content of any signal with use of the Spectrum Analyzer mode on the WaveSurfer 10. This mode provides a spectrum analyzer style user interface with controls for start/stop frequency or center frequency and span. The unique peak search automatically labels spectral components and presents frequency and level in an interactive table. Utilize up to 20 markers to automatically identify harmonics and monitor how the spectrum changes over time using the spectrogram which can display a 2D or 3D history of the frequency content.

Power Analyzer Automates Switching Device Loss Measurements

Quickly measure and analyze the operating characteristics of power conversion devices and circuits with the Power Analyzer option. Critical power switching device measurements, control loop modulation analysis, and line power harmonic testing are all simplified with a dedicated user interface and automatic measurements. Areas of turn-on, turn-off, and conduction loss are all identified with color-coded waveform overlays for faster analysis. Power Analyzer provides quick and easy setup of voltage and current inputs and makes measurements as simple as the push of a button. Tools are provided to help reduce sources of measurement errors and the measurement parameters provide details of single cycle or average device power losses.

Beyond the advanced power loss measurement capabilities, the Power Analyzer modulation analysis capabilities provide insight to understand control loop response to critical events such as a power supply's soft start performance or step response to line and load changes. The Line Power Analysis tool allows simple and quick pre-compliance testing to EN 61000-3-2. ■

teledynelecroy.com

WLAN TRAFFIC OFFLOAD – BYPASS FOR CROWDED MOBILE NETWORKS

BEFORE THE LAUNCH OF WLAN TRAFFIC OFFLOAD, THE STANDARDIZATION BODIES OF 3GPP AND IEEE HAD TO EXPAND A NUMBER OF STANDARDIZED PROTOCOLS AND PROCEDURES. IN THIS ARTICLE, THOMAS A. KNEIDEL, PRODUCT MANAGER FOR RF TEST AT ROHDE & SCHWARZ IN MUNICH, FOCUSES ON HOW THIS FEATURE WORKS WITH LTE

WLAN traffic offload – the rerouting of mobile data traffic to WLAN networks – is an interesting alternative for network operators to cope with the constantly growing data volume. Now that the specification has been completed, test operation for the new feature is the step before the official launch. The test systems play a key role, since they have to ensure smooth interoperation of a wide variety of different components used in these complex systems.

Even the most advanced mobile networks will reach their capacity limits before long, mainly due to the increasing traffic in videos via smartphones and tablets. Since the lion's share of the resultant data volume is generated inside buildings, WLANs can be used as economical alternatives augmenting mobile networks, provided that access points are available.

The two types of network ideally complement each other – mobile networks provide comprehensive coverage for mobile services, while broadband WLANs reduce the load on mobile networks for indoor applications.

The underlying technology is referred to as WLAN traffic offload; it basically works in combination with any mobile communications standard (GSM, WCDMA, CDMA2000, LTE, etc). The advantages for network operators are obvious. Almost all modern mobile devices have a WLAN interface. The acquisition costs for access points (WLAN access points – WLAN AP) are relatively low. In addition, WLANs use two license-free frequency blocks at 2.4GHz and 5GHz within the ISM bands, outside those assigned to cellular standards.

Before the launch of WLAN traffic offload, the standardization bodies of 3GPP and IEEE had to expand a number of standardized protocols and procedures. Here is how this feature works with LTE.

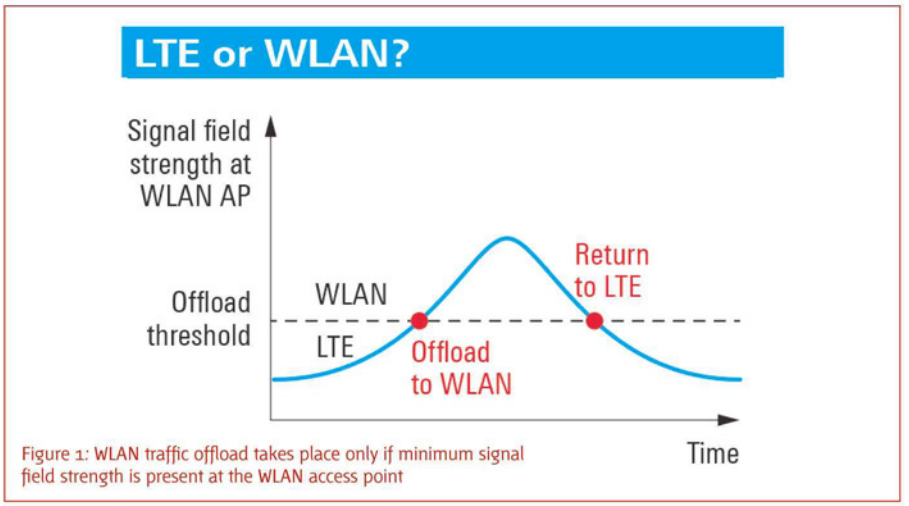


Figure 1: WLAN traffic offload takes place only if minimum signal field strength is present at the WLAN access point

AUTHENTICATION, AUTHORIZATION AND POLICY

When gaining access to the core network of a mobile network operator via WLAN, it must be ensured that access is authorized. As with the cellular standards, this is verified using the SIM card in the mobile device. To facilitate a seamless, password-free transition, the same procedure is applied as with a secure WLAN AP. Protocols have been defined to enable the SIM card data to be automatically compared via WLAN on the network operator's authentication server (extensible authentication protocols – EAP) and incorporated into the diverse cellular standards.

> *"The IEEE 802.11u amendment added further information to the beacons that a WLAN AP transmits every 100ms"*

Network operators can balance the load on their networks using a set of rules, known as policy. For this purpose, mobile devices are, for instance, informed what WLAN APs are available where and when for the offloading of which data services (audio or video telephony, Internet services, etc). This makes it easier – especially in metropolitan areas – to find WLAN APs suitable for offloading, and at the same time helps smartphones save energy.

The policy is distributed to the mobile devices by the access network discovery and selection function (ANDSF) server via Open Mobile Alliance (OMA) device management; subscribers can query the information where necessary.

Signal strength at the WLAN AP is also a key factor in the use of LTE-to-WLAN traffic offload. The mere presence of a WLAN AP is not sufficient; a specified minimum field strength must be available (Figure 1). When the required field strength is no longer present, the connection is terminated and the device returns to LTE.

Protection against eavesdropping is also required. Let us assume that a mobile subscriber makes a video call with a subscriber in the LTE network via a freely accessible WLAN AP. To ensure data protection, additional encryption is provided by establishing an IPsec tunnel to the smartphone via the WLAN AP, starting from the firewall in the LTE core network (Figure 2).

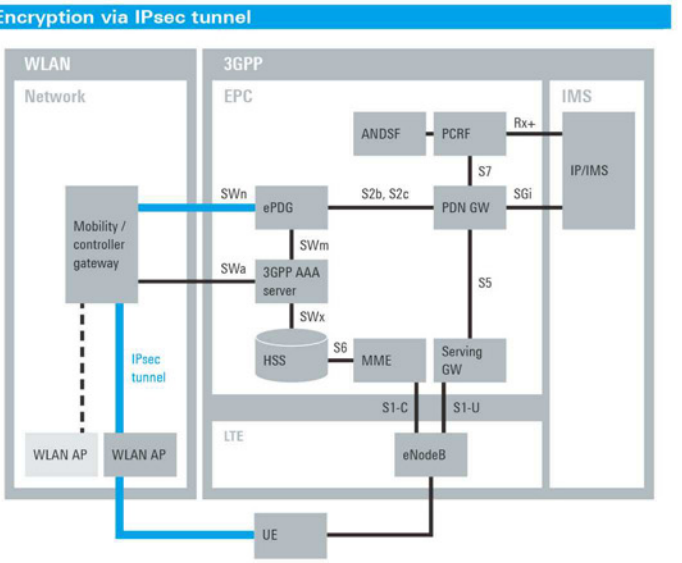


Figure 2: Protecting communications from unauthorized access: Additional encryption is provided by establishing an IPsec tunnel to the smartphone via the WLAN AP starting from the firewall in the LTE core network

ACCELERATED WLAN ACCESS

The IEEE 802.11 standardization group has expanded the WLAN access protocol in a new version (Amendment IEEE 802.11u) to include the access network query protocol (ANQP). This protocol automates and accelerates the WLAN access of smartphones to the mobile network. Even before the actual connection with the WLAN AP is made, the smartphone receives information about 3GPP mobile networks or roaming consortia that are accessible via the WLAN AP. The Wi-Fi Alliance issues a certificate (Wi-Fi Hotspot 2.0, also known as Passpoint) to ensure uniform implementation of the new standard and a maximum degree of interoperability for certified WLAN components.

The IEEE 802.11u amendment added further information to the beacons that a WLAN AP transmits every 100ms (Figure 3). Before the connection with the WLAN AP is actually established, which takes place after an authentication and association procedure, the smartphone can use the ANQP to determine via the new generic advertisement service (GAS) if a WLAN AP can be used for an offload.

An important precondition for the acceptance of WLAN traffic offload is an uninterrupted transition between the mobile network and a WLAN. No action or entry should be needed on the part of the subscriber; in the ideal case, the subscriber should not notice the transition at all.

Interruption-free continuation of IP-based services after a mobile cell change or change of the radio access technology (RAT) calls for IP flow mobility. In a world in which communication is based on client/server architecture, this requires intelligent address management with dynamic IP address assignment, which has been achieved with a number of protocol amendments by 3GPP and enhanced IP addressing.

VERIFICATION TEST SYSTEMS

Comprehensive tests need to be carried out to ensure that all system components are implemented uniformly and in conformity with the standards. The tests focus above all on the mobile device as the pivotal element of the standard amendment. The device under test (DUT), with its critical interface to the user, takes on vital significance in this scenario. In the tests, the DUT is connected to the test setup via both WLAN and LTE.

The test setup for LTE-to-WLAN traffic offload includes the following main components:

- Emulation of an LTE base station, including the LTE core network;
- Emulation of a WLAN AP (HotSpot 2.0 or Passpoint);
- Gateway/firewall at the entrance to the LTE core network from the WLAN end;

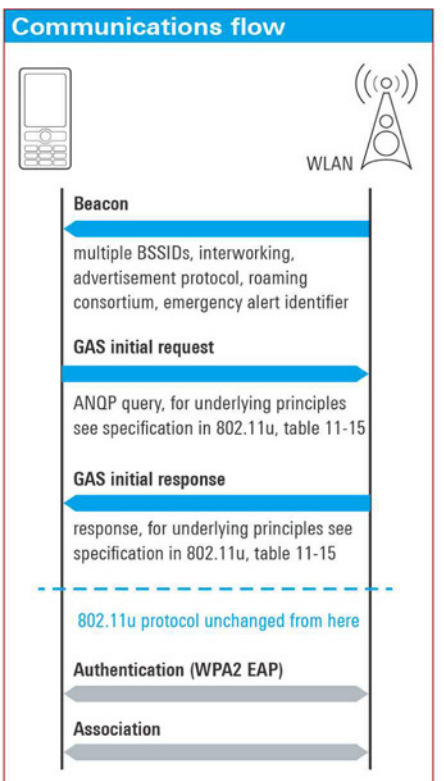


Figure 3: Additional information in the beacons provides smartphones with criteria as to whether a WLAN access point is suitable for traffic offload or not

Figure 4: The R&S CMW500 offers in a single box everything needed to verify LTE-to-WLAN traffic offload functionality

Figure 5: The R&S CMW cards graphical user interface for the R&S CMW500 makes it easy to compile signalling tests in line with the specification

- IMS server for implementing real-world applications such as video or speech telephony;
- Message analyzer for recording all protocol messages between the DUT and the WLAN AP and the LTE base station.

The individual components are either networked to form a test system or, as with a test platform for wireless devices like the R&S CMW500 wideband radio communication tester (Figure 4), integrated into a single device. As a general rule, to ensure that tests are reproducible, professional instruments should be used and the number of commercial system components kept to a minimum.

CUSTOM SOLUTIONS

For the integration of the LTE and the WLAN protocol stacks, tests on the lower protocol layers are needed in an early development phase. The required signalling tests can be performed with the test platform and suitable medium-level application programming interface (MLAPI) test scenarios.

The R&S CMW-KF650 option contains roughly 50 test scenarios, ranging from establishing a connection with the gateway of the LTE core network (ePDG) to authentication and changing the IP service from LTE to WLAN and back. The appropriate source code and interface description are also provided, allowing test scenarios to be adapted to individual requirements.

The MLAPI test scenarios offer a very wide range of testing options for the lower protocol layers, but require expert programming knowledge. An alternative could be R&S CMWcards, a graphical user interface resembling a card game. This tool makes it possible to compile signalling tests without any specific programming skills (Figure 5).

To ensure smooth communications, network operators specify test cases that all devices wishing to use their services must pass. For a number of network operators, Rohde & Schwarz offers options to verify LTE-to-WLAN traffic offload functionality.

The R&S CMW500 can be used as a callbox to develop and verify the WLAN traffic offload feature. In this case, tests range from verifying the DUT's RF characteristics to functional tests, including analysis of the LTE and WLAN protocol messages.

PROTOCOL ANALYSIS

The ability to record LTE and WLAN protocol sequences at the same time is a major bonus when verifying the process is operating according to standard, discovering errors or optimizing the process. The R&S CMWmars message analyzer could be used, for example, to verify if a smartphone has established a Hotspot 2.0 compliant connection with a WLAN AP. The message analyzer records data messages and protocol information across several layers of the ISO OSI model. Filters can be set to record precisely what is required.

The changeover of a data service, such as a video call, from LTE to WLAN should take place without interruption wherever possible and with no data packet loss. In addition to a visual check, this can be verified in detail using the message analyzer, which is also a valuable tool for error correction. Moreover, for data services, minimum stipulated data transmission rates are to be verified under a variety of conditions and operating modes. In general terms, such quality of service (QoS) criteria, including round-trip time, form part of comprehensive IP data analyses.

IN-DEVICE COEXISTENCE TEST

Ensuring operation in conformity with the standards is not the only vital issue when testing WLAN traffic offload functionality. Another focus is on determining interference between two radio standards used once within a mobile device and avoiding this interference as far as possible. In-device coexistence tests are performed to measure interference between the LTE transmitter and the WLAN receiver, and vice-versa, between the WLAN transmitter and the LTE receiver within a smartphone. To this end, for instance, a smartphone could transmit a video on LTE

band 7, while a receiver quality test (PER measurement) is carried out at the same time on WLAN channel 13, only 17MHz away. In the ideal case, no interaction will be detected here and the PER measurement will be the same without an LTE transmission.

As shown in Figure 6, possible mutual interference is particularly critical between WLAN in the 2.4GHz ISM band and the LTE frequency bands 7 and 40. While mutual interference between LTE band 40 and the WLAN channels needs to be investigated, it can be presumed that the interference caused by the transmission from LTE band 7 only affects WLAN reception.

Possible interferences between WLAN and LTE

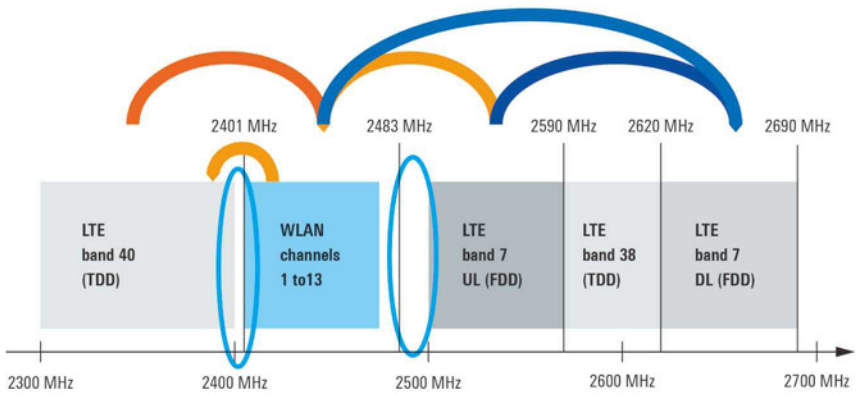


Figure 6: Mutual interference is particularly critical between WLAN in the 2.4GHz ISM band and the LTE bands 7 and 40

A MATTER OF TIME

Even if full use is made of the data transmission rates theoretically possible according to Shannon in today's mobile networks, it is only a matter of time before available capacities can no longer meet increased data throughput requirements. Alternative solutions need to be found. WLAN traffic offload is a promising technology that can significantly reduce the load on mobile networks. Following specification and standardization, there will now be a test phase prior to rollout, for which suitable test systems will be needed above all. ■

High definition oscilloscopes:
16-bit vertical resolution for signal analysis

The high definition mode increases the vertical resolution of the R&S®RTO and R&S®RTE oscilloscopes to up to 16 bit – a 256-fold improvement over 8-bit standard mode. Waveforms are sharper and show details that would otherwise be masked by noise. Users benefit from even more precise analysis results.

INCREASED RESOLUTION FOR PRECISE MEASUREMENT OF SMALL SIGNAL AMPLITUDES

High definition (HD) refers to the capability of the R&S®RTO and R&S®RTE oscilloscopes (Fig. 1) to be used for applications requiring high vertical resolution. This is especially the case when low-voltage components of a signal that also exhibits high-voltage components need to be analyzed in detail. One example is the measurement of switched-mode power supplies, where voltages across the switching device must be determined during the off and on times within the same acquisition. Because the voltage variations can be several hundred volts, a high resolution of more than 8 bit is required for precise measurement of small voltage components. Another example is amplitude-modulated signals with low modulation index as can be found in radar applications.

HD MODE OFFERS UP TO 16-BIT VERTICAL RESOLUTION

The R&S®RTO-K17 and R&S®RTE-K17 high definition options increase the vertical resolution of Rohde & Schwarz oscilloscopes up to 16 bit by applying a digital lowpass filter to the signal after it passes through the A/D converter. The filter reduces the noise, which increases the signal-to-noise ratio and improves resolution (Fig. 2). The bandwidth of the lowpass filter can be flexibly adjusted from 10 kHz to 1 GHz to match the characteristics of the applied signal. The lower the filter bandwidth, the higher the resolution and noise suppression (Table).

The increase in resolution leads to sharper waveforms, showing signal details that would otherwise be masked by noise (Fig. 3). To be able to analyze these signals in detail, the input sensitivity of the oscilloscopes has been increased to 500 µV/div. The R&S®RTO and R&S®RTE oscilloscopes have an excellent dynamic range and measurement accuracy thanks to their low-noise frontend and highly accurate single-core A/D converter. Switching on HD mode allows users to benefit from even more precise measurement results.

HD mode offers crucial advantages over high resolution decimation (also supported by Rohde & Schwarz oscilloscopes). Users know exactly what signal bandwidth is available due to explicit lowpass filtering, and there are no unexpected aliasing effects. Since HD mode is not based on decimation, the increase in resolution is not accompanied by a reduction in the sampling rate. When HD mode is switched on, the full sampling rate can be used, ensuring the best possible time resolution. Moreover, HD mode permits users to trigger on the signals with increased resolution, whereas high resolution decimation only takes place after the trigger unit.

REALTIME TRIGGERING ON SMALLEST SIGNAL DETAILS

The success of triggering on the smallest details in HD mode for more thorough examination depends greatly on the capabilities of the trigger system in use. The digital trigger system from Rohde & Schwarz has the sensitivity required to benefit from the high-resolution signal. Each of the up to 16-bit samples is checked against the trigger condition and can initiate a trigger. This means that the oscilloscopes are able to trigger on even the smallest signal amplitudes and isolate relevant signal events (Fig. 4).

Fig. 1: See more with up to 16-bit vertical resolution. The R&S®RTO-K17 and R&S®RTE-K17 high definition software options allow for a 256-fold increase in the oscilloscopes' vertical resolution.

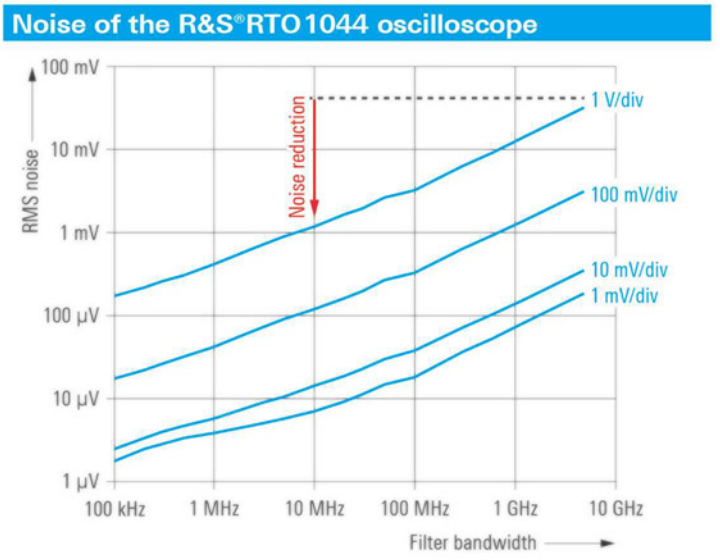


Fig. 2: Noise of the R&S®RTO1044 oscilloscope (4 GHz model) as a function of the set filter bandwidth of the R&S®RTO-K17 high definition option. Reducing the noise increases the signal-to-noise ratio, which improves resolution.

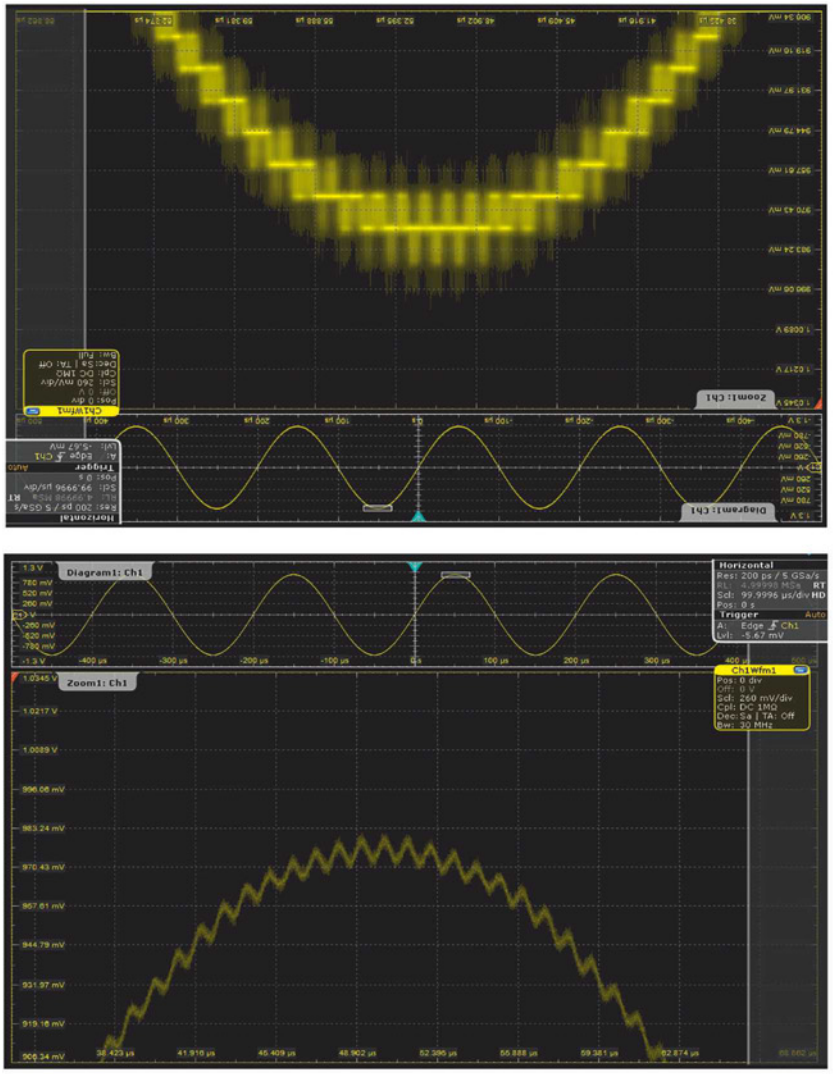


Fig. 3: Zoomed-in peak of a sine wave (a). HD mode is not activated. Only the quantization levels can be seen in the zoom window. When HD mode is switched on, the zoom window shows that another very low-amplitude sine wave is superimposed on the signal (b).

R&S®RTO	
Filter	**Resolution**
Inactive	8 bit
1 GHz	10 bit
500 MHz	12 bit
300 MHz	12 bit
200 MHz	13 bit
100 MHz	14 bit
50 MHz to 10 kHz	16 bit

R&S®RTE	
Filter	**Resolution**
Inactive	8 bit
500 MHz	10 bit
300 MHz	11 bit
200 MHz	12 bit
100 MHz	13 bit
50 MHz	14 bit
30 MHz to 10 kHz	16 bit

Table: Vertical resolution as a function of filter bandwidth

HIGH ACQUISITION RATE AND FULL FUNCTIONALITY FOR FAST MEASUREMENT RESULTS

Switching on HD mode does not compromise measurement speed or functions. Since the lowpass filtering, which improves resolution and noise suppression, is implemented in realtime in the oscilloscope's ASIC, the acquisition and processing rates remain high. The oscilloscope enables smooth operation, and measurement results are available quickly. All analysis tools, such as automatic measurements, FFT analysis and history mode, can also be used in high definition mode. ■

For more information, visit: ***www.scope-of-the-art.com/ad/press/highdefinition***

Sylvia Reitz, product manager oscilloscopes, Rohde & Schwarz

Fig. 4: The high sensitivity of the digital trigger in this example makes it possible to trigger on signal overshoots of less than 9 mV. At a vertical scale of 140 mV/div, this corresponds to only a fraction of one display division.

EXPELLING THE JITTER BUGS

LUCIO DI JASIO, ELECTRONICS ENGINEER AND TECHNICAL AUTHOR, EXPLAINS HOW TO TEST FOR JITTER TOLERANCE ON SUPER SPEED USB 3.0

Jitter tolerance (JTOL) on a Super Speed (SS) USB 3.0 receiver can be tested using a waveform generator and an oscilloscope. Data is looped back through the transmitter to the instrument – a data generator and analyser can do the same job. The received data can be compared with the one generated to count the errors. The data generator can also introduce jitter into the transmit data pattern to see how well the receiver copes.

TEST PROCEDURE

The connections from the data generator to the device under test (DUT) are specified by USB-IF in the Electrical Compliance Test Specification. The SMA connectors of the data generator should be connected to a USB-IF test fixture that has 28cm (device) or 12.7cm (host) of PCB trace going to a standard USB3 connector. From that connector, a 3m USB 3.0 cable can be attached to another USB-IF test fixture that splits out the transmit signals from the DUT to the data analyser through SMA cables and combines the transmit and receive signals into a standard USB connector to link the DUT. It is important that the SMA cables be phase- and attenuation-matched and connected to the test boards with proper torque (0.56Nm).

For loopback training, the data generator begins each test by configuring the SS port to enter loopback; see Figure 1. First, the data generator transmits low frequency periodic signals (LFPS) to imitate SS communications. The DUT then responds with an LFPS signal handshake. The data generator transmits the training sequence signal (TSEQ) with the proper noise applied, which trains the DUT to the TSEQ signal, adapting the internal filters to achieve the best performance.

> *"The connections from the data generator to the device under test are specified by USB-IF in the Electrical Compliance Test Specification"*

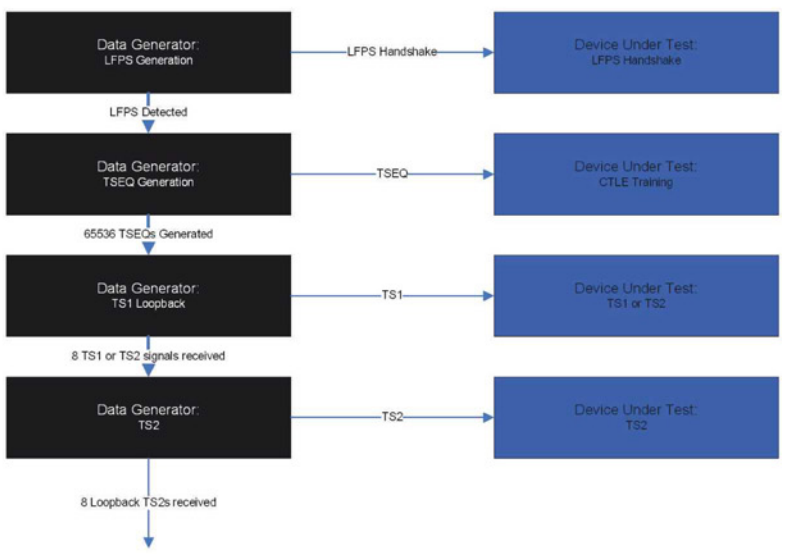


Figure 1: Loopback training sequence

Next, the data generator transmits the training sequence ordered set with the loopback bit enabled (TS1). The DUT responds with TS1 or TS2 while training, then sends eight TS2 or TS1 signals when complete. The data generator transmits TS2 also with the loopback set 16 times or more and the DUT responds with identical TS2 patterns. Finally, the data generator prepares for data packets and the DUT is in loopback.

For the noise test, after the DUT is trained, the generator will produce a random data pattern for about six seconds. The DUT loops back the same data and the two data sets are compared; only one error is allowed. The test then repeats for each noise profile.

CALIBRATION

Before a test can be run, the system needs to be calibrated, a procedure that contains numerous steps and many sources of error. It is always important to check and confirm the calibration before starting any compliance test.

De-emphasis calibration is done differently on different test products. Although the fundamental test itself is consistent across all platforms, every test vendor uses its own tools to calculate de-emphasis.

In this case, the data generator is connected directly to an oscilloscope through short SMA cables. The oscilloscope then measures the de-emphasis on a large packet of random data, generally 20µs of a 5GHz signal. The de-emphasis is then calculated and adjusted to ensure it is within the -3dB specification.

This de-emphasis calibration is important because the waveform changes across the PCB trace and 3m test cable, which affects the quality of the eye seen by the receiver. Microchip's SuperSpeed receivers can successfully compensate for small de-emphasis calibration errors through the adapt circuitry. This allows these products to be compatible with more devices and cable lengths on the market. This variation in cable length and receiver type cannot be tested in a compliance environment due to time constraints.

Once de-emphasis is calibrated, the data generator should be connected through the certification test fixtures to the oscilloscope. The generator is then set to generate a clean sine-wave with only random jitter (RJ) applied. The USB-IF SigTest tool can then be used to process the signal and calculate the RJ. RJ should be adjusted until it falls within specification (2.42ps ±10%). The sine wave gives the cleanest signal through the loss of the cable for a consistent RJ measurement.

Calibrating the RJ through the compliance test fixtures presents a few difficulties. The first is repeatability; jitter measurements always have uncertainty incorporated into the results. The second problem is that the jitter introduced is random, which adds uncertainty to the measurement. There will be variations between different oscilloscope captures even with everything else constant.

With sinusoidal jitter (SJ) calibration, the data generator should be set to generate a random data pattern with random jitter enabled. This signal can then be passed through the test fixtures into the oscilloscope. SigTest can again calculate the total jitter of the signal. SJ should then be applied and the measurement repeated. The difference in the total jitter for both measurements can be used to calibrate the SJ setting on the data generator. With this procedure, the errors in the measurements are added each time a measurement is taken, which creates a lot of variation between sequential calibration runs.

SOURCES OF ERROR

The first source of error is that the data pattern is random instead of a uniform sine-wave, which creates some small differences between total jitter measurements for each oscilloscope capture. The second source of error is that the jitter is measured at the end of the compliance test fixture. The high frequency loss through the PCB traces and 5m cable causes the edges of the waveforms to become smoother and smaller. Because the edges aren't as sharp, the jitter calculations will not be as consistent, as jitter is calculated based on the edge placement. Combine this uncertainty with the errors introduced by the random jitter applied previously, then take the measurement twice. It is possible that two calibration runs could yield data generator set points up to 4ps apart, which is equal to the entire specification range.

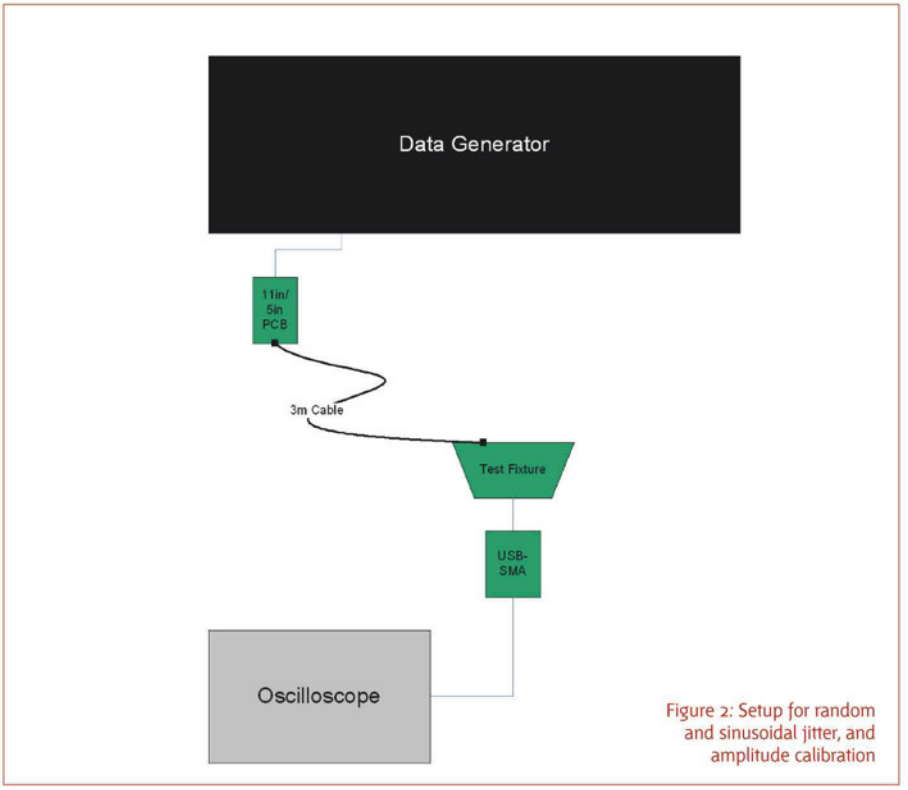


Figure 2: Setup for random and sinusoidal jitter, and amplitude calibration

Finally, the RJ, SJ and de-emphasis should be applied to a random data pattern and the signal passed through the compliance test fixtures. SigTest can calculate the eye measurements of the signal, and the amplitude can be adjusted to ensure that the smallest possible signal is being generated. The receiver should be tested with the minimum allowable margin on the eye of the random data.

Because all these measurements have some variation in their results, it is recommend that the calibration be run three to five times to check the reliability of the calibration algorithm. Figure 2 shows the setup for RJ, SJ and amplitude calibration.

EXTERNAL NOISE

Because the receiver test introduces noise into the signal coming into the DUT, any extra noise is going to add to the noise generated by the instrument. There are many external sources of noise that can impact the tested tolerance of the receiver. Power supplies, connector quality and PCB loss all can affect the results of the JTOL test.

If the voltage applied to the chip contains noise, it will be added to the signal as it travels through the receiver's buffers. This noise adds jitter to the total signal, causing the JTOL results to be lower than that of an ideal system. To reduce this noise there are a few PCB layout techniques that can be used.

Selecting a quieter noise source is the first step in cleaning up this noise. Then isolating the supply from other system components through a ferrite bead or inductor can clean up the system further. Ensure that the ferrite bead or inductor has a low resistance so the supply does not drop. Finally, adding 0.1µF bypass capacitors can filter out the remaining high-frequency noise on the supply.

Cleaning up these supplies is necessary for consistent operation of the receiver and the entire chip.

Because USB 3.0 Super Speed signalling is in the 2.5GHz range, not all connectors are equal in performance. The quality of the connector as regards impedance, isolation, crosstalk and so on can greatly impact the amount of noise added to the signal. The standard B connector is known to affect signal quality the most.

The large size of the B connector means more potential for impedance mismatch. Also, the paths that connect the USB lines to the PCB can vary from vendor to vendor, each with a different noise profile. The quality of these paths can also introduce more noise into the signals through ground isolation and crosstalk.

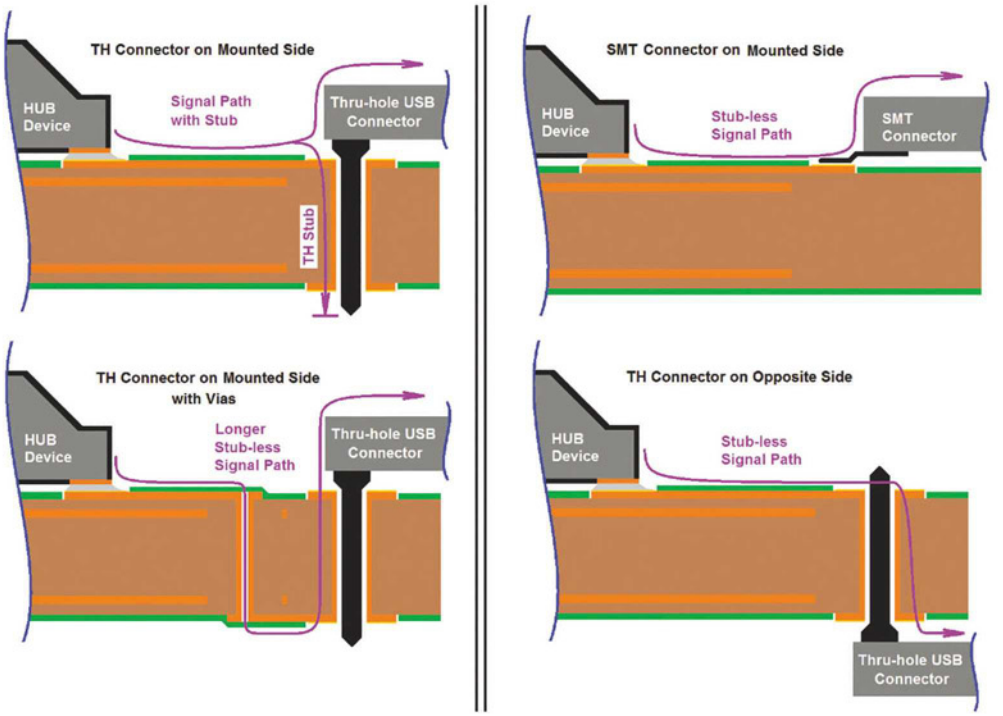


Figure 3: PCB trace paths to a through-hole connector

It is recommended to try samples of different USB connectors to find one that is optimal for the system.

The standard A connector also has potential problems, but because the profile is smaller, the distance from the USB-A line to the PCB is much shorter. And there are surface-mount options for this connector that can also clean up the signal.

The micro B connector offers the best performance because of its small form-factor and its surface-mount connection to the board.

SIGNAL PATH

The signal path from the DUT to the connector also has an impact on JTOL results. The biggest impact is the length of the trace itself and the loss in the dielectric. The 5Gbyte/s signal will lose amplitude along the trace from the connector to the DUT through the dielectric material of the PCB. The performance of the receiver is tied to the amplitude of the signal, so if the trace is shorter, the amplitude at the receiver will be higher and the receiver will perform better. Because the device or upstream hub port JTOL tests have the lowest initial amplitude, traces from the DUT to those connectors should be the shortest.

Another factor that can affect JTOL performance of a USB device is branching. The ideal signal path should have one source and one destination. If the trace branches in any way, the signal will be affected. If the traces branch to another terminated receiver, much

> *"Power supplies, connector quality and PCB loss can all affect JTOL test"*

of the signal energy will be lost, affecting JTOL performance. If the traces branch to an unterminated test point, the signal will be reflected back to the main trace, adding noise that will cause the receiver to have sub-optimal JTOL results. This open-circuit stub is also present in the standard through-hole connector, so the way the traces are routed to the connector is important; see Figure 3.
The ideal option would be to have no through-hole connectors and with the traces going directly from the DUT to the connector.

ACHIEVING OPTIMAL RESULTS

JTOL results can be optimized if certain items are checked. First, confirm that the test fixtures used include high-quality cables and connectors. Bandwidth of the SMA cables should be high enough to pass USB3 signals, and the phase of the cables should be matched. If there is anything wrong with the SMA cables, the whole test is invalid.

Second, check the calibration of the test system. There is a lot of variation in the calibration results, so multiple runs may be required to trust the final results.

And finally, the USB system needs to have the right connectors installed with the cleanest, shortest possible traces from the connector to the device. Careful attention to the USB system design and test environment is necessary to get a fully compliant USB device. ■

Don't miss the Point

Rigol's new SiFi Arbitrary Waveform Generators

Telonic Launch Rigol's new DG1000Z series of arbitrary waveform generators, the latest development in their family of fast, easy-to-use professional test instruments.

Rigol's DG1000Z series helps engineers to accomplish a wide range of testing applications by combining many functions in one easy-to-use instrument. Functions include arbitrary waveform generator, function generator, pulse generator, harmonic generator, and analogue/digital modulator.

The DG1000Z series also incorporates Rigol's Direct Digital Synthesizer (DDS) technology, ensuring that signals are delivered with stability, precision, purity and low distortion. These arbitrary waveform generators with innovative SiFi (Signal Fidelity) can generate arbitrary waveforms point-by-point and allow precisely adjustable sample rates and low jitter (200ps).

The arbitrary waveform memory is available with 8 Mpts (standard) and 16 Mpts (optional). Two full functional channels can be used as two independent generators offering ±1 ppm frequency stability and -125 dBc/Hz phase noise. The instruments have a built-in 8 orders harmonics generator and a built-in 7 digits/s full function frequency counter with 200MHz bandwidth.

Users can choose from up to 160 built-in waveforms with 14 bits vertical resolution and can benefit from a convenient arbitrary waveform editing interface. Versatile modulation types include AM, FM, PM, ASK, FSK, PSK and PWM. The instruments offer standard interfaces USB Host & Device and LAN (LXI Core Device 2011) and a 3.5" TFT colour display. All models are supported by the Ultra Station PC software tool.

There are 2 models in the DG1000Z Series of Arbitrary Waveform Generators a 30 MHz and 60 MHz unit, with pricing starting at £369 on Telonic's dedicated Rigol website www.rigol-uk.co.uk.

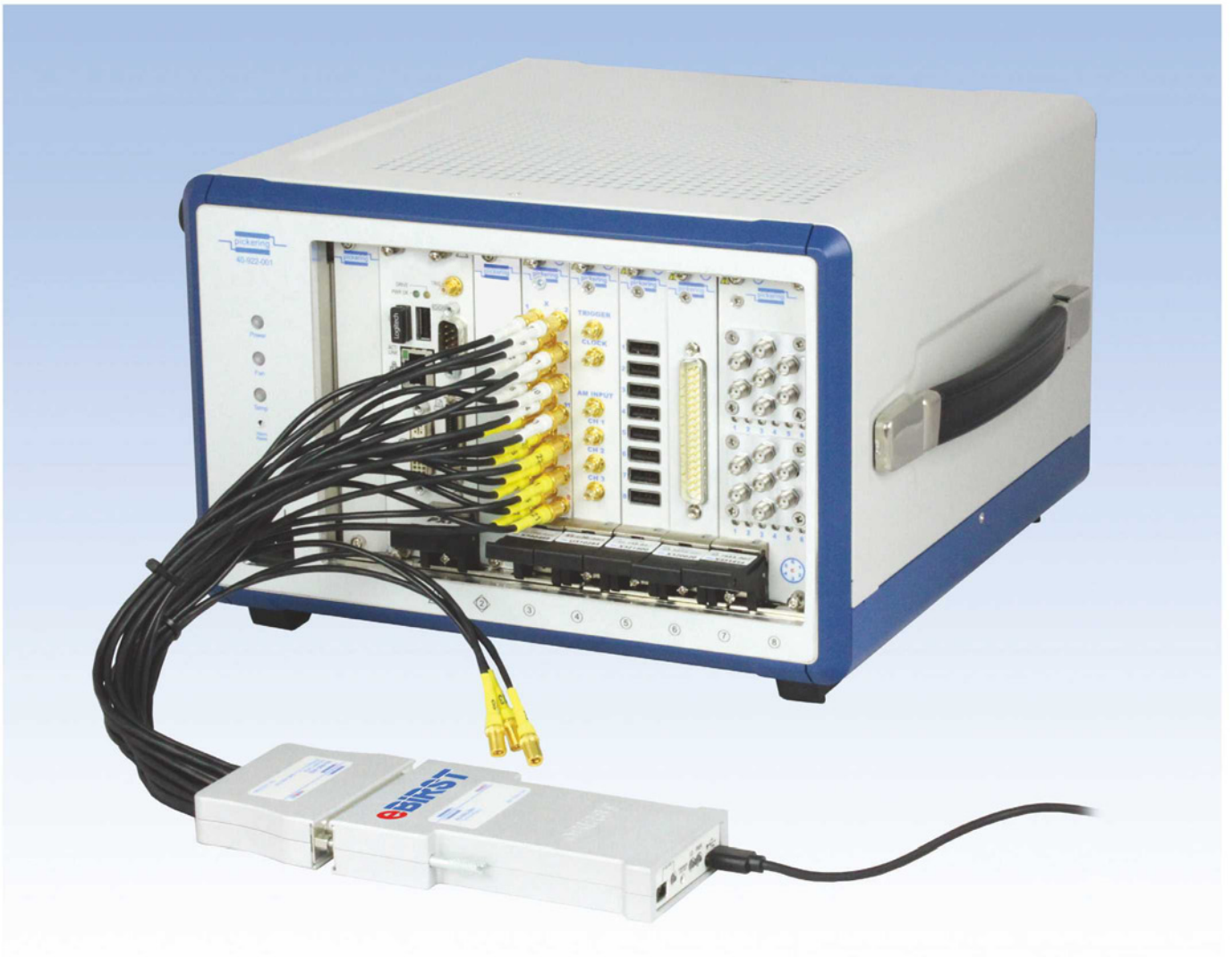
RF INSTRUMENTS

The DSA832 and DSA875 expand the DSA800 Spectrum Analyzer Series to 3.2 and 7.5 GHz respectively. With specifications that far exceed the DSA815-TG, these new instruments enable direct measurements of higher performance signals and systems. For design and development implementing Wi-Fi, Bluetooth, and other RF standards, the SSB phase noise down as low as -98 dBc/Hz at a 10 KHz offset empowers engineers to more accurately analyse modulations and noise surrounding their signals of interest. This becomes important for debugging and immunity testing of transceiver systems. The 7.5 GHz instrument enables engineers to investigate the 3rd harmonic of all of their critical 2.4 GHz applications. Additionally, resolution bandwidth settings down to 10 Hz means more precise visualization of low power RF signals.

With the EMI-DSA800 option you can enable the EMI RBW settings and the quasi-peak filter across the entire spectrum of interest for compliance and immunity testing. Whether you are still debugging your RF transceiver set, designing layout and configuration changes to maximize efficiency, or testing your system in noisy environments the DSA800 series spectrum analysers will help you to quickly and easily identify and analyse your areas of concern. Spectrum Analysers start at just £897 on Telonic's dedicated rigol website www.rigol-uk.co.uk. ■

For more information: 0118 9786911

www.rigol-uk.co.uk • www.telonic.co.uk



HOT SWITCHING, RELAY FAILURES AND HOW TO FIND THEM

DAVID OWEN, BUSINESS DEVELOPMENT MANAGER FOR PICKERING INTERFACES, DESCRIBES HOW RELAYS CAN BE DAMAGED AND THEN USE EBIRST TO FIND THOSE FAILURES

Hot switching describes operations where a relay is either opened or closed while carrying a signal. It can have a major impact on relay life; a relay in a hot switching environment will experience contact erosion and heating that does not occur during cold switching where the signal is removed before changing the relay's state.

Relay vendors provide information on ratings, but they tend to be for reproducible conditions, i.e. specified with resistive sources and loads. When relays are placed in switching systems other issues can arise, some of which are described here.

CAPACITIVE HOT SWITCHING

It is not always obvious to users what level of hot switching is experienced by relays, even in relatively low current or voltage conditions. If a low impedance source is connected to a high impedance load, but the cabling or load contains significant parasitic capacitance, on contact closure the relay can experience a high surge current as the source charges the capacitor.

High surges can also occur when the relay connects a source to a capacitive load carrying a charge from a previous state. This could happen where polarity reversal is handled by a relay system, or if a previous operation has left a charge on a high impedance load. For this reason many systems that test cable assemblies provide a mechanism for discharging any residual charge.

Switching modules normally include a maximum hot switch voltage, which is characterized into a resistive load. It should be

noted that if long cables or other capacitive loads are attached the rating may be degraded.

POWER SUPPLY CHARGE EXCHANGE

One potential misunderstanding on hot switch ratings is when a power supply is connected to a load which is already generating voltage. The load will commonly have local decoupling capacitors and the sudden connection to the power supply can result in high inrush current. This current is not limited by a current limit on the power supply since it usually arises from exchange of charge from the power supply output decoupling to the load decoupling. Some relays do have ratings for such high inrush events (above the relay's normal rating); they are designed with contacts that have large wiping action on closure and which are made of high temperature materials.

Solid state relays are generally considered more robust for hot switching power supplies because they handle inrush currents between capacitors well.

HOT SWITCH FAILURES ON CLOSURE

The most common mechanical relay hot-switching failure mechanism is either welded contacts or contacts having variable or intermittent contact resistance – particularly at low currents – due to erosion of the contact materials. Welded contacts are usually caused by high inrush currents when contacts close, creating molten or soft metal in that area.

Severe contact erosion or built-up debris can cause contacts to fail when closing.

HOT SWITCH FAILURES ON OPENING

In applications where high powers are being switched, an arc (plasma) can be generated that increases the time during which contact erosion can occur. The arc is particularly damaging if the load or source contains a significant inductive component, as this can create multiple arcs during the time the contact opens.

Operating a power relay frequently in a short time can cause additional problems, as the generated arc leads to an increase in relay temperature. The more often an arc is generated in a given time, the more erosion occurs and the more heat is generated. For this reason many high-power mechanical relays are life tested at relatively low cycle rates, particularly as they are used toward their maximum rating.

The more frequently an arc is generated, higher temperatures are reached, leading to more rapid contact erosion and damaging of mechanical parts in the relay, particularly the plastic parts that hold the contacts in place. Some relays require the package to include a vent that helps dissipate the plasma.

> *"It is not always obvious to users what level of hot switching is experienced by relays, even in relatively low current or voltage conditions"*

Arcing is a particular problem on DC signals because there it can be sustained for a long time. The trace shown in Figure 1 was taken by loading a relay with 30V and an excess carry current; the relay has then broken the connection. An arc is created as the relay opens – on very high current relays this creates a visual arc even through the packaging; in this example the arc lasted for one second before cooling enough to be extinguished.

RF HOT SWITCHING

A slightly different problem can occur when hot switching RF signals. If the source voltage standing wave ratio (VSWR) is high, then an open relay could have very high voltages appearing across the contact before it closes, or a high voltage is created. The source VSWR being high allows reflected signals to build up a high voltage; insertion loss will reduce the maximum voltage by attenuating the reflected signals.

As the operating conditions have a large impact on the hot-switching conditions for RF signals, the hot switch power is normally quoted with a low source VSWR, unless stated otherwise. If the relay is operated with poor source/load VSWR, the hot-switch performance will degrade, with the degree of it depending on the conditions.

Figure 1: Example of arc creation

POWER LIMIT

The relay specification often contains a power limit number. In the case of DC signals it should be noted that this is often limited to a single voltage/current. As a voltage increases beyond this number, the DC power the relay can handle may decrease rapidly.

The hot switch rating of power relays is often different between DC and AC switching, with the AC power ratings being higher. In DC switching, metal transfer tends to be in one direction so erosion occurs quicker. In AC applications the erosion occurs in both directions and arcs may be suppressed as the signal voltage falls toward zero.

When handling AC, signals derived from the AC supply's reactive components (inductors and capacitors) can be problematic and can reduce the relay's hot switch capacity. AC supply systems typically have many reactive components (filters, transformers) that can cause problems. Inductive sources or loads can create prolonged arcing when breaking a signal, whereas capacitive loads can create high inrush currents on path closure.

MINIMUM CAPACITY

It should be also noted that hot switching some types of electromagnetic relays (EMRs) is required to achieve the best contact-resistance stability where there is a minimum switching capacity stated. The minimum switch capacity can be quite low and, for example, residual cable charges and capacitance in a system can provide the required surge to clean contacts.

Relays intended primarily for RF switching can also exhibit problems after frequent DC hot-switch operations. The operation can strip the gold from contacts and make low-level RF switching losses more variable and frequency dependent, especially at lower frequencies.

Where possible, it is best to avoid DC switching in RF applications.

SOLID STATE RELAYS

Solid state relays can offer very long lifetimes when used within their ratings, and are not subject to arcs and contact problems found on mechanical relays.

Frequent operation of these relays (above hundreds of Hz) can generate additional heat in the switching process. The faster the switching the less heat is generated. Solid state relays are a good solution for applications where long life is needed in a hot switch environment. ■

EBIRST SWITCHING SYSTEM TEST

Q: What are switching systems used for and what should be noted when using them?

A: Switching systems are an important part of many test systems; they allow test resources to access the key parts of the unit under test. However, the switching system is in a vulnerable place and accidents can happen during development or when a connection is made to a faulty device. When those accidents happen you need a way to get the system up and running again with minimum effort and operator skills.
This is where eBIRST helps.

Q: What does eBIRST do and what are its benefits?

A: eBIRST helps quickly determine a fault in a switching system, identifies where the fault is and enables the user to take fast corrective action. This in turn saves repair costs, speeds test program development and minimizes the downtime of the switching system.

Q: How does eBIRST work?

A: It works by measuring the path resistance at the switching system's external connectors using 4-wire measurements, quickly establishing if the path is good, has increased resistance or has failed.

Q: What's needed to use eBIRST?

A: eBIRST is self-contained; all that's needed is a USB2 port on the test system Windows PC, the correct eBIRST tool(s) and the supplied application program. The program uses a Test Definition File created for each switching system that defines the testing process. Some applications require two tools to test the switching system paths between two connectors. The tools work together in a master/slave mode via a connection between their Master Slave Connectors to measure the through-path.

Q: How do I find out where faulty relays are physically located?

A: Check the test results on the graphical display that identifies which relays need attention and where they are physically located on the switching system. There is no need to refer to manuals and use lengthy tables to identify where the relays are, the tool makes fault-location information easily identifiable to simplify the repair.

Q: What happens after a repair is carried out?

A: Once repairs have been carried out, the test tool may be reconnected and the application program re-run to verify that repairs were successful.
The switching system can be re-deployed with a minimum of system downtime.

Q: Are any accessories needed for eBIRST?

A: The functionality and accuracy of the eBIRST tool can be checked with the help of an external calibration fixture that allows users to either connect two eBIRST tools together or measure a set of fixed-value precision resistors. The tools cross-check each other's performance, and the precision resistors are used to check measurement accuracy.

Q: What kind of systems does eBIRST support?

A: Any of Pickering's switching systems that use mechanical relays with precious metal contacts (typically with a rating of 2A or less) or solid state relays are supported by the use of three eBIRST tools and a set of interface adaptors. DC-coupled RF systems using SMB connectors are supported via the use of test adaptors. Each tool is generic – it will support DC-coupled switching systems that use multi-way connectors on Pickering's PCI and LXI controlled switching systems.

Q: Does the system need to be set up for every different switching system to be tested?

A: For each switching system to be tested there is a Test Definition File that describes the tests to be performed via the correct eBIRST tool(s) and the limits to apply. These Test Definition Files are regularly expanded to cover different switching systems.

mcs test equipment

Website: www.mcs-testequipment.com
Email: sales@mcs-testequipment.com
Tel: +44 (0) 8453 62 63 65

New · Used · Rental · Finance · Calibration

AEROFLEX · LITEPOINT · MAGNA-POWER · Value instruments by Rohde & Schwarz · COMM-connect · TESCOM · Vectawave · ROHDE&SCHWARZ · RIGOL Beyond Measure · COM-POWER CORPORATION

Leading suppliers of:

- Antennas (EMC)
- Attenuators
- LISNs
- Network Analysers
- RF Switches
- Spectrum Analysers
- Antenna Analysers
- Comb Generators
- Measurement Receivers
- Oscilloscopes
- Shielded Boxes
- TEM Cells
- Amplifiers (EMC)
- Electronic Loads
- Meters
- Power Supplies
- Signal Generators
- Wireless Test Sets

Calibration Services

mcs test equipment

Capability Range: DC – 18 GHz	
Frequency Counters	Signal Generators
Oscillators	Sweep Generators
Pulse Generators	Network Analysers
Waveform Generators	Communications Test Sets
Attenuators	RF Power Meters
Amplifiers	RF Power Sensors
Signal Analysers	Directional Couplers
Spectrum Analysers	Terminations

MCS Test Equipment offer quality, ISO9001 accredited calibrations.

50% off your first calibration!
Please quote "Electronics Weekly"

Tel: +44 (0) 8453 62 63 65
sales@mcs-testequipment.com
www.mcs-testequipment.com

ISO 9001 REGISTERED FIRM

From 50 MHz to 4 GHz: Powerful oscilloscopes from the T&M expert.

FROST & SULLIVAN 2015 BEST PRACTICES AWARD
Global Oscilloscopes Competitive Strategy Innovation and Leadership Award

Fast operation, easy to use, precise measurements –
That's Rohde&Schwarz oscilloscopes.

R&S®RTO: Analyze faster. See more. (Bandwidths: 600 MHz to 4 GHz)
R&S®RTE: Easy. Powerful. (Bandwidths: 200 MHz to 1 GHz)
R&S®RTM: Turn on. Measure. (Bandwidths: 350 MHz and 500 MHz)
HMO3000: Your everyday scope. (Bandwidths: 300 MHz to 500 MHz)
HMO Compact: Great Value. (Bandwidths: 70 MHz to 200 MHz)
R&S®HMO 1002: Great Value. (Bandwidths: 50 MHz to 100 MHz)

All Rohde&Schwarz oscilloscopes incorporate time domain, logic, protocol and frequency analysis in a single device.

Take the dive at www.scope-of-the-art.com/ad/all

ROHDE&SCHWARZ

TMD CELEBRATES 20 YEARS OF SUCCESS

On June 12, TMD (TMD Technologies Ltd) celebrates 20 years since the founders' Peter Butcher and Howard Smith management buy-out (MBO) in 1995 from Thorn EMI Electronics.

"Twenty years is an extremely impressive achievement for an MBO in our technology sector, but this is only the beginning," said Dave Brown, TMD's Managing Director.

TMD now boasts a substantial high-tech design and manufacturing facilities, with headquarters in Hayes, West London. The company is a supplier of microwave tubes, high-voltage power supplies and radar transmitters, EW, communications, EMC HIRF testing and other laboratory applications. Its turnover in 2013 was over 200% higher than at the start of the MBO.

"Our future goal is to be the Preferred Partner for innovative and reliable RF and microwave power solutions worldwide, and by 2018 we hope to achieve further growth of more than 60%," added Brown.

www.tmd.co.uk

ELECTRO RENT'S NEW LONDON FACILITY STRENGTHENS THE COMPANY'S PRESENCE IN THE UK

Electro Rent, a provider of electronic test equipment for rent, lease or used sales, is opening a new office in London. The corporation's European subsidiary Electro Rent Europe has already been operating successfully in the UK for 10 years and experienced a continuous growth of business. The new UK office will allow Electro Rent Europe to support current customers with better local service and drive future expansion in the region.

Electro Rent Europe is already celebrating 10 years of delivering a winning combination of service and choice throughout Europe. The growth in demand for test equipment rental has matched the company's growth in the last decade and underlines how pairing in-depth market knowledge with a commitment to maintaining an industry-leading inventory results in shared success for both Electro Rent and its strong, growing customer base.

www.electrorent.com

ROHDE & SCHWARZ EXPANDS COLLABORATION WITH AVNET AND EBV ELEKTRONIK

The Rohde & Schwarz electronics group has signed an extensive partnership agreement with Avnet EMG and EBV Elektronik, two leading distributors, to ensure optimal availability of its electronic components and the corresponding technical support.

The production of Rohde & Schwarz high-tech products makes complex demands on the company's supply chain, and needs that the delivery of electronic components and sub-systems is on time, of high quality and cost-effective. "To achieve this, we need flexible and competent suppliers," said Peter Schlindwein, VP Corporate Procurement at Rohde & Schwarz. "We have found these strong partners in Avnet and EBV Elektronik. Together, we have now laid a new foundation which consolidates the current business and provides a legal platform to extend it further."

www.rohde-schwarz.com

BELDEN PARTNERS WITH ASKOM IN TEST LAB FOR AUTOMOTIVE OEMS

Belden, a global supplier of signal transmission solutions for mission-critical applications, and strategic partner ASKOM kommunikationstechnik, a specialist in communication technology, have opened a new test lab, located at ASKOM's main premises in Wolfsburg, Germany.

The test lab is able to demonstrate a complete communication infrastructure around applications in the factory floor – and was established to meet the increasing demand for closer geographical support from automotive OEMs and their suppliers – with focus on the Volkswagen (VW) group.

The lab is equipped with a large range of products from various Belden brands, such as Lumberg Automation, Hirschmann, Tofino Security and Belden. They include EAGLE One security products; MACH4000, MACH1000 and MSP30 backbone switches; MS20/30 field switches; patch cord and IO box connectivity solutions; and HiVision software for industrial network management.

www.belden.com

RUTRONIK ENGAGED AS GLOBAL DISTRIBUTOR FOR MELEXIS

Rutronik Elektronische Bauelemente and Melexis have signed a global distribution agreement covering Melexis's entire product portfolio of sensors, sensor interface ICs, driver ICs and communication ICs.

Melexis offers an extensive array of highly integrated semiconductors that help the automotive industry to produce greener, safer cars and domestic appliance manufacturers to bring more energy efficient products to market, as well as enabling implementation of advanced industrial equipment, medical instrumentation and building automation systems. The company's sensor portfolio includes magnetic (Hall effect), optoelectronic and MEMS pressure sensors. Its driver IC offering covers high performance DC and brushless DC motor controllers, plus FET pre-drivers, while its communication ICs can be used for remote keyless entry, tire pressure monitoring, in-vehicle networking and wireless charging initiation applications.

www.rutronik.com

ACAL BFI IN STRATEGIC COLLABORATION WITH SYNQOR FOR EUROPE

Acal BFi has signed a channel partner agreement with SynQor to cover Europe, including the UK, Ireland, Denmark, Sweden, Norway, Finland, Belgium, Netherlands, Luxemburg and Italy.

SynQor supplies high-efficiency, high-reliability power conversion solutions, designing, engineering and manufacturing all of its products in the US. The company's extensive product portfolio contains a lot of industry firsts and is designed to excel in demanding environments – ideal for applications within the military, industrial, transportation, medical and communications markets. SynQor's high quality products follow an elaborate platform strategy, which allows easy, fast and inexpensive design adaptions to application needs – and ultimately results in an extraordinary high launch rate of product innovations.

The company's power portfolio ranges from 0.25W DC/DC converters to 5MW customised water-cooled AC/DC transformers.

www.acalbfi.com

Meet the industry's top experts and optimise your Connected Car service in this new automotive value chain

Connected CARS

28 - 30 September 2015, London, England

Register using the code CCEW20 to receive 20% off your booking!

Discover how to create a viable Connected Car business model and drive consumer uptake through a safer driving experience

Featuring 15 experts from across the Connected Car ecosystem including;

Dieter May
Senior Vice President Digital Business Models
BMW

David Green
Market Development Director
Volvo Group

Caroline Reichert
Director Mobility International
PSA Peugeot Citroën

Sirish Batchu
Head of Infotronics Technology & Advance Electronics,
Mahindra & Mahindra

Paul Zanelli
Chief Technology Officer,
Transport Systems Catapult

Antti Aumo
Marketing Director
Car Connectivity Consortium

Ilja Radusch
Director Automotive Services and Communication Technologies (ASCT)
Fraunhofer FOKUS

Angel David Garcia Barrio
Vice President M2M
Etisalat

Xavier Perrett
Vice President Strategic Partnerships and Open Services
Orange France

Nick Reed
Academy Director
Transport Research Laboratory

Take advantage of leading case studies:

- Develop your Connected Car business model and ensure yourself the best ROI with **Peugeot PSA Citroën**
- Learn how **BMW** positioned themselves to prepare for the shift towards the Connected Car and discover how to optimise your organisation in preparation for connected vehicles
- Unlock new opportunities through your Telematics Big Data; hear how **Orange** are using their data to create a personalised intelligent mobility experience for consumers
- Investigate how **Transport Systems Catapult** are creating the first autonomous vehicle for the Smart City and discover how the future of driving in the city might look
- Explore how Mahindra and Mahindra are securing their connected vehicles
- Discover techniques from the **Volvo Group** on how you can maximise consumer uptake for your Connected Car
- Determine how Telematics and the Connected Car will result in a safer driving experience with insight from the **Transport Research Laboratory**

"Very good opportunity to network and understand requirements posed on all OEM, latest supplier component information & future trends"

Automotive IQ Delegate - Volvo Group Trucks Technology

Early Bird Pricing Available

Please enquire at enquire@telecomsiq.com or call +44 (0) 207 368 1300 for more information!

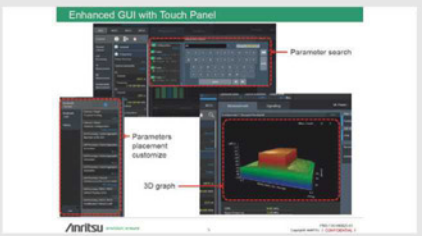
NEW ANRITSU RADIO COMMUNICATION ANALYZER SUPPORTS LTE-ADVANCED TESTING

Anritsu launched MT8821C, its new radio communication analyzer for research and development testing of mobile devices (user equipment, UE) with the widest capability for supporting LTE-Advanced.

As well as supporting LTE-Advanced, the all-in-one MT8821C operates as network simulator supporting LTE, W-CDMA/HSPA, GSM/GPRS/EGPRS, TD-SCDMA/HSPA and CDMA2000 1X/1x EVDO technologies to run RF TRX tests in compliance with the 3GPP and 3GPP2 standards, as well as parametric tests.

The easy-to-operate MT8821C makes setting and operation errors a thing of the past, simplifying configuration by using preset measurement parameters for test items specified by the 3GPP RF test standards. Additionally, parameters for all tests can be set and changed easily using the all new highly advanced Graphical User Interface, which includes touchscreen operation. The MT8821C supports additional functional tests, such as maximum throughput tests.

www.anritsu.com



RIGEL AND EQ2 LAUNCH NEW AUTOMATED INTERFACE

A new approach to medical device testing in hospitals is available following the launch of an advanced interface developed by Rigel Medical and EQ2.

The move sees the Rigel Medical 288 safety analyser integrated with EQ2's clinical equipment management system HEMS to provide a fully automated, highly accurate and portable system for capturing and documenting medical device safety records.

A new module has been incorporated into EQ2's HEMS Enterprise software to make it fully compatible with the automated Rigel analyser.

The EQ2 Rigel SA Interface enables biomed engineers to harness the 288's full capabilities to capture valuable information at the point of testing in a hospital or healthcare centre before sending the data automatically to the HEMS system to complete safety checks and link to the medical device's inventory, test library and performance history.

www.rigelmedical.com

NEW CONNECTOR COMBINATION FOR RELIABLE TRANSMISSION

The MEDI-SNAP EMC is the newest addition to ODU's extensive family of push-pull circular connectors, offering a cost-effective way to provide reliable protection against accidental contact whilst at the same time ensuring effective EMC shielding.

The demand for shielded products continues to rise, since new applications in medical technology require that more and more electronics are enclosed in smaller and smaller spaces. This latest connector variant combines the application-related benefits of both metal and plastic, and as a result it weighs less and is both autoclavable and sterilizable.

The MEDI-SNAP EMC connector retains the same benefits as the existing ODU push-pull connectors, including a wide variety of coding possibilities (both colour and mechanical), together with great chemical resistance.

MEDI-SNAP is just one of ODU's many problem-solving connectors.

www.odu-uk.co.uk

TOSHIBA OFFERS NEW HV-IPD FOR SINE-WAVE MOTOR CONTROL

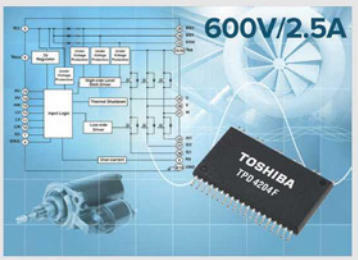
Toshiba Electronics Europe (TEE) launched a new high-voltage intelligent power device (HV-IPD) that enables the sine-wave control of brushless DC (BLDC) electric motors. The TPD4204F will find use in a range of low-power industrial fans and pumps, as well as white goods including washing machine, dishwashers and fan units.

Rated to 600V and 2.5A, the TPD4204F features six MOSFETs and a driver IC in a multi-chip configuration. The device is housed in a 30-pin SMD-type package (SOP30) that separates all small signal pins from the power pins and measures just 20 x 11 x 2mm.

The TPD4204F provides over-current, over-temperature and under-voltage protection and can be combined with either MCUs or MCDs.

TEE offers one of the industry's broadest IC and discrete product lines, including high-end memory, MCUs, ASICs and ASSPs for various applications.

www.toshiba.semicon-storage.com



WATERPROOF 36W POWER SUPPLIES FROM POWERSOLVE

Powersolve announces the PS36MK series of encapsulated power supplies designed specifically for low-voltage outdoor applications, including security and CCTV installations.

The PS36MK Series power supplies provide up to 36W respectively, working from an input voltage between 90-264VAC. Output voltages range from 5-24VDC and no-load power consumption is ≤ 0.3W max.

The power supplies are environmentally protected to IP67, meet the requirements of EN60950 and have an operating temperature range of -10°C to 40°C. They are CE marked and await cTUVus approval.

All models feature short-circuit, over-current and over-voltage protection.

The power supplies can be wall or chassis mounted to any flat surface and Powersolve can provide connectors to suit most applications. The PS36MK measures 133 x 50 x 34mm.

www.powersolve.co.uk

LITHIUM-ION CELL PACKS – HIGH ENERGY WITH EXCELLENT RECHARGING CAPABILITY

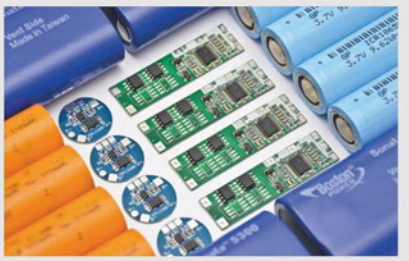
Cell Pack Solutions has extended its production capabilities to include Li-ion battery packs in its portfolio of batteries and cell packs.

Rechargeable Li-ion batteries offer a number of advantages over other battery technologies, including higher voltages, higher energy densities, excellent recharging capability, operating temperature range from -40°C to 70°C, and long life. This makes them ideal choice for applications such as asset tracking and portable test equipment where long-term power needs are critical.

Working closely with GP Batteries, Cell Pack Solutions is able to offer rapid turnaround on prototypes utilising Boston Sonata, Swing and standard 18650 Li-ion batteries.

This type of battery pack needs to be carefully protected. The company specifically incorporates cell protection control modules (PCM) into each pack.

www.cellpacksolutions.co.uk



COMPACT SINGLE-PHASE FILTER WITH HIGH SYMMETRICAL ATTENUATION

Schurter is expanding its range of block filters for single-phase systems with the new FMAB NEO series. This range of single-phase filters combines a compact design with a high level of performance. The use of large X capacitors permits high symmetrical attenuation.

Symmetrical interferences can occur because of phase-angle controllers or semi-conductor relays, for example. When the power semiconductors switch, they generate interference currents between the phase conductor and the neutral conductor. These are known as symmetrical interferences, which the X capacitors positioned between these conductors can help reduce effectively.

The new filters have a shiny steel housing with a closed filter base, thus being effectively and completely shielded, no matter the way they are going to be mounted.

www.schurter.com

NEW DESIGNSPARK MECHANICAL ADD-ON MODULES FOR 3D DESIGN TOOL AVAILABLE NOW

RS Components (RS) expanded the DesignSpark Mechanical offering with two new optional premium modules that significantly extend its functionality.

The first module is the DesignSpark Mechanical Exchange that adds advanced import/export capabilities and enables the import, modification and export of industry-standard STEP and IGES file formats, allowing full exchange of design data with CAD tools such as SolidWorks, Catia, ProEngineer and AutoCAD.

The second module is DesignSpark Mechanical Drawing, which allows the changing of designs, as well as the ability to create and modify geometry from within drawing views. It enables the creation of detailed dimensioned drawings allowing designers to move beyond concept development and the 3D printing of prototypes and on to final manufacturing.

The modules were developed in conjunction with SpaceClaim.

www.designspark.com

LINEAR 3V HALL-EFFECT POSITION SENSOR IC WITH I²C OUTPUT

The new A1454 from Allegro MicroSystems Europe is a linear 3V Hall-effect sensor IC that provides a 12-bit digital I²C output that is proportional to the strength of the magnetic field that is present.

The A1454 is targeted at the consumer, industrial and instrumentation markets with end applications to include non-life-critical medical and consumer devices that require linear position sensing. The quiescent output value of the A1454 is set at mid-scale, and the device is available in two different factory-programmed sensitivity ranges: 2 LSB/G and 4 LSB/G. The sensitivity temperature coefficient is also factory programmed to support either neodymium or ferrite magnets.

The I²C address can be set by external resistors or programmed via EEPROM to support up to 127 unique I²C addresses, allowing for multiple ICs on the same bus.

www.allegromicro.com

FAST FOUR-CHANNEL PCI EXPRESS TO CAN CARD BY KVASER

Kvaser AB introduced Kvaser PCIEcan 4xHS, a highly integrated, high-speed controller area network (CAN) card that adds four high-speed CAN channels to any standard computer board with PCI Express capability. Offering silent mode, error frame detection/generation and an on-board buffer, this small form-factor add-on board fits many embedded data acquisition systems and is CAN-FD ready.

The PCIEcan 4xHS has an average response time of 45µs. An onboard buffer ensures that there is no risk of the card 'dropping' messages, meaning that the Kvaser PCIEcan 4xHS is as robust as it is responsive. This is very useful in 'ping-pong' protocols such as firmware updates.

This is a low profile card (86 x 69mm), fully compatible with J1939, CANopen, NMEA 2000 and DeviceNet. It offers a wide operating temperature of 0°C to +85°C and galvanically-isolated CAN bus drivers.

www.kvaser.com

VERSARIEN TECHNOLOGIES LAUNCHES A STANDARD RANGE OF LOW PROFILE HEAT SINKS

Versarien developed a standard range of heat sink products based on its VersarienCu copper foam technology, designed for passive cooling applications where space is at a premium and performance crucial.

The VersarienCu heat sinks can cool any IC, in applications such as power, high-temperature environments, set-top boxes, AP routers, modems, optical networks and LED TV and flat panel displays, and others.

VersarienCu reduces the potential size requirement of individual components due to increased thermal efficiency, as the metallic foam now allows for a reduced footprint. The increased thermal efficiency of the copper foam on the component can allow for a cooling fan to be removed from products, and has the additional major benefit of increasing the life of a component by reducing overheating.

www.versarien-technologies.co.uk

SEAWARD TESTER SCRUBS-UP WELL AT PRESSURE WASHER REFURB SPECIALISTS

A firm specializing in refurbishing electric pressure washers is using the versatile HAL 103 multi-function safety tester from Seaward to ensure products leaving its factory are safe to use by consumers.

JMS Janitorial Supplies, who undertakes the refurbishment of thousands of Karcher electric pressure washers sent to its site in Surrey by retailers from across the UK, uses 6 HAL 103s to ensure improved compliance with standards for Class I and Class II electrical products.

The JMS operation, which has been in place for the last 12 months, currently sees in excess of 150 washers a day complete comprehensive earth bond, insulation resistance and flash testing.

The HAL 103 is a fast and efficient automatic industrial test solution, which records results and enables accurate testing to be carried out in line with relevant standards at all times.

www.seaward.co.uk

TEN-YEAR-LIFE POSCAP POLYMER CAPACITORS FROM PANASONIC

Panasonic Automotive and Industrial Systems's new POSCAP TC series polymer capacitors withstand high temperatures, have a low ESR and a high resistance to stress, making them suitable for industrial and other applications that require a life of 10 years. The wide operating temperature range of -55degC to +125degC ensures that devices last for 10 years at 85degC and a ripple current rating of 6.1Arms enables them to survive in high stress environments.

POSCAP TC series devices also feature a low ESR down to 5mΩ, a capacitance range of 100-1000µF and are rated for voltages from 2-10V. This combination of characteristics suits them to a diverse range of applications, including industrial PCs, servers and basestations, PSUs and voltage regulators, LED backlighting, FPGA designs, measurement and sensing, wearables and IoT.

http://eu.industrial.panasonic.com

MOUSER NOW SHIPPING INDUSTRY'S FIRST 900V SIC MOSFET FROM CREE

Mouser Electronics is stocking the C3M family of silicon carbide power MOSFETs from Cree. The latest breakthrough in silicon carbide (SiC) power device technology and the industry's first SiC 900V MOSFET platform, the C3M Power MOSFETs are optimized for high-frequency power electronic applications. The new 900V platform enables smaller and higher-efficiency next-generation power conversion systems while reducing system cost versus silicon-based solutions.

These power MOSFETs feature high blocking voltage of 900V with low on-resistance, which limits power loss and reduces the need for additional cooling components. The C3M0065090J features the lowest on-resistance rating (65mOhms) of any MOSFET device currently available on the market, and is offered in a low-impedance D2Pak-7L surface-mount package with a Kelvin connection to help minimize gate ringing.

www.mouser.com

GAN SYSTEMS POWER TRANSISTORS ARE 50% SMALLER

GaN Systems has launched what it claims is the world's smallest 650V, 15A gallium nitride transistor. With a footprint of just 5.0 x 6.5mm, the GS66504B – one of a family of 650V devices that spans 7A to 200A – is 50% smaller than competing devices.

GaN Systems is the first company to have developed and brought a comprehensive product range of devices with current ratings from 7-250A to the global market – its Island Technology die design, combined with its extremely low inductance and thermally-efficient GaNPX packaging and Drive Assist technology means the company's GaN transistors offer a 40-fold improvement in switching and conduction performance over traditional silicon MOSFETs and IGBTs. The devices are available now through its worldwide distribution network.

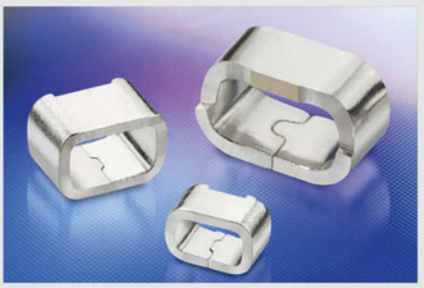
www.gansystems.com

HARWIN EXPANDS POPULAR EZBOARDWARE TEST POINTS RANGE

Due to the industry's ever increasing demand for more functionality in ever decreasing PCB space, Harwin has expanded its popular EZBoardWare portfolio with new, small-size and low-profile versions of surface mount Test Points. The two new Test Points are designed to match the 2012 and 1608 metric (0805 and 0603 imperial) electronic package sizes, whilst providing secure connection points and allowing test engineers to clip on industry standard micro test clips.

Harwin's small size surface mount EZBoardWare Test Points are fully auto-placeable to PCBs, minimizing installation costs. Available in a range of form factors to match the size of the customer's electronic package size and in three stock sizes for maximum choice, the components have been designed to provide specific targets for test engineers to use when testing PCBs.

www.harwin.co.uk



OMC OFFERS TO MOUNT ANY FIBRE OPTIC DIODE IN ANY HOUSING

OMC has announced a new service, enabling engineers to choose exactly the right fibre optic diode for their application and have it mounted in their preferred package.

"We regularly get approached by people who have identified a diode which is a perfect match for their needs, but find that it is not available in a housing, or in the specific housing that they need. As the housing itself – as well as the way the diode is mounted in the housing – can have serious implications for system performance, we decided to offer a 'mix and match' service, you specify housing and diode, we'll look after the mounting process," said OMC's Commercial Director, William Heath.

OMC's proprietary ACA (Active Component Alignment) technology ensures fibre-optic data links perform consistently and reliably from link to link.

www.omc-uk.com

SEMTECH'S SIC SCHOTTKY DIODES NOW AT ASTUTE FOR OIL AND GAS

Astute Electronic continues its support for Semtech's high-reliability discrete products by introducing the HR512031BA23C down-hole tailored SiC Schottky diode for the oil and gas industries.

The device surpasses 16 of 18 temperature ranges listed in the top three standards and has a junction temperature between -55degC and -220degC. As well as the high temperature capability, features include low switching losses, small package outline and very low reverse recovery time.

Maximum DC forward current (IF) is 10A, DC blocking voltage (VR) is 1.2kV, reverse current (IR) is 30µA typical at +25°C and 60µA at +175°C, forward voltage (VF) is less than 1.5V typical at an IF of 10A and +25°C and 2.5V at +175°C, and reverse recovery time (Trr) is less than 15ns.

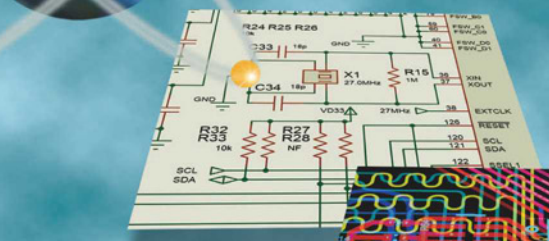
Also available in Semtech's range are diodes, TVS diodes, Zener diodes and others.

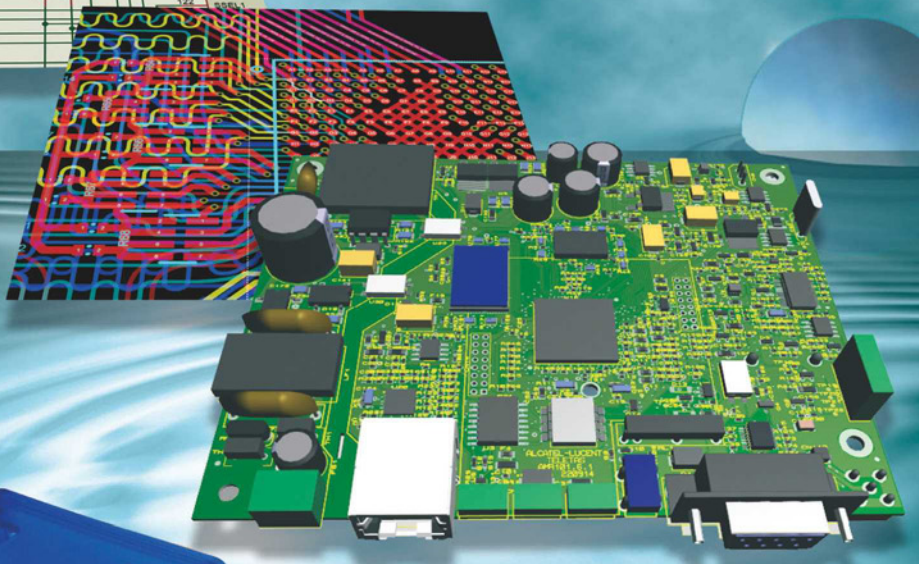
www.astute.co.uk

PROTEUS 8.3

ECAD to MCAD made easy

Data Exchange with STEP/IGES





AUTODESK. PTC

SOLIDWORKS

The Proteus Design Suite now includes full support for data exchange with Mechanical CAD packages via the STEP/IGES file formats. This allows you to better visualise your design and helps quickly solve fixtures, fittings and casement problems.

Import 3D STEP/IGES models for your parts and visualise inside the Proteus Design Suite. Export your completed board to Solidworks or other MCAD software.

Visit www.labcenter.com
Tel:+44 01756753440 E-Mail info@labcenter.com

Labcenter Electronics Ltd, 21 Hardy Grange, BD23 5AJ

Labcenter Electronics www.labcenter.com