September 2015
Volume 121
Issue 1953
£5.20

www.electronicsworld.co.uk

Electronics WORLD

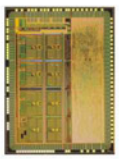
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Keysight FieldFox

Industry's first 50 GHz handheld analyzer

SPECIAL REPORT ON LOW POWER DESIGN:

- Filters
- NOCs
- SOCs



Technology
IC developed to very accurately measure Earth's magnetosphere

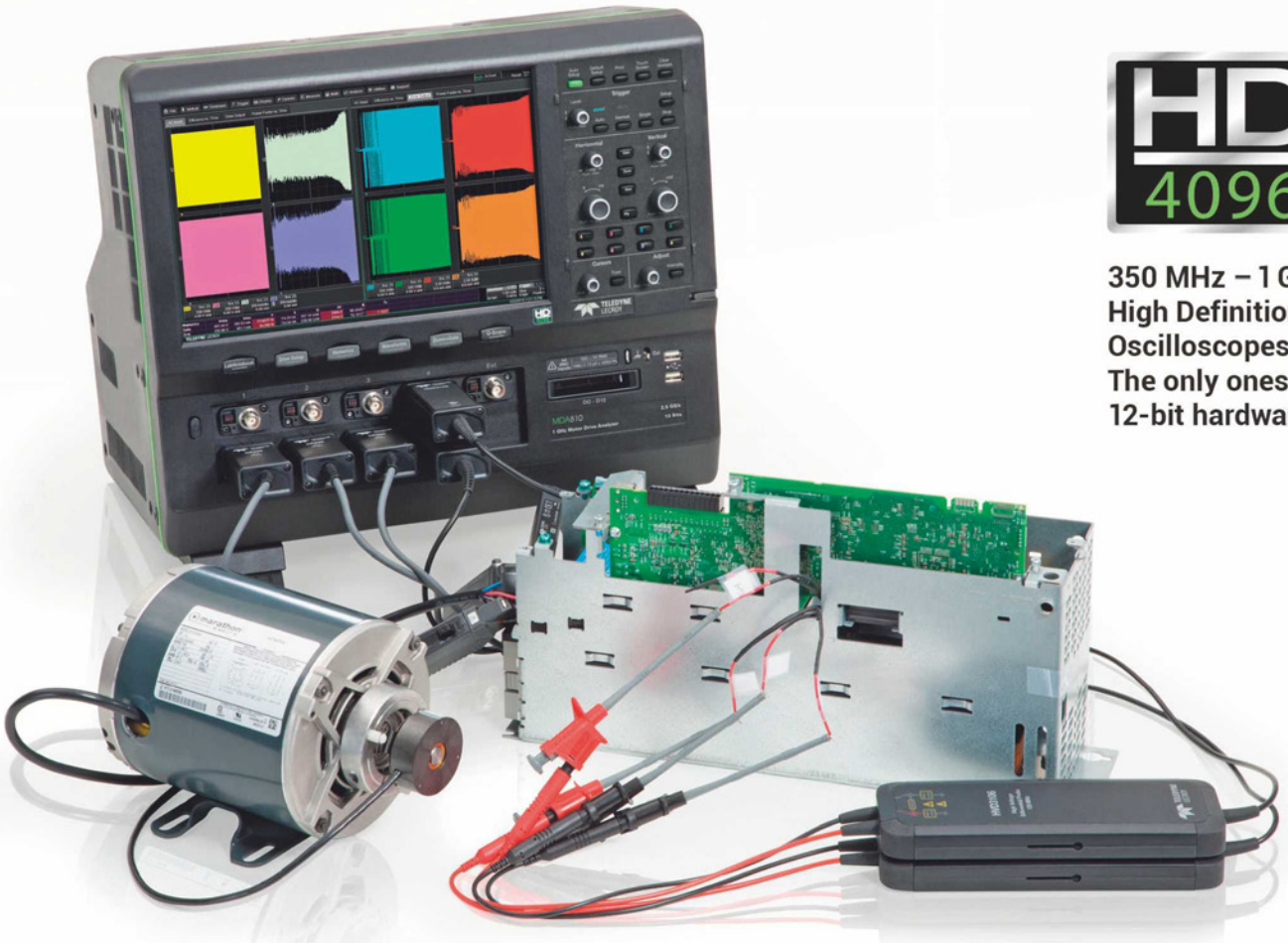
Analog Design
Past and future, according to Bob Dobkin, Linear Technology's co-founder

Products
Latest components, systems and equipment

TELEDYNE LECROY
Everywhereyoulook™

Complete Power Analysis for 3 Phase Motor Drives

NEW! Motor Drive Analyzer MDA800 – 8 Channel, 12-bit, up to 1 GHz



HD 4096

350 MHz – 1 GHz High Definition Oscilloscopes – The only ones with 12-bit hardware

Who's**doing**that?

teledynelecroy.com

Cover supplied by KEYSIGHT TECHNOLOGIES
More on pages 20-21

REGULARS

46

FEATURES

Disclaimer: We work hard to ensure that the information presented in Electronics World is accurate. However, the publisher will not take responsibility for any injury or loss of earnings that may result from applying information presented in the magazine. It is your responsibility to familiarise yourself with the laws relating to dealing with your customers and suppliers, and with safety practices relating to working with electrical/electronic circuitry – particularly as regards electric shock, fire hazards and explosions.

THE WORLD'S LARGEST SELECTION OF ELECTRONIC COMPONENTS AVAILABLE FOR IMMEDIATE SHIPMENT!™

DIGIKEY.CO.UK

0800 587 0991
0800 904 7786

- OPEN ACCOUNTS AVAILABLE FOR QUALIFYING CUSTOMERS
- FREE SHIPPING ON ORDERS OVER £50*
- LIVE WEB CHAT: 24/7, 365 DAYS PER YEAR
- PRICES ARE IN BRITISH POUND STERLING AND INCLUDE DUTIES

LOCAL SALES & TECHNICAL SUPPORT AVAILABLE

Digi-Key® ELECTRONICS

1,000,000+ PRODUCTS IN STOCK | 650+ INDUSTRY-LEADING SUPPLIERS | 3.9 MILLION PARTS ONLINE

*A shipping charge of £12.00 will be billed on all orders of less than £50.00. All orders are shipped via UPS for delivery within 1-3 days (dependent on final destination). No handling fees. All prices are in British pound sterling and include duties. If excessive weight or unique circumstances require deviation from this charge, customers will be contacted prior to shipping order. Digi-Key is an authorized distributor for all supplier partners. New product added daily. © 2015 Digi-Key Electronics, 701 Brooks Ave. South, Thief River Falls, MN 56701, USA

ecia MEMBER ecsn member CEDA

AUTOMOTIVE POWERTRAIN SEMICONDUCTOR MARKET GROWS

Increasing volumes of new vehicles and the need for fuel-efficient technologies are ramping up the automotive powertrain semiconductor market, which grew 8.3% in 2014, according to US-based analysis house IHS. Forecasts are that these revenues will continue to grow with a compound annual growth rate (CAGR) of nearly 6% in the next five years, from $7.2bn in 2014 to $9.5bn in 2019.

Electrification is propelling the powertrain semiconductor market on a global scale. This includes start-stop systems, forecast to grow at a CAGR of 21%, and plug-in hybrid vehicles, expected to grow at CAGR or 37% for the next five years. In addition, for internal combustion engines there is an increasing trend away from traditional incumbent multi-port fuel injection systems towards gasoline direct-injection systems. Direct injection systems are more efficient and require higher semiconductor content than their multi-port counterparts.

"Propulsion systems for electric and hybrid vehicles demand, on average, 10 times more semiconductor content than a conventional engine," said Ahad Buksh, analyst for automotive semiconductors at IHS. "Without electrification, the powertrain semiconductor market would have grown only 3.1% annually for the next five years, whereas electrification is now accelerating the market at 6% growth rate annually."

Some key components of electrification for the powertrain include the motor inverter, DC/DC converter, battery management system and plug-in charger, all of which require power management by analog integrated circuits (ICs) and discrete components. These systems saw growth of 24% in 2014 and another 22% increase is forecast for 2015, according to IHS, the highest of any automotive semiconductor application.

> For internal combustion engines, there is an increasing trend away from traditional incumbent multi-port fuel injection systems towards gasoline direct injection systems

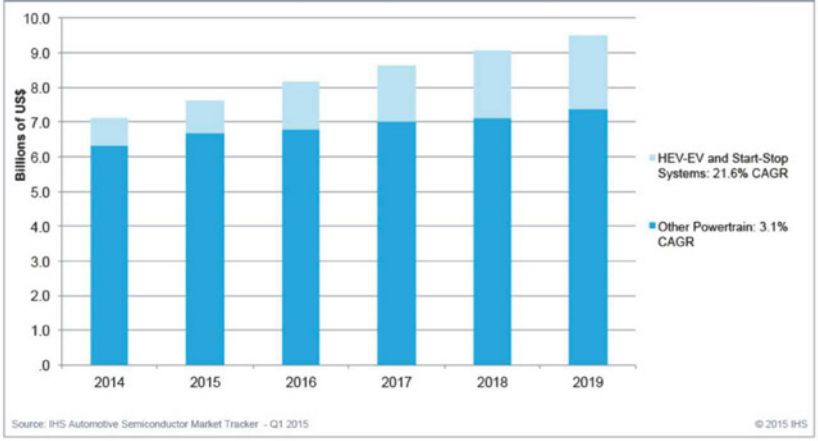
From a revenue perspective, semiconductor content in electric and hybrid vehicles are expected to generate more than $1bn in total revenue growth from 2014 to 2019, by which time IHS forecasts $1.6bn will be generated in this segment. In addition, emissions legislation efforts in most regions around the world are the main drivers for semiconductor sales in powertrain applications, while current concepts in engines and exhaust after-treatment systems for ICEs, together with a requirement for on-board diagnostics, require sensors for their operation. As a result, the market for semiconductors in internal combustion engines was $4.3bn in 2014, growing to $5.4bn in 2019, says IHS.

The engine control unit (ECU) uses most of the semiconductors in these applications, in addition to a growing trend toward electrification of various components – including fans, water pumps and oil pumps that will further contribute to powertrain semiconductor revenues in the future.

Transmissions are well-established systems for semiconductors, but recent new concepts such as dual-clutch transmissions (DCTs) and continuously variable transmissions (CVTs) have entered the market. As a result, this portion of the semiconductor market is expected to grow from $1.4bn in 2014 to $1.5bn by 2019, according to IHS. Most new growth stems from the demands on microcontrollers, particularly as a result of increased sensor content featured in new transmissions.

IHS forecasts that on a regional basis, China, Japan and eventually Europe will drive the market for DCTs, while China, South Asia and eventually North America will drive the market for CVTs.

Automotive Semiconductor Revenue for Powertrain: HEV/EV & Start-Stop Systems vs. Other Powertrain



IHS offers insight, analytics and expertise in critical areas that shape today's business landscape since 1959 (www.ihs.com)

EDITOR: Svetlana Josifovska
Tel: +44 (0)1732 883392
Email: svetlanaj@sjpbusinessmedia.com

SALES: Philip Woolley
Tel: +44 (0)20 7933 8989
Email: philipw@sjpbusinessmedia.com

DESIGN: Tania King
PUBLISHER: Justyn Gidley

ISSN: 1365-4675

PRINTER: Buxton Press Ltd

SUBSCRIPTIONS:
Subscription rates:
1 year: £62 (UK);
£89 (worldwide)
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com

SJP business media

2nd Floor,
52-54 Gracechurch Street,
London, EC3A 0EH

Follow us on Twitter @electrowo

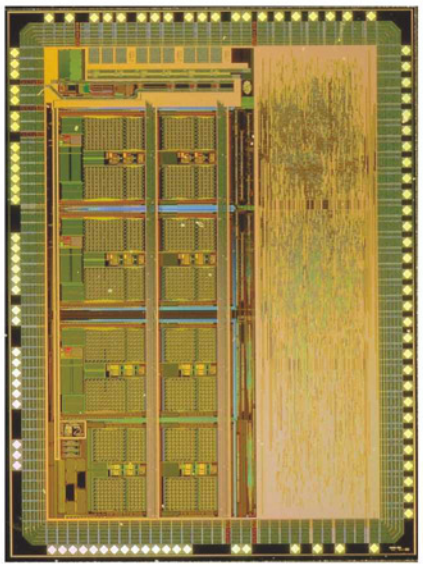
Join us on LinkedIn

PARTNERS ENABLE SATELLITE-BASED EXPLORATION OF THE EARTH'S MAGNETOSPHERE

The Fraunhofer Institute for Integrated Circuits, the Space Research Institute of the Austrian Academy of Sciences and the Full Service Foundry division of ams, a provider of high performance sensors and analog ICs, have jointly developed a new IC for highly accurate measurements of the Earth's magnetosphere from space.

As part of NASA's "Magnetospheric Multiscale" mission launched in March, four identically-equipped satellites are performing highly accurate three-dimensional measurements of the Earth's magnetosphere to assess its dynamics. The research focuses on the so-called magnetic reconnection, a physical process in which the Earth's magnetic energy is converted into kinetic and thermal energies and particle acceleration. Magnetic reconnection is one of the mechanisms responsible for the aurora, as well as for temporary disturbances in the Earth's magnetosphere.

Like all measurement instruments and equipment in satellites, the Space Research Institute's magnetometer has to be very small and light, and consume very little power. In addition, it must offer very high accuracy under harsh conditions that include radiation and very low temperatures. The satellites' digital flux-gate magnetometer (DFG) operates at a resolution of 10pT – several thousand times more sensitive than a conventional electronic compass – enabling the sensing of the smallest variations in magnetic flux.



IC for highly accurate measurements of the Earth's magnetosphere

The Fraunhofer ASIC was fabricated by ams using its specialty 0.35µm CMOS (C35) process technology, which allows for the design of complex analog/mixed-signal integrated circuits. Based on a unique process architecture, the rad-hard C35 technology is very well suited for use in space and aerospace applications.

"The ams specialty 0.35µm CMOS process enabled the team of researchers and scientists at Fraunhofer to develop a complex analog/mixed-signal integrated circuit that impressively outperformed our expectations in all respects – performance, power consumption, die area and reliability," said Johann Hauer, project manager for ASIC Development at Fraunhofer.

TOSHIBA DEVELOPS TWO NEW PROCESS TECHNOLOGIES FOR MICROCONTROLLERS AND WIRELESS COMMUNICATION ICS

Toshiba has announced a new flash memory embedded technology based on a 65nm logic process that uses less power than current mainstream solutions, and a single-poly non-volatile memory (NVM) process based on 130nm logic and analogue power process.

Applying the optimal process to diverse applications will allow Toshiba to expand its product line-up in such areas as microcontrollers, wireless communication ICs, motor controller drivers and power supply ICs.

The IoT market is seeing strong demand for low power consumption in many areas, including wearable and healthcare-related equipment. In response, Toshiba has adopted Silicon Storage Technology's third-generation SuperFlash cell technology, in combination with its own 65nm logic process. The company has also fine-tuned circuits and manufacturing processes in developing its ultra-low power consumption flash embedded logic process. Microcontrollers for consumer and industrial applications based on this process have up to 60% lower power consumption than current mainstream technology.

Following the first series of microcontrollers, Toshiba plans to release sample BLE (Bluetooth Low Energy) products in 2016.

The company aims to lower power consumption for entire systems, targeting 50µA/MHz operation. In applications where significant cost reductions are a concern, Toshiba has developed an NVM embedded process that adopts Yield Microelectronics's single-poly MTP (multi-time programmable) cells on Toshiba's 130nm logic process technology.

NVM and analogue circuits are embedded on a single chip that can incorporate multiple functions usually executed by a multi-chip system. This reduces the number of terminals and realises smaller packages. Applying MTP specifications for write times improves the new process's performance while limiting added steps in mask pattern lithography to three or fewer, or even none. By using MTP to adjust output accuracy, Toshiba will expand its product line-up in fields where higher accuracy is essential, such as power management ICs.

Slim Range with Power Meter and Surge Protection

Olson Electronics has expanded the Slim Range to now include the popular Olson Power Meter and Surge Protection.

You can now check what power is being used to ensure the PDU does not get overloaded or easily check what current is being drawn, while the surge protection helps protect equipment from voltage spikes. It's ideal for wall or floor mounting and is available in 5 different sizes.

Standard Features

- Olson Power Meter, Displaying Volts, Amps, Watts and Power Factor
- Surge Protection Varistors
- A robust steel construction
- Light grey RAL 7035 paint finish
- High integrity dual earthing and external M5 earth stud with 250mm long earth lead
- The option on three different plugs
  - UK 13A fused plug (BS1363)
  - 16A IEC 60309 (BS4343) plug
  - 32A IEC 60309 (BS4343) plug
- PDU comes with the option of 4, 6, 8, 10 or 12 UK 13A sockets (BS1363)

Technical Data

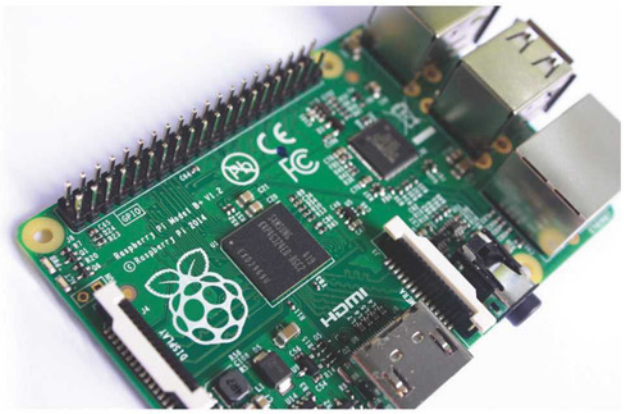
Operating Voltage	230VAC
Maximum Voltage	250VAC
Current Rating (rating matches plug)	13A/16A/32A
Manufactured to	BS5733
Approved to	BS EN60950 CE

Manufactured in the UK

OLSON ELECTRONICS LIMITED
OLSON HOUSE, 490 HONEYPOT LANE, STANMORE, MIDDX HA7 1JY
TEL: 020 8905 7273 FAX: 020 8952 1232
email: sales@olson.co.uk www.olson.co.uk

THIS SERIES PRESENTS THE RASPBERRY PI SINGLE-BOARD COMPUTER, ITS FEATURES AND BENEFITS, AND ITS USE IN VARIOUS PROJECTS

Making A Temperature Gauge With The Raspberry Pi



BY **ANDREW ROBSON** AND **MIKE COOK**

In this project we will use a DS18B20 sensor to detect temperature and display it on screen. We will also write Python code to monitor the temperature and send an e-mail alert when it exceeds a predefined level. The sensor returns a Celsius value, so we will include some optional Python code to do a Fahrenheit conversion. Below is the list of components needed for this project, which includes:

- 1 x DS18B20 sensor, which looks like a transistor but is actually a highly accurate 1-wire temperature sensor.
- 1 x 4.7kΩ pull-up resistor.
- 1 x solderless breadboard; a prototyping board to which parts and wires can be connected by clipping them on. It is used for prototyping electronics without having to solder parts together.
- Jumper wires: Male-to-male for breadboard connections, and male-to-female for connecting the breadboard to GPIO pins. Jumper wires usually come in packs of various quantities, colours and sizes. Although only six are needed for this project, 20 or 30 of each are sufficient for most projects. Any length will do for this project, but shorter male-to-male (10cm) and longer male-to-female (20cm) are best.

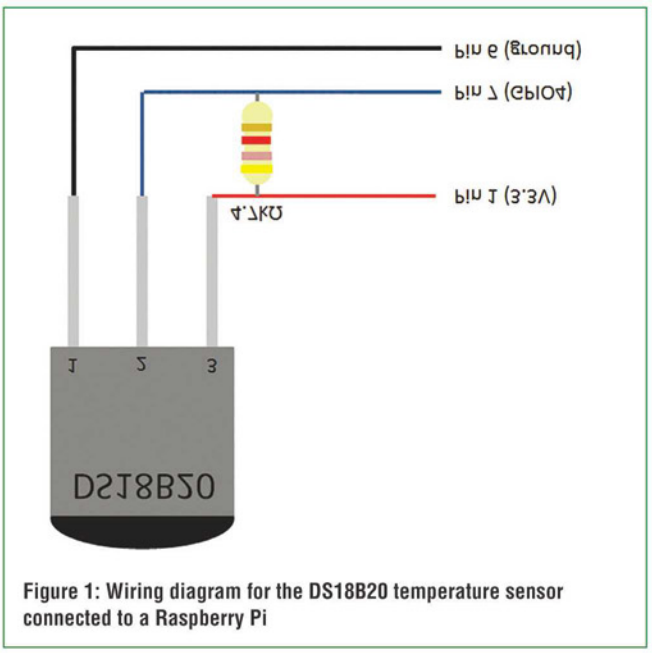


Figure 1: Wiring diagram for the DS18B20 temperature sensor connected to a Raspberry Pi

Construction

The circuit for this sensor is very easy to build. Beside the power and ground connections, all that's needed is the 4.7Ωk pull-up resistor between the signal and power as shown in Figures 1 and 2.

Use pin 7 for the sensor connection, as the software used to interface with the DS18B20 is hard-coded for pin 7. This software is built into the Raspberry Pi kernel.

We will be use an application called Modprobe to retrieve the temperature value.

At the Raspberry Pi command prompt, type the following two commands:

```
sudo modprobe w1-gpio
sudo modprobe w1-therm
```

A nice feature of the DS18B20 sensor is the unique number associated with each sensor, permitting quick access to the reading from each one. The preceding command interfaces with the sensor and retrieves the temperature, which is then written to a new directory on the Raspberry Pi, found in **/sys/bus/w1/devices/**.

To check if this file has been created, we can do a directory listing by typing **ls/sys/bus/w1/devices/**. This will show a directory that correlates to the unique number of the sensor, similar to 28-0000040be5b6, for example (since each sensor has a unique number, this will vary).

If a directory is still not showing, then we'll need to do the following:

- Check the circuit wiring.

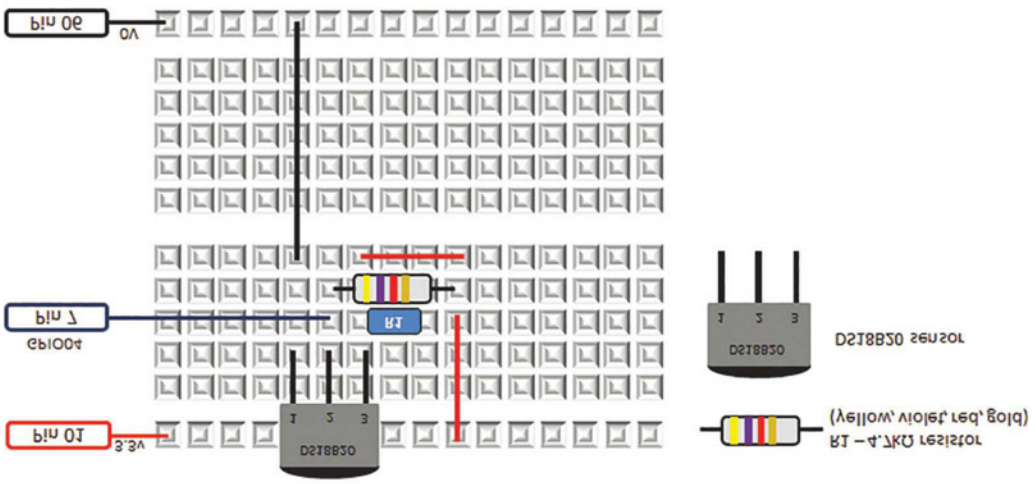


Figure 2: Breadboard diagram for the DS18B20 temperature sensor connected to a Raspberry Pi

- Make sure that the correct resistors are in place. (This is very important – yellow, violet, red, gold.)
- Feel the temperature gauge for warmth: if it feels hot, it's been wired backwards.
- If you do see the new directory, navigate into it and view the contents of the w1_slave file, which will contain the temperature value (remember to replace my number with yours):

cd /sys/bus/w1/devices/28-0000040be5b6
nano w1_slave

You will now see the contents of the w1_slave file, which contains the temperature data in Celsius. In my example (see Figure 3), the temperature is 20.812 degrees Celsius.
Press Ctrl + X, followed by N to exit.

Now that testing is complete and the sensor is working well, we'll need to write Python code to automate the preceding and print the temperature to the screen, as shown in Listing 1:

```
#!/usr/bin/env python
“””
Home Automation: temperature check
For the Raspberry Pi
“””
import subprocess
import time
def fileexists(filename):
try:
with open(filename): pass
except IOError:
return False
return True
def GetTemperature():
#set this variable to true if you want a Fahrenheit
#temperature
Fahrenheit = False
#These two lines call the modprobe application to get the
#temperature from the sensor
subprocess.call([‘modprobe’, ‘w1-gpio’])
subprocess.call([‘modprobe’, ‘w1-therm’])
#Open the file that you viewed earlier so that Python can
#see what is in it. Replace the serial number with
#your own number
filename = “/sys/bus/w1/devices/28-0000040be5b6/
w1_slave”
if (fileexists(filename)):
tfile = open(filename)
else:
return 0
# Read the w1_slave file into memory
text = tfile.read()
# Close the file
tfile.close()
# You are interested in the second line so this code will
# put the second line into the secondline variable
secondline = text.split(“\n”)[1]
```

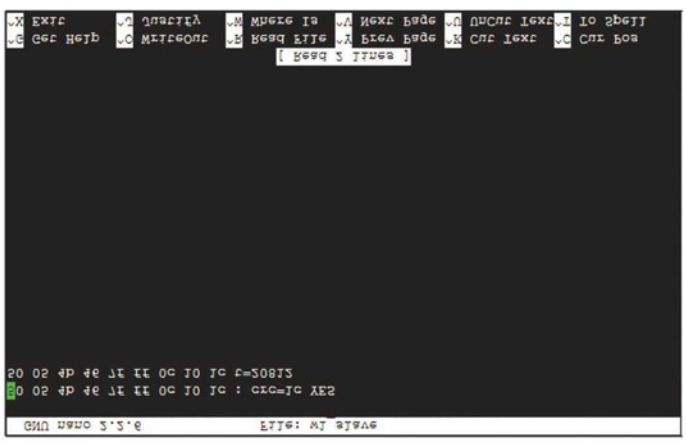


Figure 3: The temperature shown in the w1_slave file that was created by Modprobe

```
# You are interested in the 10th word on the second
line
temperaturedata = secondline.split(" ")[9]
# You are interested in the number of the 10 word so
# you discard the first two letters "t=" and convert
# the remaining number $
temperature = float(temperaturedata[2:])
# Divide the value by 1000 to get the decimal in the
# right place
temperature = temperature / 1000
temp = float(temperature)
# Do the Farenheit conversion if required
if Fahrenheit:
temp=temp*1.8+32
temp = round(temp,2)
return(temp)
def main():
# This is the main routine of the program
print "The temperature is " + str(GetTemperature())
if __name__ == "__main__":
main()
```

Listing 1: Temperature check

Lastly, we can create code to monitor the temperature and send an e-mail when it exceeds a particular value, using the SendEmail function from the e-mail project (project 4 in Chapter 13 of the book). Using this program, replace the main routine with the code in Listing 2.

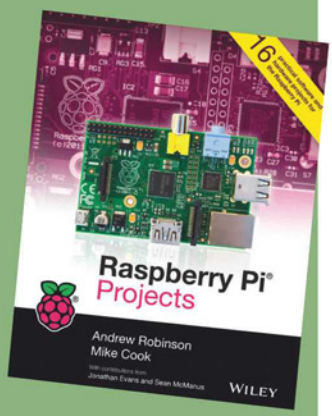
```
# This is the main routine of the program
tempind=False
while True:
temperature=GetTemperature()
if temperature > 25 and tempind==False:
#Use the SendEmail routine from the
#e-mail project
SendEmail("The temperature is "+ ;
str(temperature))
tempind=True;
else:
#This will ensure you only receive one e-mail
#once the temperature is above 25
#This variable is set back to false when the
#temperature is less than or equal to 25
tempind=False;
#Fetch the temperature every 10 seconds
time.sleep(10)
```

Listing 2: Temperature alert

This is an edited extract from the book 'Raspberry Pi Projects' by Dr Andrew Robinson and Mike Cook, published by Wiley

RASPBERRY PI PROJECTS

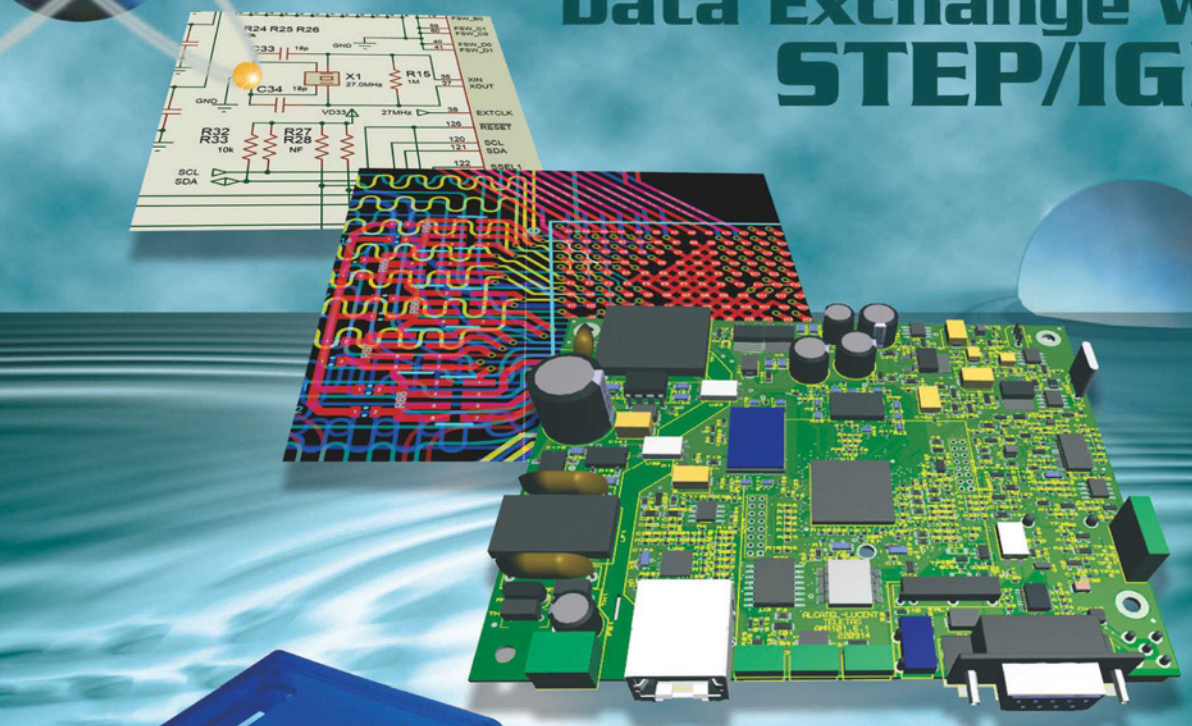
Raspberry Pi represents a new generation of computers that encourage the user to play and learn. This book is aimed at the beginner Raspberry Pi user who wants to create real-world projects.
Containing 16 practical projects, this fun and informative resource introduces readers to the skills required in order to make the most of the Pi.
Raspberry Pi Projects is available in paperback and e-book format, priced £14.99.
We have several copies of this book to give away.
To win a copy, register your interest by writing to the Editor at svetlanaj@sjpbusinessmedia.com



PROTEUS 8.3

ECAD to MCAD made easy

Data Exchange with STEP/IGES



AUTODESK. PTC

SOLIDWORKS

The Proteus Design Suite now includes full support for data exchange with Mechanical CAD packages via the STEP/IGES file formats. This allows you to better visualise your design and helps quickly solve fixtures, fittings and casement problems.

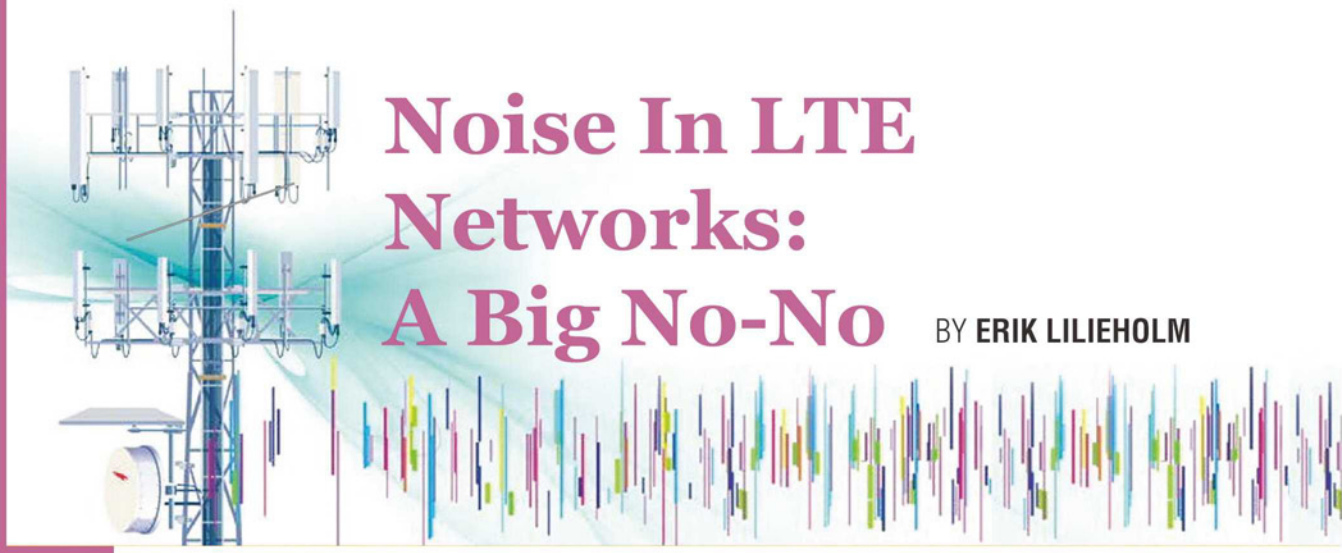
Import 3D STEP/IGES models for your parts and visualise inside the Proteus Design Suite. Export your completed board to Solidworks or other MCAD software.

Visit www.labcenter.com

Tel:+44 01756753440 E-Mail info@labcenter.com

Labcenter Electronics Ltd, 21 Hardy Grange, BD23 5AJ

Labcenter Electronics www.labcenter.com



Noise In LTE Networks: A Big No-No

BY **ERIK LILIEHOLM**

Remember the telecoms crash of 2001? Some blame it on the over-exuberant bidding for 3G wireless spectrum at the time. Auctions in the UK reaped £22.5bn, and similar amounts were gained in the US and Germany. In the bleak aftermath of the frenzy, some licence winners ended up defaulting on their payments.

The promise of 3G technology was faster data rates and higher throughput. But wait – who was using mobile data applications 10-15 years ago? At the time, 3G was really a solution in search of a problem – the elusive "killer app". The contours of the future were being drawn by the Blackberry and other devices, but 2007 is when the real killer app came into being with the launch of the iPhone. And that's when we knew we had a problem.

Fast forward to 2015: For the past several years, mobile data traffic has expanded at a compound annual growth rate (CAGR) of 60-70% according to Cisco, who predicts a ten-fold increase in the next five years. How will we make way for all those tweets, bloated attachments and cat videos? That is exactly the problem that currently occupies the minds of operators, regulators and equipment manufacturers whilst the rest of us are blissfully tapping away on our smartphones and tablets.

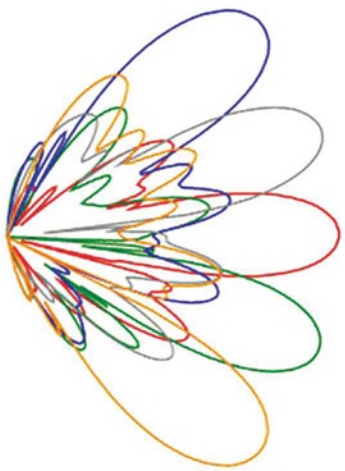


Figure 1: Multi-beam, sector-sculpting base station antennas carve out more capacity for LTE networks

More spectrum! Yes, that is obviously a step in the right direction, but spectrum is a finite resource and is becoming scarcer. In the recent AWS-3 auction in the US, bidding closed at almost $45bn. We have to believe the licensees are keenly aware of the value of the assets they bought.

LTE is another powerful weapon in the battle for capacity. Using orthogonal frequency-division multiple access (OFDMA) modulation, the spectral efficiency of LTE approaches the Shannon Limit – the theoretical maximum of bits that can be transmitted per MHz of radio spectrum. It looks like we have reached the end of the mobile radio access technology rope.

A third approach still open to pursuit is the addition of cells and cell sites. By dividing the coverage area into smaller pieces, the same spectrum can be reused and divided among a smaller group of users. Sector splitting is one way to create more cells. The traditional three 120-degree sectors radiating from a cell tower are split into six, or even nine, by using antennas with narrower beams and by adding radios.

Another method involves placing small cells within the coverage of the larger "macro" cells. Small cell antennas are installed at lower heights, around 5-10m, and are typically placed in hot-spots where they suck up local traffic to the relief of the macro cell.

Having read this far, perhaps you wonder what noise has to do with all this. Let me explain – noise is the enemy of spectral efficiency in LTE networks, the bane of capacity and data throughput. It's Shannon's Limit again – to get LTE up to its maximum speed, the signal-to-noise ratio (SNR) must be considerably higher than with earlier technologies.

Noise from various sources in the environment plays into SNR, but the dominant noise contribution comes from the wireless network itself. Noise spills over from adjacent cells where others are talking and surfing on the same channel

that brings the football match to your seat on the crosstown bus. Stronger signals don't provide the solution; they merely result in even more noise everywhere.

The main effort must be focused at reducing the spillover from cell to cell which, of course, is most difficult at the cell edges. As cells become smaller and more numerous, a higher percentage of their area will be occupied by these boundaries. Therefore, noise mitigation in LTE networks includes making the cell boundaries as sharp and narrow as possible. No clever algorithms or bleeding edge processor speeds can help here. To achieve this, we must turn to the unsung hero that has been part of every radio system since Marconi and Heaviside – the antenna.

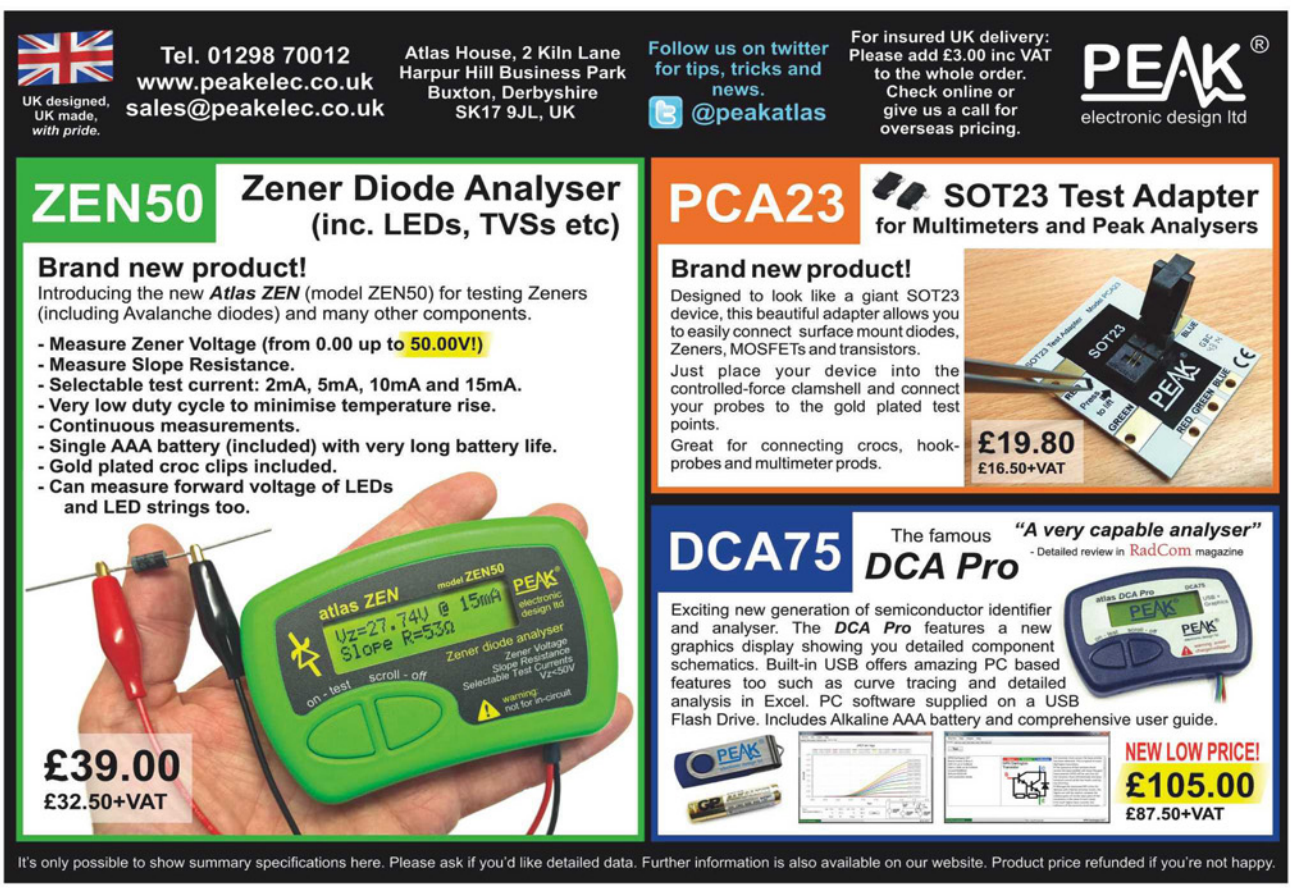
> Noise is the enemy of spectral efficiency in LTE networks, the bane of capacity and data throughput

Advances are being made steadily in the art of beam shaping, wherein base-station antennas focus their energy where we want it while reducing stray radiation in other directions. CommScope refers to this specialized RF pattern shaping as sector sculpting, which is made possible by directional antennas, both in azimuth (horizontal direction) and elevation (vertical space). Sector sculpting allows precise wireless coverage with minimal interference with neighboring cells.

Beam forming and beam switching are other emerging techniques already supported by LTE standards but are just now beginning to gain attention beyond some early implementations in Time Division Duplex (TDD) networks. The basic idea is to put a spotlight on each user and avoid illuminating the bloke one street over. The better one can do this, the higher the use that can be squeezed out of each precious slice of spectrum.

LTE is a noise-limited technology, and reducing that noise is critical to getting the best network performance and a return on that expensive spectrum. Selecting the right antennas is part of the solution, but only a part. Ensuring a clean network means limiting interference within the RF path at each cell site, between cells and between cell layers. Noise is a big no-no and RF engineers have a big role to play in keeping it out. ●

Erik Lilieholm is technical sales manager for the Wireless Network Engineering team at CommScope.
This column is an edited extract from CommScope's new eBook, 'LTE Best Practices'. Over the next few months different authors of this eBook will contribute articles to this section.



Refactoring The MLA

LUCIO DI JASIO, ELECTRONICS ENGINEER AND TECHNICAL AUTHOR, PRESENTS THIS SERIES ON EMBEDDED USER-INTERFACE DESIGN ON A BUDGET

The Microchip Library for Applications (MLA) is a relatively large and successful project, one that has been in constant evolution for over a decade.

The vision at its roots was radical and simple: a single set of libraries to support all PIC microcontrollers, regardless of their core, be it 8, 16 or 32-bit – a true unified platform for all embedded applications. As a side note, contrast it with the competing and somewhat simplistic vision that all embedded applications should unite under a single core/architecture.

Over the years MLA grew and evolved to support an even larger number of applications; it was adapted to support several new microcontroller architectures, and with code growth and time, there is always accumulation of code debt. This a relatively popular term used nowadays to indicate the compounding effect of many little implementation details, fixes and hacks, each well-meaning but sub-optimal, and although designed to preserve precious legacy and ensure stability, eventually building up to make the resulting (software) product hard to manage, rigid and fragile. The only healthy way to get rid of code debt is to refactor the code, which may call for tough decisions, some sacrifices and hard work.

So, in early 2014 the MLA design team published a brand new and vastly improved library. Officially we should refer to it as the current MLA, as opposed to the legacy version that has been archived (but is still available, together with a dozen previous revisions) on a separate page of Microchip's website. Two more releases have followed since, one being published only in May, to consolidate features and complete the refactoring process.

Changes

Let's start with what didn't change: The unified platform vision remained. The application libraries are the same (graphics, touch, file system, USB...) and the broader architectural setup is the same – hardware abstraction, module configuration, full source-code availability etc.

So far so good, so what was all the "refactoring" about? Here are the details, and better perhaps, the reasons for it and the resulting benefits:

Legacy MLA	Current MLA
<mla_install>/Microchip	<mla_install>/framework
<mla_install>/Microchip/Include	<mla_install>/framework
<mla_install>/Microchip/Help	<mla_install>/doc
<mla_install>/[demos]	<mla_install>/apps/[demos]
<mal_install>/Board Support Packages	<mla_install>/bsp

Table 1: Legacy vs updated (current) MLA

1. New folder and file naming convention and organization

This is the most visible change that will cause the most (initial) concern, but it is by far the easiest to understand. As shown in Table 1, the main source code folder is now renamed framework, all the demo projects have been grouped in an apps folder and all the documentation has been grouped in a doc folder, conveniently exposed at the top of the directory structure. More importantly, all the folders and file names have been changed to use only lower case letters, remove spaces and keep things consistent across libraries.

The primary reason for the naming conventions change is the need for cross-platform compatibility (OSX, Windows, Linux). To further improve cross-platform support, the entire set of CHM (Windows only) help files has been replaced by a Java-based help system and a set of PDF documents.

Also, you will appreciate how in the new folder structure all the included files are not separated from their source libraries, reducing "folder hopping" when adding them to your projects in MPLAB X.

2. Exclusive support for MPLAB X and XC compilers

Five years after the introduction of MPLAB X and the unification of all PIC compilers under a single umbrella with the MPLAB XC suite, it was time to let go of hundreds of old project configurations to focus exclusively on the new tool chain. This reduced demo apps clutter and allowed better streamlined testing.

Also, the unified MPLAB XC suite provides a more uniform set of preprocessor directives (pragmas, definitions...), removing the need for macros (previously defined in compiler.h) and many conditional directives (#ifdef), effectively reducing code clutter and improving readability.

3. Custom types replaced by C99 fixed-width data types

Since all the new MPLAB XC compilers support the C99 standard, usage of custom definitions, such as BYTE, WORD, DWORD, is now superseded by fixed-width data types, such as uint8_t, uint16_t, uint32_t, etc. This change helps avoid conflicts when combining MLA firmware with other (open source) libraries and applications.

4. Improving the hardware abstraction

If there is one piece of information you should have learned from all the previous columns in this series, it's the key role of the HardwareProfile(.h) as primary mechanism for abstraction of hardware detail in the MLA. But having been conceived only as an include file, it posed some serious limitations. It is now replaced by a combination of three files: system.c, system.h and system_config.h to allow a more flexible and clean abstraction mechanism.

Whereas before the hardware profile could contain only definitions for pin and peripheral names, that job is now performed by the system_config.h file, while system.c collects all the hardware initialization functions required for the target board of choice.

In Listing 1 you'll find a segment of a typical system.c file to be used in a code example for a PIC24 Mikromedia board and, in particular, the SYSTEM_BoardInitialize() function.

```
void SYSTEM_BoardInitialize(void)
{
 DisplayBacklightConfig();
 DisplayPowerConfig();
 DisplayBacklightOff();

 // Initialize the Display Driver
 DRV_GFX_Initialize();

 // make all pin digital by default
 AD1PCFG = 0xFFFF; // all inputs (not touch) digital

 // configure PPS for PIC24 Mikromedia
 PPSUnLock;

 // SPI2
 PPSInput( PPS_SDI2, PPS_RP26); // SDI2 =RP26 G7/pin
11
 PPSOutput( PPS_RP21, PPS_SCK2OUT); // SCK2 =RP21
G6/pin 10
 PPSOutput( PPS_RP19, PPS_SDO2); // SDO2 =RP19 G8/
pin 12

 // configure Serial Flash CS pin
 M25P80_CS_LAT = 1;
 M25P80_CS_TRIS = 0;

 // configure Codec CS pin
 CODEC_CS_Disable();
 CODEC_CS_Config();
 CODEC_DCS_Disable();
 CODEC_DCS_Config();

 SYSTEM_TickInitialize( 1);
 TouchInit( NVMWrite, NVMRead, NVMSectorErase,
NULL);

 // initialize the Graphics library
 GFX_Initialize();

} // Board Initialize
```

Listing 1: system.c – SYSTEM_BoardInitialize() Function

> The unified MPLAB XC suite provides a more uniform set of preprocessor directives, removing the need for use of macros and many conditional directives, effectively reducing code clutter and improving readability

Such function can now be shared among all projects targeting the same Mikromedia board instead of being repeated in the main.c file of each project. The net result is a considerable reduction of code duplication and of the number of conditional compilation directives (#ifdef) previously seen in the legacy MLA examples.

Relying exclusively on MPLAB X helps here as well, as the project organization can now use the build configuration (and file exclusion) features available, further reducing example code clutter.

5. Peripheral driver abstraction

In the past, different libraries occasionally carried along their own implementation of commonly-used peripheral drivers, making it difficult to use some libraries together by creating potential driver conflicts. In the new structure, not all drivers are fully abstracted yet, but the commonly used ones such as UART and SPI are already available. More will be ported and implemented over time.

6. A migration path to Harmony

In the last few years, USB, graphics and file system support for the PIC32 architecture has been strongly developed in the MPLAB Harmony branch. API compatibility between MLA and Harmony has been greatly improved and will continue to converge further. For example, Graphics Library v4.00 in both MLA and Harmony are already highly compatible.

API Changes

Eventually it boiled down to this: All libraries' APIs had to change, which will cost the most editing time. But equally this is the simplest kind of refactoring work, something the compiler will be quick to point out and MPLAB X auto-completion feature (CTRL-\ or ☐-\ for Mac users) will help fix really fast.

All new APIs follow a standard and uniform naming convention for all their functions:

```
[module]_[sub-module]¬_[featureActions]
```

As an example, a common macro in Legacy MLA:

```
GetPeripheralClock()
```

is now:

```
SYS_CLK_FrequencyPeripheralGet()
```

Although at first this might sound arbitrary, very soon you will notice how convenient and quick it is to guess most of the function names you'll need, based on the library name and the function/action required.

Once again, the main consequence of these changes will be reduction of naming conflicts and better integration with foreign libraries.

Summary

We've seen how the MLA vision of a uniform platform is still going strong and that the library is a living organism that keeps evolving. Refactoring the MLA was a bold decision, but a much needed one. The (new) current MLA emerging is a better one because it builds on the strength of the new tool chain (MPLAB X, MPLAB XC), and is now better structured and ready to integrate with larger application code bases. ●

USER INTERFACE DESIGN FOR EMBEDDED APPLICATIONS

Lucio Di Jasio is EMEA Business Development Manager at Microchip Technology. He has held various technical and marketing jobs in the company's 8, 16 and 32-bit divisions for the past 18 years.

Lucio has published several books on programming for embedded control applications, and we have three copies of his book *'Graphics, Touch, Sound and USB, User Interface Design for Embedded Applications'* to give away at the end of this series.

If you want to win this book, please send an email to svetlanaj@sjpbusinessmedia.com, mentioning the title in the heading.

NORTHERN 15 Manufacturing & Electronics

FREE SEMINARS | FREE PARKING

Incorporating The Road, Rail, and Air Exhibition
ROADRAILAIR
EVENTCITY MANCHESTER | 30 SEPTEMBER – 1 OCTOBER 2015

EventCity | Manchester | M17 8AS

30th September to 1st October 2015
9.30am – 4.30pm (4.00pm close Thurs)

The exciting Manufacturing Technology Exhibition in the North

Over 300+ national and international suppliers will gather in Manchester this autumn for Northern Manufacturing & Electronics 2015 together with the new RoadRailAir event. The exhibition will feature live demonstrations and new product launches of machine tools & tooling, electronics, factory & process automation, packaging & handling, labelling & marking, 3D printing, test & measurement, materials & adhesives, rapid prototyping, ICT, drives & controls and laboratory equipment.

Free industry seminar programme online @ **www.industrynorth.co.uk**

The exhibition is **free** to attend, **free** to park and easy to get to.
Doors open at 9.30am on Wednesday 30th September.

Pre-register online now for your free entry badge and show preview at **www.industrynorth.co.uk**

NORTHERN MANUFACTURING & ELECTRONICS is an ETES event organised by European Trade & Exhibition Services Ltd
Tel 01784 880890 · email philv@etes.co.uk

etes Regional Manufacturing Exhibitions

GEYER
quartz technology

YOUR PARTNER FOR QUALITY QUARTZ FREQUENCY CONTROL PRODUCTS, FROM INITIAL DESIGN TO FINAL PRODUCTION

- **A fully equipped Design & Test Centre in Munich, where our Design Engineers are available to discuss optimal timing solutions and layout issues for your initial design.**
- **3-D images available on request to help with your Design work**
- **Free Geyer Y-Quartz App analysing tool to help optimize your oscillator circuit and identify the best crystal specifications for your application**

All supported by our network of offices in Europe, Asia and America, and factories in Taiwan, S Korea and Japan.

QUALITY FOR MORE THAN 50 YEARS GEYER

GEYER ELECTRONIC UK Ltd
39 Basepoint, Abbey Park, Romsey, Hants, SO51 9AQ, UK
Tel: +44 (0) 1794 319318
sales@geyer-electronic.co.uk • www.geyer-electronic.com

Sometimes We Can Do The Impossible

BY **MYK DORMER**

Engineering usually consists of methodical application of well-understood techniques to well-defined problem. ...Well, most of the time. On rare occasions however, it can become far less predictable – and far more challenging and enjoyable – when the problem defies conventional solutions, and something innovative needs to be pulled out of the hat.

Integer-N phase-locked loop (PLL) frequency synthesizers are a very well understood and very widely used radio sub-system, providing a clean, programmable frequency source, with stability of the reference clock source.

In a nutshell, these circuits operate by dividing the output of a VCO and a fixed (crystal) reference oscillator down to a common (comparison) frequency, feeding the divider outputs into a phase comparator and using the output to tune the VCO. When the loop is "in lock" the VCO frequency is equal to the comparison frequency multiplied by the divide ratio of the (N) divider. This comparison frequency is the reference oscillator output divided down by the (R) divider.

In mathematical terms: $F_{out} = (F_{ref}/R) \times N$

There are obviously many additional implementation details that a circuit designer would have to consider, but that is the heart of the system. The finest frequency steps the synthesizer can tune in equals the comparison frequency, which is usually chosen to equal the channel spacing of the radio.

There are many newer, more sophisticated variants on this theme, notably "fractional-N" schemes, where by means of sophisticated logic design the N value is not an integer so the comparison frequency can be larger than the tuning-step size, but many radio devices still use the original, simpler technique I have described.

So what happens when a customer orders a variant of an existing (integer-N synthesizer based) radio on a frequency that is not a multiple of the usual comparison frequency?

Obviously, if the new channel frequency is a multiple of another, similar frequency (such as a change from a 25kHz channel step to 12.5kHz or 20kHz), then the R division ratio is changed to yield a new comparison frequency and N is re-calculated accordingly.

The really interesting problems arise when the new comparison frequency value cannot be generated from the existing reference oscillator frequency by an integer R value, or where the comparison frequency necessary for one or more of the channels is simply too low for acceptable loop dynamic behaviour (in typical narrowband low-power wireless equipment a comparison frequency much below 10kHz is likely to compromise setting time, so, say, a channel frequency of 153.005MHz could prove a problem).

Ideally, an engineer could meet these new requirements with a new radio, such as a new design with a fractional-N PLL, or even a reversion to a crystal-controlled radio, but in the real world, with limited engineering resources and large stocks of existing hardware, it is quite possible that no actual physical changes can be made.

In this case there is an interesting (and cunning) work-around.

While it may not be possible to come to a suitable compromise between N and R values and a comparison frequency within acceptable bounds for certain awkward frequencies, it is worth remembering that the PLL doesn't have to produce the exact-to-the-last-digit frequency; it only needs to produce a frequency within the frequency tolerance of the radio.

A typical narrowband low-power radio is designed around a frequency tolerance of somewhere around ±1kHz. The stability of the reference oscillator will have been specified accordingly, probably with a comfortable margin added in.

> If a radio has more than a handful of channel frequencies then one or more "no viable result" channels will be likely

To take our VHF example here, typical modules in this band use 5ppm crystals (or TCXOs), so have an absolute accuracy of around ±750Hz... what happens to the design if the PLL is programmed to generate a frequency that isn't exactly 153.005MHz, but is just within ±100Hz of it?

As far as the operation of the radio is concerned it doesn't matter one jot. The "error" in the PLL output frequency is swamped by the frequency tolerance of the reference, and both added together still fall inside the previously mentioned ±1kHz necessary accuracy.

Programming the N and R values, on the other hand, becomes possible.

Assume a 10MHz reference.

A 5kHz comparison would allow R = 2000, N = 30601, but we

have already decided that (to meet settling time requirements) F_{comp} must be over 10kHz.

Consider R = 599, N = 9165. The F_{comp} value is an outlandish 16.6944908kHz but the output frequency is only -8.35Hz different from the desired 153.005MHz.

By allowing small amounts of absolute frequency error in the calculations and accepting that the comparison frequency will have to be different for each channel frequency, it is possible for an integer-N synthesizer to generate output frequencies that at first inspection it should not be able to, whilst maintaining the comparison frequency within acceptable limits. It is even possible to use the same technique to push the comparison frequency up, to improve the settling time of the loop, and as such the radio's dynamic performance.

So, the fractional N synthesizer is an unnecessary complication, and the industry has been wasting this effort for thirty years? Of course not! This technique, whilst useful, has a number of significant limitations, including:

- Generating the combination of N/R values for a "close-enough" output frequency is not something done with a simple linear equation. There may be more sophisticated mathematics that can relate acceptable frequency error to N/R ratio, but it is beyond me; I use a brute force numerical analysis method and a lot of computing time.
- There is no absolute guarantee that every single combination of reference frequency, output frequency and error limit will yield a viable N/R combination. I have occasionally run into cases where no solution can be calculated. If a radio has more than a handful of channel frequencies then one or more "no viable result" channels will be likely.
- It is necessary to store separate N/R values for every channel. Existing radio firmware that generates a "table" of frequencies by assuming a constant R value and calculating N on the fly will not be usable for this method.

Within these limitations, however, this technique is a very useful "work-around" for an otherwise insoluble problem, and for the engineer it gives the enjoyable feeling of having "cheated" the physical laws we struggle with, even if only to a small degree. ●

Myk Dormer is a Senior RF Design Engineer at Radiometrix Ltd
www.radiometrix.com

RELEC ELECTRONICS LTD

Trying to keep a low profile?

Ranging from 40W to 112.5W with convection cooling and up to 225W with forced air cooling. Relec Electronics has a range of open frame ac dc power supplies on a 4" x 2" footprint with a height profile of just 25.4mm for those designs where a low profile is critical. All feature high efficiency with low standby power consumption and a universal ac input. Single fixed outputs range from 12 to 48Vdc on the lower power units and 12 to 58Vdc on the 112.5/225W unit.

Approved to IEC, EN, UL 60950-1 2nd edition, class II safety standards, the 40W & 60W PSU's have an optional function ground enabling them to meet class I when this is connected. Hold up time is between 10 and 16ms; the outputs are fully protected against over voltage and short circuits.

These power supplies are ideally suited for telecom, datacom and a wide range of industrial applications. For further information on the 40W **MPE-S040**, 60W **MPE-T060** or 112.5/225W **ABC225** series, view the Relec website or contact us directly.

Design solutions for design engineers

Relec Electronics Ltd
Tel: 01929 555800
e-mail: sales@relec.co.uk

www.relec.co.uk

Ensuring Optimum Performance of Today's Satellite Systems with FieldFox Handheld Analyzers to Ka Band and Beyond

Wilkie Yu, Keysight Technologies

According to recent announcements and forecasts, governments and private enterprises around the world are aiming to place hundreds of new satellites into orbit in the next few years. Many will be the latest generation of high-throughput satellites (HTS), some of which will use Ka-band frequencies—26.5 to 40 GHz—for up- and downlinks. The result will be tremendous increases in bandwidth and capability, and the ability to deliver advanced services to more people in more places.

In tandem, new earth stations and teleports will be constructed to manage the satellites and direct the signals they carry. To keep everything running smoothly, there is still a need for maintenance and troubleshooting of crucial earth station equipment: antennas, transmitters, receivers and transmission lines.

Testing of these elements has typically required five or six types of RF and microwave test equipment. Today, a single Keysight FieldFox handheld combination analyzer can replace the set of instruments traditionally used for measurements in the field (Figure 1).

Equipping the industry

As Hewlett-Packard, Agilent Technologies and now Keysight, we have spent decades equipping the satellite industry with exceptional high-frequency instrumentation. This includes vector network analyzers (VNAs), spectrum analyzers, power meters, and cable and antenna testers (CATs).

For field personnel, the all-in-one replacement is Keysight's FieldFox analyzer. These handheld combination analyzers are equipped to handle routine maintenance, in-depth troubleshooting and anything in between. This is possible because they can be equipped for CAT, spectrum analysis, vector network analysis, and more. In every operating mode, FieldFox delivers precise measurements at millimeter-wave frequencies—up to 50 GHz—virtually anywhere satellite maintainers need to go.

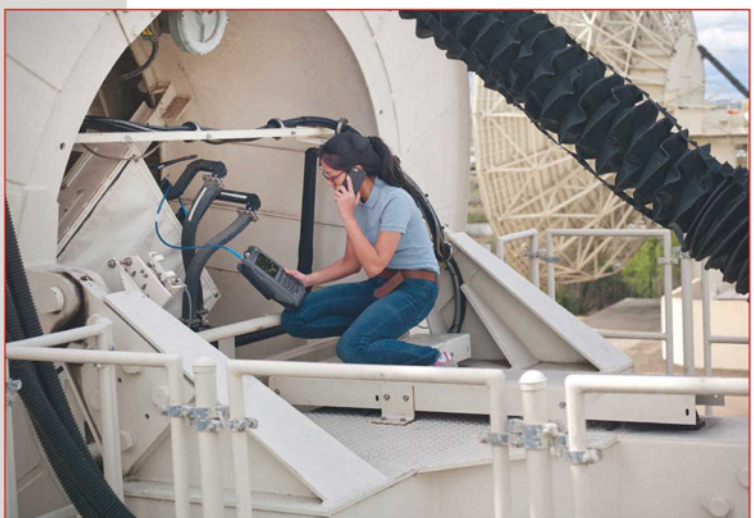


Figure 1: Easily carried to the antenna flange, FieldFox handheld combination analyzers can be equipped to handle tasks ranging from routine maintenance to in-depth troubleshooting. (Photo courtesy of INTELSAT)

While FieldFox provides important advantages in numerous measurement scenarios, spectrum analysis provides an especially compelling example. For more than 20 years, operators around the world have relied on the HP/Agilent 856x series of portable spectrum analyzers as part of their field kit for maintenance and troubleshooting. These widely used instruments are no longer in production and will soon move into the "extended support" phase.

Comparing the 856x series with FieldFox, the most obvious differences are in their physical attributes. An 856x measures 13.25 by 16.81 by 7.38 inches and weighs 38 pounds (17.2 Kg). Equipped with the latest features, functions and user-interface technologies, a 50 GHz FieldFox is just 11.5 by 7.4 by 2.8 inches and weighs 7.1 pounds (3.2 Kg) (Figure 2).

From Day 1, FieldFox was designed for durability: its mechanical design has no fans or vents. The rugged, fully sealed enclosure is compliant with US MIL-PRF-28800F Class 2 requirements. The analyzers have also been type tested to IEC/EN 60529 IP53 requirements for protection from dust and water, extending instrument durability in even the harshest environments.

Delivering modern advantages

FieldFox delivers exceptional performance, enabling engineers and technicians to carry precision with them. It starts with advanced measurement hardware and software as well as a modern digital architecture. Analog-based spectrum analyzers such as the 8565E/EC suffer from two important shortcomings: log fidelity errors, which affect amplitude accuracy, and span accuracy errors, which affect frequency accuracy. To compensate, users must adjust analyzer settings to place signal of interest at the top/center position of the display: that's the only measurement point that delivers the analyzer's best accuracy.

This is not an issue with FieldFox: its exceptional accuracy of ±0.5 dB is available anywhere on the screen, from minimum to maximum displayed frequency and from reference level to noise floor. This saves time and also provides greater confidence in measurement results. Table 1 provides a side-by-side comparison of key features and specifications.

Another timesaving advantage is the ability to start making measurements at power on: warm-up time is not needed. This comes from the "instant alignment" or InstAlign feature built into the analyzer. FieldFox is ready to make accurate spectrum measurements immediately and through any temperature changes over its specified operating range of 14 to 131 °F (−10 to +55 °C).

With these capabilities, FieldFox delivers results that match the world's highest performance spectrum analyzer to within tenths of

Figure 2: Compared to the widely used 8565E/EC family of portable spectrum analyzers (left), FieldFox handheld combination analyzers (right) provide major improvements in size, weight, performance and functionality.

	FieldFox	856x
Amplitude accuracy	±0.5 dB, no warm up	> ±4.0 dB after 30 minutes
Spurious-free dynamic range (SFDR)	104 dB	100 dB
Phase noise at 40 GHz	–74 dBc/Hz, 10 kHz offset	–69.7 dBc/Hz, 10 kHz offset
Displayed average noise level (DANL), 40 to 50 GHz	–142 dBm/Hz, preamp on	–127 dBm/Hz
Tracking generator	300 kHz to 50 GHz	300 kHz to 2.9 GHz

Table 1: FieldFox provides performance advantages in 7.1-pound package that provides a 3.5-hour battery life.

a decibel. This ensures confidence in measurements and reduces the risk of accepting bad systems, subsystems or components, or of failing good ones.

Applying the all-in-one analyzer

At an earth station, engineers and technicians can use FieldFox to validate system performance with fast, detailed analysis of uplink and downlink signals. This is true within the RF and IF portions of either signal path (Figure 3).

Calibrated CAT and VNA measurements help field personnel maintain cable, waveguide and antenna systems efficiently and consistently. The combination of network analysis, spectrum analysis, power measurements, and more, in one handheld unit enables faster diagnosis and repair of faults.

FieldFox also supports remote operation through an application that runs on a variety of Apple iOS devices. This feature enables collaboration between personnel, one example being an engineer working at a dish and another engineer below, analyzing measurement results using an iPad or iPhone.

Reducing upfront and ongoing costs

Although FieldFox replaces multiple instruments, it is priced such that each aspect—CAT, VNA, spectrum analyzer—is about one-half the cost of a comparable benchtop unit. Upfront, this provides a tremendous savings in capital expenditures.

Once FieldFox has been deployed, it also reduces ongoing costs. For example, the analyzer's design has proven its mettle in the field: FieldFox has the lowest failure rate of any complex microwave or millimeter-wave instrument from Keysight.

Another benefit of migrating to modern, field-ready technology is a reduction in operating expenses. FieldFox requires just one calibration per year, reducing annual costs compared to the traditional array of equipment that requires multiple calibrations per year. A standard three-year warranty also reduces overall repair cost.

Wrapping up

As new-generation earth stations come on line, FieldFox handheld combination analyzers offer a powerful all-in-one solution. With a robust array of essential, accurate and timesaving capabilities packed into a durable, 7.1-pound (3.2 Kg) unit, engineers and technicians will be equipped for faster diagnosis and repair of today's most advanced installations.

The recently introduced line of six millimeter-wave FieldFox instruments includes three combination-analyzer models that cover 32, 44 or 50 GHz and three spectrum-analyzer models that cover the same frequency ranges. For more information, please visit www.keysight.com/find/FieldFox.

Keysight Technologies
www.keysight.com/find/fieldfox

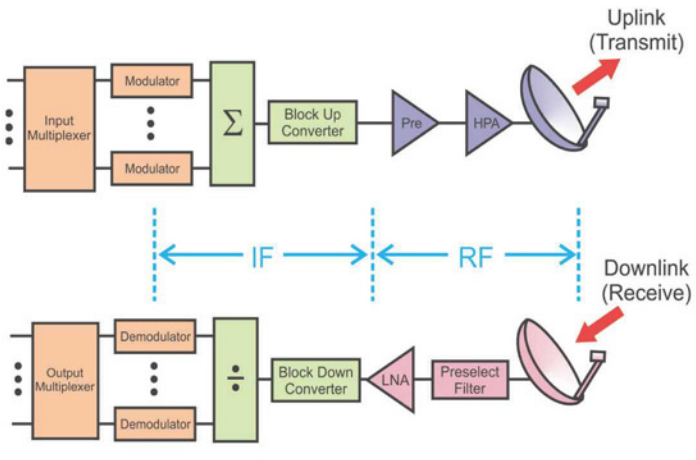
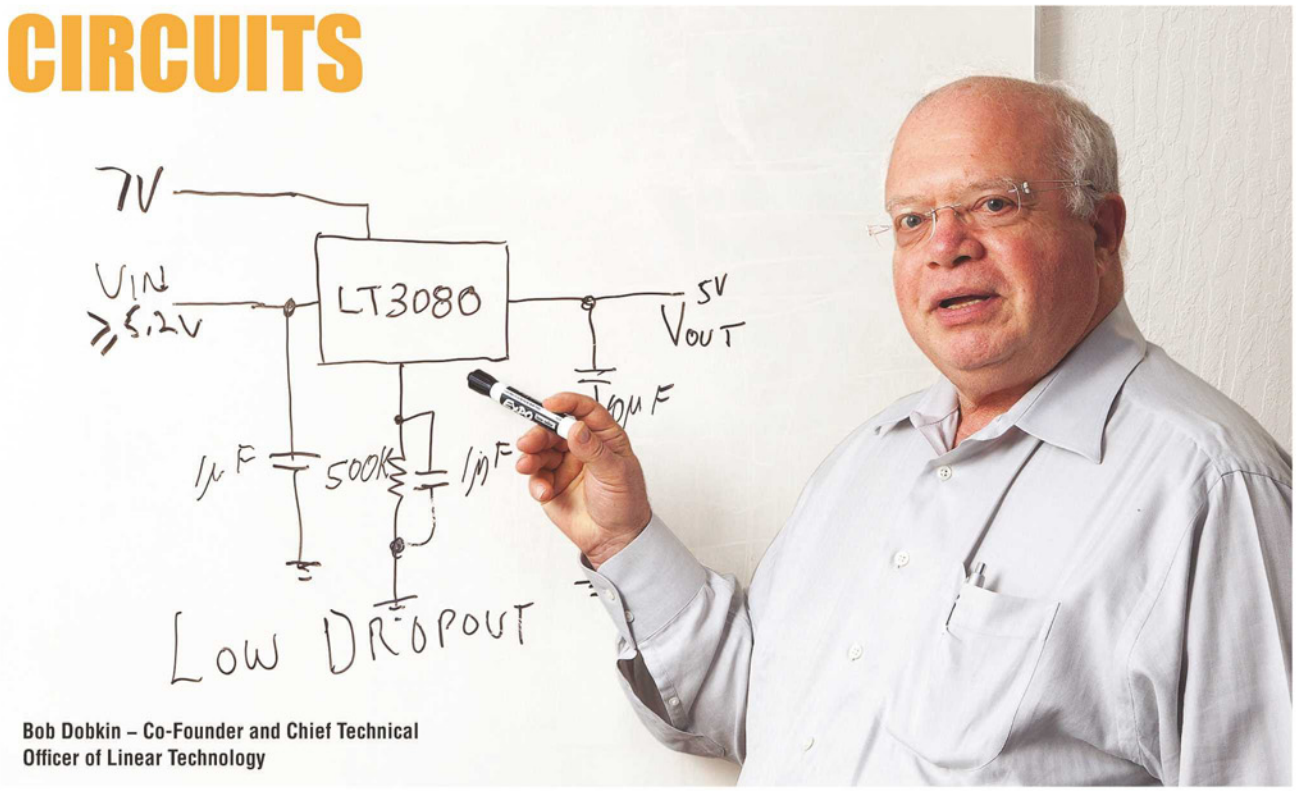


Figure 3: These simplified block diagrams of transmitter and receiver channels illustrate the elements field personnel can measure, characterize and troubleshoot using a FieldFox all-in-one analyzer.

THE EVOLUTION OF ANALOG CIRCUITS



Bob Dobkin – Co-Founder and Chief Technical Officer of Linear Technology

BY **BOB DOBKIN**, CO-FOUNDER AND CHIEF TECHNICAL OFFICER OF LINEAR TECHNOLOGY

For the last forty years, analog circuits have accounted for 20% of the total integrated circuit (IC) market. As digital ICs advanced both in complexity and function, so have analog ICs. But while digital ICs have increased in functionality, which is based on the number of transistors, analog ICs have progressed by other metrics. For digital ICs, performance advances depended on the reduction of both feature size and transistor size. Squeezing more transistors onto a chip increased the productivity of the digital IC. Analog ICs are based on real-world parameters, so power, resolution and speed, among others, are the parameters for improvements in analog productivity.

Digital is information – numbers, voltages and currents do not matter in digital circuits as long as the input and the output are correct. In a digital circuit it doesn't matter how the signal gets from input to output. Digital circuits can be gate arrays, microprocessors or discrete logic, as long as they work properly.

Analog functions take into account real-world parameters, such as voltage and current, noise and speed – all analog properties defined in analog ICs. So with analog circuits, how you get from an input signal to an output signal is critical.

Process Innovations

The process innovations for digital ICs have greatly impacted the analog side. Forty years ago analog ICs were produced using an eight-mask process. Almost all manufacturers had very similar processes and the types of devices they produced were also very similar. Now, each company manufacturing analog ICs has its own processes and variations, so there is no such thing as a plug-in second source.

> Analog ICs do not shrink the same way as digital ICs

Process improvements for analog are not only in transistor size, but also in process complexity. Analog ICs are frequently manufactured with as many as 50 mask layers, and contain a mix of bipolar, CMOS, thin film resistors and other specialized IC components needed for the analog functions.

Analog ICs do not shrink the same way digital ICs do. Some

parameters for analog ICs such as voltage and current require certain chip areas too. Higher voltage demands larger transistors and greater spacing, so new lithography cannot shrink the chip. High-current operation requires large-area transistors, and shrinking parameters do not improve the ability of the transistor to carry high currents. Also, power dissipation requires large chip area and good thermal connections for proper operation. As a result, analog circuitry is more physically tied to the function it performs.

Further Improvements

The density improvements originally designed for digital have been adopted for analog ICs as well. Smaller transistors operate faster, so applications have flourished using the new transistors enabled by tiny line widths. High-speed RF circuits running at low power at gigahertz frequencies are now common.

Analog-to-digital converters with resolution of over 20 bits, or converters that operate at gigahertz frequencies, are the direct result of having fast, small CMOS transistors as part of the process. As these fine line processes are driven down in cost by the huge volume of digital circuits they support, the analog circuits produced in these processes continue to be more cost-effective and more widely available.

Switching regulators operating at multiple megahertz with 95%-plus efficiency are the result of the finer line transistors. The smaller transistor size allows analog ICs to have an immense amount of digital support circuitry, as well as faster analog circuitry.

Analog component parameters have improved as well, among them op-amp speeds and DC precision. Linear regulators (LDOs) have lower dropout, lower supply current and analog monitoring outputs. New architectures for linear regulators enable the paralleling of devices without specialized external circuitry and adjustment to zero output. One particularly interesting new LDO has an output noise of 1μV from 10Hz to 100kHz – better than many low-noise amplifiers.

Commitment

These developments result from new circuit innovations, cleaner fabs, better masking, better defect density in masks and wafers, and larger wafers. Analog integrated circuits have improved their performance, in addition to implementing greater system performance on chip.

Neither digital nor analog ICs have had step function changes from year to year. Development has been a steady progression of improved performance parameters over the last 40 years. Over the next decade and beyond we can look forward to further improvement in analog circuit innovation and performance. ●

BOB DOBKIN, CO-FOUNDER AND CHIEF TECHNICAL OFFICER OF LINEAR TECHNOLOGY CORP ON…

… the big difference between analog technology in the 1990s and today:

There are many big differences. Circuits are much more complex because of the ability to simulate with good accuracy, so problems can be identified before going to silicon. Also, complex circuits with significant digital content can be combined with analog circuitry on one chip.

Higher performance of analog circuitry is now available; complex power switching circuitry combined with feedback and telemetry is now available; data converters with high speed and high accuracy are in production at multiple manufacturers; higher speed amplifiers with high accuracy are commonplace; and, linear regulators are available in new configurations with monitoring functions.

With data converters, speed and resolution are increasing. A 20-bit data converter is available with less than one ppm resolution and less than one ppm linearity. This has trickled down to make 16-bit converters the workhorse of the industry with 18-bit converters the upgrade.

… Moore's Law:

Linear circuits are typically several generations behind cutting-edge digital technology; whilst digital circuits are at 14nm, very few linear circuits are below 65nm.

Analog circuits do not need cutting-edge digital line widths. In fact, many analog circuits require bigger feature sizes, since high voltage and high current do not benefit from scaling transistors down. Relatively large sizes, such as 0.35 micron for MOS and 7 micron for bipolar, are the norm.

… analog designers:

Some people like doing analog circuits and really appreciate the environment at Linear Technology. We have an easier time hiring analog designers because we are known for analog design. Other companies may find it more difficult, and find analog designers a more precious commodity.

We hire analog designers straight out of college, and they continue their training while with us. We also hire experienced designers.

… the future of analog design:

Analog is still needed with ever-higher performance. We keep discovering new things both in the silicon and in the circuits to make new products. The future was bright when we started Linear Technology and it's much brighter now; we clearly know more today about analog circuitry and processes than when we started the company.

Looking at our knowledge now, we did a lot of stumbling along. Analog IC development is more scientific and less "black art" – although there is still a good portion of art in it.

PUSHING THE LIMITS

LUCIO DI JASIO, ELECTRONICS ENGINEER AND TECHNICAL AUTHOR, EXPLAINS HOW TO INCREASE USB CURRENT TO CHARGE PORTABLE DEVICES MORE EFFICIENTLY

The universal serial bus (USB) is the most used computer interface. It started as an expansion bus for personal computers, but quickly proliferated because of its flexibility, performance and hot-plug capability. Most portable electronic devices that require PC connectivity use USB for file transfers, including MP3 players, digital cameras, mobile phones and tablets.

Since a standard USB bus downstream port can provide at least 500mA (USB 2.0) or 900mA (USB 3.0) of current, it was convenient to use it for charging these devices. But, if this current limit was increased, the charging could be more efficient. This can be achieved with the Microchip USB2534 hub controller with RapidCharge.

If the current required exceeds the limit, then both the charging device and port must follow a protocol to enable battery charging.

A downstream battery charging port is responsible for providing the proper handshake signalling to the charging device to indicate that it is attached to a charging port and can draw current above the standard USB limits. The proper signalling varies depending on the portable device. Some portable devices follow the USB-IF BC1.2 protocol, but there is an installed base of devices that use proprietary handshake protocols for battery charging, also known as legacy modes.

> Some portable devices follow the USB-IF BC1.2 protocols, but there is an installed base of devices that use proprietary handshake protocols, also known as legacy modes, for battery charging

Legacy devices support some form of battery-charging detection intended for use with a dedicated charger. Some of these chargers short D+ to D- directly or connect them through a series resistor. For charger detection, some legacy devices assert a voltage on D+ by connecting a pull-up resistor and then sensing a voltage on D-. If a positive voltage is detected, the device can assume it is plugged into a dedicated charger and not a standard USB port.

Other devices pull down one data line while pulling up the other. Once the device detects a charger by the presence of a voltage on D-, it can start charging from the V_{bus} connection at current levels that exceed the USB specification.

Other legacy devices that rely on the charger to drive fixed voltages (more than 1V) on the D+ and D- data lines, are referred to as SE1 chargers. If these voltages are sensed by the charging device, the device assumes it is plugged into a dedicated charger and starts charging. A standard USB downstream port would not present these fixed voltages on the D+ and D- lines.

Charger Detection

The portable device is responsible for charger detection and Figure 1 shows the necessary hardware.

There are five functional blocks shown in Figure 1 – V_{bus} detect, data contact detect, primary detection, secondary detection and ACA detection. A portable device includes a session valid comparator. V_{bus} has to be above the threshold voltage before charger detection is initiated. This is shown as $V_{OTG\_SESS\_VLD}$ on the diagram.

Data contact detect is an optional block used to confirm that the data lines made contact during attachment. A current source on D+ and a pull-down resistor on D- are turned on. If the D+ line goes low, it indicates the data lines are attached to a charging port or a standard port and the logic proceeds to start primary detection. A timeout circuit is needed to ensure that primary detection starts following a set time after attachment, in case contact is not detected or the data contact detect block is not present.

A portable device is needed to implement primary detection, used to distinguish between a standard downstream port (SDP) and a charging port. Figure 2 shows what happens when the device is connected to a dedicated charging port (DCP); Figure 3 when it is

connected to a charging downstream port (CDP); and Figure 4 when it is connected to an SDP.

Secondary detection is used to distinguish between a DCP and a CDP. If a portable device is ready for enumeration within a set time after V_{bus} detection, it can bypass secondary detection; otherwise, it needs to implement it. Only portable devices with a USB Micro-AB connector can support ACA detection, and thus it's optional. Detection is done by measuring the resistance of the ID pin.

Battery Charging

The Microchip USB2534 hub controller includes RapidCharge technology for providing the proper handshake signalling to portable devices on downstream ports to enable battery charging. It also includes the capability for USB upstream battery-charger detection.

To charge most portable devices it is necessary to provide the proper handshake signals for legacy chargers, SE1 chargers, chargers compliant with Chinese Telecommunications Industry battery-charger specification YD/T 1591-2009, and BC1.2-compliant devices. The hub controller includes all these protocols to implement complete battery-charging, supporting devices from Apple, Samsung and others.

If a USB downstream port is configured to support battery charging, the port is a CDP if it can enumerate the device or DCP if it cannot. If the port is not configured to support battery charging, the port is an SDP.

The downstream ports can also be enabled for battery charging by adding a pull-up resistor (10kΩ) on the battery-charging configuration strap for the corresponding port. These straps are sampled at reset, and if they are sampled high the corresponding port is enabled for battery charging.

Battery charging can be also enabled by using battery-charging configuration registers that reside in the USB2534. These configuration registers are used by the internal ROM firmware to configure the battery-charging functionality for each port. The registers can be modified by a configuration programmed in the one time programmable (OTP) memory using the ProTouch programming tool, which was developed by Microchip for configuration and programming of the USB2534 hub controller.

When there is no upstream V_{bus}, and consequently no USB host connected on the upstream port, the downstream battery-charging-enabled ports will operate as DCP ports. The battery-charging-enabled ports will exit this mode if the upstream port has a host connection. DCP mode will be also entered if the USB2534 is suspended and remote wakeup disabled.

In DCP-mode battery charging, the port will attempt to handshake with and identify the BC-capable device. Here the device always starts in SE1 mode. It cannot detect that an SE1 device is attached, but can detect that a non-SE1 device is attached when the device toggles DM or DP.

Upon entering RapidCharge mode, the USB2534 goes into SE1 charging mode and the port presents the SE1 voltage levels. If an SE1 device is attached, it will passively detect the SE1 levels and begin to charge. The DCP will not be able to detect the presence of the SE1 device; the port remains in SE1 charging mode while the SE1 PD is charging.

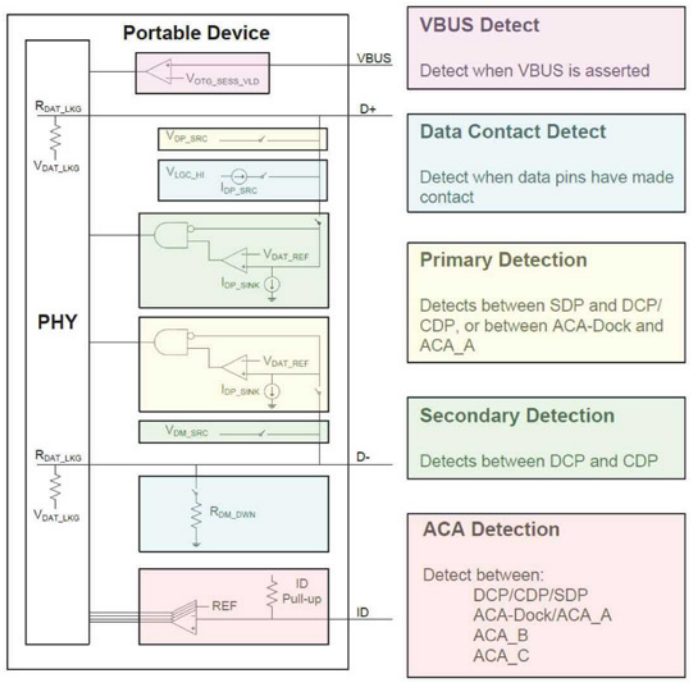


Figure 1: Charger detection hardware

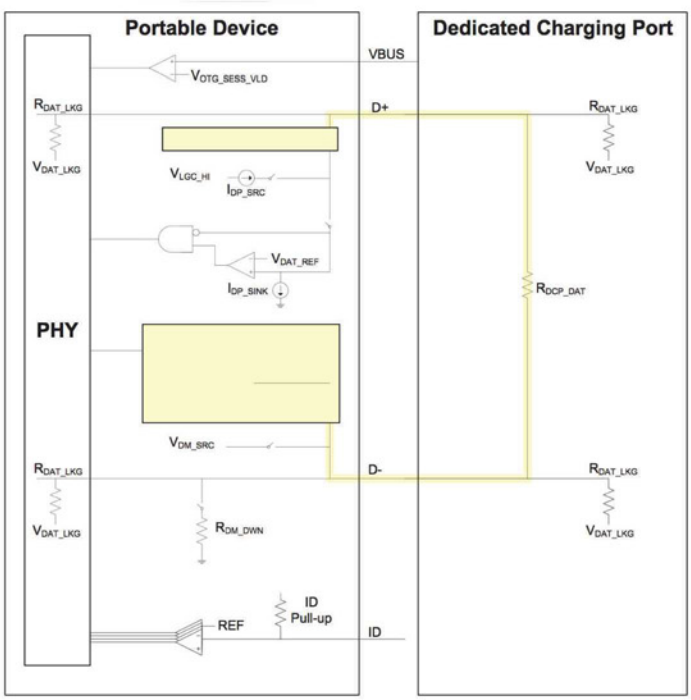


Figure 2: Primary detection with a dedicated charging port

If a BC 1.2 device is attached, its current is enough to pull the D- line low. Likewise, legacy charging devices have been observed to pull the D- line low when attached. To accommodate this, the downstream port transitions to legacy charging mode (Figure 5) if the classic D- line state is detected as low. The D- line state is de-

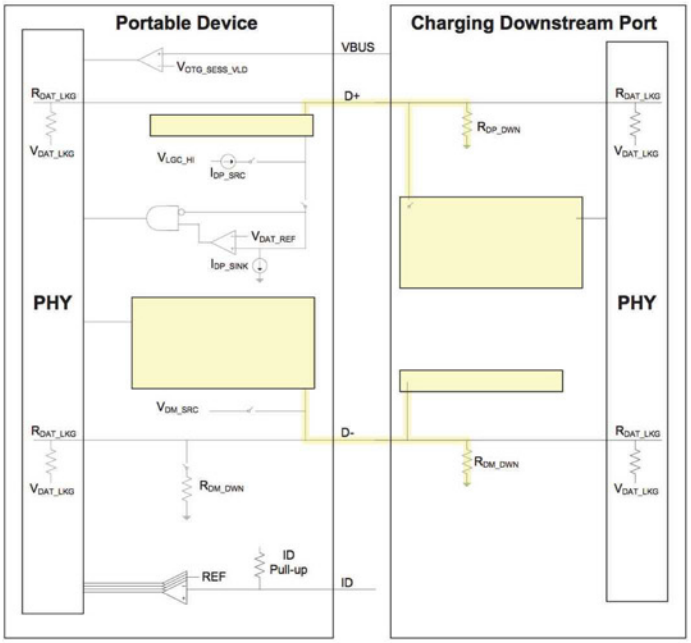


Figure 3: Primary detection with a charging downstream port

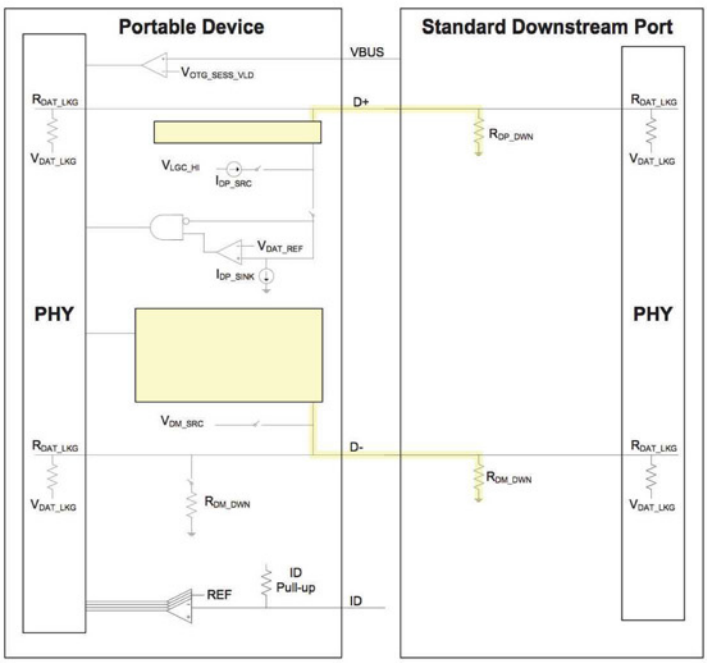


Figure 4: Primary detection with a standard downstream port

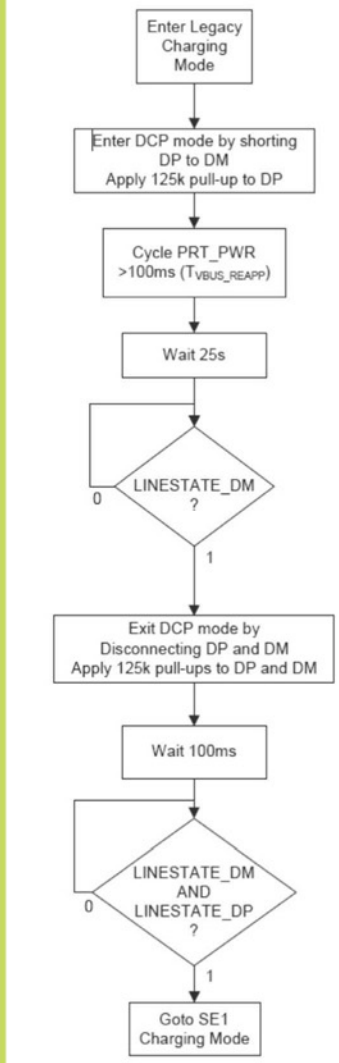


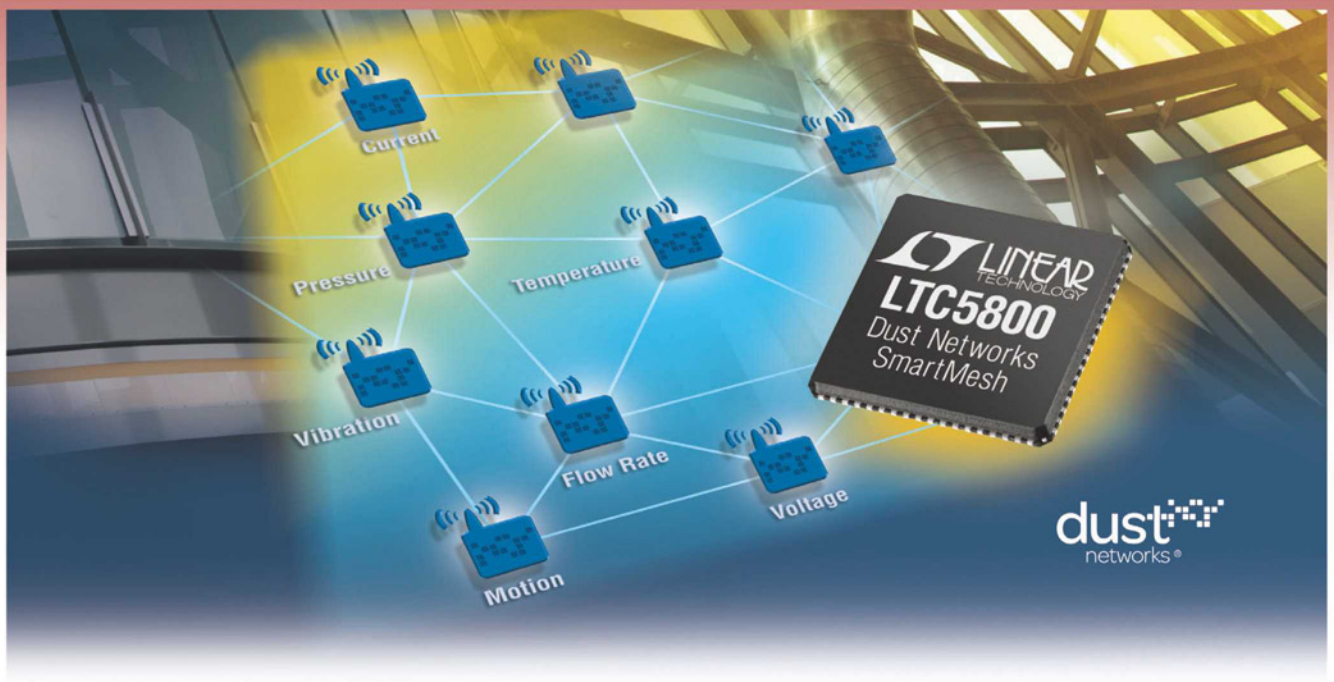
Figure 5: Legacy charging mode

bounced to avoid false detects from device plug-ins.

The battery-charging-enabled ports will exit DCP mode and enter CDP mode if the upstream port gets a host connection. Upon detecting the USB-host-set address command, any BC-enabled port will be turned off for at least 250ms before it can be turned on, to allow the port power to decay. If the host sends a command to turn on the port power, the command will be delayed appropriately; if the command is received after the timer has expired, it will be executed immediately.

An external MCU can override the automatic charger detection sequence by modifying the SMBus runtime battery-charging registers. Because the start of battery-charging detection is set to occur by default, the MCU must write to the battery-charging control register or the configuration interlock register to disable the automatic sequence before it begins. If the automatic sequence is disabled, the MCU can still initiate it manually. ●

Wireless Mesh Network. Wired Reliability.



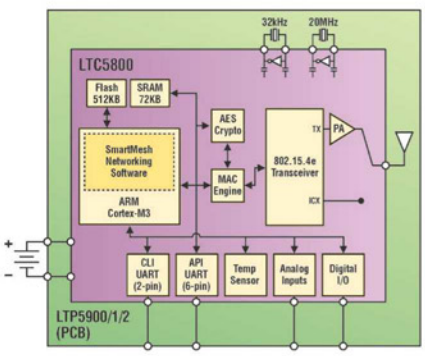
Every Node Can Run on Batteries for >10 Years at >99.999% Reliability

The Dust Networks LTC®5800 and LTP®5900 product families from Linear Technology are embedded wireless sensor networks (WSN) that deliver unmatched ultralow power operation and superior reliability. This ensures flexibility in placing sensors exactly where needed, with low cost "peel and stick" installations. The highly integrated SmartMesh® LTC5800 (system-on-chip) and LTP5900 (PCB module) families are the industry's lowest power IEEE 802.15.4e compliant wireless sensor networking products.

Features

- Routing Nodes Consume <50µA Average Current
- >99.999% Reliability Even in the Most Challenging RF Environments
- Complete Wireless Mesh Solution – No Network Stack Development Required
- Network Management and NIST-Certified Security Capabilities
- Two Standards-Compliant Families: SmartMesh IP (6LoWPAN) and SmartMesh WirelessHART (IEC62591)

Highly Integrated LTC5800 and LTP5900 Families



Info and Purchase

www.linear.com/dust

Linear Technology (UK) Ltd.,
3 The Listons, Liston Road,
Marlow, Buckinghamshire,
SL7 1FD, United Kingdom.

Phone: 01628 477066
Fax: 01628 478153
Email: uksales@linear.com

Experience SmartMesh Networks

www.linear.com/starterkits

LT, LTC, LTM, LTP, Linear Technology, the Linear logo, the Dust Networks logo and SmartMesh are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

Arrow Electronics UK Ltd 01279 626777
Farnell 08447 11 11 11

LINEAR TECHNOLOGY

LINEAR EXPRESS
Linear Technology (UK) Ltd. 01628 477066

NOVEL HIGH-PERFORMANCE MECHANISM
FOR THE PREDICTION OF INTER-ROUTER SWITCH ALLOCATION

JIAN CAO, HAI JIAO, YUAN WANG, QIHUI ZHANG AND **XING ZHANG** FROM THE SCHOOL OF SOFTWARE AND MICROELECTRONICS AT PEKING UNIVERSITY PROPOSE A NOVEL MECHANISM TO INCREASE NETWORK SATURATION THROUGHPUT AND MINIMIZE PACKET AVERAGE LATENCY THANKS TO A THREE-STAGE ROUTER PIPELINE AND A LOOK-AHEAD ROUTING ALGORITHM

With today's increasing demand for computational power and the shrinking transistor sizes, chip complexity is rising at an ever faster speed, aided by the number of cores integrated onto a single die.

Nowadays, the focus of chip design has largely moved from computation-centric to communication-centric, the network-on-a-chip (NoC) being a typical example. NoC was developed to efficiently tackle the tough communications requirements, with hundreds and even thousands of cores integrated onto a single chip. Essentially, the main goal of most NoC router designs is to maximize network throughput whilst minimizing packet average latency at lower power consumption.

> In our design, we combined the benefits of switch allocation prediction and reduced pipelined stages, and as such created a novel router

Over the past few years there has been substantial research on different aspects of the NoC, including routing algorithms, fault tolerance, quality-of-service, and so on. The router architecture at the centre of the NoC has a great impact on the area and power consumption of the entire network, as well as packet latency and throughput; therefore, many research projects have been devoted to the effective and efficient design of the NoC router's micro-architecture.

Previously, a lot of effort focused on router pipelined design and quality of switch allocation. Packet chaining and pseudo-circuit are some of the design schemes that maximize the quality of router switch allocation by performing 'predictions' based on historical events and future requests respectively. A speculative router pipelined design successfully reduces the pipelined stages, which offers a lower network zero-load-latency; however, the scheme suffers from a large chip area as it has to integrate more logic for the miss-speculative cases.

In our design, we combined the benefits of switch allocation prediction and reduced pipelined stages, and as such created a novel router. We used a look-ahead routing algorithm for passing routing calculation information from the upstream router directly to the downstream router before the actual data packets arrive, whilst switch allocation is being optimized in a predicted manner. Thus, a speculative pipelined design could be used together with switch allocation prediction.

Router Architecture

Our proposed router design belongs to the virtual-channel router family, where each physical channel contains multiple virtual channels to increase the router's efficiency and improve

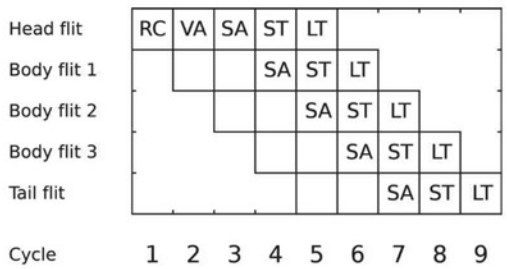


Figure 1: Traditional five-stage pipelined design

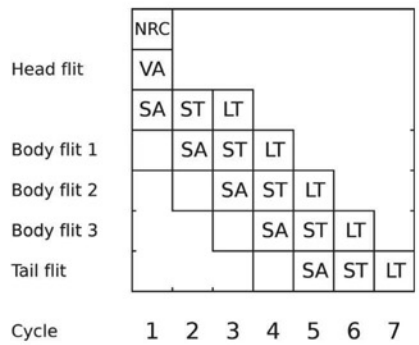


Figure 2: Our proposed router pipelined design

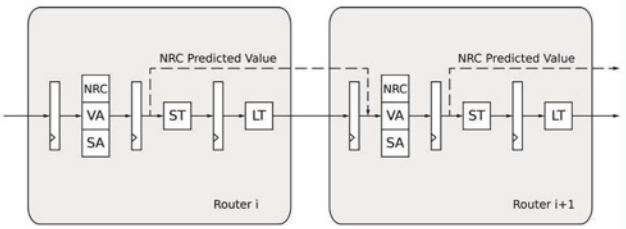


Figure 3: Passing NRC information

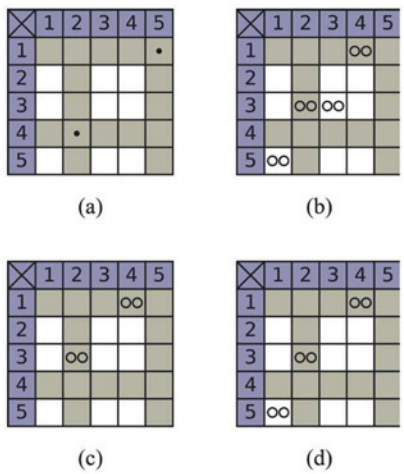


Figure 4: Priority matrix

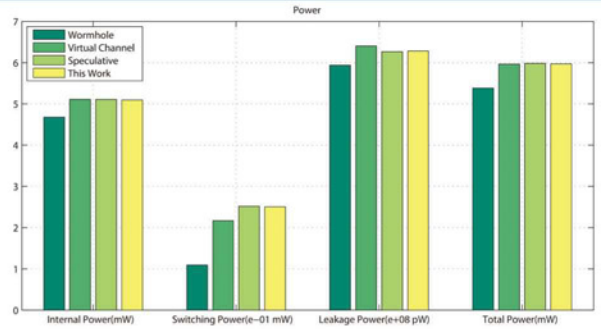


Figure 5: Power consumption of different routers

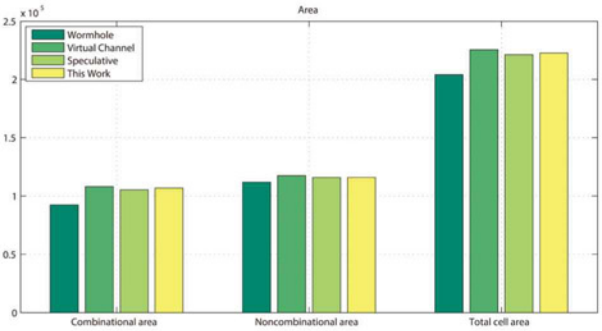


Figure 6: Comparison of router area usages

network throughput. The router architecture has a three-stage pipeline: starting with the paralleled execution of routing computation (RC), speculative virtual-channel and switch allocation (Spec-VA/SA), followed by switch traversal (ST) and link traversal (LT), as shown in the space-time diagram of Figure 2.

Since only the head-flit of each packet needs to perform RC and VC allocation, the shorter the package length, the larger the advantage in terms of average packet latency compared to traditional five-stage pipeline router designs as shown in Figure 1.

The next-route-computation (NRC) information from an upstream router transmits directly to the downstream router as shown in Figure 3, before the actual arrival of data packets in the former router design carrying routing information in the head-flit. During this time, the downstream router uses the NRC information for switch allocation optimization to increase network throughput, and decrease packet transfer latency and network zero-load-latency. We know that under moderate network traffic, speculative VA and SA stages can be performed successfully, thus producing a lower per-hop packet latency.

A switch allocator priority matrix is designed to resolve conflicts when multiple input and output requests occur simultaneously. The form of this priority matrix is identical to that of the request matrix, but with ones and zeroes being illegal entries.

As shown in Figure 4a, the predicted request is displayed as a black dot which represents a pending input/output port request in the next allocation cycle. When such a prediction exists, the priority level of the entire row and column of the matrix is raised to 1, shown with colour cells in the matrix.

To simplify the circuit, when multiple predictions are presented simultaneously, cells in the matrix with prediction intersections, such as (1, 2) and (4, 5) for example, will remain at the same priority level as their neighbours. If conflict within the priority matrix continues, a winner is chosen arbitrarily.

Figures 4b to 4d show an example of the input/output port switch allocation; symbols inside the matrix represent requests in the current cycle, and the colour cells are where allocation priority exists.

A conflicting request is resolved by choosing one with priority; such as for example, eliminating request (3, 3) and leaving (3, 2) as shown in Figures 4b and 4d. Requests outside the priority cells with no conflicts, such as (5, 1) for example, are left within the request matrix after allocation; see Figure 4d.

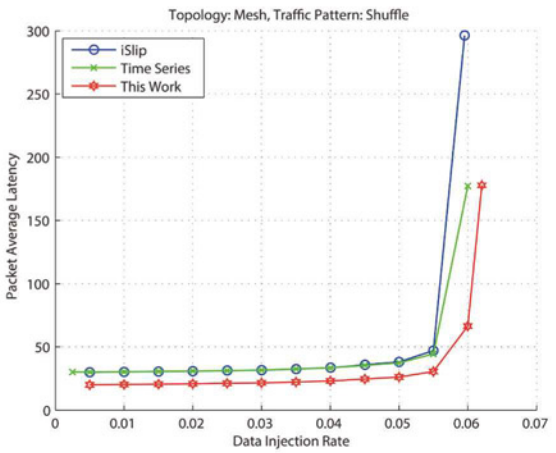


Figure 7: Shuffle traffic on mesh topology

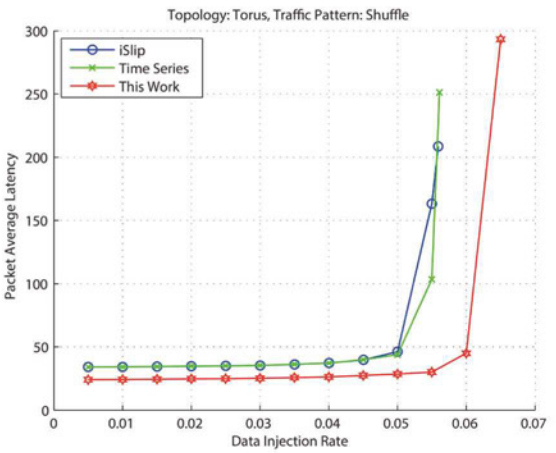


Figure 8: Shuffle traffic on torus topology

Router Implementation

To determine our proposed router's power consumption and area, we used a design compiler from Synopsys, with Verilog RTL codes, and synthesized the design using the TSMC 90nm standard cell library.

Comparisons of power consumption and area with other modern router designs are shown in Figures 5 and 6 respectively. It can be seen that the proposed router has comparable power consumption and slightly higher area usage due to the included inter-router switch allocation prediction mechanism.

Booksim 2.0, a cycle-accurate NoC simulator, was used to perform estimates of network throughput and average latency. The results were compared with TS-Router and iSlip respectively. The default configurations of the simulator are shown in Table 1. If these configurations are modified in a specific simulation, they will be mentioned to avoid confusion.

The evaluation of the network's average packet latency versus traffic injection rate is iterative, when changing the traffic injection rate on every simulation run; the synthetic traffic used in the evaluation is generated internally by the simulator.

The same experiment is performed both on mesh topologies and more path-diversified torus topologies. The networks' saturation throughputs can easily be observed from the traffic injection rate versus latency results, by defining an upper latency limit. When the packet's average latency becomes higher than this limit, we can say the network is saturated. In all our experiments the limit was set to 350 clock cycles.

Simulator's default configurations

Topology	Mesh
K	8
N	2
Routing Function	Dimension Order
Number of VCs	8
VC Buffer Size	8
Packet size	4
Injection Process	Bernoulli

Table 1: Default configurations

Router Architecture

In this experiment, shuffle traffic patterns are injected into 8-ary two-cube mesh and torus networks respectively. The performance evaluation of the proposed router is compared with TS-Router and iSlip in those configurations. As we see in Figures 7 and 8, the proposed router has outperformed its references both on packet average latency and saturation throughput. This proposed router's zero-load-latency is obviously lower than its counterparts', credited to the speculative three-stage pipelined design.

The advantage of our novel router's saturation throughputs can be more clearly seen in the torus network configuration experiment, partly due to the inter-router switch allocation prediction mechanism implemented in its design, which provides a higher quality of allocation in the SA stage, and partly due to the richer path diversity of the torus network topology, in which more routing paths can be selected.

Uniform Traffic Experiment

In this experiment, a uniform traffic pattern is injected into the network. As previous experiments showed, the same dimension mesh and torus network are used for the evaluation. From average latency versus data injection rate simulations, shown in Figures 9 and 10, we can see that the proposed router outperforms its reference models. The saturation throughputs

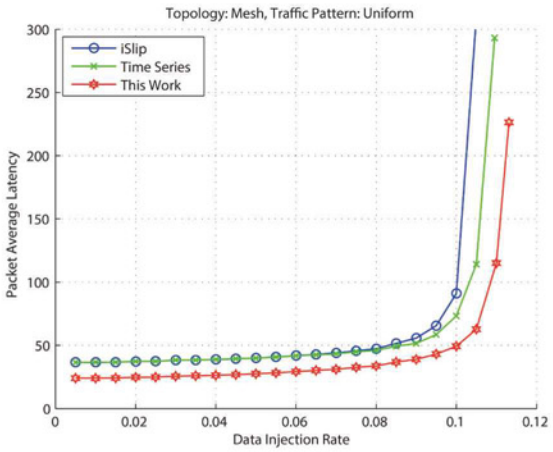


Figure 9: Uniform traffic on mesh topology

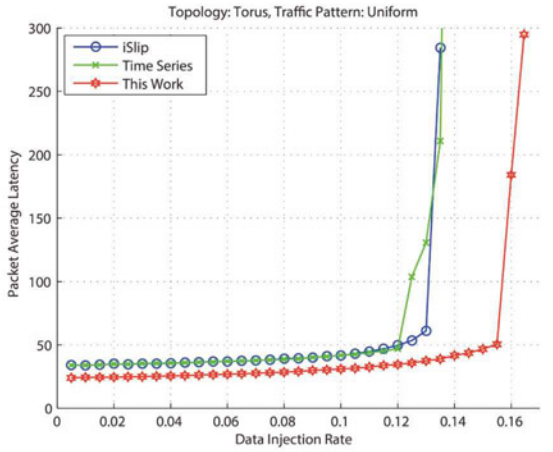


Figure 10: Uniform traffic on torus topology

of both configurations are higher than those of previous experiments in which a shuffle traffic pattern was used. Thus, with more variety of routing destinations, such as a uniform traffic pattern, the network resource is better used.

The same is also applicable to homogeneous multi-process chips and system-on-chip designs, in which one task can be accomplished with any of the same functional cores compared to a specific heterogeneous design.

Saturation Throughputs

A comparison of saturation throughputs of the proposed router versus its counterparts is provided for both mesh and torus topological networks, and shown in Figures 11 and 12. The proposed router outperforms its counterparts in mesh topology under shuffle, tornado and uniform traffic pattern cases where there are more routing destinations varieties, and the advantage is seen in the torus network configuration experiments where there are more routing diversities.

Novel Mechanism

The novel mechanism for inter-router switch allocation prediction is implemented into our proposed router's specifically-designed pipelined stage, where VA and SA are performed speculatively, together with look-ahead routing algorithm to generate the switch prediction information for the downstream router.

The downstream router uses this information for switch allocation optimization to maximize the quality of allocation not only on the current cycle but also on the average quality of a series of allocations.

The performance evaluation experiments show that our proposed router has lower packet average latency over other models and higher saturation throughputs on average, with maximum increase performance of 21.3% in the best case.

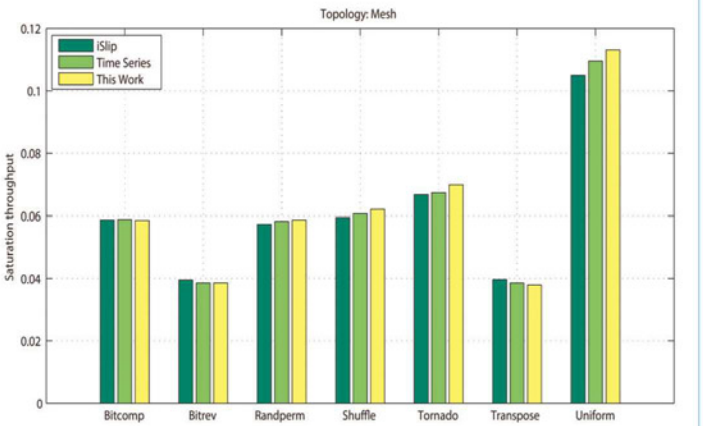


Figure 11: Saturation throughputs on mesh topology

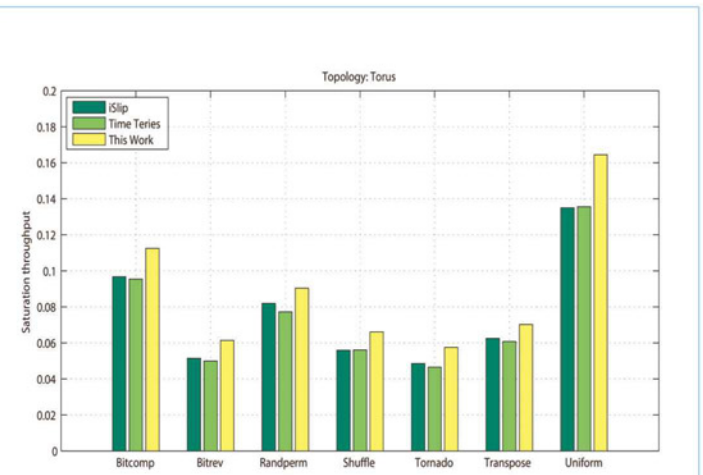


Figure 12: Saturation throughputs on torus topology

PERFORMANCE ANALYSIS OF DIFFERENT DIGITAL LOGIC FAMILIES FOR THE SYNTHESIS OF NAND GATES

LEAKAGE POWER HAS BECOME A SIGNIFICANT CONCERN FOR THE DESIGN OF LOW-POWER SOCS IN DEEP SUBMICRON NANOMETER CMOS PROCESS TECHNOLOGIES. **MOMNA ASGHAR, SIDRA ASHRAF** AND **SHABBIR MAJEED** FROM UNIVERSITY OF ENGINEERING AND TECHNOLOGY IN TAXILA, PAKISTAN, INVESTIGATE

Digital integrated circuits (ICs) are a vital building block in the design of systems-on-a-chip (SoCs), and many are embedded in devices where power is limited, such as mobile phones, laptops, tablet PCs, watches and so on.

Efforts are continually under way to achieve high performance and high density in digital circuits but at low power consumption. Power consumption in a digital circuit occurs due to charging and discharging of the capacitive load; during transitioning of the logic gates (from the short-circuit current due to the brief self-induced conducting path between the supply voltage and ground); and because of the leakage current that exists due to reverse-bias transistor current and sub-threshold current.

Improved performance and high density have been largely achieved by reducing the feature sizes of the CMOS transistors, and also by scaling down their threshold voltage. In turn however, transistor leakage power has increased dramatically.

A	B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

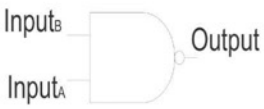


Figure 2: The truth table and symbol of the basic NAND gate

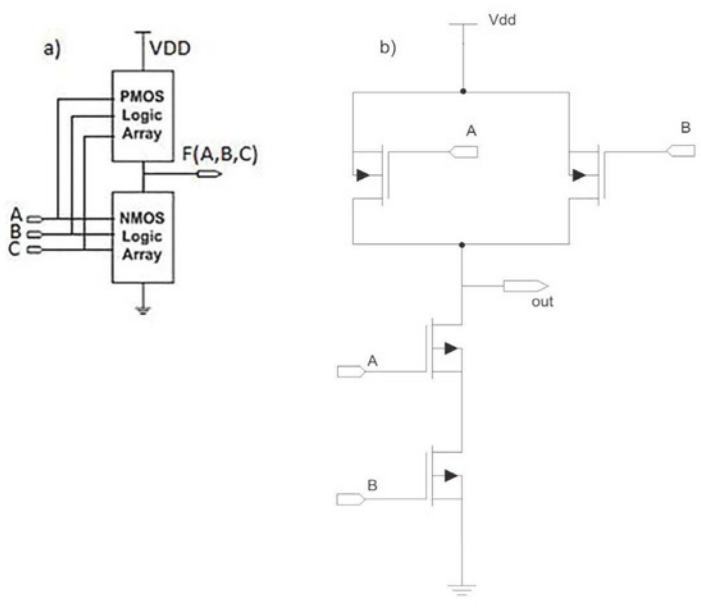


Figure 1: (a) Static NAND gate; (b) Static CMOS logic gate structure

Improved Performance

Static CMOS logic was one of the earliest technologies used in circuit design. It offers advantages such as low power and high noise-tolerance, and it does not require a clock. On the other hand, it needs more transistors for the implementation, which is a major disadvantage, along with lower signal speeds and longer signal delays.

For the implementation of high-speed and low-power VLSI circuits, dynamic CMOS, especially the so-called domino logic, has been widely used. Its limitations however include charge sharing, charge leakage and clock skew among others, and one key disadvantage is that it can only be implemented with non-inverting logic.

Another popular logic implementation, particularly in low-power circuits, is pass-transistor logic (PTL), which uses a set of controlling signals at the gate of an NMOS transistor. The advantages of PTL over standard CMOS logic include high speed, low power dissipation, reduced number of transistors and a small chip area. However, on the negative side, the PTL has two issues: slow operation at reduced power input and static power dissipation.

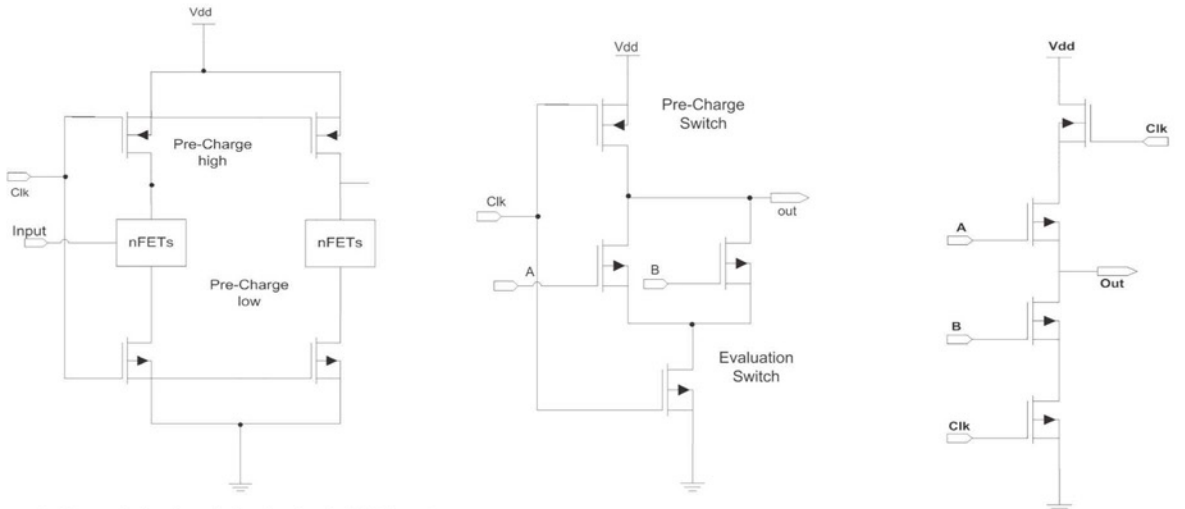


Figure 3: Dynamic logic and domino logic NAND gate

The Basic Static Cell

A static CMOS gate consists of two parts: a pull-up network (PUN) and a pull-down network (PDN); see Figure 1a. Each configuration is designed so that only one of the networks conducts in steady state, irrespective of input. A false (0) output results if both gate inputs are true (1); if one or both inputs are false (0) the result will be true (1).

The NAND gate is a key building block in ICs because it can be used to implement any Boolean function. Figure 1b shows its implementation using static logic.

The mathematical expression for the NAND gate is:
Output = $(Input_A)' + (Input_B)' = (Input_A . Input_B)'$
its truth table is shown in Figure 2.

Dynamic Logic

Static logic has certain disadvantages, which include high power consumption and low switching speed. To solve these issues, dynamic logic was developed, which consists of a single clock.

When the clock is low, the evaluation nFET will turn off and the pre-charge pFET will turn on. The output node is charged to V_{dd}, whereas the rest of the nodes charge to V_{dd}-V_{th}, depending on the input values.

When the clock goes high, the evaluation nFET will turn on and the pre-charge pFET turns off. The output node discharges if the inputs are configured to conduct to ground.

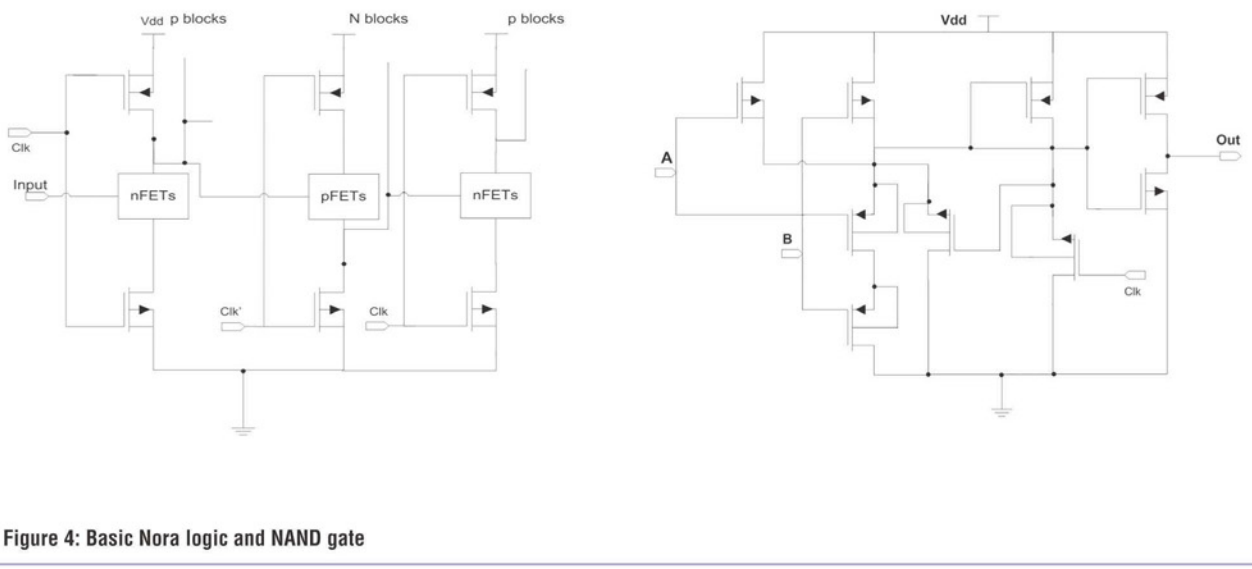


Figure 4: Basic Nora logic and NAND gate

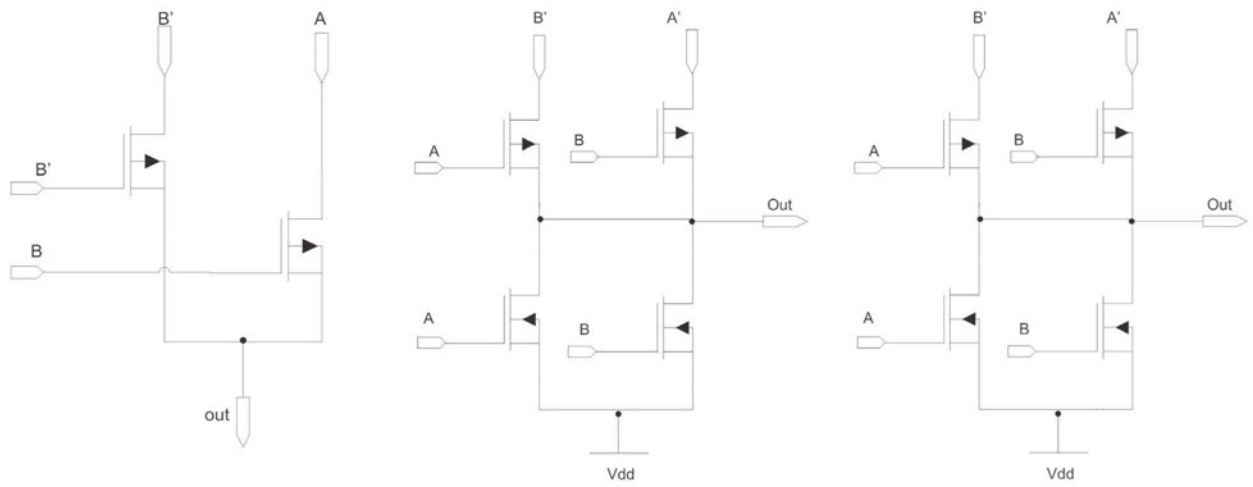


Figure 5: CPL, DPL and DVL NAND gates

Domino Logic

When the clock goes low, the dynamic node will be high and its output low. The nFETs in the next cascaded logic block will be turned off.

When the clock goes high, the dynamic node will discharge and its output will go high. Since discharging happens once, the output can make only one low-to-high transition; thus, many cascaded gates can evaluate in one evaluation cycle (see Figure 3).

NORA Logic

It is possible to make logic that 'pre-charges' to low and 'discharges' to high, by turning the dynamic gate 'upside down' and using pFETs.

To eliminate the 'racing problem' in nFETs, an alternating sequence of regular nFETs is used, which excludes the inverter present in the domino logic.

The NORA logic (the NP domino logic) is very vulnerable to noise, as information is dynamically stored during the evaluation phase. NAND gate topology using this logic is shown in Figure 4.

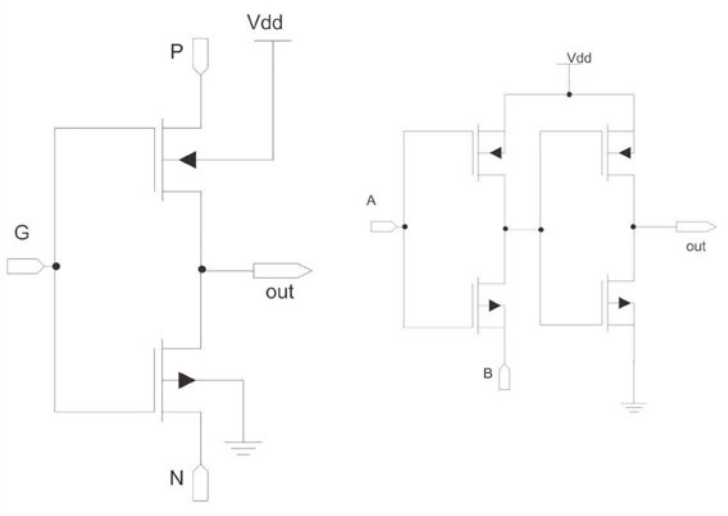


Figure 6: Basic GDI logic and its NAND gate

Pass Transistor Logic

PTL has two main circuit styles: one uses only NMOS circuits like CPL (complementary pass transistor logic), and the other uses both PMOS and NMOS circuits, like DVL (dual value logic) and DPL (double pass-transistor logic).

CPL has complementary inputs and outputs, a CMOS output inverter and an NMOS pass-transistor network. The circuit consists of pull-up and pull-down networks.

CPL has been applied to building blocks of arithmetic circuits, due to a reduced transistor count and small input capacitance.

The basic NAND gate topology implemented with CPL is shown in Figure 5.

To maintain noise margins in CPL, twin PMOS transistor branches are added to an N-tree in DPL, resulting in high input capacitance. The full swing operation of the circuit improves performance at reduced input voltage with limited scaling of the threshold voltage.

However, the main drawback of DPL is its redundancy. To overcome this, new logic called DVL has been introduced using DPL. It conserves the full swing operation of DPL with reduced transistor count.

DVL circuits are derived from DPL circuits using three steps:

- Eliminating redundant branches;
- Selecting faster halves;
- Signal resize.

Technology	Static	Domino	Nora	Gdi	Dvl	Dpl	Cpl
90nm	4	4	9	4	4	4	2
130nm	4	4	9	4	4	4	2
180nm	4	4	9	4	4	4	2

Table 1: Transistor count

Technology	Static	Domino	Nora	Gdi	Dvl	Dpl	Cpl
90nm	12.19	6.35	448.5	4.929	1274	7520	7200
130nm	11.47	50.75E-9	72.09	3.823	232.7	2496	776.7
180nm	2.636	953.7E-9	48.07	2.624	350	1383	87.3E-9

Table 2: The power trend (in mW)

Technology	Static	Domino	Nora	Gdi	Dvl	Dpl	Cpl
90nm	91.75	53.96	136.54	50.37	60.05	66.45	36.46
130nm	92.79	55.02	136.9	81.16	62.92	79.26	55.61
180nm	96.54	56.11	137.19	115.42	75.35	81.42	57.2

Table 3: The area trend (in μm^2)

Technology	Static	Domino	Nora	Gdi	Dvl	Dpl	Cpl
90nm	131.2e-9	287.1e-15	1.67e-6	96.72e-6	5.42e-6	12.18e-9	40
130nm	78.4e-3	9.47e-6	2.87e-3	313.4e-6	9.442e-6	746.5e-9	25
180nm	23.0	16.12e-6	5.77e-3	29.96e-3	12.34e-6	87.6e-6	25

Table 4: Corresponding delays (in µs) for each logic implementation and process technology

Technology	Static	Domino	Nora	Gdi	Dvl	Dpl	Cpl
90nm	1.599e-15	1.82e-21	7.47e-13	4.77e-13	6.9e-12	9.15e-14	2.88e-4
130nm	8.99e-10	2.38e-23	2.07e-10	1.2e-12	2.19e-12	1.86e-12	1.94e-5
180nm	6.06e-8	5.84e-21	2.77e-10	7.86e-11	4.69e-13	1.2e-10	2.18e-15

Table 5: The power delay product (PDP) trend (in watt/m^2)

Gate Diffusion Input Technique

Delay, area and power dissipation are the basic issues in cell design. In low-power applications, optimizations of power and speed are a significant problem, so using the gate diffusion input (GDI) technique helps (see Figure 12).

At first, the basic GDI cell looks like a standard CMOS inverter, but there are some significant differences:

- The GDI cell contains three inputs: G (gate input of pMOS and nMOS), P (input to drain/source of pMOS) and N (input to the drain/source of nMOS).
- Both pMOS and nMOS bulks are connected to P or N, so it can be biased (in contrast to a CMOS inverter).

The implementation of a GDI NAND gate is shown in Table 6.

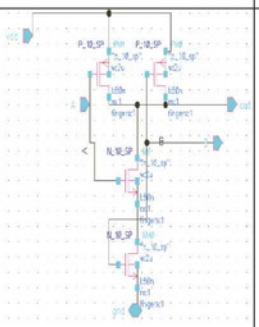
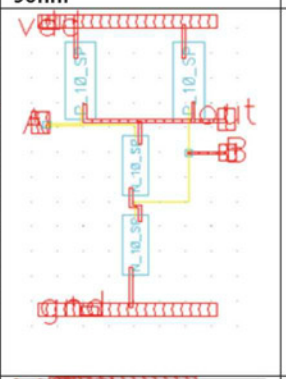
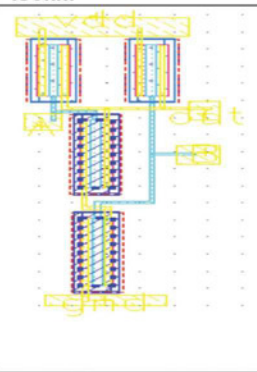
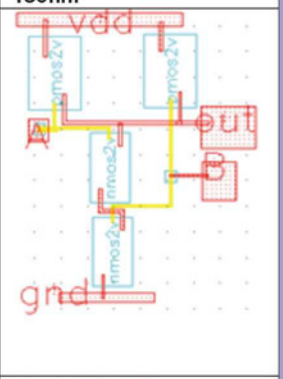
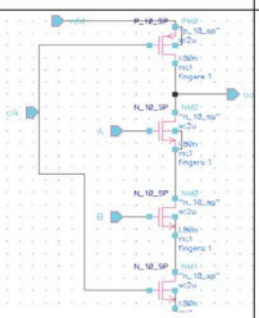
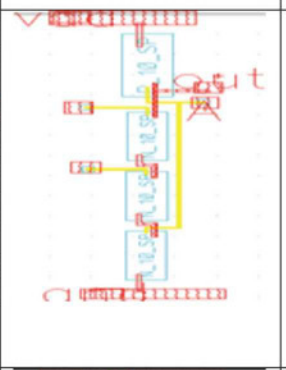
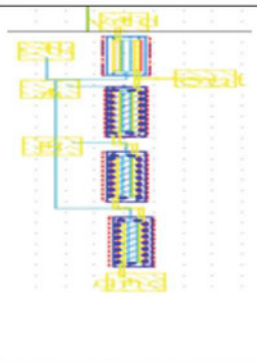
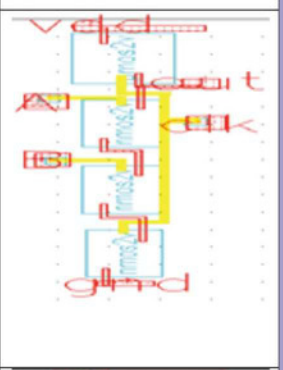
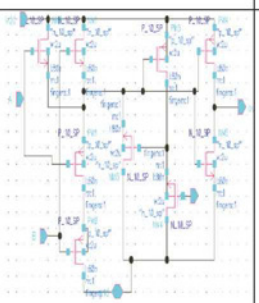
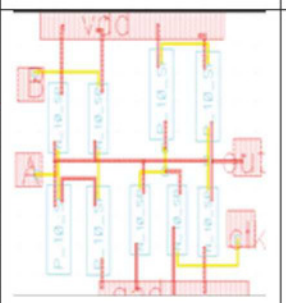
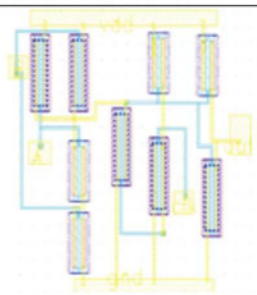
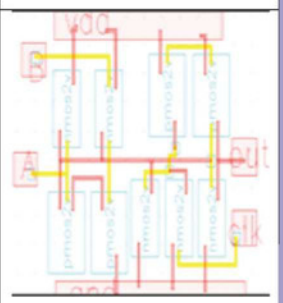
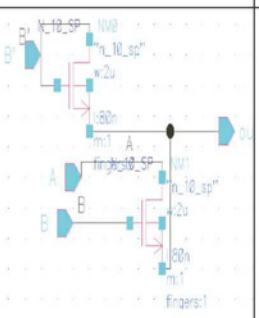
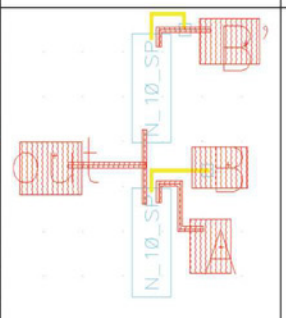
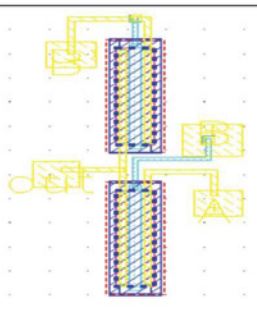
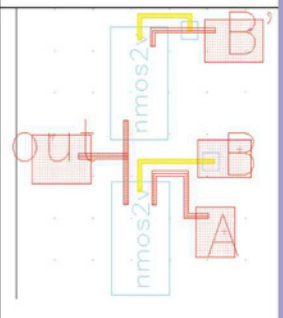
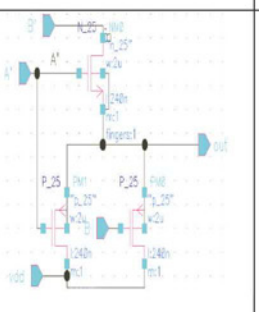
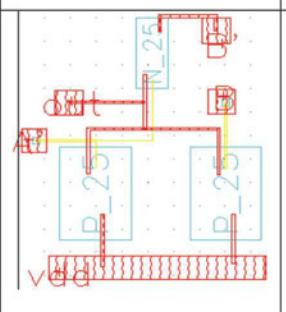
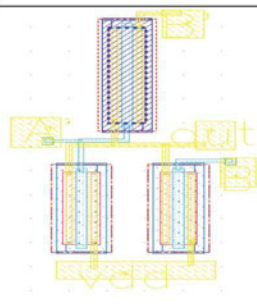
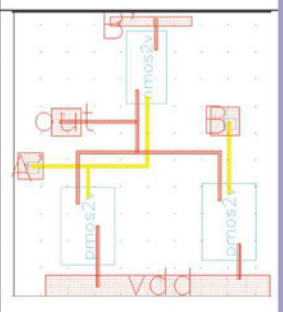
Simulation Results

Our team analyzed the performance of a NAND gate using static, dynamic, PTL and GDI techniques for three different CMOS process technologies: 1P-9M low-K UMC 90nm, 1P-8M LP TSMC 130nm and 1P-6M LP TSMC 180nm. The schematic and layout implementations were carried out using Cadence IC615.

The goal of these post-layout simulations is to report the effective area, power consumption, transistor count, signal delay and power delay product (PDP) performance trends within a single CMOS process technology using different logic, and in the different CMOS process technologies using different logic.

For all seven logic circuits the number of inputs remained the same, so total energy consumption and switching capacitance are determined by using the total inputs and outputs.

The transistor count varies in all seven cases (see Table 1). CPL logic utilizes the smallest number of transistors among all the logic styles. The NORA logic uses the most transistors; the rest of the five logic versions use four transistors each. However, as we will see in the results, the transistor count may not directly translate into the effective area of the implemented logic style.

Logics	Schematic	Layouts		
		90nm	130nm	180nm
STATIC				
DOMINO				
NORA				
CPL				
DVL				

Power Dissipation

Power dissipation is defined as the average value of power dissipations of all possible combinations of inputs of the CMOS circuit. For a 2-input NAND gate, there are four possible input combinations, hence the power dissipation will be an average of of all four.

The dissipated power is calculated by simulating the circuits for seven logics as discussed earlier; see Table 2. Minimum power is consumed by the domino logic when implemented in 1P-8M LP TSMC 130nm CMOS process technology. The most power is consumed by the DPL logic when implemented in 1P-9M low-K UMC 90nm CMOS process technology. Domino logic outperforms all others when it comes to power, even when implemented in all three CMOS process technologies.

Chip Area

For all seven logic circuits the number of inputs remains the same, but the transistor count varies, hence the device area is affected.

Similarly, with smaller CMOS technology the area is also reduced.

In Table 3 are the corresponding areas of these logic circuits with respect to various technologies. CPL logic requires the smallest area when implemented in 1P-9M low-K UMC 90nm CMOS process technology, whilst NORA logic needs the largest area when implemented in all three CMOS process technologies.

Delay

A switched-on transistor encounters a delay caused by the charging of junction capacitance; when turned off, the same capacitance is discharged causing a delay in total circuit's response.

With smaller CMOS feature sizes, the area is also reduced, resulting in reduced parasitic capacitance and delay, thus improving speed.

Table 4 shows the corresponding delays of these logic implementations for each technology. Domino logic has the smallest delay during the operation of a NAND gate when implemented in 1P-9M low-K UMC 90nm CMOS, whereas CPL logic has the highest delay when implemented in all three technologies.

Power Delay Product

Power delay product, also known as switching energy, is a figure of merit related to the logic gate's energy efficiency. It is a product of the input-output delay-time's power consumption.

Table 5 shows the corresponding PDP of the various logic implementations for the different CMOS process technologies. Domino logic has the smallest PDP when implemented in all three CMOS technologies, whilst CPL has the largest when implemented in 90nm and 130nm technologies. ●

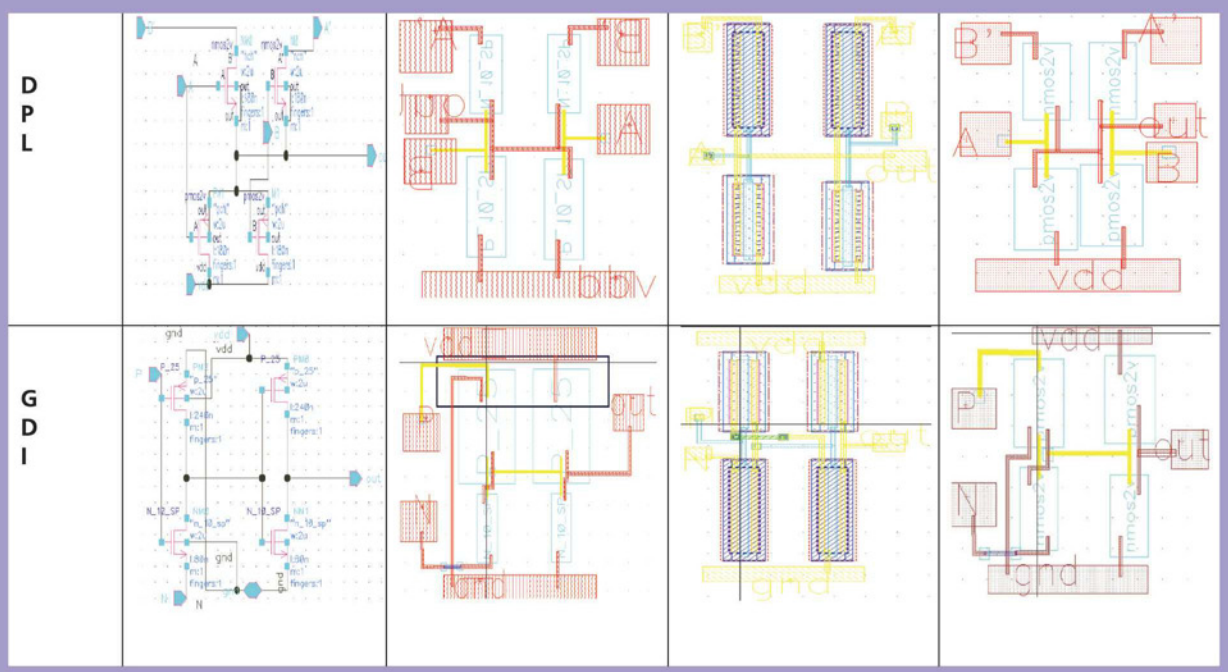


Table 6: Logic schematics and their layouts

SINGLE CCII-BASED FIRST-ORDER CURRENT-MODE ALL-PASS FILTER

FIRAT YUCEL OF AKDENIZ UNIVERSITY AND **ERKAN YUCE** OF PAMUKKALE UNIVERSITY, BOTH IN TURKEY,
PRESENT A CURRENT-MODE FIRST-ORDER ALL-PASS FILTER CONSISTING OF ONLY TWO GROUNDED RESISTORS AND A FLOATING CAPACITOR, WHICH DISSIPATES VERY LOW POWER

All-pass filters (APFs) are widely used in modern communications and instrumentation systems to change the phase of electrical signals whilst keeping their amplitudes constant at all frequencies. APFs were previously built with operational amplifiers (op-amps), but these have some drawbacks, such as slew-rate limitations. Second-generation current conveyors (CCIIs) as current-mode (CM) active devices were then used in building APFs because CM active elements offer advantages such as wider bandwidth, greater linearity and larger dynamic range over op-amps.

A CM first-order APF employing only two grounded resistors, a floating capacitor and a minus-type CCII (CCII-) is discussed in this article.

Circuit Description

The block diagram of the CCII- device with three terminals is shown in Figure 1. It can also be represented by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} \beta & 0 \\ 0 & 0 \\ 0 & -\alpha \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \end{bmatrix} \quad (1)$$

where α and β are the frequency-dependent non-ideal current and voltage gains respectively, and both ideally equal one. At sufficiently low frequencies, α and β can also be $\alpha = 1 - \varepsilon_\alpha$ ($|\varepsilon_\alpha| << 1$) and $\beta = 1 - \varepsilon_\beta$ ($|\varepsilon_\beta| << 1$) in which ε_α and ε_β are the current- and voltage-tracking errors and are ideally zero.

The internal structure of the CCII- shown in Figure 2, built by E. Bruun, is used in simulations of the proposed APF. It is assumed that all the MOS transistors are operated in their saturation regions. Bulks of all the MOS transistors are connected to the relevant sources to prevent any body effects.

The Proposed First-Order APF

Figure 3 shows the suggested CM first-order APF, which consists of only one CCII-, two grounded resistors and a floating capacitor.

The transfer function (TF) of the APF in Figure 3 with $R_1 = R_2 = R$ can ideally be written as:

$$\frac{I_{out}}{I_{in}} = -\frac{1 - sCR}{1 + sCR} \quad (2)$$

Here, the phase response is evaluated as:

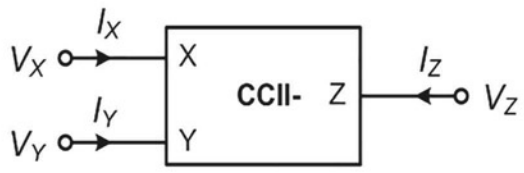


Figure 1: Block diagram of the CCII-

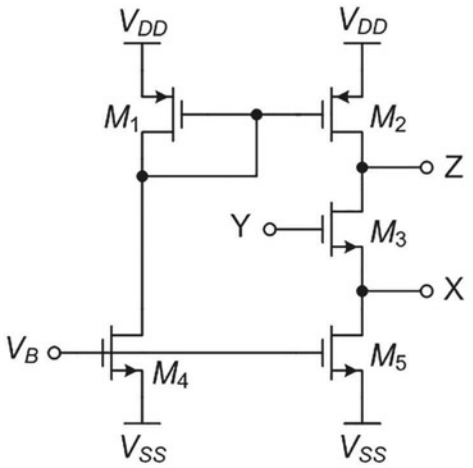


Figure 2: The internal structure of the CCII-

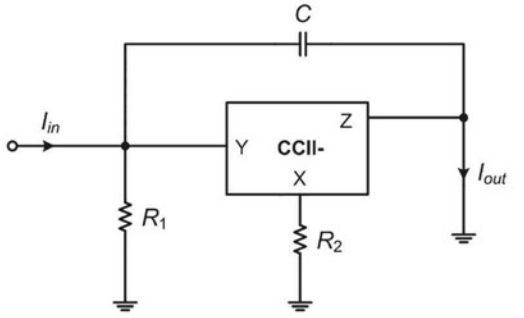


Figure 3: Proposed first-order CM APF circuit

$$\varphi(\omega) = \pi - 2\tan^{-1}(\omega CR) \quad (3)$$

where the phase changes from 180° to 0° as the frequency varies from zero to infinity. In Figure 3, if an RC-CR transformation is achieved, the CM APF employing s single floating resistor and two grounded capacitors has the following TF:

$$\frac{I_{out}}{I_{in}} = \frac{1 - sCR}{1 + sCR} \quad (4)$$

In Equation 4, the phase response is determined as:

$$\varphi(\omega) = -2\tan^{-1}(\omega CR) \quad (5)$$

where the phase changes from 0° to -180° as the frequency varies from zero to infinity.

A straightforward analysis of the APF in Figure 3 with non-ideal gains gives the following TF:

$$\frac{I_{out}}{I_{in}} = -\frac{\alpha\beta\frac{R_1}{R_2} - sCR_1}{1 + sCR_1} \quad (6)$$

Here, the phase response of the APF can also be obtained as:

$$\varphi(\omega) = \pi - \tan^{-1}\frac{\omega CR_2}{\alpha\beta} - \tan^{-1}\omega CR_1 \quad (7)$$

Results

Simulations of the proposed APF were undertaken using the SPICE program. The proposed APF in Figure 3 is simulated using 0.13µm IBM CMOS technology parameters. Symmetrical DC power supply voltages are chosen as $V_{DD} = -V_{SS} = 0.75V$. The bias voltage V_B in Figure 2 is chosen to be -0.16V.

The aspect ratios (W/L) of the MOS transistors in Figure 2 are given in Table 1. The parasitic resistor of the CCII- X terminal is 187Ω and the value of L_X is very small. The passive components of the CM APF in Figure 3 are selected as $R_1 = 1k\Omega$, $R_2 = 1k\Omega$ (the effects of R_X are included) and C = 100pF, which results in a pole frequency of $f_o \cong 1.59MHz$.

TRANSISTOR TYPE	W / L
NMOS transistors	13µm/0.52µm
PMOS transistors	1.3µm/0.52µm

Table 1: Aspect ratios of the MOS transistors

The gain and phase responses of the proposed CM APF are shown in Figure 4. Sinusoidal input signals with peak value of 100µA at frequencies of 100kHz, 500kHz, 1MHz, 10MHz and 100MHz are separately applied to determine the time-domain performance. The inputs and their corresponding outputs are given in Figures 5 to 9. It can be seen that the outputs of the CM APF have some offset currents which arise from the non-idealities of the CCII- MOS transistors.

A sinusoidal input current with a peak value of 100µA at the frequency of 1.59MHz is applied to the CM APF. Also, the widths of only the M_3, M_4 and M_5 transistors with step of 0.13µm are varied between 11.7µm and 14.3µm. The input and output currents of the CM APF circuit are shown in Figure 10, where it can also be seen that these variations of the parameter W affect the offset currents of the CM APF.

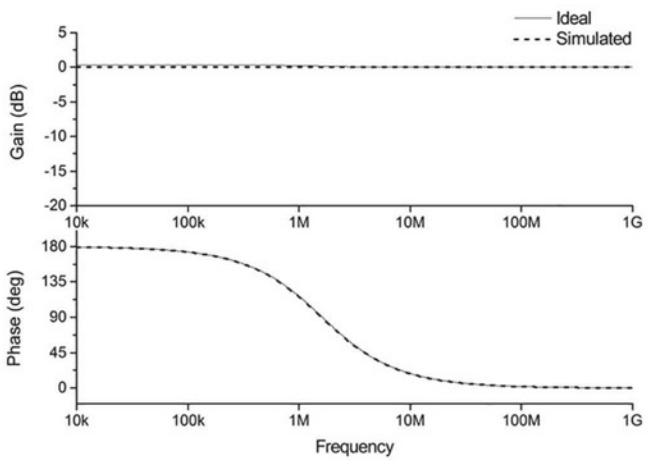


Figure 4: Gain and phase response of the suggested APF circuit

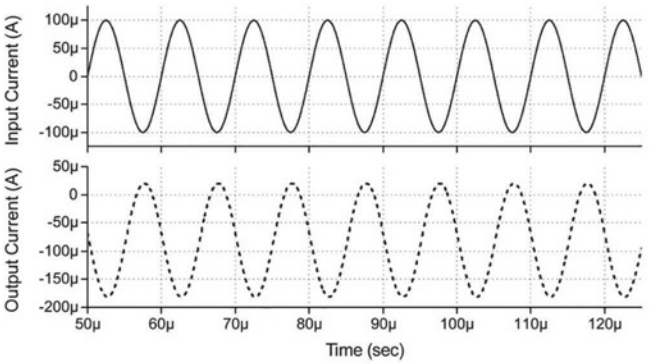


Figure 5: Input and output of the suggested APF at 100kHz

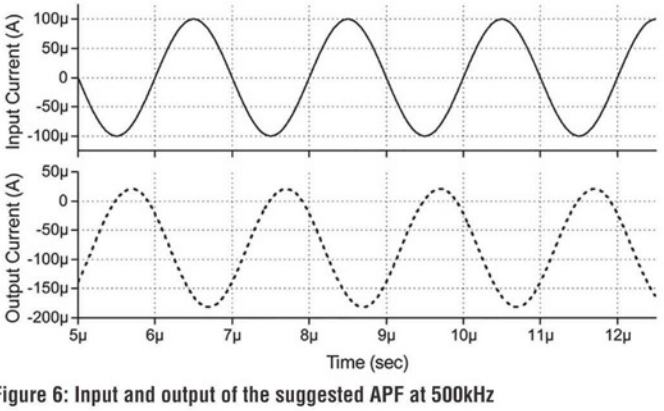


Figure 6: Input and output of the suggested APF at 500kHz

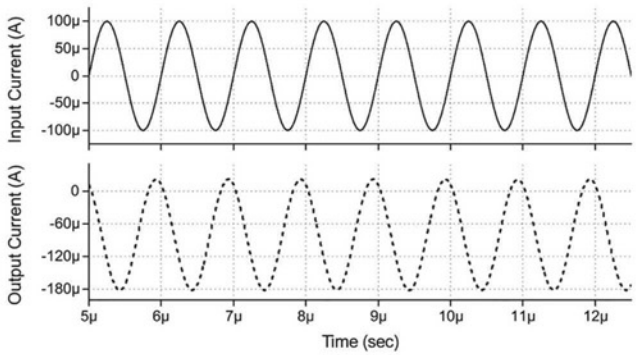


Figure 7: Input and output of the proposed APF at 1MHz

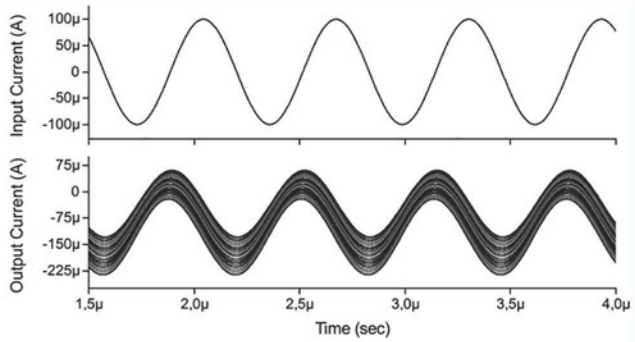


Figure 10: Analysis of the proposed APF by changing W of the transistors M_3, M_4 and M_5

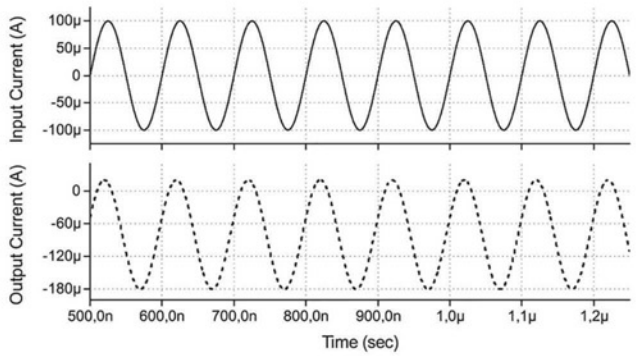


Figure 8: Input and output of the proposed APF at 10MHz

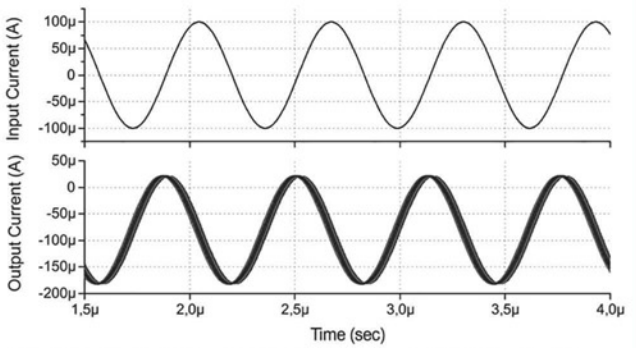


Figure 11: Monte Carlo analysis of the suggested APF circuit with changing values of C

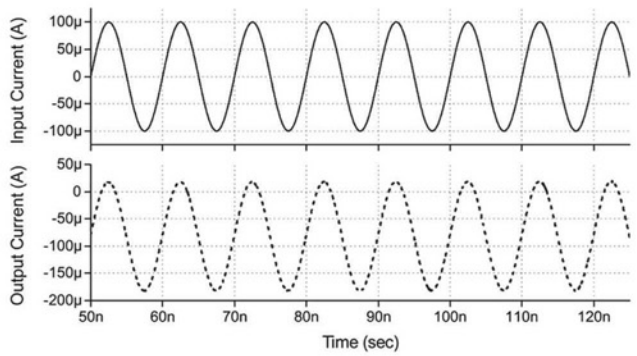


Figure 9: Input and output of the proposed APF at 100MHz

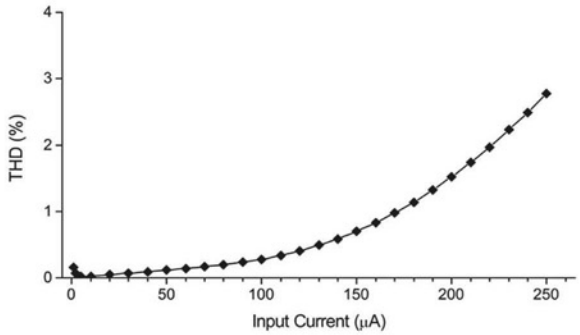


Figure 12: THD versus peak value of the applied sinusoidal signal for the suggested APF

A Monte Carlo analysis is performed with fifty runs for variations of 20% of the capacitance C in the CM APF, to which a sinusoidal input current with peak value of 100µA at 1.59MHz is applied. The input and output currents are shown in Figure 11, where it can be seen that a change in capacitor values varies with CM APF's resonance frequency.

Total power dissipation of the CM APF is calculated as 0.77mW; total harmonic distortion (THD) variations with respect to the peak value of the applied sinusoidal current at 1.59MHz are shown in Figure 12.

Conclusion

CM first-order APF using only two grounded resistors, a floating capacitor and a single CCII- which consumes low power. Nevertheless, it needs a single matching constraint. Also, it does not have low input and high output impedances.

A number of time-domain and frequency-domain simulations were performed to verify the theory. There is a small discrepancy between the ideal and the simulations, which can be attributed to the non-idealities of the CCII-, such as the frequency-dependent non-ideal gain and parasitic impedances. ●

LOW-VOLTAGE LOW-POWER LOW-COST CURRENT MODE LNA

MINGLIN MA, XIANGLIANG JIN, YUAN CHEN, CHENGWEI LI AND **ZHIJUN LI** FROM XIANGTAN UNIVERSITY IN CHINA PRESENT A LOW-VOLTAGE, LOW-POWER AND LOW-COST CURRENT-MODE DIFFERENTIAL LOW NOISE AMPLIFIER, OPERATING AT 2.4GHZ, BASED ON A STANDARD TSMC 0.18μM RF CMOS PROCESS

The rapid growth of portable RF-communications systems has led to the demand for single-chip solutions, which also have to feature small size, high integration and low cost.

To meet the circuit demands for speed and good power dissipation, CMOS has been the technology of choice.

RF Front-End

In a typical receiver system, the low noise amplifier (LNA) is the first active stage in an RF front-end, followed by a variable gain amplifier. However, there are many tradeoffs involved in designing the LNA, such as good noise factor (NF), linearity, gain and impedance matching, in addition to the expected low cost and low power dissipation.

An RF front-end has several stages, each designed with the voltage-mode approach that typically uses current-to-voltage and voltage-to-current converters. With all these converters onboard, the single chip requires a large chip area. In addition, owing to the existence of high-impedance nodes, these voltage-mode circuits have many drawbacks, such as limited bandwidth and high supply voltage.

The current mode approach has several advantages, including extended bandwidth, high linearity, ease of operations such as adding, subtracting and multiplying signals, a simple circuit

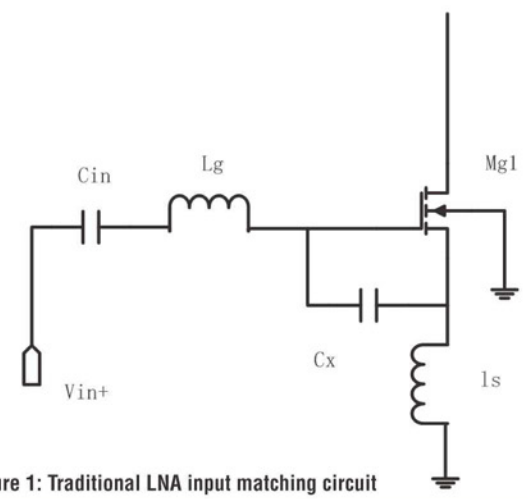


Figure 1: Traditional LNA input matching circuit

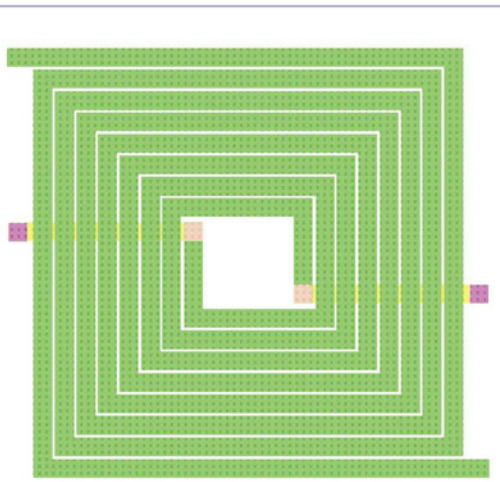


Figure 2: The transformer used in this project

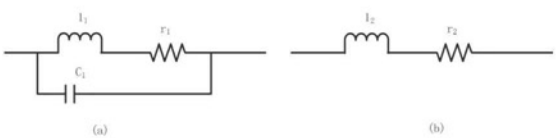


Figure 3: Parallel LC network and its equivalent circuit

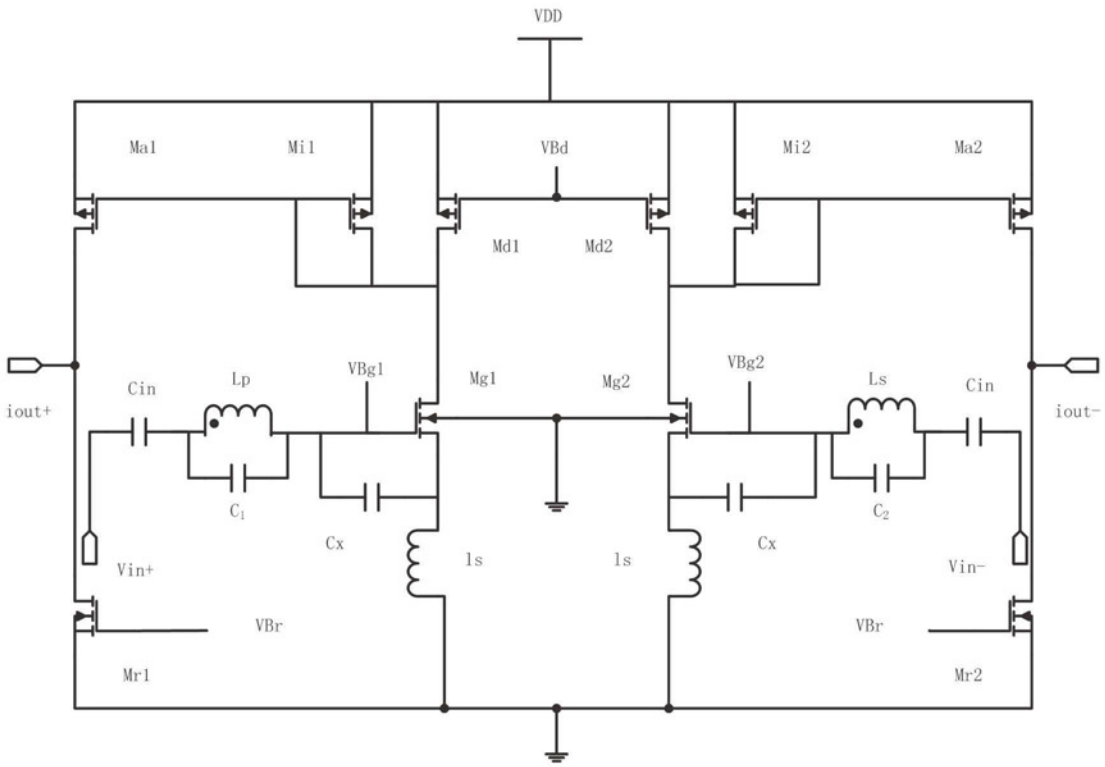


Figure 4: A complete current-mode differential LNA

structure, high dynamic range, suitability for use in reduced power supply environments, low voltage operation and so on.

Over the past few years, many have proposed current-mode RF receivers with performance improvements over voltage-mode circuits.

LNA Design

The requirements set for the LNA input stage are: source impedance matching, minimum noise contribution and maximum transconductance gain. Furthermore, the IIP_3 of the LNA should be maximized.

Conventionally, the inductively degenerated NMOS input stage, consisting of C_{in}, L_s, C_x, M_g and L_g, allows us to achieve the minimum noise figure, matched input impedance and maximum transconductance gain; this circuit is shown in Figure 1.

The conditions for input impedance matching and the expression for the resonant frequency are summarized in Equation 1:

$$Z_{in}(s) = \frac{1}{sC_{gs}'} + s(L_g + L_s) + \frac{g_m}{C_{gs}'}L_s \quad (1)$$

where:

$$C_{gs}' = C_{gs} + C_x \quad (2)$$

L_s (source inductance) and L_g (gate inductance) together with the capacitances C_{gs} and C_x form an impedance-matching network used to produce the 50-ohm resistance. The gate inductance is used to set the resonance once L_s is chosen to satisfy the criterion for a 50-ohm pure resistance. To reduce the gate inductance L_g, a capacitance C_x is introduced in parallel to the gate capacitance of the differential amplifying transistor. If the capacitance is too large, the quality factor of the input stage will be too small. We can also increase the input transistor's width, however this will result in a larger drain current (corresponding to larger power consumption).

In order to reduce the gate inductance, we use a transformer (composed of L_p and L_s) instead of two single inductors. Two capacitances ($C_{1,2}$) are also added in parallel to the primary coil (L_p) and the second coil (L_s) of this transformer; see Figure 2.

This type of transformer ensures that the electrical characteristics of the primary and secondary coils are identical when they have the same number of turns, through the use of identical windings. The transformer's terminals are also positioned on opposite sides of the physical layout, facilitating connections to other circuitry.

In realizing an effective inductance, the transformer takes advantage of the mutual coupling between its windings, and as a consequence exhibits lower series resistance and shunt capacitance and occupies a smaller die area compared with two equivalent, separate inductors.

The self-inductances (l_p and l_s) of the transformer's primary

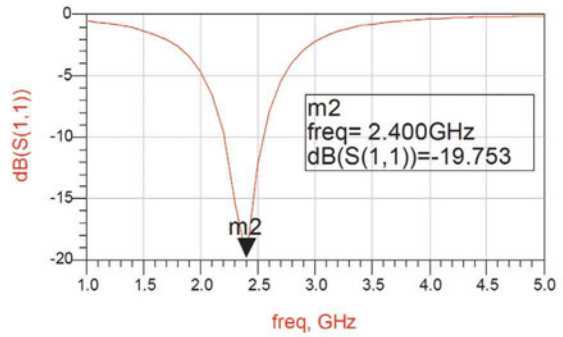


Figure 5: Simulated S_{11} result

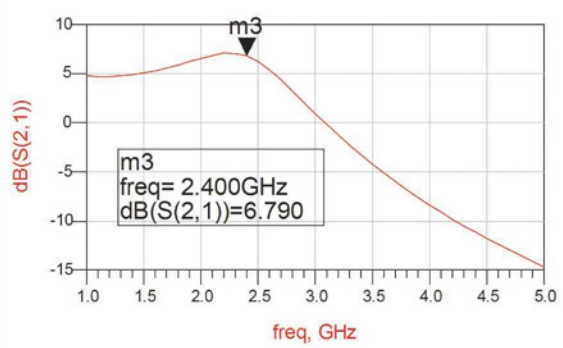


Figure 6: Simulated gain of our LNA

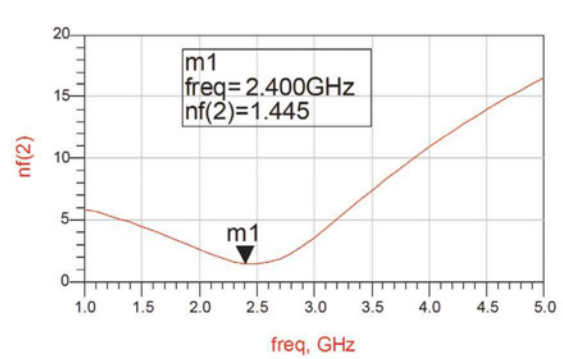


Figure 7: Simulated NF of our LNA

and secondary parts, with a typical k factor of 0.8, are 3nH, resulting in two 5.4nH equivalent inductors:

$$lp = ls = 3nH \tag{3}$$

$$k = 0.8 \tag{4}$$

$$l_1 = l_0(1+k) = 5.4nH \tag{5}$$

The l_1c_1 parallel network, shown in Figure 3a, is equivalent to an ideal inductor l_2 in series with a resistance r_2, shown in Figure 3b. We use r_1 to represent the parasitic resistance of the transformer coils.

For this project we need an inductor (L_g) of 7.4nH:

$$l_2 = 7.4nH \tag{6}$$

We can represent the impedance of the l_1c_1 parallel network with z:

$$z = \frac{(r + j\omega l_1)\frac{1}{j\omega c_1}}{r + j\omega l_1 + \frac{1}{j\omega c_1}} \approx \frac{l_1/c_1}{r + j(\omega l_1 - \frac{1}{\omega c_1})} \tag{7}$$

Assuming:

$$X = \omega l_1 - \frac{1}{\omega c_1} \tag{8}$$

then:

$$z = \frac{l_1/c_1}{r + jX} = \frac{l_1(r - jX)}{c_1(r^2 + X^2)} = \frac{l_1 r}{c_1(r^2 + X^2)} - j\frac{l_1 X}{c_1(r^2 + X^2)} \tag{9}$$

So,

$$-j\frac{l_1 X}{c_1(r^2 + X^2)} = j\omega l_2 \tag{10}$$

We get:

$$c_1 = 0.22pF \tag{11}$$

The signal received from the antenna is voltage, while the current-mode LNA will be used in the current-mode RF receiver and the input of the following mixer should be current. So, we can use current mirrors to process the currents generated by the LNA, instead of current-to-voltage and voltage-to-current converters.

In this project, current mirrors are M_{i1}, M_{a1} and M_{i2}, M_{a2}. In the transconductance stage, M_{g1} and M_{g2} are biased to operate in a linear region. Transistors $M_{i1\text{-}2}$ and $M_{a1\text{-}2}$ operate as current mirrors rather than as a transconductance amplifier, so they are not operating in a linear region.

Avoiding mirroring the direct components of transconductance stage, the bypass transistors M_{d1} and M_{d2} are connected in parallel with a controlling side of the two current mirrors. At the same time, two bypass transistors, M_{r1} and M_{r2}, are connected so the direct current component of the LNA output stage will not flow into the next stage, the current mode mixer.

Simulation Results

This LNA was simulated in 0.18µm RF CMOS technology. The RF signal is injected into the LNA input via a 1:1 balun, used to convert the single-ended signal provided by the RF signal source into a differential signal. Figure 5 shows the plot of simulated S_{11} in the range 1-5GHz. At 2.4GHz S_{11} is less than -19dB, which proves the effectiveness of the narrowband input matching realized by this modified inductively-degenerated input stage.

Figure 6 shows the voltage-conversion gain, simulated with a low-impedance load, instead of the high-impedance load in voltage-mode circuits. The peak gain is 6.79 dB at 2.4GHz, which is enough in current-mode circuits. Figure 7 shows the minimum NF is 1.455dB at 2.4GHz. Due to the high linearity of the current-mode approach, the IIP_3 simulated at 2.4GHz is 7dBm. The LNA consumes a total of 5mW for a 1V supply.

The comparison of this LNA with the published literature is summarized in Table 1. Its advantages of low power consumption, low noise figure, high linearity, low cost, less passive components and simple structure can easily be seen. ●

Parameters	This work	[7]	[3]	[5]	[13]
Frequency (GHz)	2.4	2.4	2.2	1.8	2.47
S_{11} (dB)	-19.753	-26.47	< -13	< -20	-10.62
S_{21} (dB)	6.79	12.63	10	8.26	18.9
NF (dB)	1.445	1.47	1.87	1.97	2.0
supply (V)	1	1.2	1.8	1.0	1.5
Power (mW)	5	6.49	16.2	1.36	6.45
IIP_3 (dBm)	7	--	-2.0	1.77	2.42
topology	differential current mode	differential current mode	differential voltage mode	single-ended current mode	differential voltage mode
CMOS process	0.18μm	0.18μm	0.35μm	0.18μm	0.18μm
inductor	2 inductors and a transformer	8	6	4	6

Table 1: Performance comparison

[3] Fan X, zhang H. *A noise reduction and linearity improement technique for a differential cascode LNA. IEEE Journal of Solid-state Circuits*, 2008, 43(3): 588-599

[5] Lee L, Jamuar S S. *current-mode approach for a variable-gain low-noise amplifier, in 13th IEEE International Conference on Networks*. 2005. p. 4

[7] Kim H-S, Li X. *A 2.4GHz CMOS low noise amplifier using an inter-stage matching inductor. Circuits and Systems*, 1999: 1040-1043

[13] Alam S K, DeGroat J. *A 1.5-V 2.4 GHz Differential CMOS Low Noise Amplifier for Bluetooth and Wireless LAN Applications, in IEEE North-East Workshop on Circuits and System*. 2006. p. 13-16

SPECIAL OFFERS for full sales list check our website

www.stewart-of-reading.co.uk

Check out our website, 1,000's of items in stock

Used Equipment – **GUARANTEED**
All items supplied as tested in our Lab
Prices plus Carriage and VAT

IFR 2025	Signal Generator 9kHz - 2.51GHZ Opt 04/11	£1,250
Fluke/Philips PM3092	Oscilloscope 2+2 Channel 200MHZ Delay etc	£295
HP34401A	Digital Multimeter 6.5 digit	£325
Agilent E4407B	Spectrum Analyser 100HZ - 26.5GHZ	£5,000
HP3325A	Synthesised Function Generator	£195
HP3561A	Dynamic Signal Analyser	£650
HP3581A	Wave Analyser 15HZ - 50KHZ	£250
HP3585B	Spectrum Analyser 20HZ - 40MHZ	£1,500
HP53131A	Universal Counter 3GHZ	£600
HP5361B	Pulse/Microwave Counter 26.5GHZ	£1,250
HP54600B	Oscilloscope 100MHZ 20MS/S	from £125
HP54615B	Oscilloscope 2 Channel 500MHZ 1GS/S	£650
HP6032A	PSU 0-60V 0-50A 1000W	£750
HP6622A	PSU 0-20V 4A Twice or 0-50V 2A Twice	£350
HP6624A	PSU 4 Outputs	£350
HP6632B	PSU 0-20V 0-5A	£195
HP6644A	PSU 0-60V 3.5A	£400
HP6654A	PSU 0-60V 0-9A	£500
HP8341A	Synthesised Sweep Generator 10MHZ-20GHZ	£2,000
HP83731A	Synthesised Signal Generator 1-20GHZ	£2,500
HP8484A	Power Sensor 0.01-18GHZ 3nW-10uW	£125
HP8560A	Spectrum Analyser Synthesised 50HZ - 2.9GHZ	£1,950
HP8560E	Spectrum Analyser Synthesised 30HZ - 2.9GHZ	£2,400
HP8563A	Spectrum Analyser Synthesised 9KHZ-22GHZ	£2,750
HP8566B	Spectrum Analsyer 100HZ-22GHZ	£1,600
HP8662A	RF Generator 10KHZ - 1280MHZ	£1,000
HP8970B	Noise Figure Meter	£750
HP33120A	Function Generator 100 microHZ-15MHZ - no moulding handle	£295
Marconi 2022E	Synthesised AM/FM Signal Generator 10KHZ-1.01GHZ	£325
Marconi 2024	Synthesised Signal Generator 9KHZ-2.4GHZ	£800
Marconi 2030	Synthesised Signal Generator 10KHZ-1.35GHZ	£750
Marconi 2305	Modulation Meter	£250
Marconi 2440	Counter 20GHZ	£295
Marconi 2945	Communications Test Set Various Options	£2,500
Marconi 2955	Radio Communications Test Set	£595
Marconi 2955A	Radio Communications Test Set	£725
Marconi 2955B	Radio Communications Test Set	£850
Marconi 6200	Microwave Test Set	£1,950
Marconi 6200A	Microwave Test Set 10MHZ-20GHZ	£2,500
Marconi 6200B	Microwave Test Set	£3,000
IFR 6204B	Microwave Test Set 40GHZ	£10,000
Marconi 6210	Reflection Analyser for 6200 Test Sets	£1,250
Marconi 6960B with	6910 Power Meter	£295
Marconi TF2167	RF Amplifier 50KHZ - 80MHZ 10W	£75
Tektronix TDS3012	Oscilloscope 2 Channel 100MHZ 1.25GS/S	£800
Tektronix 2430A	Oscilloscope Dual Trace 150MHZ 100MS/S	£350
Tektronix 2465B	Oscilloscope 4 Channel 400MHZ	£600
R&S APN62	Syn Function Generator 1HZ-260KHZ	£225
R&S DPSP	RF Step Attenuator 139dB	£300
R&S SMR40	Signal Generator 10MHZ - 40GHZ with Options	£13,000
Cirrus CL254	Sound Level Meter with Calibrator	£40
Farnell AP60/50	PSU 0-60V 0-50A 1KW Switch Mode	£195
Farnell H60/50	PSU 0-60V 0-50A	£500
Farnell B30/10	PSU 30V 10A Variable No Meters	£45
Farnell B30/20	PSU 30V 20A Variable No Meters	£75
Farnell XA35/2T	PSU 0-35V 0-2A Twice Digital	£75
Farnell LF1	Sine/sq Oscillator 10HZ-1MHZ	£45
Racal 1991	Counter/Timer 160MHZ 9 Digit	£150
Racal 2101	Counter 20GHZ LED	£295
Racal 9300	True RMS Millivoltmeter 5HZ-20MHZ etc	£45
Racal 9300B	As 9300	£75
Black Star Orion	Colour Bar Generator RGB & Video	£30
Black Star 1325	Counter Timer 1.3GHZ	£85
Ferrograph RTS2	Test Set	£50
Fluke 97	Scopemeter 2 Channel 50MHZ 25MS/S	£75
Fluke 99B	Scopemeter 2 Channel 100MHZ 5GS/S	£125
Fluke PM5420	TV Gen Multi Outputs	£600
Gould J3B	Sine/sq Oscillator 10HZ-100KHZ Low Distortion	£60
Gould OS250B	Oscillator Dual Trace 15MHZ	£50
Gigatronics 7100	Synthesised Signal Generator 10MHZ-20GHZ	£1,950
Panasonic VP7705A	Wow & Flutter Meter	£60
Panasonic VP8401B	TV Signal Generator Multi Outputs	£75
Pendulum CNT90	Timer Counter Analyser 20GHZ	£995
Seaward Nova	PAT Tester	£125
Solartron 7150	6 1/2 Digit DMM True RMS IEEE	£65
Solartron 7150 Plus	as 7150 plus Temp Measurement	£75
Solatron 7075	DMM 7 1/2 Digit	£60
Solatron 1253	Gain Phase Analyser 1mHZ-20KHZ	£750
Tasakago TM035-2	PSU 0-35V 0-2A 2 Meters	£30
Thurlby PL320	PSU 0-30V 0-2A Digital	£50
Thurlby TG210	Function Generator 0.002-2MHZ TTL etc Kenwood Badged	£65
Wavetek 296	Synthesised Function Generator 2 Channel 50MHZ	£450

STEWART OF READING
17A King Street, Mortimer, Near Reading, RG7 3RS
Telephone: 0118 933 1111• Fax: 0118 933 2375
9am – 5pm, Monday – Friday
Please check availability before ordering or **CALLING IN**

NORTHERN 15 Manufacturing & Electronics

EventCity | Manchester | M17 8AS

Wed 30th Sept - Thurs 1st Oct 2015

www.industrynorth.co.uk

Northern Manufacturing & Electronics returns to Manchester

Northern Manufacturing & Electronics, the free-to-attend industrial technology and electronics show, returns to EventCity, Manchester from September 30th to October 1st 2015. Taking a look at the impressive exhibitor list lined up for this year's event, visitors appear to be set for another hectic two days.

Now in its third year, the show is the partner event into the well-established Southern Electronics show, focusing mainly on the Northern and Western regions of the UK. With the electronics industry such a key activity within the show's catchment area, it's no surprise to learn that components and electronics subcontracting have been high priorities for visitors to previous events. This year will be no different. With around 250 businesses expected to take part, Northern Manufacturing & Electronics 2015 promises to be an extremely worthwhile event for electronics professional across the North.

Following hard on the heels of its famously successful southern sibling, Northern Manufacturing & Electronics show has very quickly established itself as a key event for the electronics business in the North. The number and variety of electronics vendors participating this year creates a particularly broad appeal and enables visitors to tackle a number of production issues in a single visit. Within a single show it's possible to meet PCB makers, component distributors, enclosure specialists, CEMS, test equipment manufacturers, designers and all manner of business support specialists such as finance and IP protection. This chance to address multiple issues with great efficiency is one of the show's best features. Its location close to the centre of Manchester means it is very accessible by train, tram or bus, road or air putting it in easy reach of a substantial swathe of electronics firms all around the North, Scotland, Wales, Northern Ireland and Eire.

A brand name element that is new Northern Manufacturing 2015, RoadRailAir, will focus on the region's significant supply chain strengths to the automotive, public transport and aerospace manufacturing sectors. The aerospace industry in the North West alone contributes over £7bn to the UK economy each year. But this is only one aspect of the North's highly dynamic manufacturing sector that includes the two fastest regions of high tech industrial growth in the UK.

As an important marketplace for components, Northern Manufacturing & Electronics is a fascinating showcase for design engineers. The array of products on show is immense; from sensors, data acquisition and optical electronics, through to discrete components, cable carriers and connectors. With its mixture of larger suppliers and smaller specialists, there is an excellent chance that whatever device or component you are looking for, you'll find it at Northern Manufacturing & Electronics. Over 40% of visitors at last year cited components as the number one reason for their visit.

A extensive representative slice of the UK Electronics sector, along with a large number of associated services and products from general industry, such as for example sheet metal working, enclosures, consumables and production equipment, gives the event a unparalleled profile and guarantees visitors an absorbing and worthwhile few hours at least.

Some of the notable firms confirmed for 2015 include LCL Electronics, Lemo, BAE Systems, European Circuits, Henkel, MagDev and PACE Europe. However, components are simply one aspect of a far larger exhibition which involves almost everything related to manufacturing industry. Robotics & automation, sensors, enclosures, test equipment, optical inspection, hand tools, storage and countless others will all be on show. Technology trails guide attendees around the event, allowing them to make the most effective use of time at the event.

Subcontract services highlighted include 3D printing, electronic assembly, laser cutting & marking, sub-contract manufacturing, cable making and fabrication. Northern 2015 also hosts many big-name machinery manufacturers such as Trumpf, Amada, Bystronic, Bruderer and Haas Automation giving live demonstrations for the two-day event.

The North West Aerospace Alliance (NWAA) is the key group for the aerospace manufacturing business into the North West, and its Chief Executive, Dr. David Bailey, will deliver one of many keynote sessions of the 2015 programme, entitled Technology Opportunities and Challenges into the Aerospace Supply Chain.

Wayne Kite of Stanford Marsh will provide a synopsis associated with the rising technology of 3D Printing, including case studies illustrating how it may be applied in almost unlimited situations in industry. Alistair Williamson of Lucid Innovation will investigate how additive manufacturing is literally forming the future of manufacturing across a wide selection of industries, from food & drink, to aerospace and medical technology.

Admission to Northern Manufacturing & Electronics 2015 is free to business visitors, and EventCity provides 3000 free on-site parking spaces, with easy accessibility by road or public transport. To register online for free tickets, visit **www.industrynorth.co.uk**

ECOC

28-30 September 2015
Feria Valencia, Spain
www.ecocexhibition.com

ECOC 2015
VALENCIA
CELEBRATING 20 YEARS OF THE ECOC EXHIBITION
28-30 September 2015, Feria Valencia, Spain

The ECOC Exhibition Celebrates 20 Years

The ECOC Exhibition, the largest European optical communications event, remains a crucial meeting place for the fibre optic communication technology industry. This year marks 20 years of the ECOC Exhibition; the event joined the conference in 1995 and since then the exhibition has become one of the must-attend events for the optical communications industry.

Over the past 20 years, the ECOC Exhibition travelled to 12 different countries and 17 different venues. The very first exhibition was held in Brussels in September 1995, opening its doors to approximately 100 visitors. Now, the show has more than 300 different exhibitors attracting over 5500 attendees, and it's the place to get your business on the fibre optic map.

The landmark 20th exhibition will be held at the Feria Valencia in Spain, between 28th and 30th September 2015. The spectacular venue will play host to a plethora of manufacturers, suppliers and service providers of optical communications to show their products, services and vision for the industry as well as network with the industry's top decision makers.

Free Market Focus Seminars

Free market focus seminars will be located in the exhibition hall, and running across the full three days. They are free to attend for visitors and exhibitors. There you will gain insight into the latest in the telecoms market and the latest hot topics.

One of the most popular feature areas of the exhibition, the FTTx Centre will provide unique opportunity to meet specialist suppliers, and watch live and interactive demonstrations of the latest FTTx technologies, including fibre optic network delivery methods and OSP and ISP for FTTx vendor independent products.

Learning New Skills

A series of short-course training sessions have been specifically designed to help participants tackle key techniques including modern fusion splicing and passive optical network testing. Led by CTTS, the first choice training provider for many system operators throughout Europe, these hands-on, practical sessions will take place in the CTTS Training Zone located on the exhibition floor.

REGISTER FOR THE ECOC EXHIBITION 2015
AND YOU COULD WIN A KINDLE FIRE!

VISITOR REGISTRATION FOR THE 2015 ECOC EXHIBITION
IS NOW OPEN.

Taking place from 28-30 September 2015 at the Feria Valencia in Spain, the show will once again provide an unrivalled opportunity for manufacturers, suppliers and service providers of optical communications products and services to come together to meet and network with top decision makers from across the industry.

The event provides the chance to network with over 5,500 colleagues from across the industry, get information from over 300 exhibitors as well as attend short course training programmes and market focus seminar sessions and see the latest interactive FTTx demonstrations.

The exhibition and all feature areas are free to attend, register for your free place today on **www.ecocexhibition.com**.

WIN A KINDLE FIRE!

The ECOC Exhibition organisers are offering the chance for one lucky pre-registered visitor who attends the show to win a Kindle Fire HD.

To participate in the competition, simply register online before 28th September 2015 and attend the show between 28-30 September when you will be entered into the prize draw. The lucky winner will be notified, and can claim the prize, on the ECOC site at the show in Spain in September.

Register for a free exhibition pass at **www.ecocexhibition.com http://nexus.circdata-solutions.co.uk/RFG/publish/ECOC15/?source=electronicsworld**

ECOC 2015
VALENCIA
CELEBRATING 20 YEARS OF THE ECOC EXHIBITION
28-30 September 2015, Feria Valencia, Spain

THE ECOC EXHIBITION

Bringing the World the Latest in Optical Communications

Network with over **5,600** industry colleagues and get information from over **300** exhibitors plus…

2015 MARKET FOCUS — Attend free business level seminars on the show floor

FTTx CENTRE — See the latest FTTx products and live demonstrations in 11 interactive zones

ctts Cable Telecommunications Training Services Ltd — Take part in practical short course training sessions

For full details and to register for your free exhibition pass please visit:

www.ecocexhibition.com

ALTIUM TO EXPAND ITS PORTFOLIO WITH NEW BUSINESS ACQUISITIONS

Altium is in the process of acquiring two industry-leading electronic parts content and search providers, Octopart and Ciiva. A definitive purchase agreement has been signed to acquire Octopart, a provider of electronic parts data and specialized inventory search. In addition, a finalized agreement has been signed to acquire Ciiva, a cloud-based electronic component management system that controls and tracks components throughout the product lifecycle management process. The acquisitions will enable Altium to expand its product lineup to include an integrated content strategy for enhanced component management workflows.

"The acquisitions of Octopart and Ciiva represent a significant step forward in the evolution of the Altium content strategy," said Aram Mirkazemi, CEO at Altium. "Tightly integrated CAD models and part supply information will bring a state change to the way parts selection and component management are performed during and after the design process is completed."

The acquisition of Octopart provides Altium with direct access to over 30 million electronic and industrial components, allowing Altium to expand its content offering. Altium customers will also benefit from an extensive supplier database network provided by Octopart, allowing designers to directly connect to the electronic component distributors and manufacturers.

www.altium.com

AWS ELECTRONICS GROUP INTRODUCES COMPANY-WIDE REAL-TIME OPERATIONAL CONTROL SYSTEM

AWS has developed and implemented an updated real-time control system at its manufacturing plants in the UK (Newcastle-under-Lyme) and Slovakia (Namestovo) to cover every aspect of its business at the two facilities. The £50,000 bespoke ERP system enables the company to monitor activities and provide immediate feedback to customers concerning their orders.

"We have had our ERP software in place for many years controlling and monitoring numerous activities within our business processes from receipt of orders through to despatch to customers. However, we have been working on our vision for full shopfloor control to supplement our current system for some while and we are now ready to enter the era of the Smart Factory – or Industry 4.0," said AWS's CEO Paul Deehan.

www.awselectronicsgroup.com

ROHM SEMICONDUCTOR RECEIVES "SUPPLIER OF THE YEAR 2014 AWARD"

ROHM Semiconductor has been recognized by the Continental Automotive Group for its Discrete and Standard ICs in the Electronics category with the "Supplier of the Year 2014 Award".

The highly renowned supplier prize, granted since 2008, rewards outstanding achievements in the production and delivery of products and services. In total, Continental awarded 15 companies, among them three electronic providers, out of 900 strategic suppliers.

ROHM received the award during the International Purchasing Manager Meeting in Dusseldorf by Dr Elmar Degenhart, Executive Chairman of the Board, Continental AG, and Günter Fella, Head of Purchasing at Continental Automotive.

www.rohm.com

NEW SIX-TERMINAL SIGNAL SPLITTER GIVES MORE FUNCTIONS IN A SINGLE CONNECTOR

Amphenol Industrial Products Group has introduced a signal splitter featuring six-terminal inputs to allow higher combinations of functions in a single connector and help reduce the number of connectors needed in an application.

The new splitter receives power and signal from one cable and splits it into two equal, yet separate, sets of power and signal as output, saving money and space whilst allowing additional functionality.

The Tru-Loc splitters are designed for use in CANbus networks: CAN-high, CAN-low, ground or shielded, I/O power, low amperage power distribution as well as sensor harnessing. They are manufactured from thermoplastic material and capable of operating in environments up to 150°C, and feature 120 Ohm ±10% of controlled impedance between two sets of contact pairs.

www.amphenol-industrial.com

AMETEK ADDS DC REGENERATIVE SINK OPTION CAPABILITY

AMETEK Programmable Power has added the ability to sink DC current to its California Instruments's RS and MX Series power sources.

The addition of this option to an RS or MX Series power source with AC Sink installed allows users to source and sink both AC and DC currents at up to 100% of the source's rated output power. When sinking current, the current is regenerated and returned to the electrical grid reducing the operating cost of electricity.

There are many applications for sinking AC current, such as the prevalent need to regenerate current back to the electrical grid while testing grid-tied inverters. A common DC sink application, among others, is to simulate batteries connected to a bidirectional converter in hybrid electric vehicle motor drive systems.

www.programmablepower.com

NEW EMBEDDED PROCESS DETECTOR FROM MOORTEC SEMICONDUCTOR

The New Moortec Embedded Process Detector (MEPD) circuit provides the means for advanced node Integrated Circuit (IC) developers to detect the process variations brought about by manufacturing variability and drift of advanced node core digital MOS devices. The Process Detector can be used to enable a continuous Dynamic Voltage & Frequency Scaling (DVFS) optimisation system, monitor manufacturing variations on and if required, across chip, gate delay measurements, critical path analysis, critical voltage analysis and also monitor silicon 'aging'.

Moortec Semiconductor says that on-chip Process, Voltage and Temperature (PVT) monitoring has become a vital factor in the design and performance optimisation of small-geometry designs. Using monitors embedded within System on Chip (SoC) designs allows for greater dynamic performance optimization.

www.moortec.com

MINIATURE DUAL-CHANNEL ROTARY JOINT SAVES SPACE IN SATELLITE SYSTEMS

Link Microtek has introduced a new miniature dual-channel rotary joint that has been specifically designed to save space in antennas for Ka-band satellite-on-the-move communications systems, which are now being deployed for high-data-rate applications in both the military and commercial sectors.

With its high-power transmit channel implemented in a right-angle WR28 waveguide on the fixed (input) side and a female K-type coaxial connector on the rotating (output) side, the AM28CORJD rotary joint measures just 31.75mm (D) x 74.68mm (H), excluding the 50mm-diameter UBR320 standard bulkhead flange.

The central transmit channel covers Ka-band frequencies from 29-31GHz and delivers excellent microwave performance, with a maximum power rating of 40W CW, a typical insertion loss of only 0.6dB and a maximum VSWR of 1.25:1.

The L-band receive channel operates over the frequency range DC to 2.15GHz.

www.linkmicrotekeng.com

NEAR EYE DISPLAY MINIATURE OLED DISPLAYS FROM MICROOLED AT ASTUTE

Astute Electronics has signed a worldwide franchise agreement with MICROOLED of France to stock its small, high-definition, low-power OLED displays that target Near-Eye Display (NED) applications such as video glasses, head-mounted sports devices, camera viewfinders, medical applications and many other professional devices. MICROOLED's low voltage device architecture features a unique sub-pixel arrangement resulting in highest pixel density and lowest power.

The design of MICROOLED's displays provides ultra-high contrast, ensuring 'black is black', which is essential for high image quality. Unlike other displays, no 'grid matrix' is visible, further improving resolution, and the manufacturing technology enables a wide viewing angle with no loss in contrast or changes in colour. Power consumption is typically two or three times less than competing products.

www.astute.co.uk

LATTICE SEMICONDUCTOR EXPANDS USB TYPE-C PRODUCT FAMILY

Lattice Semiconductor expanded its USB Type-C product family with three new offerings: Sil7012, Sil7013 and Sil7014 port controllers.

Port controllers are used to configure the USB Type-C upstream facing port (UFP) or downstream facing port (DFP), detect cable orientation and negotiate power delivery (PD) on the USB Type-C connection.

The Sil7012 and Sil7013 port controllers offer a single integrated solution that can detect and decode configuration channel (CC) and biphase mark code (BMC) messaging over USB Type-C connectors without the need for discrete components. These ICs work in conjunction with existing application processors (AP) and embedded controllers (EC) to provide cost-optimized USB Type-C port controllers.

The solutions are compliant with the latest PD and CC requirements defined in the USB specifications.

www.latticesemi.com

SILICON LABS SI88X2X MODULES NOW AT MOUSER ELECTRONICS

Mouser Electronics is now stocking Si88x2x Dual Digital Isolators from Silicon Labs. The Si88x2x modules integrate proven digital isolator technology with an on-chip isolated DC-DC converters to provide regulated output voltages of 3.3V or 5.0V at peak output power of up to 5W with external power switch.

The Silicon Labs Si88x2x Dual Digital Isolators include a DC/DC controller with user-adjustable frequency for minimizing emissions, a soft-start function for safety, shutdown option and loop compensation.

The Si88x2x modules' topology allows them to sense the output voltage on the secondary side without requiring additional optocouplers and support circuitry to bias those optocouplers. This allows the DC-DC converter to operate with excellent line and load regulation while reducing external components and increasing lifetime reliability.

www.mouser.com

NEW 'PLUG & PLAY' PROXIMITY SWITCHES FROM PANASONIC

Panasonic Automotive & Industrial Systems has introduced a new series of human detection proximity sensors that are 35% thinner than previous versions and are simple to install thanks to their 'plug and play' nature. The new devices also feature built-in trigonometric background suppression, so they are unaffected by changing scenes or by people passing by, outside the detection range. Changing light conditions and bright daylight measuring up to 30klux at the sensor's surface will not affect the performance of the sensor either.

Like previous versions, the proximity sensors measure 10mm wide and 20mm high, but their depth is only 12.7mm compared to 19.5mm. The timing of the signals can be adjusted so each adjacent sensor's beam frequency does not interfere with the other's.

http://eu.industrial.panasonic.com/

HARWIN SIMPLIFIES MINIATURE EMC SCREENING

Harwin has expanded its popular EZBoardware range with three new RFI Shield Clips suitable for small and low profile shield cans with wall thicknesses of between 0.15 and 1.0mm. The additions include two clips of only 3.9mm length, allowing users to fix smaller sized cans to the PCB using this cost effective method.

The range of clips now available also includes the S0961-46R, specifically designed to provide significantly higher retention forces on the shield can, typically up by 30%, ideal for those users seeking to maximise retention of the shielding can to the board.

Supplied taped and reeled, EZShield Can Clips are designed to be automatically placed and surface mounted to the PCB, saving time-consuming, costly and potentially damaging secondary processing operations.

www.harwin.co.uk

4CH 50MHz only at
WWW.RIGOL-UK.CO.UK

RIGOL
WWW.RIGOL-UK.CO.UK

ONLY
£239 +VAT

Apacer
THE MOST RELIABLE STORAGE FOR INDUSTRIES

Industrial MEMORY SOLUTIONS

www.apacer.com

Industrial SSD SOLUTIONS

embedded@apacer.nl

IntelliConnect
A DIFFERENT KIND OF CONNECTOR COMPANY

'From drawing to delivery in just seven weeks' – not a claim that many manufacturers of custom RF connectors can make, but by using locally sourced components and UK manufacture, IntelliConnect are able to offer this exceptional service – and at very competitive prices.

Products include:
- **Standard range RF connectors**
- **Waterproof (Pisces range)**
- **MMWave products**
- **Cable assemblies**
- **Multipin & Triaxial**
- **Dustcaps**

For further information, please call us on ***01245 347145****, email* ***sales@intelliconnect.co.uk*** *or visit our website.*

From drawing to delivery in 7 weeks !!

THE UK'S ***ONLY*** MAJOR MANUFACTURER OF 50Ω COAXIAL CONNECTORS

www.intelliconnect.co.uk
ABMS • BMA • C • N • SMA • TNC • Dustcaps
Waterproof RF Connectors • Cable Assemblies

KESTREL
Electronic Components Limited
Telephone: 01840-770028
Fax: 01840-770705
7 Gavercoombe Park Tintagel, Cornwall PL34 0DS
www.kestrel-electronics.co.uk

100+ PRICES
many other PICS available

PIC18F13K22-I/SO	0.75	PIC16F1933-I/SS	0.71
PIC18F23K20-I/SS	0.78	PIC16F1933-I/SO	0.71
PIC18F24J10-I/SS	0.68	PIC16F1934-I/PT	0.81
PIC18F26K22-I/SS	1.28	PIC16F1936-I/SO	0.78
PIC18F43K22-I/PT	1.08	PIC16F1936-I/SP	0.93
PIC18F44J10-I/PT	0.95	PIC16F1936-I/SS	0.71
PIC18F44J11-I/PT	0.92	PIC16F1937-I/PT	0.84
PIC18F45K20-I/PT	0.96	PIC16F1938-I/SO	0.89
PIC18F45K22-I/PT	1.03	PIC16F1938-I/SS	0.82
PIC18F46K22-I/PT	1.31	PIC16F1939-I/PT	0.94
PIC18F64J11-I/PT	1.17	PIC16F1827-I/SO	0.62
PIC18F65J10-I/PT	1.19	PIC16F1828-I/SO	0.63
PIC18F65J11-I/PT	1.32	PIC18F4520-I/PT	2.22
PIC18F65J15-I/PT	1.33	PIC18F6585-I/PT	4.55
PIC18F65K22-I/PT	1.48	PIC18F6621-I/PT	4.45
PIC18F66J10-I/PT	1.37	PIC18F6622-I/PT	3.35
PIC18F67J11-I/PT	1.19	PIC18F8722-I/PT	4.35
PIC18F67K22-I/PT	1.79	M27C2001-10F1	2.81
PIC18F87K22-I/PT	2.04	M27C1001-10F1	2.44
PIC12F629-I/SN	0.36	M27C512-10F1	1.95
PIC12F629-I/P	0.45	M27C256B-10F1	1.75

We can also supply Maxim/Dallas, Lattice, Linear Tech
PLEASE VISIT OUR WEB SITE FOR FULL LIST

TELONIC KIKUSUI
www.telonic.co.uk info@telonic.co.uk

AC POWER SUPPLIES / FREQUENCY CONVERTERS

DC ELECTRONIC LOADS

ELECTRICAL SAFETY TESTERS

PROFESSIONAL DC POWER SUPPLIES

Tel : 01189 786 911 Fax : 01189 792 338

CCLIX
perfectly into place

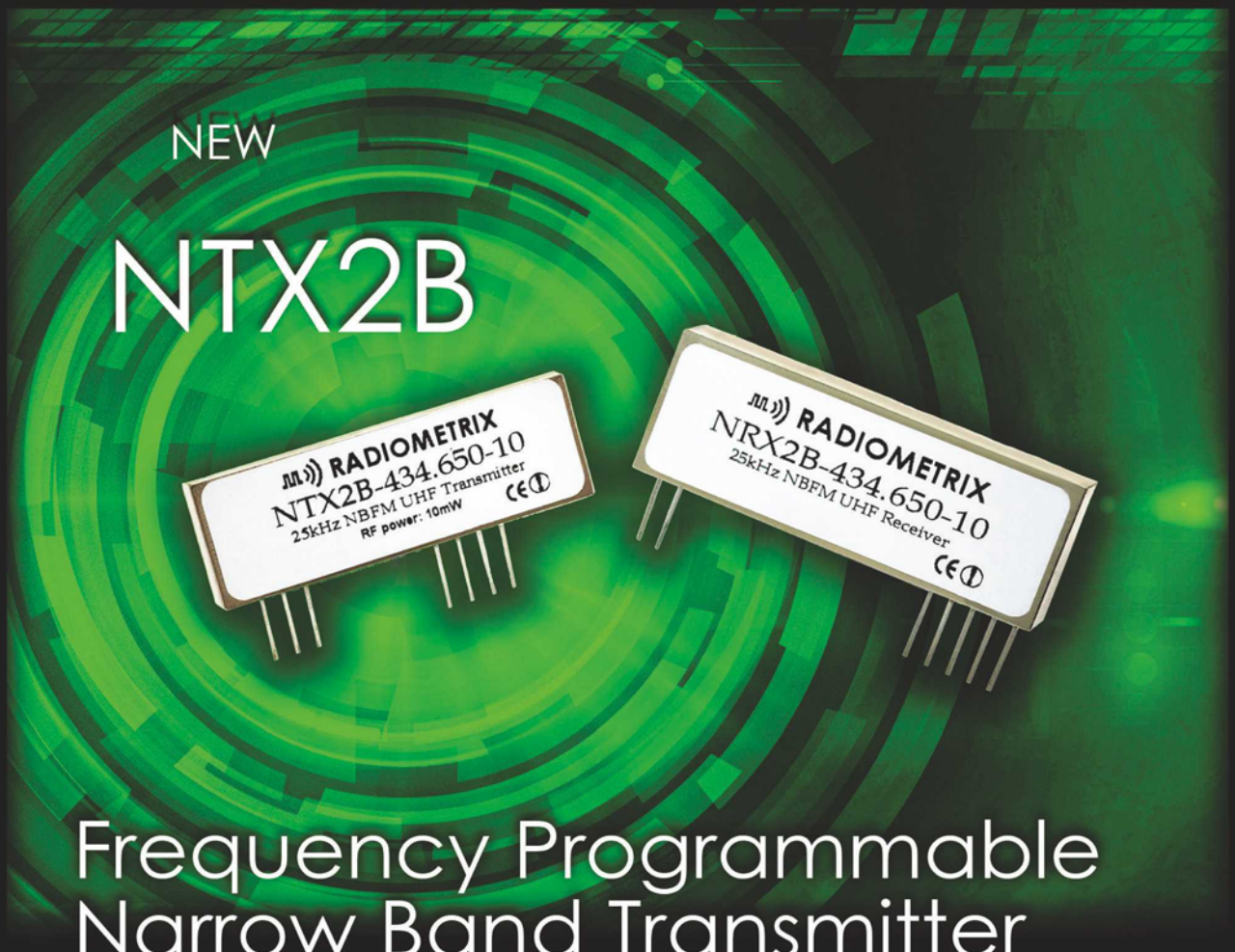
LOW COST Industrial Computer
INSTANT Start up
MQX Real Time Operating System
POWERFUL Development Tools
SOURCE Level, Task Aware Debugging
OVER 30 yrs of UK support for clients
Check out our Website for full details:
www.CCLIX.co.uk

The perfect place for answers

CAMBRIDGE MICROPROCESSOR SYSTEMS LTD
Unit 17 Zone 'D' Chelmsford Road Industrial Estate,
Great Dunmow, Essex UK CM6 1XG

RADIOMETRIX

www.radiometrix.com



Frequency Programmable Narrow Band Transmitter

New range of highly flexible, frequency programmable, RF power adjustable radios.

True Narrow Band FM performance, available on user/factory programmable custom frequencies between 425MHz & 470MHz. Matching receiver available.

VISIT http://radiometrix.com/content/ntx2b

CALL +44 (0)20 8909 9595 *REAL RADIOS FOR REAL APPLICATIONS*

Authorised global distributor of the **NEWEST** electronic components.

mouser.com/new

You can't invent the future with the products from the past.

Design with the **NEWEST** PRODUCTS ahead of their time.

MOUSER ELECTRONICS

The Newest Products for Your Newest Designs®

Mouser and Mouser Electronics are registered trademarks of Mouser Electronics, Inc. Other products, logos, and company names mentioned herein, may be trademarks of their respective owners.