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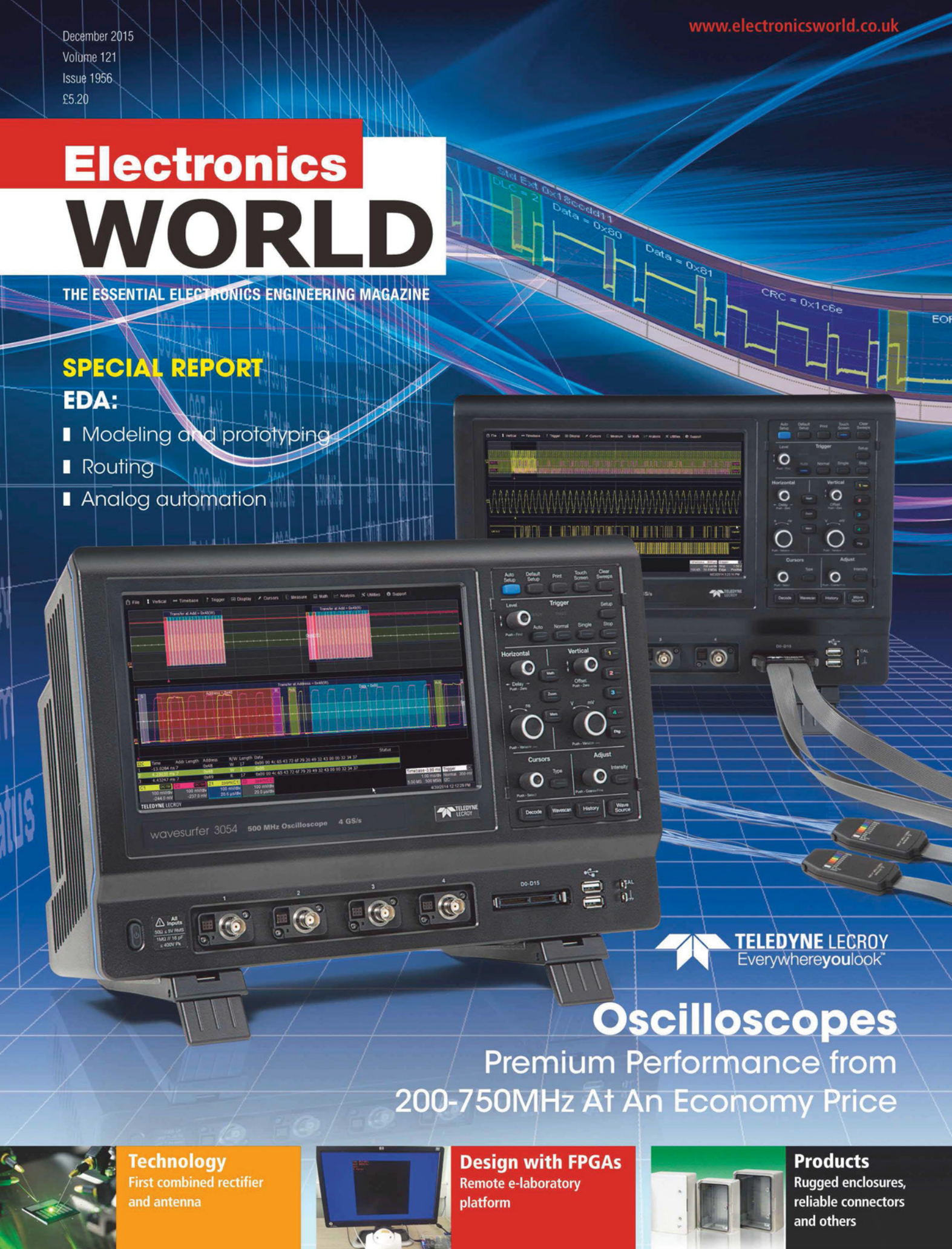

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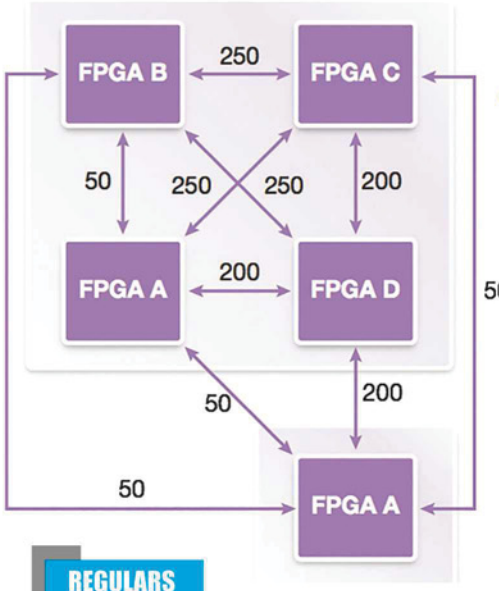

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REGULARS

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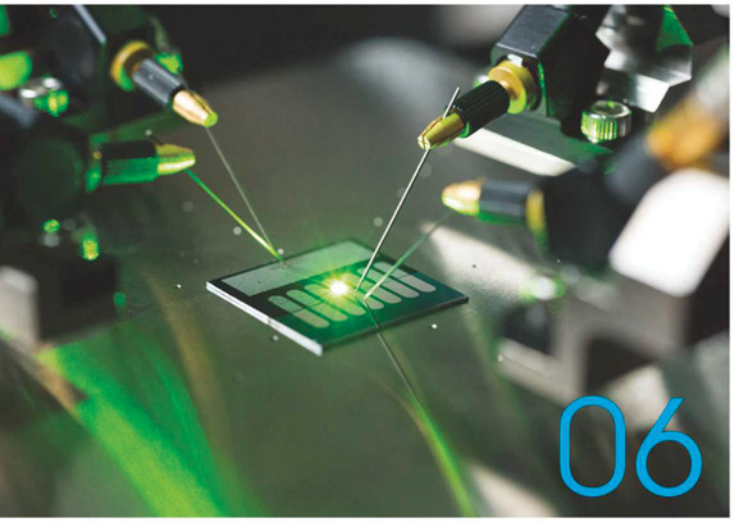

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SONY PLANS TO SPIN OFF ITS SEMICONDUCTOR GROUP

Japanese semiconductor and consumer electronics giant Sony has announced a plan to spin off its semiconductor group into a new entity. But, could this make its image sensor business even stronger?

The announcement was made on October 6, 2015, when Sony announced its plan to divest its semiconductor business from Sony Corporation into a new entity, called Sony Semiconductor Solutions.

The transfer, scheduled for completion by April 2016, is both expected and surprising at the same time. Over the past two years, Sony has spun off its audio and video business (February 2015), and its TV and PC businesses (February 2014).

However, the semiconductor spin off is different. While the TV, PC and A/V businesses had been struggling to some extent with increased competition and a slow-growing world economy, the semiconductor business has generated a significant amount of Sony's recent revenues and profitability, driven by image sensors, historically a successful and profitable business for Sony.

Analysis

Sony is obviously moving in a new direction to ease planning, shorten time-to-market and increase profitability. But, what will be the ultimate effect of this spin off on Sony's image sensor business?

Sony has been very successful in the growing and highly-competitive image sensor market. This has been true since the 1980s, when Sony CCDs powered devices such as camcorders and corporate security cameras.

The company was able to transition smoothly as the market moved to CMOS image sensors for camera phones and tablets. Today, it dominates the CMOS image sensor business with Q2 2015 revenues of over $1bn, more than 42% of the worldwide market and nearly three times the revenue of its closest competitor, Samsung Electronics.

In the face of this market dominance of image sensors, the question arises for Sony: why interfere with a good thing? The current Sony corporate structure seemed to be working well enough to ensure image sensor success. How will the new Sony Semiconductor Solutions benefit the image sensor business? The answer may be by simplifying a corporate structure so it can react more rapidly.

> At first glance, it seems unlikely that Sony could improve its already dominant position in the image sensor market

If Sony has had a weakness in the image sensor market, it has been exploiting new markets and getting new sensors to market quickly. A recent example is the release of CMOS sensors with 1.0-micron pixels, the next step in CMOS phone sensor design. Both OmniVision and Samsung have already announced 1.0-micron models, while Sony has not.

Also, Sony has been slow to embrace new, emerging applications such as automotive cameras. It just entered the automotive space in 2015, while competitors such as ON Semiconductor (through its acquisition of Aptina) have dominated the market for years.

Sony has stated that one of the purposes of its semiconductor spin-off strategy is "to more rapidly adapt to changing market environments and generate sustained growth".

The old Sony structure was somewhat difficult for the image sensor business. In addition to its size presenting a barrier to quick decisions, the old system included Sony Semiconductor Corporation for image sensor manufacturing and Sony LSI Design for design operations. Under the new structure both will be combined under Sony Semiconductor Solutions.

At first glance, it seems unlikely that Sony could improve its already dominant position in the image sensor market. However, the spin off to a new organization that allows Sony to respond more quickly to market changes and speed time-to-market for new designs may have precisely that result.

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FIRST COMBINED RECTIFIER AND ANTENNA CONVERTS LIGHT TO DC CURRENT

Researchers at Georgia Institute of Technology in the US have shown the first optical rectenna, a device that combines the functions of an antenna and a rectifier diode to convert light directly into DC.

Based on multiwall carbon nanotubes and tiny rectifiers fabricated onto them, the optical rectennas could be a new technology for photodetectors that operate without the need for cooling, and energy harvesters that convert waste heat into electricity, which will be a new way to efficiently capture solar energy.

"We could ultimately make solar cells that are twice as efficient at a cost ten times lower, and that to me is an opportunity to change the world in a very big way," said Baratunde Cola, associate professor for Mechanical Engineering at Georgia Tech. "As a robust high-temperature detector, these rectennas could be a completely disruptive technology."

In optical rectennas, the carbon nanotubes act as antennas to capture light. As light waves hit them, the nanotubes create an oscillating charge that moves through the attached rectifier devices. The rectifiers switch on and off at record high petahertz speeds, creating a small direct current. Billions of rectennas in an array can produce significant current.

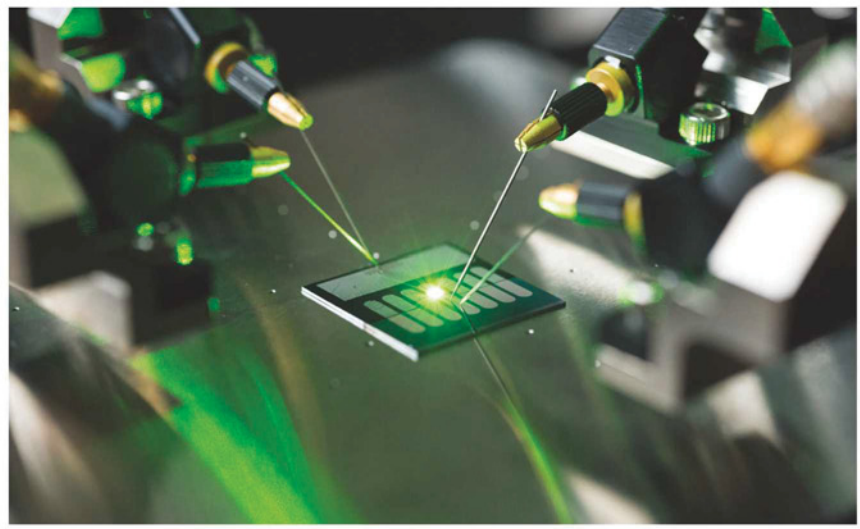
The efficiency of the devices demonstrated so far remains below 1%, but researchers hope to boost that output through optimization techniques, and believe that commercial rectennas may be available within a year.

RECTENNA TECHNOLOGIES

Rectennas developed in the 1960s and 1970s have operated at wavelengths as short as ten microns, but for more than 40 years researchers have been attempting to make devices at optical wavelengths. There were many challenges, such as making the antennas small enough to couple optical wavelengths, and fabricating a matching rectifier diode small enough and fast enough to capture the electromagnetic wave oscillations.

The newly created rectennas harness the wave nature of light rather than its particle nature.

"A rectenna is basically an antenna coupled to a diode, but when you move into the optical spectrum, that usually means a nanoscale antenna coupled to a metal-insulator-metal diode," said Georgia Tech's Baratunde Cola. "The closer you can get the antenna to the diode, the more efficient it is. So the ideal structure uses the antenna as one of the metals in the diode – which is the structure we made."



A carbon nanotube optical rectenna converts green laser light into electricity [Credit: Rob Felt, Georgia Tech]

X-FAB SETS NEW BENCHMARKS FOR LOW-NOISE 0.35µm AND 0.18µm CMOS TRANSISTORS

Germany-headquartered X-FAB Silicon Foundries has announced mixed-signal 0.35µm and 0.18µm CMOS process transistors with drastically reduced flicker noise. Both, n-channel devices in its 0.35µm process and p-channel devices in its 0.18µm process had their flicker noise reduced by a factor of five, setting a new industry benchmark.

With such low noise, these transistors allow improved and more compact circuit designs at lower cost. They could also be the basis for lower-noise amplifier variants with a significantly higher signal-to-noise ratio.

"The combination of complementary XH035 n- and p-channel transistors offers designers more freedom in their circuit designs. They are no longer limited only to low-noise p-channel devices, and additional mask layer expense. The new XH018 p-channel device makes it possible to develop noise-critical designs for 0.18µm processes," said Dr Jens Kosch, Chief Technical Officer at X-FAB.

The new transistors are available immediately for new designs. Noise parameters are included within the device models to facilitate an accurate simulation of the noise behaviour of a circuit prior to its actual use.

"For the 0.18µm XH018 process, the new lower-noise 3.3V p-channel MOSFET will become available for new designs in November 2015," added Dr Kosch.

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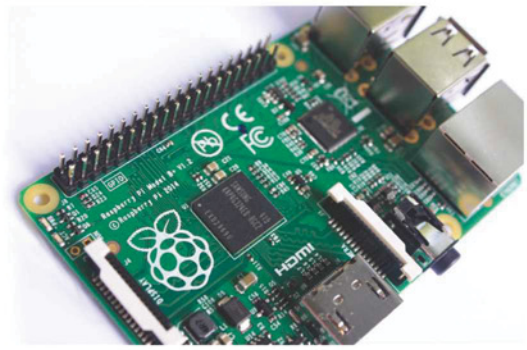
THIS SERIES PRESENTS THE RASPBERRY PI SINGLE-BOARD COMPUTER, ITS FEATURES AND BENEFITS, AND ITS USE IN VARIOUS PROJECTS

The Sauce Bottle Game



BY **MIKE COOK, JONATHAN EVANS** AND **BROCK CRAFT**

The project in this column is just about the most fun you can have with a single contact input. Whether you call it catsup, ketchup or sauce, it's a thixotropic fluid, which means it changes its viscosity according to the agitation of the fluid.

The game is simply an interactive sauce bottle where shaking can be sensed by the Raspberry Pi. This is mirrored on screen by a graphic of the same bottle. However, on the screen, the sauce bottle can be seen to empty slowly in response to the shaking. The idea is to get the bottle emptied in the shortest possible time.

This game is a great introduction to the interaction of hardware and software.

Parts

The parts needed for this project are simple, and can be substituted if the exact ones are not readily available. The ones we used are:

- Plastic sauce bottle: we used a Heinz Tomato Ketchup bottle, but any similar one will do.
- Two meters of twin core cable: we used shielded microphone cable.
- Tilt switch: The tilt switch consists of a metal ball in a small tube. When the ball rolls to one end, it shorts out the two wires leading into the tube.
- Two single-pin header sockets: Any connecting method to the general-purpose input/output (GPIO) pins will do.
- Hot melt glue and glue gun.
- Silicon sealant.

Schematic

The arrangement in Figure 2 is very easy to follow.

It doesn't matter which way around the wires are connected on the switch; they just connect and disconnect the GPIO pin 2 to ground, a pin normally used for the I2C interface. On the board, pin 2 is connected to a pull-up resistor connected to the 3V3 supply, which ensures that the logic level on this pin is normally 1, unless the pin is connected to ground, in which case it becomes logic 0.

Construction

Here are the steps in building this project:

1. Drill a hole in the top of the bottle for the wire to go into.
   Our wire was 1.5mm in diameter so we drilled a 2mm hole.
2. Push the wire through the hole into the bottle.
   This step is critical. Pushing in the wire from the outside of the bottle is easy; pushing the wire through the hole from the inside of the bottle is impossible.
3. With silicon sealant, glue the tilt switch onto the small flexible membrane on the bottle lid, which normally holds back the sauce.
   Allow the sealant to set.
4. After the sealant sets, wire the screened cable to the tilt switch, as shown in Figure 3.
5. Apply some hot glue over the tilt switch and run it around the base of the cap.
   Don't overfill it or you'll never get the screw bottle back on the cap.
6. Screw the cap back onto the bottle and then put a blob of hot glue where the cable comes out of the bottle to fix it.
   Make sure there's enough slack in the bottle to remove the cap if any repairs are needed.

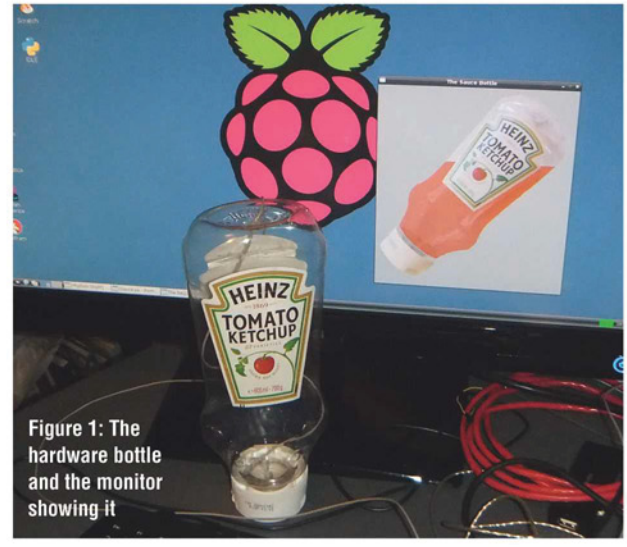


Figure 1: The hardware bottle and the monitor showing it

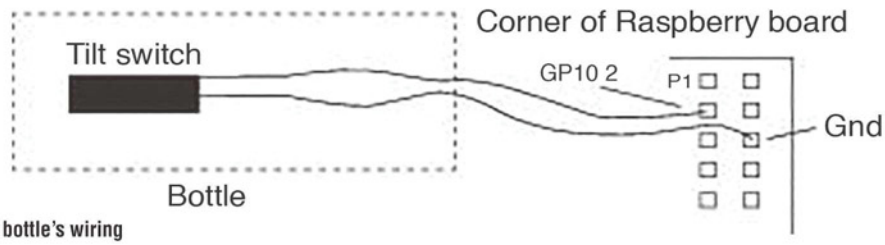


Figure 2: The sauce bottle's wiring

7. Attach the other end of the cable to the Raspberry Pi. This can be done in a variety of different ways with various breakout boards. Because there are only two wires, we used two single-pin sockets and shells and connected them directly to the GPIO connector, as shown in Figure 4. We soldered the end of the cables to these two wires and covered the joint with heat-shrink cable, but an insulating tape could also be used instead. Then we carefully placed them on the GPIO connectors before booting up the Raspberry Pi. As a rule, nothing should be connected to the Raspberry Pi while it's powered up.

Figure 3: Wiring the screened cable to the tilt switch

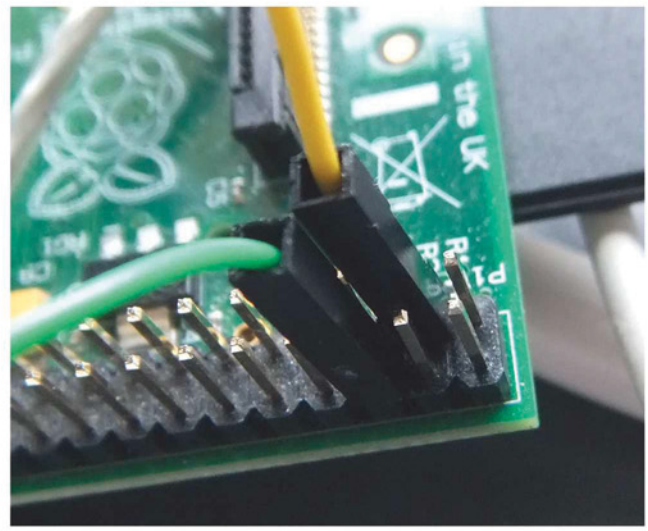


Figure 4: Connection to the GPIO pins

Testing

The next step is to test the switch. In order to access the GPIO pins, you need a special library. There are a few of these around, but one of our favorites is WiringPi by Gordon Henderson. There is a Python front-end, easy to install. From the desktop open a command-line prompt and type the following:

```
sudo apt-get install python-dev python-pip
sudo pip install wiringpi2
```

That should be it. You can test that it's installed correctly by typing:

```
sudo python
import wiringpi2
wiringpi2.piBoardRev()
```

The revision number of the board should be seen. However, to access things as root user, the sudo command should be used. You can still program in the IDLE environment by opening it and typing the following from a command-line prompt:

```
gksudo idle
```

Then everything you do is as a root user. Get into IDLE like this, open a new window from the file menu and type the program in Listing 1. This is a very simple program and shows the basis for reading a GPIO pin. It starts off by importing an instance of the wiringpi2 library. A warning about being a root user shows up. (If the program crashes on the next instruction, it means you aren't the root user.)

The io.wiringPiSetup() function is then called, which initializes the library. This sets up the pins with pin mapping that automatically takes care of swapping them when needed on this header, which has occurred in the different editions of the board. Here, GPIO 2 (or GPIO 0 on a Raspberry Pi 1 board) is on connector P1 on pin 3, but it's referred to as pin 8 in the software.

It may sound complex, but the point is that pin 8 will access the same pin on the GPIO connector no matter what board revision of the Raspberry Pi you have.

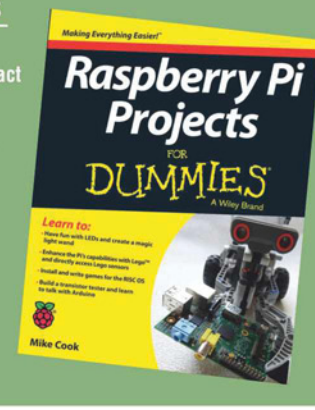
```
#!/ #!/usr/bin/env python
"""
Sauce bottle switch test
"""
import wiringpi2 as io
print "if program quits here start IDLE with 'gksudo
idle' from command line"
io.wiringPiSetup()
io.pinMode(8,0) # Physical Pin P1,3 GPIO 2
print "Pin test - Ctrl C to quit"
lastPin = 0
while True :
pin = io.digitalRead(8)
if pin != lastPin:
print "Pin now ", pin
lastPin = pin
```

Listing 1: Switch test

The io.pinMode(8,0) call then makes this pin an input, and finally io.digitalRead(8) returns the logic value of this pin. A variable called lastPin holds the previous value on the pin and prevents it from being printed out if it hasn't changed. Run the code and you'll see how the pin state changes with the tilt of the switch. If you don't see any changes, check the wiring and chase down the fault. ●

RASPBERRY PI PROJECTS FOR DUMMIES

This column is an edited extract from 'Raspberry Pi Projects For Dummies' by Mike Cook, Jonathan Evans and Brock Craft, published by Wiley. To check if you have won this book or any of the previous ones in this series of articles, turn to page 45.



Making Meaningful Methodical Measurements

BY **MYK DORMER**

In the low-power RF sector, we throw specification figures around like they are about to go out of fashion. Everything is "longer-ranged", "faster" and "more robust" than the competition, and sooner or later something is being lauded for having a receive sensitivity of this many "dBm", or having that many dB of selectivity or blocking ... but what do these arcane figures mean, and how do we (consistently) measure them?

The first point to cover is the mysterious "dB" or "decibel": whatever the origin or usage of this unit in other fields, in RF engineering it is simply used to denote a logarithmic measurement scale. Unless followed by a qualifying unit, it does not denote an absolute amount of anything; it is a ratio or comparison. When RF engineers say "-60dB spuri" they mean that the spurious signal is 60dB lower in (usually) power than another signal (usually the wanted carrier).

So why the "dB" jargon? Why not just use a simple numerical ratio?

The reason has to do with the huge range of signal level (in terms of power, or voltage) that RF systems deal in. Even simple radio receivers can just as happily resolve signals anywhere (for example) between a volt and a microvolt. In linear scale terms that is a ratio of one to one million, or six orders of magnitude, but expressed on a logarithmic scale it's a more easily handled 120dB (20log(V1/V2)).

Having said that dB is a unitless scale, here we must complicate matters slightly. It is also useful to use logarithmic scales for absolute measurements. In these cases the complete terminology would be "dB relative to (for example) a microvolt" (dBuV) or "dB relative to a power of one milliwatt in a given termination impedance" (the dBm, at last! For RF systems, this impedance is usually 50 ohms). The second of these is particularly useful and widely used.

To return to our "one to a million" example: In dBuV terms a volt is +120dBuV and, obviously, a microvolt is 0dBuV (not 1dBuV – remember that the value of log(1) is zero).

In a 50-ohm-impedance system, then a volt (allowing that we are talking about rms volts) is 20mW, and a microvolt is 0.02 of a picowatt. Express the same power levels in dBm however and we have +13dBm and -107dBm ... much easier to mentally grasp and work with.

Notice that voltage levels are expressed as 20log(V/V), while power levels are 10log(P/P), but that they result in the same (in this case) 120dB difference. At first sight this looks strange, but for a fixed impedance, power relates to the square of the voltage, and 20log(x) = 10log(x^2)).

Meaningful Measurements

Given a usable system of expressing our measurements, we can now examine the measurements themselves. A few specifications – such as transmitter power output – will consist of simply stated absolute levels ("500mW, or +27dBm, into 50 ohms"), usually related to regulatory maximum limits. The remainder of the specifications are much more interesting: they relate either to stated performance conditions, or to another specified condition.

Receiver sensitivity is always given as a signal level for a stated level of performance. This can be anything from an S/N level to a bit error rate, but it must always be explicitly stated. Claiming a "sensitivity of -115dBm" means nothing without associating it with a measurable performance, such as "for a bit error rate of 0.1%, at 5kbit/s". This defined performance threshold is also vital to the process of making meaningful measurements of the other relevant parameters.

Although various regulatory documents (and different drafts of the same document, in many cases) specify different performance thresholds, a very similar underlying test protocol is often found:
a) Establish the sensitivity (input signal for a given threshold performance);
b) Increase the wanted signal by a given amount (usually +3dB);
c) Increase the interferer level until performance drops back to threshold.

The rejection level in question is then the difference between the wanted and the interfering signals.

It is worth mentioning that there is a second method sometimes encountered, where a fixed level of wanted signal is applied, at least 10dB above the actual threshold, and the interferer is increased until performance drops back to threshold once again. Oddly, this usually results in very similar results, even though the tests are conducted at higher signal levels.

Although there are dozens of different thresholds in use, a good "in the lab" first-cut approximation method for typical low-power wireless modules employs a performance threshold defined as "12dB SINAD (at the audio output pin), in 0.3 -3.4kHz audio measurement bandwidth". Most commonly used RF communications test-sets can support this measurement (or a decent approximation to it), although what really matters is that a consistent method is adopted, not the actual specifics of the method selected. ●

The Next Generation Of Wireless Backhaul Antennas

BY **DIPESH RATTAN**

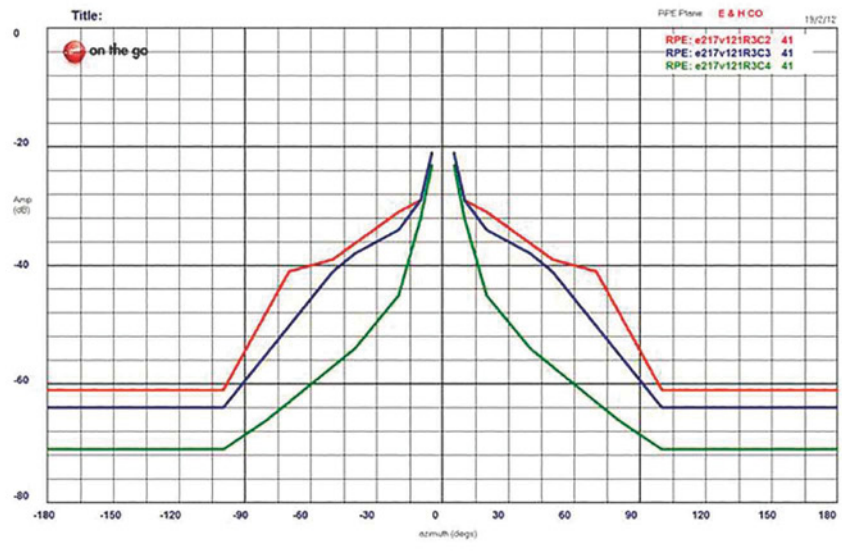
More than half of the world's cell site backhaul is accomplished using microwave radios with parabolic dish antennas. Line-of-sight, point-to-point (P2P) microwave antennas enable signal transport from the cell tower to another place, often a rooftop or second tower, and ultimately into the core fibre network.

The need among mobile network operators (MNOs) for more capacity is giving rise to a new discussion on the importance of these antennas. They are a critical, yet often undervalued component of the microwave radio system. But, it turns out that not all microwave antennas perform as claimed.

CommScope has undertaken several extensive studies on microwave radio link backhaul antenna performance. In an initial study, sample antennas were obtained on the open market from every manufacturer known to be providing P2P microwave antennas to the industry at the time. The results showed that a significant proportion of antennas were substantially non-compliant to their published specification (mainly the declared sidelobe or off-axis gain performance along with cross-polar performance).

Furthermore, it was noted that antennas exhibited changing performance, with the sidelobe or off-axis gain performance degrading over time. Of course, this is bad news for the industry because the declared sidelobe or off-axis gain affects link capacity. It is also a representation of the interference threat one link presents to another. If interference does occur, then link availability and capacity – and hence data throughput – are

Microwave systems are the most common form of backhaul at wireless cell sites



ETSI Class 4 microwave antennas have a tighter radiation pattern that offers significant benefits to operators, including cost and capacity improvements

compromised, leading to a reduction in operator revenues.

In response to this study, CommScope examined the cost to the network operator in terms of capacity and quality of service (QoS). Unsurprisingly, it was found that both were negatively impacted; in addition, there were significant constraints on the ability to reuse spectrum (frequency reuse), potentially limiting the number of deployed links for a given amount of spectrum.

In a subsequent study, CommScope chose to investigate the potential benefits to capacity and QoS when superior performing antennas were deployed, offering substantially better than specified performance.

In conjunction with EE, CommScope studied the benefits of moving from industry-standard European Telecommunications Standards Institute (ETSI) Class 3 antennas to Class 4 ones. The study showed substantial benefits possible for backhaul network operators who upgrade to these antennas on their networks.

ETSI Class 4 antennas have a tighter radiation pattern that offers significant benefits to operators, including cost and capacity improvements. Class 4 antennas contain the radiation pattern more tightly than lower classes, improving the carrier signal-to-interference ratio. This ratio is a comparison of the amount of the carrier's intended radio signal received at a certain point against how much interference distorts it. A better ratio means there's more capacity in the backhaul network.

This network case study was done on MBNL's UK microwave backhaul network of 6,259 links that operate in the 40GHz and 10GHz frequency bands. Comsearch's iQ.linkXG, a microwave planning and optimization tool, was used to model the network. The core findings were:

- Over $5m in total cost of ownership (TCO) saved over five years – 192 links failed in both 40GHz and 10GHz frequency bands, as reported by EE. These links were not operational with existing Class 3 antennas due to microwave signal frequency congestion. By using Class 4 antennas on the failed links, a minimum of 88 of these total 192 failed microwave links can be recovered in the available spectrum. Some 96% and 31% of frequency congested links in 40GHz and 10GHz, respectively, were assigned a channel.
- $44,000 in TCO savings in license fees over five years – the 88 failed links could now be assigned a channel without buying additional channel licenses from Ofcom, thus saving additional spectrum license cost.
- $4.5m in TCO savings per year based on optimizing capacity by freeing congested channels – by using Class 4 antennas, 68 microwave links could be upgraded to higher capacity 56MHz wide-channel radios and still meet the MNOs' availability objective.

> A significant proportion of antennas were substantially non-compliant to their published specification

CommScope brands its Class 4 microwave antennas as Sentinel

- 3,000 more radio links can be added to the network where none had been possible before – the small sidelobes of Class 4 antennas improve frequency reuse in an existing network, allowing more links to be deployed in the now under-used channels.
- 582-hour quality of service (QoS) improvement (dropped calls) – reducing the interference level improves the availability for link traffic.

There is also a strong temptation to trade some of the above benefits for reduced antenna size, which itself would reduce TCO in the form of tower lease costs. These results suggest that microwave link planners should seriously consider using better antennas or, at least, modelling their network with the improved specifications as validation of their current implementation efficiency.

The opportunity coming from utilizing better antennas highlights the risks of using inferior ones. CommScope found that when poor-quality antennas are used, design objectives for radio links are not met. As a result, many networks underperform or do not meet their design capacity as data throughput demands rise. This adversely affects the subscriber experience and, consequently, may contribute to increased churn of mobile customers.

The microwave antenna's performance in the backhaul network has become a compelling opportunity, as well as a significant threat to QoS. Its anonymity and lack of control has led to QoS problems, and P2P links that cannot possibly deliver their design capacity, particularly given the increased use of adaptive coding and modulation. In the face of growing capacity demands – particularly the exponential growth of mobile video applications – the performance of the antenna in backhaul applications can no longer be ignored. ●

Dipesh Rattan is Product Line Manager for Microwave Antenna Systems at CommScope.

This column is an edited extract from CommScope's new eBook, 'LTE Best Practices'. Different authors of this eBook will contribute articles to this section.

WAVESURFER 3000 OSCILLOSCOPES

Premium Performance from 200 MHz – 750 MHz at an Economy Price

WaveSurfer 3000 200 MHz to 750 MHz oscilloscopes feature the MAUI advanced user interface with large 10.1" touch screen to shorten debug time. Quickly identify and isolate anomalies with long memory, WaveScan, Fast Display, and History Mode for faster troubleshooting; LabNotebook enables easy documentation. Now it is even more powerful as all Serial Data TD Options are included as well as the integrated function generator for a starting price of just € 3,140.-

Large Display with MAUI

The large and bright 10.1" touch screen display with max. grid area for your signal is significantly bigger than typical other oscilloscopes in this class. MAUI is the most advanced oscilloscope user interface developed to put all the power and capabilities of the modern oscilloscope right at your fingertips. Designed for touch; all important oscilloscope controls are accessed through the intuitive touch screen. Made for simplicity; time saving shortcuts and intuitive dialogs simplify setup. Built to solve; a deep set of debug and analysis tools help identify problems and find solutions quickly.

Capture, Debug, Analyze, Report

The very long memory lets you acquire your signal with high sample rate over a long capture window. Combining a fast waveform update rate with History Mode and WaveScan, the WS3000 is an outstanding tool for waveform anomaly detection. Debug, analyze and docu ment problems through the math and measurement capabilities, segmented memory, and LabNotebook.

Quick Problem Finder

Using Parameter Measurements the WS3000 measures up to 1,000 values of Frequency, Rise Time, Pulse Width, etc in a single acquisition. Other oscillo scopes measure only one value per parameter and acquisition. If you have captured an event somewhere in your acquisition, the parameters will show it immediately! No need to run multiple acquisitions until the event is hitting your small single measurement

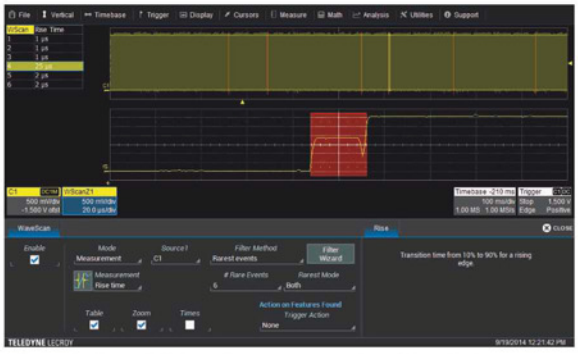


Figure 1: Powerful WaveScan automated problem finder now is standard in an entry level oscilloscope

Memory Segmentation Mode

Use Sequence mode to save waveforms into segmented memory. This is ideal for capturing fast pulses in quick succession or when capturing events separated by long time intervals. Combine Sequence mode with advanced triggers to isolate rare events over time. Trigger times and time between segments are provided for additional insight.

LabNotebook Documentation Tool

LabNotebook is a one-button tool to save and restore waveforms, measurements and settings without navigating multiple menus. Saved waveforms can be measured and analyzed later both on the oscilloscope or offline using the WaveStudio PC Utility.

Superior Math and Measurement Capabilities

A deep set of 20 math functions adds to the problem solving capability of WaveSurfer 3000. Math functions provide quick insight into waveforms and help point to the cause of the most challenging problems. Functions like the powerful FFT provide details of the frequency domain while averaging effectively filters noise out of the signal.

With 24 measurement parameters, the WaveSurfer 3000 can measure and analyze every aspect of analog and digital waveforms. Statistics and histicons go beyond traditional measurement tools providing insight to how a waveform changes over time. Measurement data can be trended to create a visual representation of changing measurements.

Multi-Instrument Capabilities

Beyond traditional oscilloscope functionality the WaveSurfer 3000 has a variety of multi-instrument capabilities including waveform

Figure 2: Automated measurement of up to 1,000 periods per Acquisition. Statistics with max, min, last value, average and standard deviation is displayed for all captured periods of data

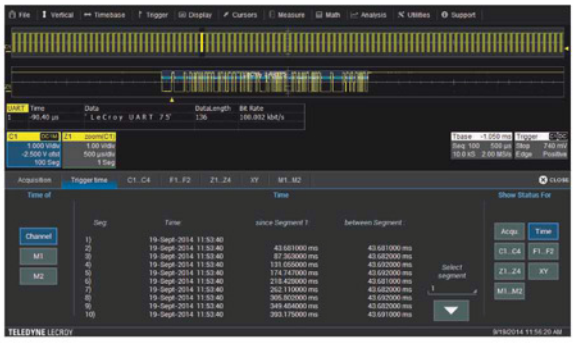


Figure 3: CAN Bus messages captured in Sequence Mode. The table is showing time stamps of every segment

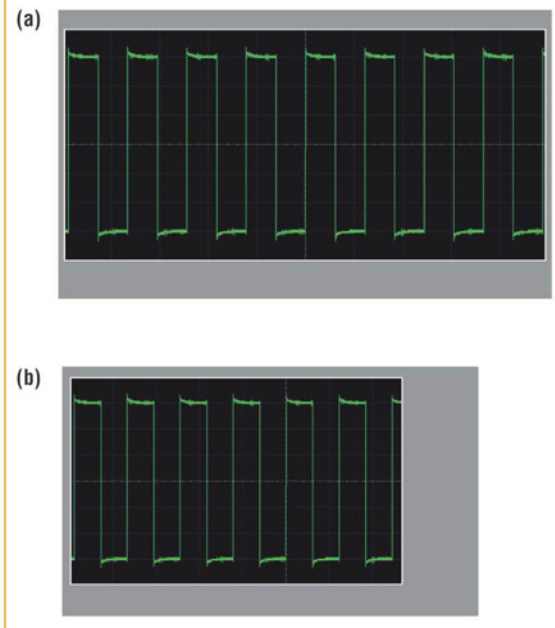


Figure 4: (a) WS3000 – 10.1" display with large max grid area (b) Competitor – 8.5" display with lower resolution and significantly smaller grid area

generation with a built-in function generator, a digital voltmeter, protocol analysis with serial data trigger and decode, and logic analysis with an 16 channel mixed signal option.

Powerful Solution for Serial Data

The WS3000 features a wide range of serial data solutions. Solving serial data problems requires intimate knowledge of the protocol to get started. The WS3000 is the expert. Simply connect your probes or cables and the scope will provide correct level of detail needed to view, debug, and analyze the serial data signals. Protocol decoding is shown directly on the waveform with an intuitive, color-coded overlay and presented in binary, hex or decimal. Decoding is fast even with long memory and zooming in to the waveform shows precise byte by byte decoding.

The serial data trigger will quickly isolate events on a bus eliminating the need to set manual triggers hoping to catch the right information. Trigger conditions can be entered in binary or hexadecimal formats and conditional trigger capabilities allow for triggering on a range of different events.

To further simplify the debug process all decoded data can be displayed in a table below the waveform grid. Selecting an entry in the table will display just that event. Additionally, built-in search functionality will find specific decoded values.

POWER TO PERFORM WITH A DUAL-CLUSTER 64-CORE GPU

SATISFYING THE REQUIREMENTS OF APPLICATIONS SUCH AS WEARABLES, MOBILE DEVICES, HIGH-END GAMING AND COMPUTING IS ONLY POSSIBLE BY CREATING ARCHITECTURES THAT CAN DELIVER THE HIGHEST LEVELS OF PERFORMANCE WHILE MINIMIZING BOTH AREA AND POWER. BY **ANDY JOLLEY**, SENIOR STAFF APPLICATION CONSULTANT FOR FPGA-BASED PROTOTYPING AT SYNOPSYS

A key challenge faced by many design teams is how to test graphics processing units (GPUs) as they become larger and more complex. Historically, prototyping based on field programmable gate arrays (FPGAs) has been limited as top-end GPUs exceed the capacity of the largest available FPGA devices, and the manual partitioning of the data-path-intensive GPU structures to multiple FPGAs has proven a time-consuming and difficult process. As a result, the only feasible approach had been to fabricate test chips – an increasingly expensive and lengthy process that extends final product lead times.

GPU Prototyping Requirements

Electronic design automation (EDA) tools provider Synopsys has been working with Imagination Technologies's design teams to explore ways of using multiple FPGAs to model its largest GPUs. An FPGA-based prototyping methodology must be able to support all configurations of the entire GPU family for standalone implementation and testing, as well as rapid GPU integration for system-on-a-chip (SoC) development.

The Synopsys team first worked on a proof-of-concept project to demonstrate an FPGA-based prototype for Imagination's PowerVR Series6 devices. The prototyping environment required a top-level test infrastructure (Figure 1) to enable standalone regression tests to be run. The test infrastructure had to support connection to a PC host via PCIe, and a DDR3 memory interface to support the storage of test stimuli and results. The test interface required extensive use of rate conversion logic to enable the test team to control and analyze the GPU, including the ability to configure the system through a Universal Multi-Resource Bus (UMRBus) and access the test and results data from the PC host.

The team manually partitioned the design for implementation on a Synopsys HAPS- 70 S48 prototyping system comprising four FPGAs. To successfully partition the largest GPU configuration took

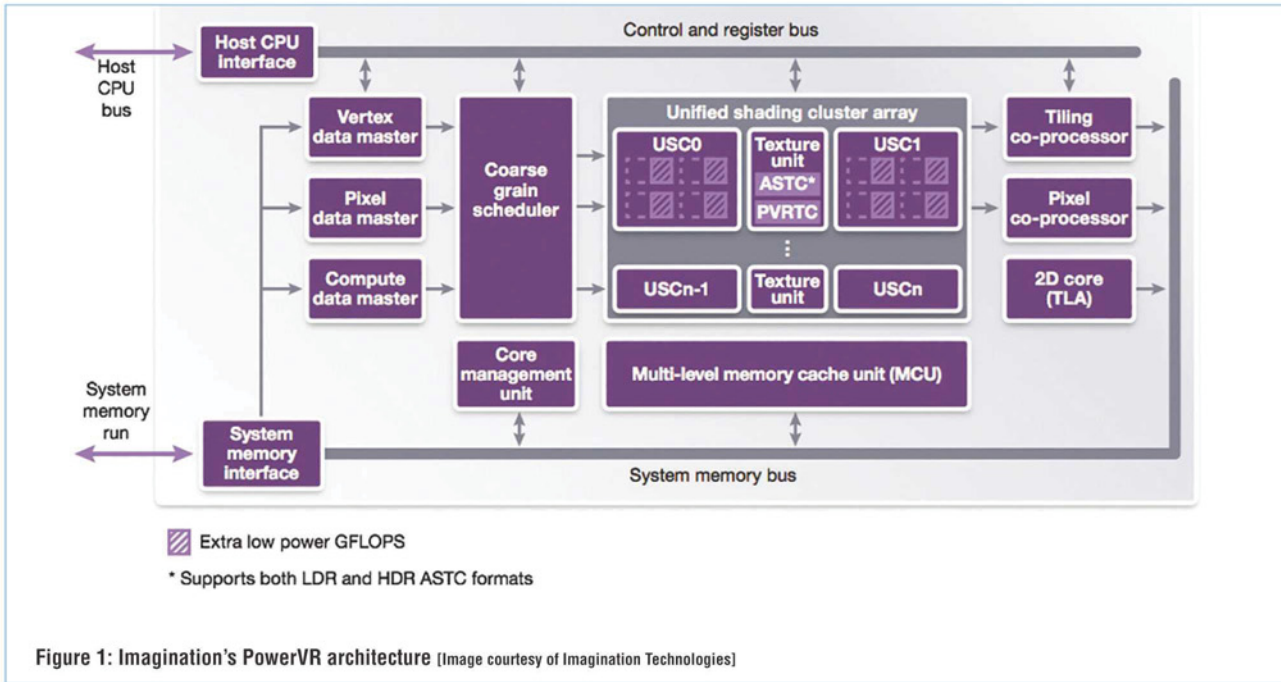
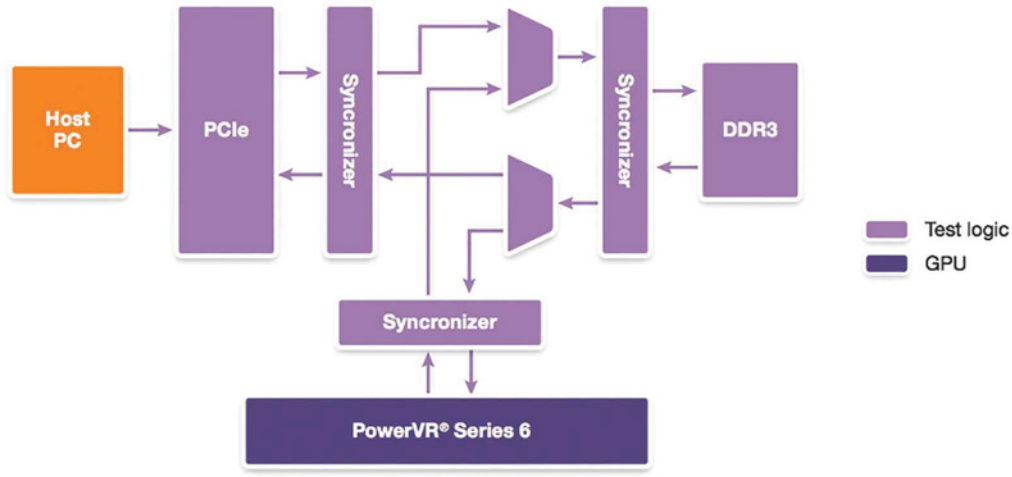


Figure 1: Imagination's PowerVR architecture [Image courtesy of Imagination Technologies]

Figure 2: Top-level test infrastructure to support regression tests



two weeks of manual design effort, iterating the partitioning to trade off the I/O multiplexing ratio and performance, and then debugging the system, running synthesis and place-and-route, and finally bringing up the prototyping system.

FPGA utilization varied between 55% and 90%, and the prototype achieved a clock speed of 8MHz, which enabled successful completion of 7,000 regression tests – all without the need to implement a test chip (Figure 2).

New Developments

While the proof-of-concept project was underway to prototype the PowerVR Series6 GPUs with Synopsys HAPS prototyping boards and Certify software, Imagination's design team was busy working on the next generation: PowerVR Series6XT GPU family.

The Series6XT GPUs offer processing performance that scales to the TFLOPS range, thanks to using significant parallelism within the GPU implementation. The Imagination design team wanted to see if prototyping could handle the largest Series6XT device.

> While Imagination had been developing its next generation GPU, Synopsys had also been working on a second generation of automated FPGA partitioning tools

The challenge was not only to partition the derivative design, which was an even larger device than the Series6 GPU, but also create additional test logic and sufficient performance to enable output of live video as part of the test.

Initial estimates of the test logic and GPU top-level design suggested that these blocks alone would exceed 100% utilization of a single Virtex 7 2000T FPGA, hence the need to repartition the original Series6 prototype design.

To compound the engineering challenge, the Imagination team needed some kind of prototype as soon as possible; reducing time to first prototype was crucial.

The Synopsys prototyping team considered two possible development routes. The first was to repartition the existing HAPS-70 48 system. While this was perfectly possible, it required a muxing ratio of 32:1, which would reduce the system performance to 2MHz – a significant compromise in terms of run times, and too slow to support analysis of live video output.

While Imagination was developing its next generation GPU, Synopsys had also been working on a second generation of automated FPGA partitioning tools. ProtoCompiler is designed to minimize the effort and time required to bring up and use a Synopsys HAPS series system for IP validation and software development. It incorporates automation features for design planning, logic synthesis, debug and connectivity to other verification environments like Synopsys VCS and ZeBu. The prototyping software is tightly integrated with the HAPS series to deliver system performance.

Testing To The Max

The Synopsys team captured the additional test infrastructure logic, which included a frame buffer and logic for the DriverLive Active Video Out, and initially allocated six FPGAs to the prototyping environment. The team also ported the basic partitioning constraints from the previous PowerVR Series6 configuration to speed the repartitioning process. Other constraints were also used to ensure there was sufficient FPGA capacity, to limit FPGA utilization to 80% and select a simple pin-muxing strategy.

Abstraction flows (Figure 4) were applied to investigate FPGA-to-FPGA interconnects – a feature within ProtoCompiler that enables the effects of various partitions to be explored very quickly. Typically scenarios can be investigated in runtimes of a minute or so.

ProtoCompiler's abstraction flows feature enabled the prototyping team to identify communication bottlenecks between FPGAs and quickly analyze the effect of increasing the

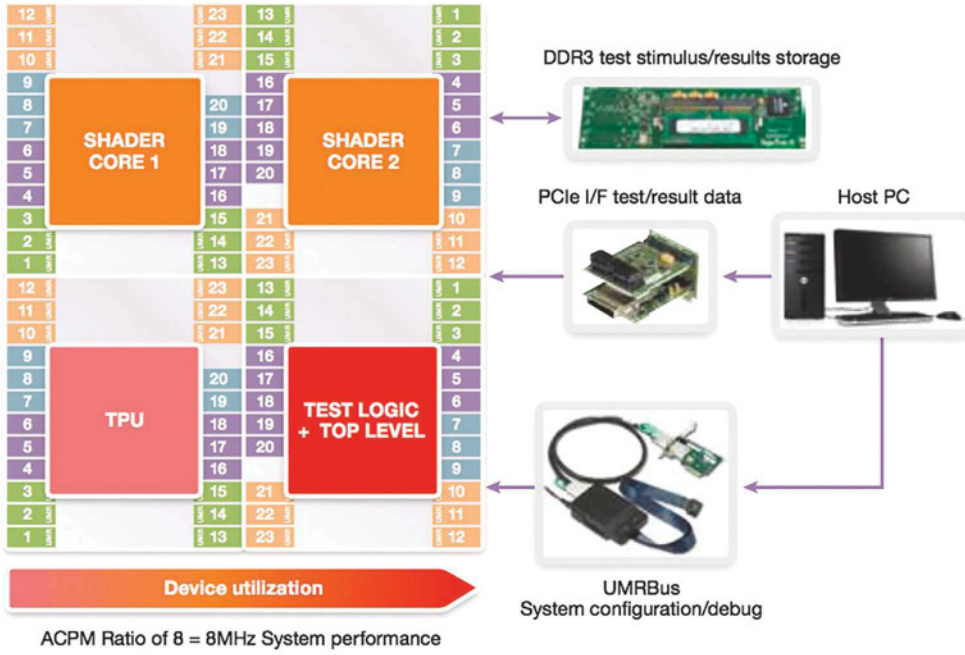


Figure 3: Imagination Technologies PowerVR Series6 on HAPS-70

interconnect capacity on the hardware. One of the key features of the HAPS environment is that the prototype configuration is not constrained by fixed I/O; it can be used by ProtoCompiler too. The team concluded that constraining the multiplexing ratio to 12 would enable the prototype to run at a respectable 7.3MHz.

The additional logic to support the DriverLive Active Video output was merged with the existing test logic, with no impact on the overall FPGA partitioning. The prototype design can easily be modified since ProtoCompiler supports incremental updates without having to re-compile the entire design. Adding the live video output feature gives the Imagination design team a very powerful debug capability – the ability to review moving images in real time at the GPU prototyping stage.

With the prototyping design mapped to just five of the six available FPGAs, the team took the opportunity to optimize for performance. High-speed time-domain multiplexing (HSTDM) I/O sharing increases FPGA interconnection bandwidth. All HAPS-70 connectors support HSTDM, while ProtoCompiler automates the complete HSTDM implementation, including assigning source synchronous clocks, splitting multi-terminal nets for point-to-point HSTDM communication and handling direct and HSTDM net assignment to the HAPS platform.

By using an HSTDM ratio of 24x2 the team improved the performance of the prototype to 12.0MHz. A single engineer spent around half a day to explore the prototype, and a further half-day to implement it.

Compelling Results

The collaboration between Imagination and Synopsys showed how, with the right environment, design teams can use FPGAs to support early prototyping of the largest and most complex GPU devices.

The success of both the PowerVR Series6 and Series6XT prototypes will mean that the Imagination design team is less dependent on the use of test chips to bring new GPUs to market. Early access to physical prototypes enables system validation

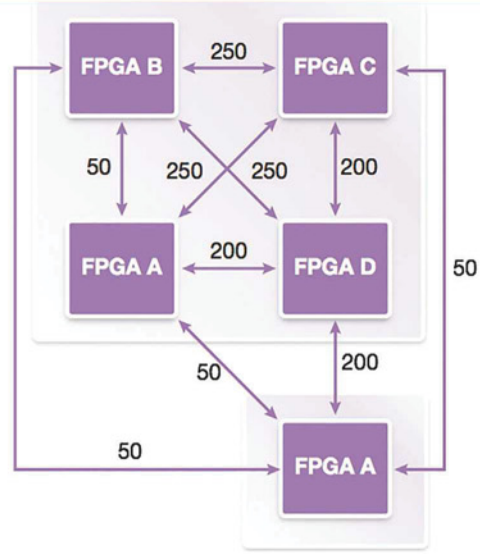


Figure 4: Abstraction flows used to investigate FPGA-to-FPGA interconnect

and earlier software development, and eases hardware-software integration.

The 12MHz performance achieved with the prototyping platform helped Imagination to execute thousands of tests in a matter of hours and provided a platform for early software development. In addition, supporting the video output from the HAPS system allowed the use of real-time, real-world I/O to enable inspection of the correctness and quality of the image processing.

The Synopsys FPGA-based prototyping platforms enabled the team to quickly partition the very large GPU design and additional test infrastructure across multiple FPGAs, and subsequently accommodate changes to the RTL and optimize the performance of the system using high-speed TDM.

The ability to reduce the time to first prototype assists Imagination in bringing new products to market and helps Synopsys's and Imagination's mutual customers when they integrate Imagination GPUs into their SoCs.

Synopsys is working with Imagination to investigate the feasibility of adding extensive configurability to the test infrastructure. This will enable customers to more easily integrate Imagination GPUs within Synopsys design and verification flows.

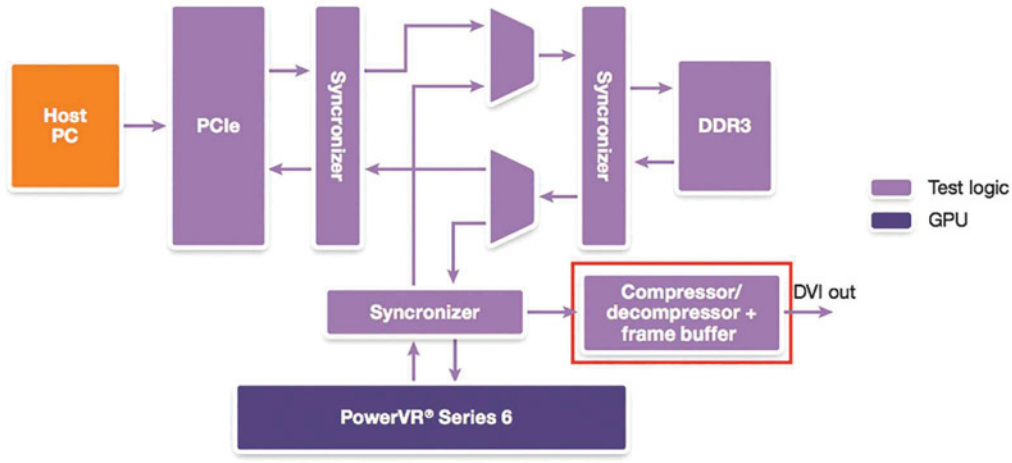


Figure 5: Addition of compress and decompress frame buffer for live video output

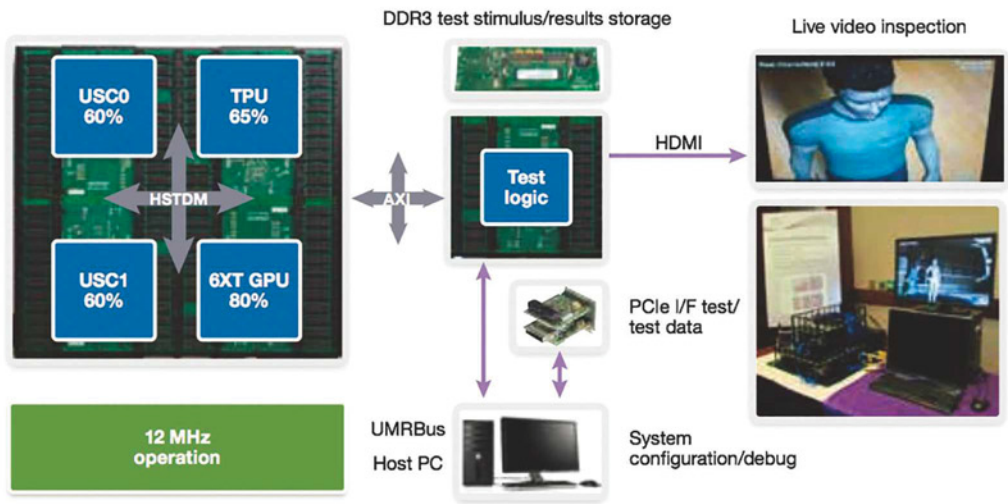


Figure 6: PowerVR Series 6XT on HAPS with DriverLive support

ASIC-COMPATIBLE ALTERNATIVE TO TRADITIONAL FPGA PROTOTYPING TOOLS

JUERGEN JAEGER, PRODUCT MANAGEMENT DIRECTOR FOR FPGA-BASED PROTOTYPING AT CADENCE DESIGN SYSTEMS, PRESENTS A NEW ASIC-COMPATIBLE CONCEPT AS ALTERNATIVE TO TRADITIONAL FPGA PROTOTYPING TOOLS, AND COVERS MEMORY MODELLING, CLOCK TRANSFORMATION, MULTI-FPGA PARTITIONING AND RUNTIME OPTIMIZATION

FPGA-based prototype systems are an integral and indispensable part of the development and verification of digital systems on chip (SoCs) and their embedded software/firmware. However, implementing this type of SoC design in more than one FPGA is a challenging and time-consuming undertaking.

FPGA Prototypes Popularity

FPGA-based prototypes have been around for a long time, but it's only in the last couple of years that this technology has seen such a meteoric rise. The reasons are obvious: it's all about software. ASIC development is no longer the biggest obstacle to reaching the tapeout stage.

Software is the dominant factor in development costs and schedules; software makes a product different and can add a competitive advantage. Consequently, it's important to start the software development and hardware/software integration process as early as possible, long before the actual chip is available. And that's precisely where FPGA-based prototypes come in.

> It's critically important to start the software development and hardware/software integration process as early as possible, long before the actual chip is available

Let's begin by taking a look at the verification tools used in a typical development project (Figure 1).

In the early phases, when the design is still evolving and unstable, a large number of simulations are conducted. But there comes a point when the simulator is simply no longer fast enough and runtimes are too long, which is when simulation accelerators and emulators come into play.

These days, as hardware design becomes more stable, the embedded software development can be started in parallel; this is also the right time to get the FPGA prototypes up and running, to help software developers work more efficiently.

Nothing's Perfect

Sound good? Not so fast!

The biggest challenge with FPGA prototypes is that it takes far too long to implement the ASIC design in multi-FPGAs and get them up and running properly. It can often take from three to six months until the prototype is operational, the main reasons being:

- RTL (Verilog, System Verilog, VHDL) written for an ASIC design can be problematic to compile in FPGAs, and in many cases has to be revised and rewritten. The most common problems which FPGAs are unable to process directly are gated clocks, latches and tristates.
- Memories are another factor: it can take weeks to convert ASIC memories into FPGA memories.
- ASIC designs won't normally fit into a single FPGA, so the design has to be partitioned and, because there are not enough connections between the FPGAs, pin-multiplexing logic has to be added. That's another two to four weeks.
- And once all these modifications are completed, we must verify that the functionality of the original design is still intact, which can take several more weeks.

Before we know it, months have gone by – time that software developers could have made good use of, if only the prototype had been available earlier.

Does it really have to take so long and be so difficult?

Everything's Easier With The Right Tools

The solution is to forget traditional FPGA development methods and tools and switch to a new approach using a method based on solid and efficient ASIC verification procedure.

This approach, introduced in the Protium rapid prototyping system from Cadence, speeds up prototype construction and reduces the time required to achieve a functioning prototype from several months to just a couple of weeks; see Figure 2.

First, compilation is performed with an ASIC synthesis tool which converts all incompatible elements automatically, including gated clocks, latches and so forth. This compilation software also converts all ASIC memories to FPGA memories, again automatically. Both these features save weeks of work.

Partitioning into multiple FPGAs is a fully automatic process, taking just hours or days, depending on the size of the design – another dramatic time-saver.

Before the design goes into the still-time-consuming FPGA place-and-route phase, there is the option of validating performance in a simulator or emulator – a process known as "post-partition validation".

The advantages are clear: instead of having to wait hours for the place-and-route process to finish, functionality can be checked in just a few minutes and corrected if necessary.

By combining these innovative methods and technologies, the FPGA prototype system can now be used productively after just a few weeks as opposed to several months.

High Performance

Generally, when it comes to FPGA prototypes, the faster, the better. This is why the Protium platform has several performance options:

- In fully automatic mode, everything takes place at the touch of a button, right down to generating the FPGA bit file. The result is a functioning prototype within days or weeks, and with a good clock speed.
- Since the software developers are already using the system, the clock speed can be further optimised. This requires knowledge of the design structure in order to eliminate bottlenecks, and typically increases performance up to 50%.
- To achieve speeds of over 100MHz, sometimes necessary in order to operate interfaces such as PCIe or Ethernet directly, the "black-boxing" option can be used. This means isolating the part of the design to work at this speed, optimising it for maximum performance separately from the rest of the design.

All three methods can be combined as required; in the end, it's a question of how much extra effort and expense to put into it, and if the outcome justifies them.

Justifying The Expense

FPGA-based prototype systems have become indispensable to modern-day ASIC and system development; they are the method of choice when it comes to early, pre-silicon software development of digital SoC designs. Some people argue that this approach is too difficult and takes too long, and that can certainly be true if wrong methodology and wrong tools are used.

On the other hand, the results do justify a certain amount of extra expenditure, which can be substantially reduced by using the right tools and the right prototyping systems. ●

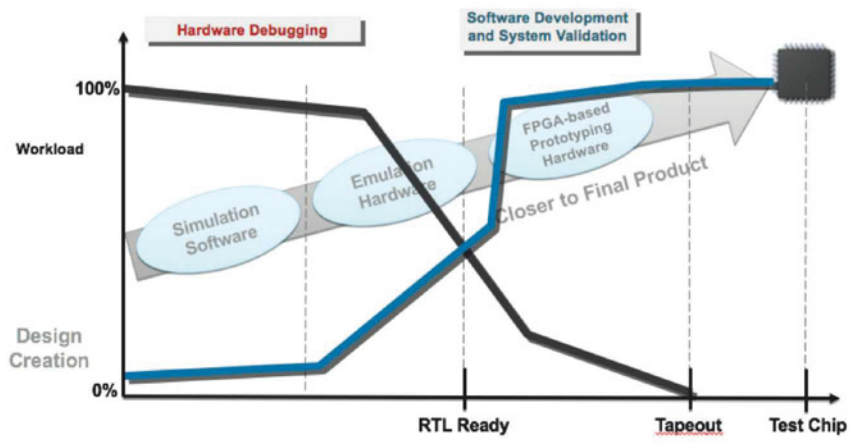


Figure 1: Typical verification tools in ASIC development

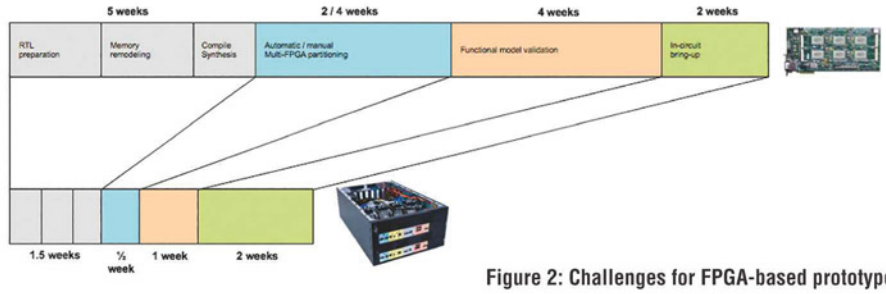
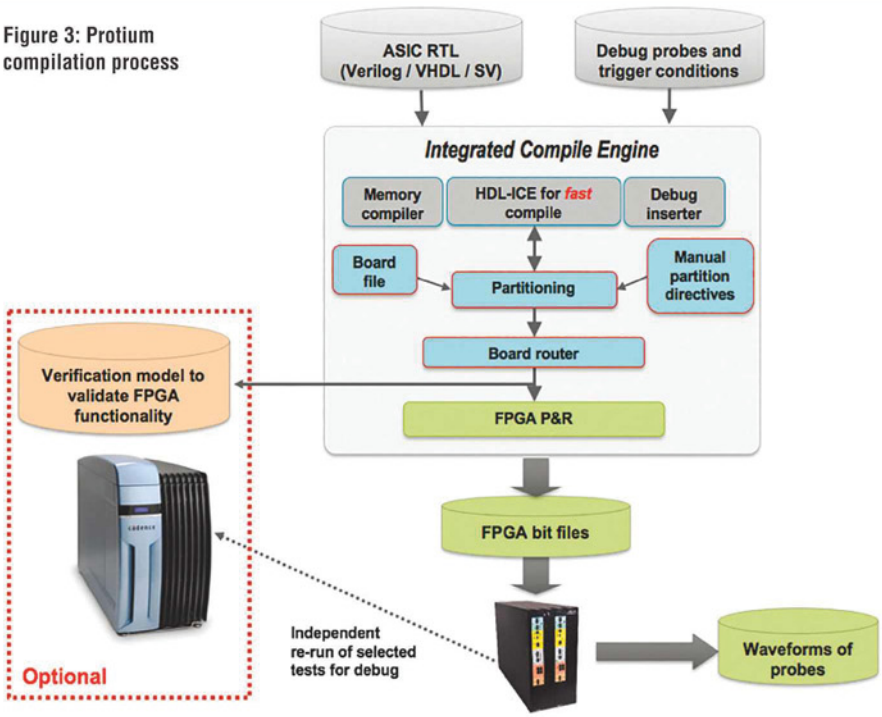


Figure 2: Challenges for FPGA-based prototypes

Figure 3: Protium compilation process



THE REASONS FOR SWITCHING AND ROUTING SOFTWARE

ROUTING AND SWITCHING SOFTWARE OR LOW-LEVEL PROGRAMMING – WHICH IS BETTER FOR SWITCHING APPLICATIONS, ASKS **NICK HICKFORD**, UK SALES FOR PICKERING INTERFACES

Within small switching system configurations or when utilizing single-switch modules, the designer typically applies device drivers with the provided API to control the relays. Simple CLOSE and OPEN commands with additional parameters like module or channel numbers control the required relays.

The user must always take care to avoid shorts or malfunctions, even when performing simple switching tasks. If there are many relays involved, the risk of error increases significantly.

Example

Our example (see Figures 1 and 2) shows a four-wire resistance measurement where the digital multimeter (DMM) and the device under test (DUT) are connected to the matrix's X-axes, turning a simple switching setup into something more complex.

For a correct measurement, all four signal paths between the DMM and DUT must be properly set; meaning all crosspoints on all four Y-axes must be closed at the correct X position. Even with one wrong would end up in erroneous measurements or possible shorts to adjacent unit under test (UUT) terminals.

On a further example, an additional four-wire resistance measurement takes place on the second matrix. Two two-pole relays are cascading both matrices by interconnecting Y-bus 1 to 4. Now, even more relays distributed on three different modules have to be programed properly to achieve correct measurement.

It is obvious that the complexity of the switching system increases when multiple modules are configured and interconnected carrying signals routed throughout the system. For this reason switching and routing software's role is to manage configurations of any complexity, easily, securely and safely.

Tecap Switching

Tecap switching virtually describes any switching architecture, processes and stored project data for switching and routing at runtime. A multivendor and platform-independent switch module library provides the models which are added to the project. In addition, the physical interconnections as well as the endpoints have to be defined. Endpoints are the boundary of the system where measurement and stimuli equipment and all the UUT access points are connected.

By calling point-to-point or point-to-multipoint functions, the routing is processed and the required relays are controlled to establish a signal path between these endpoints. The router will never interfere with existing routes, and will find an alternate bypass or will terminate with an error message if not successful.

Continuing the first example and extending it to a four-wire

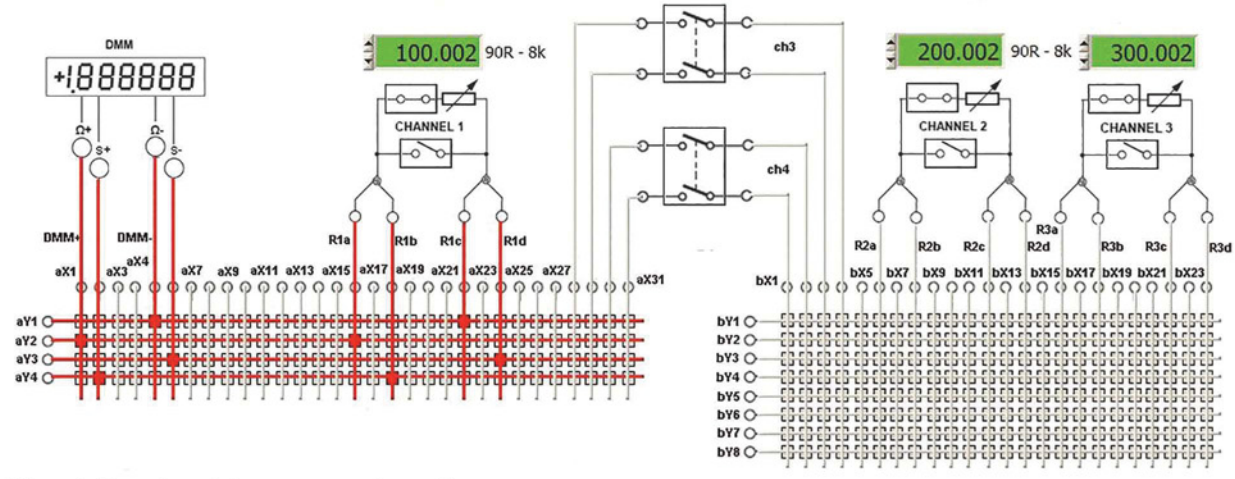


Figure 1: Four-wire resistor measurement example

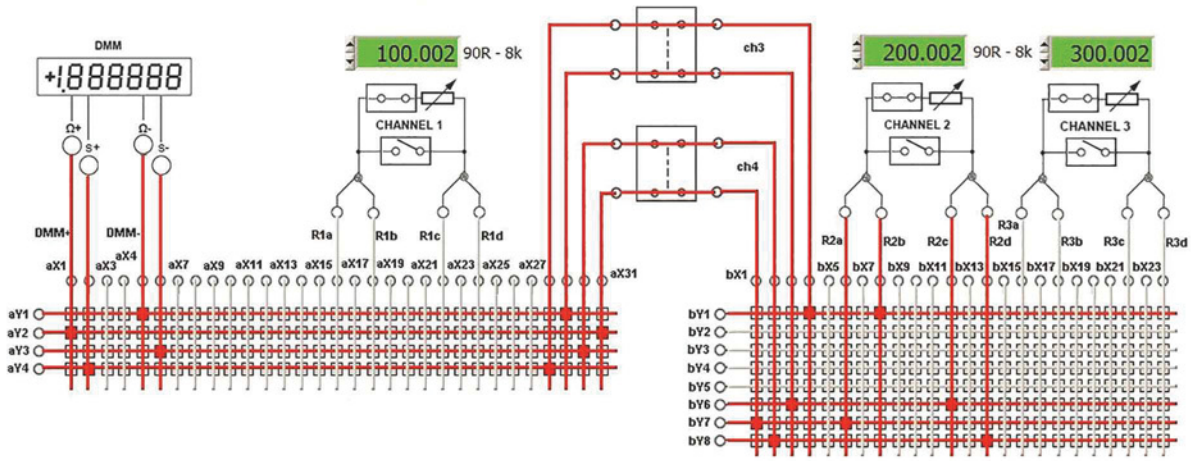


Figure 2: DMM connected to R2 via DPST relays

resistance measurement DMM to R2 (Channel 2 in Figure 2), there are four routes to be established and therefore four CONNECT functions to be called. When using the device driver, 18 CLOSE commands have to be sent to achieve the same setup. Besides the increasing number of commands, good knowledge of the system is required to understand which crosspoints have to be used.

- **Connect Endpoints (DMM+, R2a) - to disconnect: Disconnect Endpoints (DMM+, R2a), etc.**
- **Connect Endpoints (s+, R2b)**
- **Connect Endpoints (DMM-, R2c)**
- **Connect Endpoints (s-, R2d)**

Listing 1: Tecap switching with auto-routing

- **Close Crosspoints (module1, y1, x1) - to disconnect: Open Crosspoints (module1, y1, x1), etc.**
- **Close Crosspoints (module1, y2, x2)**
- **Close Crosspoints (module1, y3, x5)**
- **Close Crosspoints (module1, y4, x6)**
- **Close Crosspoints (module1, y1, x29)**
- **Close Crosspoints (module1, y2, x31)**
- **Close Crosspoints (module1, y3, x30)**
- **Close Crosspoints (module1, y4, x28)**
- **Close Channel(module2, ch3) - to open: Open Channel (module2, ch3) , etc.**
- **Close Channel(module2, ch4)**
- **Close Crosspoints (module3, y1, x4)**
- **Close Crosspoints (module3, y6, x3)**
- **Close Crosspoints (module3, y7, x1)**
- **Close Crosspoints (module3, y8, x2)**
- **Close Crosspoints (module3, y1, x14)**
- **Close Crosspoints (module3, y6, x6)**
- **Close Crosspoints (module3, y7, x8)**
- **Close Crosspoints (module3, y8, x12)**

Listing 2: Classic device driver

If frequently recurring routes are required it might be more efficient to create fixed routes instead of calling endpoint-to-endpoint connections. Those routes can be grouped together to make connecting and disconnecting even simpler.

Each separate route holds an attribute called auto-route or static-route, and thus determines in advance whether a route selects an independent path based on the current switch status or a static one, which might fail if an existing route is blocking the way.

For the R2 four-wire measurement four single routes (R2_DMM-, R2_DMM+, R2_DMMs+, R2_DMMs-) are grouped (GRP_DMM_R2) and switched by single Connect Route Group command:

- **ConnectRouteGroup (GRP_DMM_R2) – to disconnect: DisconnectRouteGroup(GRP_DMM_R2)**

Tecap switching handles individual relay control as well: a relay group, which is a group of one or more relays, is called by function:

- **ConnectRelayGroup (RELAYGRP) – to disconnect: DisconnectRelayGroup(RELAYGRP)**

For example, relay group RELAYGRP contains the relay channel information of crosspoints Y2/X10, Y2/X11, Y3/X10, Y3/X11.

Short Circuit Detection (SCD)

A very important aspect when applying routing software is short circuit detection. If not handled correctly, routing might create shorts in the switching system.

In the configuration of Figure 4, there are two switching systems interconnected via a normally closed relay. With an existing route established between A and B, a second route from C to D would cause an unwanted short between the two systems.

Tecap switching short circuit detection (SCD) prevents this condition, returns an error message and will not switch this second route.

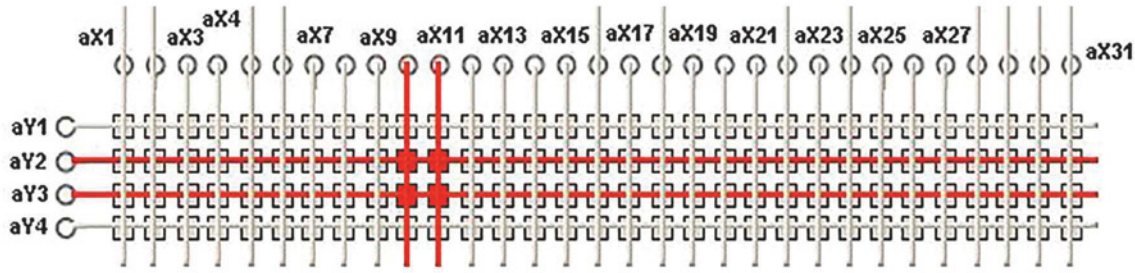


Figure 3: Switched relay group of four relays

Another, more obvious example (see Figure 5) illustrates short-circuit detection when using multi-pole relays. Two matrices are interconnected on their Y1 and Y2 lines via a two-pole relay. The blue and green routes have already been switched. Another signal path from X1 left side to X3 right side would allow a route over one pole of the two-pole relay, but Tecap switching prevents the closing, as on the first pole the green and the blue existing routes would then inadvertently be shorted.

Signal Isolation

If the switching system's signal leads are not isolated and, therefore, used for routing, it can lead to unintended connections and thus to short circuits. Figure 6 illustrates this within the following task:

establish two independent connections Y1-Y4 and Y2-Y3

The router searches the best unused path and switches the crosspoints, regardless of what is connected. Figure 6a shows an unwanted connection to the DMM+ and s+ leads, because at that point the router does not know which signals are applied to given nodes. Figure 6b shows the routes on absolute free paths without any connections to the outside world. This happens because X1, X2, X5 and X6 (used for the DMM) are defined as "isolated" in the system configuration.

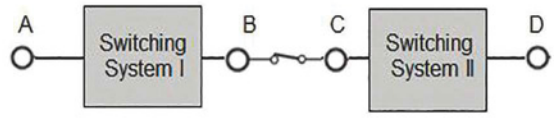


Figure 4: Two independent switching systems interconnected can cause shorting

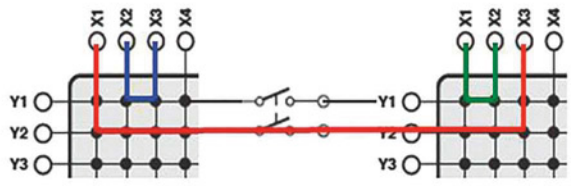


Figure 5: Short circuit detection (SCD) avoids two-pole switching on red path, X1 left to X3 right

Unbeatable

For a smooth and easy implementation of switching applications with minimal coding, routing and switching software is unbeatable compared to low-level programming. A correct setup helps minimize the risk of short-circuit switching.

The performance speed of routing software should be considered separately. Such systems will always be slower compared to optimized direct programming, especially when used in small switching configurations with one switch module or a very few. However, these delays are small, in the order of milliseconds. ●

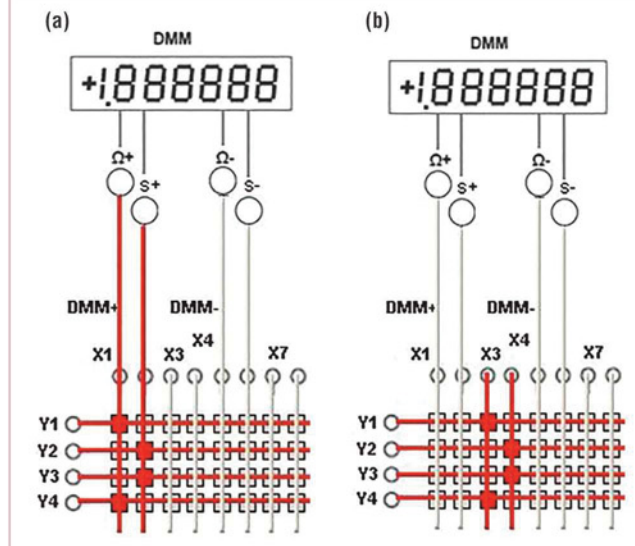
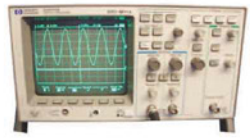


Figure 6: (a) Unwanted connection to the DMM+ and s+ leads; (b) the routes to free paths without any connections to the outside world

HP 34401A Digital Multimeter 6 ½ Digit



HP 54600B Oscilloscope Analoque/Digital Dual Trace 100MHZ

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HP83731A	Synthesised Signal Generator 1-20GHZ	£1,800
HP8484A	Power Sensor 0.01-18GHZ 3nW-10uW	£75
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Farnell AP60/50	PSU 0-60V 0-50A 1KW Switch Mode	£195
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Farnell B30/10	PSU 30V 10A Variable No Meters	£45
Farnell B30/20	PSU 30V 20A Variable No Meters	£75
Farnell XA35/2T	PSU 0-35V 0-2A Twice Digital	£75
Farnell LF1	Sine/sq Oscillator 10HZ-1MHZ	£45
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Fluke 99B	Scopemeter 2 Channel 100MHZ 5GS/S	£125
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Solatron 7075	DMM 7 1/2 Digit	£60
Solatron 1253	Gain Phase Analyser 1mHZ-20KHZ	£600
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MODELING A STACKED SIX-PORT TRANSFORMER FOR A QUADRATURE OSCILLATOR

MINGLIN MA, CHENGWEI LI, YUAN CHEN, ZHIJUN LI AND **XIANGLIANG JIN** FROM XIANGTAN UNIVERSITY IN CHINA PRESENT A NEW EQUIVALENT-CIRCUIT MODEL FOR STACKED SIX-PORT TRANSFORMERS ON SILICON

Any modern communication systems, such as zero-IF receivers, image rejection architectures, clock and data recovery (CDR) systems, and QPSK modulators require oscillation with 90° phase difference (I/Q signals), making quadrature oscillators their indispensable part.

The performance of quadrature oscillators can affect a system's overall performance, so a lot of effort goes into the design of low voltage, low power, low cost, low phase noise, highly integrated and robust quadrature oscillators. Some circuits and methods used in quadrature signal generation include poly-phase RC-CR filters, ring oscillators, frequency dividers and harmonics coupling.

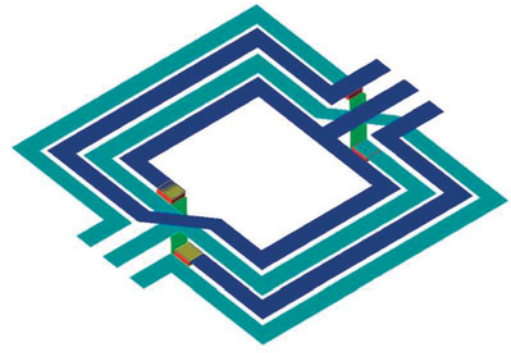


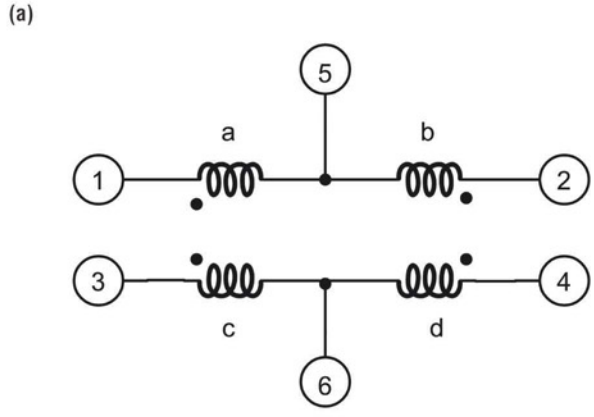
Figure 1: The 3D view of the transformer

Harmonics-Coupling Quadrature LC Oscillators

Due to the low phase noise and low power consumption, harmonics-coupling quadrature oscillators with LC tanks have received a lot of attention recently.

Harmonics-coupling quadrature LC oscillators are usually made of coupling two identical negative resistor LC oscillators in which oscillating signals are injected from one oscillator to the other and vice versa.

Quadrature oscillators based on coupling the first harmonics of two identical oscillators by transistors suffer from a tradeoff between quadrature accuracy and phase noise. Moreover, the coupling transistors increase power



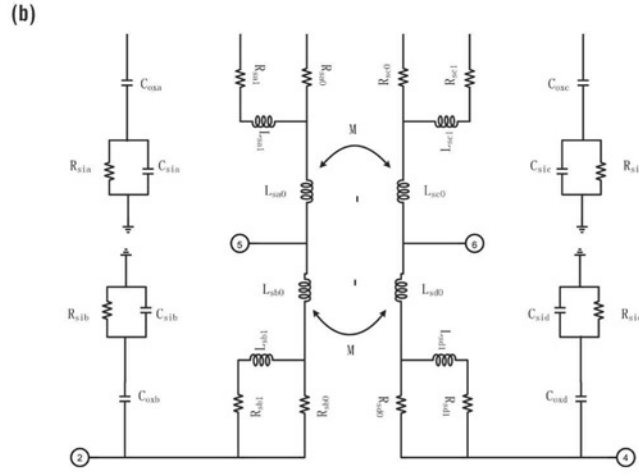


Figure 2: (a) Six-port transformer;
(b) The equivalent circuit model of the six-port transformer

COMPONENT	VALUE	COMPONENT	VALUE
$L_{sa0,sb0}$ [nH]	3.69	$R_{sa0,sb0}$[ohm]	20.8
$L_{sc0,sd0}$[nH]	3.48	$R_{sc0,sd0}$[ohm]	21.2
$L_{sa1,sb1}$[nH]	0.47	$R_{sa1,sb1}$[ohm]	2.6
$L_{sc1,sd1}$[nH]	0.43	$R_{sc1,sd1}$[ohm]	2.8
$C_{oxa,oxb}$[fH]	49.4	$R_{sia,sib}$[ohm]	189.3
$C_{oxc,oxd}$[fH]	53.5	$R_{sic,sid}$[ohm]	188.4
$C_{sia,sib}$[fH]	33.6	M[nH]	3.4
$C_{sic,sid}$[fH]	34.3		

Table 1: Transformer model parameters

consumption. On the other hand, quadrature oscillators based on coupling the second harmonics of two identical oscillators by transformers occupy a large chip area. Quadrature oscillators based on coupling the second harmonics of two identical oscillators by capacitors also need a high supply voltage.

A popular architecture referred to in the literature nowadays is the transformer-based oscillator. This type oscillator was introduced to decrease die area and phase noise, and expand the tuning range of the LC-oscillator through dual-mode implementation.

Several studies have focused on transformer-based quadrature oscillators. A quadrature oscillator stacked with a divide-by-two has been proposed, but it operates at double frequency. A transformer-based gate-coupled quadrature VCO was also proposed, but here using four transformers makes the chip area large.

We suggest using a mutual compensation structure to improve phase noise performance.

Modeling Of The Six-Port Transformer

Transformers are often modeled as four-terminal devices with two terminals for the primary and two for the secondary. In RF integrated circuits (RFICs) however, transformers are frequently used differentially or in balun applications with centre tap on the primary and/or the secondary. Therefore, a more useful model needs to include six terminals, including the centre taps on the primary and the secondary.

To minimize the chip area, the transformer is arranged in a stack configuration (see Figure 1). It was simulated in a 180nm 1P6M CMOS process with substrate resistivity of about 10Ω/cm and top metal thickness of 3µm, with line width and line spacing of 15µm and 1.5µm respectively.

The model of the six-port transformer is shown in Figure 2. Each winding is divided into two impedance segments, with the primary ones indicated by symbols a and b, and the secondary by c and d. There is magnetic coupling between the primary and secondary segments.

The ladder elements ($L_{sa1, sb1, sc1, sd1}$, $R_{sa1, sb1, sc1, sd1}$) represent the skin and proximity effects. There is also shunt admittance (C-R-C) to ground attached to each terminal. $R_{sia, sib, sic, sid}$

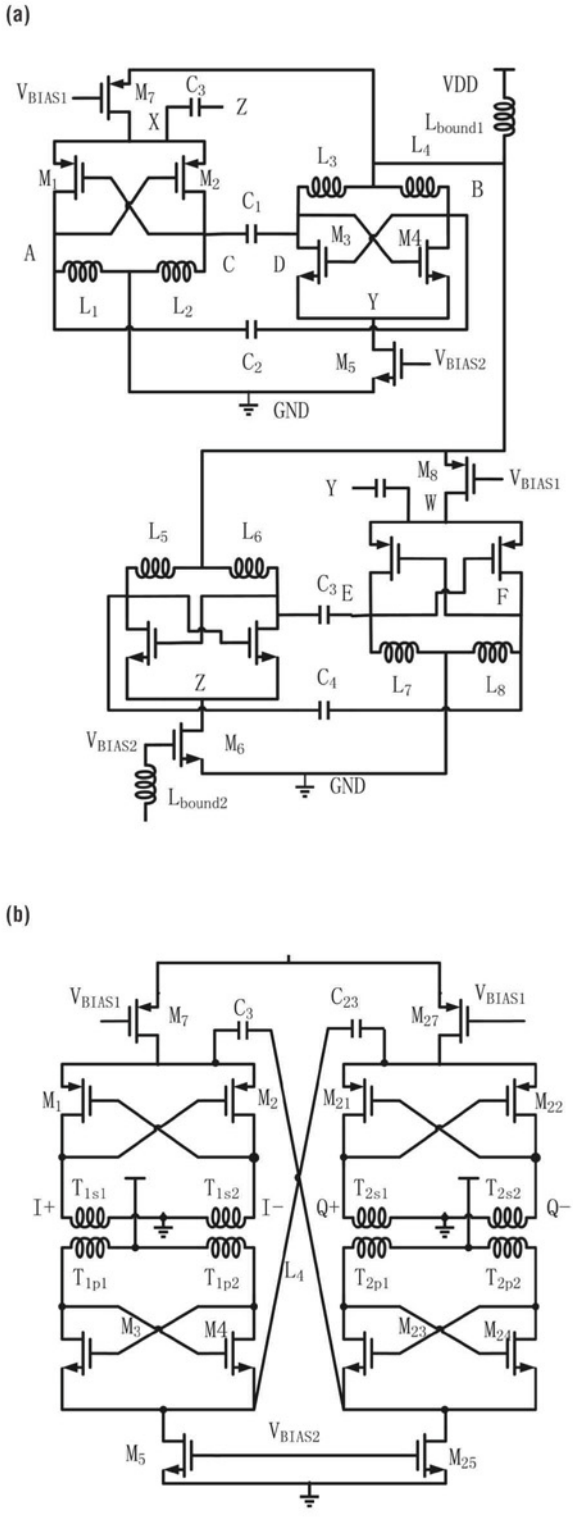


Figure 3: (a) Schematic of the QLCO coupled by capacitors; (b) Transformer-based low voltage, low phase noise, quadrature oscillator

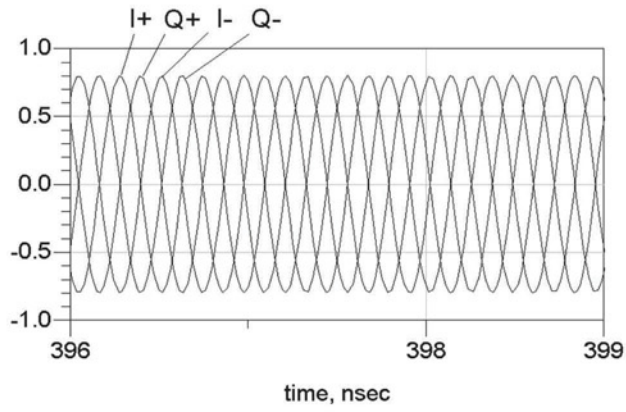


Figure 4: Simulated quadrature outputs of this oscillator based on the transformers

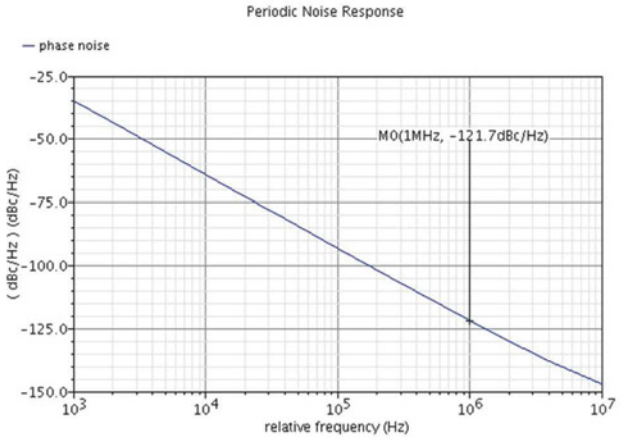


Figure 5: Phase noise of a quadrature oscillator based on six-port transformers

represents the substrate resistance, $C_{sia,\ sib,\ sic,\ sid}$ the substrate capacitors and $C_{oxa,\ oxb,\ oxc,\ oxd}$ the oxide capacitance between the spiral and the silicon substrate. The transformer behavior becomes more complex with multiple ports, and more intricate electrical and magnetic interactions between the windings' segments.

Model generation begins with running EM simulations of the six-port transformer to obtain the device parameters; the model is directly extracted from these simulations, with no optimization or tuning. With this model, we can simulate the quadrature oscillator based on a six-port transformer; its parameters are shown in Table 1.

The Circuit

To decrease the supply voltage of the quadrature oscillators based on coupling the second harmonics of two identical oscillators, a coupling quiet quadrature oscillator has been proposed as shown in Figure 3a. But in this oscillator, eight inductors ($L_{1\text{-}8}$) and four capacitors ($C_{1\text{-}4}$) occupy a very large die area.

> We suggest using a mutual compensation structure to improve phase noise performance

We suggest a quadrature oscillator composed of two LC oscillators based on stacked six-port transformers. Its topology is shown in Figure 3b.

For one LC oscillator, the top and bottom parts are coupled by a six-port transformer (composed of $T_{is1,2,}$ $T_{ip1,2}$) with center tap, so they can be biased independently at low voltage. For the whole quadrature oscillator, the left and right parts are coupled by two capacitors ($C_{3,}$ C_{23}) to generate the quadrature outputs without any noise or power consumption. This oscillator uses a transformer resonator based on establishing resonating tanks at both sides of the transformer, each with the same capacitance.

Consider an ideal transformer with primary and secondary inductance L_p and L_s ($L_p \approx L_s \approx L$), each with quality factor Q ($Q_s \approx Q_p \approx Q$) and coupling factor $k \approx 1$. The resonant frequency of this tank is:

$$f_o = \frac{1}{2\pi\sqrt{(L+M)C}}$$

where C is the parasitic capacitance and M the mutual inductance (here $M \approx L$). For $L_s \approx L_p$ and $k \approx 1$ ($M \approx L$), the transformer-based resonator acts as an LC resonator with 2L inductance. However, the Q of the ideal transformer-based resonator is double that of a standard LC resonator with L and the same inductor quality factor.

Analysis

Our quadrature oscillator operates at 2.15GHz. At 0.8V supply voltage, its simulated phase noise is -121.7dBc/Hz at 1MHz offset from the carrier, as shown in Figure 5.

The complementary structure offers higher transconductance for a given current, which results in faster switching cross-coupled differential pairs. It also offers better rise and fall time symmetry, which results in a smaller $1/f^3$ noise corner.

The NMOS and PMOS cross pairs are biased independently, so this quadrature oscillator can operate at a low voltage. The stacked structure of the six-port transformer results in a small die area. This, combined with its low supply voltage, low phase noise, low cost and accurate 90° quadrature outputs, makes this oscillator attractive for many applications. ●

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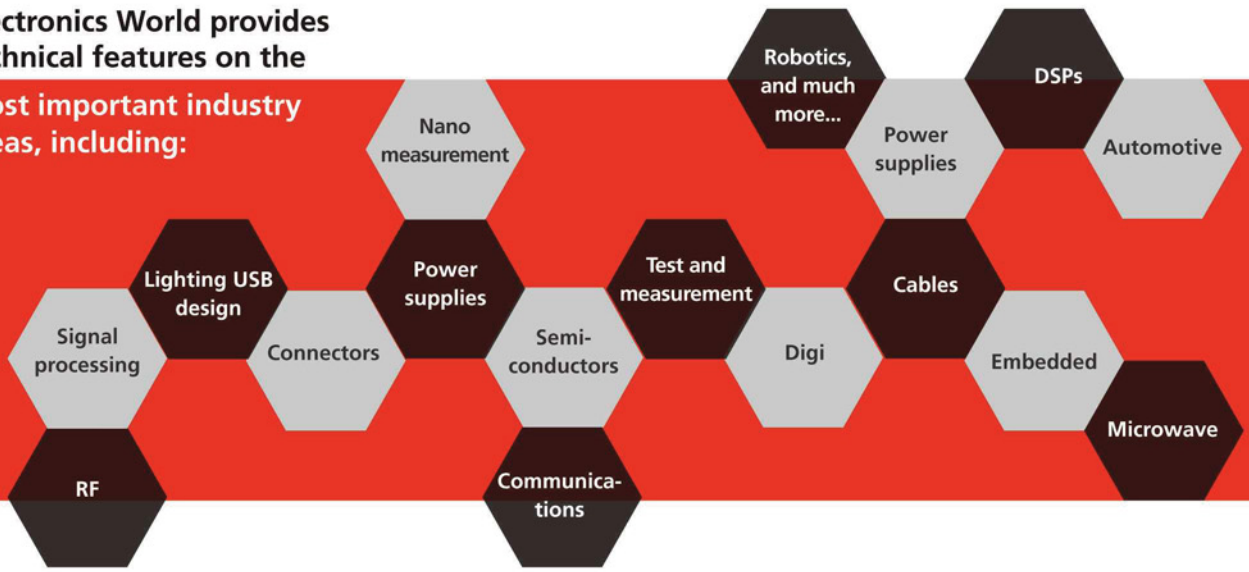

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THE ASONIKA SYSTEM – A NEW ELECTRONICS DEVELOPMENT TOOL

A.S. SHALUMOV PROFESSOR AT THE INTERNATIONAL INFORMATIZATION ACADEMY, **E.O. PERSHIN** FROM THE NANOMODEL R&D CENTRE AND **O.E. KULIKOV** OF ASONIKA, ALL IN RUSSIA, DISCUSS HOW THE THERMAL, MECHANICAL AND ELECTROMAGNETIC ASPECTS OF ELECTRONIC DESIGN CAN BE MADE EASY WITH A SPECIFIC PLATFORM

All modern systems use electronic components and circuits – it's almost inevitable. But for all their prevalence, if one of these electronic components doesn't work, then it's most likely that the whole system won't function either.

Vibration, shock, heat, electromagnetic fields, radiation and other external factors can all impair the operation of electronics. That's why tests are a very important part of electronic equipment manufacture.

Tests, however, are costly, can take a long time and yet still not cover all the conditions an electronic system might go through in practice. Only too often we hear of high-impact disasters including spacecraft crashes, such as GLONASS, Fobos-Grunt, Meridian, PROTON and others. It doesn't help that there are hardly any spacecraft electronic system simulation tests available covering a very wide range of factors that may affect these systems in real life. It is also impossible to carry out spacecraft electronics simulation tests without specialized software that tests not just the electronics and its components, but also the materials they are made of.

To counteract the lack of a comprehensive testing environment, we developed a computer-aided equipment reliability and quality assurance system, which we call ASONIKA. With it it's possible to foresee and prevent most – if not all – potential malfunctions of the not-yet-manufactured electronic system. Test results are normally available within hours, and include information about critical errors (helping to fix them during the design stages); ways of improving the design processes; the complete production life-cycle stages of system design, from marketing and research, to use in accordance with the Continuous Acquisition and Life cycle Support, or CALS, standards; all the potential factors that might influence the system (from mechanical and thermal to electromagnetic and gamma-rays radiation); and so on.

At the 2009 engineering exhibition in Saint Petersburg, Russian President Putin showed interest in the importance of CAD and simulation software used in the design and development of radio-electronic facilities (REF), and aerospace and defence equipment. President Putin learned of the ASONIKA system, emphasized its importance to home-grown projects so much so that he recommended that the subject ministries should support its further development.

Now, by Presidential decree, ASONIKA will be used for military and special mission designs.

> ASONIKA helps advance to a conceptually new technical information level, which expands production output, cuts product rejects and failures, and reduces production costs

Materials And Methods

The ASONIKA system is designed to solve four main issues relating to modern REF development:

- Prevent possible malfunctions early on in the design, thanks to complex modelling;
- Provide safety for those on-board aircraft, thanks to complex computer-aided analyses of aircraft control systems and their behaviour in different circumstances and critical modes;
- Reduce time and costs associated with the design process, thanks to simulation and predictive software;
- Automate the REF model's workflow through different software, which includes background systems and data control, as well as the entire system's life-cycle.

In addition, the ASONIKA software takes into account the wear, tear and aging processes of the REF. It then generates a list with all the performed simulations and calculations. An electronic virtual experimental model is created, which can easily be ported into various manufacturing stages.

ASONIKA also allows the integration of other, external design packages, such as those from Mentor Graphics and Altium.

The ASONIKA modelling tests are presented as graphs, easily ported into the equipment's experimental model, and in tune with the ISO 10303 STEP standard. This data is used for further REF life-cycle stages analysis and improvements.

The ASONIKA Sub-Systems

Currently, the ASONIKA system consists of thirteen subsystems:

1. ASONIKA-M, REF standard design unit for analyzing shocks;
2. ASONIKA-M-SHKAF, REF standard design cabinets and analysis of shock and other mechanical stresses;
3. ASONIKA-M-3D, the creation of a three-dimensional frame structure and analysis of its durability under stress, made with platforms such as ProEngineer, SolidWorks and other CAD systems in the IGES and SAT formats;
4. ASONIKA-V, construction and analysis of the REF's mechanical stability, assembled with vibration isolators;
5. ASONIKA-T, analysis of thermal characteristics;
6. ASONIKATM, analysis of REF printed circuit assemblies under thermal and mechanical stresses;
7. ASONIKA-R, computer-aided design and analysis of REF electronic components' working modes (EC);
8. ASONIKA-B, analysis of REF reliability, considering its real-life working modes;
9. ASONIKA-BD, REF's electronic components and their materials reference database with physical, mechanical, thermal, electrical and reliability parameters;
10. ASONIKA-ID, identification of optimal parameters for the REF model;
11. ASONIKA-UST, analysis of the stability and reliability of the REF printed circuit assemblies and electronic components;
12. ASONIKA-EMC, analysis of the REF electromagnetic compatibility;
13. ASONIKA-UM, REF modeling.

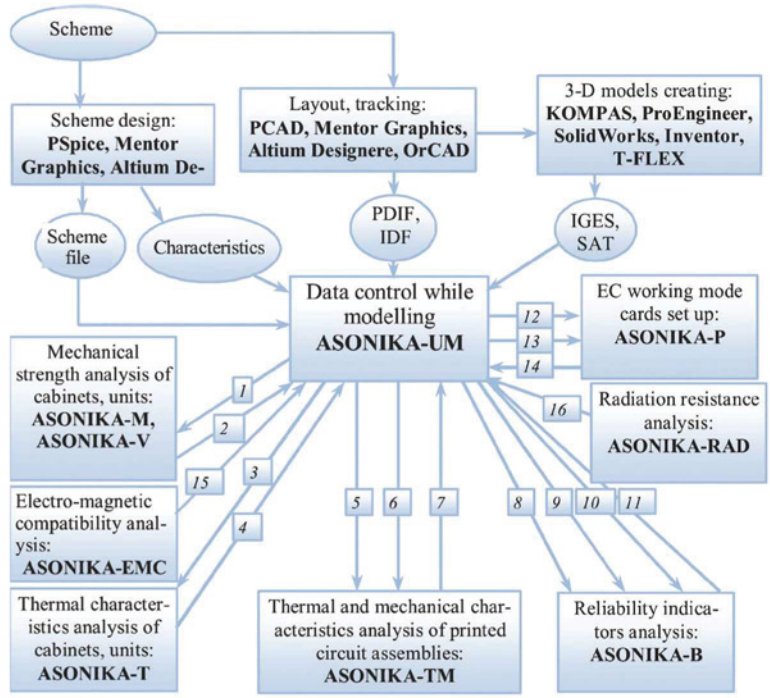

Figure 1: Computer-aided ASONIKA structure

The ASONIKA system also includes the following converters for certain CAD systems:

- ASONIKA-R, a system integration module for PSpice schemes;
- ASONIKA-B for integration with Mentor Graphics and Altium Designer systems;
- ASONIKA-TM, a system integration module for printed circuit assemblies with PCAD, Mentor Graphics and Altium Designer;
- ASONIKA-M or ASONIKA-M-3D, 3D model integration module for KOMPAS, ProEngineer, SolidWorks, Inventor and T-FLEX systems in the formats IGES and SAT.
- An REF radiation stability subsystem, ASONIKA-RAD, is to be developed.

The ASONIKA structure is shown in Figure 1.

A specialist graphics editor creates an REF model, which is then saved in the projects database. PCAD output files in PDIF format or Mentor Graphics and Altium Designer IDF formats are saved either in ASONIKA-UM or sent to an environment such as AUTOCAD, KOMPAS, ProEngineer, SolidWorks, Inventor or T-FLEX for drawings. ASONIKA-M and ASONIKA-V further analyze the mechanical processes of the REF cabinets and units, followed by ASONIKA-T analyzing the thermal processes.

Modelling results are also saved in ASONIKA-UM, and printed circuit assembly drawings and their specifications, as well as PDIF and IDF files, are sent to ASONIKA-TM for more complex thermal and mechanical analysis. ASONIKA-T handles the air temperature values.

The REF's list of electrical properties, temperature, mechanical and thermal stresses, electromagnetic and potential gamma-rays radiations are all saved in ASONIKA-UM, together with the results of the system's overall stability analysis by subsystem ASONIKA-B.

To work with the ASONIKA system a designer does not need special training, since the processes are simple enough, by just inputing the information presented in drawings in the language available to the designer. For example, information input of a very sophisticated cabinet can only take 30 minutes, with the other process analyses completed within a day.

Improved Processes

The aim of the ASONIKA system is to increase work efficiency of companies' structural departments, bring them into compliance with modern standards, reduce dependence on science-based REF development and increase the reliability of complex REF.

Implementation of this program will help save on resources by the sheer reduction in the number of tests. ASONIKA helps advance to a conceptually new technical information level, expands production output, cuts product rejects and failures, and reduces production costs. ●

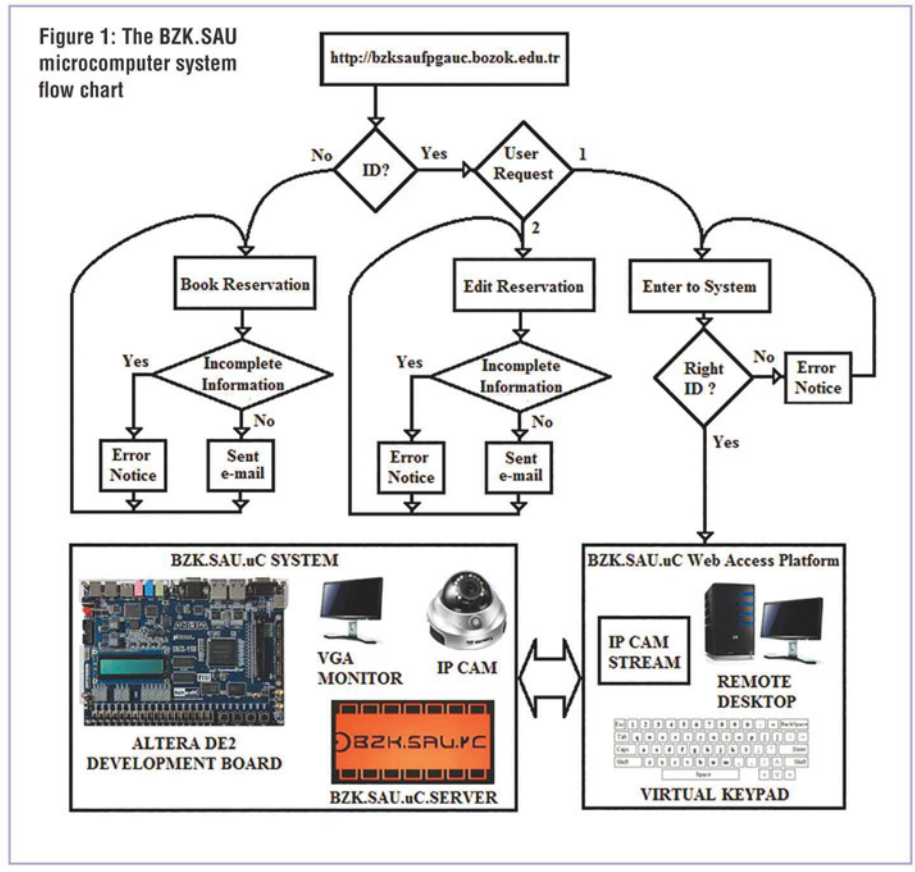

Figure 1: The BZK.SAU microcomputer system flow chart

BY **HALIT OZTEKIN, M. SERDAR BASCIL** AND **FEYZULLAH TEMURTAS** FROM BOZOK UNIVERSITY, AND **ALI GULBAG** FROM SAKARYA UNIVERSITY IN TURKEY

REMOTE E-LABORATORY PLATFORM FOR AN FPGA-BASED MICROCOMPUTER SYSTEM

Field programmable gate arrays (FPGAs) are digital integrated circuits made up of programmable logic blocks and interfaces. They can be configured after manufacture, which is why designers find them very useful in creating systems around them.

We designed the BZK.SAU.FPGA10.0 and BZK.SAU.FPGA10.1 microcomputer architectures based on FPGAs to help students learn about programming and electronic design.

In the literature, educational purpose studies are often combined with remote access platforms, so users can access systems any time from anywhere – even from home – with only an Internet link, and operate and test their own designs. Some of these studies are based on client/server architectures, others on remote desktop connection architectures, and then there are those that use client/host architectures with a web access platform – which our study is based on.

> We used the Altera Cyclone II development board, which we found to be an excellent vehicle for learning about digital logic, computer organization and FPGAs

Our remote access platform is typically established on a host computer and interfaced with Microsoft Visual Studio.NET platform – a visual interface for executing assembly code that's been written remotely.

Web Access Platform

We used the Altera Cyclone II development board, which we find to be an excellent vehicle for learning about digital logic, computer organization and FPGAs. In addition, we used a VGA monitor, an IP-based camera and a serial port. Those who work remotely can try their designs by booking a reservation via the web. A flow chart of the system is shown in Figure 1.

Users who access the system's home page can choose from two options, depending on their identification code (ID), or login password. The ID allows to create an appointment by going on to the "Book Reservation" page. The required fields are marked with *; incomplete information results in an error notice; otherwise, the system prepares an ID and sends it to the user's e-mail account.

Users with IDs can select from two options: first, they can edit their reservation by going to the "Edit Reservation" page, where they can update or cancel an appointment with the system. Any update of this kind creates a new ID, which is sent directly to the user's email account. Aborting an appointment is achieved with the "Cancel Reservation" button.

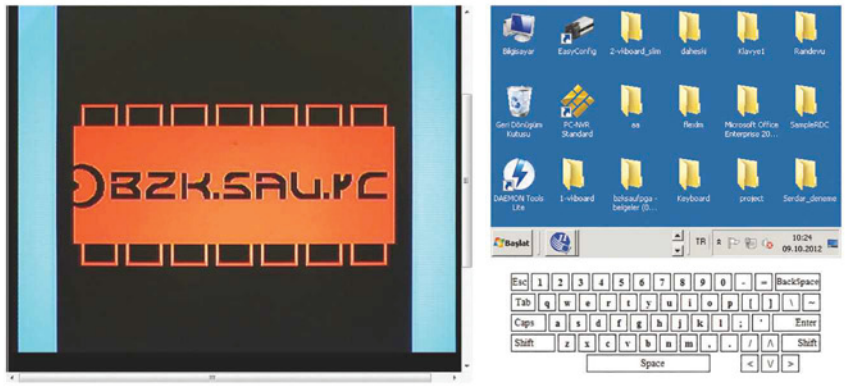

Figure 2: BZK.SAU.uC web access platform

Second, users can access the system directly via the "Enter System" page.

System Structure

We created our platform with Microsoft Visual Studio 2008; it consists of three different applications, as shown in Figure 2. At the left of the page is the camera stream from the VGA monitor that shows the system running in real time. At the upper right is the host remote desktop connection, and at the bottom is the virtual keyboard application which helps enter commands into the microcomputer.

After logging in, users can run "Quartus (64-bit)" installed on the host to transfer their files. They can also trace their work step by step with the real-time camera stream.

Users can create a variety of applications, and test them. When their time booked on the system runs out, the system automatically switches off. This has been optimized for the BZK.SAU.uC (shown in Figure 3) to create a complete virtual environment.

The camera is located in front of the VGA monitor, continuously transferring the monitor's video stream to the host, which is connected to the FPGA board. The host computer transmits this stream to all users via the Internet. Also, the virtual keyboard sends written assembly codes, first to the host, then to the FPGA board, via the RS232 protocol. The results are then shown on the VGA monitor.

This basic cycle is continuous; the remote desktop connection is used to configure the FPGA board with Quartus.

Application Example

A 16-bit register is created (PC-Register), which has LDA, Inc, Decr, and Clr with VHDL. Written register code is copied to the host's remote desktop. The "BZK.SAU.FPGA.uC" folder opens and "BZK_SAU_FPGA.gpf" runs. The Quartus program then starts and shows up on the screen (see Figure 4).

The "Project" > "Add" path adds the written register code to the project.

"File" > "Create/Update" > "Create Symbol Files for Current File" path converts this code file into a symbol file.

The symbol file is then added to the "BZK_SAU_FPGA.bdf" design and tied up to the "User-Defined Register" zone, as seen in Figure 4.

Double-clicking the "Sys_Usr_Reg_Ctrl" acts as the control task between the Register_Interface unit and the user register in "BZK_SAU_FPGA.bdf" (with its least significant bit set to 1, as shown in Figure 5).

Lastly, all arrangements are compiled and loaded on to the FPGA board with the remote desktop. In this way, all required operations are performed with the BZK.SAU.uC web access platform.

To make a simple multiplication with the user-defined register, first press the "ESC" key with the virtual keyboard to pass though the command line from BZK.SAU.uC screen logo, as shown in Figure 2, at the left. The "C:\" command line then appears on screen.

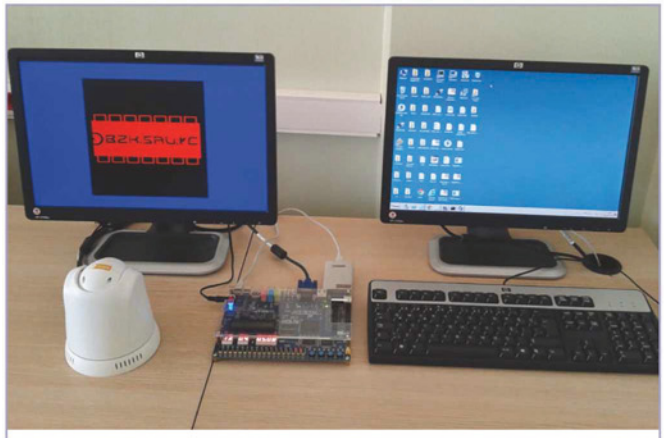

Figure 3: BZK.SAU.uC system design

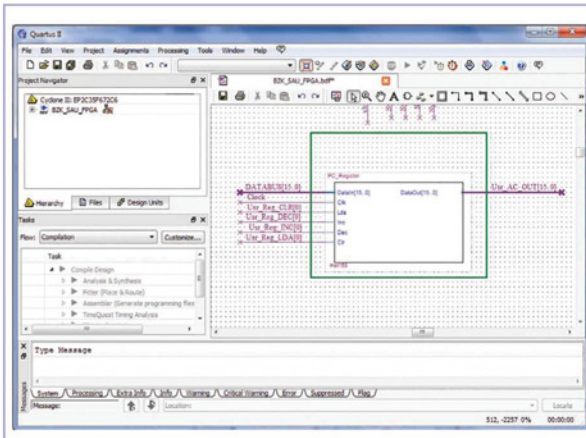

Figure 4: Quartus program with BZK_SAU_FPGA.bdf

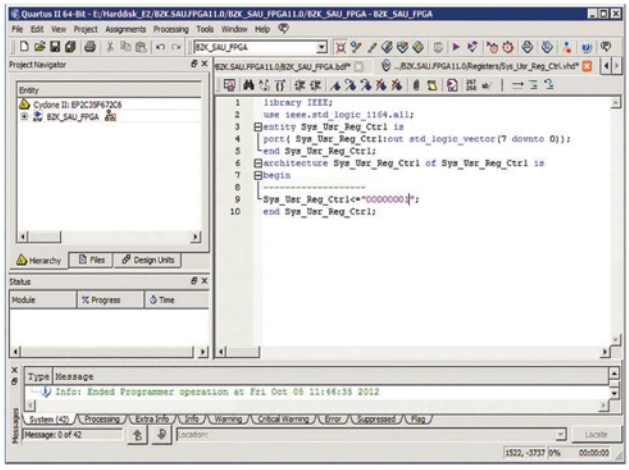

Figure 5: "Sys_Usr_Reg_Ctrl" VHDL file in "BZK_SAU_FPGA.bdf"

Writing "new" and pressing "Enter" with the virtual keyboard makes the system figure out that a new program will start operating, so it waits for the new user commands.

The "lda #1234h;" > "Enter" > "mul #0002h;" > "Enter" > "htl." commands entered into the system would make it multiply "1234" by "2". The "C:\run" > "Enter" then makes it display "2468" on the FPGA board's seven-segment display. These actions are shown in Figure 6.

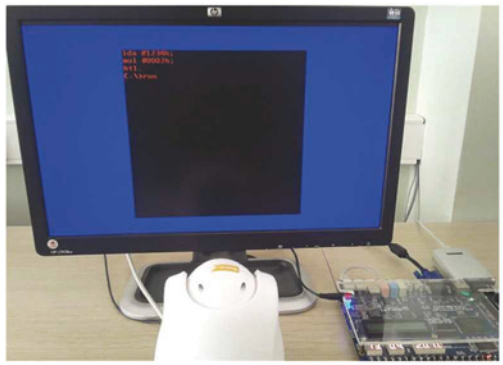

Figure 6: 16-bit user defined register multiply example on a VGA monitor using the web access platform

Open Access

Our previously designed 16-bit microcomputer architecture (BZK.SAU.FPGA) and the modular configuration of this system are available to anyone interested in this topic, accessible on http://bzksaufpgauc.bozok.edu.tr/homepage.aspx.

The system has a reconfigurable hardware (FPGA), allowing users to integrate their own units in it, operate and test those units, and fine-tune their designs – all remotely.

Combining a remote desktop, virtual keyboard and live video stream on a single platform via the Internet enables users to work on their designs with great ease and flexibility. ●

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IMPROVING THE PERFORMANCE OF CMOS GIGABIT ADCs

DR SHABBIR MAJEED CHAUDHRY, RIZWAN RASHID, ALI NASEER BUTT AND **BASHIR ASHRAF** FROM THE UNIVERSITY OF ENGINEERING AND TECHNOLOGY IN TAXILA, PAKISTAN, COMPARE VARIOUS CMOS GIGABIT ADCS AND DISCUSS TECHNIQUES HOW TO OVERCOME THEIR PERFORMANCE LIMITATIONS

Applications such as radar, wideband radio receivers, optical communication links and electronic measurement devices (transient digitizers and digital oscilloscopes) require sampling rates in the gigahertz range, which can be achieved with flash analog-to-digital converters (ADCs) – also known as parallel ADCs or direct conversion ADCs; their parallel operation allows sampling at a very high rate.

Although they're very fast, ADCs' power consumption is a major factor that needs improvement. However, by limiting the device's power consumption, its performance may suffer. To avoid this, different techniques may be used.

Demand for smaller and faster devices and advancements in CMOS technology are constantly changing the way ADCs are made. For example, sophisticated electronic devices require ADCs with minimum possible active area; and an ADC's supply voltage depends on the CMOS technology used for its fabrication. So far, 180nm CMOS has been the prevalent technology for fabricating ADCs, but Wismar et al report a 90nm implementation running at 0.2V supply voltage (operational @ 0.18V) – the lowest V_{DD} published to date.

Offset Calibration

A flash ADC consists of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

The operation of a flash ADC depends on the exact definition of the reference voltage detected by each comparator. The output voltage is called 'reference level', but that is not accurate because comparators have an inherent error called 'offset voltage'. Some ADC characteristics, such as differential nonlinearity (DNL) and integral nonlinearity (INL), are also affected by this offset voltage. So, before designing an ADC, this error has to be taken into account, and there are various ways to help reduce it. Techniques such as

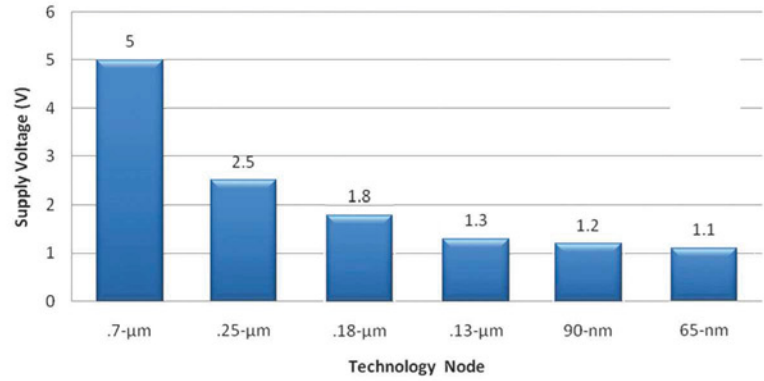

Figure 1: ADC supply voltage decreases with each new technology node, which also decreases the power consumption

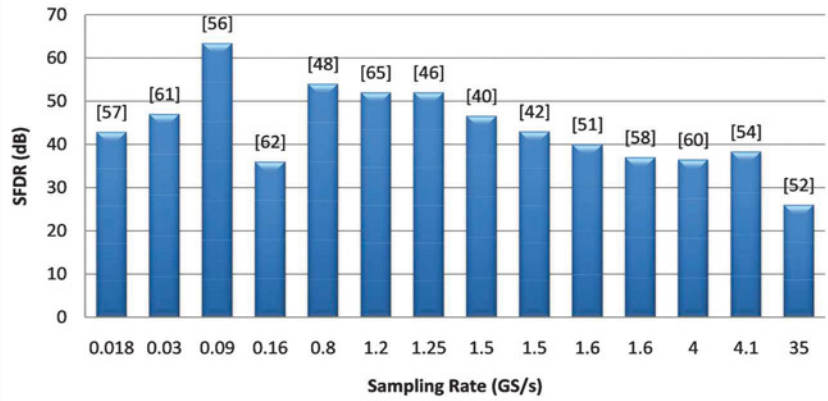

Figure 2: Graph showing the difficulty and challenge of increasing SFDR with increasing sampling rate. The highest SFDR is achieved in [56] for which a cascade of flash and successive approximation registers (SARs) were used. SFDR does not change much to 1.25GS/s; after that it decreases

device sizing, offset averaging, auto-zeroing, calibrated redundancy and comparator random chopping calibration were developed to cancel the effects of offset voltages.

In recent years, digitally-controlled trimming techniques have also been developed, where a feedback loop senses the offset and then digitally adjusts the biasing current of each ADC comparator to counteract it. Or, a pair of calibration transistors in shunt with the comparator input transistors can be used to correct the comparator offset. These methods can efficiently compensate for large offsets of ADC comparators due to device mismatches; as a result, small and fast devices can be used in the comparator to save power and enhance speed.

On the other hand, those calibration devices can introduce extra capacitive loading into the high-speed analog signal path and lower the high-speed performance of multi-gigasample-per-second flash ADCs.

Often, offset voltages are corrected by trimming, or more resistors are used in the reference ladder, and a more appropriate reference level selected for each comparator to deliver a much finer resolution.

There are also methods where a voltage-trimmable offset-cancelling buffer is placed between each comparator and its resistor ladder reference to offer adjustable reference voltages. There's also a calibration technique based on modifying the bulk voltages of input differential pairs in pre-amplifiers to calibrate the preamplifier and comparator offsets.

Noise

Noise is a factor that restricts the resolution and bandwidth of ADCs. Quantization

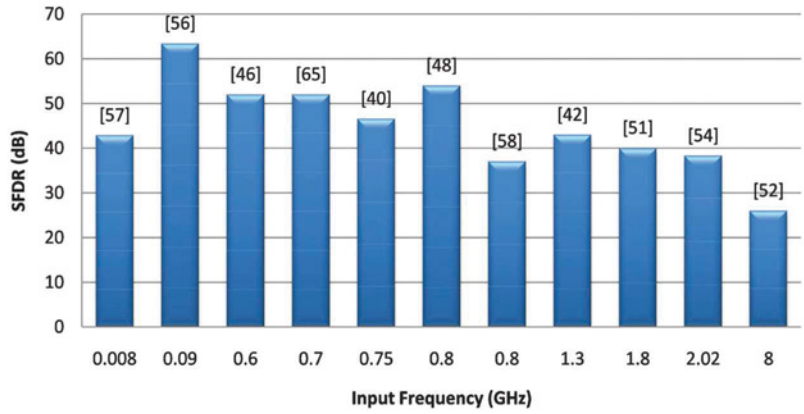

Figure 3: Communications applications have been a key driver for ADC linearity. Without a sufficiently linear signal path, the interfering signal will produce harmonics or intermodulation artifacts that may totally block the in-channel signal. The trend of SFDR with input frequency is almost the same as with sampling rate. With increased input frequency it's difficult to increase SFDR

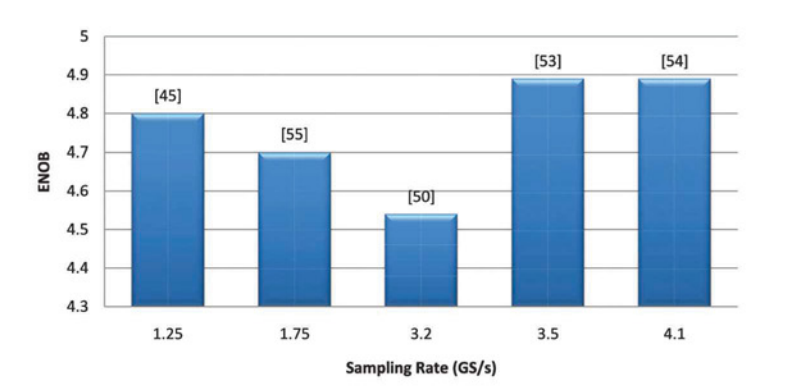

Figure 4: The graph shows that ENOB decreases with an increase in sampling rate but the relation of ENOB and sampling rate cannot be completely defined by this graph, since it depends on the techniques applied to a particular ADC

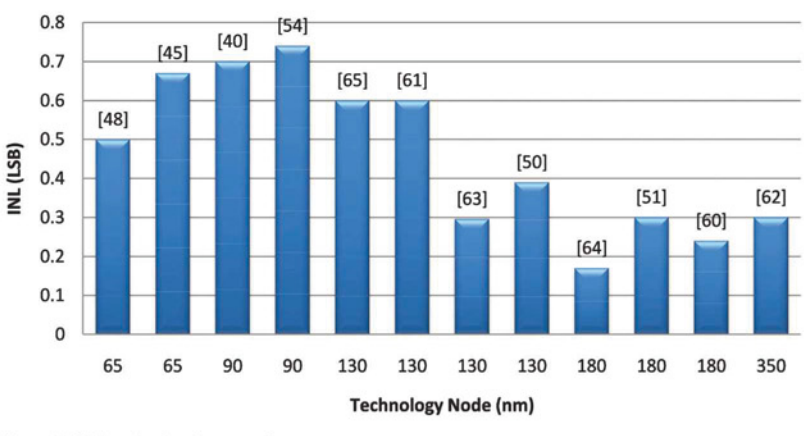

Figure 5: INL vs technology node

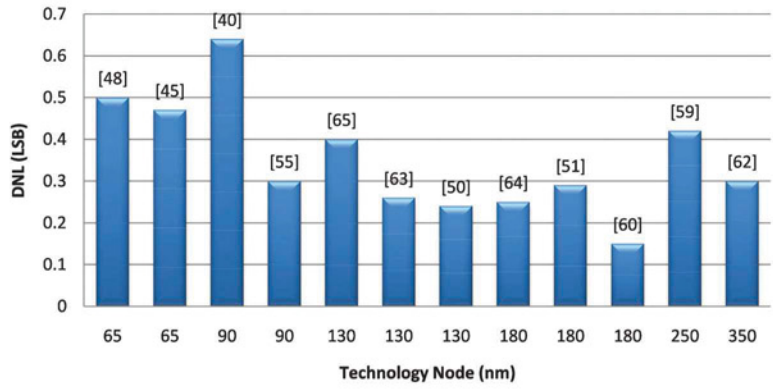

Figure 6: This graph shows that CMOS technology advancement introduces non-linearity. However, it's not the only factor on which linearity depends, which is why the trend deviates in certain places in this graph

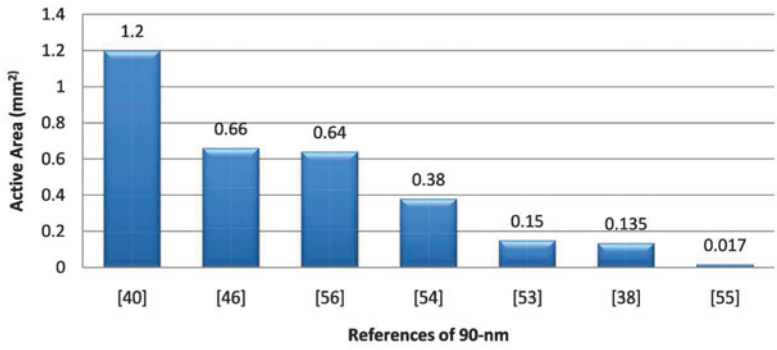

Figure 7: The smallest reported area depends heavily on the CMOS technology node used

errors, thermal noise, flicker noise, switching noise and jitter all contribute to the overall noise power on the ADC output. The ideal quantization error is often treated as a noise component, although in reality it is a deterministic signal with a large number of harmonics, resulting in a noise-like spectrum for the ADC with enough number of bits N. Any noise above the ideal quantization noise level is due to the actual circuit implementation, called 'circuit noise', and stems from both the analog and digital circuits.

The effects of flicker noise can be reduced by chopper methods or the use of correlated double sampling.

Switching noise results from transients produced by the switching of analog and digital circuits during operation. Such interference propagates as transients on the power supply lines through the substrate, or by inductive and capacitive coupling. Its effect can be supressed using supply separation, decoupling, guard-rings and electromagnetic shielding, and by adjusting the slope or timing of the leading transients, such as those created by digital output pins.

Due to component mismatch, real ADC implementations have finite (non-zero) differential non-linearity (DNL) errors. Such errors produce a non-uniform distribution of decision levels that raise the quantization error above that of the ideal quantizer. The precise amount of additional noise depends on the magnitude and distribution of DNL errors across the converter code range and not just the worst-case DNL error usually reported.

Unlike non-linear distortion, memory effects, etc, thermal white noise is totally random from sample to sample and thus impossible to predict or compensate for by calibration. It is therefore a more fundamental limitation of ADC performance than non-linear distortion or memory effects. A basic model of ADC noise refers to a noisy input source resistance R_n while assuming the rest of the signal route is noiseless. The signal to noise ratio (SNR) is defined as:

$$SNR = 10 \times \log_{10}(V^2_{fS}/16kTR_nf_s) \quad (1)$$

Equation 1 describes a theoretical limit on the attainable SNR for an ADC with a given input swing and impedance level.

Jitter

Jitter included in the sampling clock reduces the SNR required for the desired operation. This becomes noticeable for high analog-input frequencies. For exact results provide the ADC with a sampling clock, with a low value of jitter.

For applications needing modest resolution, typically up to 8 bits, and sampling frequencies of several hundred MHz, flash architecture may be the only feasible alternative; the user must provide a low-jitter clock to guarantee good ADC performance.

For applications with high analog-input frequencies, the selected ADC should have internal track-and-hold. The jitter of the sampling clock of an ADC is measured by a stochastic time-to-digital converter (TDC), with the measured jitter statistics used to correct the ADC sampling error and increase SNR.

The future evolution of ADC jitter performance will have great influence on the development of advanced communications infrastructures, or any other application where sampling at radio frequencies is needed.

A detailed assessment of past and present jitter evolution trends is therefore a highly valuable reference for system-level planners, giving a clue to what kind of ADC performance is to be expected in the future.

ADC jitter can be measured by subtraction techniques in a dual-channel sampling system. Synthesizers' phase noise, voltage noise and ADC nonlinearities are removed to give the sum of both ADCs' jitter. Then, a third ADC is used to determine one ADC jitter value by successive measurements. Jitter error can be cancelled in the digital domain.

Spurious Free Dynamic Range

Spurious free dynamic range (SFDR) is the ratio of the RMS amplitude of the essential (maximum signal component) and the RMS value of the next largest spurious element eliminating DC offset. It is expressed in decibels (dB) in relation to the carrier.

ENOB

Effective number of bits (ENOB) is a measure of dynamic presentation of an ADC and its related circuitry. The resolution of an ADC is specified by the number of bits used to denote the analog value, in principle giving 2N signal levels for an N-bit signal. However, all real ADC circuits produce noise and distortion, so ENOB specifies the resolution of an ideal ADC circuit with the same resolution as the circuit under observation.

DNL And INL

Differential non-linearity, also known as Differential Linearity Error, defines the deviation between ideal step-size and actual step-size observed for each ADC code.

INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of a real transfer function from a straight line. The INL error value then depends directly on the position selected for this line.

The comparator bank has redundancy and re-assignment to correct DNL errors.

Capacitor-matching errors, residue amplifier gain, settling errors and linearity error are the major sources of ADC linearity errors. Linearity errors are very dependent on comparator offset errors. As the signal quantization level decreases, DNL and INL become serious problems in ADC design.

ADC linearity can be increased if calibration is done on the reference pre-distortion. Cascode bias currents, use of long channel-length devices or dynamic biasing with feedback, also increases output swing and overall linearity.

Since ADC performance has a strong relation to linearity, there are many techniques that improve it, including averaging networks, redundancy, re-configurability and digital calibration.

Power Consumption

These days, system designers are increasingly faced with the challenge of minimizing power consumption of systems and devices.

Flash ADC contains a great number of active components, including a chain of comparators (with latches at their outputs) and fast encoder circuitry that makes them a major consumer of power within a receiver front-end. A power-reducing technique uses pre-sensors to check for any unused blocks in this semi-pipeline chain of latches and encoders.

Digital calibration (common-mode calibration) and reference voltage play a vital role in saving power. Stochastic flash ADCs are designed using random comparator offsets to set trip points; here comparators are implemented in digital cells.

Capacitive interpolation offers great advantages when designing for low-power applications – there's no need for a reference resistor ladder, or implicit simple-and-hold operation. No edge effects in the interpolation network and very low input capacitance result in low power consumption. Exclusion of the over-range voltage headroom used by the dummy pre-amplifiers reduces power consumption.

To further reduce power consumption, we can use near-minimum size comparators, with an offset that decreases through foreground calibrated trim-DAC circuitry.

Active Area

Today's sophisticated electronic devices have a much smaller active area, and contain very different components or modules, so every component should be manufactured using the most advanced

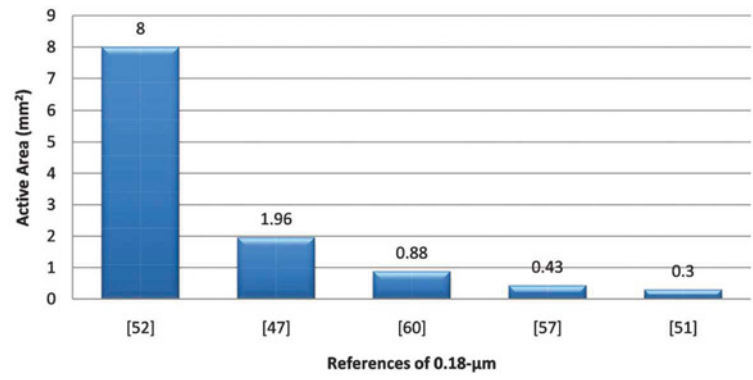

Figure 8: Graph showing that the minimum area achieved using 0.18µm CMOS is 0.3mm²; while for 90nm CMOS it is 0.017mm² using a dynamic folding technique

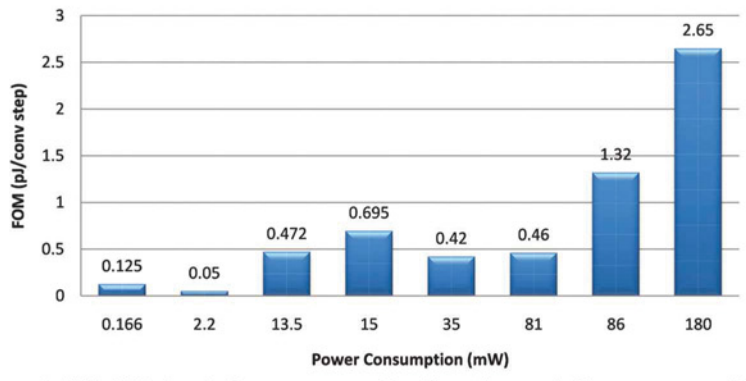

Figure 9: FOM plotted against power consumption. It can be seen that power consumption is directly proportional to FOM

CMOS technology. This should also be the case with flash ADCs.

Active area depends solely on the area normalized to a number of effective quantization steps, known as the generic measure of area efficiency. It is seen that state-of-art absolute area has a strong connection with resolution and the CMOS technology node. To decrease active area and power consumption, front-end track-and-hold circuits in the flash ADCs can be substituted for dynamic ones.

State-of-the-art A is approximately proportional to 2^{ENOB}; the area per effective quantization-step (A_Q) is normalized area measure:

$$A_Q = A/2^{ENOB}$$

Because of device geometry scaling, A is likely to be a function of the process node used for implementation.

Figure Of Merit

Figure of merit (FOM) is an important parameter for ADCs. It can be calculated from:

$$F_{A1} = P/(2^{ENOB} \times f_S)$$

where P = power dissipation
ENOB = effective number of bits
f_S = Nyquist sampling rate

The effective number of bits is defined by SNDR (signal-to-noise and distortion ratio) as:

$$ENOB = (SNDR - 1.76)/6.02$$

FA1 links the ADC's power dissipation to its performance, characterized by sampling rate and conversion error amplitude.

Observable Trends

By observing all the trends, it can be stated that a high-performance flash ADC should have a high sampling rate, high EBRW, low power consumption and a smaller active area.

Power consumption can be lowered by segmentation, or with dynamic folding techniques, and by using advanced CMOS technology, which helps reduce the required supply voltage.

As chip size gets smaller, the ADC will generate less heat and use less power. But not all ADC parameters can be optimized simultaneously, because changing one parameter affects others.

It can be seen from Figures 5 and 6 that with advances in CMOS technology, the linearity of an ADC decreases. So, to make your device linear, you will need to compromise on technology. Minimum power consumption is achieved by using 65nm CMOS technology and capacitive folding technique, where most of the power is used charging and discharging a small capacitor. For best results, a balance between these two parameters should be struck.

Different circuit topologies with different CMOS fabrication technologies can be combined to give optimized performance for gigabit ADCs. ●

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Features

- Universal 90-264VAC Input
- IEC320 C8 2 pin AC Input Connector (UK power cord included)
- Outputs switchable from 10 x 5V 1A or 5 x 5V 2.4A
- Will charge most devices powered by standard USB 5VDC chargers
- EMC to EN55022'B', CISPR22 'B' & FCC 'B'
- Full International Safety Approvals & CE marked
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INTELLIGENT IP DESIGN FLOW

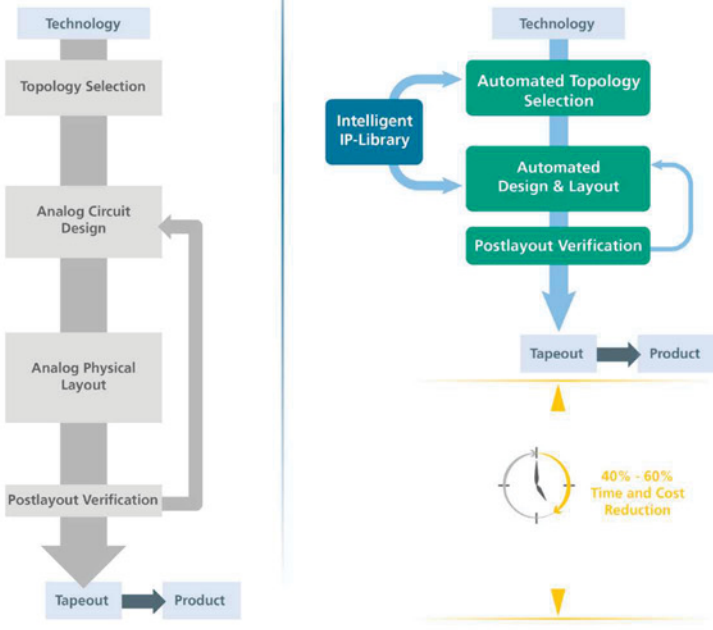
BENJAMIN PRAUTSCH AND **DR TORSTEN REICH** FROM GERMAN-BASED FRAUNHOFER INSTITUTE IIS
DESRIBE A GENERATOR-BASED DESIGN SOLUTION FOR ANALOG INTEGRATED CIRCUITS

Today's integrated circuits and systems are efficiently designed and developed almost entirely using software. But for the important analog components in SoCs (system-on-chips) however tools are largely missing for automating the design. That is why complex manual work is necessary for these components, even though they often occupy only a small part of the total chip area.

Decade-Old Problem: Analog Design

Continuous "flows" in digital design make it possible to fully automate the creation of the devices' physical representation (layout) to achieve their desired behaviour. Developers can thus quickly and reliably create large circuit blocks with millions of transistors, with optimized data rates, power loss and area. However, the situation is different in analog design. Here, there is no automated flow and the design effort is therefore high. To date, this represents an enormous cost factor for the development of integrated systems with mixed-signal circuits and also prolongs the time until a product is ready for market.

Figure 1: IIP design flow concept



This even applies to technologies with large structure sizes which can be well controlled. It becomes much worse in deep submicron technologies since here the number of design rules to be observed is quite large. Is efficient design of robust analog or mixed-signal ICs even possible under such conditions?

One thing is certain: analog components in SoCs will play an important role in future markets, such as the Internet-of-Things or autonomous driving. And the semiconductor technologies for these markets keep shrinking in order to, for example, guarantee minimal power losses or short latencies. The cost pressure will rise. Significantly higher volumes then lead to lower prices per unit. Both development and product cycles become shorter. With these constraints, analog design will become even more problematic in the future.

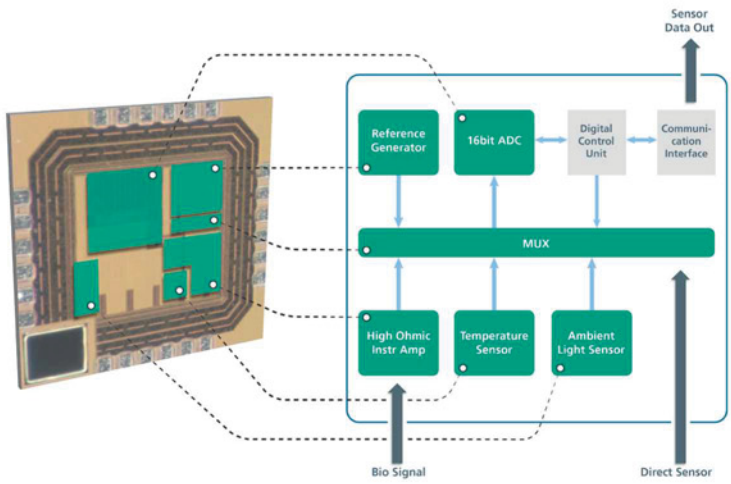
But how can analog design be automated today? Almost everything is done manually. Only elementary layout structures, such as basic components (MOS transistors, resistors, capacitors, etc), are realized as configurable, automatically-created cells (pCells) and the concept of configurable layout blocks is still rarely used beyond these fundamental components. So the question arises whether this generation should not also be used in higher levels of hierarchy, and for schematics as well as layouts. Is there a limit to expected usefulness if integrated systems' complexity increases? And not least: what do analog designers say about such concepts? Are they open to new ideas and approaches, and adopting new practices, or do they stick to "design as usual?"

Flexible Intelligent IPs

Researchers at the Dresden Design Automation Division EAS, part of the German Fraunhofer institute IIS, deal with precisely these issues. They have developed a generator-based design solution for analog integrated circuits – the Intelligent IP Design Flow. The Intelligent Intellectual Properties (IIPs) used – not to be confused with conventional analog IP – are configurable building blocks useful with a variety of technologies: from the current technology nodes between 350nm and 90nm dominant in the market, down to 28nm to 22nm, which will become important in the future.

In the course of the design, the IIP software also creates all data (schematics, layouts, test-benches, behavioural models), developed during the manual design, but does this automatically go through configurable and deterministic program sequences?

Figure 2: IIP design flow for smart sensor Asic



While the design of all components takes place manually in the conventional design flow, frequently used basic blocks (e.g. current mirrors or differential pairs) are automatically created in the IIP Design Flow, and so are more complex components, such as operational amplifiers, ADCs and DACs.

The great strength of these off-the-shelf solutions lies in their determinism. Developers can freely configure complex components directly within seconds, instead of manually doing these tasks. At the same time, the generated circuit topologies and layout structures are determined in advance, as opposed to purely optimization-based approaches; this reduces known hurdles and largely frees up the user.

Automation is supported in advance by a targeted topology selection and subsequent optimization. The core of the entire IIP Design Flow is the generic IIP Library. Through the use of a high-grade, technology-independent programming interface (API), generic IIPs are created which can be reused hierarchically in other IIPs. The IIP generators always provide DRC and LVS-clean solutions. Only then is a rapid exploration of the circuit space and its layout effects possible – normaly a lengthy process in manual design.

> Today's integrated circuits and systems are efficiently designed and developed almost entirely using software

With their approach, the developers at Fraunhofer IIS/EAS are able to show significant time and effort savings in several design projects. Above all, necessary corrections to the design, both at the beginning and during the verification phase, are significantly faster and more flexible. This is partly enabled by the automated approach, which generates proven layout structures and schematics, of which parasitic effects can be immediately investigated in the overall context of the circuit. The other part is that these layout structures are immediately verified and readily available. In addition, design results can often be reused in subsequent projects – and without manual redesign – under new boundary conditions; especially frequent recurring tasks can then be done at the proverbial push of a button.

The manual design is of a static nature, which means designs are tailored to very specific problems, and existing circuits always need to be re-edited with great effort, so a design environment that allows generator-based design at the outset is highly desirable.

The initial extra effort of the Intelligent IP Design Flow is only needed once before use. If this environment exists once, however, the advantages of configurable IIP design immediately bear fruit. If designers create IIPs themselves, familiarization is still required, since the layout is described entirely as source code. An experienced designer, however, can far surpass the efficiency of manual design. This is especially true for regular structures or specific "programming-friendly" patterns.

Apart from this, only slightly more time is required with the Fraunhofer approach for the verification of self-made generators. With matching circuit topologies and layout structures, IIP Design Flow can dramatically shorten the total time of design – either through library IIPs or self-developed ones. This is particularly true where layout parasitics have an especially high impact on the circuit. Furthermore, efficiency gains are particularly evident when specifications and semiconductor technologies change or where a flexible action is required.

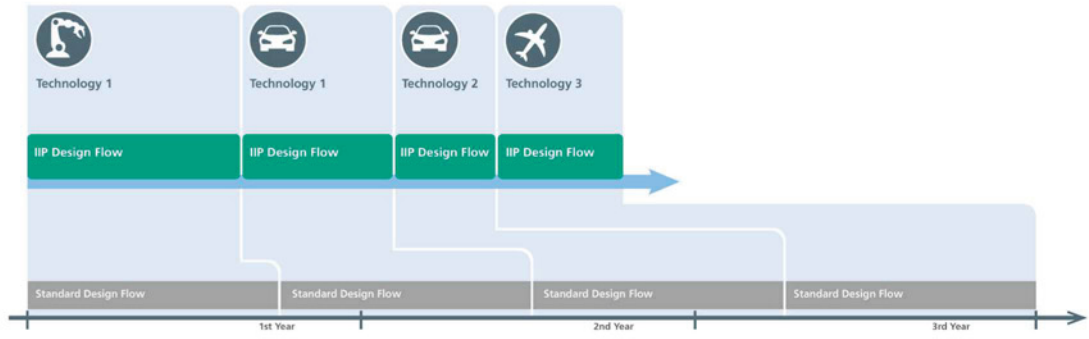
Design Examples

The work at Fraunhofer IIS/EAS has intensively targeted development of the IIP Design Flow since 2010. At the same time, the results were incorporated into mixed-signal design projects, making it possible from the start to reach design standards of varying complexities.

To compare with conventional design flow, experienced analog designers at both Dresden EAS and Fraunhofer IIS in Erlangen, working in parallel, developed a complex "SMART Sensor ASIC". One design group worked with conventional design flow and the other group had access to the IIP Design Flow. Comparing the development time and costs showed significant advantages of the IIP methodology.

In phase 1, the scope of the IIP library was limited to basic circuits of low complexity (match-sensitive current mirrors, differential pairs, capacitor arrays, etc.) increases in efficiency

Figure 3: IIP design flow for time comparison



of up to 15% were seen; and design time was shortened from five months to under four months.

In phase 2, the designers used a more extensive IIP library with more complex components (e.g. various operational amplifiers, switches and ADC cores). For the ASIC design, savings of up to 40% were achieved; and now, three months sufficed from conception to production as a result of the entire layout process being automated and substantially faster. There were also savings in the post-layout verification, since fewer iterations were necessary between design and verification.

Even clearer was the advantage of the IIP Design Flow in the third phase: adapting the existing ASIC for a new application with new requirements (from low power to high data rate). The savings were most evident here: at two weeks the full redesign using the IIP Design Flow was 75% faster than with manual redesign.

IIP Design Flow has been used in customer projects since 2014 – its use was previously limited to IIPs for basic circuits in technology nodes up to 180nm. Marketability of the comprehensive IIP library with over 50 sometimes-complex analog components is expected to be reached in 2016.

There are also initial reference projects with a view to "More Moore" technologies. The entire current output stage of a 12-bit 80MS/s DAC in modern 28nm FD-SOI technology could thus be designed in just one month using IIP Design Flow. Due to its very complex but regular structure, this stage lent itself very well as to independent, new IIP, since it offered a "programmer-friendly" pattern. Various layout-induced effects could be efficiently created and compensated for through generation of the entire layout. The manual expense of the same task would hardly be sustainable.

In 2016, the generic IIP library will also support 22nm technology.

Is The Analog Design Problem Solved?

Rapid exploration of a circuit, including its parasitic effects, is made possible in the first place through efficient IIP methodology. Nevertheless, compared with digital design, this flow too is hardly automated, since many processes are still manual. IIPs are thus currently used as modules not yet incorporated into a complete and cohesive solution. Key components are still missing, such as generic dimensioning of existing blocks, in order to quickly achieve the initial solution or automated support for converting static layouts into generic IIP descriptions. This implementation will be the subject of additional work at Fraunhofer IIS/EAS.

Nevertheless, complex circuits can already be flexibly described in a generic way today and executed in various technologies whose minimal structure sizes span more than an order of magnitude. The IIP methodology is thus already an extremely valuable resource for efficient design and reuse. It is thus a significant step and a fundamental building block on the way to a comprehensive solution for the analog design problem for "More Moore" technologies.

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But what about "More than Moore"? This is primarily about a variety of solutions for a variety of applications. The big challenge is to efficiently realize IIP development and so reduce initial effort using this methodology. Such effort is always worthwhile if one considers the fact that a once-created flexible IIP contains the programmed expert knowledge of a designer. If this knowledge will be in demand again in the future (reuse), then time spent implementing the IIP will pay off quickly. Simply because an off-the-shelf solution already exists, it will be in most cases more efficient than the reconstruction of knowledge and manual design under time pressure.

For the future of analog design it will be essential if one-time designs are created or a complete rethink takes place – which has happened before. This will increase the long-term efficiency of analog design and improve readiness for the long-desired analog synthesis. ●

WHAT THE READERS SAY...

AT A LOSS?

On reading the article in Electronics World (October 2015 vol. 121) *"Characteristics of Microwave and RF Signal Filters"* by Stojce Dimov Ilcev I am somewhat puzzled by the context and relevance in an RF context, especially in a higher-frequency domain.

Basic filter types such as bandpass, bandstop, lowpass, highpass are presented as expected (in general form) and characteristics such as rolloff and passband ripple are addressed; however then discussion of the filter types, their topologies and their implementations (using R's and C's) bear no likeness to those which would actually be realised for general RF use, let alone microwave.

Whilst I do not have reason to doubt the knowledge or experience of Stojce Ilcev I have to pass a number of observations on the article.

Important aspects in RF such as impedance matching, return loss and so on do not appear to be touched upon, and both the formulae as shown and the schematics as displayed are very different from what one would use at RF and are also completely different (even by reference) to the filter units shown in the accompanying photographs in the article.

I am at a total loss as to the relevance of the article, its general content is what I would consider elementary, it has no extra value in the RF 'world'.

Has anybody else queried this or am I missing something totally?

F.C. Trevor Gale

AUTHOR STOJCE DIMOV ILCEV REPLIES:

The difference between RF and audio filters is obvious. Audio filters are working in the frequency range from 0Hz to beyond 20kHz, so in my article the kHz range is not included. However, RF filters are designed to operate on signals in the range of MHz to GHz. As I wrote in my article, for wideband filter applications the available frequency range is from 0.5-500MHz. As for filtering functions both type filters are using almost the same methods.

You can find samples of the miniature bandpass filters illustrated in Figure 3c of the article online at the US-based Microwave Filter Company (**www.microwavefilter.com**).

By doing a search on line you can read more about active bandpass filters and find other good tutorials in this category, whereas at **http://www2.ece.ohio-state.edu/~anderson/Outreachfiles/AudioEqualizerPresentation.pdf** you can find out more about audio filters.

All type of filters with the formulas described in my article are not my inventions or scientific research, but a retrospective of knowledge and research from valuable resources and manufacturers' manuals.

My article does not adopt a scientific but informative approach, showing the possibility of practical use for the said filters.

Just to add to that, I am expert in radio and satellite communication, and navigation and surveillance (CNS) with several published books. I am also author of many articles and papers in eminent journals and conference proceedings.

BOOK WINNERS

Over the course of the past year we introduced several regular columns focusing on different aspects of electronic design. Each of these columns run a competition to win the associated books.

The winners of these books are:

GRAPHICS, TOUCH, SOUND AND USB, USER INTERFACE DESIGN FOR EMBEDDED APPLICATIONS
by Luico di Jacio
Robert MacKay, Canada
Richard Shadbolt, UK
Hylton Brenner, Israel

RASPBERRY PI FOR DUMMIES, 2ND EDITION
by Sean McManus and Mike Cook
Mark Gamble, UK

RASPBERRY PI PROJECTS FOR DUMMIES
by Mike Cook, Jonathan Evans and Brock Craft
David Fitter, UK

RASPBERRY PI USER GUIDE
by Eben Upton and Gareth Halfacree
Athul Jayaram, Kerala

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MEAN WELL

DIN Rail
Power Supplies

For Further Information:

Call: 01844 204420

Website: ecopacpower.co.uk

Email: sales@ecopacpower.co.uk

AWS ELECTRONICS GROUP WILL SUPPORT EMS MARKET IN FRANCE

AWS, a specialist electronics manufacturing services (EMS) provider, is now supporting French customers with the appointment of DSA Commerce as representative in this strategically-important European market.

Headed by Alfredo Desa, DSA Commerce is well established in France and especially active in key markets such as automotive, aerospace, rail, medical and nuclear.

"Many companies in France are looking for a reliable EMS partner that can provide a high-quality service on technically-challenging designs, yet keep costs competitive. AWS, with its high volume facility in Namestrovo, Slovakia, meets the needs of our customers in France perfectly," said Desa, owner and director of DSA Commerce.

AWS has six lines in Slovakia with 18 pick-and-place machines and a large area dedicated to mechatronics and box build, replicating the exact AWS systems at its European HQ.

www.awselectronicsgroup.com

ASTUTE ELECTRONICS CERTIFIED TO MIL/AERO ANTI-COUNTERFEIT STANDARD AS 6081

Astute Electronics gained certification to AS 6081, the SAE aerospace standard for counterfeit mitigation, designed to provide a very high level of protection for companies in the aerospace and defence industries.

This makes Astute the first British as well as first European company to gain this certification, and only the fourth company in the world to achieve it. Astute is also the first company worldwide to have more than one location certified – in the UK and the US.

AS 6081 standardizes practices and methods to mitigate the risks of purchasing and supplying fraudulent/counterfeit electronic parts. It covers activities such as identifying reliable sources to procure parts; assessing and controlling suspect or confirmed fraudulent/counterfeit parts; and reporting suspect and confirmed fraudulent/counterfeit parts to users and the authorities.

www.astute.co.uk

YUASA LAUNCHES NEW EUROPEAN WEBSITES

Yuasa Battery Europe has launched a series of ground-breaking new European websites for automotive, industrial and motorcycle markets.

The five new Yuasa sites were switched on at the beginning of November with the UK, Germany, France, Spain and Italy being served by their own individual sites, offering an informative and engaging resource for customers, distributors, industry professionals and retailers.

The websites are mobile-ready with easy navigation, industry-leading battery finders and in-depth information resources. There is also plenty of engaging content, including updates on Yuasa's products, in-depth technical information, news, exclusive Yuasa motorsport content and other informative guides and features.

The websites show the entire range of Yuasa products including specifications, part numbers and photographs, and include downloadable brochures, datasheets and so on.

www.yuasaeurope.com

AURORA GROUP UNVEILS 2016 CATALOGUE AT LUXLIVE

The Aurora Group, a global manufacturer of smart LED lighting solutions, has unveiled its new catalogue, 'Lighting 2016 Edition 1', at LuxLive 2015.

The catalogue reveals new products that Aurora will be releasing in the new year, and demonstrates how the company intends to deliver 'Value Beyond Illumination' going forward. For the first time, the catalogue represents the entire Aurora Group branded portfolio, including the recently rebranded retail lighting specialists, Microlights, which has over 30 years' experience in assisting customers enhance their retail sales through lighting.

The 2016 catalogue presents Aurora Group's combined expertise and products under one brand, as Richard Sells, Group Managing Director, explains: "With a consolidated approach we can offer a complete range of products to accommodate five sectors – residential, hospitality, retail, commercial and industrial."

www.auroralighting.com

GOOEE MAKES IT SEVEN OF THE BEST WITH NEW OEMS ON BOARD

Gooee is working in association with five more original equipment manufacturers (OEMs) relating to its 'Gooee Inside' technology, bringing the total number of manufacturers to seven. Gooee's partners will now be able to use the world's first 'Full-Stack' IoT platform, developed by Gooee, and connect their products to the Internet of Things.

The partnerhips will ensure lighting manufacturers can take advantage of a new trend toward intelligent lighting solutions and integrate the latest smart IoT technology into their extensive ranges.

"We are dedicated to developing the latest technologies that exceed the market's expectations," said Jan Kemeling, Gooee's Chief Commercial Officer. "That means creating high-performance smart components and software solutions that present no surprises, no disappointments and no compromises."

www.gooee.com

NEW FROM TÜV SÜD

TÜV SÜD Product Service launched this month its automated test rig service to help manufacturers and retailers enhance their brand reputation through improved product reliability and quality.

The new service will test products that have a repetitive use, for example those that incorporate switches or hinges. TÜV SÜD will build a bespoke test rig to accommodate individual products and develop a test schedule set against expected usage for the lifecycle of the product.

Manufacturing a reliable product at an attractive price point has become a key competitive differentiator as the market continues to demand value for money.

"Product reliability testing has become increasingly important as cash-strapped consumers demand a long product life and look for products with a positive brand image," said Richard Poate, Senior Manager at TÜV SÜD Product Service.

www.tuv-sud.co.uk

TÜV SÜD Product Service

NEW RIGEL SAFETY ANALYSER SPEEDS UP MEDICAL DEVICE TESTING

Faster and safer testing of medical devices and installed equipment in hospitals and healthcare facilities is provided by the new, battery-powered, 288 Plus from Rigel Medical.

This automated safety analyser is one of the smallest around and incorporates a host of new features for enhanced performance and faster testing of electrical safety to IEC 62353, and leakage tests in accordance with IEC 61010, IEC 60601, NFPA, AAMI and AS/NZ3551.

While most conventional testers rely on mains power, the 288 Plus retains operational integrity, even without mains connection, due to standard AA battery power compatibility. This provides greater flexibility for users and makes it quicker to complete in-service testing of point-to-point leakage as well as earth continuity and insulation resistance. There's also a short boot-up times between tests.

www.rigelmedical.com

24-BIT 2MSPS SAR ADC ACHIEVES 145DB DYNAMIC RANGE

Linear Technology has introduces the LTC2380-24, a breakthrough no-latency 24-bit 2Msps successive approximation register (SAR) analog-to-digital converter (ADC). The LTC2380-24 features an integrated digital filter that averages 1-65,536 conversion results in real time, dramatically improving the dynamic range from 101dB at 1.5Msps to 145dB at an output data rate of 30.5sps. This makes the LTC2380-24 ideal for seismic, medical and many other applications demanding high dynamic range.

Using an on-chip digital filter to average conversion results, the LTC2380-24 eliminates the processing burden from the digital host, conserving digital resources and the associated power. Moreover, the LTC2380-24 allows results to be read out with a serial clock as low as 2MHz, easing interfacing to microprocessors, enabling use with slower devices. The LTC2380-24 achieves true 24-bit noise performance from a single 2.5V supply.

www.linear.com

HIGH-PERFORMANCE OSCILLOSCOPES OFFER 16-BIT VERTICAL RESOLUTION

Now available from Link Microtek are the latest Rohde & Schwarz RTO-series high-performance digital oscilloscopes that offer high-definition signal analysis with a vertical resolution of up to 16 bits, clear and simple touchscreen operation and the world's first real-time digital trigger system.

As part of the Rohde & Schwarz general-purpose 'Value Instruments' range, the oscilloscopes are designed to provide a precise, reliable and affordable solution for a wide variety of test-and-measurement applications.

The RTO series includes 2- and 4-channel versions with bandwidths ranging from 600MHz to 4GHz. The oscilloscopes combine high acquisition rate of one million waveforms per second with a very low inherent noise level of 1% of full scale at 1mV/div and 1GHz, enabling precise measurements to be made even at low signal amplitudes.

www.linkmicrotek.com

MOUSER NOW SHIPPING MOLEX HIGH-PERFORMANCE MEDISPEC CONNECTORS

Mouser Electronics is now stocking the MediSpec Medical Plastic Circular (MPC) interconnect system from Molex. This is an affordable, high-performance interconnect solution that combines premium performance and ease-of-use to meet the stringent standards of medical devices. In addition, the MediSpec is also recommended for use in avionics, high-use entertainment equipment, and test and measurement devices.

The Molex MediSpec MPC Interconnect System uses the Molex Low Force Helix (LFH) contact system to ensure a reliable electrical interface over thousands of insertions. MediSpec connectors offer a simple push-pull engagement with optional locking sleeve for ease-of-use. The connectors use lightweight medical-grade plastic housing on the standard male plug and panel-mount female receptacles, which can withstand medical industry sterilization processes, including autoclave, ethylene oxide (EtO), gamma and chemical.

www.mouser.com

RELIABLE COAX CONNECTION EVEN FOR CHALLENGING ENVIRONMENTS

Harwin launched a range of standard layout, multiport coaxial Datamate connectors with 6GHz, 50Ω contacts, perfect for hi-rel applications. Suitable for RG178 cables, the ganged connectors are available from stock with two, four, six or eight contacts.

Based on Harwin's proven high-reliability Datamate connector family, the new coax connectors are designed with a single body moulding to resist extremes of shock, vibration and temperature in challenging application environments such as defence, aerospace, satellites, UAVs, undersea and others. Devices are equipped with hexagonal slotted jackscrews for secure fixing to the PCB, and mouldings are polarised to facilitate quick, error-free mating. Vertical and horizontal orientation styles are available and devices Harwin offers a choice of products to suit two PCB thicknesses, 3.5 and 5mm.

www.harwin.co.uk

RUGGED IP65 DOOR ENCLOSURES NEED NO HIDDEN EXTRAS

Hylec-APL has extended its DE range of IP65 door enclosures known for their rugged, maintenance-free and cost-effective protection in long-life applications.

All DE door enclosures are supplied with a galvanised-steel back plate, external mounting brackets and a lock and key as standard. Made from flame-retardant ABS, the enclosures feature wall thicknesses of up to 3.5mm to offer impact resistance of IK08 (protection against impacts with an energy up to 5J). Because ABS is non-corrosive, the enclosures deliver protection from continued exposure to external conditions, even in marine applications. Liquid gasket seals – a standard feature throughout the range – ensure IP65 protection is maintained, even when the doors are repeatedly opened and closed for regular access.

The range comprises 10 sizes; from 200 x 300 x 130mm to 600 x 800 x 260mm high.

www.hylec-apl.com

3M ELECTRONIC ASSEMBLY SOLUTIONS FOR THERMAL MANAGEMENT

3M is offering an extensive range of thermal management materials (TIMs), designed to provide simple, fast and effective solutions for thermal management in a wide variety of electronic design environments.

Products in this range dissipate heat while accelerating assembly time. They are also designed to reduce waste and weight, plus improve reliability due to reduced heat. A variety of flexible options suit a broad choice of applications, such as medical devices, consumer electronics, high-end automotive, batteries and lighting.

"As devices become ever smaller and more powerful, so does the pressure on every individual component – including tapes and pads – to deal with additional heat generation. 3M offers an extremely high-quality range of products that address these demands," said Terry Clark from UK-based DK Thermal Ltd, which distributes the 3M range.

www.3M.co.uk

FEMALE VERSION OF HARTING M12 SLIM DESIGN CONNECTOR

Harting has expanded its product portfolio for Gigabit Ethernet connectivity by introducing a female version of the M12 Slim Design connector. The new connector complements the existing male version, so that all the company's compact M12 variants are now available in crimp connection technology.

The new connectors have been significantly reduced both in diameter and length: the outer diameter has been slimmed down to 16.5mm, allowing a high integration density to be achieved with appropriate devices such as switches. In addition, the housing is significantly more robust, being able to withstand torques of up to 1.5Nm. The connectors with x-coding conform to IEC 61076-2-109, and comply with Cat. 6A and Performance Class EA.

The Harting Group develops, manufactures and distributes electrical and electronic connectors, network components, pre-assembled system cables, and backplane assemblies.

www.harting.co.uk

CADENCE ANNOUNCES PALLADIUM Z1 FOR DATACENTRE-CLASS EMULATION

Cadence Design Systems unveiled the Cadence Palladium Z1 enterprise emulation platform, the industry's first datacentre-class emulation system, delivering up to 5x greater emulation throughput than the previous generation, with an average 2.5x greater workload efficiency than the closest competitor. With enterprise-level reliability and scalability, the Palladium Z1 platform executes up to 2304 parallel jobs and scales up to 9.2 billion gates, addressing the growing market requirement for emulation technology that can be efficiently utilized across global design teams to verify increasingly complex systems-on-chip (SoCs).

Palladium Z1 enterprise emulation platform features rack-based blade architecture to provide enterprise-class reliability, a 92% smaller footprint and 8x better gate density than the Palladium XP II platform. It offers a unique virtual target relocation capability, and payload allocation into available resources at run time, avoiding re-compiles.

www.cadence.com

UNMANAGED SWITCH MAKES IT EASY SENDING LONG-DISTANCE DATA

Belden is now offering the SPIDER III Standard Line, unmanaged entry-level industrial Ethernet rail switches capable of bridging long distances without disruptions. The latest switches are based on the proven Hirschmann technology for high quality, cost-effective way to transfer large amounts of data. The switch has up to eight Fast Ethernet or Gigabit Ethernet ports, and two of the ports can be fibre optic.

The SPIDER III Standard Line of switches is future-proof thanks to Gigabit speed. The switches are designed for use in harsh environments and have the necessary certifications, making them ideal for the manufacturing, machine building, solar power and traffic control industries. They also work on the principle of plug-and-play that allows easy installation without compromising quality or reliability. Users can connect multiple devices without the need for a complex configuration process.

www.belden.com

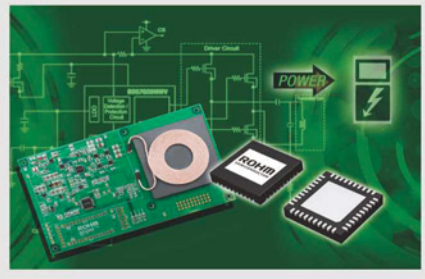
FIRST QI-CERTIFIED MEDIUM POWER TRANSMITTER REFERENCE DESIGN

ROHM has received certification from WPC (Wireless Power Consortium) for its reference design using the BD57020MWV wireless power transmitter IC. This is the first device in the world certified to be compliant with the new Qi medium power specification.

WPC's Qi standard for medium power has attracted attention as a next-generation standard for inductive power transmission that will enable wireless charging of tablet PCs while allowing smartphones and other mobile devices to be charged up to 3x faster than the existing low-power standard (5W). In addition, a Foreign Object Detection (FOD) function is included to provide greater safety by detecting foreign metallic objects before power transfer to protect against possible damage due to overheating.

ROHM also developed a reference design that will help accelerate adoption in applications that will benefit from wireless charging.

www.rohm.com/eu



THE RIGHT MASS FLOW METER FOR EVERY MEDICAL DEVICE

Swiss sensor manufacturer Sensirion adds three new products to the SFM3xxx platform for flow measurement in medical applications. For the first time, the flow sensor range now includes autoclavable mass flow meters, thus the five products in the platform now offer the right solution for all gas flow measurement applications in medical technology.

All sensors in this range share characteristics such as high precision and robustness. The fully calibrated and temperature-compensated sensors measure the flow rates of air and other non-aggressive gases bidirectionally and highly accurately. They also impress with very low pressure drop and fast response time.

The digital mass flow meter SFM3000 is particularly suitable for high-volume applications where cost is paramount. With the SFM3100, Sensirion offers an analog product that can be easily integrated into existing devices.

www.sensirion.com/gasflow

900MBPS MIPI D-PHY SUPPORT FOR LATTICE'S MACHXO3 FAMILY

Lattice Semiconductor announced that its award-winning MachXO3 family of devices supports 900Mbps per lane operation for MIPI D-PHY interfaces, enabled by the latest Lattice Diamond version 3.6 design tool suite software update. This means that MachXO3 devices can now be used to bridge a wide variety of image sensors and displays with MIPI D-PHY, CSI-2 or DSI interfaces at speeds of up to 900Mbps.

Lattice Diamond design software is a complete suite of FPGA design tools with an easy-to-use interface, efficient design flow, superior design exploration and more. The new software release, version 3.6, will enable MachXO3 customers to design more powerful yet low power, small form-factor FGPA bridging and I/O expansion solutions.

MachXO3 FPGAs are increasingly becoming popular choices for image sensor and LCD bridging solutions in cameras, displays and machine-vision applications.

www.latticesemi.com

HIGH-SENSITIVITY CURRENT PROBES FOR YOKOGAWA OSCILLOSCOPES

Two new high-sensitivity current probes are now available for Yokogawa's families of mixed-signal oscilloscopes and ScopeCorders.

The 701917, covering a frequency range from DC to 50MHz, and the 701918, covering DC to 120MHz, offer sensitivities ten times higher than previous models (typically 1V/A), along with low-noise levels of typically 60µA RMS. They are ideally suited to the measurement of low-level currents from about 1mA to 5A.

The probes feature a slim, lightweight sensor head which is easy to use in confined spaces. Automatic zero adjustment and demagnetisation are accessed via a button on the termination box, making setup quick and easy. An overload/jaw-unlocked warning is included for added safety.

to the instrument is via the front-panel BNC connector. Power can be from the oscilloscope's probe power option or a separate probe power supply.

tmi.yokogawa.com

TWO-DIMENSIONAL SPEED AND DIRECTION SENSOR IC

The new A1262 from Allegro MicroSystems Europe is a unique dual-channel Hall-effect latch featuring two-dimensional (2D) sensing via a combination of vertical and planar Hall elements.

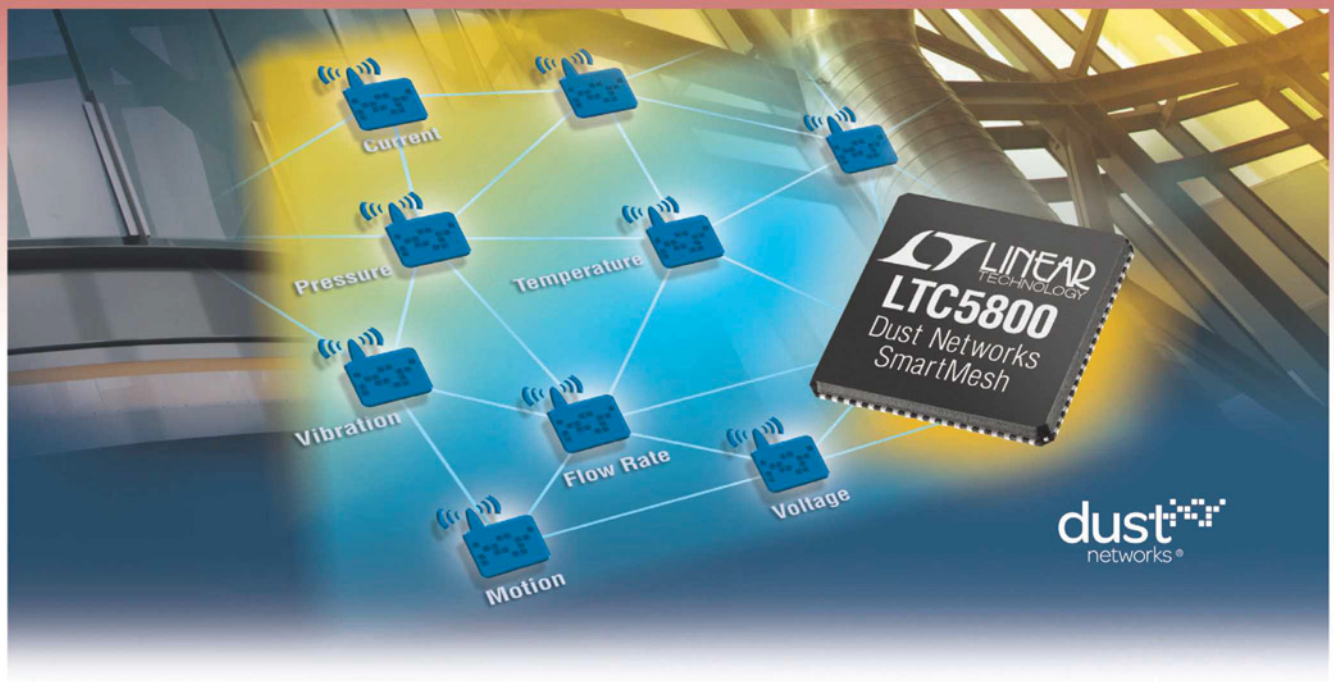
The quadrature outputs of the A1262 allow rotation direction and position to be determined in applications such as sensing a rotating ring-magnet target. The unique 2D operation of the combined planar and vertical Hall elements allows the user to achieve an ideal 90° of phase separation between channels which is also inherently independent of ring magnet geometry and pole pitch.

Using the A1262, system designers can achieve new mechanical configurations not necessarily feasible with traditional planar Hall sensors, including replacing pairs of through-hole single-inline packaged devices with a single, tiny surface-mount SOT23 IC.

The new device is suitable for the automotive, industrial and consumer markets.

www.allegromicro.com

Wireless Mesh Network. Wired Reliability.



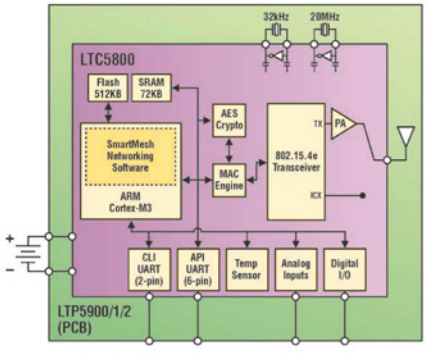
Every Node Can Run on Batteries for >10 Years at >99.999% Reliability

The Dust Networks LTC®5800 and LTP®5900 product families from Linear Technology are embedded wireless sensor networks (WSN) that deliver unmatched ultralow power operation and superior reliability. This ensures flexibility in placing sensors exactly where needed, with low cost "peel and stick" installations. The highly integrated SmartMesh® LTC5800 (system-on-chip) and LTP5900 (PCB module) families are the industry's lowest power IEEE 802.15.4e compliant wireless sensor networking products.

Features

- Routing Nodes Consume <50µA Average Current
- >99.999% Reliability Even in the Most Challenging RF Environments
- Complete Wireless Mesh Solution – No Network Stack Development Required
- Network Management and NIST-Certified Security Capabilities
- Two Standards-Compliant Families: SmartMesh IP (6LoWPAN) and SmartMesh WirelessHART (IEC62591)

Highly Integrated LTC5800 and LTP5900 Families



Info and Purchase

www.linear.com/dust

Linear Technology (UK) Ltd.,
3 The Listons, Liston Road,
Marlow, Buckinghamshire,
SL7 1FD, United Kingdom.

Phone: 01628 477066
Fax: 01628 478153
Email: uksales@linear.com

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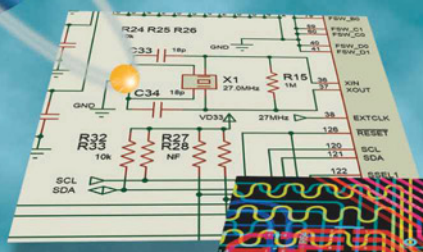
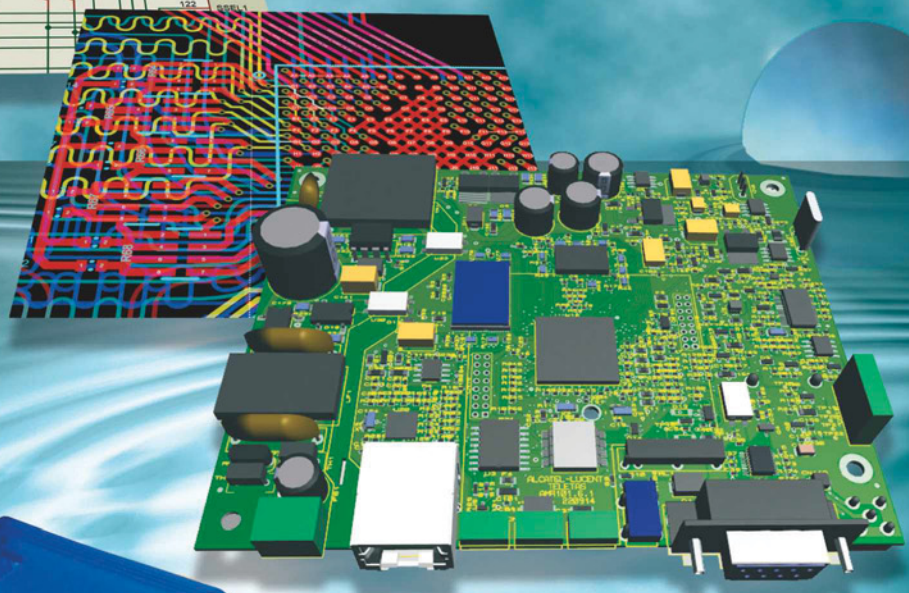
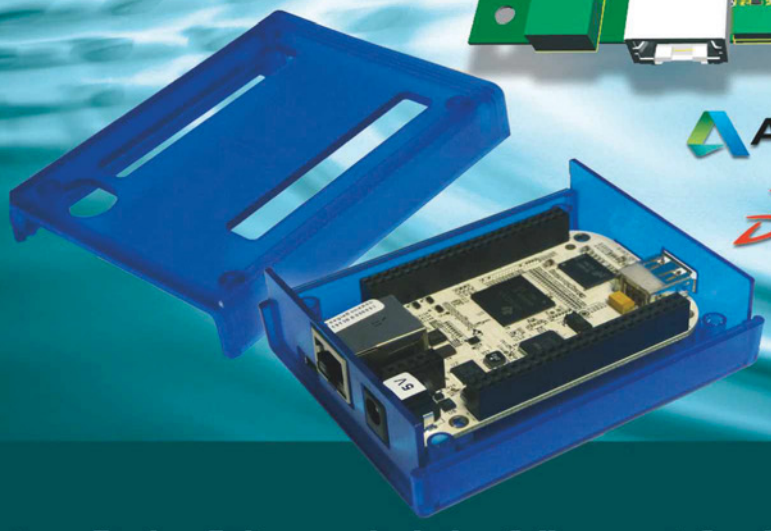
PROTEUS 8.3

ECAD to MCAD made easy

Data Exchange with STEP/IGES







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SOLIDWORKS

The Proteus Design Suite now includes full support for data exchange with Mechanical CAD packages via the STEP/IGES file formats. This allows you to better visualise your design and helps quickly solve fixtures, fittings and casement problems.

Import 3D STEP/IGES models for your parts and visualise inside the Proteus Design Suite. Export your completed board to Solidworks or other MCAD software.

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