

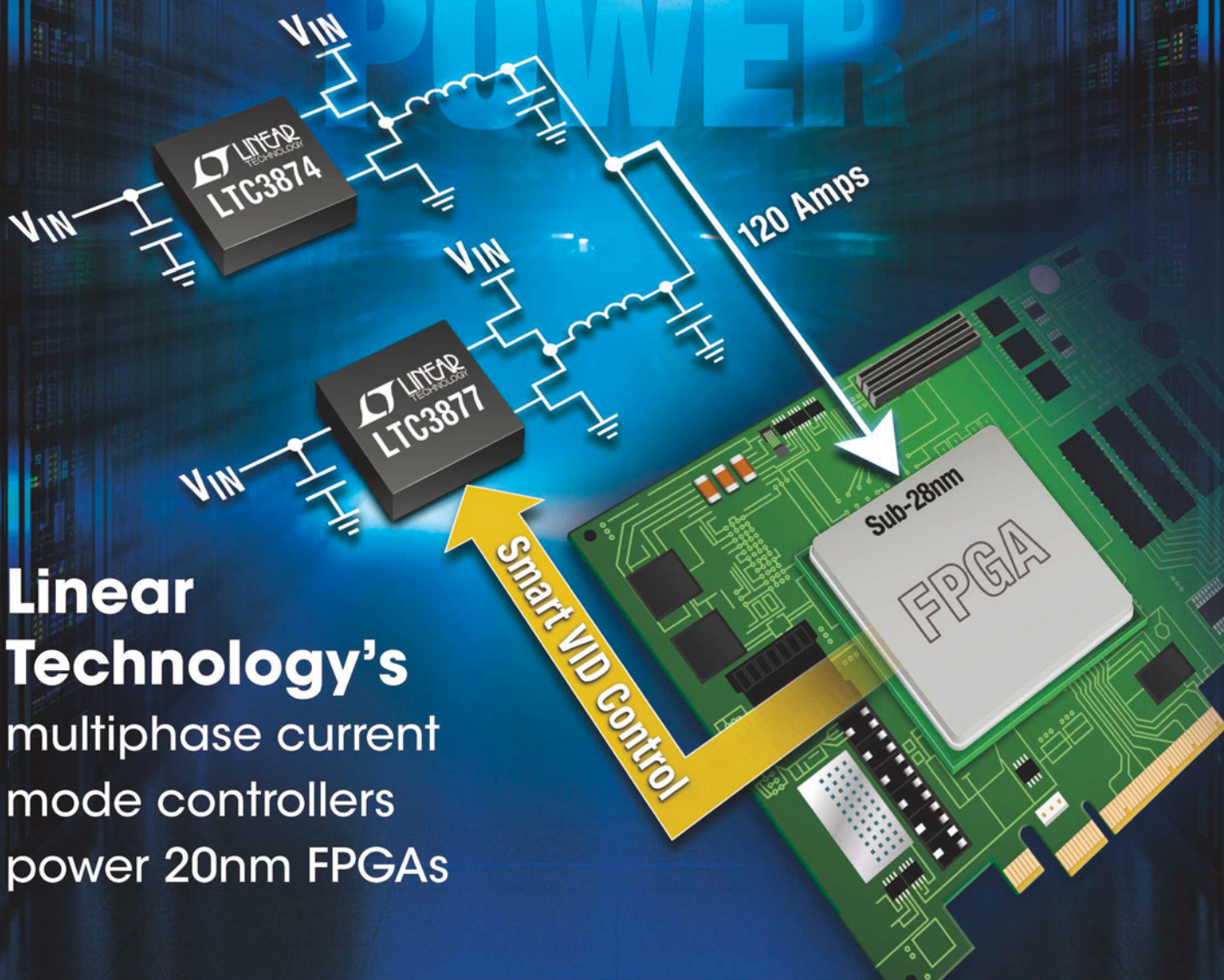
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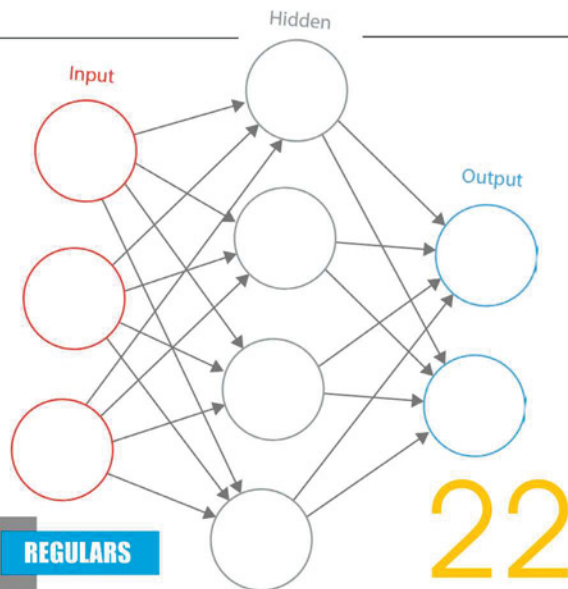
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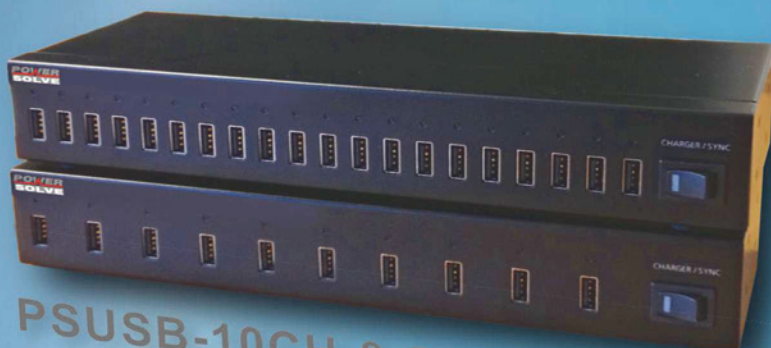
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FUTURE AUTOMOTIVE INDUSTRY ADVANCES



The automotive industry has gone along a long and winding road. In just 120 years this business has blossomed from Henry Ford's modest 1896 Quadricycle to the 40 million new cars that now roll off the world's production lines every year, each one boasting features like front and rear radar, traffic sign recognition, pedestrian detection and self-parking. And, we expect still more innovations to come:

1. Autonomous Cars

Google unveiled its first autonomous vehicle in December 2014, creating a new wave of excitement for the media and consumers alike. However, fully autonomous vehicles are not expected to be the norm for at least five years.

2. Driver Override Systems

Similar to autonomous technology, driver-override systems will enable vehicles to make their own decisions through advanced sensors and multiprocessing, regardless of the driver's commands. Brake override and smart pedals are fully integrated electronic systems in which a multitude of sensors in the vehicle transmit signals to the electronic control unit (ECU). The ECU can recognise when the gas and brake pedals are being pressed at the same time. Since this isn't how people normally drive, the car's central computer will take over and slow it down safely. There are several ways of doing this, depending on the individual manufacturer, but it could be anything from adjusting the throttle position to reducing the amount of fuel getting to the engine, with the same ultimate goal: a safe stop.

3. 3D Printing

Advancements in metal-additive manufacturing are making 3D printed car-parts a viable and competitive market. 3D-printed systems are already appearing in many of the world's powerful cars, particularly in Formula 1.

Advantages of 3D printed parts or additive manufacturing include freedom of design, lighter weight, lower complexity, greater customisation and better performance. The additive manufacturing process also allows product designers to add internal air cooling channels within parts, particularly useful in an environment that is subject to high temperatures and overheating.

“Advancements in metal-additive manufacturing are making 3D printed car-parts a viable and competitive market

As for fully 3D-printed cars, some punters predict they could hit the road as soon as this year, and the concept vehicle called Strati, by Local Motors, may be one of them.

4. Connectivity

Internet connectivity is already almost everywhere, but for the average car full connectivity is expected by 2020. In the coming years more sweeping changes will come to in-car connectivity, allowing cars to have not only secure Internet access but wireless local area networks too. By using onboard sensors and Internet connectivity, vehicles will be able to optimize their operation and maintenance, with increased comfort and safety for drivers and passengers alike.

5. Augmented Reality

GPS and satnavs have been getting motorists from A to B for over two decades, but advanced augmented-reality dashboards will go beyond this. Such dashboards will overlay a digital display on the windscreen, highlighting hazards and displaying directions to the driver with improved clarity and safety.

While all of these advancements are very exciting, factors such as connectivity, safety and overdependence on technology may prove of great concerns to manufacturers as well as consumers over the years to come – issues that many will focus on with great intensity. The automotive industry has advanced rapidly in the past century, from the first diesel engines of the early 1900s to today's cars that have the computing power of 20 PCs, contain around 100 million lines of code and can process up to 25GB of data every hour. This is certainly set to change yet again, and the numbers can only increase.

Jonathan Wilkins is Marketing Director of industrial automation parts supplier European Automation

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EUROPEAN ENERGY RESEARCH PROJECT SUCCESSFULLY COMPLETED

The E2SG (Energy to Smart Grid) research project, headed by Infineon and supported by 29 partners, has completed its goal of laying foundations for greater stability, energy efficiency and data security in the smart grid.

The project started in 2012 with a budget of €64m, with half contributed by the project

partners, and the rest by the European Commission's initiative ECSEL JU and each participating project partners' country of origin.

The smart grid can be described as the Internet of Things at the power supply level. It is a power network with interconnected nodes that exchange information about processes and

their environment to generate more efficient on-demand power. The research results of the E2SG project will allow more sustainable energy production and more efficient energy conversion. For example, a bi-directional voltage converter – with efficiency of over 96% – will facilitate efficient power supply of electricity from different energy sources. This supports the use of renewable energies and makes the power supply more flexible and more stable. By using optimized MOSFET power switches with over 10% lower on-resistance in voltage systems such as power supplies, together with advanced high-voltage technologies, power and conversion losses can be reduced, along with CO₂ emissions.

The project also focused on making the smart grid more reliable and secure to protect it from unauthorized access. One of the E2SG project components was the development of new security controllers with advanced encryption.

There are 29 partners from nine European countries in the project, among them Infineon Technologies, NXP Semiconductors, ON Semiconductor and STMicroelectronics.



METAL-ORGANIC FRAMEWORKS PROMISE WILL LEAD TO IMPROVED MICROELECTRONICS DEVICES

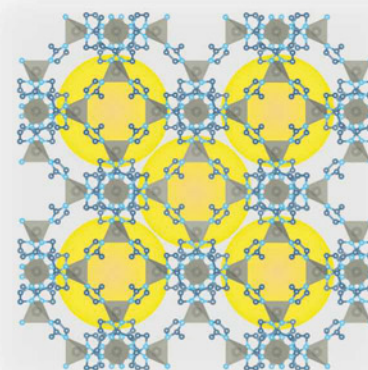
Bioscience engineers from KU Leuven, Belgium, have developed an alternative method for producing metal-organic frameworks (MOFs), a new type material with nanoscale pores. Such materials can be formed into very thin films for use in microelectronics.

MOFs were recently developed and consist of a nanoporous grid of organic molecules and metal ions. They take shape as the organic molecules push the metal ions apart, developing a regular pattern of tiny holes, or nanopores.

The size of the pores can be tuned at the nanoscale level. The internal surface of an MOF, formed by all these pores, varies in size from 1,000 to 5,000 square metres per gram of material.

MOFs can be seen as microscopic sponges that absorb a lot, opening the doors to many interesting applications, especially when the production methods for these materials develop and become less costly, such as using vapours and gases instead of the traditional liquids.

"This alternative production method opens up new possibilities for MOFs in terms of applications and industries. Chemical vapour deposition is a common technique in nanofabrication. Therefore, new MOF applications can be developed relatively quickly: gas sensors, nanochip components and improved batteries," said Ivo Stassen from KU Leuven.



3D structure of the metal-organic framework. The yellow sections are the nanopores

USING CONVENTIONAL POLYOLEFIN SEPARATORS IN LITHIUM ION BATTERIES CARRIES RISK

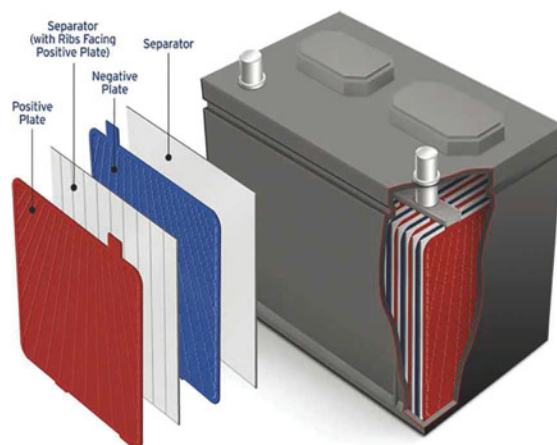
A team of investigators led by Dreamweaver International has investigated the effects of heat and nail penetration on lithium ion cells by performing autopsies on cells post-test. The investigators found that conventional separators shrink, melt, crack, split and burn under extreme conditions, while separators made of more thermally-stable materials show much less damage, and in some cases none of these effects.

Cells were built with identical construction except for the separators, and then several conventional safety tests were performed. The two most remarkable were a 170°C hot-box and nail penetration. In the hot-box, cells made with conventional separators underwent thermal runaway, bursting the package and venting the electrolyte, while cells made with more thermally-stable separators continued to hold their voltage for the full one-hour test and still function.

The biggest surprise came with the nail penetration test, in which cells made with ceramic coated polyolefin separator underwent immediate thermal runaway, the surface of the cell rising within two minutes to over 100°C.

These cells were then sent to Spectra Power, an independent battery facility, to be disassembled and investigated.

"These investigations show that while a shutdown function may be attainable in thermal equilibrium, in a fast, dynamic, thermal event, such as those that might happen in an electric vehicle or a hoverboard, the shutdown often attributed to conventional separators will not uniformly turn the cell off. Portions at lower temperatures will still function and can deliver energy to other parts of the



Conventional separators shrink, melt, crack, split and burn under extreme conditions

cell that will continue to overheat," said Professor Sungjin Cho of the Joint School of Nanoscience and Nanoengineering in the US.



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MULTIPHASE CURRENT MODE CONTROLLERS POWER THE LATEST GENERATION 20 NANOMETER FGAs

By Bruce Haug, Senior Product Marketing Engineer, Linear Technology

The sub-28 nanometer Field Programmable Gate Arrays (FGAs) now available feature the industry's only hard floating-point digital signal processing (DSP) blocks with speeds up to 1,500 Gbps floating-point operations. Built on sub-28nm process technology, these FGAs provide up to 17.4Gbps for long-reach backplane support and with data rates up to 28.3Gbps to bring high-end bandwidth performance into midrange devices.

These new FGAs require up to 105A to power their cores and use VID (Voltage Identification) 6-bit interface to tightly control its operating voltage in 10mV steps for optimum performance. For such high currents it is critical to minimize power supply conduction losses by making the resistance of the current sense element as low as possible. However, a low-resistance current sensing element produces a lower ramp voltage which is not conducive for stable operation when using a current mode controller. Low ramp voltages causes a current mode controlled switching power supply to have significant jitter and it may become unstable. Accordingly, a voltage mode controller is routinely used instead, even though it has performance deficiencies and potential reliability concerns.

Nevertheless, a current mode controlled switching power supply has several advantages over a voltage mode alternative. These are as follows:

1. Higher reliability with fast, cycle-by-cycle current sensing for output short circuit and overload protection.
2. Simpler feedback loop compensation
3. Accurate current sharing in high current multiphase designs.
4. Faster transient response.

However, for high current outputs, typically greater than 20A per phase, sub-milliohm DCR ferrite inductors are required for high efficiency. However, these inductors will not produce enough of a voltage ramp signal for a current mode controller to be stable under all operating conditions. And so, a voltage mode solution becomes more attractive. That is, until now.

The recently released current mode dual phase DC/DC step-down controller, LTC3877, has the ability to sense very low ramp voltages and maintain excellent stability. It operates with true current mode control and can be used with very low DC resistance (DCR) power inductors down to 0.3mΩ, due to its novel sensing scheme that enhances the signal-to-noise ratio of the current sense signal. This sensing scheme dramatically reduces the switching jitter normally associated with low DCR resistance applications and the LTC3877's adjustable current limit can be configured for very low sense voltages from 10mV to 30mV to minimize power loss. This lower inductor DCR allows the maximum output current to be as high as 30A per phase due to the reduced inductor power loss and the ability to sense a lower ramp voltage. As a result, a 4-phase design is able to support a 120A load.

The LTC3877 also incorporates 6-bit VID control that enables 10mV step resolution of the output voltage, a necessary feature

when powering FGAs and ASICs with very tight input voltage tolerances. Up to 12-phases can be paralleled and clocked out-of-phase to minimize input and output filtering. The LTC3874 phase extender can also be used for high phase count applications which complements Linear Technology's low DCR peak current mode controllers and provides all the necessary functions for multiphase slave designs, including accurate phase-to-phase current sharing for steady state and dynamic loads. When outputs are paralleled, the LTC3877 maintains better than ±2.5% current mismatch between phases, making it ideal for very high current requirements up to 300A.

The LTC3877 maintains ±1% output voltage accuracy (including internal resistor divider and differential remote sense amplifier errors) over a -40°C to 125°C operating temperature range. Dual onboard differential amplifiers enable remote output voltage sensing for both outputs. High step-down ratios at high operating frequencies are possible due to its 40ns minimum on-time. The LTC3877 has a selectable fixed operating frequency from 250kHz to 1MHz or it can be synchronized to an external clock. Its powerful onboard all N-channel gate drivers minimize MOSFET switching losses while its DCR temperature compensation maintains a constant current limit threshold over a broad temperature range. Additional features include adjustable soft-start or tracking, foldback current limit, short-circuit soft recovery, output overvoltage protection and two power good output voltage signals. The LTC3877 is housed in a 44-lead 7mm x 7mm QFN package.

As a result, the LTC3877 and LTC3874 combination can be used to provide power for the core rail by taking advantage of the 6-bit VID interfaces to reduce the FGA's static and dynamic power consumption.

120A Current Solution with VID

The simplified schematic in Figure 1 shows the LTC3877 being used in conjunction with the LTC3874 dual channel phase extender. The resultant 4-phase design is able to produce up to 120A with the VID controlled output voltage ranging from 0.6V to 1.23V. Each phase is clocked out-of-phase resulting in lower output ripple and faster load step transient response.

The full load efficiency for a 1.2V output at 120 amps is 88.8% and peaks to 92% at 60A as shown in Figure 2. This high efficiency is a result of the strong onboard gate drivers, short dead times of the two controller ICs, MOSFET selection and low DCR ferrite inductors.

The inductors used in this design have a wire resistance of 0.32mΩ, resulting in the four inductors having a combined DCR power loss of $(120A/4)^2 \times 0.00032 \times 4 = 1.2$ watts, using the equation $P_{LOSS} (DCR) = I^2 \times DCR \times \# \text{ of phases}$. A normal current mode controller, without the sub-milliohm DCR sensing feature would need an inductor resistance of at least 1mΩ, which results

in a higher power loss of $(120\text{A}/4)^2 \times 0.0010 \times 4 = 3.6$ watts. This lower resistance inductor design reduces the power loss by 2.4W and increases the full load efficiency by 1.3% when using it with a 1.2V output.

The LTC3877 comprises two current sense pins (SNSD+ and SNSA+) to acquire the inductor ramp voltage signal and processes it to provide a 14dB signal-to-noise ratio improvement to the low voltage sense signals. The current limit threshold is a function of the inductor peak current and its DCR value and can be accurately set from 10mV to 30mV in a 5mV steps. The part-to-part current limit error is only 1mV over the full temperature range assuring excellent accuracy.

In addition, the LTC3877 includes two differential amplifiers for applications that require remote sensing. Differentially sensing the load greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget. The LTC3877 uses a constant frequency peak current mode control architecture, it guarantees cycle-by-cycle peak current limit and excellent current sharing between power supplies phases. It is especially well suited to low voltage, high current supplies because of a unique architecture that enhances the signal-to-noise ratio of the current sense circuit. The improved signal-to-noise ratio minimizes jitter due to switching noise, which could potentially corrupt the signal.

Both the LTC3877 and LTC3874 use a proprietary DCR current sensing architecture designed for sub-milliohm DCR sensing which allows for tight control of the current sharing and current limit. Figure 3 shows the current sharing performance of the 4-phase converter in Figure 1. The current sharing error is less than a 1mV between phases when sensing the voltage drop across the output inductors.

Conclusion

The LTC3877 allows the use of sub-milliohm DCR inductors in conjunction with its current mode control architecture for increased efficiency in high current applications. A current mode controller provides several benefits over a voltage mode controller of higher reliability with fast cycle-by-cycle current sensing, accurate current sharing between phases, simple feedback loop compensation and faster transient response. The LTC3877 is ideal for high current point-of-load VID applications, typically found in the latest generation of FPGAs, and can easily support up to 30A/phase (total 60A). For higher power applications, adding the LTC3874 phase extender allows for additional 30A/phase, for a total of 120A. Furthermore, the added efficiency gain minimizes the thermal design due to the reduced power loss of this converter combination.

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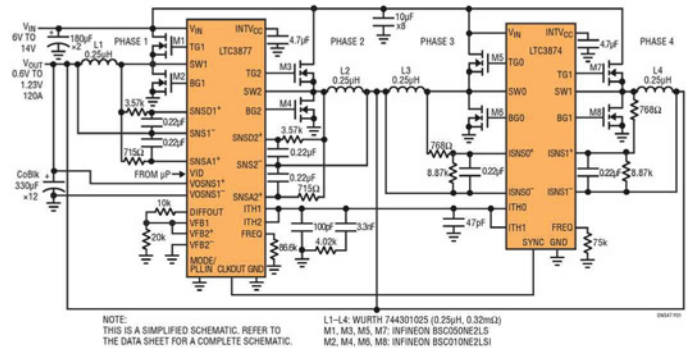


Figure 1: The LTC3877/LTC3874 Schematic for low Voltage 120A Output

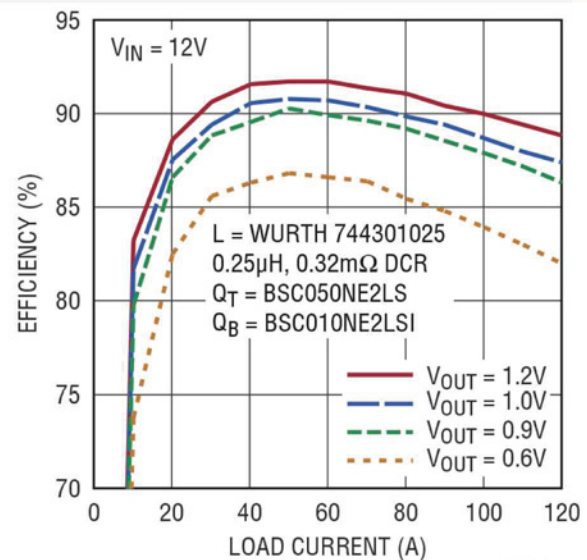


Figure 2: Efficiency of 4-Phase 120A VID Converter

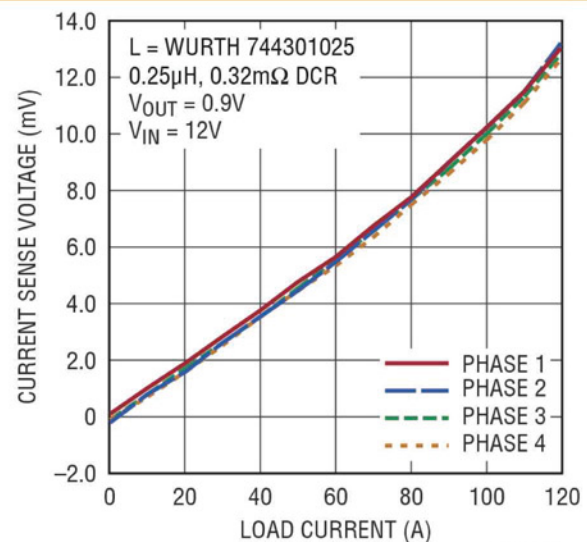


Figure 3: Current Sharing of the 4 Phases with the LTC3877 & LTC3874



Embedded Xpress

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

"X"

press" is actually (part of) the name of a new tool announced by Microchip at the Embedded World show in February. It's called MPLAB Xpress (<https://mplabxpress.microchip.com>) and it is much more than just MPLAB X bottled in a browser; see Figure 1. With it, Microchip has put the IDE in the cloud!

Your initial reaction may be one of two: "It's about time!" or "Why would anybody need anything like that?!"

"It's About Time"

A bunch of millennials might take this position first; after all, for them being online is part of the natural order of things. For them, not being available 24/7, everywhere and from any computing platform is the anomaly.

In the past few years, many integrated development environments

(IDEs) have moved to or have been created within the cloud, but whereas this is more naturally fitting in web application development (using javascript, HTML, CSS, PHP) and general computing (Java, Python, Ruby...), the embedded development community lagged. After all, the target system in embedded applications is intrinsically more physical.

"Why On Earth?!"

The other group, perhaps more varied in age and technical background, is now wondering what kind of benefits could be had by moving the development environment to the browser. They actually see more drawbacks than positives in this, and might therefore need more reassurance and an explanation.

IDE And Compiler In The Cloud

First the benefits: Modern IDEs have become very powerful but

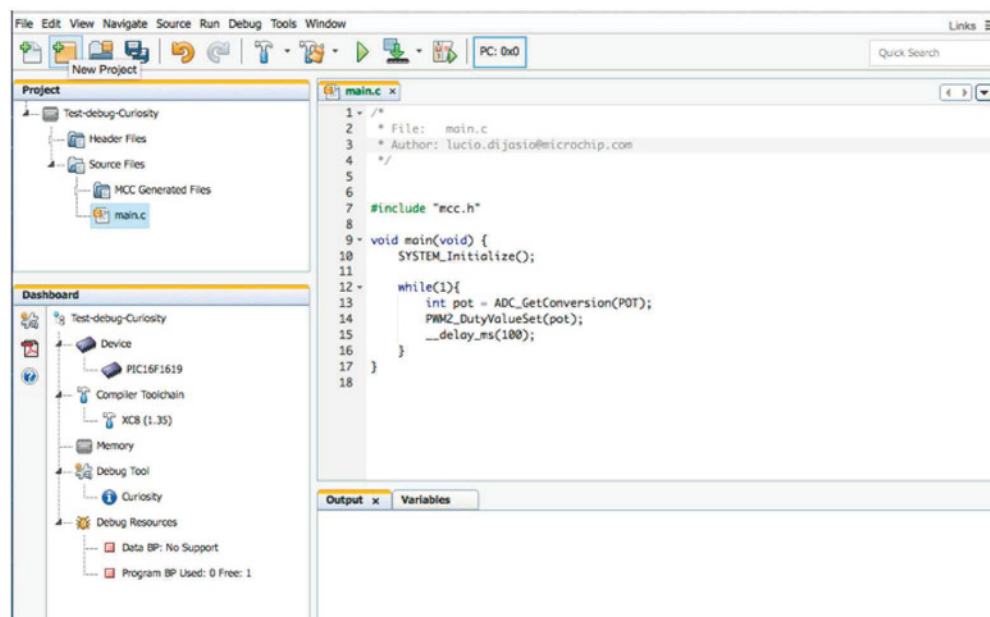
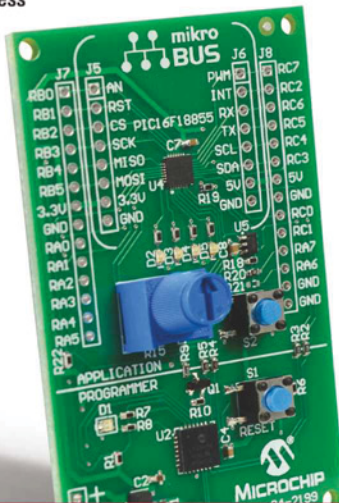


Figure 1: MPLAB X or MPLAB Xpress?

Figure 2: MPLAB Xpress evaluation board



are also large beasts that need frequent updates and maintenance. MPLAB X, which is based on the Netbeans (open source) project, covers thousands of different microcontroller models and is updated on a monthly cycle, each time requiring a download of approximately 350Mbytes. The C compilers that plug into it, MPLAB XC compiler suite, have a less frequent cycle but require approximately 100Mbytes. If we add a few more plugins, such as the MPLAB Code Configurator, we can quickly reach the half-GByte quota.

On top of that, we need to take into account the time spent to perform the actual installations and general maintenance. If you run even a small lab in a school or university, you know how much work is required to keep it all up to date and in good shape. In such environments there are also great concerns about permissions required to install applications on shared computing equipment.

Imagine the relief when all that work turns into a simple online login. Instantaneously, the most up-to-date revision of each

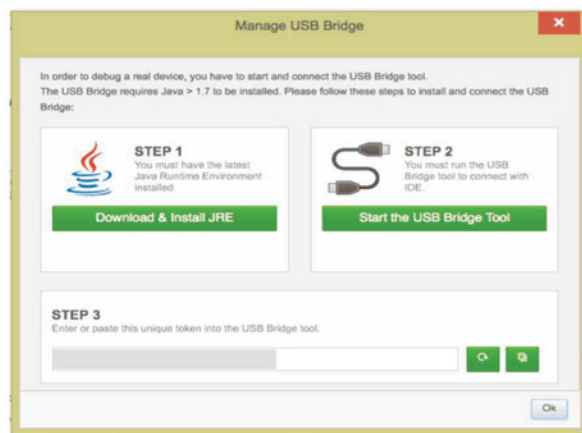


Figure 3: A USB bridge to standard microchip programmers and debuggers

component of the toolchain – or an archived one of your selection – becomes available to you.

However, being online adds totally new dimensions to the embedded development experience. Once an IDE is “virtualized” it can move quickly from workstation to workstation, and work started in the office (or class) can easily move to a new location. Sharing and communicating among close or geographically-dispersed teams becomes more natural in addition to being easier to set up and maintain.

Now, the few examples of Embedded IDE (and compiler) available today in the cloud, have been limited to a very restricted set of products, typically the latest and most recent product families launched and/or revolving around one or few specific development boards.

The MPLAB Xpress launch is dramatically different in that respect. In the usual Microchip horizontal approach, support is provided across the entire microcontroller portfolio, which includes over 1,000 models

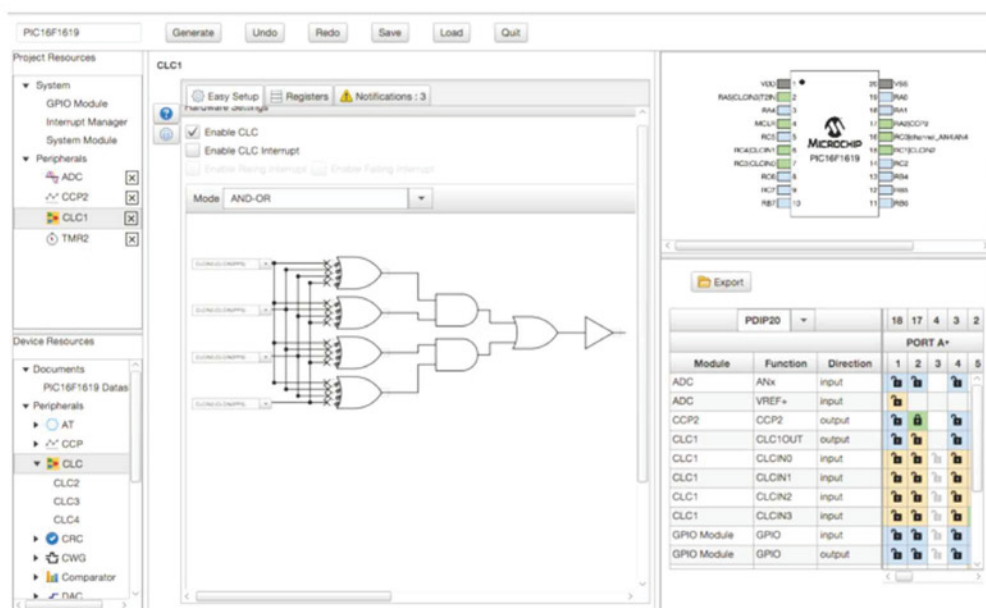


Figure 4: MPLAB Code Configurator 3.0 in the cloud

of 8-bit microcontrollers alone, new and old, from the very first PIC16C (in OTP technology!) to the latest PIC16F1 and PIC18.

Boards In The Cloud

So what about the hardware? As you might expect, the MPLAB Simulator has been included in the online toolchain, offering the most basic means of debugging for the simplest applications. Beyond that, there are two paths available for exploration:

1. Using the new MPLAB Xpress evaluation board (Figure 2), the first of a new series of inexpensive evaluation boards. This one features the latest PIC16F18855, a strong candidate to succeed the enormously popular PIC16F88x family/tradition of general-purpose microcontrollers, with the largest selection of core-independent peripherals.

These boards will trick your computer (PC, Mac or Linux) into thinking it is talking to a hard drive (USB mass storage), and by simply dragging and dropping your application executable (.hex) files into it, you can program the target, without needing drivers or installation.

The board will also automatically register your PC as a virtual serial port (USB-CDC), allowing the terminal program of your choice to connect directly to the target PIC microcontroller UART. Windows users will need to load an .inf file to enable this feature the first time, Linux and Mac users get it automatically.

2. Connecting via a USB bridge – a minuscule Java plugin (Figure 3) – to standard hardware debuggers and programmers such as the PICKit3 or directly to the Curiosity board and its built-in programmer/debugger.

This second method opens the door to the entire set of Microchip and third-party demonstration boards and, of course, any custom board.

MCC In The Cloud

The MPLAB Code Configurator tool is the newest incarnation of the MCC 3.0 (Figure 4), in beta for the past six months, redesigned entirely for integration with the cloud compiler and IDE. In my opinion, the result of the integration effort is greater than the sum of the parts.

Previous or competing online IDEs simply offered access to libraries or integrated new simplified subsets (a la Arduino). With MPLAB Xpress we get the ultimate rapid development tool, ready to configure not only our peripherals but also to integrate and configure for our specific needs entire library modules such as touch and proximity sensing, LIN communication, a lightweight TCP/IP stack, or a bootloader, and many more that will be added in the coming months.

Performance Concerns

When thinking about a development environment that requires constant presence online, many may immediately start to worry about

the speed and cost of the connection. Having been initially among the doubters, I had a particularly critical eye for this aspect of the online experience. After all, in my job I travel a lot, and I often get poor connections, frequently only via my mobile phone 3/4G and, more often than not, roaming.

After having played with the tool extensively for a couple of months (through the alpha and beta stages), I have only words of great appreciation for the developers. MPLAB Xpress is an excellent piece of AJAX technology. It makes the most use of your browser's ability to run code locally (asynchronously and using javascript,

hence the A and J part of the acronym), so the application (AX) is always very responsive and does not require every single keystroke to be sent to a server.

File transfers do occur, but only when a file is saved or opened for editing. Those are typically small text files (.c, .h, .hex) easily exceeded in number and size by the average images (and ads) loaded by any modern website.

When compiling your code instead, the server is working entirely on the local copies and the process is surprisingly fast. In fact, I have seen the server regularly outperform my

laptop and the little Xpress board programming the target faster than in my usual experience with a PICKit3.

Security Concerns

The concerns about security of any cloud application are a delicate subject.

Clearly, millions of dollars are being spent in marketing by very rich and large corporations to convince us that our data (or code in this case) is perfectly safe once in the cloud. The best arguments I have heard so far from the two opposite sides go more or less like this:

- **Doubters:** If there is sufficient value (motivation), attackers will eventually find a way in. I find this to be a rule that is generally true for all things, and that includes any private corporation code "vault" too.

- **Believers:** The (large) companies that do provide cloud service are also very motivated and in the best position to use very specialized resources to keep the data secure. These are probably far superior to the resources the average business organization IT department can afford.

In the coming years each of us will be exposed to this technological dilemma and we will have to choose whether the risks are greater than the benefits offered by a multitude of new cloud services. So, whether a doubter or a believer, I think you should give MPLAB Xpress a try – it's free. The sheer number of devices supported and the integration with rapid development tools such as the new MCC put MPLAB Xpress in a class of its own.

I am excited to see how new generations will use this tool and how embedded control will change in the era of the cloud. To be continued... ●

Figure 5: MPLAB Xpress IDE logo





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Using accelerometers with microcontrollers

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY IN CYPRUS

An accelerometer is an electromechanical sensor for measuring acceleration. Acceleration can be static – caused by the earth’s gravity, or dynamic, caused by a moving or vibrating object. By measuring the static acceleration of an object we can find its angle in relation to ground. By sensing the dynamic acceleration, the performance of a moving object can be analyzed and we calculate the forces acting on that object, such as speed, orientation, distance travelled and so on.

Prolific Use Of Accelerometers

For many years accelerometers were only found in expensive professional equipment. Nowadays, they are found in most smart mobile devices, especially for screen orientation and gaming.

Laptop manufacturers use accelerometers to protect hard drives from damage if the laptop is accidentally dropped; the accelerometer detects the sudden freefall and disengages the disk-drive heads so that they don’t crash on the platters.

Camera manufacturers use accelerometers to stabilise a camera and to detect and eliminate camera shake during picture taking.

Heating appliances, such as electric heaters and electric irons, have built-in accelerometers that detect when they fall over and switch them off to avoid causing fire.

Vehicle manufacturers use accelerometers to analyze the dynamic performance of new vehicles, to determine vehicle acceleration, the time it takes for the vehicle to reach a certain speed in a given period.

Vehicle crash safety measurements are based on accelerometers

where the deceleration and position of a vehicle are measured before, during and after a test crash. Vehicle accidents are detected by accelerometers, which cause the air bags to deploy.

Accelerometers are also used in other parts of vehicles, such as detecting the angle a vehicle makes as it goes around a sharp bend, measuring the tilt of the headlamps, or the roughness of a road and adjusting the car accordingly for maximum comfort, and so on.

Accelerometers are also used heavily in modern defence and aerospace applications, such as measuring the tilt angle of artillery, the forces acting on an aircraft, in short-range missiles, guided munitions and inertial navigation, and various other military equipment and land vehicles.

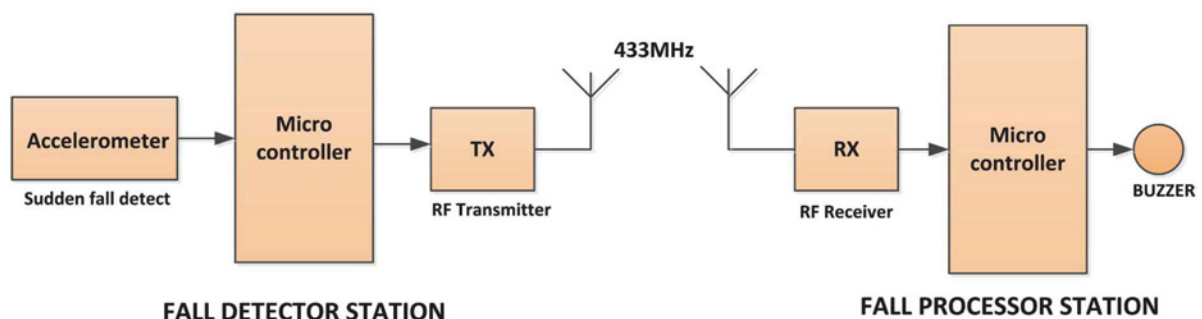
Accelerometers also find applications in the medical field. For example, the movement of a patient can be analyzed using accelerometers. The gait changes of older patients can be identified and measures taken to help balance and avoid sudden falls.

Accelerometer Types

There are many different types of accelerometers. Perhaps the oldest type is the mechanical one which consists of a mass attached to a spring and suspended inside a case. During acceleration, the mass and the spring move with a displacement proportional to the acceleration. By measuring the distance the spring stretches, we can measure the force and acceleration of the body.

Capacitive accelerometers are electromechanical devices where the distance between the plates of a capacitor changes with movement. By measuring the change in capacitance, we can

Figure 1: Block diagram of the designed system



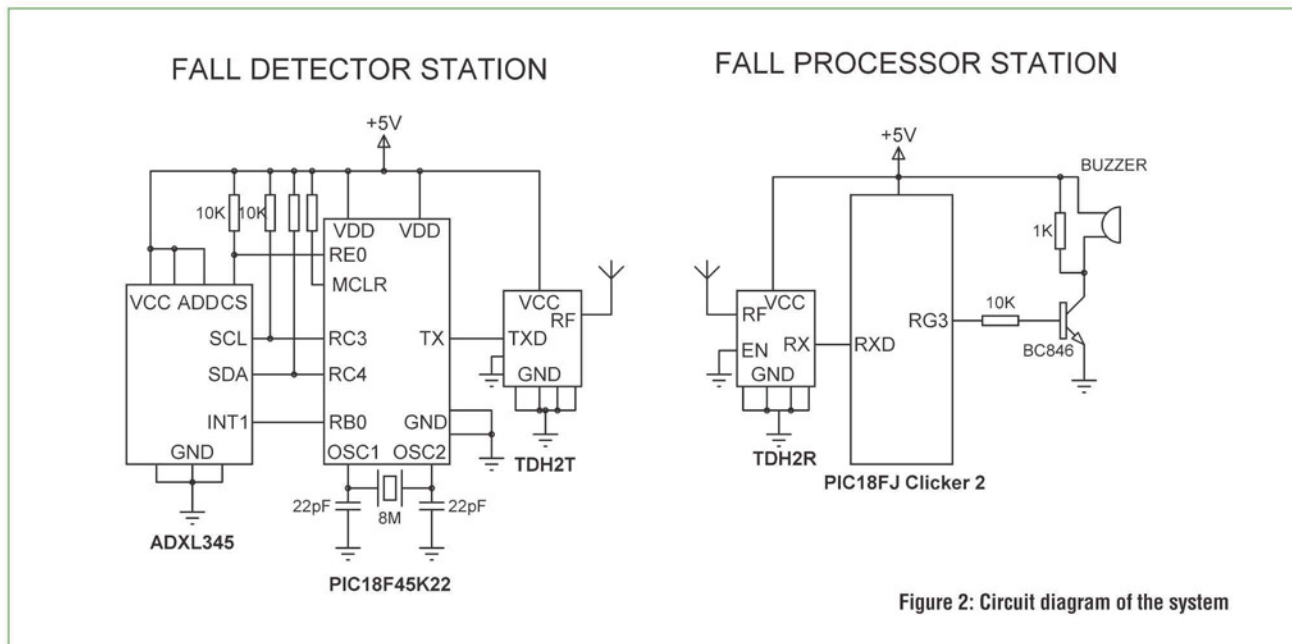


Figure 2: Circuit diagram of the system

determine the acceleration of the body.

In piezoelectric crystal-based accelerometers, the crystal is attached to a mass, and when the mass moves and squeezes the crystal, a tiny voltage is generated which can be measured and related to the acceleration of the body.

Hall-effect accelerometers operate by measuring the change in magnetic field when a Hall-effect sensor moves under the influence of an external force.

Modern accelerometers are based on MEMS (micro electro-mechanical systems) technology. The first MEMS-based accelerometer was developed in 1979 at Stanford University but took over 15 years to become available in large volumes. These are tiny semiconductor devices where polysilicon springs suspend the MEMS structure above the substrate such that the sensor body can move freely. Acceleration of the device causes deflection of the sensor body from its at-rest position. This movement is measured using differential capacitors placed around the four sides of the sensor body. Both static and dynamic acceleration can be measured; the output is usually a voltage proportional to the acceleration. Some accelerometers output a pulse-width-modulated (PWM) voltage.

Accelerometers can be used to measure the acceleration in either two or three axes. MEMS-based accelerometers have the advantages of being very small and very light; they consume very little power and are low in cost.

Selecting An Accelerometer

Here are some of the decisions to be made before selecting an accelerometer:

- **Output voltage:** Accelerometers can have analog or digital output voltages. The decision here depends on the required

accuracy and the availability of an analog-to-digital converter (ADC). Digital accelerometers usually output parallel binary (e.g. 2's complement) data proportional to the acceleration. Some digital accelerometer outputs are in the form of PWM signals.

- **Axes:** This choice depends entirely on the application, since accelerometers are available as either 2-axis or 3-axis devices.
- **Maximum Output Level:** In general, for static measurements $\pm 1.5G$ accelerometers are enough. For measuring the motion of a vehicle or a fast moving object, $\pm 2G$ or over may be required.
- **Bandwidth:** For static applications, a bandwidth of 50Hz is usually sufficient. For dynamic applications, at least 100Hz or higher may be required.

The System's Design

Here, I present an accelerometer- and microcontroller-based radio telemetry system (see Figure 1) to be worn by a person, to detect a sudden fall and send an alarm to a remote station.

The system consists of two stations: Fall Detector and Fall Processor. The Fall Detector station will detect sudden falls via an accelerometer and a signal sent to a microcontroller, which in turn transmits an alarm message through an RF transmitter module.

At the Fall Processor station, the received alarm message is handled by a microcontroller, and a buzzer is turned on to sound an alarm. This is a simple example for use by one person only. In real life, more than one person can be equipped with a Fall Detector system, each with a unique identifier.

The circuit diagram of the system is shown in Figure 2. The Fall Detector station uses the EasyPIC V7 development board, incorporating the medium range PIC18F45K22 microcontroller, operated with an 8MHz crystal. A 3-axis Accel Click board (see Figure 3) with an ADXL345 accelerometer chip on board is used

Figure 3: Accel Click board (ADXL345)

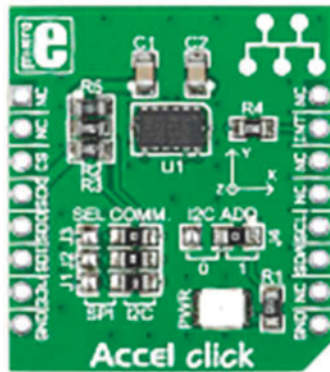
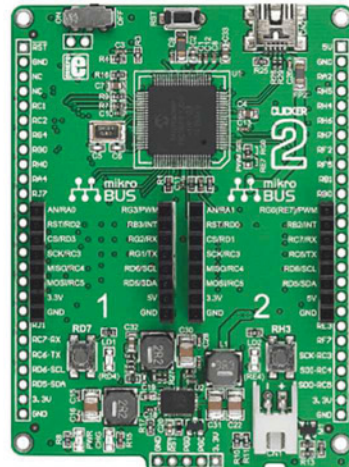


Figure 4: PIC18FJ Clicker 2 board



in the design and is interfaced to the microcontroller with an I2C bus through the SCL and SDA clock and data lines respectively. The interrupt output of the accelerometer (INT1) is connected to the external interrupt input pin (RBo) of the microcontroller. ADXL345 can be used to detect several events such as single tap, double tap, activity, inactivity and sudden freefall. The chip can be programmed to generate interrupts when one or more of these events occur.

In this system the chip is programmed to generate an interrupt when a sudden freefall is detected. The UART transmit output of the microcontroller (TX) is connected to a TDH2T radio telemetry transmitter module.

On the Fall Processor side, a compatible radio telemetry receiver module TDH2R is used to pass the received alarm message to a PIC18FJ Clicker 2 (see Figure 4) microcontroller development board, incorporating a PIC18F87J50 microcontroller and operating with an 8MHz clock. A Buzzer Click board is plugged into socket 1 of the board. The buzzer is activated when a sudden fall is detected.

TDH2T and TDH2R are compatible 433.925MHz UHF radio transmitter and receiver modules respectively. Both are multi-channel, 9600 baud, half-duplex, professional quality radio modems, operating with +5V power supply (50mA transmitter, 22mA receiver). Transmitter output power is +14dBm, while receiver sensitivity is

```
//ADXL345 register definitions
#define POWER_CTL           0x2D
#define INT_ENABLE          0x2E
#define THRESH_FF          0x28
#define TIME_FF            0x29
#define DATA_FORMAT       0x31
#define ACCEL_ADDRESS      0x3A

sbit ACCEL_CS at LATEo_bit;
sbit ACCEL_CS_DIR at TRISEo_bit;

//
// Write to I2C bus
//
void ADXL345_Write(unsigned short address, unsigned short data1)
{
    I2C1_Start();
    I2C1_Wr(ACCEL_ADDRESS);
    I2C1_Wr(address);
    I2C1_Wr(data1);
    I2C1_Stop();
}

//
// Initialize the accelerometer (adjust as required, see ADXL345 Data
// Sheet)
//
void AccelInit()
{
    ADXL345_Write(INT_ENABLE, 0x04);
    ADXL345_Write(THRESH_FF, 0x06);
    ADXL345_Write(TIME_FF, 0x14);
    ADXL345_Write(DATA_FORMAT, 0);
    ADXL345_Write(POWER_CTL, 0x08);
}

//
// Interrupt service routine. Send an Alarm message to the Fall
// Processor
//
void interrupt(void)
{
    UART1_Write_Text("FALL-J.JONES:");
    INTCON.INT0IF=0;
}

//
// Start of MAIN program
//
void main()
{
    ANSELB = 0;           // Configure PORTB as digital
    ANSELC = 0;           // Configure PORTC as digital
    ANSELE = 0;           // Configure PORTE as digital
    UART1_Init(9600);      // Initialize UART
```

Continued on facing page >


```

TRISB = 1;           // Configure RBo as input
TRISC = 0x10;
ACCEL_CS_DIR = 0;    // Enable accelerometer
ACCEL_CS = 1;
I2C1_Init(100000);   // Initialize I2C Bus
AccelInit();         // Initialize accelerometer

INTCON.INT0IE = 1;   // Enable RBo pin external
interrupt
INTCON2.INTEDG0 = 1; // Interrupt on rising edge
INTCON.GIE=1;        // Enable interrupts

while(1);           // Wait for interrupt

```

Figure 5: Fall Detector program listing

-105dBm. Both transmitter and receiver are 100% pin-compatible with the lower-power module TDL2A. The pin-compatible TDH2 module can be used in applications where two-way data communication is required.

Program Listing

The programs are written using the mikroC Pro for PIC programming language. Figures 5 and 6 show the program listings for the Fall

```

void main()
{
    unsigned char buff[30];
    TRISG = 0;
    // Configure PORTG as output
    UART1_Init(9600); // Initialize UART
    Sound_Init(&PORTG, 3); // Initialize sound library

    while(1) // Do Forever
    {
        if(UART1_Data_Ready() == 1) // If data received
        {
            UART1_Read_Text(buff, ":", 255); // Wait for data
            if(buff[0]=='F' && buff[1]=='A' && buff[2]=='L' && buff[3]=='L')
            {
                while(1) Sound_Play(1000,200); // Sound the alarm
            }
        }
    }
}

```

Figure 6: Fall Processor program listing

Detector and Fall Processor stations respectively. In this simple example, the text "FALL" followed by the identification of the person (name) is sent to the Fall Processor. ●

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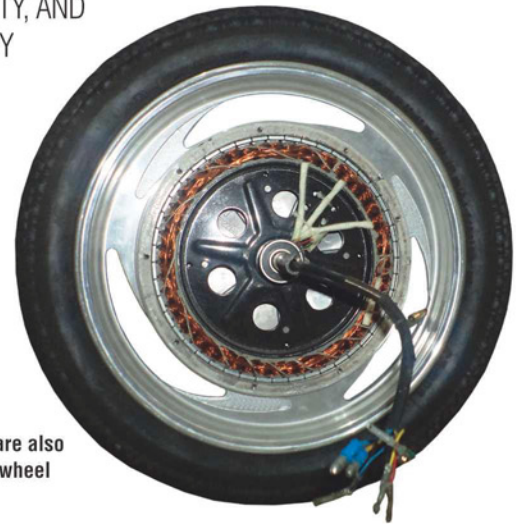
REAL-TIME FAULT DIAGNOSIS OF HUB MOTORS USING A FUZZY-LOGIC CONTROLLER

BY MEHMET ŞİMŞİR AND RAIF BAYIR FROM KARABÜK UNIVERSITY, AND YILMAZ UYAROĞLU FROM SAKARYA UNIVERSITY, BOTH IN TURKEY

Electrical motors are an intrinsic part of vehicles. As such, motor condition monitoring and fault diagnosis are two very important aspects in maintaining their long operational life and low cost. Faults not detected and tackled immediately will cause performance degradation and potentially major system failures.

Fuzzy-logic systems are commonly used in fault diagnosis and fault-tolerant systems. In this article we present a highly-reliable condition monitoring and fault diagnosis system of hub motors based on fuzzy logic.

Hub motors, or in-wheel motors, are a type of BLDC (brushless direct current) motor, commonly found in small, low-power electrical vehicles. Although they look like wheels, these motors have an electric motor inside, making the whole system highly efficient compared to conventional DC motors. This is because hub motors don't need any drivelines such as gears or differential systems with their mechanical losses; hub motors drive vehicles directly from their electrical input.



Hub motors are also known as in-wheel motors

Test-Set

In our project to create a highly-reliable fault diagnosis system, we used a special test-set (see Figure 1) to acquire source-current, speed and torque data for a 250W, 48V, 3-phase hub motor, based on which we used Matlab to design a fuzzy-logic controller.

The test-set consisted of a torque sensor, an alternator for loading the hub motor, a DC generator for measuring the speed of the hub motor in RPM, a current probe for measuring the source current and a belt-and-pulley system. We used a belt-and-pulley system because the hub motor has a less frequently-used, unique style with inverted stator and rotor placements compared to conventional motors. The stator is the inner part of the motor, wrapped around the shaft, and the rotor, mounted inside the wheel, surrounds the stator.

Data was acquired with an Advantech 1716L data acquisition card via the terminal board, and a Matlab Simulink model was designed for filtering and storing the data; all measurements were taken during half-load operation.

Fault-diagnostic studies are based on detecting differences between defined conditions, such as normal operation and possible faults in the hub motor. After obtaining data for the normal condition, all faults can be pinpointed using fault data from the hub motor. Figure 2 shows data for the hub motor in normal condition, and Figure 3 shows the data for an open circuit.

Figure 3 shows that the source current, speed and torque values have decreased by comparison with the normal-condition data in Figure 2.

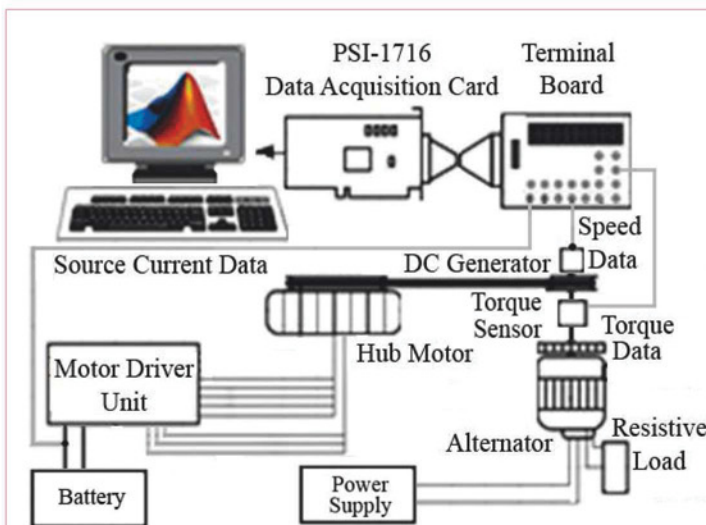


Figure 1: Test-set designed for real-time data acquisition and fault diagnosis of hub motors

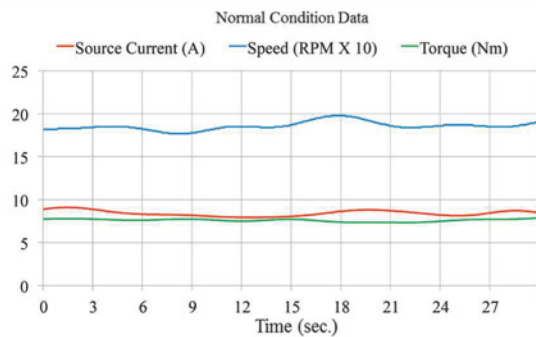


Figure 2: Normal-condition data curves for the hub motor

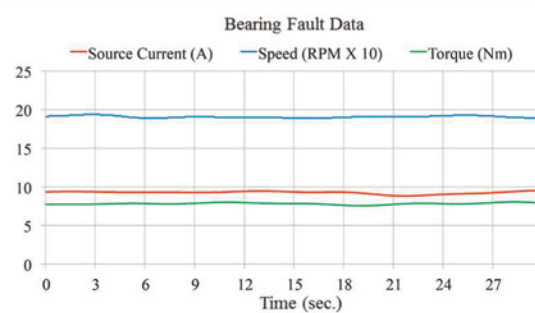


Figure 4: Bearing fault data curves for the hub motor

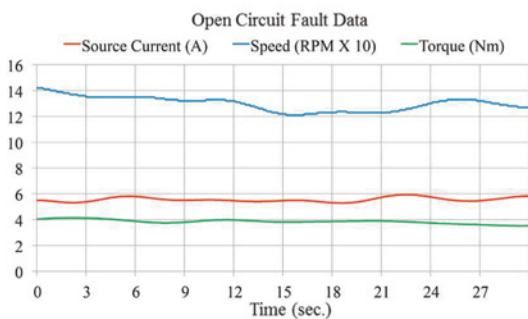


Figure 3: Open-circuit fault data curves for the hub motor

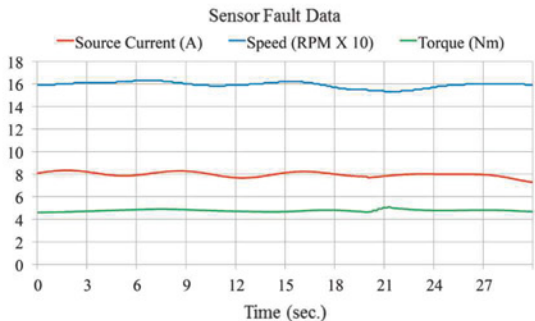


Figure 5: Sensor fault data for the hub motor

Figure 4 shows data for a bearing fault in the hub motor, which caused a small increase in source current because a damaged bearing makes the motor consume more power.

A sensor fault in the hub motor causes the speed, source current and torque to decrease in relation to the normal condition; see Figure 5.

Figures 6 and 7 show the curves for one- and two-coil short-circuit conditions. The one-coil short-circuit fault is characterized by lower speed and torque but higher source current, whereas the two-coil short circuit causes lower speed, higher source current and very low torque. Analyzing this information helps distinguish between conditions and identify more quickly the fault in the hub motor.

Figure 8 shows the fuzzy-logic controller's current, torque and speed as inputs and the state of the motor as output.

The controller's output consist of six parts: normal condition, open circuit, short circuit for one coil, short-circuit between two coils, sensor fault and bearing fault. The input functions and output data were connected with 66 rules, written specifically for the fuzzy-logic controller, and they contain all possible conditions for the hub motor.

After designing the fuzzy-logic controller, a real-time fault diagnosis system was created with Matlab Simulink; see Figure 9.

The left side of the controller also handles the data acquisition and data storage, whereas its right side classifies the results, per the fuzzy-logic controller's decisions. The level and amplitude of

the input voltage were chosen and applied to the hub motor by the analog output port of the data acquisition card.

Results

We tested the system with previously acquired data of some 5000 input sets. We cross-referenced the outputs with 5000 known outputs, of which 1000 sets were for normal conditions, and 800 each for open circuit fault, one-coil short circuit, two-coil short circuit, bearing fault and sensor fault. In total, 4956 data outputs were correctly paired with the expected values for all 5000 data-sets, giving us a 99.12% success rate for diagnosing a fault in hub motors.

Then, we connected the hub motor to the fault diagnosis system in real time and tested it with homogeneously separated numbers for all faults and in normal conditions; 98 results were 'stable correct', one was 'false' and one 'unstable correct' (sometimes correct and sometimes false), which we classified as a false result.

Both false results were linked to a bearing fault, diagnosed incorrectly as a normal condition.

So, our fault diagnosis system had a success rate of 98% in real time, showing it to be a reliable system.

Applications

The use of hub motors can vastly be increased by developing an electronic differential to distribute rotational speed according to

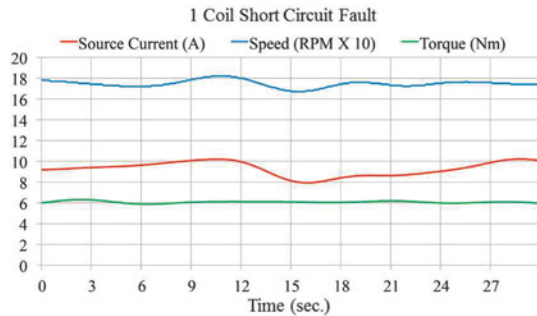


Figure 6: One-coil short circuit fault data

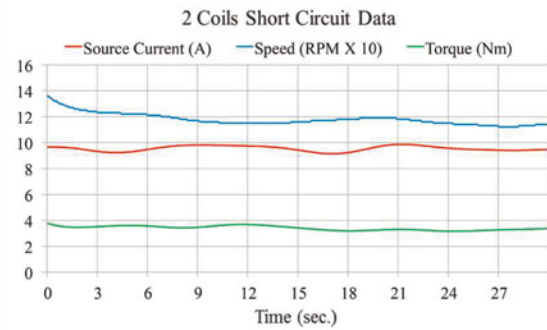


Figure 7: Two-coil short circuit fault data

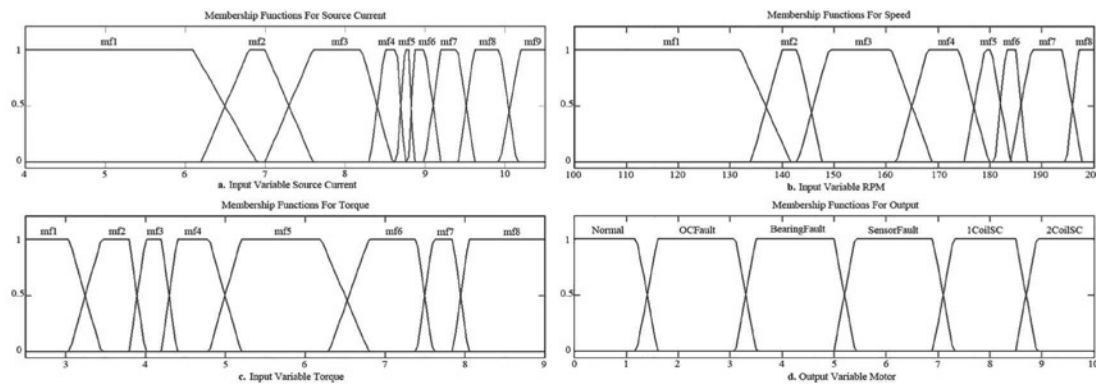


Figure 8: Controller functions for: (a) source current; (b) speed; (c) torque; (d) output variables

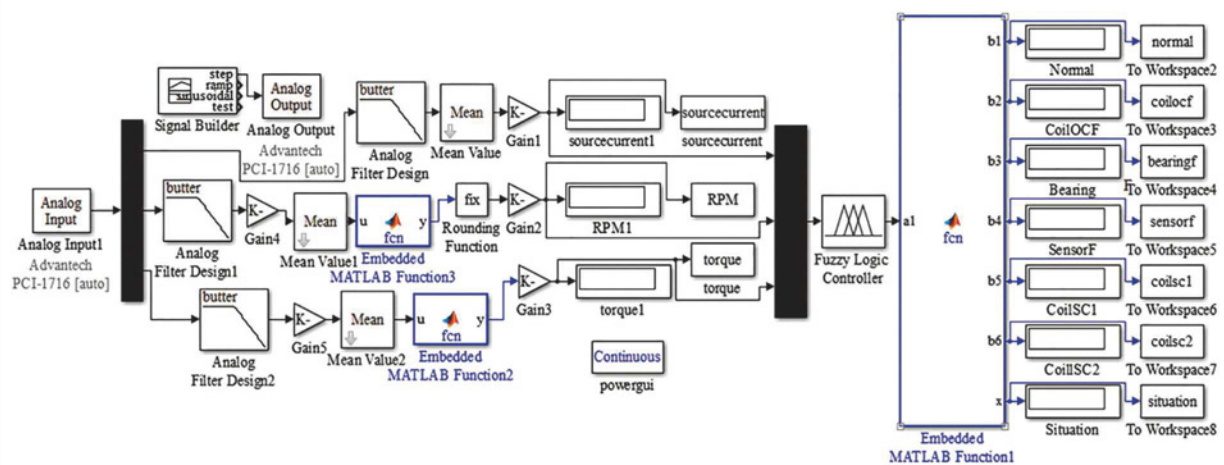


Figure 9: The fuzzy-logic controller is embedded in the real-time fault diagnosis and condition monitoring system

the position of the steering wheel for front-wheel-, rear-wheel- and four-wheel-drives without causing energy losses. On the other hand, adding a transmission system to the hub motor will enable it to achieve a wider speed range.

With minor modifications, our system can be easily applied to larger vehicles with hub motors, by embedding the fuzzy-logic controller into a microcontroller, and by adding a user panel to

the dashboard that indicates the hub motor(s) conditions.

Other applications may include trip computers for electrical vehicles driven by hub motors, where by taking into account the source current, the driver can be aware of the remaining travel distance left within the battery, driving characteristics, performance, battery charging level, faults and conditions of the hub motor, power consumption and overall efficiency of the system. ●

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HOW CONVOLUTIONAL NEURAL NETWORKS CAN ENHANCE IMAGE RECOGNITION

BY **SAMER HIJAZI, RISHI KUMAR AND CHRIS ROWEN** FROM CADENCE DESIGN SYSTEMS

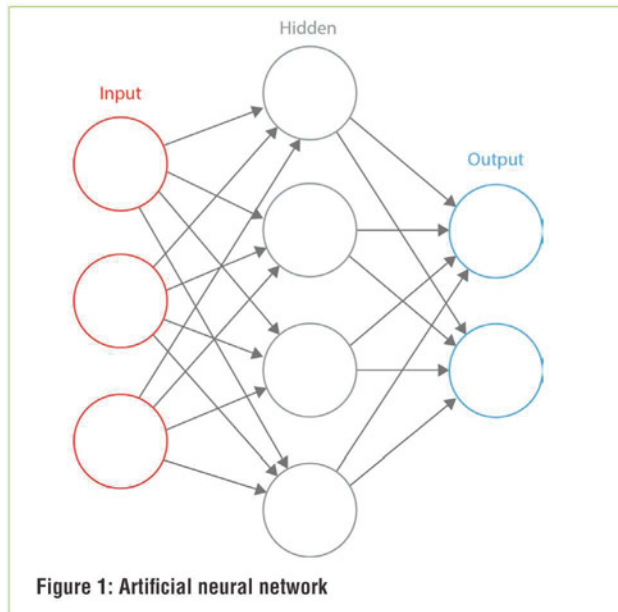


Figure 1: Artificial neural network

Convolutional neural networks (CNNs) – a layer-based system of interconnected artificial neurons that exchange messages between each other – are commonly used in pattern recognition applications, including image recognition. In this article, we will provide an understanding of how CNNs work, discuss algorithms and implementation software that can trade between computational-burden and energy-consumption challenges for a modest degradation in recognition rates, examine the challenges of using CNNs in embedded systems and present a digital signal processor (DSP) solution, ideal for a variety of CNN applications.

Layers Of Pattern Recognition

In a neural network, there are multiple layers of feature-detecting neurons that respond to different combinations of inputs from the previous layers. The layers, shown in Figure 1, are built up such that the first layer detects a set of primitive patterns in the input, the second layer detects patterns of patterns and the third layer detects patterns of those patterns, and so on. CNNs typically use anywhere from 5-25 distinct layers of pattern recognition.

The connections in a neural network have numeric weights that get tuned during the training process, so the network

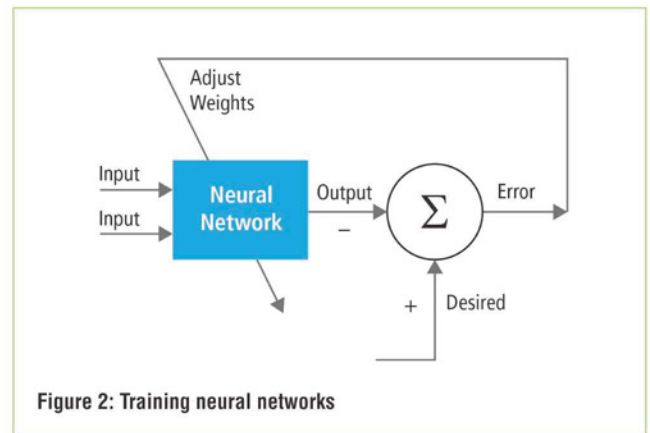


Figure 2: Training neural networks

responds correctly when it is presented with an image or a pattern. As part of the training, a labelled dataset of inputs in a wide array of representative input patterns is tagged with the intended output response. General-purpose methods iteratively determine the weights for intermediate and final feature neurons. See Figure 2 for a depiction of the training process at a block level.

Neural networks are inspired by biological neural systems – a neuron is a basic computational unit of the brain, connected with others via synapses; Figure 3 shows how a biological neuron compares with a basic mathematical model.

In the neural network computational model, the signals that travel along the axons (e.g. x_o) interact multiplicatively (e.g. $w_o x_o$) with the dendrites of the other neuron based on the synaptic strength at that synapse (e.g. w_o). Synaptic weights, which can be trained, control the influence of one neuron on another. The dendrites carry the signal to the cell body, where they all are summed. If the final sum is higher than a specified threshold, the neuron fires to send a spike along its axon.

Based on the rate code interpretation, the firing rate of the neuron is modelled with an activation function f that represents the frequency of the spikes along the axon. Sigmoid is a common choice of activation function. So, to summarize, each neuron calculates the dot product of inputs and weights, adds the bias and applies non-linearity as a trigger function, for example, following a sigmoid response function.

A CNN is a special case of the neural network described here, consisting of one or more convolutional layers, often with a

subsampling layer. These layers are followed by one or more fully connected layers as in a standard neural network.

Improving Performance

Figure 4 shows a typical CNN for recognizing traffic signs. As it can be seen from the figure, each feature of a layer receives inputs from a set of features located in a small neighbourhood in the previous layer, called a local receptive field. Local receptive fields enable features to extract elementary visual features, such as oriented edges, end points and corners. These visual features are then combined by the higher layers.

Traditionally, in pattern/image recognition, a hand-designed feature extractor gathers relevant information from the input and eliminates irrelevant variabilities. The extractor is followed by a trainable classifier, a standard neural network that classifies feature vectors into classes. In a CNN, convolution layers (which are not hand-designed) act as feature extractors. Convolution filter kernel weights are determined during the training process.

Convolutional layers can extract the local features because they restrict the receptive fields of the hidden layers to be local. With their enhanced network structures, compared to those of traditional pattern-recognition models, CNNs can help minimize memory requirements and computation complexity, as well as provide better performance for applications where the input has local correlation, such as image and speech.

For pattern- and image-recognition applications, CNNs have demonstrated the best possible correct detection rates (CDRs) compared to other detection algorithms. Here are some examples of what CNNs have achieved:

- A CDR of 99.77% using the MNIST database of handwritten digits;
- A CDR of 97.47% with the NORB dataset of 3D objects;
- A CDR of 97.6% on ~ 5600 images of more than 10 objects.

CNN Common Layer Types

Fairly complex architectures can be built for various classification problems by stacking multiple and different layers in a CNN. Some common layer types include convolution layers, pooling/subsampling layers, non-linear layers and fully connected layers.

A convolution operation extracts different features of the input. The first convolution layer extracts low-level features like edges, lines and corners; higher level layers extract higher level features.

The pooling/subsampling layer reduces the resolution of the features to make them robust against noise and distortion; max pooling and average pooling can be applied. In both cases, the input is divided into non-overlapping two-dimensional spaces. For example, in Figure 4, layer 2 is the pooling layer. Each input feature is 28×28 , divided into 14×14 regions of size 2×2 . For average pooling, calculate the average of the four values in the region. For max pooling, select the maximum value of the four values.

CNNs are suited to deal with distortions; from changes in shape due to the camera lens, to different lighting conditions, different poses, the presence of partial occlusions, and horizontal and vertical shifts

CNNs rely on a non-linear “trigger” function to signal distinct identification of likely features on each hidden layer. There are a variety of specific functions that a CNN can use to efficiently implement non-linear triggering. For instance, rectified linear units (ReLUs) implement

the function $y = \max(x, 0)$ so that the input and output sizes of this layer are the same. Using ReLUs allows the network to train many times faster than other non-linear functions.

The final layers of a CNN are often the fully-connected layers, which mathematically sum a weighting of the previous layer of features. They indicate the precise mix of “ingredients” that form a specific target output result.

In a fully-connected layer, all elements of all the features of a previous layer are used to calculate each element of each output feature.

CNN Advantages To Image Recognition

Compared to more traditional pattern-detection methods, CNNs offer a number of advantages. For one, CNNs are suited to deal with distortions; from changes in shape due to the camera lens, to different lighting conditions, different poses, the presence of partial occlusions, and horizontal and vertical shifts.

CNNs are however shift-invariant, since the same weight configuration is used across space. CNNs also have fewer memory requirements – in the convolutional layer, the same coefficients

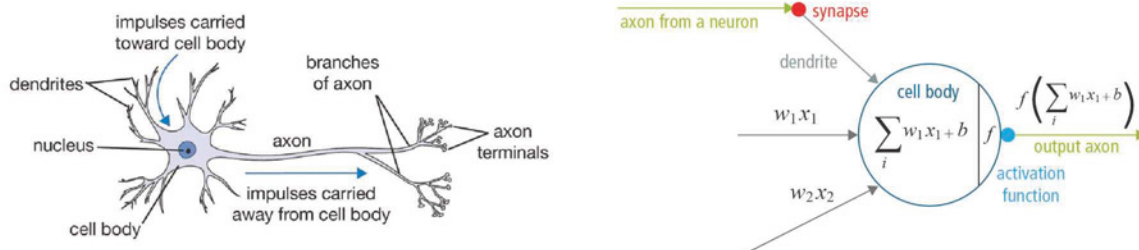
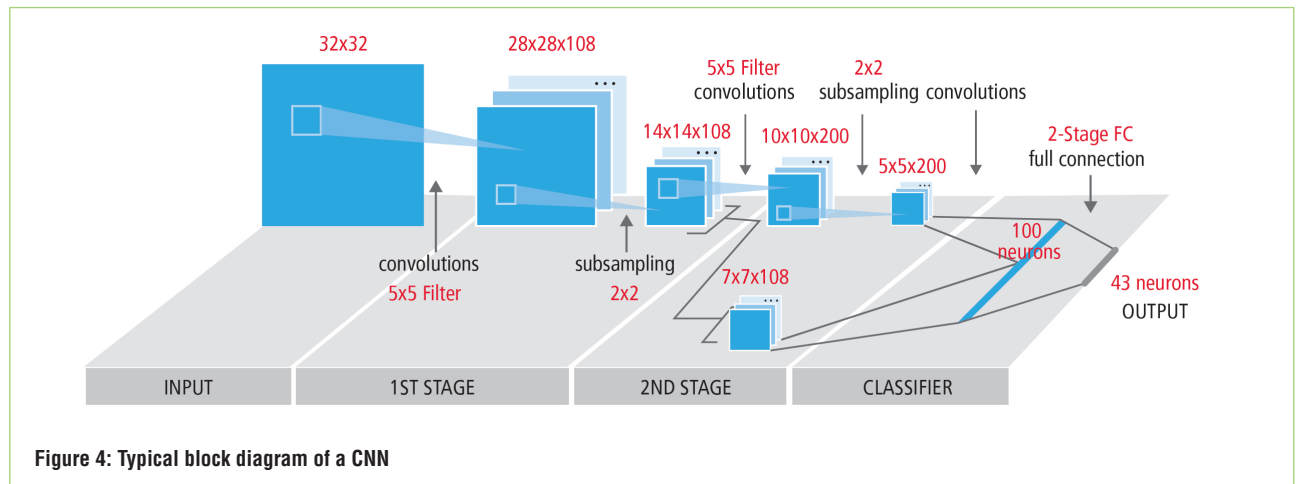


Figure 3: A biological neuron (left) and its mathematical model (right)



are used across different locations in the space, significantly reducing the memory requirement.

The training process is easier with CNNs. Since the number of parameters is reduced substantially compared to traditional neural networks, the training time is proportionately reduced and less noise is added in the training process.

CNNs In Embedded Systems

A vision subsystem needs a substantial amount of image processing in addition to a CNN. Running CNNs on a power-constrained embedded system that supports image processing calls for the following:

- **High computational performance:** there should be support for typically billions of MACs per second;
- **Larger load/store bandwidth:** with a fully connected layer used for classification; for example, each coefficient is used in multiplication only once. Therefore, the load/store bandwidth

requirement is greater than the number of MACs performed by the processor.

- **Low dynamic power:** to meet this requirement, fixed-point implementation is needed, which results in the need to use the minimum possible finite number of bits to meet performance requirements.
- **Flexibility:** this allows an easy upgrade of the existing design to a better-performing one.

In an embedded system, computational resources are always a constraint. As a result, if an application can accommodate small performance degradation, then it's helpful to have an algorithm that helps minimize computational complexity for the tradeoff.

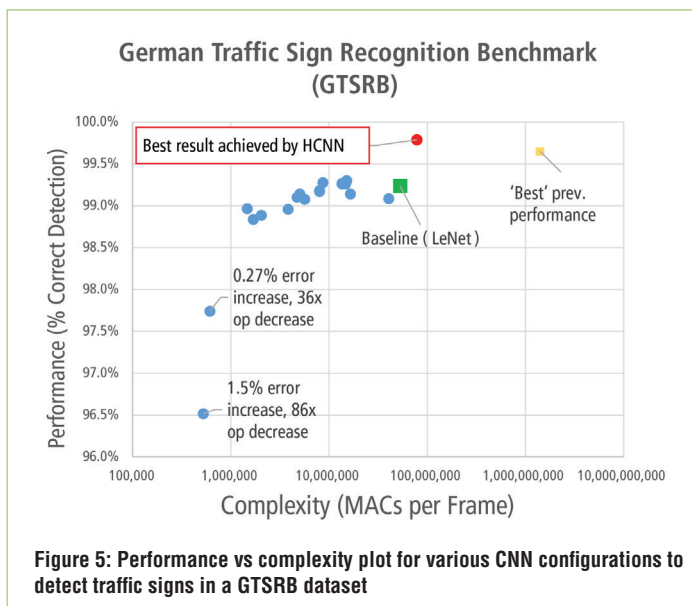
Example: Traffic Sign Recognition

As an example of a CNN in action, consider the German Traffic Sign Recognition Benchmark (GTSRB), a multi-class, single-image classification challenge, held at the International Joint Conference on Neural Networks (IJCNN) 2011. There were nearly 52,000 images of German road signs in 43 different classes, with the images ranging from 15 x 15 to 222 x 193.

Based on the GTSRB dataset, Cadence developed various algorithms in MATLAB for traffic sign recognition. Using a proprietary hierarchical CNN approach, Cadence achieved a better correct detection rate than a previously established baseline; see Figure 5 for the results.

The company's researchers divided 43 traffic signs into five families, and implemented six smaller CNNs. The first CNN decided which family the received traffic sign belonged to. Once the family of the sign was determined, one of the remaining five CNNs corresponding to the detected family was run to determine the traffic sign within that family.

The researchers also reduced the complexity of the CNN, without any performance degradation, using a proprietary algorithm based on eigenvalue decomposition that reduces a trained CNN to its canonical dimension. This proprietary algorithm helps control the complexity of CNNs in embedded applications.



NEW VISION-PROCESSING DSP

Cadence offers a new high-performance, low-power DSP that was designed for image and computer vision processing.

The Tensilica Vision P5 DSP has a VLIW architecture with SIMD support, five issue slots in an instruction word of up to 96 bits, and the ability to load up to 1024-bit words from memory every cycle.

The DSP's internal registers and operation units range from 512-1536 bits, with data represented as 16, 32, or 64 slices of 8b, 16b, 24b, 32b, or 48b pixel data.

The DSP features the following characteristics, making it ideal for implementing CNNs in embedded systems:

- **High computational performance:** the DSP offers instruction support for all stages of CNNs, as well as advanced support for implementing image signal processing. For convolution operations, it has a very rich instruction set, supporting multiply/multiply-accumulate operations of 8b x 8b, 8b x 16b, and 16b x 16b for signed/unsigned data. It can perform up to 64 8b x 16b and 8b x 8b multiply/multiply-accumulate operations in one cycle and 32 16b x 16b multiply/multiply-accumulate operations in one cycle. For max pooling and ReLU functionality the DSP has instructions to do 64 8-bit comparisons in one cycle. For implementing non-linear functions with finite ranges like tanh and signum, it has instructions to implement a lookup table for 64 7-bit values in one cycle. In most of the cases, instructions for comparison and lookup table are scheduled in parallel with multiply/multiply-accumulate instructions, without requiring any extra cycles.
- **Larger load/store bandwidth:** the DSP performs up to two 512-bit load/store operations per cycle.

- **Low dynamic power requirement:** as a fixed-point machine, the DSP can flexibly handle a variety of data types, providing full performance and energy advantage for mixed 16b and 8b computation at a minimal loss of accuracy.
- **Flexibility:** the programmability of the DSP means that a system can be upgraded to a new version via firmware.
- **Optional vector floating-point unit.**

The Tensilica Vision P5 DSP comes with a complete set of software tools, including a high-performance C/C++ compiler with automatic vectorization and scheduling to support the SIMD and VLIW architecture without having to write assembly language. The toolset also includes the linker, assembler, debugger, profiler and graphical visualization tools.

With its comprehensive instruction set simulator (ISS), simulation and performance evaluation can be achieved quickly. When working with large systems or lengthy test vectors, the fast, functional TurboXim simulator option reaches speeds 40 to 80x faster than ISS for efficient software development and functional verification.

Cadence implemented a single-layer architecture CNN on the DSP for the traffic sign recognition example discussed in the article. It achieved a correct detection rate of 99.4% with 16-bit quantization for data samples and 8-bit quantization for coefficients in all the layers for this architecture.

The CNN has two convolution layers, three fully-connected layers, four ReLU layers, three max pooling layers and one tanh non-linear layer. The average performance is 38.58MACs/cycle for the complete network, including the cycles for all the max pooling, tanh and ReLU layers. For the third layer, the effort yielded a best-case performance of 58.43MACs per cycle, including the cycles for tanh and ReLU functionalities. This DSP running at 600MHz can process more than 850 traffic signs in one second.



HP 34401A Digital
Multimeter 6 1/2 Digit



HP 54600B Oscilloscope Analogue/Digital
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MARCONI 2955B Radio
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HP8566B	Spectrum Analyser 100Hz-22GHz	£1,200
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Marconi 2024	Synthesised Signal Generator 9KHz-2.4GHz	£800
Marconi 2030	Synthesised Signal Generator 10KHz-1.35GHz	£750
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Farnell B30/20	PSU 30V 20A Variable No Meters	£75
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Solartron 1253	Gain Phase Analyser 1mHz-20KHz	£600
Tasakago TM035-2	PSU 0-35V 0-2A 2 Meters	£30
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DESIGNING MICROSTRIP PATCH ANTENNAS USING AN HEURISTIC APPROACH

BY MUHAMMAD ZUBAIR, JAWWAD AHMAD AND SYED SAJJAD HUSSAIN RIZVI
OF IQRA UNIVERSITY IN PAKISTAN

To achieve the desired radiation pattern, communications engineers spend a lot of time tweaking the physical and electrical parameters of antennas – normally a costly, time-consuming and imprecise activity. So, it is obvious that a soft scientific optimization technique is needed to determine antenna parameters precisely, at low cost and with less time and effort.

Over the years, numerous soft computing techniques have emerged in the field of antenna design. These can be broadly classified into three major groups: fuzzy logic (FL), artificial

neural networks (ANN) and evolutionary algorithms (EA); see Figure 1.

The evolutionary algorithms are the most used in optimizing complex electrical problems, including those related to antenna radiation fields. Moreover, EAs themselves encompass a variety of heuristic algorithms using selection, reproduction and mutation phases. The most used EA variants are shown in Figure 2.

From all EAs, the genetic algorithm (GA) and the particle swarm optimization (PSO) algorithm are the most robust and efficient in finding better results; see Figure 3.

The antenna is the most important part in the field of electromagnetics. Its radiation pattern and other electrical characteristics depend primarily on its size and geometry. Modern communications systems are built to occupy less space and weigh less, to enhance mobility and portability, for satellite, radar, spacecraft, rocket, missile, wireless and portable applications. The microstrip patch antenna meets these requirements, so it is widely used. In addition, it is simple to manufacture, robust, easily placed on different surfaces, versatile in shape, and with a range of resonant

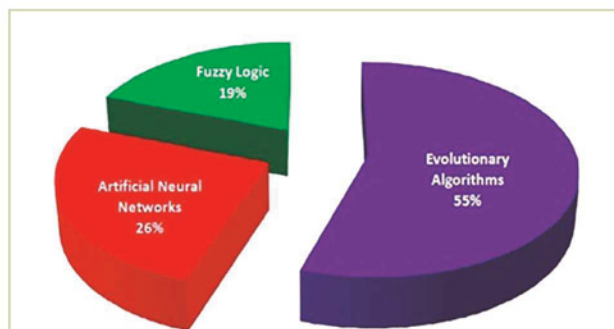


Figure 1: Soft computing approaches applied to complex electrical problems over the past decade

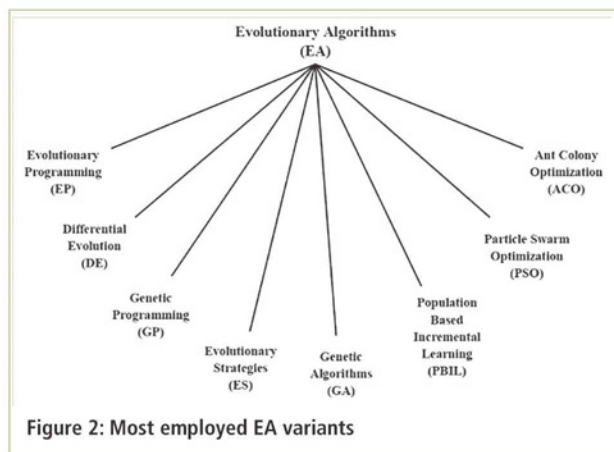


Figure 2: Most employed EA variants

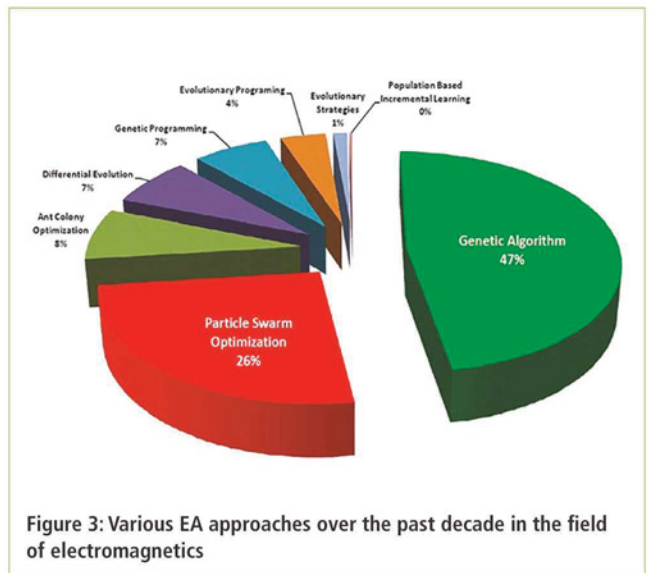


Figure 3: Various EA approaches over the past decade in the field of electromagnetics

frequencies, polarization patterns and impedances. Because of all these benefits, research over the last decade has focused quite heavily on the design of microstrip patch antennas; see Figure 4.

Genetic Algorithm

Genetic algorithm (GA) is one of the most popular types of heuristic algorithms. It is based on natural evolution processes such as crossover, inheritance and mutation.

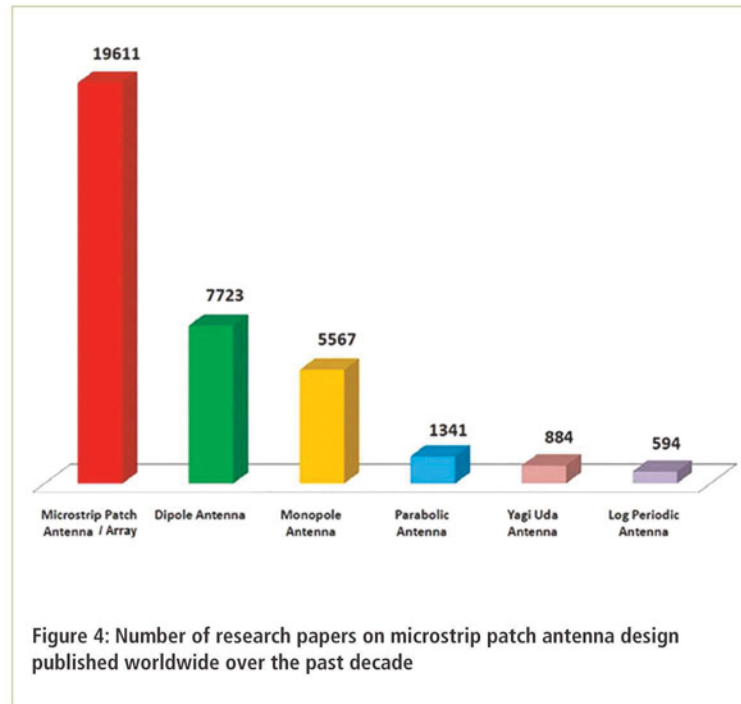
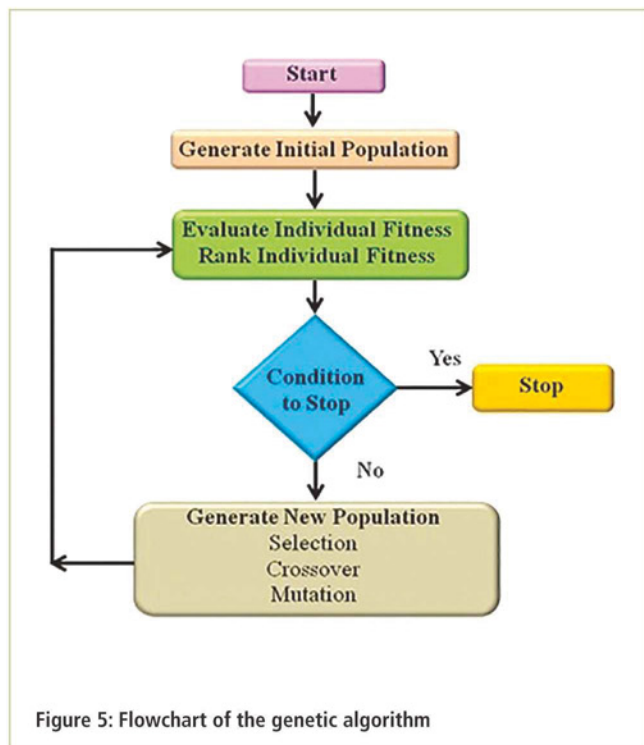
Particle swarm optimization is another important heuristic algorithm, inspired by groups of animals, such as bird flocks or cattle herds

Strings of population (chromosomes) start the evolutionary process, and offer optimized solutions to a problem. With each new iteration, these chromosomes increasingly go toward more optimized results.

The optimized solutions are represented in a

binary pattern; however, any other pattern can emerge. In each generation, the fitness of all individual chromosomes is examined, and those with high fitness values are selected for the next iteration. But before then, these selected chromosomes are also mutated and crossed over to achieve the highest fitness values.

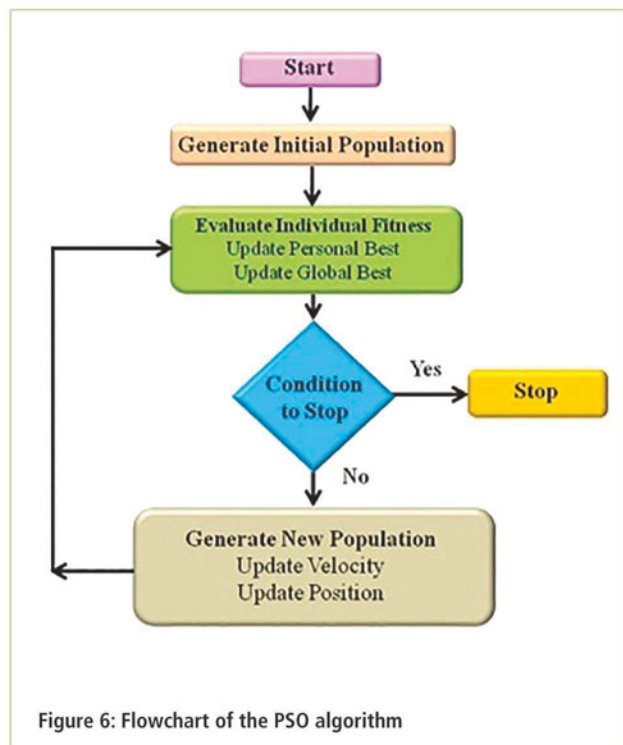
Running the algorithm depends on a predefined number of iterations or a threshold fitness value. A typical flow chart of the algorithm is shown in Figure 5.

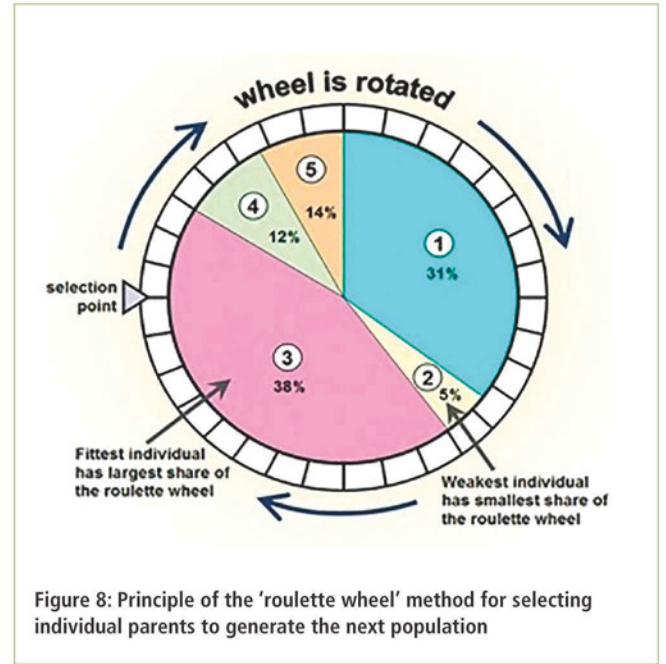
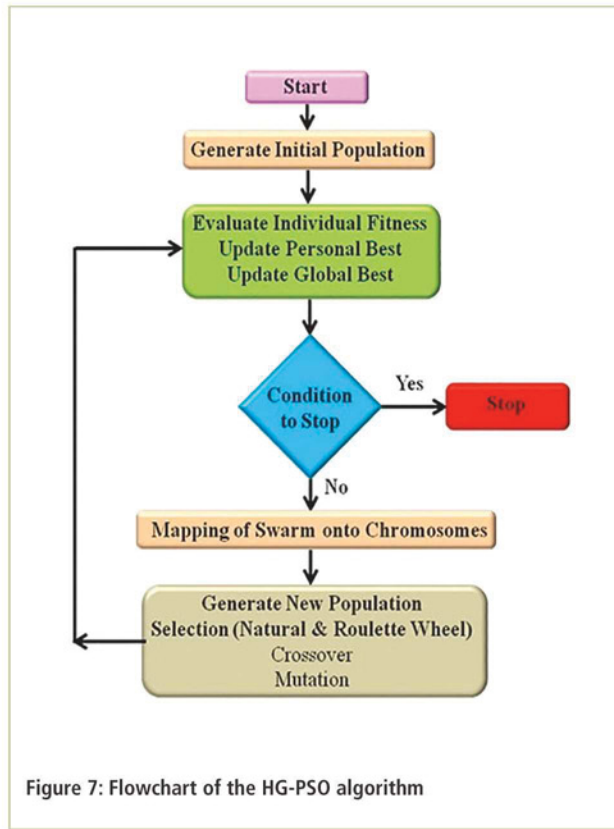


Particle Swarm Optimization

Particle swarm optimization (PSO) is another important heuristic algorithm, inspired by groups of animals, such as bird flocks or cattle herds with an inherent capability to share information between group members.

A typical PSO flowchart is shown in Figure 6.





Set	Bounds			Optimum Estimated Values	Desired Directivity	Estimated Directivity
	ϵ_r	h (mm)	f_r (GHz)			
1.	2 – 4	2 – 4	9 – 11	$\epsilon_r = 2.00034000$ $h = 3.99413277$ $f_r = 10.9983511$	5.25	5.2534559
2.	4 – 6	2 – 4	9 – 11	$\epsilon_r = 4.01876136$ $h = 3.99790123$ $f_r = 10.9988012$	4.25	4.2532111
3.	2 – 4	4 – 6	9 – 11	$\epsilon_r = 2.00009156$ $h = 5.99713238$ $f_r = 10.9894345$	5.25	5.2511001
4.	4 – 6	4 – 6	9 – 11	$\epsilon_r = 4.00036612$ $h = 5.99891098$ $f_r = 10.9994511$	4.25	4.2543211
5.	2 – 4	2 – 4	7 – 9	$\epsilon_r = 4.00009109$ $h = 5.99774786$ $f_r = 7.99646341$	5.00	5.0902311
6.	4 – 6	2 – 4	7 – 9	$\epsilon_r = 4.00018312$ $h = 3.99911345$ $f_r = 8.99767786$	4.50	4.4893312
7.	2 – 4	4 – 6	7 – 9	$\epsilon_r = 2.02341123$ $h = 5.99587342$ $f_r = 8.99755868$	5.25	5.2543209
8.	4 – 6	4 – 6	7 – 9	$\epsilon_r = 4.00009151$ $h = 5.99890034$ $f_r = 8.99411134$	4.00	4.0991239
9.	8 – 10	2 – 6	7 – 9	$\epsilon_r = 8.00003052$ $h = 5.98287501$ $f_r = 8.99997123$	3.75	3.7312233
10.	5 – 10	2 – 8	7 – 11	$\epsilon_r = 5.00015263$ $h = 7.99267583$ $f_r = 10.9840088$	4.00	3.9823982

Table 1: The HG-PSO natural selection approach

Hybrid Genetic PSO

The hybrid genetic particle swarm optimization (HG-PSO) algorithm combines all the features of the GA and PSO algorithms; see its typical flowchart in Figure 7.

In our study we adopted the HG-PSO to estimate the optimum values of certain geometrical and electrical parameters of a microstrip patch antenna, using two selection criteria to generate new populations:

- Natural selection, where higher fitness (or lower cost) individuals are selected statistically to be parents for the next iteration. However, with this approach, the 'best gene' can be lost during the truncation process.
- Roulette wheel selection, a stochastic selection process. The selection chance is proportional to higher fitness (or lower cost). The selection of individuals is similar to a spinning roulette wheel. As shown in Figure 8, the individuals with highest fitness (or lowest cost) have a better chance of being selected.

Microstrip Patch Antennas

The basic design structure of a microstrip patch antenna comprises a very fine, thin metallic patch, fabricated on an insulating surface (substrate). The opposite side of the substrate connects to a ground plane.

The patch can be made in different dimensions and shapes, such as square, rectangular, hexagonal, triangular, circular, elliptical and so on.

The free-space wavelength (λ_0) is the deciding factor in designing the overall size and other dimension of the patch antenna:

Length of the metallic patch L ,
 rectangular: $0.3333\lambda_0 < L < 0.5\lambda_0$
 Thickness of the patch t : $t \ll \lambda_0$
 Thickness of substrate h : $0.003\lambda_0 \leq h \leq 0.05\lambda_0$
 Dielectric constant of substrate ϵ_r : $2.2 \leq \epsilon_r \leq 12$

The most widely used geometric configuration is the rectangular patch, shown in Figure 9, with width W , length L and thickness t .

The patch is mounted on a substrate of dielectric constant ϵ_r . Copper or gold is normally used for the metallic patch using photoetching technique.

Directivity Estimation

The directivity of an antenna is determined using a relative comparison between the antenna's radiation intensity and that of an isotropic radiator:

$$D = \frac{U}{U_0} = \frac{4\pi U}{P_{\text{rad}}}$$

where D is directivity (unitless), U is radiation intensity

(Watts/steradian), U_0 is radiation intensity of an isotropic element (W/steradian) and P_{rad} is the average value of antenna radiated power (W). It is important to note that radiation intensity, radiated power and, consequently, directivity of the patch antenna depend on the substrate's height h , dielectric constant ϵ_r and resonant frequency f_r . So, along with mathematical calculations, there are many heuristic algorithms available to estimate these parameters.

However, estimating antenna directivity using mathematics is laborious. On the other hand, our HG-PSO algorithm makes it much easier to find the optimum values for the substrate's parameters to achieve the desired directivity. The two selection criteria we used for generating a new population are shown in Tables 1 and 2.

The estimated values for the directivities through both selection processes are shown in Figure 10. It can be seen that although the roulette wheel selection approach appears better than the natural selection method in most cases, for the HG-PSO algorithm (applied to antenna design), the natural selection one is most effective and appropriate compared with the roulette wheel selection. ●

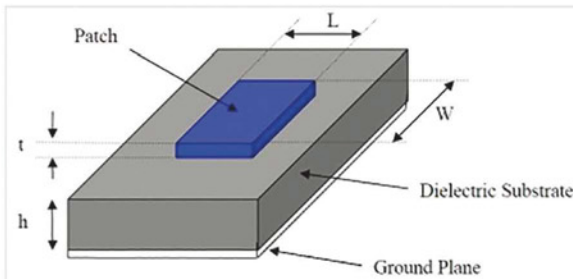


Figure 9: Rectangular microstrip patch antenna

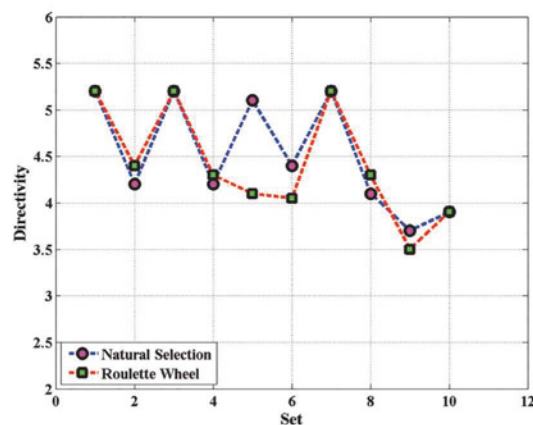


Figure 10: Estimated directivity using Natural and Roulette Wheel Selections

Set	Bounds			Optimum Estimated Values	Desired Directivity	Estimated Directivity
	ϵ_r	h (mm)	f_r (GHz)			
1.	2 – 4	2 – 4	9 – 11	$\epsilon_r = 2.00006103$ $h = 3.99921455$ $f_r = 10.9998734$	5.25	5.2511012
2.	4 – 6	2 – 4	9 – 11	$\epsilon_r = 4.00003210$ $h = 3.99992133$ $f_r = 10.9998788$	4.25	4.4732211
3.	2 – 4	4 – 6	9 – 11	$\epsilon_r = 2.00001234$ $h = 5.99996123$ $f_r = 10.9989931$	5.25	5.2511023
4.	4 – 6	4 – 6	9 – 11	$\epsilon_r = 4.00010111$ $h = 5.99990811$ $f_r = 10.9998168$	4.25	4.2876542
5.	2 – 4	2 – 4	7 – 9	$\epsilon_r = 2.00012392$ $h = 3.99997233$ $f_r = 8.99887085$	5.00	4.1222342
6.	4 – 6	2 – 4	7 – 9	$\epsilon_r = 4.00012201$ $h = 3.99997231$ $f_r = 8.99899292$	4.50	4.0902342
7.	2 – 4	4 – 6	7 – 9	$\epsilon_r = 2.00000012$ $h = 5.99984723$ $f_r = 8.99999911$	5.25	5.2528983
8.	4 – 6	4 – 6	7 – 9	$\epsilon_r = 4.00000011$ $h = 5.99899349$ $f_r = 8.99914551$	4.00	4.3456212
9.	8 – 10	2 – 6	7 – 9	$\epsilon_r = 8.00000002$ $h = 5.99994891$ $f_r = 8.99999889$	3.75	3.5021344
10.	5 – 10	2 – 8	7 – 11	$\epsilon_r = 5.00000163$ $h = 7.99999146$ $f_r = 10.9998988$	4.00	3.9123222

Table 2: The HG-PSO 'roulette wheel' selection approach

NEURAL-NETWORK-BASED CURRENT FORECASTING ON HIGH-VOLTAGE UNDERGROUND CABLES

IN THIS STUDY, **BAHADIR AKBAL** FROM SELCUK UNIVERSITY IN TURKEY EXAMINES THE FORMATION AND REDUCTION OF SHEATH CURRENT IN HIGH-VOLTAGE UNDERGROUND CABLES

The transmission and distribution of power is typically handled by overhead and underground cables. High-voltage cables have an insulation layer, so they are more reliable than overhead lines, making them the preferred method for power distribution in urban environments.

Issues Caused By Sheath Currents

Cross-linked polyethylene (XLPE) is a widely used material for insulating high-voltage underground power cables, and this insulation is further protected by sheath and armour. However, there's sheath current generated in the metal sheathing, which causes faults in the cables and a risk of electroshock. The sheath current also increases cable temperature and reduces its ampacity – the maximum current it can carry before starting to deteriorate. In short, cable performance decreases significantly due to sheath current.

To prevent the effects of sheath current, bonding methods are used where the cable's metallic sheath is grounded. There are several of these methods including single-point, solid and cross bonding (see Figures 1-3), each with its own benefits and drawbacks. For example, single-point bonding is suitable for use on short cables, whereas the other two methods are used for long ones. Sheath voltage in solid bonding is lower than that of cross bonding, but, on the other hand, sheath current of cross bonding is lower than that of solid bonding.

Choosing the best bonding method for reducing sheath current is further helped by using the optimum grounding resistance.

Formation Of Sheath Current

The most important factor in the formation of sheath current is the unbalanced phase current. Unbalanced phase current refers to currents that are out of phase with each other, caused

by unbalanced loads in a three-phase system. In simulation studies, when unbalanced current increases, sheath current increases too.

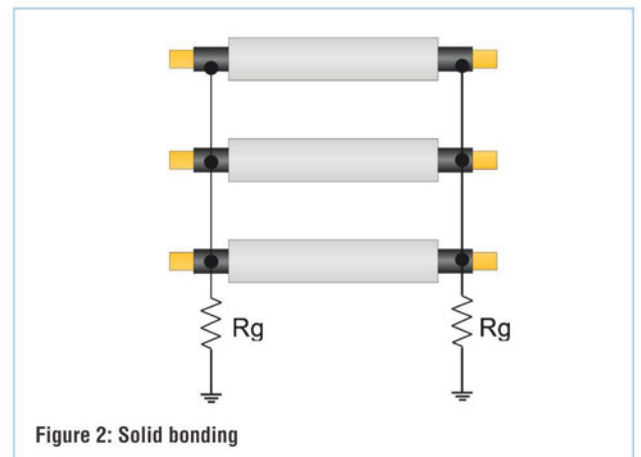
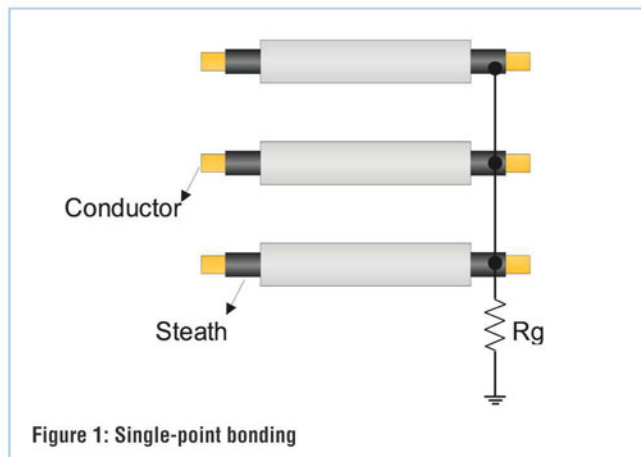
Cable configuration is another factor influencing sheath current. High-voltage cable is

made in both trefoil and flat configurations; see Figure 4.

Eddy and hysteresis losses occur in high-voltage cables, but they tend to be less than that of sheath current, so they may be ignored. Sheath current is also affected by magnetic flux in the cable.

All in all, there are many factors influencing sheath current, some of which are not even measurable. Therefore, determining the value of sheath current is very complex and difficult. Some forecasting methods can help, one of which is the artificial neural network (ANN) method.

Cable performance decreases significantly due to sheath current



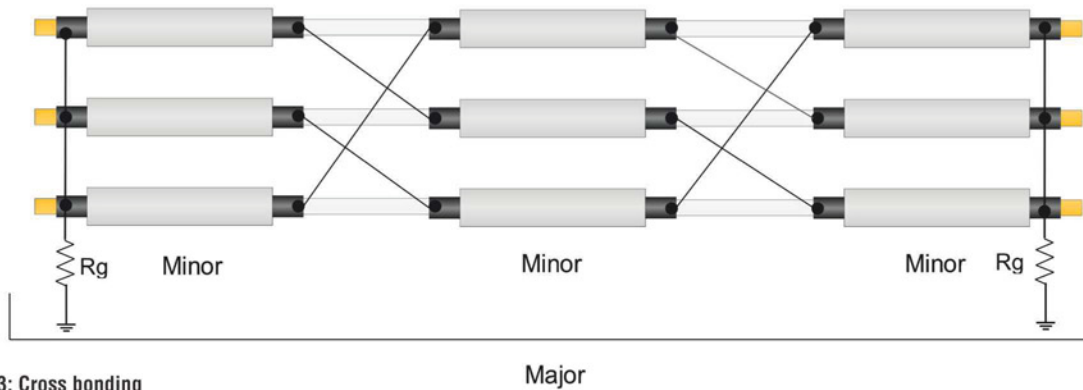


Figure 3: Cross bonding

Artificial Neural Networks

ANN learning is based on mathematical models. An ANN structure typically consists of input, hidden and output layers; see Figure 5. A basic unit of an ANN is a 'neuron'. Neurons typically reside in the hidden layer, and their numbers, as well as the number of hidden layers, can grow depending on the problem type.

Neurons work as a transfer function, see Equation 1; a neuron processing diagram is shown in Figure 6.

$$y_i = f_i \left(\sum_{j=1}^n w_{ij} \times x_j + b_i \right) \quad (1)$$

where x_j is input, w_{ij} is weight, b_i is bias, f_i is transfer function and y_i is output of the neuron. The activation functions can be sorted as step, linear, log-sigmoid, tan-sigmoid, softmax or Gaussian.

The training data inputs are $x_1, x_2, x_3 \dots x_p$, and the output is O_i . In the training process, the actual output and calculated output of the ANN are used to determine the training error by using the mean square error (MSE) method; see Equation 2:

$$E(t) = \frac{1}{n_i} \sum_{i=1}^n (p(i) - o(i))^2 \quad (2)$$

where $E(t)$ is estimation error at the t^{th} iteration, $p(i)$ is the actual value for the i^{th} output and $o(i)$ is the forecast value for the i^{th} output. MSE must be minimized to obtain realistic outputs, so the weights are updated by using Equation 3 in a classic ANN. Weights that make minimum MSE are called the 'best weights'.

$$w_i(t+1) = w_i(t) + \Delta w_i(t) \quad (3)$$

The best weights are obtained at the end of the training process. They will be used to forecast other parameters, such as the forecasting error, which is obtained at the end of the forecasting process. The ANN performance can then be determined by the training and forecasting errors.

If the minimization of MSE does not achieve the desired value, the ANN training data and iteration number are increased, which will also greatly increase the computational

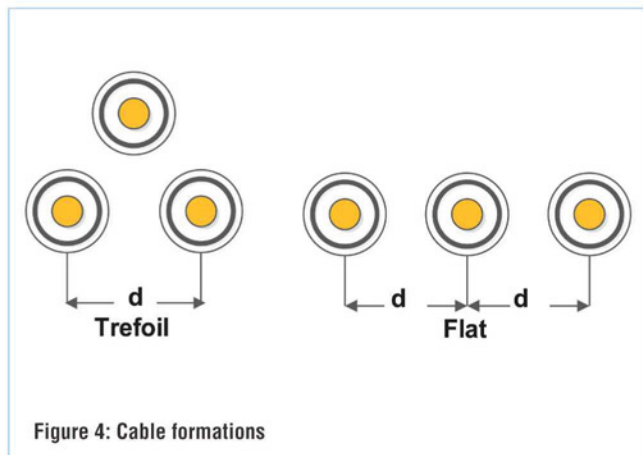


Figure 4: Cable formations

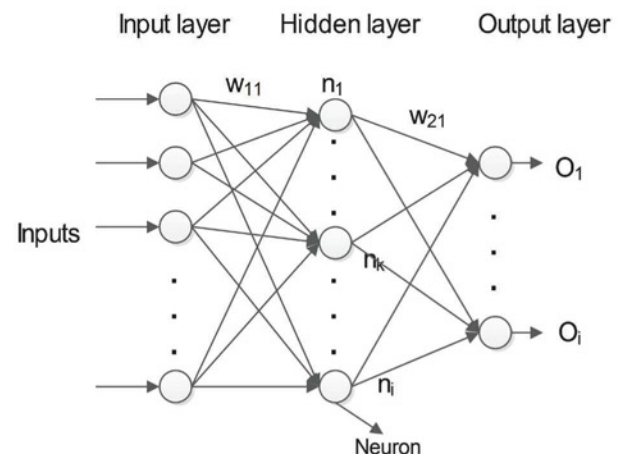
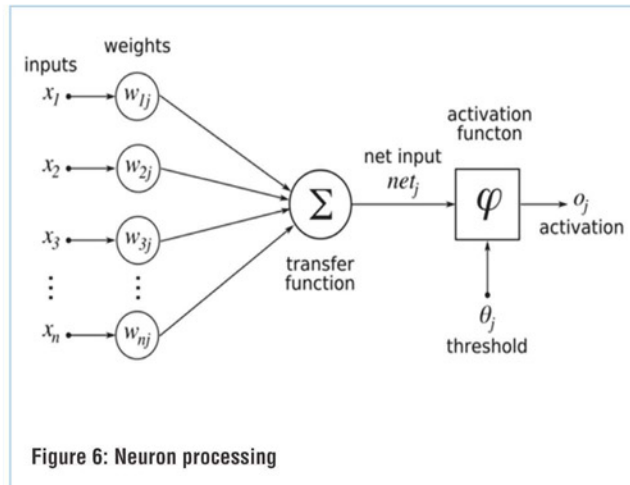


Figure 5: The basic structure of an artificial neural network (ANN)



time. In this case, instead of Equation 3, fuzzy logic or optimization methods are used to update the ANN's weights. In a fuzzy logic algorithm, expert opinion and rule base are applied, and the two have to match; otherwise, realistic results can't be obtained. In fuzzy logic, the membership functions and rule base are used to control a system or object, so the rule base is necessary, created by using 'expert opinion', which comes from the software developer.

Normally, when optimization methods are used to update the weights of an ANN, the rule base is not needed, so using optimization methods is an advantage to train an ANN. There are several such optimization methods, including genetic algorithm (GA), particle swarm optimization (PSO), differential evolution algorithm (DEA), clonal selection algorithm (CSA), hybrid DEA-CSA and artificial bee colony (ABC). When optimization methods are used with the ANN, they are called hybrid ANN methods; see Figure 8.

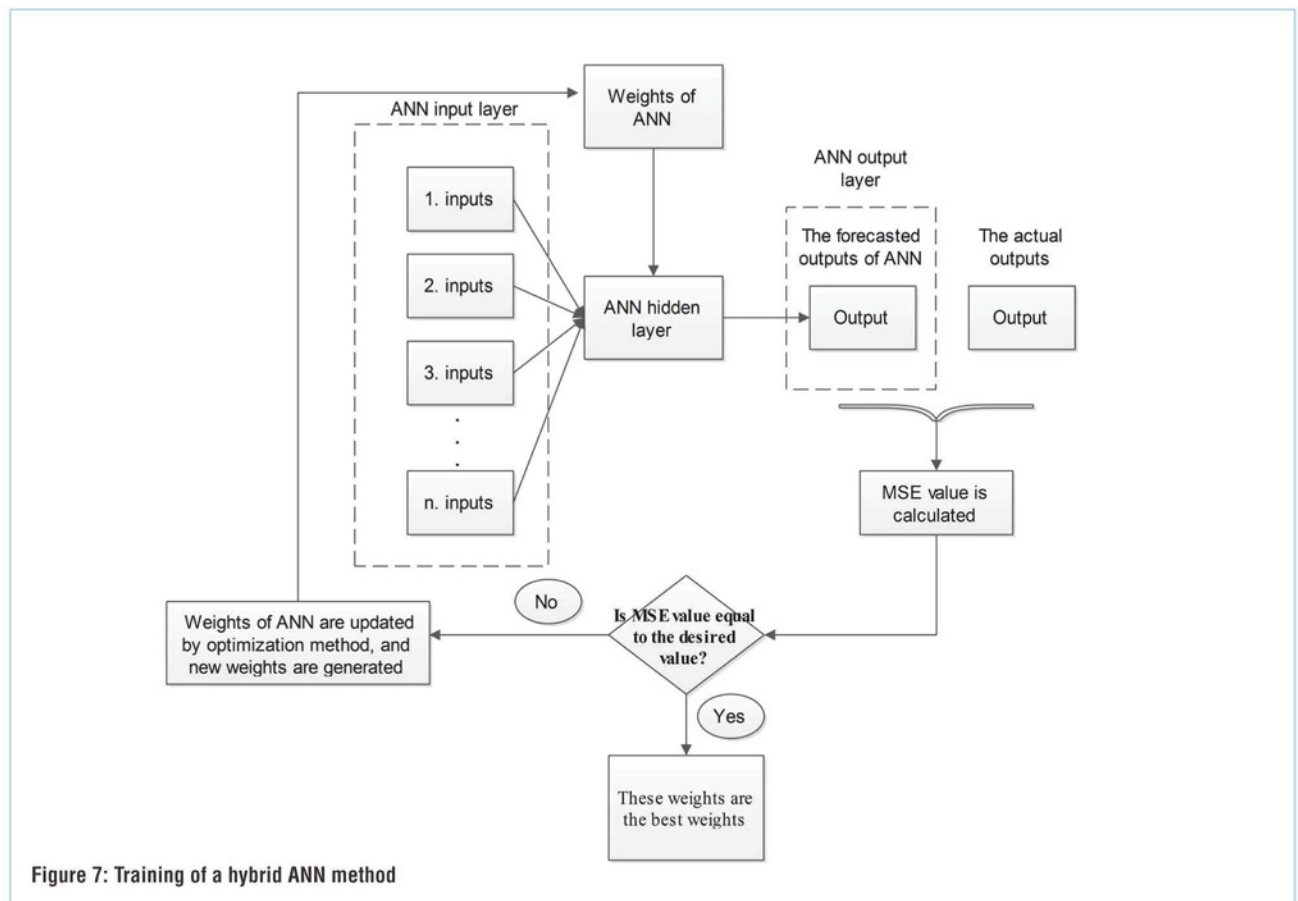
Simulation Of A High-Voltage Cable

In this study, we modelled a 36kV cable in PSCAD/EMTDC; see Figure 5.

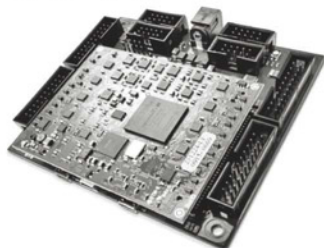
Cable length (L), distance between phases (d), unbalanced phase current (I_{UB}) and grounding resistance (R_g) are all important factors in the formation of sheath current, so training data is generated by using these parameters, and the actual sheath currents are measured in PSCAD/EMTDC.

PSO-ANN, GA-ANN, ABC-ANN, DEA-ANN, CSA-ANN and DEA-CSA-ANN methods are used to forecast this current, their results compared, and the best method that minimizes MSE is selected.

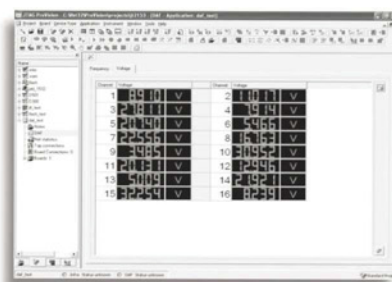
The number of iterations for the training process is 200, and the population size is 100 for each optimization method. There



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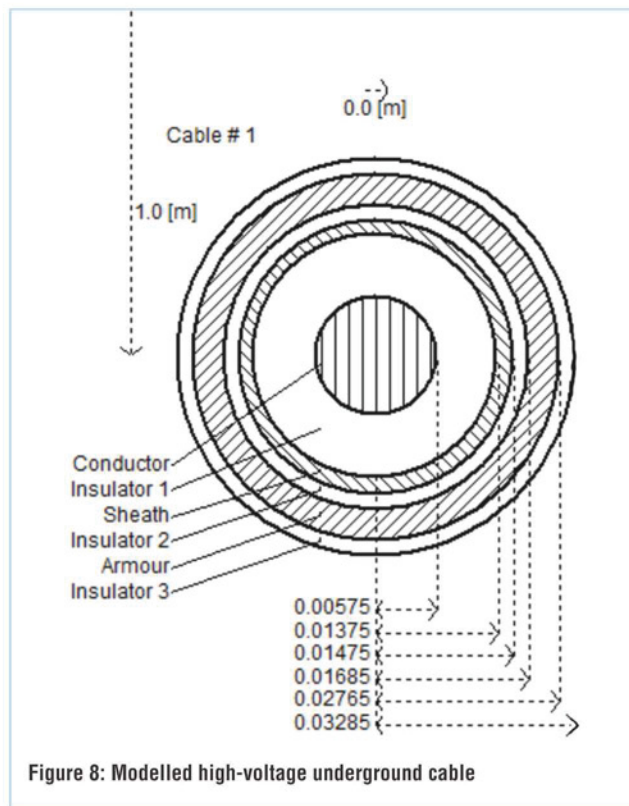


Figure 8: Modelled high-voltage underground cable

are three layers in the hidden layer section, each with five neurons. The training errors for several hybrid ANN methods are calculated to be 2.065, 0.1880, 0.1966, 0.3072, 0.2122, 0.1363 and 0.1309 for ANN, PSO-ANN, GA-ANN, ABC-ANN, CSA-ANN, DEA-ANN and DEA-CSA-ANN respectively. It is seen that the training error for DEA-CSA-ANN is lower than that of the other methods.

The forecasting errors for each of these methods are also determined, and the input data (shown in Table 1) used to forecast the sheath current. The table shows 12 different cases

that were generated in PSCAD/EMTC. Also, ISA is the actual value of the sheath current, obtained with the simulations. The forecasted sheath current values (ISF) of these cases are shown in Table 2.

The forecasted errors for each of these algorithms are 1.586, 0.2377, 0.2916, 0.7415, 0.1756, 0.4307 and 0.1109 respectively. Table 2 shows that results of the DEA-CSA-ANN method are closest to the actual sheath current. Also, both the training error of DEA-CSA-ANN and the forecasting error of DEA-CSA-ANN are lower than that of the other methods, therefore the DEA-CSA-ANN method is recommended as most suitable for parameter forecasting studies.

For example, if a high-voltage underground cable line is a $1 \times 95 \text{ mm}^2$ XLPE cable with the conditions of case 11 in Tables 1 and 2, then the sheath current forecast by the DEA-CSA-ANN method is 3.51A. The appropriate precautions can then be applied to the cable to reduce this current. These measures can also use resistance and inductive reactance. Choosing high values for these is necessary to reduce sheath currents, but the high sheath voltage carries risk of electroshock. In this case, the solid bonding method is used so the sheath voltage is reduced to 'touch' voltage. ●

	I_{ub}	L	d	R_0	I_{SA}
Case 1	224.630	250	0.1	6	3.61
Case 2	224.630	500	0.1	10	3.30
Case 3	224.630	500	0.1	40	1.08
Case 4	224.630	500	0.5	9	4.42
Case 5	224.630	250	0.5	6	3.34
Case 6	464.120	250	0.5	10	4.48
Case 7	464.120	400	0.1	35	2.20
Case 8	464.120	700	0.1	40	3.32
Case 9	464.120	500	0.5	35	2.54
Case 10	464.120	500	0.5	40	1.97
Case 11	464.120	1000	0.5	50	3.48
Case 12	224.630	1000	0.1	50	1.71

Table 1: Input data for forecasting the sheath current

	ISA (A)	ISF (A)						
		ANN	PSO-ANN	GA-ANN	ABC-ANN	DEA-ANN	CSA-ANN	DEA-CSA-ANN
Case 1	3.61	4.54	3.00	4.21	3.26	3.48	7.17	3.61
Case 2	3.30	4.54	3.32	4.17	4.49	4.49	3.42	4.42
Case 3	1.08	4.54	2.27	2.88	4.53	1.34	2.86	0.86
Case 4	4.42	4.54	3.36	4.22	4.49	4.62	3.43	4.51
Case 5	3.34	4.54	3.00	4.22	3.26	3.05	2.97	3.58
Case 6	4.48	4.54	2.82	3.15	3.49	3.98	3.40	4.40
Case 7	2.20	4.54	2.24	2.15	4.26	2.19	3.25	2.23
Case 8	3.32	4.54	2.60	2.10	5.73	3.38	3.77	3.18
Case 9	2.54	4.54	2.41	2.22	4.75	2.79	3.44	2.71
Case 10	1.97	4.54	2.23	2.00	4.75	2.26	3.35	2.12
Case 11	3.48	4.54	2.81	1.84	7.22	4.07	4.19	3.51
Case 12	1.71	4.54	2.86	2.72	6.99	3.15	3.70	2.25

Table 2: The forecasted sheath current results of the hybrid ANN methods



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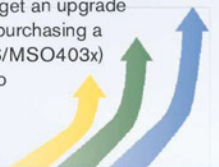
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3D V-NAND WITH NVME – THE FINAL PIECE IN THE SSD JIGSAW

THOMAS ARENZ, DIRECTOR AT SAMSUNG SEMICONDUCTOR EUROPE, GIVES A DETAILED COMPARISON BETWEEN THE TRADITIONAL APPROACHES TO STORING AND MANAGING GROWING VOLUMES OF DATA IN REAL TIME AND THE NEW, FORWARD-MOVING OPTIONS

W

ith the rise of big data and the Internet of Things (IoT), data centres are now required to process and store more information than ever before. As it stands, the volume of data being produced around the world is doubling every two years, with 2.5 exabytes of data being created

every day. At this rate, it is predicted that the total volume of data will reach 44 zettabytes (44 billion terabytes) by 2020.

While this is great news for those hoping to utilise big data to develop more advanced models for business intelligence, it does present challenges from a hardware and information analysis perspective.

Despite the vast quantities of data currently being created, less than 1% is analyzed and used to create any lasting value. This situation is improving, with the quantity of useful data expected to increase from 1ZB to 15ZBs over the next five years. But, for this to happen, we must first look to the necessary hardware infrastructure. As it stands, there

“It is predicted that the total volume of data will reach 44 zettabytes (44 billion terabytes) by 2020

is little point in attempting to analyze data if there isn't the capacity for storing and managing it.

Traditional approaches to storing and managing vast volumes of data in real time are rapidly becoming unsuitable. Outdated legacy hardware is suffering, with traditional hard-disk drives no longer providing adequate performance and acceptable storage-to-size ratio. Fortunately, numerous advancements in information storage technologies have helped lay the groundwork for the future of data centre management, so big data will no longer be a big problem.

HDDs vs SSDs

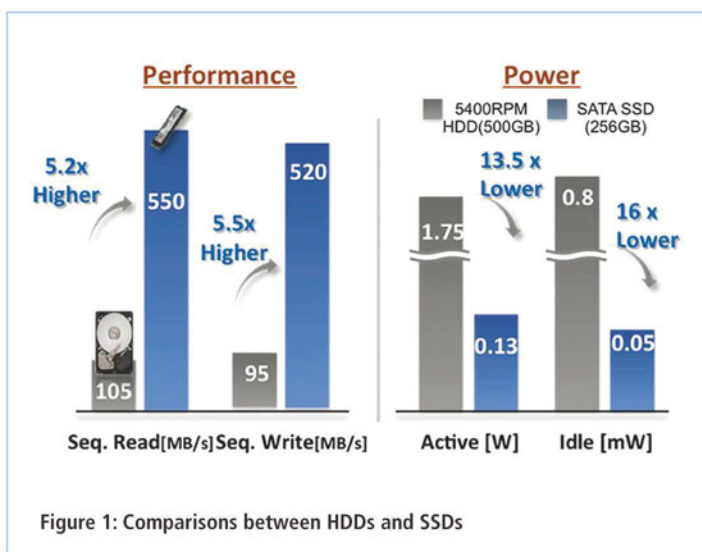
The first of these ground-breaking technologies was the move from traditional hard disk drives to solid state; the future of data centre storage is almost undeniably flash-based. Many solid state drives (SSDs) offer 5x higher performance with 16x lower power consumption. Flash offers considerably better performance, reliability and speed benefits for real-time access to data than hard disk drives (HDDs).

While still roughly six times more expensive than spinning HDDs, the falling price of flash storage has helped make SSDs more appealing to data centre managers, who are looking for smaller, cooler and more energy-efficient drives.

Responding to these demands, memory manufacturers started shrinking their flash components to accommodate more storage per hard drive and, ultimately, more hard drives per data centre. However, this resulted in its own set of problems, which have been solved by Samsung by thinking differently.

When Samsung's first storage with NAND flash was developed in 1999, it was based on a design rule of 120nm. This ultimately shrank devices to the '10nm class' (10-20nm), allowing manufacturers to fit 64 times more cells into the same space. Generally speaking, this reduction in size has followed Moore's Law, with the number of cells roughly doubling every two years.

As fabrication technology reached the 10nm class and beyond, engineers have grown increasingly aware that they may one day reach a potential 'scaling limit' – as ever more cells are crammed into the same physical space, a number of significant challenges arise, such as cell-to-cell interference. As the space between cells decreases, they begin to affect each other's behaviour through coupling, an interference that can



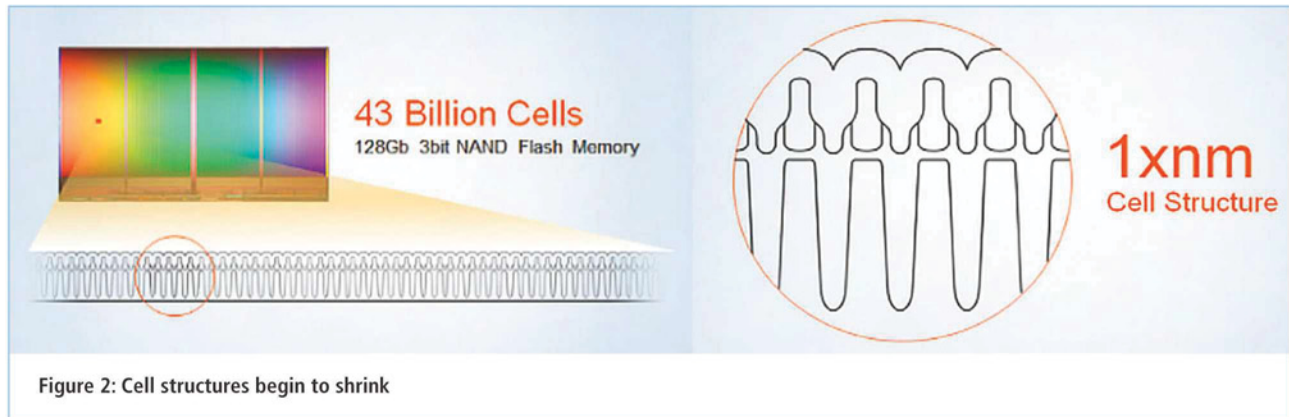


Figure 2: Cell structures begin to shrink

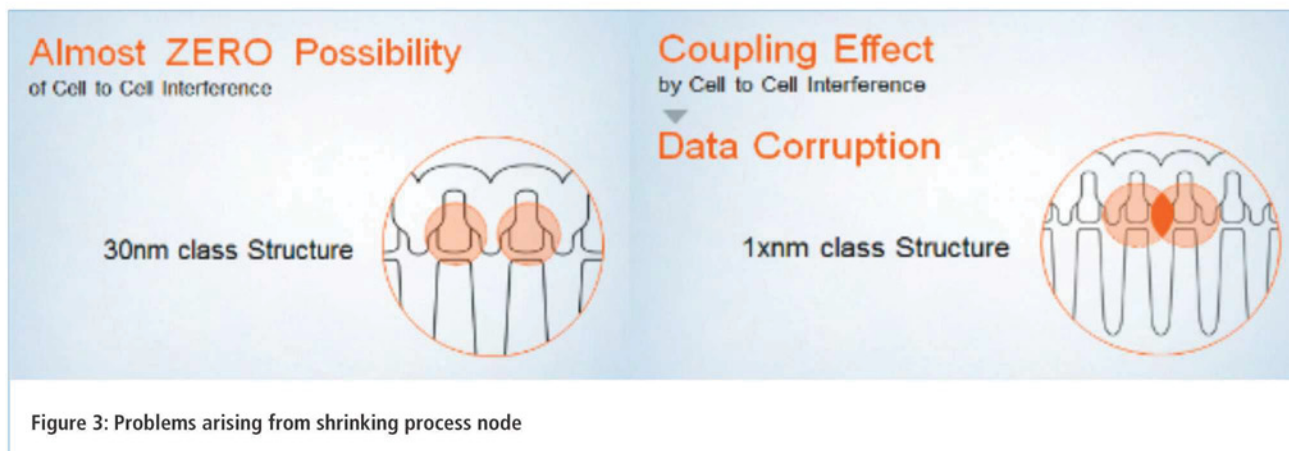


Figure 3: Problems arising from shrinking process node

ultimately lead to damage and data corruption.

Generally, when cells are based on process technology of 30nm or above, cell-to-cell interference can easily be controlled through design. As the technology node becomes smaller, however, the probability of data corruption dramatically increases.

Shrinking NAND cells also leads to growing difficulties in the photolithography process. As the design rule gets smaller, it becomes increasingly difficult to find an appropriate light source. As one example, the light source for a 40nm class design rule can be used to inscribe photo mask patterning on a NAND wafer without any problems. However, once the design approaches 1nm, this light source cannot penetrate the smaller pattern. As a result, the development of an adequate light source for 1x nanometer patterning requires a huge investment in new equipment.

In summary, in order to reduce the size of their components, manufacturers are forced to squeeze memory cells ever closer together. As the space between these cells becomes smaller, solid-state drives are more likely to suffer a

higher level of interference and potential data corruption. This scaling limit would have made such products less reliable for inclusion within servers, and ultimately unsuitable for data centres.

3D V-NAND

In order to address this issue, Samsung set about developing a new form of “vertical” memory, incorporating more cells without pushing them closer together. Launched in 2013 as 3D V-NAND (Vertical NAND), this new technology would accommodate more memory by building vertically on top of existing structures, rather than attempting to squeeze more cells into the same horizontal space.

The idea originally started its life as a simple analogy between living in a house and living in an apartment building. The benefits of layering vertically are much the same as building vertically. Where once a two-story home could only house four people, apartment blocks meant that hundreds more people could be housed in the same area, without reducing the overall size of their housing units. The result was a much higher population density in the same area as a single dwelling.

By layering the cells on top of each other, Samsung was able to apply this analogy to its NAND memory, building

“ In terms of SSD output, the result is much like a donkey dragging a Ferrari

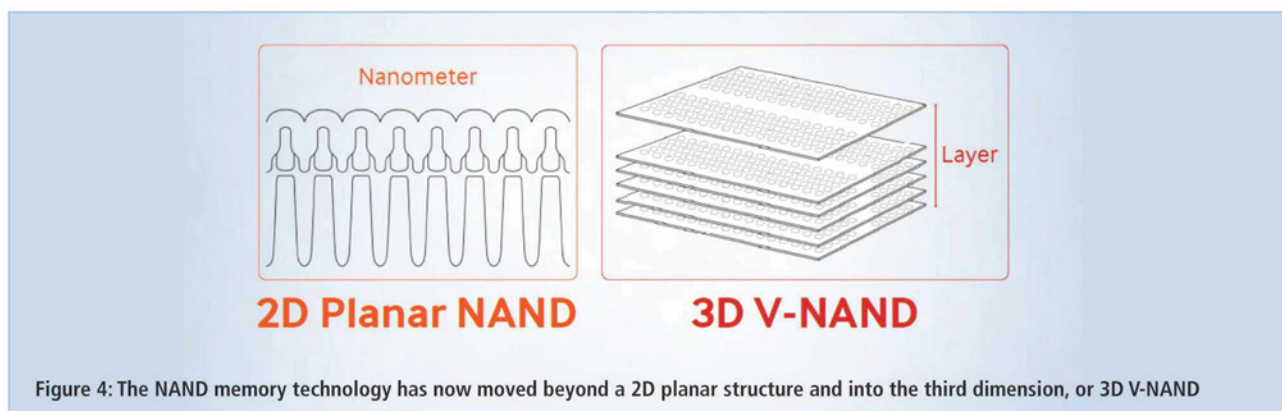


Figure 4: The NAND memory technology has now moved beyond a 2D planar structure and into the third dimension, or 3D V-NAND

vertically to create the new V-NAND (Vertical NAND) structure. Initially, this structure consisted of 24 vertical layers; this has already increased to 48 layers. As a result, the technology has now moved beyond a 2D planar structure and into the third dimension – thus, 3D V-NAND.

The benefits of the third dimension help increase storage capacity, but also improve each individual cell's endurance. If its job is write-intensive, then users will see up to a five-fold improvement in the longevity of their devices. If on the other hand it is read-centric, users can expect up to a tenfold improvement. There can also be as much as 100% increase in write speed, helping to lower energy consumption and save on additional maintenance costs.

While the idea of moving from the horizontal to vertical planar structure appears simple enough, it actually took almost a decade to develop one that works. As the first memory manufacturer to offer Vertical NAND, Samsung Semiconductor had to secure more than 300 patents just to cover the base-level components involved in overcoming the various challenges of the design.

Key among these decisions was the type of materials used. Instead of using conductors, through which charges can move freely, V-NAND technology required insulators. Insulators are closer to solids, making charges struggle to move through them at the required pace. To solve this issue, Samsung's research team examined 10-year-old CTF (Charge Trap Flash) technology, ultimately revamping its cylinder-shaped

architecture. This allowed the development of an architecture in which electric charges were temporarily placed in a holding chamber composed of silicon nitride (SiN) until required. This new technique was then used as an alternative to traditional

floating gates, helping prevent further interference between neighbouring cells.

Solving these initial challenges of 3D V-NAND did not come cheap. However, with the rise of big data, Samsung understood that the memory market needed a revolution to keep up with the latest storage and retrieval demands. Unfortunately however, while 3D V-NAND has proved an international success, on its own

it would not be enough to effectively manage big data. There remained one piece of the server-side jigsaw puzzle yet to be addressed.

NVMe: A Firmware Foundation

When SSDs first came to market, manufacturers traditionally built with SATA and SAS buses for interfacing with the rest of the computer. At the time, these buses worked well for SSDs, because the solid state was comparable with HDDs in terms of speed. Now that the speed of SSDs has increased so significantly,

“Despite the wider industry finally committing to 3D NAND, this shift will not be enough without the connecting infrastructure necessary to support it”

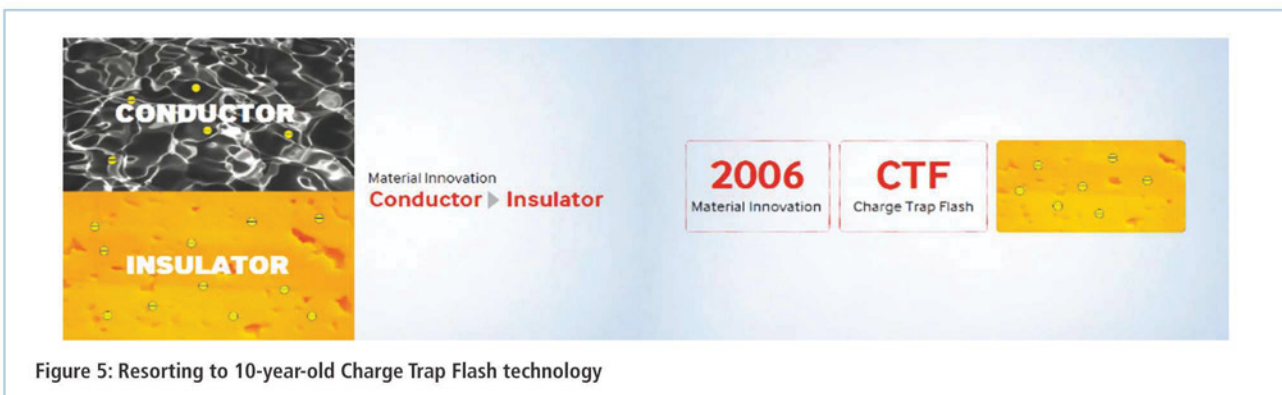


Figure 5: Resorting to 10-year-old Charge Trap Flash technology

these antiquated buses are starting to hold SSDs back. In terms of SSD output, the result is much like a donkey dragging a Ferrari. No matter how much technology goes into the Ferrari, or how much faster Ferraris become over time, if the donkey doesn't speed up, the Ferrari will never reach its full potential.

The proof is in the numbers. SATA's 600Gbps maximum speed means that most state-of-the-art SSDs will operate at the same speed, roughly 500Mbps, despite their different speed capacities. SSD tech is capable of so much more; it's just that the technology around it has to be up to the task.

Non-Volatile Memory Express (NVMe) is the technology that will give these SSDs room to stretch their legs. In a nutshell, NVMe is a game-changing storage standard for PCIe-connected drives. Combined with a U.2 (SFF-8639) connector, it is set to replace both SAS and SATA for high-speed, low-latency storage. More specifically, its firmware – a communications interface protocol – works as part of the server's existing high-bandwidth peripheral component interconnect express (PCIe) bus. NVMe helps to define both a command set and a feature set for PCIe-based SSDs, managing the underlying data transport layer for graphics and other add-in cards.

The NVMe-enabled PCIe works specifically with the latest SSDs and is capable of extracting the most value from an SSD. PCIe 2.0 offers 500Mbps per lane and PCIe 3.0 offers 985Mbps. But, by installing a card in a four-lane PCIe 2.0 slot, bandwidth will increase to 2Gbps, and by installing a card in a PCIe 3.0 slot, bandwidth will soar to 4Gbps – perfect for today's fastest SSDs.

Using NVMe, PCIe offers faster speeds, lower latency and lower energy consumption than SATA. This enables an entirely new breed of storage architecture, making data available to the CPU in large chunks, ultimately offering massive bandwidth and IOPS (input/output operations per second) improvements over both SATA and SAS. Based on Samsung Semiconductor's own tests, NVMe SSD offers up to four times the read/write performance of SAS, 2.1x faster latency and 13.5x lower power consumption than active SATA SSDs.

In short, NVMe optimises the processor's driver stack so it can handle the high IOPS associated with flash storage. At the same time, the greater queue depth provided by NVMe helps to open up the flash storage for maximum use. This means a new form of data management, offering high performance (SM953- Seq. R/W: 1.75/0.85GB/s) with significantly lower active power (< 8W).

This new relationship between bus and firmware enables OEMs to produce faster, better and more robust SSDs without compromising on either size or energy efficiency. Combined with the existing benefits of V-NAND technology, this represents a huge incentive for those looking to manage big data and considering an ultimate transition away from traditional hard disks.



Figure 6: NVMe SSD benefits

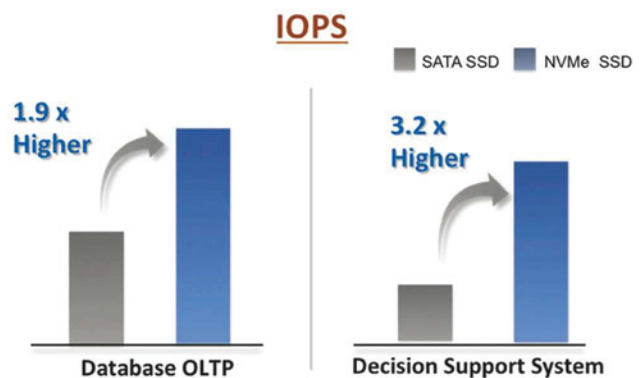


Figure 7: NVMe SSD vs Sata SSD

Forward-Looking

While Samsung Semiconductor may have been the first to develop 3D V-NAND technology, several other manufacturers are launching their own three-dimensional, stacked memory solutions. This shift is extremely positive, highlighting that the entire industry is finally pulling in the same direction and ultimately working toward the same universal standards – a rarity in much of the electronics space.

But despite the wider industry finally committing to 3D NAND, this shift will not be enough without the connecting infrastructure necessary to support it. Storage and processing may improve dramatically over the next few years, but as long as they continue to run obsolete firmware and connect through antiquated buses, the bottlenecks will remain the same. V-NAND or otherwise, SSDs cannot reach their potential without NVMe in place. It's time to unharness the donkey and let the Ferrari fly. ●

ACCURATE MECHANISM FOR PREDICTING THE STATE OF SENSORS

JING QI, YUMEI WEN AND PING LI FROM CHONGQING UNIVERSITY IN CHINA HAVE DEVELOPED AN ACCURATE SENSOR-STATE PREDICTION MECHANISM TO ENHANCE THE EFFICIENCY OF SENSOR SEARCH SYSTEMS

R

apid developments in embedded sensor techniques, wireless communication technologies and information processing have contributed to the emergence of the Internet of Things (IoT), an integrated platform that connects all aspects of the world. Sensors are being attached to objects to connect them to the Internet,

allowing them to be accessed using a web browser. Some novel web-based services like pachube.com, Xively and Microsoft SenseWeb, publish that sensor data on the web. For example, Bicing is a public bicycle-sharing system in Barcelona that allows a user to check for occupancy and position of bicycles in the city via the web. Such developments pave the way for content-based sensor searches to be in great demand in the IoT future.

IoT And Sensors

In the IoT network, the states of sensors are rapidly changing. Because the classic search engines, such as Google, Chrome and Yahoo, are used mainly for static searches or slowly varying unstructured content (web pages, PDFs and Word files), they are not able to cope with more dynamic searches. Also, accessing all available sensors and collecting their states results in tremendous communication overhead.

In 2010, researchers at the Swiss Federal Institute of Technology in Zurich (ETHZ) proposed a novel sensor search engine called Dyser to efficiently search for real-world entities based on the data they produce. However, Dyser relies on descriptive data rather than specific readings (for example, “warm” vs “30°C”). It also relies on the repetitiveness of that information, which may be limited in some applications where an output is a specific reading.

In response to this, researchers at the University of Lübeck in Germany presented a content-based sensor search engine (CSS) in 2013, which searches for raw output data without expectation of any repetitiveness. A light-weight prediction model based on fuzzy logic is applied to CSS to estimate the probability of a state of a sensor that matches a given search. However, the prediction model in CSS is time-independent, so it's unable to accurately present the latest trends of sensor states. Moreover, the prediction model in CSS is created by each sensor itself, which implies that sensors should have powerful computing capacity and power resources, which is impractical.

Therefore, we developed an accurate sensor state prediction mechanism (ASPM) to address these issues; see Figure 1.

System Design

ASPM consists of four main parts: terminal, gateway, database and sensor. The user initiates a sensor search through the terminal. We define the search query as a combination of information, such as geographical location, type of sensors used, search range and so on. For example, the search query can be “the coast of the United States, water level, $[a,b](t_q)$ ”, meaning the user wants to find out the water level readings satisfying the $[a,b]$ range at time t_q .

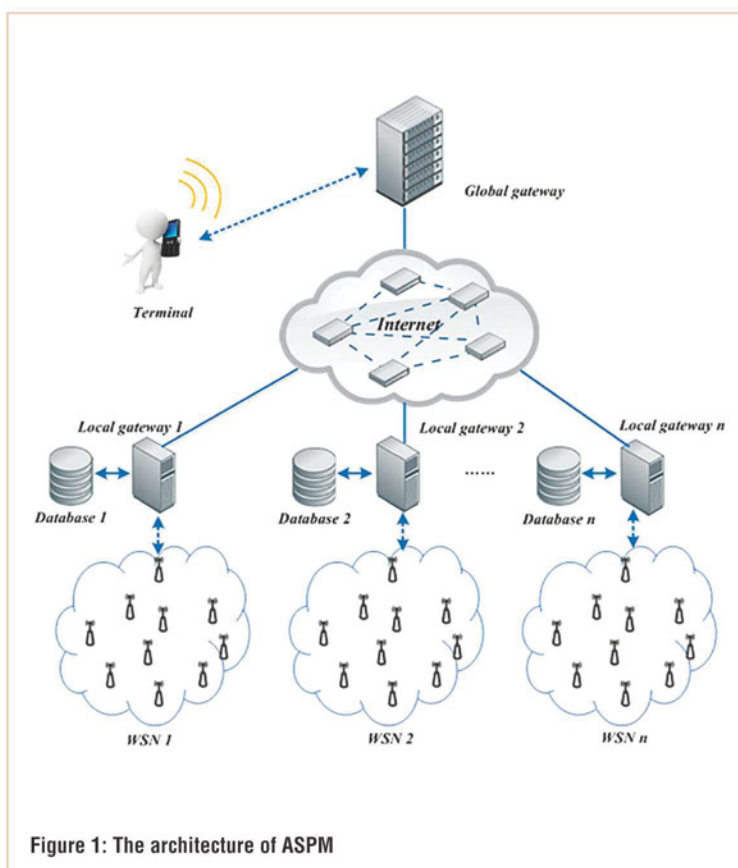


Figure 1: The architecture of ASPM

The gateways distribute the data across the Internet in a layered structure. The top-layer gateway, named global gateway, responds to the search query and sends it to the appropriate level lower gateway.

ASPM contains a method to approximate the collected sensor state values in a time-dependent manner. This information is sent to the local gateway which then predicts the future state values for all the sensors it manages. The search process is shown in Figure 2.

Each local gateway has a database where the prediction data is stored, so it is the local gateway that finds the candidate sensors whose values fit within the search range. The match list is then sent to the global gateway, which decides which sensors to query and asks for their actual readings, with the final results being made available to the user.

With this method, the communication overhead is significantly reduced because only sensors with readings that belong to the search range are accessed.

3.1 Approximation Method

The frequency of collecting sensor data is usually much higher than the frequency of reporting it, which means the sensor will consume more power to transmit data to the gateway. To counteract this, we propose an approximation approach based on the Piecewise Linear Representation (PLR) theory.

PLR is about approximation of a time series T , of length n , with K straight lines. Because K is typically much smaller than n , this approximation would largely reduce the transmission of data and save power for the sensor. As most sensors in the IoT have limited computing and energy resources, we cannot assign complex computing tasks to them. So, we adopt the Sliding Window algorithm, which is an online PLR method that executes whenever a new value arrives, without scanning the entire data-set, to approximate the collected values.

The approximation algorithm runs by anchoring the left point of a potential segment at the first data point of a time series, and then tries to fit the first data point and the right data point into increasingly longer segments. We assume the collected sensor state values in the time series are $S = \{t_p, s_p\}$, $i = 1 \dots \rho$ where ρ is the reporting period. At the segment point i , if the approximation error is larger than the predefined threshold,

Communication overhead
is significantly reduced because only sensors with readings that belong to the search range are accessed

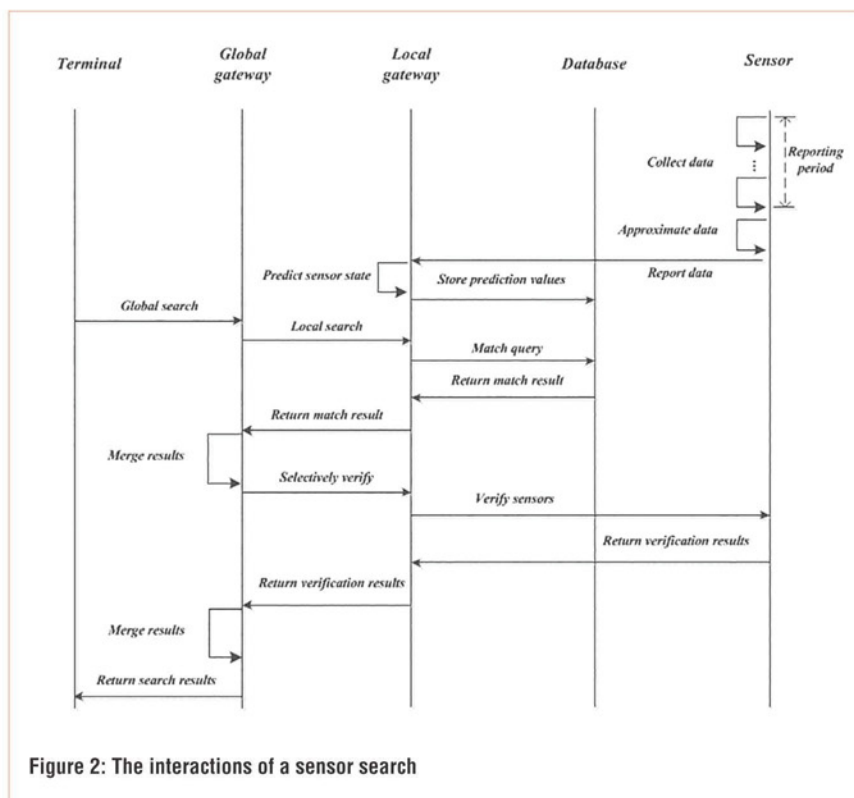


Figure 2: The interactions of a sensor search

then the anchor to point $i-1$ is considered as a segment. We move the anchor to the next segment point i and repeat the process until S has been transformed into a piecewise-linear approximation, which is an approximation of several segments represented in a linear equation. Thus, we deduce that the computational complexity of the approximation method is $O(Ln)$, where L is the average length of segments.

3.2 Time-Dependent Prediction Method

As mentioned earlier, current sensor-state-prediction methods are mainly time-independent and so fail to accurately determine the temporal correlations between data. So we devised a prediction method based on the Least Squares Support Vector Machines (LS-SVM), which is a state-of-the-art time-dependent regression prediction theory.

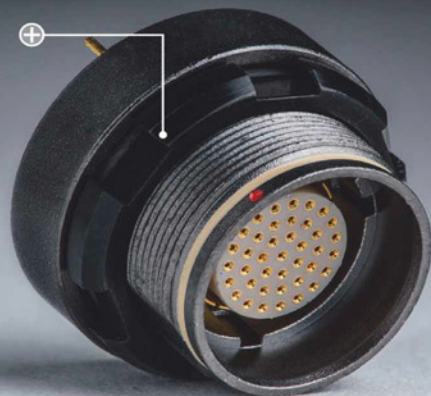
Our prediction method nonlinearly maps the collected data into a high-dimensional input space and constructs an optimal separating hyper-plane in this space. It then exploits Mercer's theorem to avoid explicit formulations of the nonlinear mapping.

LS-SVM can achieve better and more stable regression prediction performance by discarding unimportant information and highlighting the important information.

In general, our prediction method better exploits the temporal correlations between the collected sensor data, and is more accurate in predicting sensor states with only

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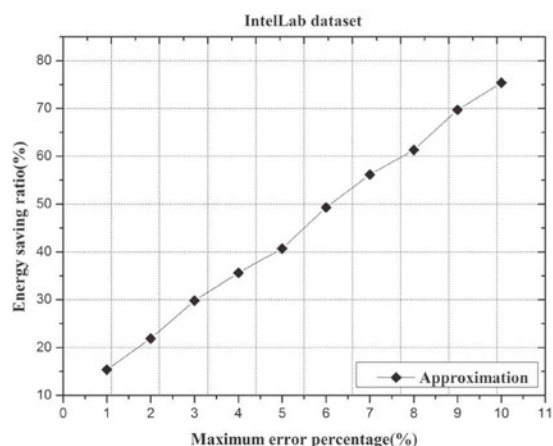


Figure 3: Power-saving ratio performance for IntelLab

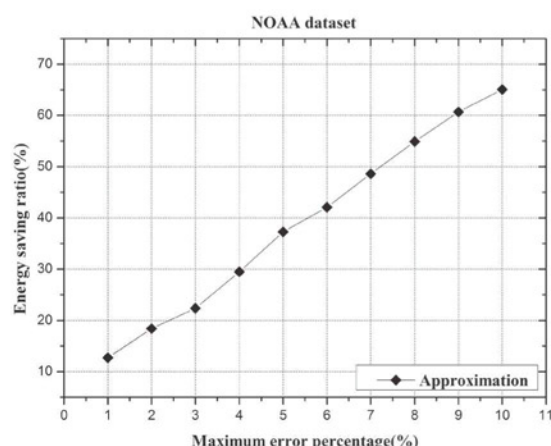


Figure 4: Power-saving ratio performance for NOAA

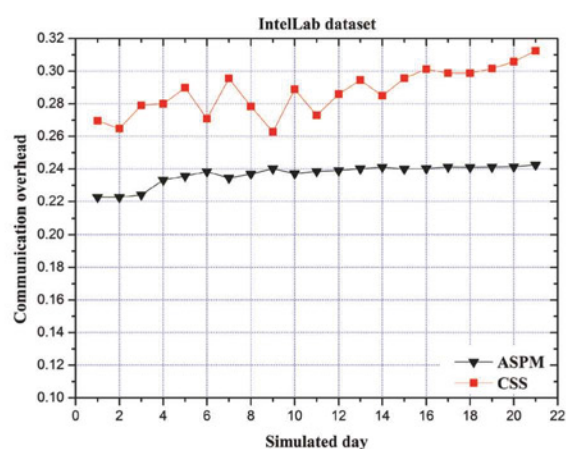


Figure 5: Communication overhead with different simulated days for IntelLab

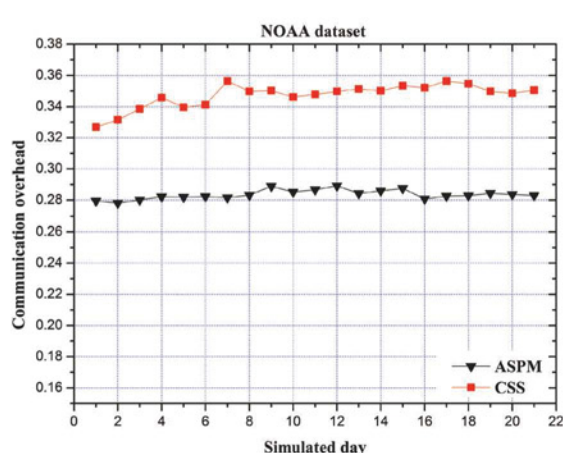


Figure 6: Communication overhead with different simulated days for NOAA

a small number of samples. After the local gateway receives the approximated values reported by the sensor, our prediction method estimates the future sensor output at any query time during the next reporting period.

Performance Evaluation

To evaluate the performance of our prediction mechanism, we used 54 temperature sensors at the Intel Berkeley Research lab (IntelLab) and 98 water temperature sensors located along the American coast, provided by NOAA. The experiments were handled by a PC with Intel Core i7 CPU and 8GB RAM running MATLAB 2014b. Each simulation result averaged 100 runs.

To evaluate the performance of our approximation method and the communications overhead, we introduced a power-saving ratio proportional to the number of sensors used. So, the maximum error percentage is the ratio of maximum error

to the range of collected values (see Figures 3 and 4).

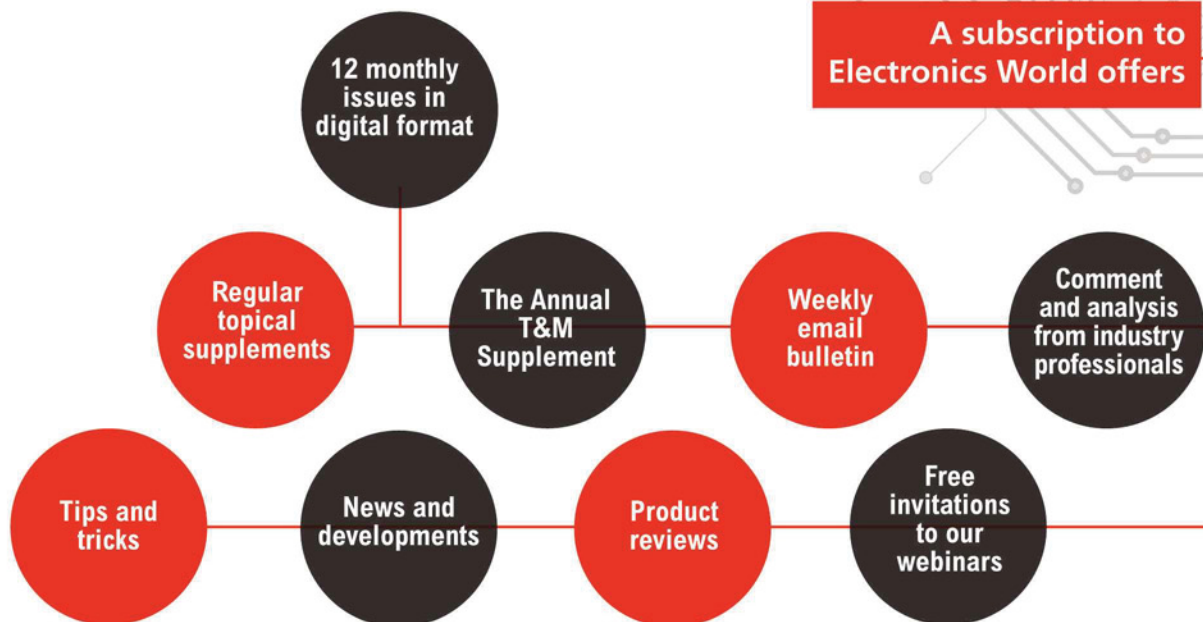
It can be seen that the power-saving ratio increases with the maximum error percentage, because the growing maximum error percentage reduces the number of segments, which in turn lowers the amount of data that needs to be transferred to the gateway. This in turn reduces the transmission energy; our approximation method saves some 45.5% of power for IntelLab and 39.2% for NOAA.

In Figures 5 and 6, we see that ASPM stays relatively stable, while CSS shows a large degree of volatility. The reason is that our prediction method does an excellent generalization. Also, the prediction accuracy of ASPM does not change much, keeping the communication overhead stable. Actually, we've noted that ASPM decreases the communication overhead about 17.4% and 18.3% for IntelLab and NOAA respectively in comparison to CSS. ●

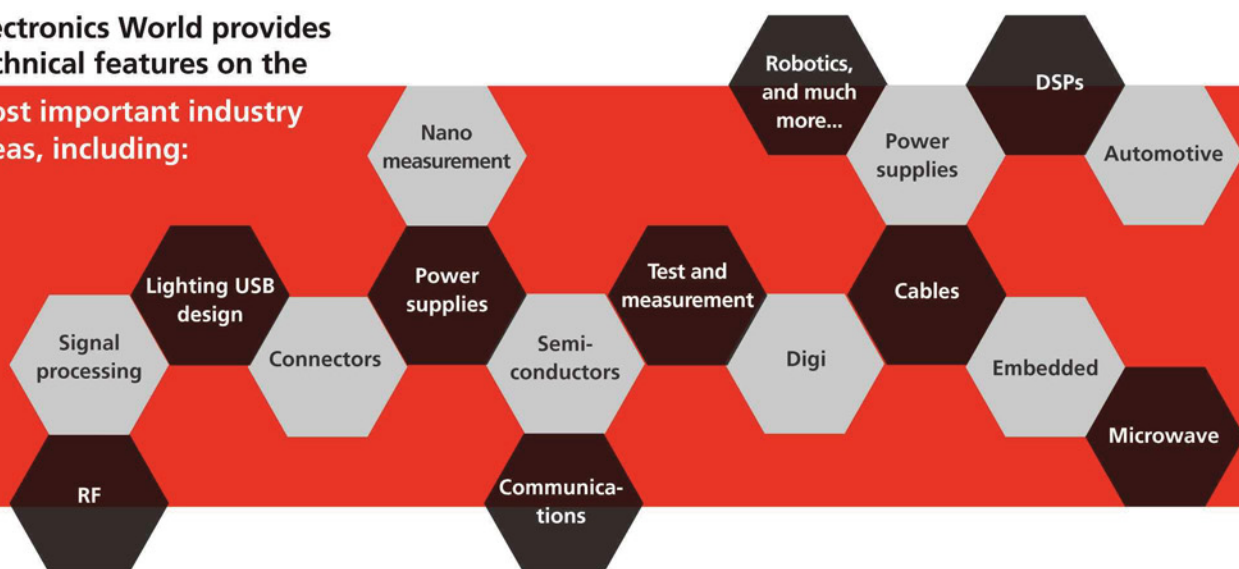
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RS Components and Allied Electronics, trading brands of Electrocomponents, are placing a greater focus on their Private Label business with the launch of the new RS Pro brand, creating a single unifying value proposition for their private label product range. The RS Pro range of more than 40,000 high quality, competitively-priced industrial products and electronic components will evolve and expand, extending its reach in the UK, Europe, Asia Pacific and North America.

The range offers customers choice where the combination of quality, performance and price create exceptional value. To ensure customers have complete confidence in the RS Pro offering, all products and components will now be backed by the RS Seal of Approval, representing leading industry standards for audit, inspection, test and certification.

www.rs-online.com



AUTOCLAVABLE MASS FLOW METER REUSABLE SENSORS BY SENSIRION

Sensirion has been making flow metering sensors for many years. Until now, these sensors have been used in ventilation and anesthetic devices in medical environments to measure the volume of clean air administered to a patient. As both procedures also require metering the flow of exhaled air, known as either proximal or expiratory flow metering, Sensirion has been working on suitable solutions. In both cases, a sensor comes in contact with air from the patient that may be infected with germs and pathogens, potentially compromising the equipment. So, for the sterilization process, several approaches are possible.

The solutions used today are either hot-wire anemometers or (variable) apertures combined with a differential pressure sensor. However, the sensor is not always exchangeable or sterilizable. In measurements involving the differential pressure process particularly, only the metering section is replaced.

www.sensirion.com



RITTAL WILL EXHIBIT AT DRIVES AND CONTROLS 2016

Visitors to Rittal's stand D230 at Drives and Controls 2016 in Birmingham in April will be able to view its innovative modular enclosures, power distribution and climate control systems. Of particular note will be the presence of the new, award-winning Blue e+ climate control system, launched last year, offering outstanding energy savings and flexibility.

There will also be the chance to understand more about panel building automation, as well as servicing and maintenance programmes, designed to maximize system's efficiency, flexibility and longevity.

Rittal infrastructure system called "Rittal – The System" offers five perfectly matched modules: rack, power, cooling, security and monitoring and remote management.

The company will also show live demonstrations of its products on stand D964, offering a hands-on experience.

www.rittal.co.uk



ODU EXCEEDS EURO140M TURNOVER MARK

For over 70 years, ODU has been leading the way in high-performance connector technology for demanding applications. In 2015, the internationally active company managed to increase its turnover from euro 139m to 146m euros, a 5% growth rate.

"We actually exceeded our original target of crossing the 140-million-euro threshold. We're particularly pleased with this result considering the context of the global economy, which, on the whole, has cooled down quite significantly," said Dr Joachim Belz, CEO at ODU. "Our goal for 2016 is to cross the 150-million-euro threshold."

A number of measures help secure the company's continued success; in addition to expanding its R&D department and laboratory, ODU is also focusing on its new global management structure.

"This strategically crucial step is helping us strengthen the business in Europe, North America and Asia," said Belz.

www.odu.de



ELM EV ADOPTS NEW TEST TECHNOLOGY

Elm Electric Vehicle Charging Solutions has become one of the first companies to use a new test technology for fast and efficient fault-finding and maintenance of charging installations.

Its new EV100 test instrumentation was developed by Seaward for comprehensive validation testing and fault finding on all types of AC electric vehicle charging equipment. Elm is independent electric vehicle supply equipment (EVSE) company, responsible for over 2,000 charging-point installations for private and public sector clients throughout the UK.

For diagnostic testing, the dedicated EV100 tester simulates several different vehicle faults and measures the EVSE response, including disconnection time and the amplitude, frequency and duty cycle of the PWM signal. Tests and maintenance schedules are done automatically and in accordance with IEC 61851.

www.seaward.co.uk/EV100



HAND-SOLDERING COMPETITION

Coming back to the NEC is the IPC Hand-Soldering Competition in association with Advanced Rework Technology, returning to National Electronics Week from 12th-14th April 2016. There are cash prizes and a ticket to SMT Nuremberg 2017 for the winner who will pit their skills against an international pool of experts.

Participants will compete to build a functional electronics assembly within a 45-minute time limit. Assemblies will be judged on soldering in accordance with IPC-A-610F Class 3 criteria, the speed at which the assembly was produced and overall electrical functionality of the assembly.

If interested in competing this year, contact: marketing@neweventsLtd.com



GRAMMATECH ANNOUNCES BINARY ANALYSIS SUPPORT FOR ARM

GrammaTech, provider of software assurance, hardening, and cyber-security solutions, expanded its CodeSonar's static analysis engine to include binary analysis for ARM, the dominant processor of the Internet of Things (IoT). CodeSonar is the only commercially-available static analysis tool on the market to provide binary analysis, allowing engineering teams to analyze application software, middleware and firmware.

Analyzing machine code has become extremely important in the expanding world of IoT, where deployed devices are subjected to countless cyber-attacks. Today's systems are at significant risk without knowing exactly what defects and vulnerabilities may lie within operating systems, drivers, middleware, or supplier applications. CodeSonar's binary analysis allows you to analyze your x86 or ARM system via binary-only or mixed-mode analysis, identifying both source and binary defects hazardous to your device. www.grammatech.com



HARTING PRELINK CONNECTION TECHNOLOGY NOW AVAILABLE IN HAN 3A HOUSING

Harting preLink end-to-end Ethernet connection technology is now also available in the form of an RJ45 connector face in a robust Han 3A connector housing.

PreLink offers a fast and easy way to set up enterprise-wide networks that extend all the way from IT through to the manufacturing level. With the preLink concept, Harting has succeeded in separating the previously fixed connection of cables and connectors into two independent, reusable components: the preLink termination block and the interchangeable sockets and connectors.

The preLink termination block incorporates a holder for 4- or 8-wire Ethernet cable, which can be assembled with 100% certainty in a single step using the dedicated preLink assembly tool. This termination block fits into a variety of RJ45 or M12 sockets and connectors.

www.harting.co.uk



NEW FAMILY OF COMPLETE MICROSTEPPING MOTOR DRIVER ICs FROM ALLEGRO

Allegro MicroSystems Europe has introduced a new family of complete microstepping motor driver ICs with built-in translators. Its A5976, A5977 and A5979 have been designed to operate bipolar stepper motors in full, half, quarter, eighth, (A5977) and sixteenth (A5976/79) step modes. All have the output drive capability of 40V and $\pm 2.8A$ and include a fixed off-time current regulator that has the ability to operate in slow, fast, or mixed-decay modes. This current-decay control scheme results in reduced audible motor noise, increased step accuracy and reduced power dissipation.

These new devices are targeted at the office and industrial automation markets, including textile and sewing machines, vending machines, printers, scanners, copiers, closed circuit TV camera positioning, ATM machines, 3D printing systems and food industry applications.

www.allegromicro.com



NEW 50A OR DUAL 25A MODULE REGULATOR FROM LINEAR

Linear Technology has introduced the LTM4650, a dual 25A or single 50A output step-down μ Module regulator with onboard shielded inductors, MOSFETs and a dual DC/DC regulator IC, housed in a small thermally enhanced plastic package. The device is offered in a 16mm x 16mm x 5.01mm BGA with a patented built-in heat sink. The heat sink, attached to the MOSFETs and inductors, rapidly moves heat from the interior of the package to the top, where the surface of the heat sink is exposed to air. Thermal dissipation is further improved with airflow, or a combination of airflow and attachment to an external heat sink. With no external heat sink, the LTM4650 delivers 50A from 12VIN to 0.9VOUT at up to 71°C ambient temperature with 200LFM airflow or up to 77°C with 400LFM.

www.linear.com



MULTI-GIGABIT BASEBAND PROCESSOR FOR WIRELESS FIBRE APPLICATIONS

Lattice Semiconductor announced the company's new baseband processor – the SB6541 – designed for use in conjunction with Lattice's Si16340 and Si16342 RF transceivers to target fixed wireless access and wireless backhaul of urban broadband infrastructure, such as LTE small cells and metro Wi-Fi access points.

Increasing demand for gigabit IP data to the home is driving demand for fixed wireless broadband access. In addition, in high data-density areas, gigabit IP data connectivity is required for metro Wi-Fi and LTE deployments. The 60GHz band is ideal for these applications due to the large bandwidth available and the unique propagation characteristics of the band that allow high spectrum reuse, both of which are essential for next-generation wireless network architectures. The chipsets offer the industry's first complete solution in the 60GHz frequency band, leveraging SiBEAM technology.

www.latticesemi.com



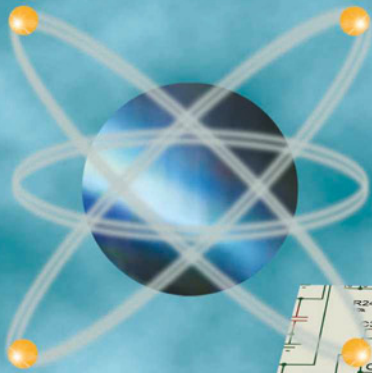
SEMTECH'S MIL-PRF-19500/406M-QUALIFIED 1.5W ZENER DIODE FAMILY NOW AT ASTUTE

Astute Electronics now offers new DLA and QPL-qualified Zener diodes from Semtech. The new 1N4460 and 1N4461 devices feature breakdown voltages from 6.2-200V and are qualified and designed to meet the high reliability requirements of some of the most demanding applications, including satellites, industrial machinery, automobiles and medical equipment.

The newly-qualified 1.5W Zener diode voltage regulators are available in all QPL levels from 1N through JAN, JANTX, JANTXV to JANS (space level), and along with the rest of the /406 product family, are hermetically glass-sealed, passivated devices that are available with axial leads or square end tabs for surface mounting.

"The new Zeners round up Semtech's /406 family of rectifiers, Zeners and transient voltage suppressors, which are produced in a state-of-the-art manufacturing facility, certified to MIL-PRF-19500. Devices feature the rugged construction required by demanding industries. Semtech expects to continue expanding its QPL product line in the near future," said Mike Blee, Marketing Manager, Astute Electronics.

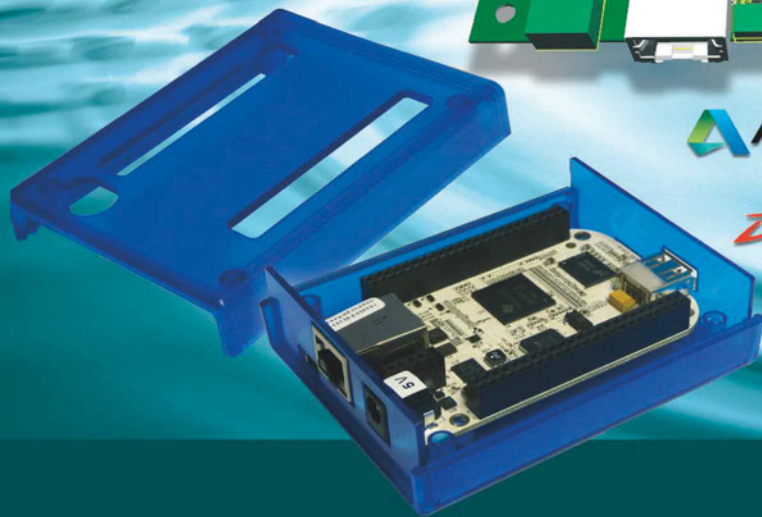
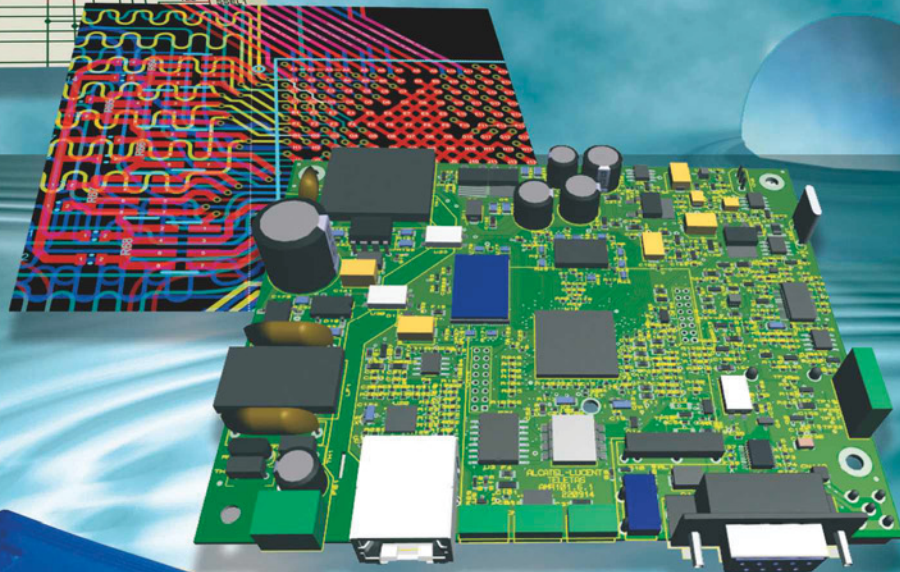
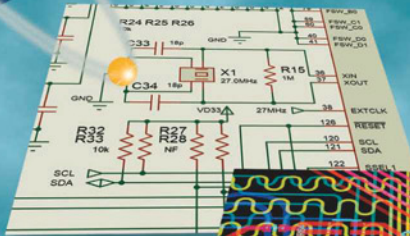
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