May 2016
Volume 122
Issue 1961
£5.60

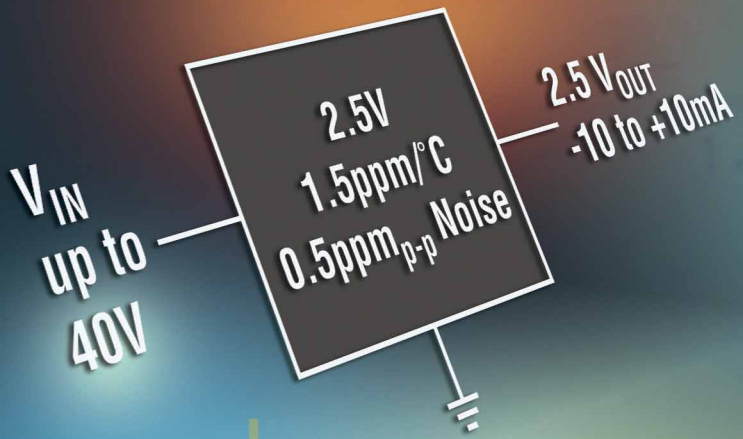
www.electronicsworld.co.uk

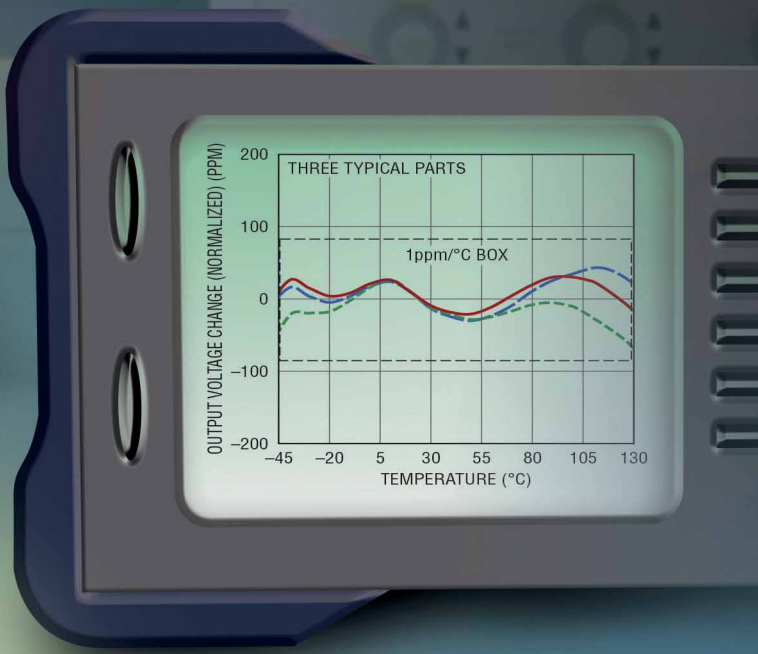
Electronics WORLD

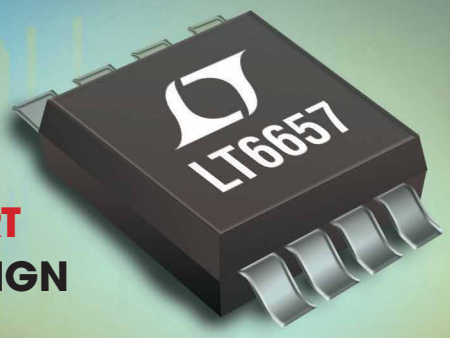
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Solving Data Acquisition Compatibility Problems

with Linear Technology







SPECIAL REPORT

EMBEDDED DESIGN

- Interfaces
- Peripherals
- FPGAs
- Software

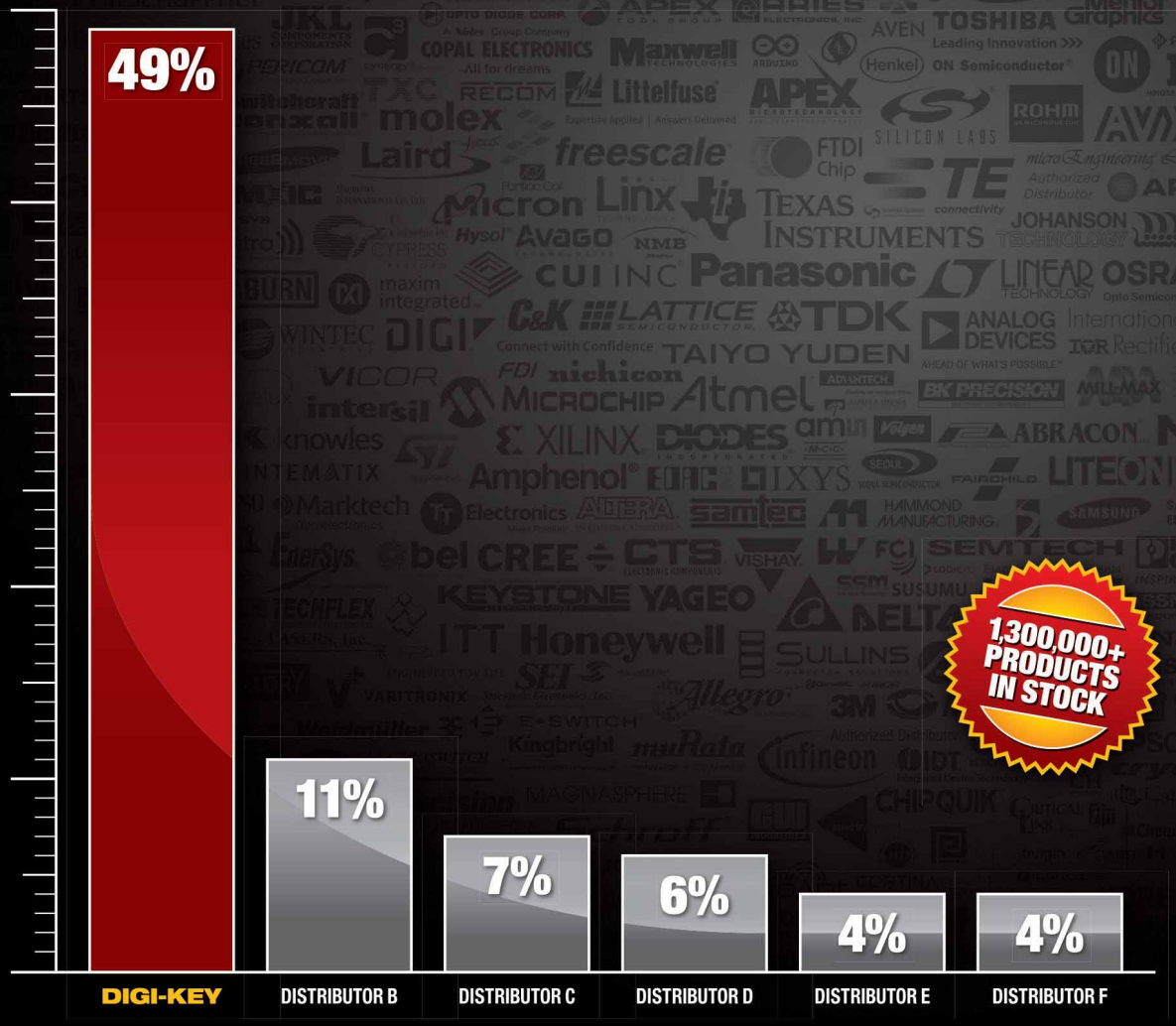
Technology
Newly developed SiC analogue circuit is op-amp-like

Regular column
Integrating pyroelectric sensors in wireless designs

Products
IoT hardware, software and applications

BEST OF CLASS: BROADEST OVERALL PRODUCT SELECTION

Source: AspenCore 2015 Design Engineering and Supplier Interface Study



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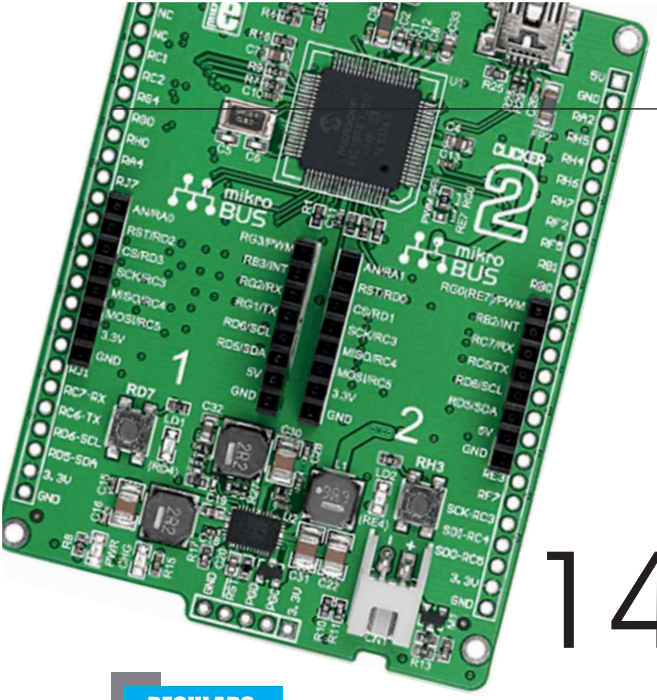

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REGULARS

Cover supplied by LINEAR TECHNOLOGY
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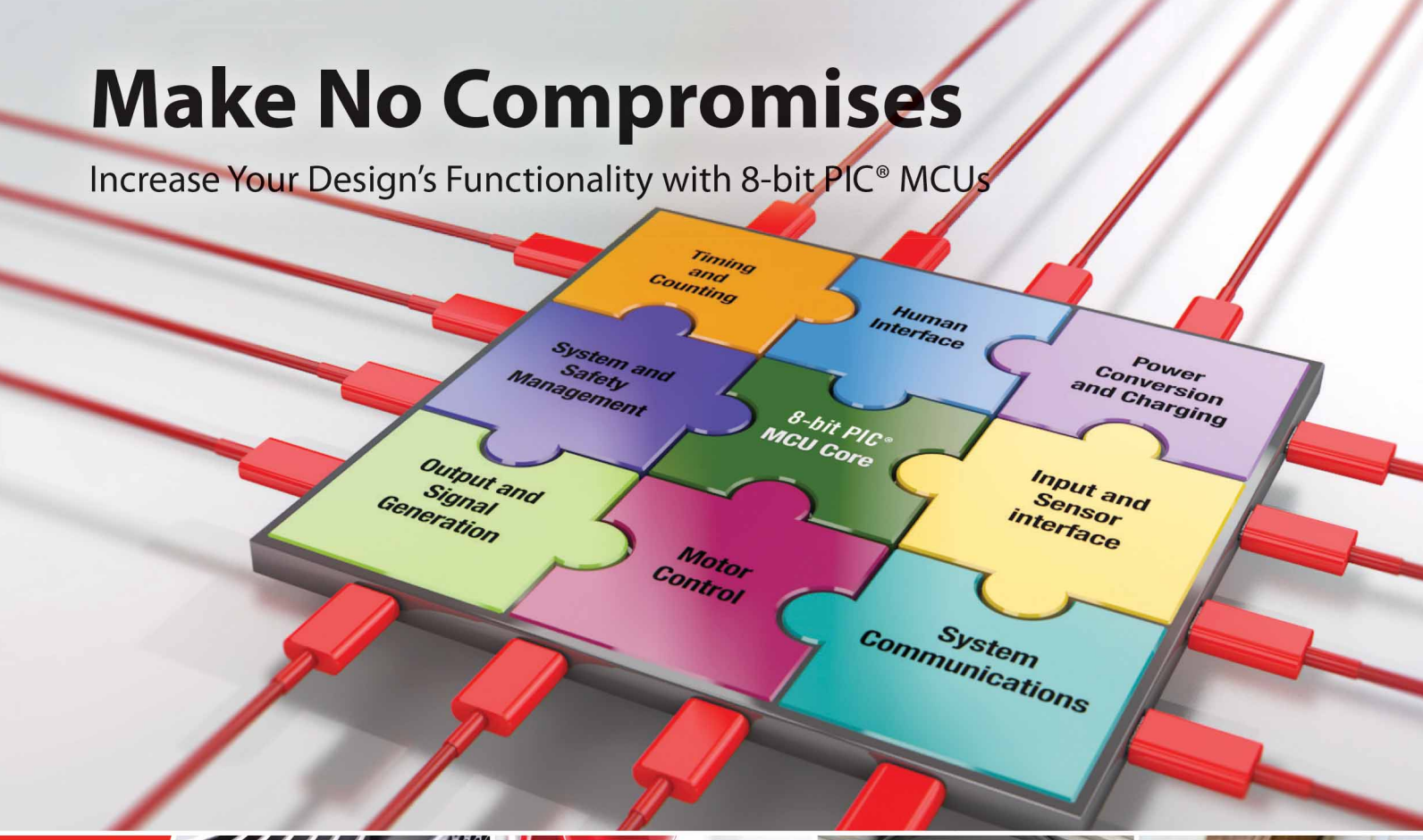

In embedded system design, reality demands that compromises are made at every phase. Tradeoffs between performance, functionality and cost often prevent you from bringing your best ideas to market. We believe there's a better way. That's why we've architected our latest 8-bit PIC® microcontrollers (MCUs) with flexible, "core independent" blocks of hardware intelligence that react quickly, consume very little power and are much more code-efficient than a software-based approach. In essence, Core Independent Peripherals help you easily combine many complex system functions onto a single MCU, increasing speed and flexibility, while reducing power consumption and cost. Design with 8-bit PIC MCUs, and you won't have to compromise.

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TRENDS IN INDOOR WIRELESS FOR ENTERPRISE BUILDINGS

> The next frontier for indoor wireless are the mid- and large-size enterprise buildings – office complexes, high-rise apartments and commercial buildings – which are typically privately owned

Over the last several years, wireless operators have focused on delivering cellular services to the largest public access venues – stadiums, arenas and airports – as there it's all about providing high network capacity to a high concentration of subscribers. In US football stadiums, for example, some operators have deployed distributed antenna systems (DAS) with over 60 sectors for each frequency band. This design delivers plenty of capacity to fans for watching video replays and other data-intensive applications. Future upgrades for adding more capacity and frequency bands will be necessary, but solid foundations for wireless are already in place.

The next frontier for indoor wireless are the mid- and large-size enterprise buildings – office complexes, high-rise apartments and commercial buildings – which are typically privately owned. The challenges of deploying wireless in private venues are significantly different in terms of the customers and channels involved, as well as the technical requirements. The most significant difference is the operators' willingness – or lack thereof – to fund these systems.

The operators recognise they need to invest in wireless for large public venues because their subscribers demand services there. But the return on investment for private enterprises is less certain, so their willingness to fund in-building wireless in private enterprises is not as strong, particularly as they pursue other investments such as new spectrum, acquisitions and network virtualisation.

The enterprises will likely need to invest in equipment themselves. This is a very different model and, overall, there is no consistent process to help enterprises know how to acquire and deploy a system successfully. Even if an enterprise is willing to fund a system, an operator has to provide the radio and backhaul to their network. The process for getting approval differs from one operator to another, making the situation daunting and confusing for many.

This is partly due to private enterprises generally having to deal with IT organisations, not directly with the RF managers from major network operators who are intimately familiar with cellular communications; a significant learning curve stands between these worlds. Enterprises typically have little to no understanding of cellular. They like it no more complicated than Wi-Fi – and, unfortunately, that generally isn't the case. The IT installation companies they know are probably only slightly more knowledgeable about cellular, too.

To remedy this barrier to in-building wireless in the enterprise space, vendors need to provide wireless systems that look and act more like the infrastructure that IT managers know. Many, like CommScope, are doing exactly that. DAS continues to be enhanced to better meet the needs of commercial buildings. Small cells offer a great alternative for cost-effective coverage for enterprises, particularly for single-operator applications with a limited number of frequency bands. Managing interference inside buildings can be challenging, but newer solutions address this issue. The key stakeholders in the enterprise need a bit of a mind-set change, too. Recent research commissioned by CommScope found that just over half (56%) of building managers, facilities managers, real-estate managers and architects consider mobile connectivity for building's tenants as a factor when working on projects. However, almost three quarters (73%) of the same respondents cited it as an 'important' or 'very important' factor.

There is a disconnect here. Building owners and managers have to ensure that tenants are always connected in today's increasingly mobile, data-intensive era, future-proofing the buildings for tomorrow. Better planning for indoor wireless networks, beginning in the earliest design phase, would help ensure adequate wireless coverage and capacity. Deployment in the building construction phase can avoid significant disruption to tenants when systems must be retro-fitted, as well as saving on the associated costs. The sooner architects, building owners and managers start planning for wireless, the easier it is to deliver high-quality, high-bandwidth networks.

This year we expect to see more enterprises start to invest in wireless systems. Early adopters will lead the evolution to a new model where building owners and IT managers take the lead in buying and deploying in-building wireless solutions. DAS and small cells will continue to evolve to support this important market segment. The needs of mobile users in commercial spaces are too great to ignore. The paradigm shift to new funding models and ways of thinking about wireless systems is already underway in North America.

By Matt Melester, Senior Vice President and General Manager for distributed coverage and capacity solutions at CommScope (www.commscope.com)

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DESIGN: Tania King

PUBLISHER: Wayne Darroch

ISSN: 1365-4675

PRINTER: Buxton Press Ltd

SUBSCRIPTIONS:
Subscription rates:
1 year: £65 (UK); £94 (worldwide)
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com
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THE WORLD'S BLACKEST MATERIAL IS NOW AVAILABLE IN SPRAY FORM

Many new applications – including consumer products – can now benefit from the world's blackest surface-coating material called Vantablack, thanks to an innovative new spray-paint version believed to be the blackest ever created.

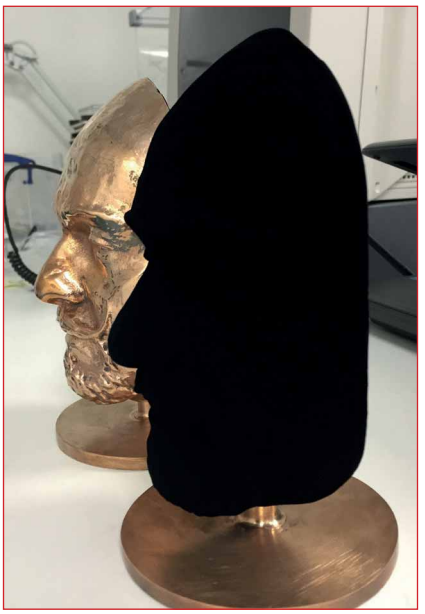
Vantablack's nanomaterial structure absorbs virtually all incident light; it was designed to optimize the performance of precision optical systems. Now, the material's developer, UK-based Surrey NanoSystems, has created a version that can be sprayed on to objects, rather than being grown using a chemical vapour deposition (CVD) process.

The new nanomaterial spray-paint is called Vantablack S-VIS, and it greatly widens the range of applications, making it possible to coat much larger and more complex shapes and structures, as well as many new materials, including engineering polymers.

Even though the material is applied using a simple spraying process, it traps 99.8% of incident light hitting its surface. A surface coated with Vantablack S-VIS looks very odd to the human eye, often described by observers as appearing like a two-dimensional gap or "black hole". The only other commercially available material in the world that is darker is the original Vantablack, which set a world record for blackness when it was launched, as it traps 99.965% of incident light in the visible spectrum.

Vantablack was originally developed for aerospace engineering applications, such as satellite-based optics like star trackers and earth observation imaging and calibration systems. It increases the sensitivity of these optical systems by improving the absorption of stray ultraviolet, visible and infrared light. It is some 17 times less reflective than the current super-black paint used on the Hubble space telescope for minimizing stray light.

The active element of the Vantablack S-VIS spray-paint is a carbon nanotube material. The super-black coating is applied using a patented manufacturing and spray-painting process, combined with pre- and post-spray steps developed to produce extreme levels of absorption.



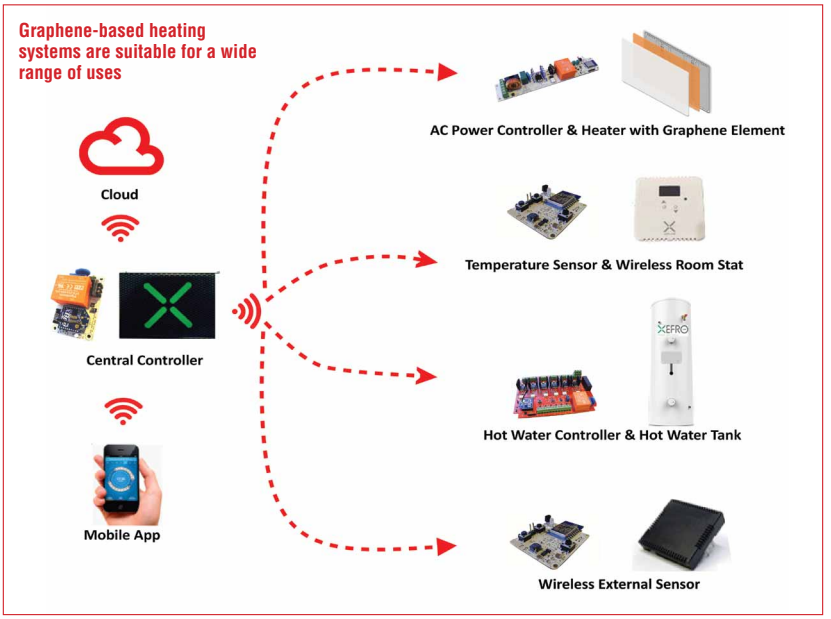
Two 3D masks of a face, one covered in Vantablack S-VIS

WORLDS' FIRST GRAPHENE-BASED COMMERCIAL HEATING SYSTEM IS BEING TRIALLED NOW

UK-based technology firm Xefro is the first to use graphene in a commercial heating system. It harnesses a single-atom-thick material for heating elements that offers extremely efficient energy transfer – 100% of electrical energy is converted into heat, with the potential of reducing energy costs up to 70%.

The Xefro intelligent heating system consists of a central heating controller that communicates via RF signals with hot water controllers and various zones, each consisting of a radiator or at least one heating element with AC power controller and temperature sensors. The user interface for the entire system is via a mobile app.

European Circuits Limited (ECL) will design the hardware and software for the system, as well as manufacture it. The system is currently undergoing trials.



GRAPHENE PROPERTIES

Graphene is suitable for use in heating systems due to several of its properties, including:

- **High surface area – it generates heat extremely efficiently;**
- **Low thermal mass – it offers instant heat, without any waste;**
- **High conductivity, since electrons travel at 1/10 the speed of light.**

FICOSA TRANSFORMS POLICE CARS INTO MOBILE POLICE STATIONS

Barcelona-based high-tech connectivity company Ficosa has created the most advanced police car in the world (right), turning it into a mobile police station.

The patrol car's centre console has been equipped with a 10-inch touchscreen laptop, a 3G/4G Telefónica connection for sending images, video and data in real time, and an automatic license plate reader (ALPR), which digitizes and encodes licence plate images, verifying them with a central database. The vehicle also has three video surveillance cameras located at the front and rear of the car and a cabin camera. An integrated antenna system using fractal technology enhances the vehicle's connectivity.

The Connected Police Car project is a collaboration between Ficosa and Telefónica, and is currently in pilot phase, which consists of several such cars being used throughout Spain. After the trial period, up to 200 high-tech patrol cars are expected to be introduced to the streets of Spain.

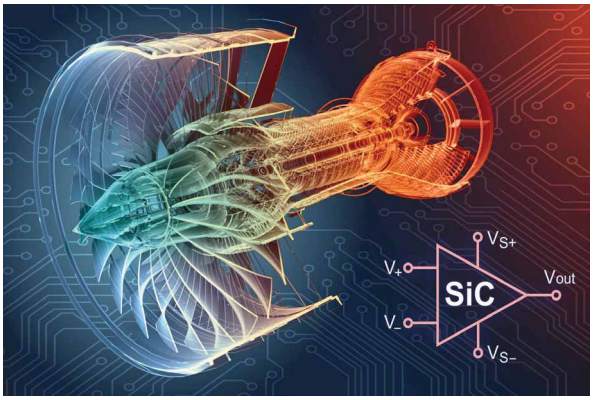
"We have been working on this project for more than three years," said Xavier Pujol, Ficosa's CEO. "The Connected Police Car is an important step in enabling policemen to carry out different procedures without having to be at the police station, as well as offering them new tools to facilitate their work."

INDUSTRY AND ACADEMIA TEAM DEVELOPS SIC-BASED ANALOGUE CIRCUIT

Raytheon UK and Newcastle University have produced silicon-carbide-based (SiC) analogue circuitry with op-amp-like characteristics for high-temperature and harsh-environment monitoring applications

"To date, the focus on silicon carbide semiconductors has been power electronics and exploiting the material's ability to dissipate internally-generated heat," said Dr Alton Horsfall, the Reader in Semiconductor Technology at Newcastle University. "For this project we've focused on creating circuitry that can operate in high temperature and other harsh environments. This could lead to condition-monitoring circuitry mounted on gas turbines or within the primary coolant loop of a nuclear reactor, which runs at about 350°C."

At the heart of the circuit is a lateral small-signal Junction Field Effect Transistor (JFET), which offers a significant improvement in reliability in hostile environments due to a lack of a gate oxide layer. This enables greater stability in the threshold voltage and a reduction in intrinsic noise, making these structures ideally suited for the realization of high-temperature, low-noise amplifier circuits. The current circuit is a fully differential, three-stage amplifier, with a source follower final stage, optimised to operate on a ±15V supply.



New SiC-based analogue circuit

Modifications enable voltage supplies of ±45V for increased headroom of the circuit.

Laboratory tests have shown the amplifier circuit has an open circuit gain of over 1500 at room temperature. A high temperature gain of 200 has been recorded at 400°C, but this is limited by the passive components used in the circuit.

The amplifier was recently monolithically integrated into a single chip.

"We believe this amplifier circuit represents the furthest anyone has gone down the lab-to-fab route. In this instance, it is Newcastle University's design expertise and understanding of harsh environments, combined with our silicon carbide processing expertise, that have the potential to result in the full commercialization of a high-temperature version of a fundamental electronic building block, the humble op-amp," said Phil Burnside, Business Development Manager of Raytheon UK.

SOLVE DATA ACQUISITION COMPATIBILITY PROBLEMS

By Brendan Whelan, Design Manager, Signal Conditioning Products, Linear Technology

Modern data acquisition and signal generation systems are both sophisticated and refined. Decades of IC and application development and generations of designs have optimized performance and features, while broadening both. New designs must differentiate from the prior with well-chosen combinations of performance, size, supply range, stability, and more. Simultaneously, high performance integrated circuits such as DACs, ADCs and voltage references have been pushed to the limit for performance. Concerning the voltage reference, often design choices must be made between precision and features. When highest performance is required, flexibility and compatibility can be lacking.

Historically, the highest precision and most stable systems have been designed using deep buried Zener references, as shown in Figure 1. The combination of low drift, high stability and low noise enables systems with both high dynamic range and good stability. However, Zeners are generally not suitable for most new systems. They require significant supply voltage to operate, and many designs are optimized only for particular systems, such as those with greater than 10V supplies, large available board area, and well-understood load impedance. These assumptions are rarely applicable in many new designs. Furthermore, there has been little new development using Zener architectures, so more commonly used reference voltages less than 5V, such as 4.096V, 2.5V and 1.25V, are rare.

In contrast, bandgap voltage references have long been the best choice for a combination of features and performance. The bandgap architecture, while sacrificing some stability as compared to the Zener architecture, has made it possible to design references with many useful features, including low dropout, wide temperature range, low power, small size, wide operating range and wide load current capability. These features have given rise to a host of high-performance LDO regulators as well as precision voltage references. The relatively low bandgap voltage of approximately 1.2V facilitates the design of products with many output voltages, including 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V and 10V. It also makes it possible to operate from a supply of only a few millivolts above the output voltage, as in Figure 2.

For voltage references, the largest error is usually the temperature coefficient (TC). For many precision systems, a voltage reference with 20ppm/°C temperature coefficient is appropriate. However, over an industrial temperature range (-40°C to 85°C), this temperature coefficient would give a maximum error of 2500ppm, or 0.25%. By comparison, the error due to the initial accuracy (0.1%), thermal hysteresis (usually around 100ppm) and long-term drift (50ppm/√(kHr) is small. While sufficient for many industrial and medical systems, precision applications such as test and measurement, as well as wide temperature range automotive applications, demand better stability.

Over time, bandgap performance has improved, and in some cases exceeded buried Zener stability and noise. New architectures, processes and manufacturing techniques have pushed the limits of precision and stability. Where previous "precision" bandgap references might have boasted 20-50ppm/°C temperature coefficient, newer products provide temperature stability of less than 5ppm/°C. Simultaneously, the range of features has been preserved or improved.

Such is the case for the LT6657, a high precision bandgap voltage reference. The LT6657 provides a new alternative, giving highest precision while retaining significant flexibility for a wide array of system requirements and limitations.

With a temperature coefficient of 1.5ppm/°C, the LT6657 is the lowest temperature coefficient bandgap voltage reference. High-order temperature compensation keeps the output voltage error low and predictable over temperature (Figure 3), while state of the art manufacturing ensures consistent performance from part to part and lot to lot. To ensure that every device meets this high level of performance, the LT6657's temperature coefficient is guaranteed by 100% five-temperature testing. From -40°C to 125°C, the LT6657 guarantees less than 250 parts per million of error due to temperature drift.

It should be noted that a box is included in Figure 3 to indicate 1ppm°C of error. A typical LT6657 unit fits well within this box, allowing for reasonable yield to the 1.5ppm/°C limit in automated production testing.

Adding to the overall stability are low thermal hysteresis and excellent long-term drift stability. These measures predict how well the system will stay within specification over time and temperature cycles. For systems that are located remotely or difficult to calibrate, lower thermal hysteresis and long-term drift translates to fewer calibration events, saving time and expense. While typical values in the electrical table provide helpful guidance, it is never clear if these represent a mean, a deviation, or a single unit. Linear Technology provides substantial data to give meaningful guidance when designing with voltage references. Long-term drift and hysteresis distribution data is available in the LT6657 data sheet showing that both are low and consistent.

Another aspect of voltage reference performance is noise. Many systems are not sensitive to long-term drifts such as temperature or aging, but require very low noise to enable high-resolution measurements. With the LT6657, noise performance is comparable to some of the best low-noise buried Zener references. At only 0.5ppm, the noise is appropriate for many high dynamic range systems. The LT6657 produces only 1.25µV peak-to-peak noise in 0.1Hz to 10Hz for a 2.5V reference voltage. Wideband noise is also low, at 0.8ppm (2µV) RMS to 1 kHz. The low noise of the device makes it a good candidate for high dynamic range and very low noise systems. To illustrate the importance of this low noise, a 20-bit converter with 5V full-scale input has an LSB of only 4.8µV (~1ppm).

In addition to the low temperature drift, high stability and low noise, the LT6657 adds further features. The LT6657 requires only 50mV of headroom for operation. It is possible to power a 2.5V reference from less than 2.6V with no DC load, or less than 3V with a heavy DC load current. The supply range extends to 40V with less than 1ppm/V of line regulation error and excellent ripple rejection, allowing the flexibility to power the reference from almost any

available power supply which is a big differentiator over a Zener reference.

As with most of Linear Technology's recent voltage reference products, the LT6657 exhibits low output impedance over frequency. This reduces the effect of changing load over frequency and helps prevent signals present at the load from backfeeding the reference and causing interference, errors or noise. This feature is critical for reference settling when driving a high performance analog to digital converter (ADC), or surviving operational tests such as bulk current injection in automotive systems. In addition, the LT6657 is designed to drive large output capacitance. Given that many high-performance ADCs draw large charge-injection currents from the voltage reference during sampling, the combination of fast settling and the ability to remain stable by design into a large charge-reservoir capacitor gives this voltage reference an edge in squeezing the best performance from a high dynamic range converter.

The LT6657 also has ample drive capability, and can source and sink up to 10mA of load current, with less than 1ppm per milliamp of load regulation error. This load-driving capability enables the LT6657 to bias a variety of sensors, drive difficult ADC reference inputs, drive multiple ADCs and DACs, or power a small subsystem with reference-grade precision. This little-utilized feature can help a system designer make the most of board area and power dissipation by merging the power and reference functions in some small data acquisition systems. It is ideal when the ADC or DAC uses the same voltage for both power and reference voltages; the small MSOP package of the LT6657 adds to the space-savings. Furthermore, the LT6657 includes current and thermal protection to avoid damage from excessive load during fault conditions.

Finally, the LT6657 can operate as a shunt reference. One benefit of shunt-mode operation is the ability to create a negative voltage reference. Shunt mode operation also allows the LT6657 to work from a very high supply voltage or to operate from the lowest possible dropout voltage. Figure 4 shows a positive shunt configuration for the LT6657.

In conclusion, the LT6657 offers high precision, low noise and high stability, combined with the flexibility provided by its many features. The device's features enable design of a system that is power and area efficient, compatible with a wide range of supply voltages and environmental conditions, and capable of the highest precision, stability and dynamic range. The additional features and performance of this groundbreaking voltage reference, combined with manufacturing quality, make it ideal for many application circuits.

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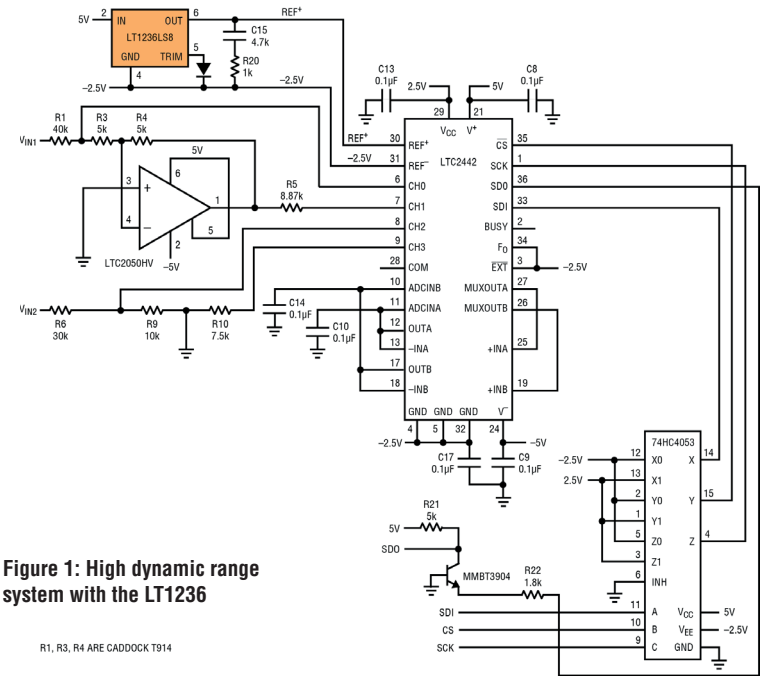


Figure 1: High dynamic range system with the LT1236

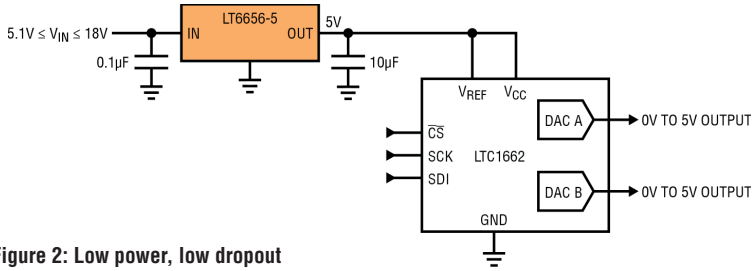


Figure 2: Low power, low dropout voltage reference circuit

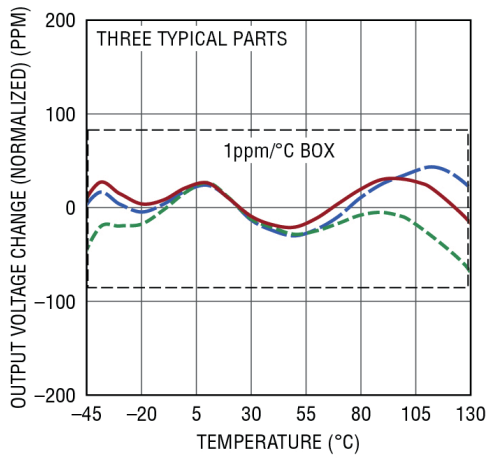


Figure 3: LT6657 temperature drift

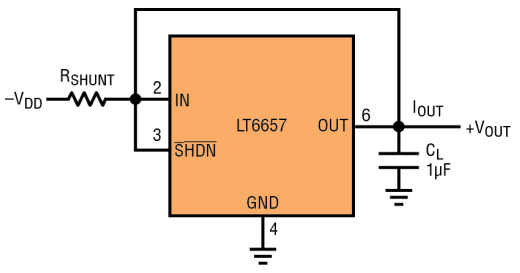


Figure 4: LTC6811 Delta Sigma Converter

Building your own peripherals

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

During the Microchip Masters Conference last summer (held annually in the warmth of Phoenix, Arizona), my seven-year-old son Luca and I participated in a father/son event. It was great to work together on a project, developing a simple talking robot – not much more than a PIC board in a cardboard box and a servo to move the lid. We called it the "Cookie Monster" (see Figure 1). Luca was a bit too young to contribute to the coding part but he provided the key inspiration, recorded the voice of the monster, did an accurate drawing of the assembly and wiring, and decorated it in true *'Sesame Street'* style.

It was impressive to see how much excitement a single moving part – the servo – could generate! Luca went on for hours telling everybody about the little monster and making practical demonstrations – eating 'cookies' and even fingers too, in case of slow reflexes.

So, thinking about next year, I figured it could be even more fun teaching an eight-year-old how to build a new robot using two, three, four or even eight or more servos.

I quickly realized though that beside the cost (local shops sell micro servos, like the one we used for the cookie monster, for less than 5 Euros), a limiting factor could be the number of servo channels available on a low-cost PIC microcontroller. In particular, I was planning to again use the MPLAB Xpress cloud IDE so the project could easily be replicated by other father-and-son teams in minutes, without lengthy and complex software installations.

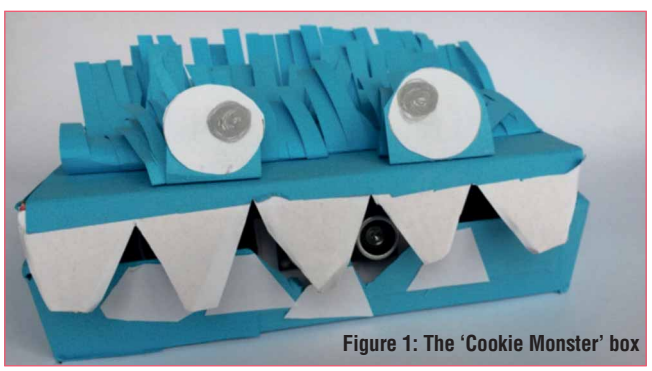


Figure 1: The 'Cookie Monster' box

The MPLAB Xpress evaluation board (see Figure 2) featuring a PIC16F18855, a 28-pin device loaded with many core independent peripherals, looked like a promising replacement for the previous year's 20-pin prototype.

Servo Control

In practice, controlling a servo is as simple as generating a PWM signal where the period can be anything between 4ms and 20ms, but it is the T_{on} time that controls the actual position of the servo actuator; a centre position is usually achieved with T_{on} of 1.5ms. Increasing the duration up to 2.5ms will produce a rotation of the actuator up to 90 degrees (clockwise), while decreasing it to 0.5ms will produce an opposite (anti-clockwise) 90-degree rotation. Controlling multiple servos then requires just an equal number of PWM modules, all linked to a single timer providing the common period.

The PIC16F18855 has only five Capture Compare and PWM modules (CCP1 through CCP5), I used the PWM function.

There are two more PWM proper modules (PWM6 and PWM7); I am not sure if the odd number was intentionally chosen by the device architect to tease, but it sure felt like a challenge.

Home-Made PWM

One can nowadays find an endless list of examples online illustrating how to produce the servo PWM timing in software by "bit banging" an I/O pin using a timer (optionally an interrupt) and a lot of CPU cycles. But while I will confess doing that in the past, it did feel like a huge waste of the microcontroller resources. Besides, since I was planning to implement a few extra functions (ultrasonic range detection, audio playback, etc.), bit-banging would definitely not be the way to go. It was time to put the core independent peripherals of the PIC16F18855 to work! After all, some of the timers on the device (the even numbered ones) have been enhanced with so-called HLT capabilities. Despite the cryptic acronym – HLT stands for Hardware Limit Timer (as if that made it any clearer) – these new timers can operate automatically as monostable circuits. Instead of simply generating an interrupt as the (8-bit) timer matches the period register value, they can

produce an output signal that can be routed directly to a pin or other internal logic. They can also re-arm automatically in sync with other timers via a (re-)trigger input.

To complete a new PWM module then, all we need is a single flip-flop, a Set Reset or SR-Latch to be precise. Luckily, this is a function already found in the Configurable Logic Cells, of which the PIC16F18855 has no less than four.

Figure 3 illustrates how the three elements: Timer2, HLT (aka Timer4) and the SR-latch combine to form a new PWM module.

Quick Configuration With MCC

Creating a new project using the MPLAB Xpress IDE takes seconds and is as easy as opening a browser, entering the MPLAB Xpress URL: https://mplabxpress.microchipcom and logging in to your own MyMicrochip account.

Thanks to the MPLAB Code Configurator, populating the project with the correct initialization code for the device and all the required peripheral drivers is a matter of minutes and a few mouse clicks. Here's the procedure, step by step:

- Select the System Module configuration.
- Accept the default configuration: 4MHz, internal clock.
- Add sequentially all the CCP and PWM modules to the project resources.
- Add Timer2 and Timer4 to the project resources.
- Add CLC1 to the project resources.
- Configure Timer 2 as the time base for all servo PWMs. This requires selecting the 'Roll Over Pulse' mode and using FOSC/4 as the clock input (see Figure 6).
- Configure Timer4 as a monostable. This requires selecting the monostable mode, selecting the Timer2_postscaled trigger input and start on rising edge (of the trigger) as the start/stop option (see Figure 7).
- Configure all CCP modules to operate as PWMs with Timer2 as the time base.
- Configure all PWM modules to use Timer2 as the time base.
- Configure CLC1 as the SR-Latch and connect the first and the third input gate multiplexers respectively to the Timer2 output and Timer4 output (see Figure 8).
- Select the Pin Manager configuration table and assign all output pins as you see fit. Note that the new PWM will be the output function of CLC1 (see Figures 4 and 5).

The PIC16F18855 has PPS (peripheral pin select), so there's plenty of flexibility on where to connect each servo output function. You can use the mikroBUS connector or simply the external ring of contacts of the MPLAB Xpress evaluation board.

Eventually I decided to add a serial port connection so I could conveniently control all eight servo/PWM outputs from a terminal program. For that you will need to:

- Add the EUSART module to the project resources list.
- Select to the preferred baud-rate for your application (9,600 baud is a good default) and enable the 'continuous receive' function (add the transmit function if you want to receive feedback from the board as well).
- Enable the 'STDIO redirection to the USART' to be able to use the standard C library I/O functions (printf, putch, getch).

With the "Generate" button, the MPLAB Code Configurator will produce the configuration files and place them in the project sources. We are now ready to start focusing on the core of the application.

In 10 Lines Of Code

The MCC-generated drivers provide the PWMx_DutyValueSet() function to control the duty cycle (T_{on} duration) of the CCP modules.

Please note that, as of this writing, MCC rev 3.03 uses a different function-naming convention for the PWM modules, using the PWMx_LoadDutyValue() instead.

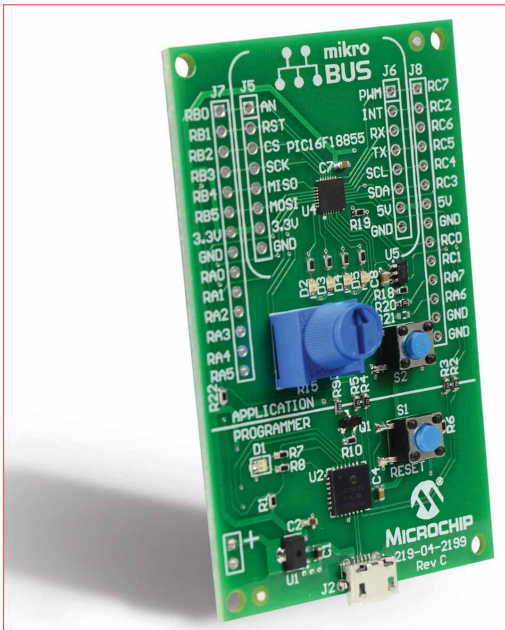


Figure 2: MPLAB Xpress Evaluation board

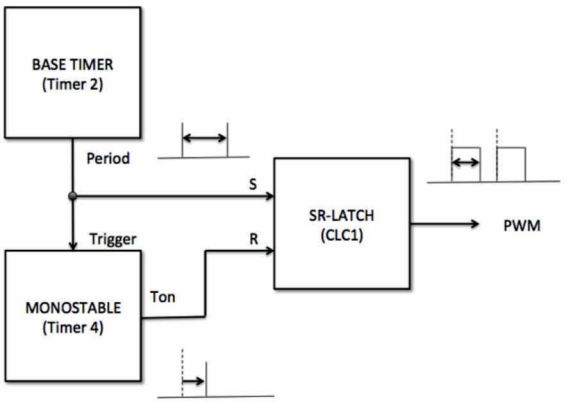
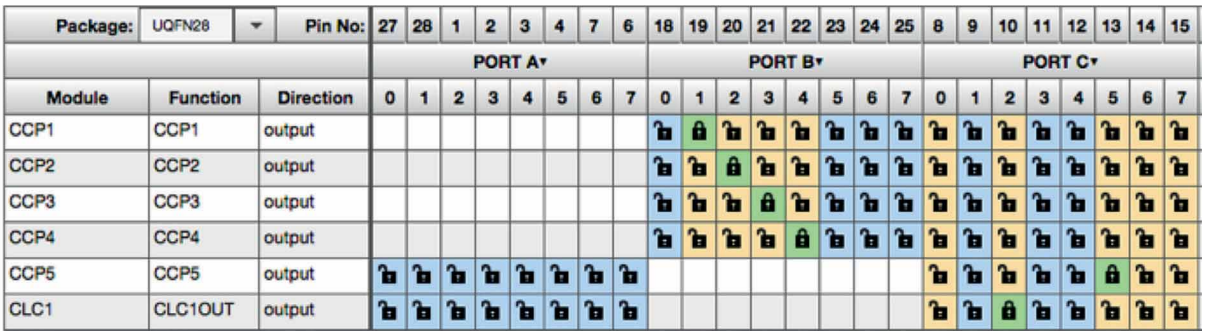
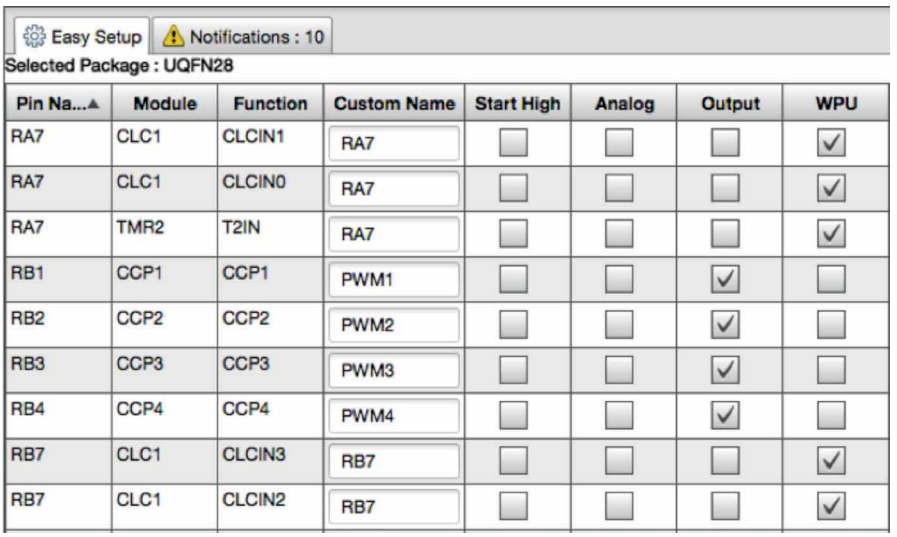


Figure 3: Servo – PWM construction



Package: UQFN28	Pin No:	27	28	1	2	3	4	7	6	18	19	20	21	22	23	24	25	8	9	10	11	12	13	14	15
		PORT A								PORT B								PORT C							
Module	Function	Direction	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
CCP1	CCP1	output																								
CCP2	CCP2	output																								
CCP3	CCP3	output																								
CCP4	CCP4	output																								
CCP5	CCP5	output																								
CLC1	CLC1OUT	output																								

Figure 4: MCC pin manager



Easy Setup | Notifications : 10

Selected Package : UQFN28

Pin Na...	Module	Function	Custom Name	Start High	Analog	Output	WPU
RA7	CLC1	CLCIN1	RA7	☐	☐	☐	☑
RA7	CLC1	CLCIN0	RA7	☐	☐	☐	☑
RA7	TMR2	T2IN	RA7	☐	☐	☐	☑
RB1	CCP1	CCP1	PWM1	☐	☐	☑	☐
RB2	CCP2	CCP2	PWM2	☐	☐	☑	☐
RB3	CCP3	CCP3	PWM3	☐	☐	☑	☐
RB4	CCP4	CCP4	PWM4	☐	☐	☑	☐
RB7	CLC1	CLCIN3	RB7	☐	☐	☐	☑
RB7	CLC1	CLCIN2	RB7	☐	☐	☐	☑

Figure 5: Pin module configuration

Eventually, our eighth PWM will be controlled via the Timer4 period register, accessible via the TMR4_LoadPeriodRegister() function.

Since the original PWM functions assume a 10-bit input value, while the Timer4 period is only an 8-bit value, we can achieve an identical control function by simply shifting left by two positions the same control value as shown in Listing 1.

```
#include “mcc_generated_files/mcc.h”

void main(void)
{
 uint8_t i, duty[8];

 SYSTEM_Initialize();

 while (1) // main loop
 {
 if (getch() != ‘\02’) // start of text
 continue;
 for (i=0; i<8; i++)
 duty[i] = getch();
 // values from 32 to 156 correspond to 0 to 180deg

 if (getch() == ‘\03’) { // end of text
 putch(‘\06’); // ack
 PWM1_DutyValueSet(duty[0]<<2);
 PWM2_DutyValueSet(duty[1]<<2);
 PWM3_DutyValueSet(duty[2]<<2);
 PWM4_DutyValueSet(duty[3]<<2);
 PWM5_DutyValueSet(duty[4]<<2);
 PWM6_LoadDutyValue(duty[5]<<2);
 PWM7_LoadDutyValue(duty[6]<<2);
 TMR4_LoadPeriodRegister(duty[7]);
 }
 }
}}
```

Listing 1: Displaying the pattern for digit ‘1’ side by side

As you can see from the top of the main loop, I have opted for implementing a very (very!) simple serial communication protocol with the MPLAB Xpress board. A 'Start of Text' (ASCII 0x02 or CTRL-B) character is used to prefix a string of eight characters, interpreted directly as T_{on} values. A space (ASCII 0x20) will correspond to a maximum-left position. Upper-case alphabetical characters will produce increasingly larger rotations to the right. Lower-case alphabetical characters will rotate even farther to the right and so on. An 'End of Text' (ASCII 0x03 or CTRL-C) character is expected to terminate the string that is eventually acknowledged sending back the Ack (ASCII 0x06 or CTRL-F) value.

Build the project and program the MPLAB Xpress evaluation board using the 'Make and Program' button from the MPLAB Xpress IDE toolbar.

If all's well, you'd be able to immediately verify the presence of a default 50%-duty-cycle PWM signal on each chosen output pin. Any connected servo will position itself to a mid-right position.

By connecting a terminal to the MPLAB Xpress virtual communication port and playing with the command strings you can test the effectiveness of all eight modules.

For example, enter the following string on your terminal:

CTRL-B A B C D E F G H CTRL_C

The Xpress board with reply with:

CTRL-F

This should position all eight servos at slightly increasing angles (1.4-degrees apart), starting from approximately 45 degrees from the left-most position.

In Closing

Adding an eighth PWM module is quite simple. The question then becomes: where is the limit? Can we do nine, ten, perhaps twelve PWMs?

I'll leave you with this challenge in the assumption that you will try to use the many more timers (2x SMT, 2x HLT, NCO...) and configurable logic cells available to create even more interesting core-independent solutions.

The new PWM module we just assembled has the right resolution and uses no additional CPU cycles, leaving all the processing power of the PIC core available for other tasks the little robot will need to perform this summer.

Stay tuned. ●

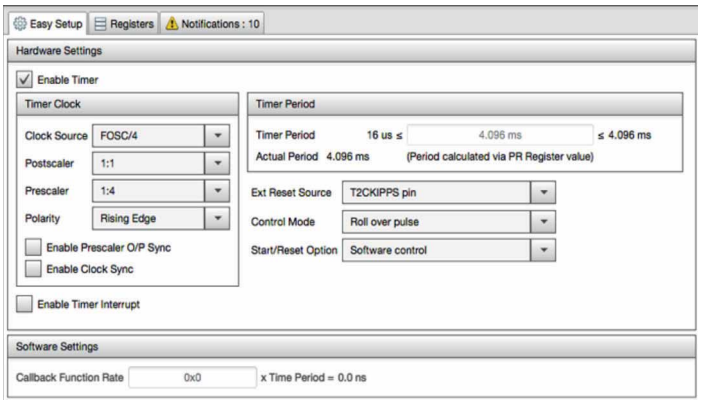


Figure 6: Timer2 configuration

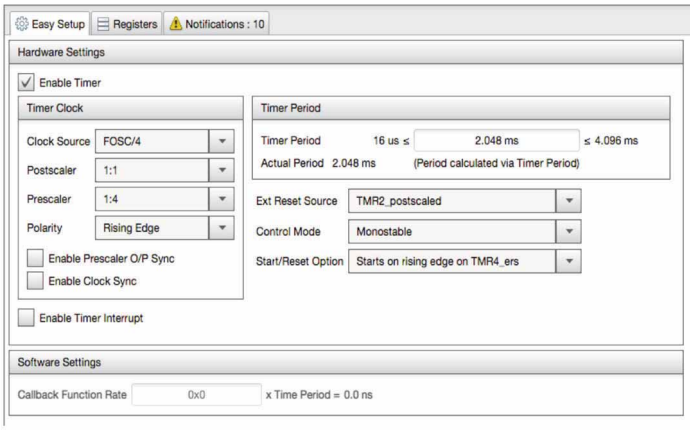


Figure 7: Timer4 configuration

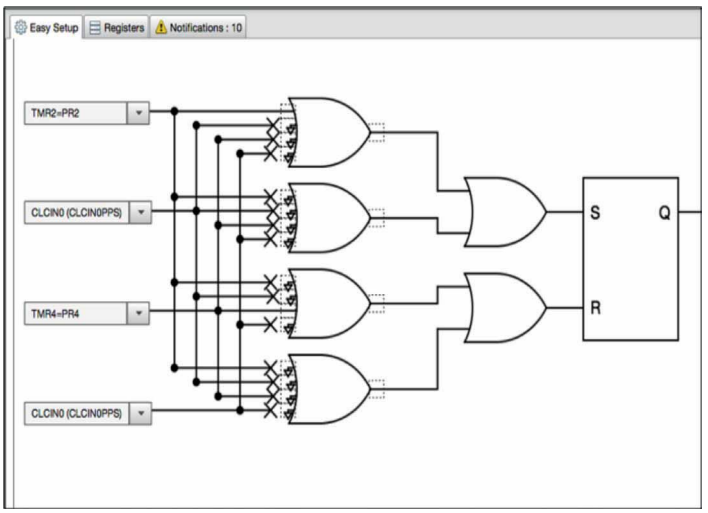


Figure 8: CLC1 configuration

Using pyroelectric sensors in embedded applications

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

Pyroelectric sensors are also known as 'passive infrared' sensors – PIR for short, or presence detectors; they detect thermal radiation.

Infrared radiation has wavelengths longer than visible light but shorter than microwaves. When objects generate heat they also generate infrared radiation. Although this radiation cannot be seen, it can be detected easily using transducers to convert the infrared signal to detectable voltage. Humans emit infrared radiation at a wavelength of 10μm at normal body temperature.

Pyroelectric Detectors

Pyroelectric is not same as thermoelectric. In a thermoelectric device (e.g. a thermocouple), voltage is generated at a junction of dissimilar metals at different temperatures. In a pyroelectric device a surface charge is generated when the device is exposed to infrared radiation; the amount of charge depends on the amount of radiation hitting the device surface. In short, whenever there is a change in infrared radiation striking the detector, there is a voltage generated at the detector terminals.

Pyroelectric detectors will only respond to changes in incoming radiation levels. These detectors are capable of sensing IR sources, their size, temperature, direction of motion, speed of movement, wavelength and emissivity.

A pyroelectric detector is made of infrared sensitive crystalline material such as lithium tantalite deposited on both faces of the detector; it's easy to think of the pyroelectric detector as a flat-plate capacitor. In practical detectors an FET is used as a buffer, and a shunt resistor is used to convert the FET current to output voltage, which is then amplified to useful levels. In addition, since the detector is sensitive to wide range of radiation, a filter window is added to make the detector more sensitive to human detection.

In practise, dual- or quad-element detectors are used to detect the direction of movement and also eliminate environmental noise and thus increase the sensitivity. In a two-element detector both elements detect the same amount of IR from the walls, doors, etc. When the body of a person or animal passes by, one element detects this and causes a positive differential change. When the person leaves, the reverse happens, resulting in a negative differential change. Additionally, a plastic plano-convex Fresnel lens is added to the front of the PIR detector, with its focal length chosen to increase the sensitivity to human body radiation (8-14μm, strongest at 9.4μm). The Fresnel lens provides a wider field of view to the sensor.

Figure 1 shows the internal structure of a typical pyroelectric detector housed in a metal can.

In addition to tracking movements of people and animals, some other common application areas for PIR detectors include automatic building light and door control, flame detection, thermal imaging, infrared-based missile guidance systems, medical applications, industrial control for heat leakages, gas detection and pollution monitoring and IP cameras.

Advantages And Disadvantages

Pyroelectric detectors have traditionally been sensitive to ambient light reflections, such as those from bright-coloured objects and strong ambient light sources (direct sunlight, for example).

In general, the advantages and disadvantages of these detectors can be summarized as follows:

Advantages

- Low power consumption;
- Low cost;
- Small size;
- Easy to set up and use;
- Compatible to microcontroller interfacing;
- Easy human or animal detection.

Disadvantages

- Sensitive to strong ambient light;
- Sensitive to unwanted sources of thermal radiation;

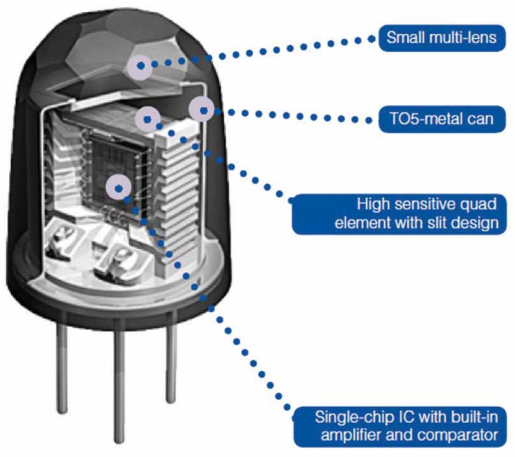


Figure 1: Internal structure of a typical pyroelectric detector

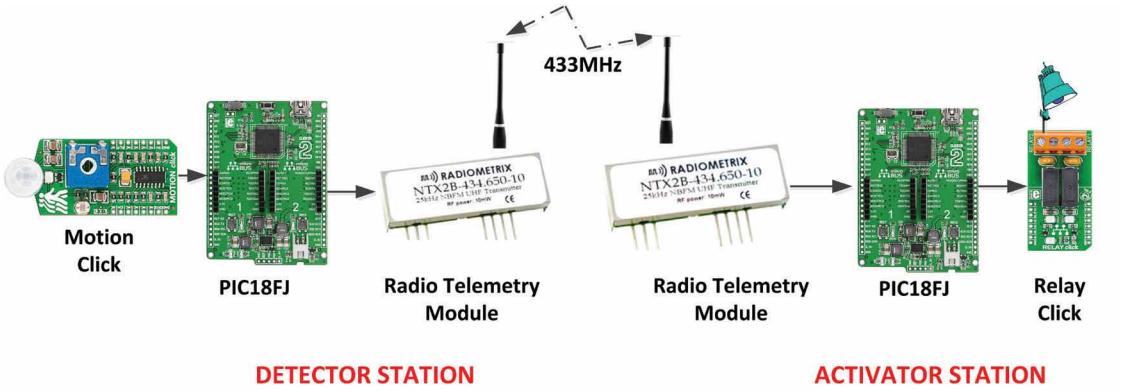


Figure 2: Block diagram of the example system

- Short detection range;
- Insensitive to stationary objects;
- Narrow sensor field of view.

Microcontroller-Based Example

A microcontroller-based wireless pyroelectric detector system is easily designed using standard off-the-shelf components. In this application the system detects the presence of someone in a room and sends signals to a remote station to activate the lights in that room for a pre-set time, using a relay. After this time the lights automatically turn off.

As shown in Figure 2, the system has two parts: detector station and activator station. At the detector station there is a small PIR detector board with its output fed to a microcontroller development board. An RF transmitter module then receives commands from the microcontroller and sends them to the receiver at the activator station. There's another microcontroller development board at this station that is connected to lights in a room. Once a movement is detected inside the room, upon receiving a command, the lights turn on for two minutes. After this time they turn off automatically, ready for the next activation.

In other applications the lights can be replaced by other devices, such as alarm generators for example.

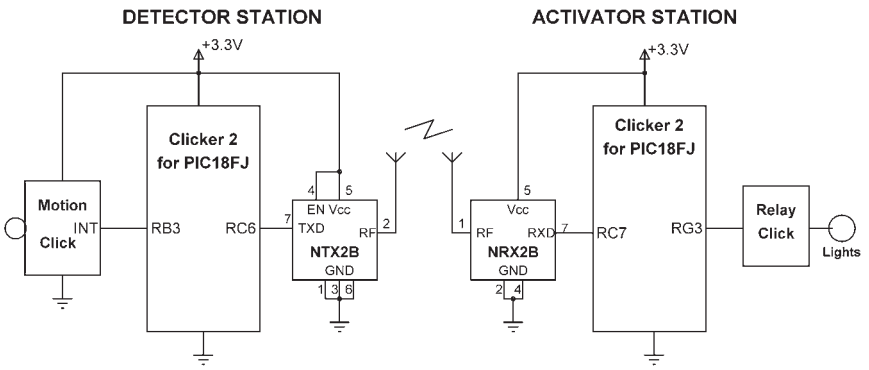


Figure 3: System circuit diagram

The Hardware

Figure 3 shows the system's circuit diagram. A Motion Click board from mikroElektronika is used as a PIR detector. This board carries a PIR500B pyrometer sensor and a BISS0001 IC that generates a logic pulse when exposed to infrared light. The duration of this pulse can be set by external resistor and capacitor pair.

The maximum range of the sensor is up to four metres, although an on-board potentiometer can be used to adjust the detection range (some industrial sensors have ranges over 10m). In this example, the output of the Motion Click board (INT) is connected to pin RB3 of the development board.

Any type of microcontroller can be used in this design since the processing speed, memory requirements or I/O pin numbers are not limiting factors. In this design, a Clicker 2 for PIC18FJ (Figure 4) type microcontroller development board (based on the PIC18F87J50 microcontroller operating at 8MHz) is used, with the Motion Click board plugged-in to mikroBUS socket 1 on the detector side. On the activator side, a Relay Click board is connected to mikroBUS socket 1 of a similar development board. The output of the development board (RG3) is connected to the Relay Click board. The lights to be controlled are connected to the relay terminals. The click boards are powered from the development boards.

The NTX2B transmitter (Figure 5) and compatible NRX2B receiver (Figure 6) modules are also used in this design.

Readers should note that other communications technologies such as Wi-Fi, Bluetooth, ZigBee, etc, can also be used in wireless pyroelectric projects. The choice depends on factors such as cost, reliability, security and ease of use.

The Software

The software in this example is based on the mikroC Pro for PIC language. Figure 7 shows detector station operation as a program description language. Here, after configuring the input-output ports, the motion sensor is enabled and the program enters a loop, inside which the output voltage of the PIR detector is checked

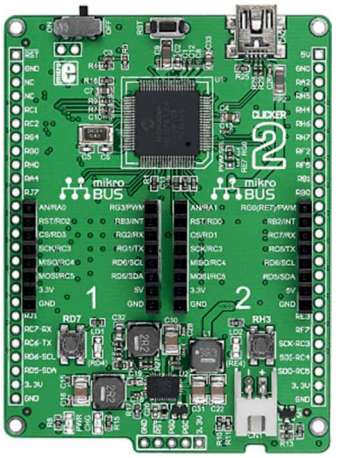


Figure 4: Clicker 2 for PIC18FJ development board

Figure 5: NTX2B transmitter module

Figure 6: NRX2B receiver module

```
BEGIN
        Configure I/O ports
        Enable motion sensor
        DO FOREVER
        IF PIR output at logic 1 THEN
                Send 1 to transmitter module
                ELSE
                Send 0 to transmitter module
                ENDIF
        ENDDO
END
```

Figure 7: Transmitter program

```
BEGIN
        Configure I/O ports
        DO FOREVER
                De-activate the relay
                Read receiver module
                IF 1 received THEN
                        Activate the relay
                        Wait 2 minutes
                        De-activate the relay
                ENDIF
        ENDDO
END
```

Figure 8: Receiver program

and a signal sent to the transmitter module if a movement is detected. This process is repeated continuously.

The operation and transmitter programs are similar; see Figure 8. The input-output ports are configured at the beginning of the program. The main program loop is executed endlessly, inside of which the output of the receiver module is checked and the relay activated if a valid command is received from the transmitter module. The relay stays energised for two minutes. After this time, the relay automatically releases so the system is ready for the next activation.

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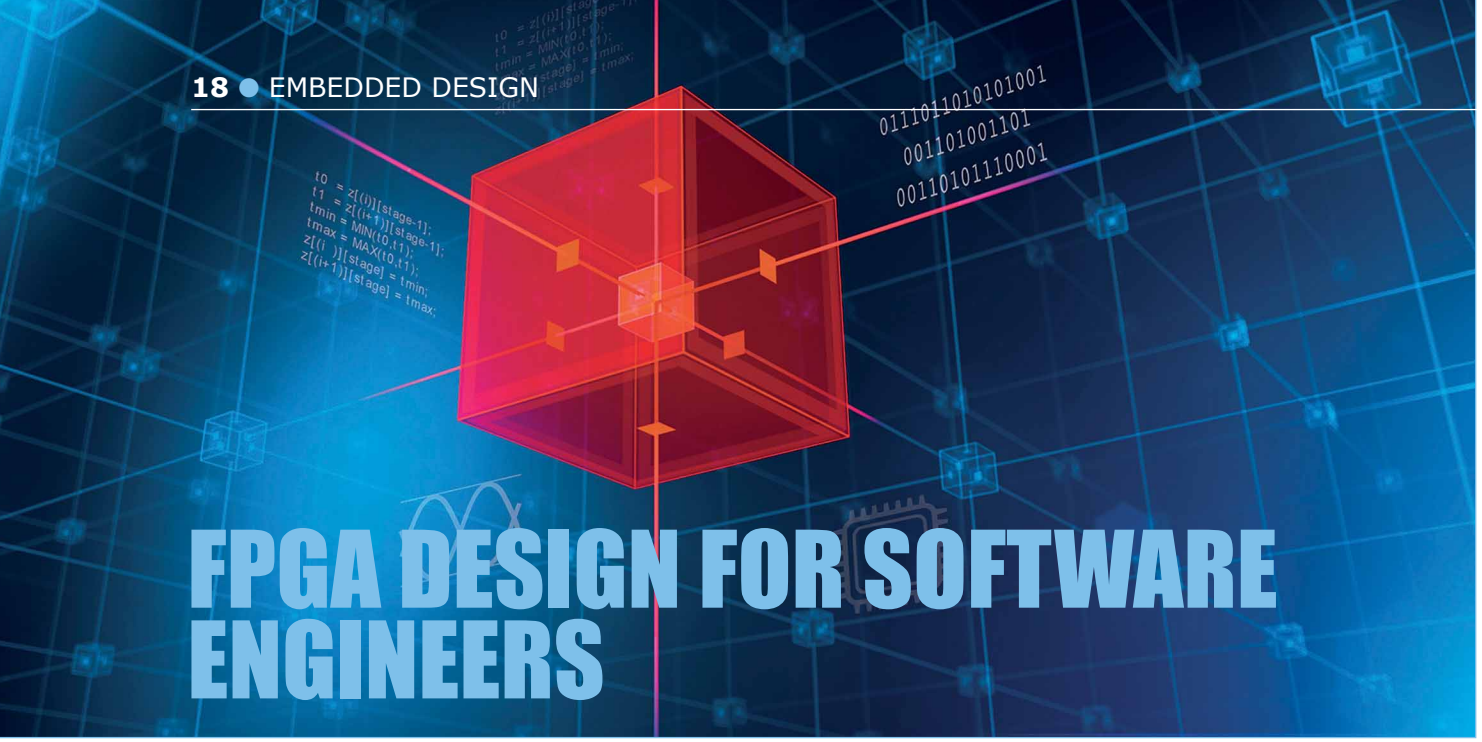


FPGA DESIGN FOR SOFTWARE ENGINEERS

NEW FPGA DESIGN METHODOLOGY ALLOWS SOFTWARE ENGINEERS TO BUILD HIGH-PERFORMANCE COMPUTING ENGINES, USING FAMILIAR TOOLS AND TECHNIQUES. BY **STEPHANE MONBOISSET**, MARKETING AND BUSINESS DEVELOPMENT DIRECTOR AT PLDA GROUP

Booming demand for data services in cloud-based storage and analytics is driving computing loads that are beyond the capabilities of conventional CPUs. Current CPUs' limited capacity for parallelisation means having to add extra processors and more virtual machines, driving costs and power consumption to unacceptable levels. However, data-centre equipment manufacturers already know that massive parallelism is possible with field programmable gate arrays (FPGAs), which will help achieve the processing performance and I/O bandwidth needed to keep pace with such demands and within a highly efficient power budget. Traditionally, however, implementing a hardware computing platform in an FPGA has been a complex challenge.

> Traditionally, implementing a hardware computing platform in an FPGA has been a complex challenge

Moving On To Software

Although some recent FPGA-design methodologies incorporating High-Level Synthesis (HLS) tools and software programming languages such as OpenCL, C and C++ have simplified the task, they have not eliminated the need for specialist FPGA-design expertise. There is need for high-level workflow that enables software engineers to use the FPGA as a software-defined computing platform, without the pain of hardware design. Hence, such a workflow should be able to:

1. Create functional hardware from pure software code;
2. Incorporate existing hardware IP blocks if needed;
3. Infer and create all of the support hardware (interfaces, control, clocks, etc.);
4. Support the use of commercial, off-the-shelf (COTS) boards and custom platforms;
5. Eliminate hardware debug by ensuring the generated hardware is correct;
6. Support debug of functional blocks using standard software debug tools only.

Consider a software algorithm comprising two basic functions: data is processed into one function and then sent to another for further processing. From a software perspective, this implementation is as simple as a call to Function1(), followed by a separate call to Function2() using pointers to the location of the data to be processed.

Implementing such an algorithm on an FPGA-based hardware platform without the right hardware abstraction tool flow would require the software developer to come up with a hardware design resembling that in Figure 2, where Kernel 1 and Kernel 2 are the respective hardware implementations of Function 1 and Function 2.

The hardware design would need to include both control and data planes. The control plane is the execution engine that generates clocks and resets, manages system startup, orchestrates data plane operations and performs housekeeping functions. The data plane instantiates and connects the processing elements, Kernel 1 and Kernel 2, as well as the necessary I/O interfaces required to read data in and write processed data out. In the example shown in Figure 2, those interfaces are Ethernet and PCI Express (PCIe).

Figure 1: Functions to be performed on data

Familiar Challenges

A software developer without specific hardware expertise could generate Kernel 1 and Kernel 2, using a high-level synthesis tool such as Xilinx's Vivado HLS to compile the software functions Function1() and Function2() as written in C or C++ into FPGA hardware descriptions in VHDL or Verilog. However, the non-algorithmic elements of the design, such as interfaces, control, clocks and resets cannot be generated with HLS tools. Hardware designers would need to create these as custom hardware description language functions or IP. The job of sourcing those elements and connecting them poses yet another challenge, as some elements may not be readily available or may have different types or sizes of interface, as well as different clocking requirements, specific startup sequences and so on.

Implementing the design presents equally tough challenges. These include mapping the design onto the resources of the selected FPGA platform, generating the appropriate constraints and confirming that those constraints are met after logic synthesis and implementation on the FPGA hardware. An experienced hardware designer has been known to take weeks to achieve even the simplest design of a new piece of FPGA hardware.

New Approach

PLDA Group, a developer of embedded IP, has created QuickPlay to allow software developers to accomplish these tasks and, hence, implement applications intended for CPUs, partially or fully, on FPGA hardware. In this software-centric methodology, the designer first develops a C/C++ functional model of the hardware engine and then verifies the functional model with standard C/C++ debug tools. The target FPGA platform and I/O interfaces (PCIe, Ethernet, DDR, QDR, etc.) are then specified and the hardware engine compiled and built.

For this process to work seamlessly, the generated hardware engine must be guaranteed to function identically to the original software model. This means the model must be deterministic, in order to yield the same results as the hardware, however fast that hardware implementation may run. Unfortunately, most parallel systems suffer from non-deterministic execution. Multithreaded software execution, for example, depends on the CPU, on the OS and on unrelated processes running on the same host. Multiple runs of the same multithreaded program can have different behaviours.

Such non-determinism in hardware would require debugging the hardware engine itself, at the electrical waveform level. This would defeat the purpose of a tool aimed at software developers, but QuickPlay's dataflow model guarantees deterministic execution regardless of the execution engine. The model consists of concurrent functions, called kernels, communicating with streaming channels, which correlates well with how a software developer might sketch an application on a whiteboard. The contents of any kernel can be arbitrary C/C++ code, third-party IP, or even HDL code.

The QuickPlay design flow is straightforward as shown in Figure 3.

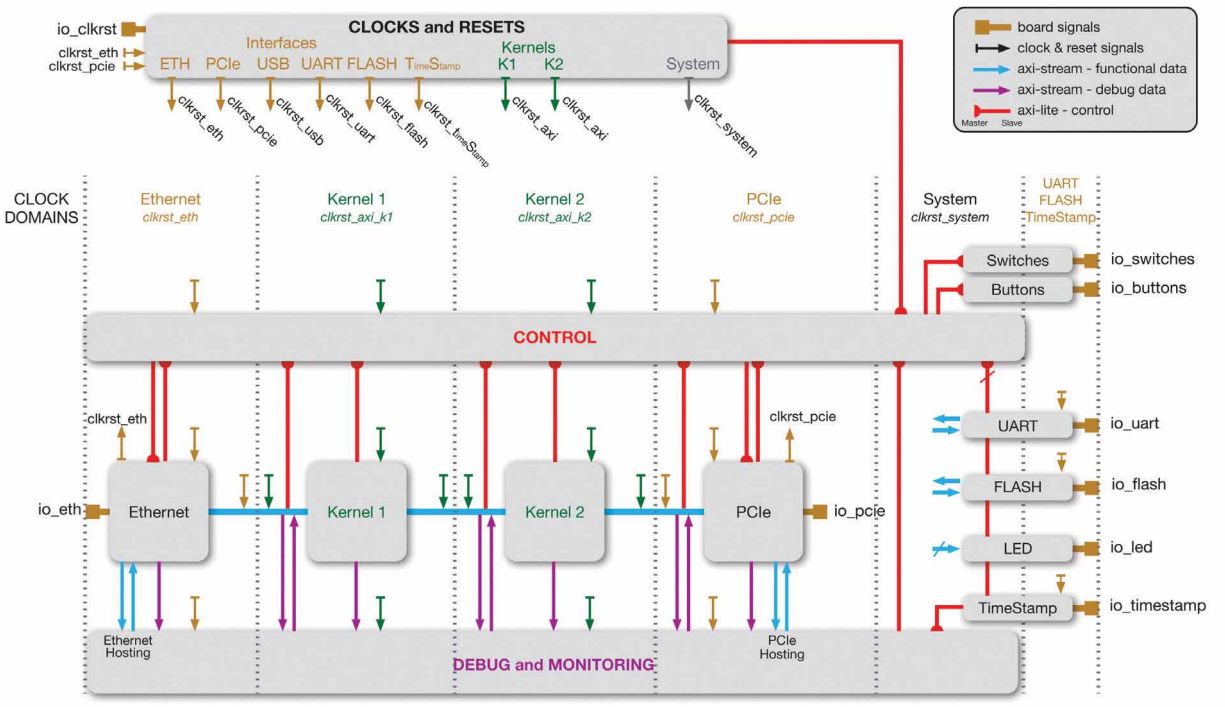


Figure 2: Detailed hardware implementation of a two-function algorithm using traditional FPGA tools

The Design Flow

1. **Stage 1:** Pure software design. The FPGA design is created by adding and connecting kernels in C and specifying the communication channels, using the host development software. The QuickPlay IDE provides a C/C++ library and API to create kernels, streams, streaming ports and memory ports, and to read and write to and from streaming ports and memory ports.
2. **Stage 2:** Functional verification ensures that the software model works correctly. The model is compiled on the desktop and executed with a test program that sends data to the inputs, verifying the correctness of the outputs.
3. **Stage 3:** The FPGA hardware is then generated from the software model. At this stage the target FPGA, and also the physical interfaces and protocols to map to the design input and output ports, are selected using simple drop-down menus.
4. **Stage 4:** System execution is similar to functional verification, except that the FPGA design runs on the selected FPGA board, while the host application still runs in software. Real data can be streamed in and out of the FPGA board. Many more tests can be run at this stage than during functional verification.
5. **Stage 5:** System debug. Debugging at the hardware level is never necessary, even if a bug is discovered after executing a function in hardware, because QuickPlay guarantees functional equivalence between the software model and hardware implementation. Thus any bug in the hardware version also exists in the software version.
6. **Stage 6:** (Optional) Optimization. While the entire infrastructure built by QuickPlay is highly efficient in terms of performance and utilization, the overall quality of the design will depend on the quality of the user-created kernels. As generic C code will not produce the most efficient hardware implementation, there are a few techniques and guidelines that software developers can follow to greatly improve the efficiency of the HLS generated code. Further optimization can also be done by using Xilinx Vivado HLS or by recoding certain kernels in HDL.

This simple methodology opens up FPGA-based computing to a large segment of software engineers, who can now do their modelling in software, using familiar techniques, then build the system and test in hardware. No other tool has taken this approach as far and offers a framework where software engineers can design and debug exclusively at the source level.

The efficiency of the hardware generated also makes QuickPlay a great tool for hardware engineers to save weeks or months of design effort by letting QuickPlay take care of the mundane hardware design tasks, while they concentrate on their true value add: the processing kernels.

QuickPlay's dataflow model of computation makes it ideal for a large number of FPGA applications, whether for pure CPU co-processing, pre- or post-processing of acquired data by a CPU, or simply in systems with no CPU involved, for example in applications such as networking, broadcast, vision, medical, wireless and more. ●

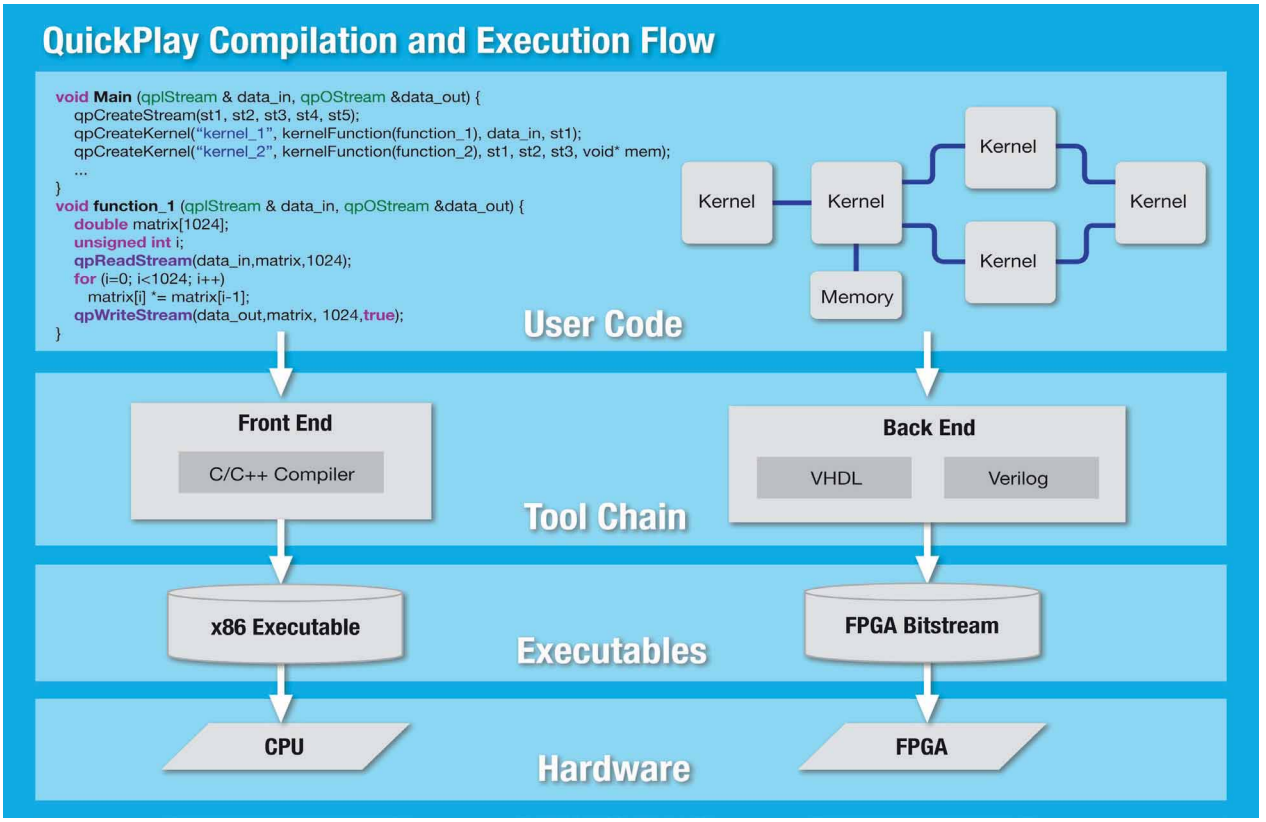
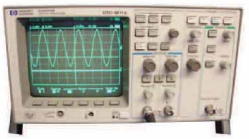


Figure 3: QuickPlay compilation and execution flow

HP 34401A Digital Multimeter 6 ½ Digit



HP 54600B Oscilloscope Analogue/Digital Dual Trace 100MHZ

LAMBDA GENESYS	PSU GEN100-15 100V 15A Boxed As New	£325
LAMBDA GENESYS	PSU GEN50-30 50V 30A	£325
HP34401A	Digital Multimeter 6.5 digit	£275-£325
HP33120A	Function Generator 100 microHZ-15MHZ	£260-£300
HP53131A	Universal Counter 3GHZ Boxed unused	£500
HP53131A	Universal Counter 225MHZ	£350
HP54600B	Digital Oscilloscope 100MHZ 20MS/S	from £75
IFR 2025	Signal Generator 9kHz - 2.51GHZ Opt 04/11	£900
Marconi 2955B	Radio Communications Test Set	£800
R&S APN62	Syn Function Generator 1HZ-260KHZ	£195
Fluke/Philips PM3092	Oscilloscope 2+2 Channel 200MHZ Delay etc	£250
HP3325A	Synthesised Function Generator	£195
HP3561A	Dynamic Signal Analyser	£650
HP6032A	PSU 0-60V 0-50A 1000W	£750
HP6622A	PSU 0-20V 4A Twice or 0-50V 2A Twice	£350
HP6624A	PSU 4 Outputs	£350
HP6632B	PSU 0-20V 0-5A	£195
HP6644A	PSU 0-60V 3.5A	£400
HP6654A	PSU 0-60V 0-9A	£500
HP8341A	Synthesised Sweep Generator 10MHZ-20GHZ	£2,000
HP83731A	Synthesised Signal Generator 1-20GHZ	£1,800
HP8484A	Power Sensor 0.01-18GHZ 3nW-10uW	£75
HP8560A	Spectrum Analyser Synthesised 50HZ - 2.9GHZ	£1,250
HP8560E	Spectrum Analyser Synthesised 30HZ - 2.9GHZ	£1,750
HP8563A	Spectrum Analyser Synthesised 9KHZ-22GHZ	£2,250
HP8566B	Spectrum Analsyer 100HZ-22GHZ	£1,200
HP8662A	RF Generator 10KHZ - 1280MHZ	£750
Marconi 2022E	Synthesised AM/FM Signal Generator 10KHZ-1.01GHZ	£325
Marconi 2024	Synthesised Signal Generator 9KHZ-2.4GHZ	£800
Marconi 2030	Synthesised Signal Generator 10KHZ-1.35GHZ	£750
Marconi 2305	Modulation Meter	£250
Marconi 2440	Counter 20GHZ	£295
Marconi 2945	Communications Test Set Various Options	£2,500
Marconi 2955	Radio Communications Test Set	£595
Marconi 2955A	Radio Communications Test Set	£725
Marconi 6200	Microwave Test Set	£1,500
Marconi 6200A	Microwave Test Set 10MHZ-20GHZ	£1,950
Marconi 6200B	Microwave Test Set	£2,300
Marconi 6960B with	6910 Power Meter	£295

MARCONI 2955B Radio Communications Test Set

FLUKE/PHILIPS PM3092 Oscilloscope 2+2 Channel 200MHZ Delay TB, Autoset etc

Tektronix TDS3012	Oscilloscope 2 Channel 100MHZ 1.25GS/S	£450
Tektronix 2430A	Oscilloscope Dual Trace 150MHZ 100MS/S	£350
Tektronix 2465B	Oscilloscope 4 Channel 400MHZ	£600
Cirrus CL254	Sound Level Meter with Calibrator	£40
Farnell AP60/50	PSU 0-60V 0-50A 1KW Switch Mode	£195
Farnell H60/50	PSU 0-60V 0-50A	£500
Farnell B30/10	PSU 30V 10A Variable No Meters	£45
Farnell B30/20	PSU 30V 20A Variable No Meters	£75
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Racal 2101	Counter 20GHZ LED	£295
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Fluke 99B	Scopemeter 2 Channel 100MHZ 5GS/S	£125
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Panasonic VP7705A	Wow & Flutter Meter	£60
Panasonic VP8401B	TV Signal Generator Multi Outputs	£75
Pendulum CNT90	Timer Counter Analyser 20GHZ	£750
Seaward Nova	PAT Tester	£95
Solartron 7150	6 1/2 Digit DMM True RMS IEEE	£65
Solartron 7150 Plus	as 7150 plus Temp Measurement	£75
Solatron 7075	DMM 7 1/2 Digit	£60
Solatron 1253	Gain Phase Analyser 1mHZ-20KHZ	£600
Tasakago TM035-2	PSU 0-35V 0-2A 2 Meters	£30
Thurlby PL320QMD	PSU 0-30V 0-2A Twice	£160-£200
Thurlby TG210	Function Generator 0.002-2MHZ TTL etc Kenwood Badged	£65

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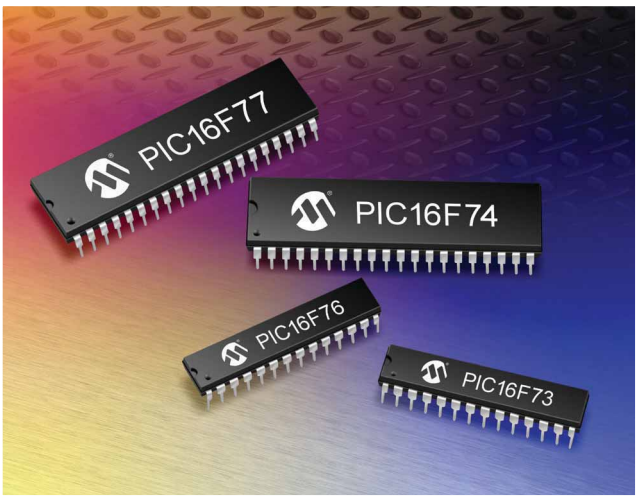
GETTING THE MOST OUT OF PERIPHERALS



MARK PALLONES, TEAM LEAD AT MICROCHIP TECHNOLOGY, DISCUSSES HOW TO CONFIGURE AND INTEGRATE PERIPHERALS ON 8-BIT MID-RANGE MICROCONTROLLERS

To get the most out of modern microcontrollers, it is necessary to ensure that its peripherals are properly configured. Sometimes this involves configuring them one step at a time before putting them together. This is particularly important when the microcontroller is chosen because its peripherals match the application; without care, the peripherals may not provide the desired output.

As an example, look at the PIC16F7X and PIC16C7X families of 8-bit mid-range microcontrollers from Microchip. The PIC16F7X is a flash device and the PIC16C7X is a one-time-programming (OTP) device. The peripherals for both devices include an analogue-to-digital converter (ADC), timers, capture-compare PWM (CCP) and the universal synchronous asynchronous receiver transmitter (USART).

ADC Module

The ADC module converts an analogue input signal into a corresponding 8-bit digital number. The output of the internal sample-and-hold circuit is input to the converter, which generates the result via successive approximation.

The analogue reference voltage is software-selectable to either the device's positive supply voltage (VDD) or the voltage level on the Vref pin. The ADC has the unique feature of being able to operate while the device is in sleep mode. The block diagram of the circuit is shown in Figure 1.

The module has three registers, the two control registers are ADcon0 and ADcon1 and the single result register is ADres. ADcon0 controls the operation of the ADC module.

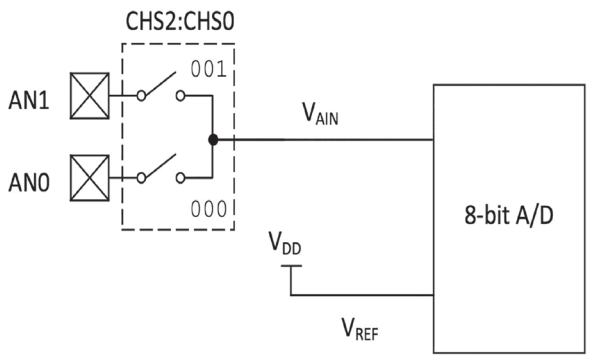


Figure 1: Analogue-to-digital conversion block diagram

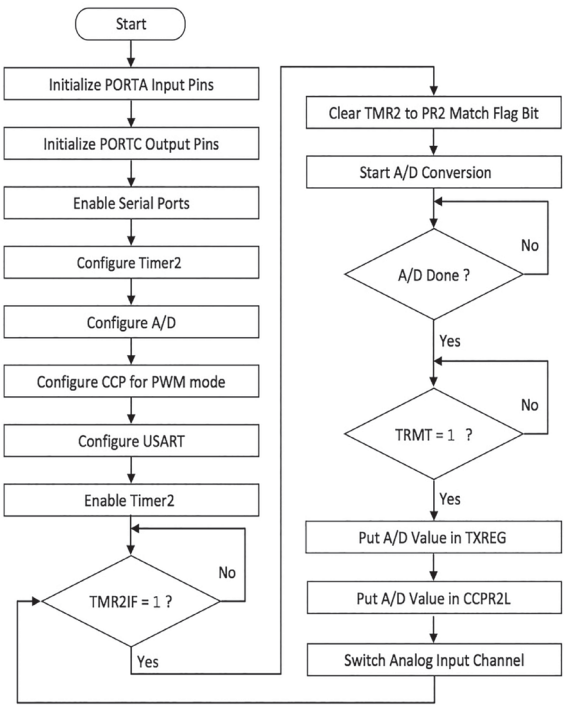


Figure 2: Firmware flowchart

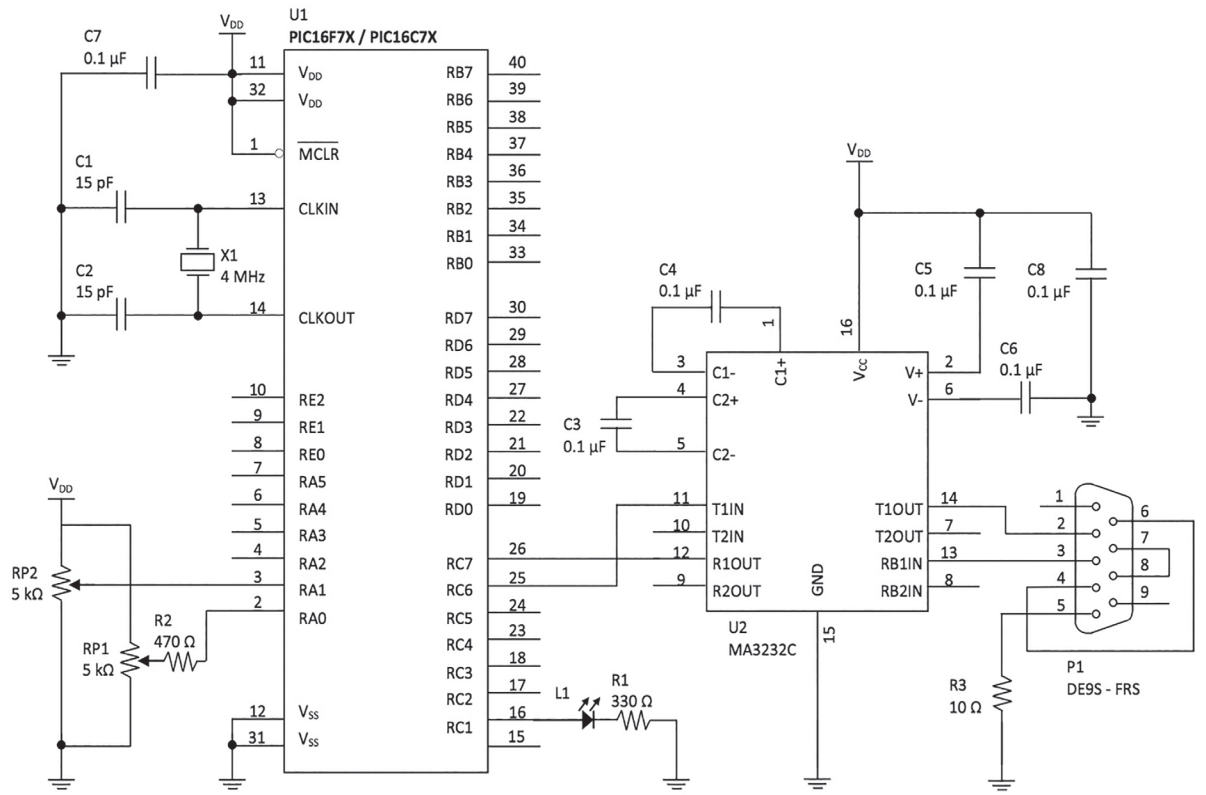


Figure 3: PIC16F7X and PIC16C7X demo schematic

This register is used to select the conversion clock frequency and the analogue channel. It is where the start and end of conversion are determined. ADcon1 configures the functions of the port pins. The microcontrollers have either five or eight I/O pins that can be configured as analogue inputs.

After ADcon0 and ADcon1 are configured, the go/done bit in ADcon0 is set to a one to start the conversion and then monitored to track when the conversion is complete. At that stage the result is loaded into the ADres register, the go/done bit is cleared and the A-D interrupt flag bit (ADif) is set.

> To get the most out of modern microcontrollers, it is often necessary to ensure that its peripherals are properly configured

Simple code is available that reads the ADres register and passes it to the USART and CCP modules. Switching between the two analogue input channels is done by changing the value of the CHS2:CHS0 bits of the ADcon0 register. Figure 1 only shows AN1 and AN0, but any of the analogue input channels can be selected via CHS2:CHS0.

Timers

The microcontrollers have three timer modules – timer0, timer1 and timer2 – each can generate an interrupt to indicate that an event, such as a timer overflow, has occurred. Timer0 is a simple 8-bit timer-counter. Timer1 is a 16-bit timer-counter consisting of two readable and writable 8-bit registers.

Timer2 is an 8-bit timer with a pre-scaler, post-scaler and period register. Using the pre-scaler and post-scaler at their maximum settings, the overflow time is the same as that of a 16-bit timer. Timer2 is the PWM time-base when the CCP module is used in the PWM mode.

For PWM mode, the registers to be configured are the timer2 period register (PR2), timer2 control register (T2con) and PIR1 register. The PWM output has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is inverse of the period, specified by writing to the PR2 register.

In addition, there are two capture-compare PWM (CCP) modules, each containing a 16-bit register that can operate as a 16-bit capture register, a 16-bit compare register or a 10-bit PWM master-slave duty cycle register. The CCP modules are identical in operation except for the special event trigger.

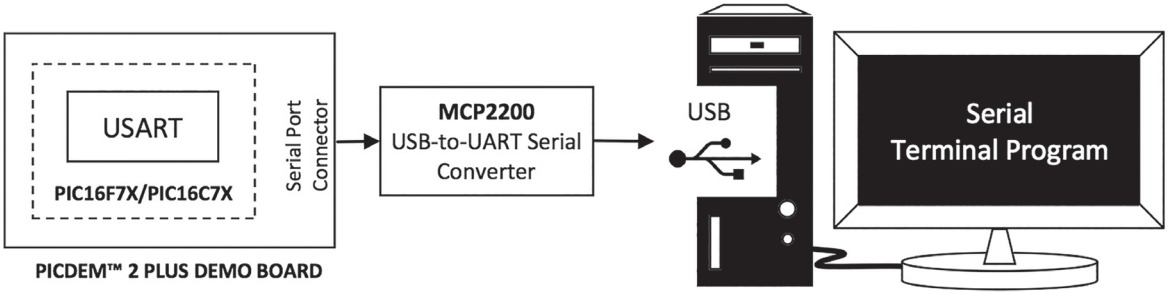


Figure 4: Serial transmission block diagram

USART

The USART module is one of the two serial I/O modules, the other being the SSP. The USART is also known as a serial communications interface, or SCI. It can be configured as a full-duplex asynchronous system that can communicate with peripheral devices such as personal computers, or as a half-duplex synchronous system that communicates with peripheral devices such as A/D or D/A integrated circuits and serial EEPROMs.

In the sample programme, it is configured as a full-duplex asynchronous system to communicate with a PC. In this application, the USART is only used for transmission. The registers needing to be set up are the baud rate generator register (SPBRG), transmit status and control register (TXSTA), receive status and control register (RCSTA) and transmit data register (TXreg).

The dedicated 8-bit SPBRG controls the period of a free-running 8-bit timer. In asynchronous mode, one bit also controls the baud rate; in synchronous mode, this bit is ignored.

The TXSTA is where the asynchronous mode and 8-bit transmission are selected. The transmit enable (TXen) bit of the TXSTA enables transmission and the transmit shift register status bit (TRMT) is a read-only bit that indicates the status of the transmit shift register (TSR). To start transmission, it is necessary to set the serial port enable bit (SPen) in the RCSTA register. Writing to the TXreg then initiates the transmission. The code example copies the A-D result into the TXreg; the value is automatically moved into the TSR and shifted out on the RC6/TX pin.

Peripheral Integration

After each peripheral has been configured it needs to be integrated with the others. The loop code segment in the

sample programme shows how peripherals are connected to each other. The firmware flowchart in Figure 2 combines the configuration and integration processes.

All I/O ports are first initialised. Serial ports are also enabled for USART transmission, followed by the configuration of the timer2, ADC, CCP and USART peripherals. For the ADC, only one analogue input channel is selected during the configuration process. Timer2 is enabled and the programme starts polling the TMR2IF flag bit. TMR2IF sets whenever there's a match between the TMR2 and PR2 registers, at which point TMR2IF is then cleared in software and A/D conversion begins.

After the A/D conversion is completed, the programme monitors the TRMT bit to be set, indicating the TSR register of the USART is empty and ready for transmission. The A/D value is written to the TXreg and CCPR2L registers. Then the next analogue channel is selected and the process repeated. The USART and CCP outputs are received and processed by external hardware devices.

Hardware

The schematic diagram of the hardware is shown in Figure 3. It is basically part of the PICDEM 2 Plus schematic with a few additional components.

The RP1 and RP2 trim pots are used to demonstrate a method of switching between analogue input channels. They also determine the input voltage levels fed to the ADC.

LED L1 is connected to the PWM output pin, RC1/CCP2, which is in series with the current-limiting resistor R1. U2 is an RS232 line driver that provides the electrical interface between the USART and the P1 serial port connector.

When the analogue input voltage is fed to the ADC, it is converted into a corresponding digital value. The input comes from AN0 or AN1 depending on the configured analogue input channel. The digital results will be sent to both the USART and the CCP. The USART then sends this value to a serial terminal programme, which displays an output value in a certain format, depending on the terminal configuration. Likewise, the PWM of the CCP varies the duty cycle of the output pulse to control the brightness of the LED.

For serial transmission and display, the USART output is sent to the serial terminal programme by connecting the USB-to-UART serial converter to the serial port connector in the PICDEM 2 Plus demo board and to the USB port of a PC, as shown in Figure 4. Microchip's MCP2200 can be used as the USB-to-UART serial converter.

Since two analogue channels are used in the ADC, two values will also be displayed on the PC monitor. A serial terminal programme is used to capture, control and debug binary streams of data. It must be set to 2400 baud, eight data bits, one stop bit and no parity to match the USART software configuration. The displayed value can also be set to either ASCII, ANSI, hexadecimal, binary or other types of numerical representation, depending on the serial terminal programme features. ●

A SOFTWARE PACKAGE FOR THE PCB DESIGN ENVIRONMENT

BY **ROBERT HUXEL**, TECHNICAL MARKETING MANAGER FOR EMEA AT ALTIUM

Many will agree that a design engineer may spend only a fraction of his day actually designing. Sometimes this portion is frustratingly small, since time is spent on other parts of the job, a large portion of which is managing information. Automation can make a big difference here, especially with the right systems.

Printed circuit board design can be viewed as a pivotal design function. In a way, it both defines and is constrained by the overall format of the final product: There is an exchange of information with the mechanical world (ECAD to MCAD software packages in terms of design systems) that relates to the external dimensions of the product, and to how the electronic assemblies are packaged within the outer casing.

From another perspective, the PCB is where all the circuit design work converges, including component selection and procurement, plus all the verification efforts for the electrical, mechanical and thermal domains.

> The PCB is where all the circuit design work converges, including component selection and procurement plus all the verification efforts for the electrical, mechanical and thermal domains

All these aspects represent information that has to be sourced, maintained and exchanged between various systems. Viewed from that high level, it is necessary that the design process and tools access common data formats and exchange information in a seamless manner, even though the reality is rather different.

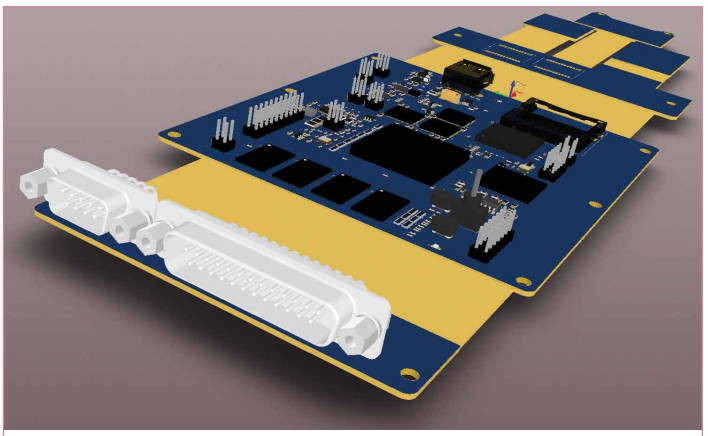


Figure 1: True collaboration gives both ECAD and MCAD designers visibility into incremental component placement changes simultaneously

Interfacing Domains

The interface between mechanical and electrical PCB design environments is a well-known case in point. For a start, the PCB needs an enclosure, with a space that is most likely to be pre-determined. Repeated exchanges or iterations between the mechanical and electrical design spaces to fit the PCB and enclosure are common. Over time, a variety of off-the-shelf and "home-built" systems have evolved to facilitate this exchange; where files are passed back and forth between ECAD and MCAD, the two file formats that have been in common use.

IDF (Intermediate File Format) is long established but falls short of passing comprehensive geometry. It is not a full 3D representation, rather a layout or footprint plus the heights of individual components from their models.

STEP (Standard for The Exchange of Product model data) takes things forward a stage with a true 3D representation of design data and can be used for PCBs, components, mechanical assemblies/housings and any other design files that may be worked on by multiple designers using different programs. This, however, still involves exporting and importing files between software packages, which typically complicates version control and adds errors.

There are benefits and limitations associated with using STEP for bi-directional transfer between programs. Native 3D PCB editing tools running within ECAD software for mechanical design, or at least alignment, placement and export of 3D mechanical models, allow much of the work to be done in a single software package. Altium Designer, for instance, includes capabilities for aligning 3D component models to footprints, modelling and clearance-checking for housings/enclosures and, if necessary, standard exports of complex PCB features for MCAD interfacing. More recently, Altium created a new PCB tool that comprehensively integrates PCB data with full 3D CAD in SolidWorks.

Costly Business

The true costs of not having a coherent link between ECAD and MCAD can be considerable. These include missed schedules and extended time to market; inefficient use of skilled staff, perhaps leading to higher headcount than necessary; and designs taken

to market in a less elegant form (due to restricted opportunity for design exploration), leading to reduced sales, added to which are the immediate development-budget impacts of repeated prototype revisions.

Any significant error can result in an unwanted prototype spin. Getting a conflict-free outcome on the first iteration is, in reality, only the first step. The design process will typically require a number of revisions and changes – not counting those occurring from file transfer. As with any development, the cost of a change order rises sharply as the design proceeds. On average, engineering change orders (ECOs) cost about €1,800 to implement during development, rising to almost €10,000 once a design has been released to manufacturing.

There can be more subtle costs resulting from lack of automated data exchange, or not having confidence in the accuracy of the parameters. Tolerances and clearance allowances can be increased just to be sure, resulting in larger designs than need be, using more materials and larger bill of materials (BoM). In an era of ever-more compact and portable products, this is increasingly unacceptable.

Designers can resort to traditional methods of ensuring fit and clearances, such as paper/card physical models ("paper dolls"). Aside from the wasted resource of having skilled circuit and board designers spending their time making cardboard cutouts, these cannot accurately represent aspects such as bend radii of rigid/flex assemblies – for that, software, such as Altium Designer, is the best fit.

Fit For Space

More recently, technology has offered the alternative of a 3D printed physical model to evaluate form and fit. These models give a real-world impression of how the end product will look and feel, but compared with an integrated ECAD/MCAD environment, they are a very limited verification vehicle to confirm fit and clearance.

A typical conventional design flow will start with a draft layout that may be set by constraints, either mechanical ("it has to fit into this space") or electrical ("the PCB layout looks like this, the enclosure needs to fit around it"). In either case, if the first-pass PCB fits the draft case, with all components falling within their expected envelopes and no unexpected conflicts, then that layout can become "untouchable". Any major revisions are simply too painful.

With a seamless design environment, electrical and mechanical designers can both explore alternative layouts and shapes in a virtual environment, without incurring the costs of a major design re-spin for every variation.

Component Data

A PCB layout must be populated with components, and a comprehensive and accurate component library is a further key aspect of the integrated design environment. For many years, one of the impediments to operating an integrated PCB and 3D design environment was the limited availability of component

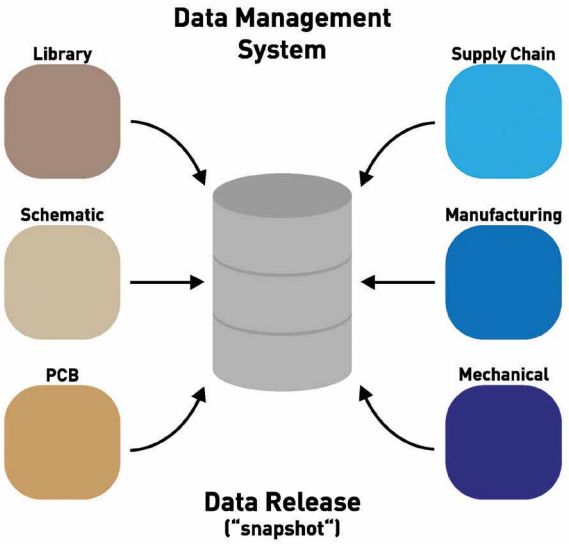


Figure 2: A design release includes all design information and other pertinent domains for bringing a product to market

data. Today's situation is much improved, with component manufacturers and their distributors making dimensions and parameters routinely available in common formats.

As with the ECAD/MCAD interface, there are great benefits to having a joined-up design environment with full access to all aspects of component data. The circuit designer first comes to component selection from the electrical/electronic performance perspective, but that is only a part of the complete description of a component that resides in the full database. Other attributes include a physical model with complete geometry (and rendered visualisation), symbols, the PCB footprint and visibility into the e-commerce supply chain for real-time parts availability and pricing information. The data sets will also include a part's status: Has it been approved, or superseded? Is it "recommended for new designs" – or has it been tagged as end-of-life? Is it preferred, are there similar parts that meet the requirements? Have any issues arisen with use of the part in the past? If it must be added to the library, what is the lead time to do so? And so on.

The power of having that data tightly linked to the design environment hardly needs stating. Less obvious, perhaps, are the potential costs of inefficient management of ECAD libraries. Inefficient processes can add to administrative overhead, with increased operational cost through redundant or non-centralised infrastructure, and can lead to duplication of effort in – for example – sourcing and qualifying parts similar to those already listed, instead of exploiting common libraries and preferred electronic component lists. This in turn can push up inventory cost, with redundant parts being stocked and eventually obsoleted and written-off.

Component data of less than ideal quality also has costs.

Incomplete information or insufficient part qualification processes can leave room for ambiguity and may cause costly rework of a product when design verification reveals shortcomings, delaying volume production and shipping. Worse, the issues may go undetected until after a product has been brought to market.

Tools Are Just As Important

The integrated library and ECAD/MCAD design environment must therefore not only provide seamless support to the design processes but also need a comprehensive set of tools to manage the data they contain. This includes comprehensive access control; who has the authority to create, modify, delete parts, as opposed the designer's need to access, import into a project and, where necessary, add commentary.

A number of options exist to implement this function; it can be – and frequently has been – provided by custom-built, internally-developed solutions. These largely stand apart from the CAD/EDA environment and are difficult to integrate closely, lacking the ability to track and conform to evolving industry standards. Alternative solutions include those based on a product lifecycle management platform, but these too can lack the ideal level of integration.

Key performance metrics related to an integrated library solution can be stated as:

- Increased engineering efficiency;
- Shortened design cycles with fewer library- and component-related design spins;
- Improved product quality through approved vendors and parts, reduced inventory cost and new part introductions;
- Improved overall library quality leading to fewer issues downstream;
- Reduction of infrastructure cost and overhead.

To meet these needs, Altium introduced Altium Vault, which provides component data repositories with all the attributes needed by the ECAD/MCAD flow. It embodies complete revision control and lifecycle management, both for objects acquired (i.e. components) or assemblies manufactured.

The organisation using it has, effectively, its own part catalogue from which to select, built around its own priorities and visibility into the supply chain. Parts lists and BoM are checked in real time for issues – either historical or anticipated – with any devices listed, and will be withheld from release until resolved.

The Vault gathers all expected and required information in one system, with no data redundancy; it supports fast component searches with integrated supply-chain information. Geographically-distributed users can have worldwide intranet access to a single database, and the engineering function gains data consistency from design process to board assembly. ●

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MANY EMBEDDED DESIGNS REQUIRE MINIMUM INPUT-OUTPUT PIN-COUNT. **PROFESSOR DOGAN IBRAHIM** OF NEAR EAST UNIVERSITY, CYPRUS, DESCRIBES HOW A TEXT-BASED LCD CAN BE CONTROLLED WITH ASCII COMMANDS OVER JUST A SINGLE DATA LINE

LCDs are used in most microprocessor- and microcontroller-based projects to display data, and there are two main types: text-based and graphics-enabled.

Most text-based LCDs are based on the familiar HD44780 display controller chip. LCDs are sold as modules with integrated controllers and a SIL connector for interface and control. They can display from one to four lines of data, with each line consisting of up to 16 characters. Software LCD driver routines are used to control the characters' actual positions. In addition, various display commands are available, such as clearing, underlining or blinking, and others.

As well as the two power pins and a contrast adjustment pin, the HD44780-based LCDs normally also require eight data pins and three control pins for their operation. However, it is possible to control these LCDs using only four data pins and two control pins. In these reduced-pin applications, an 8-bit character (or data) is sent twice. Communication to the LCD is in one direction where the LCD only receives data and, as a result, one of the LCD pins (WE) can be permanently connected to ground.

When using small microcontrollers in LCD projects, there's a limited number of I/O pins and it may not be possible to allocate six of them to just control the LCD. Reducing the interface pin-count requirements without complicating the hardware or the software would be a definite advantage in these projects.

Possible Solutions

There are various solutions in reducing the LCD pin-count; almost all use a shift register to convert serial data coming from the host into parallel form, to drive the LCD. In some projects a port expander is used to extend the microcontroller's I/O port count. Most of these systems are controlled by SPI or I2C bus structures and require at least two or more I/O pins.

Some systems use a single wire, a shift register and RC low-pass filters to control the LCD data and command timings. The drawback of these systems is that the host needs complex software to drive the LCD correctly to display the required data. In addition, different types of microcontrollers require different software to control the LCDs, making such systems even more problematic.

Simplified System

The system suggested here is a low-cost 18-pin PIC microcontroller (see Figure 1), which receives LCD data in ASCII form from its RS232-based serial input port, converts this data into parallel form and presents it to the LCD. The LCD is connected to the microcontroller in 4-bit data mode with two control signals. Interface to the circuit is through a single TTL-based serial pin, connected to the TX pin of the host UART.

The circuit diagram of the proposed system is shown in Figure 2. The design is based on a low-cost PIC16F1847 8-bit PIC microcontroller – a high performance device with 8K of program memory, 1K data memory, 16 I/O pins including a UART, four 8-bit timers, two comparators, twelve 10-bit ADC channels and a number of clock options. The reasons for choosing this microcontroller include its low cost, small footprint, on-chip UART and high-accuracy, high-speed, internal clock (up to 32MHz).

Any other PIC microcontroller or any other type of microcontroller (e.g. Arduino) can also be used in this project. The only requirement is that the microcontroller have an accurate clock (e.g. internal clock, or external crystal) and a UART module

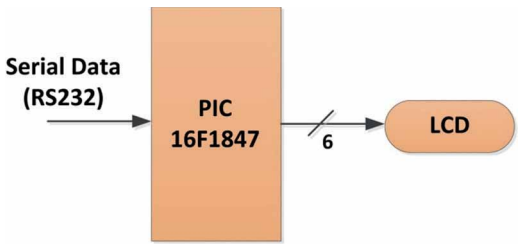

Figure 1: Block diagram of the system

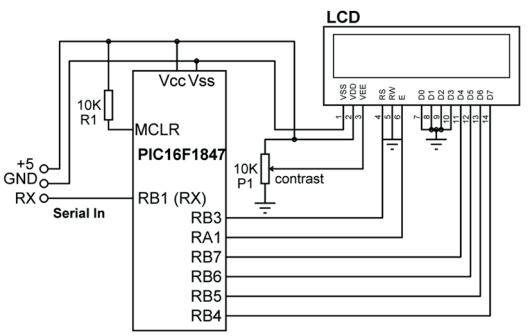

Figure 2: Circuit diagram of the system

(although a serial port can be emulated in software if no UART module is available).

The microcontroller PORTB pins RB7:RB3 are connected to the LCD DB4:DB7 pins, respectively. RB1 and RB2 pins are internally reserved for the hardware UART and thus could not be used for the LCD interface in this project. RB1 and RB2 are the UART RX and TX pins respectively, although here only the RX pin is used to receive data from the host. RA1 pin is used to control the LCD.

The internal high-accuracy clock, configured to operate at 16MHz, provides clock pulses to the microcontroller so the component count can be kept at a minimum. LCD contrast is set with a 10K potentiometer.

The system's basic technical features are shown in Table 1.

One-wire UART interface
ASCII commands
Low cost
Compatible with any type of microcontroller
Standard LCD modules

Table 1: Technical features of the system

System Operation

Operation of the system is described in Program Description Language (PDL) in Figure 3.

After initializing the LCD and the UART modules, the program enters a loop, where serial data and commands are received from the UART and then the LCD is controlled as required to display the required data.

The data is sent to the LCD in serial ASCII format, preferably from the output of a UART of the host microcontroller. Commands are provided for positioning the cursor at the required row and column to clear the display, shift the data, and so on. These commands are similar to the LCD commands provided by the mikroC Pro for PIC language. Table 2 gives a list of the available commands.

Notice that the commands are case-sensitive and must be entered exactly as shown in the table. The row and column numbers must be one and two digits respectively. For example, to display the text "EW", starting from row 1, column 3 position, the following data should be sent to the system, preferably through a UART:

Lcd_Out(1,03EW)

To display character "x" at the current cursor position enter:

Lcd_Chr_Cp(x)

Similarly, to clear the display, send the following command:

Lcd_Cmd(_LCD_CLEAR)

```
BEGIN
Initialize LCD
Initialize UART
DO FOREVER
        Wait to receive data from UART
        IF command is Lcd_Out THEN
        Display data at the given row and column
        ELSEIF command is Lcd_Out_Cp THEN
        Display data at current cursor position
        ELSEIF command is Lcd_Chr THEN
        Display character at the given row and column
        ELSEIF command is Lcd_Chr_Cp THEN
        Display character at current cursor position
        ELSEIF command is Lcd_Cmd THEN
        Send command to the LCD
                ENDIF
        ENDDO
END
```

Figure 3: System operation

COMMAND	DESCRIPTION
Lcd_Out(n,mmText)	Display Text at n,mm
Lcd_Out_Cp(Text)	Display Text at current cursor position
Lcd_Chr(n,mmx)	Display character x at n,mm
Lcd_Chr_Cp(x)	Display character x at current cursor position
Lcd_Cmd(command)	Send command to LCD

Table 2: Available commands

The Program

The program listing is shown in Figure 4. It was written using mikroC Pro for PIC integrated development environment (IDE).

At the beginning of the program, the interface between the microcontroller and the LCD is defined with a 'sbit' statement: At the beginning of the main program the clock is configured to operate at 16MHz (it can be set to 32MHz) by setting register OSCCON to 0x7A. The internal oscillator (INTOSC) must be selected with the PLL disabled in the configuration fuse settings during the programming; see Figure 5.

PORTA and PORTB are then configured as digital ports by clearing registers ANSELA and ANSELB. Port pin RB1 and RB2 are configured as UART RX and TX pins respectively by clearing registers APFCON0 and APFCON1.

Notice that only the RX function is used in this project. The LCD is initialized by the command Lcd_Init(). Similarly, the UART module is initialized using command UART1_Init(9600) to operate at 9600 baud. By default, the data width is seven bits; parity is not used and only one stop bit is used. The baud rate can be increased if desired for faster processing.

The remainder of the program operates in a loop formed using a 'while' statement. Inside this loop, the UART is checked

for the availability of data using the statement UART1_Data_Ready(). ASCII data is read from the UART using the statement UART1_Read_Text(buff, ")", 255). Here, the program blocks until the terminator character ")" is received and the received data is stored in character array 'buff'. The program then looks for various LCD commands using the string compare statements 'strstr' and controls the LCD accordingly.

The system recognizes five commands with the following command numbers (or modes):

Command	Mode
Lcd_Out_Cp	1
Lcd_Out	2
Lcd_Chr_Cp	3
Lcd_Chr	4
Lcd_Cmd	5

```
/*********************************************************
                        1-LINE LCD PROJECT
                        ==================
This project controls an LCD using only one line. The system is
based on a PIC microcontroller that receives serial commands
and sends out parallel commands to the LCD. Operation is at
9600 baud, 8 bits, no parity, 1 stop bit.

The valid commands are:

Lcd_Out(n,mmText)       e.g. Lcd_Out(1,02Hello) displays
                        Hello at 1,2
Lcd_Out_Cp(Text)        e.g. Lcd_Out_Cp(Hello) displays
                        Hello at current cursor position
Lcd_Chr(n,mmb)          e.g. Lcd_Chr(1,02p) displays p at
                        1,2
Lcd_Chr_Cp(p)           e.g. Lcd_Chr_Cp(p) displays p at
                        current cursor position
Lcd_Cmd(command)        e.g. Lcd_Cmd(_LCD_CLEAR)
                        clears the display
*********************************************************/
// LCD module connections
sbit LCD_RS at LATB3_bit;
sbit LCD_EN at LATA1_bit;
sbit LCD_D4 at LATB7_bit;
sbit LCD_D5 at LATB6_bit;
sbit LCD_D6 at LATB5_bit;
sbit LCD_D7 at LATB4_bit;

sbit LCD_RS_Direction at TRISB3_bit;
sbit LCD_EN_Direction at TRISA1_bit;
sbit LCD_D4_Direction at TRISB7_bit;
sbit LCD_D5_Direction at TRISB6_bit;
sbit LCD_D6_Direction at TRISB5_bit;
sbit LCD_D7_Direction at TRISB4_bit;
// End LCD module connections
void main()
{
unsigned char buff[50], txt[50];
unsigned char row,column,l,j,mode,cmd;
char *p;
unsigned int q;
OSCCON=0x7A;
TRISA =0;
TRISB = 0;
ANSELA = 0;                 // Configure PORTA as digital
ANSELB = 0;                 // Configure PORTB as digital
APFCON0 = 0;                // Configure RB1 as UART RX
APFCON1 = 0;                // Configure RB2 as UART TX
TRISB.RB1 = 1;              // Configure RB1 as input
Delay_Ms(1000);
Lcd_Init();                 // Initialize LCD library
Delay_Ms(1000);
UART1_Init(9600);           // Initialize UART library
Delay_Ms(100);
Lcd_Cmd(_LCD_CLEAR);        // Clear LCD to start with
Delay_Ms(100);
//
// Main program loop
//
while(1)
{
mode = 0;
if(UART1_Data_Ready() == 1)          // If data received
{
UART1_Read_Text(buff,")",255);       // Wait until ")" received
if(strstr(buff, "Lcd_Out_Cp") != 0x0)mode = 1;
else if(strstr(buff, "Lcd_Out") != 0x0)mode = 2;
else if(strstr(buff, "Lcd_Chr_Cp") != 0x0)mode = 3;
else if(strstr(buff, "Lcd_Chr") != 0x0)mode = 4;
else if(strstr(buff, "Lcd_Cmd") != 0x0)mode = 5;
p = strstr(buff, , "Lcd");
q = p – buff;
if(mode == 2 || mode == 4)
{
l = strlen(buff+q);
row = buff[8+q]-'0';
column = 10*(buff[10+q]-'0')+buff[11+q]-'0';
if(mode == 2)
{
l = l - 12;
for(j=0; j < l; j++)txt[j] = buff[12+j+q];
txt[j]=0x0;
Lcd_Out(row,column,txt);
}
else
Lcd_Chr(row,column,buff[12+q]);
}
else if(mode == 1 || mode == 3)
{
if(mode == 3)Lcd_Chr_Cp(buff[11+q]);
else
{
```

```
l = strlen(buff+q);
l = l - 11;
for(j=0; j < l; j++)txt[j] = buff[11+j+q];
txt[j] = 0x0;
Lcd_Out_Cp(txt);
}
}
else if(mode == 5)
{
l = strlen(buff+q);
l = l - 8;
for(j=0; j < l; j++)txt[j] = buff[8+j+q];
txt[j] = 0x0;
if(strstr(txt,"_LCD_CLEAR") != 0x0)cmd = 1;
else if(strstr(txt,"_LCD_RETURN_HOME") != 0x0)cmd = 2;
else if(strstr(txt,"_LCD_MOVE_CURSOR_LEFT") != 0x0)cmd
= 0x10;
else if(strstr(txt,"_LCD_MOVE_CURSOR_RIGHT") != 0x0)cmd
= 0x14;
else if(strstr(txt,"_LCD_BLINK_CURSOR_ON") != 0x0)cmd =
0x0F;
else if(strstr(txt,"_LCD_FIRST_ROW") != 0x0)cmd = 0x80;
else if(strstr(txt,"_LCD_SECOND_ROW") != 0x0)cmd = 0xC0;
else if(strstr(txt,"_LCD_SHIFT_LEFT") != 0x0)cmd = 0x18;
else if(strstr(txt,"_LCD_SHIFT_RIGHT") != 0x0)cmd = 0x1C;
else if(strstr(txt,"_LCD_CURSOR_ON") != 0x0)cmd = 0x0E;
else if(strstr(txt,"_LCD_CURSOR_OFF") != 0x0)cmd = 0x0C;
Lcd_Cmd(cmd);
}
}
```

Figure 4: mikroC Pro for PIC program listing

Figure 6 shows a sample display when the mikroC Pro for PIC program shown in Figure 7 is run using a PIC18F87J50 microcontroller with its TX output (RC6) connected to the RX input of the system.

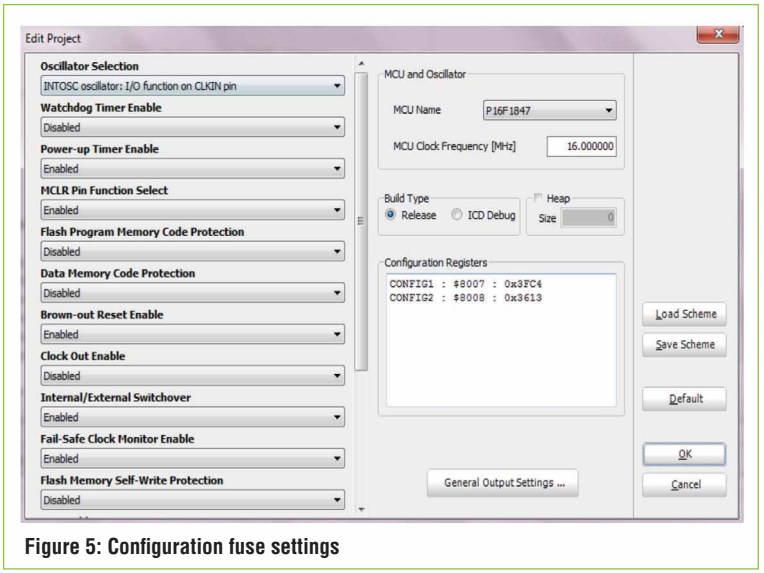

Figure 5: Configuration fuse settings

Figure 6: Sample display (see Figure 7)

```
void main()
{
        UART1_Init(9600);       // Initialize UART1 (pin
                                RC6)
        UART1_Write_Text("Lcd_Out(1,01Received)");
        Delay_Ms(10);
        UART1_Write_Text("Lcd_Out_Cp(Data:)");
        Delay_Ms(10);
        UART1_Write_Text("Lcd_Out(2,01Test
message..)");
        while(1);
}
```

Figure 7 Program to display the text in Figure 6

USING EMBEDDED ACTIVE RFID AND WIRELESS MESH NETWORKS IN AGRICULTURE

BY **NURSYAHIDA MOHD NOOR** AND **CHE ZALINA ZULKIFLI** FROM SULTAN IDRIS EDUCATION UNIVERSITY, MALAYSIA

Agriculture is the largest user of water in the world, so water management should be as efficient as possible without affecting production.

Most water issues stem from lack of good monitoring and control at farm level. Crop yields depend on water but can suffer due to excessive irrigation too. Here, we propose an automated irrigation system based on real-time remote monitoring and control that replaces human-to-human (H2H) and human-to-machine (H2M) interfaces with a machine-to-machine (M2M) setup. The system uses embedded active radio frequency identification (RFID) devices, such as moisture sensors needed for data including soil moisture and condition.

It is paramount that farmers are aware of all aspects and conditions of their farm, which nowadays is amply aided by new technologies. Our setup uses RFID devices built into a monitoring control system and a wireless mesh sensor network (WMSN). WMSN is suitable because it combines the reliability of hardwiring with the versatility of wireless networking at only a small compromise in speed. WMSNs consist of cost-efficient, battery-powered sensor modules and embedded networking intelligence.

Combining RFID with WMSN offers the potential to gather and provide information by sensing environmental conditions such as temperature, light, humidity, pressure, vibration and sound, as well as detect the presence and location of an object. Real-time information from the fields will provide a solid base for farmers to adjust their strategies at any point, instead of taking decisions based on hypothetical average conditions.

RFID Basics

RFID is an effective automatic identification technology for objects and animals. The most important function of RFID is the ability to track the location of a tagged item.

The RFID architecture typically comprises tags, a reader and a computer/host (see Figure 1). The RFID reader collects the information from the tags and passes it on to the computer for analysis. RFID software helps with this collection and processing of data.

Each tag has a unique identification number and a memory that stores additional information, such as manufacturer and product type, and an object's environmental details, such as temperature, humidity and others.

RFID tags come in two types: active and passive; see Table 1 for comparison.

Active tags are powered by a built-in battery, which allows data to be transmitted over long distances but also for the device to operate at higher frequencies: 455MHz, 2.45GHz and 5.8GHz. The tag's battery is normally replaceable, anywhere between one and seven years.

By comparison, passive RFID tags are smaller, low in cost and range, and rely on the reader for power. Their read-range is limited and not possible through metal or liquid.

RFID systems can be categorised by the frequency band they operate in: low, high and ultra-high (see Table 2). The low frequency (LF) band is from 30kHz to 300kHz. Typically, LF RFID systems operate at 125kHz, with some at 134kHz. This

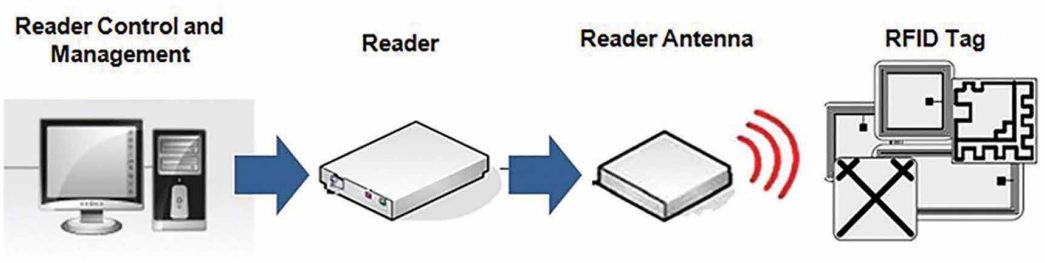

Figure 1: Basic RFID system

	ACTIVE RFID	PASSIVE RFID
Distance	Up to 100 feet	Up to 20 feet
Power Source	Internal-Battery powered	External-Relies on reader
Data Storage	128kb large read/write data	128b small read/write data
Tag Expired	About 5-10 years depending on the battery's life	Often longer than a lifetime depending on the environment
Size	Large enough to accommodate the battery. Usually bulky	As small as a microchip to as large as a paperback book

Table 1: The difference between active and passive RFID tags

FREQUENCY BAND	NAME (FREQUENCY)	RANGE	SYSTEM NAME (RFID)
30kHz – 300kHz	Low Frequency	10cm	LF Systems
3MHz – 30MHz	High Frequency	10cm-1m	HF Systems
860MHz – 960MHz	Ultra High Frequency	12m	UHF Systems

Table 2: Classification by frequency

frequency band provides a short read-range of 10cm and a slower read speed, but it's not so sensitive to radio interference.

The high frequency (HF) band covers 3-30MHz. Most HF RFID systems operate at 13.56MHz with read ranges between 10cm and 1m. These systems experience moderate sensitivity to interference.

The ultra-high frequency (UHF) band covers the range from 300MHz to 3GHz; systems complying with the UHF Gen2 standard for RFID operate in the 860-960MHz band.

There are variances in this frequency from region to region, but in most countries UHF Gen2 RFID systems operate between 900MHz and 915MHz.

> Real-time information from the fields will provide a solid base for farmers to adjust their strategies at any point, instead of taking decisions based on hypothetical average conditions

ZigBee

ZigBee, pioneered by the ZigBee Alliance, originated in 1998 and is based on the IEEE 802.15.4 standard. It can support a large number of nodes, providing a low-cost network.

The IEEE standard defines the physical (PHY) layer as well as the addressing and control (MAC) layers with ZigBee adding the network and application layers, application profile and security mechanism. ZigBee power consumption is minimal, allowing a longer battery life. The technology also supports functionalities for channel selection, link quality estimation, energy measurement and clear channel assessment.

There are three ZigBee topologies: star, mesh and cluster, as shown in Figure 2. In the star topology, each end-node is connected to the ZigBee coordinator (ZC), which handles all communication.

In the mesh topology, each device communicates with any other within its radio range or through multi-hopping; whereas in the cluster arrangement, there is a single routing path between devices.

ZigBee is largely known for its mesh topology, so for our application of crop field monitoring we chose this topology at the 2.4GHz operating frequency.

Wireless Sensor Network (WSN)

The main difference between a wireless sensor network (WSN) and an RFID system is that RFID devices have no cooperative capabilities, whereas WSN allows different network topologies and multi-hop communication.

Wireless sensor nodes can reduce the time and effort required to monitor a particular environment. Sensor nodes can be placed in critical positions without the need for personnel, especially in hazardous situations. Such monitoring systems (see Figure 3) ensure quicker responses in adverse conditions, better quality control of the environment and lower labour costs. They also allow for remote measurement of factors such as temperature, humidity, atmospheric pressure, soil moisture

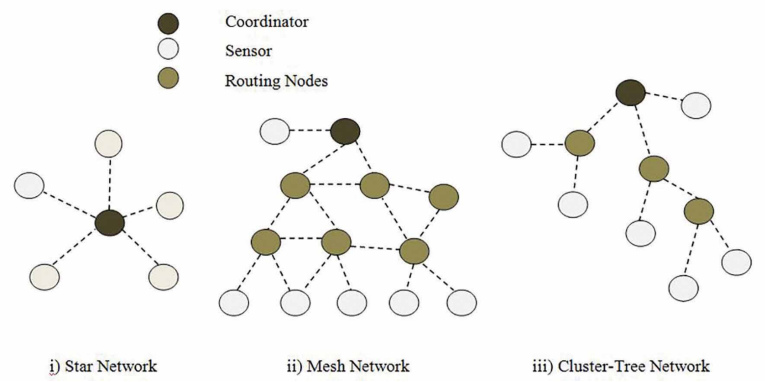

Figure 2: ZigBee topologies

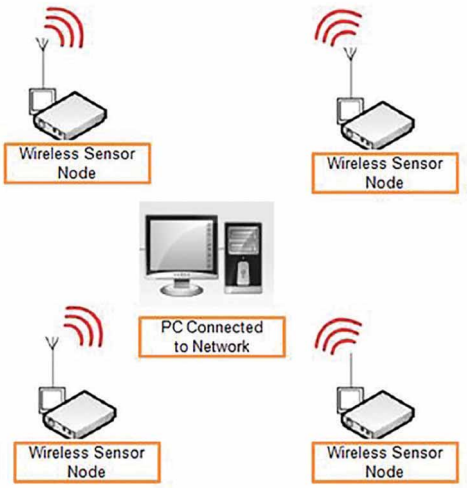

Figure 3: Concept of wireless monitoring in agriculture

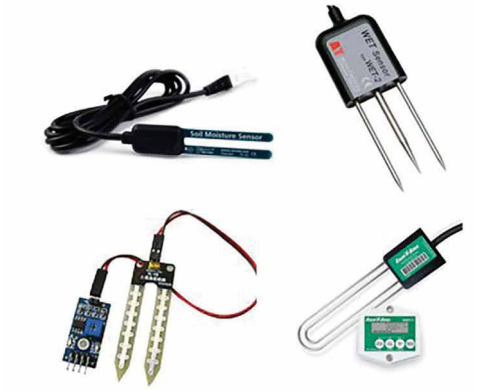

Figure 4: Types of moisture sensors

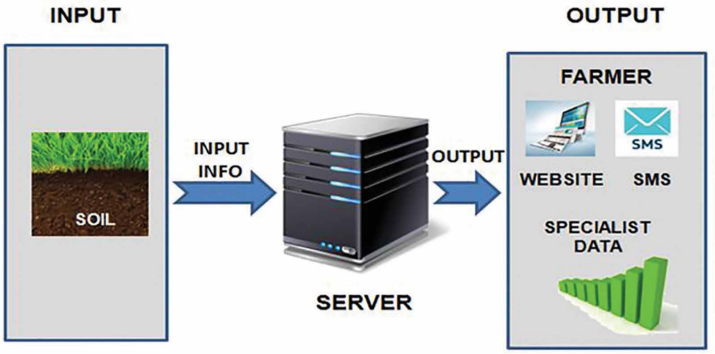

Figure 5: Input and output of the proposed system

(see Figure 4), water level and light detection, among others.

In our system, a sensor node and sprinkler will be combined. Table 3 shows the functionality of the sensor.

When the sensor detects low levels of water in the soil, sprinklers are turned on to supply more, and vice versa. The embedded sensors work on the principle of conductivity: wet soil conducts electricity easily (less resistance), whilst dry soil conducts electricity poorly (more resistance). Using embedded technology with moisture sensing helps reduce water consumption: water can be spared when not needed and the fields can be irrigated only when necessary, removing any guesswork or archaic methods of soil assessment.

The Proposed System

Our proposed irrigation management scheme using WSN and RFID can be applied from planting to harvest as a tool for an appropriate irrigation strategy to improve crop yields. Despite potential stressful environmental conditions, it increases the efficiency of an irrigation system by 50%.

Figure 5 shows the proposed system, where the server gets information from the soil and then processes the output.

The proposed concept is shown in Figure 6. Sprinkler, active RFID and moisture sensor are embedded together, becoming one node.

Figure 7 shows the data that will show in the monitoring base station, also capturing the time and date of the readings. The sensor in the 0-30% range sets off the sprinkler to supply a larger volume of water, since the soil is in a dry state. The sensor in the range of 30-70% senses some moisture in the soil, reducing the sprinkler's water supply by 50%, saving a tremendous amount of water. The sprinkler stops supplying water altogether when the moisture sensors send data of about 85-95%, since in this condition the soil is wet so there is no need for more water.

The conventional method uses the same amount of water to irrigate every day. Over-irrigation can cause crop damage or death and water wastage, and it's labour-intensive and time-consuming.

ITEM	CONDITION	MIN	TYPICAL	MAX	AMOUNT OF WATER
OUTPUT	Sensor in dry soil	0%	~	30%	High
	Sensor in humid soil	30%	~	70%	Medium
	Sensor in water	70%	~	85%	Low
	Sensor in water	85%	~	95%	None

Table 3: System operation examples

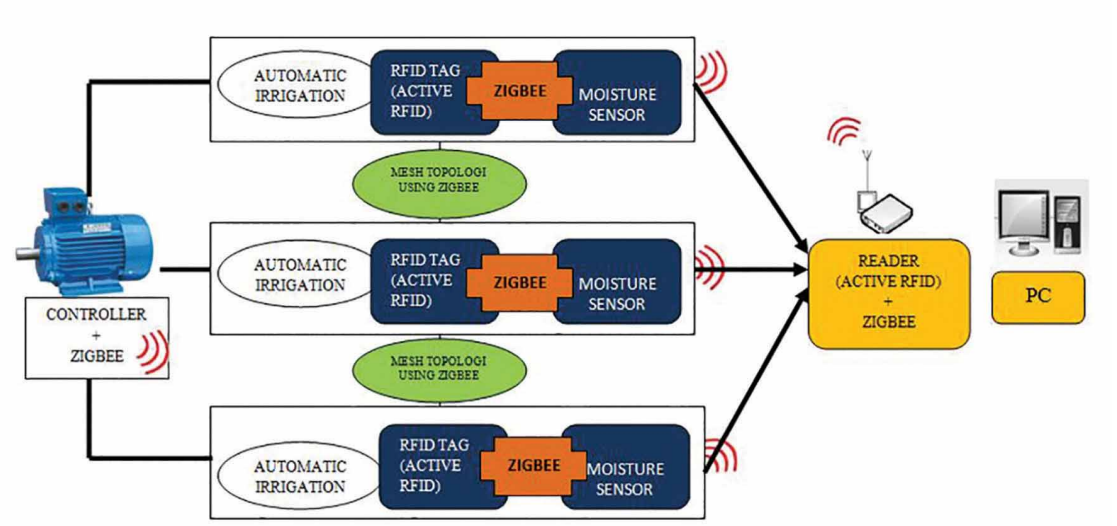

Figure 6: The proposed system

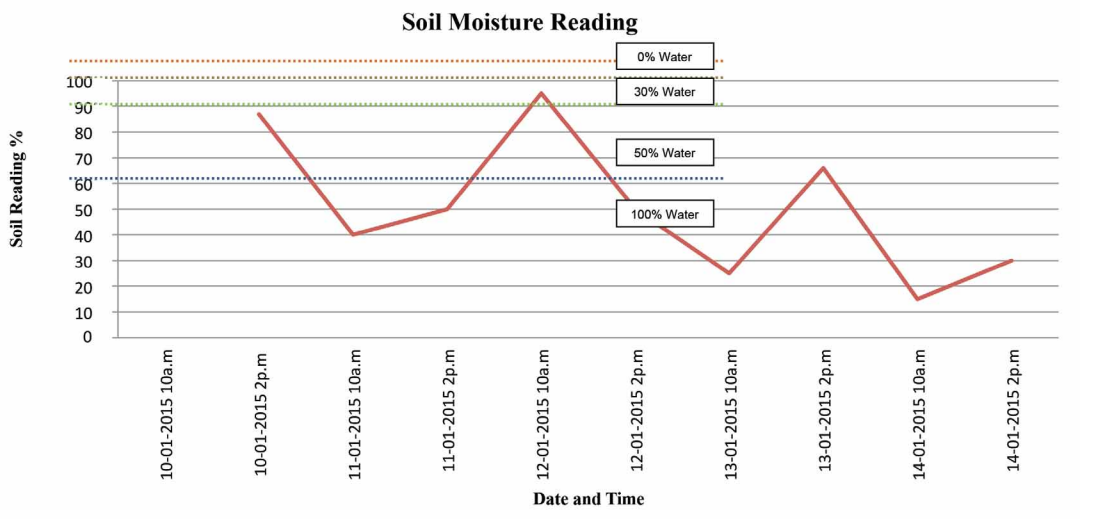

Figure 7: Data collected from the wireless sensor node; y axis is the soil reading in %

WSN also eliminates the need to wire sensor stations across the field and reduces maintenance costs. Since installation of WSN is easier than existing wired solutions, sensors can be more densely deployed to provide detailed local data.

The development of WSN applications in agriculture makes it possible to increase efficiency, productivity and profitability while minimizing unintended negative impacts on the environment.

NEW MODEL FOR ON-CHIP STACKED TRANSFORMERS THAT INCLUDES AN LR AND LRC SERIES BRANCHES

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Integrated transformers are widely adopted to implement resonant loads and to perform single-to-differential-ended and differential-to-single-ended conversions needed in integrated circuit (RFIC) designs. More recently, on-chip monolithic stacked transformers have received great attention in this field, because of their high quality and area-efficient performance. But, on-chip stacked transformers require accurate lumped-element models suitable for circuit simulation and design optimization.

A variety of compact transformer models and circuit extraction approaches have been proposed in recent years, such as models based on layout and process specifications, models that consider skin and substrate effects and so on. But none of the commonly used transformer models include higher-order effects with increasing frequency, which may result in underestimated power consumption.

Accurate Modeling

Key to accurate modeling is the ability to identify the loss mechanisms in a transformer, including mutual inductive couplings and their effects. In some cases, modeling work has been limited to extraction and curve fitting from measured data.

We developed a new lumped-element circuit model of two-port stacked transformers, discussed here. The model accurately captures conductor losses in the transformer windings and substrate parasitic losses. Model components are calculated with analytical extraction from two-port S-parameter measurements.

Figure 1 shows the circuit topology of a stacked transformer, coupled with two single π models. Here, R_{i0} (i = p, s) accounts for the spiral coil's conductor loss in the substrate return path, and C_{i0} (i = p, s) is the sum of the coupling capacitance between adjacent metal tracks and the overlap capacitance between the spiral and underpass metal lines.

DC current is uniformly distributed inside the conductor, characterized by R_i and L_i (i = p, s). As the frequency goes up, skin and proximity effects will push the AC current to the metal surface, and an additional LR and LRC ladder in parallel to the R_i and L_i is needed to capture the conductor's different current densities. The magnetic couplings between two coils are represented by L_m.

The conventional substrate parasitic can be modeled by C_{ox}, C_{sub} and R_{sub}, with C_{ox} being the metal-oxide

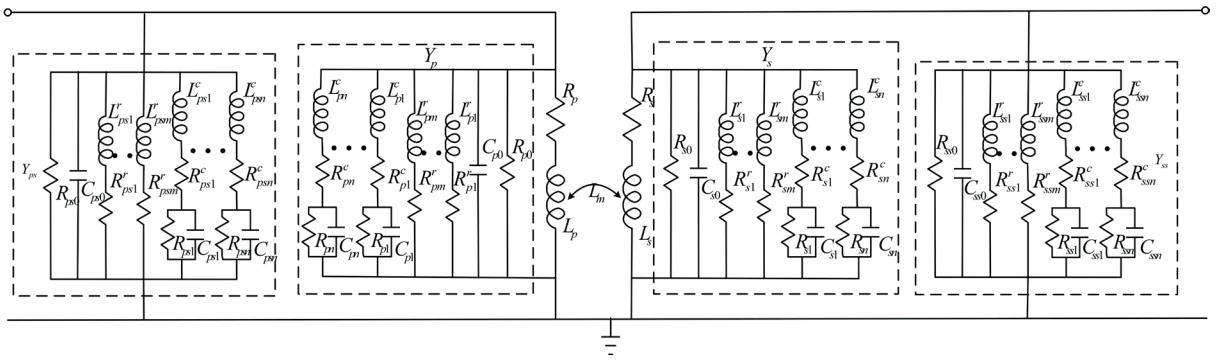


Figure 1: New, compact model for transformers

capacitance and C_{sub} and R_{sub} the substrate capacitance and resistance.

For high-order effects in the substrate, such as eddy currents, characterizing capacitive and resistive coupling alone is not enough. As shown in Figure 1, a new block (Y_i (i = ps, ss)) was introduced to model the substrate's parasitic losses, R_{i0} (i = ps, ss) for substrate resistance, and C_{i0} (i = ps, ss) is the capacitance between the metal-oxide and substrate. *LR* and *LRC* series branches were used to account for the high-order effects. Adding more branches will describe the high-order effects even more accurately.

For convenience, the portions including R_{i0}, C_{i0}, *LR* and *LRC* in the series branch of the equivalent circuit will be denoted by Y_i (i = p, s, ps, ss).

Parameter Extraction

Using decoupling technology and other simple transformation steps, we can see the 2-port topology with two back-to-back cascading π cells shown in Figure 2 where $[A]=\begin{pmatrix} A & B \\ C & D \end{pmatrix}$ is the ABCD matrix for the entire device. Using conversions between the 2-port network parameters, we can determine

$$A = \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} \quad (1)$$

$$B = Z_0\frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \quad (2)$$

$$C = \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2Z_0S_{21}} \quad (3)$$

$$D = \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \quad (4)$$

where Z_0 is the characteristic impedance of the test ports; the values of the *S*-matrix can be obtained from the 2-port measurement.

The ABCD matrix of the 2-port network equals the product of two cascading cell ABCD matrices, therefore:

$$[A]=\begin{pmatrix} A & B \\ C & D \end{pmatrix}=[A_1]\times[A_2]=\begin{pmatrix} a_1 & b_1 \\ c_1 & d_1 \end{pmatrix}\times\begin{pmatrix} a_2 & b_2 \\ c_2 & d_2 \end{pmatrix} \quad (5)$$

where $[A_1]=\begin{pmatrix} a_1 & b_1 \\ c_1 & d_1 \end{pmatrix}$ and $[A_2]=\begin{pmatrix} a_2 & b_2 \\ c_2 & d_2 \end{pmatrix}$ are the ABCD matrices of the two back-to-back cascading π cells. According to the definition of the ABCD matrix, then:

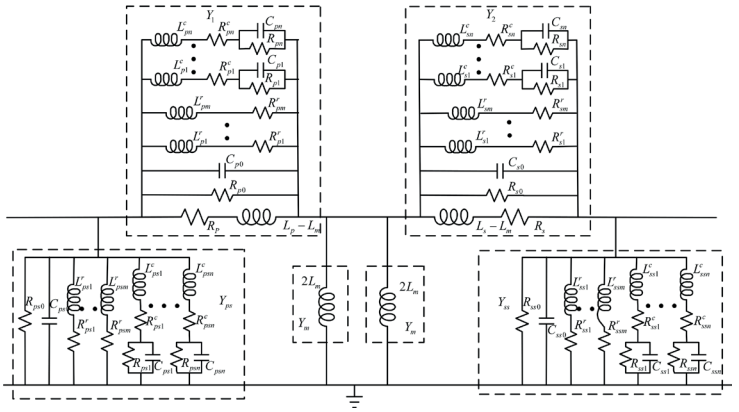


Figure 2: Model with two back-to-back cascading π cells

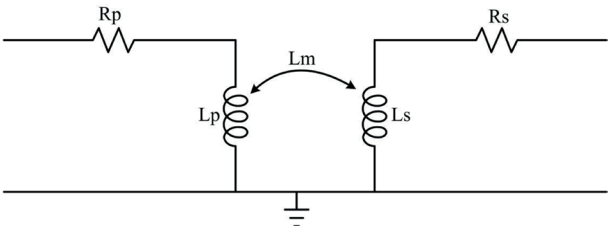


Figure 3: Model for low frequencies

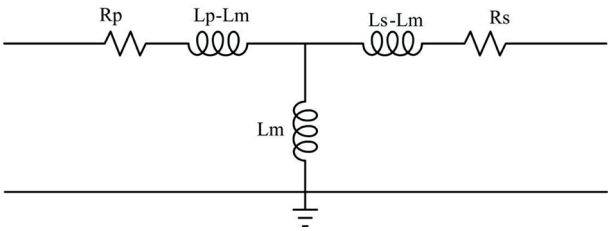


Figure 4: Decoupled conversion

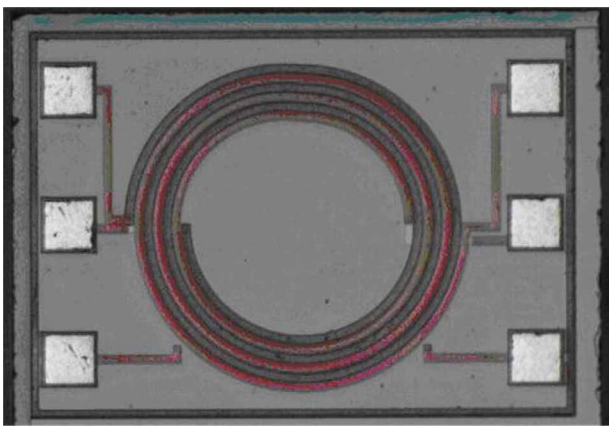


Figure 5: Top view of the fabricated on-chip transformer

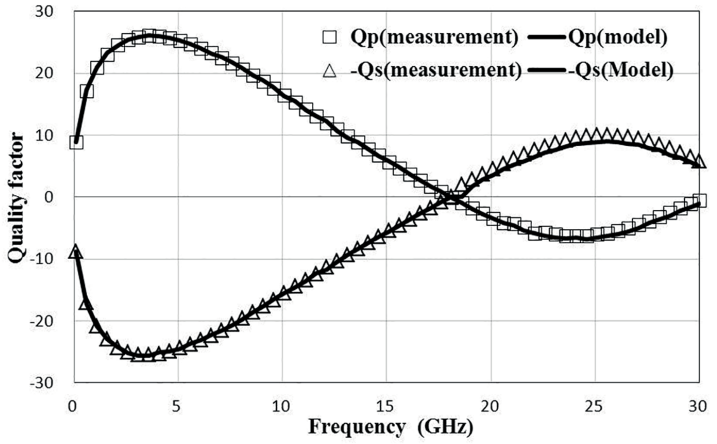


Figure 6: Quality factor comparison

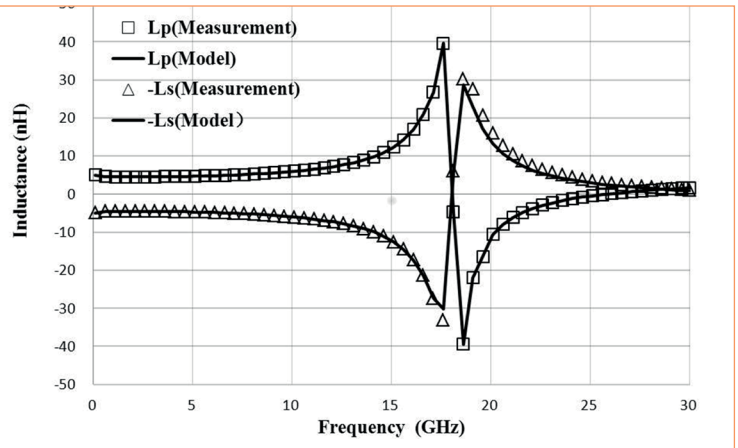


Figure 7: Inductance comparison

$$[A_1]=\begin{pmatrix} a_1 & b_1 \\ c_1 & d_1 \end{pmatrix}=\begin{pmatrix} 1+\frac{Y_m}{Y_1} & \frac{1}{Y_1} \\ Y_{ps}+Y_m+\frac{Y_{ps}Y_m}{Y_1} & 1+\frac{Y_{ps}}{Y_1} \end{pmatrix} \quad (6)$$

$$[A_2]=\begin{pmatrix} a_2 & b_2 \\ c_2 & d_2 \end{pmatrix}=\begin{pmatrix} 1+\frac{Y_{ss}}{Y_2} & \frac{1}{Y_2} \\ Y_{ss}+Y_m+\frac{Y_{ss}Y_m}{Y_2} & 1+\frac{Y_m}{Y_2} \end{pmatrix} \quad (7)$$

From Equations 5-7, we can determine:

$$Y_{ps}=\frac{A+Dk-\sqrt{A^2-2ADk+k(4+D^2k+8BY_m)}}{2Bk} \quad (8)$$

$$Y_{ss}=kY_{ps} \quad (9)$$

$$Y_1=\frac{(2-A+Dk)Y_m+\sqrt{Y_m^2[A^2-2ADk+k(4+D^2k+8BY_m)]}}{-1+A+k-Dk+2BkY_m} \quad (10)$$

$$Y_2=\frac{[A-(-2+D)k]Y_m+\sqrt{Y_m^2[A^2-2ADk+k(4+D^2k+8BkY_m)]}}{1-A-k+Dk+2BY_m} \quad (11)$$

where k represents the ratio of two coils without the fringing effect; Y_m can be determined at DC frequency. At low frequencies, the physical transformer model can be described as shown in Figure 3. Here, R_i and L_i (i = p, s) are the DC resistance and inductance of the corresponding coils respectively, and L_m is the mutual inductance between the primary and secondary coils. We can easily convert this π-topology to the T topology shown in Figure 4. Then we can determine R_i, L_i (i = p, s) and L_m as:

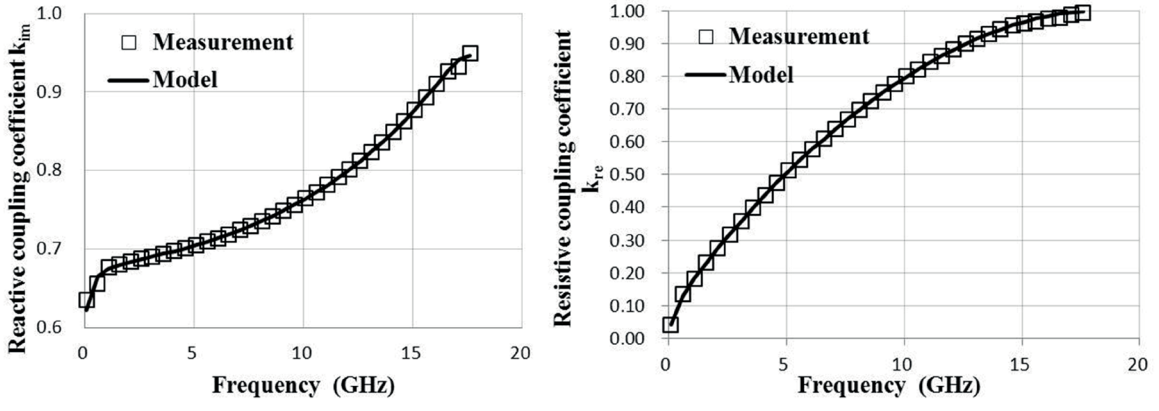


Figure 8: Coupling coefficient comparison

$$L_m = \left.\frac{im\left[(Z_{12}+Z_{21})/2\right]}{w}\right|_{w\to 0} \tag{12}$$

$$R_i = re(Z_{ii}-Z_{12})\big|_{w\to 0}\ (i=p,s) \tag{13}$$

$$L_i = L_m + \left.\frac{im(Z_{ii}-Z_{12})}{w}\right|_{w\to 0}\ (i=p,s) \tag{14}$$

Circuit parameter extractions for this model consist mainly of Y_p, Y_s , Y_{ps} and Y_{ss}. When the elements L_p, R_p, L_s, R_s and L_m are extracted, Y_i (i = p, s) can be calculated by using

$$Y_p = Y_1 - \frac{1}{R_p + jw(L_p - L_m)} \tag{15}$$

$$Y_s = Y_2 - \frac{1}{R_s + jw(L_s - L_m)} \tag{16}$$

Expanding the admittance Y_i (i = p, s, ps, ss) with the pole-residue formulation will simply implement the extraction.

$$\begin{aligned} Y(s) &= d + se + \sum_{i=1}^{m}\frac{r_i^r}{s-p_i^r} + \sum_{i=1}^{n}\frac{r_i^c}{s-p_i^c} + \frac{r_i^c 0}{s-p_i^c} \\ &= d + se + \sum_{i=1}^{m}\frac{r_i}{s-p_i} + \sum_{i=1}^{n}\frac{\lambda_i s+\gamma_i}{s^2+\alpha_i s+\beta_i} \end{aligned} \tag{17}$$

In Equation 17, d, e, r_i and p_i are real, p_i^c, p_i^c, r_i^c and r_i^c complex, while α_i 、 β_i 、 γ_i and λ_i are real parameters.

In order to synthesize a lumped equivalent circuit by $Y(s)$, Y_j (j = p, s, ps, ss) is expressed by R, L, C as:

$$\begin{aligned} Y_j(s) &= \frac{1}{R_{j0}} + sC_{j0} + \sum_{i=1}^{m}\frac{1/L_{ji}^r}{s+R_{ji}^r/L_{ji}^r} \\ &+ \sum_{i=1}^{n}\frac{(1+L_{ji}^c)s + 1/L_{ji}^c C_{ji} R_{ji}}{s^2 + (R_{ji}^c/L_{ji}^c + 1/C_{ji}R_{ji})s + (1+R_{ji}^c/R_{ji})/(L_{ji}^c C_{ji})} \end{aligned} \tag{18}$$

The superscripts r and c stand for real and complex poles. The order of real poles and complex poles are m and n. Compared with $Y(s)$, the R, L, C components of the circuit in Figure 1 can be determined using:

$$\left.\begin{aligned} R_{j0} &= 1/d \\ C_{j0} &= e \end{aligned}\right\}(j=p,s,ps,ss) \tag{19}$$

$$\left.\begin{aligned} L_{ji}^r &= 1/r_i^r \\ R_{ji}^r &= -p_i^r/r_i^r \end{aligned}\right\}(j=p,s,ps,ss;i=1\mathrm{L}\ \ m) \tag{20}$$

$$\left.\begin{aligned} L_{ji}^c &= 1/\lambda_i \\ R_{ji}^c &= L_{ji}^c(\alpha_i - L_{ji}\gamma_i) \\ R_{ji} &= \beta_i/\gamma_i - R_{ji}^c \\ C_{ji} &= 1/L_{ji}^c R_{ji}\gamma_i \end{aligned}\right\}(j=p,s,ps,ss,i=1\mathrm{L}\ \ n) \tag{21}$$

and, as such, all elements in Y_p, Y_s, Y_{ps} and Y_{ss} can be determined. This method was then implemented in the MATLAB environment using the VF (vector fitting) approach.

Model Verification

For verification, a 1:1 stacked transformer with din = 130µm, w = 10µm and s = 2µm was fabricated using 0.5µm L50G CMOS process. The transformer primary coil is placed on the top layer and the second coil on the other layer. The measured S-parameter is determined with a two-step (open and short) procedure to cancel out undesired pad parasitics.

The model's accuracy in a wide frequency range is further confirmed by the comparisons shown in Figures 6-8. In Figures 6 and 7, we compare the curves of $-L_s$ and $-Q_s$ instead of L_s and Q_s for better clarity. The RMS deviations of the simulated Q_p and Q_s in Figure 6 are less than 3.46%, and that of the simulated L_p and L_s in Figure 7 are less than 7.53%.

The chosen frequency range for the RMS calculation is 0.1-30GHz.The relative deviation is lower than 3.47% for the DC inductance L, and below 2.84% for the peak value of Q. Moreover, Figure 7 shows the accuracy of the adopted lumped model in terms of k_{re} and k_{im} up to the self-resonant frequency.

As shown in these figures, there's excellent agreement over a broad frequency band, showing that the model in Figure 1 is an accurate and highly efficient model for these types of transformers over a broad frequency range. ●

FLEXIBLE GLASS FOR PRINTED ELECTRONICS

The special glass expert Schott showed its ultra-thin glasses that enable various functionalities in printed electronic components as a flexible substrate material at the international trade fair for printed and organic electronics LOPEC 2016 in Munich in April. Schott also unveiled its plans to transfer ultra-thin glass substrates into mass production for applications in organic and printed electronics with development partners.

With thickness of only 25 micrometers (microns), these innovative glasses are thinner than a human hair, flexible and yet robust, and offer many advantages over other substrate materials such as plastics, metals or silicon.

The ultra-thin glasses from Schott combine the classic chemical, physical and mechanical advantages of the inorganic material of special glass.

www.schott.com

VERSASENSE PRESENTS MICROPNP AT HANNOVER MESSE

VersaSense showed live demonstrations of its award-winning MicroPnP product range at the end of April at Hannover Messe, on the Linear Technology Stand H23, Hall 9.

MicroPnP is based on SmartMesh IP embedded networking and uses Internet of Things (IoT) technologies to realize zero-configuration wireless sensing and actuation at a significantly lower price-point than traditional wired solutions.

MicroPnP is a complete IoT hardware and software platform that dramatically reduces the total cost of ownership for sensing and control systems. It provides a unique proposition through its true plug-and-play identification of sensors and actuators at 10 million times lower power than USB, and ultra-reliable networking through SmartMesh IP from Linear Technology (> 99.999% end-to-end reliability).

www.versasense.com; www.linear.com

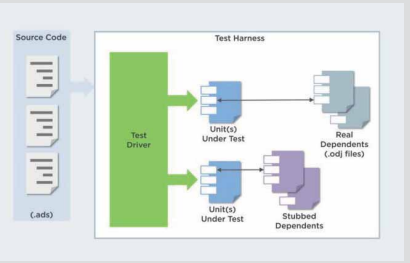
MOST COMPREHENSIVE ADA SOFTWARE QUALITY SOLUTION

Vector Software announced its latest release of VectorCAST/Ada, a dynamic software test solution that automates Ada unit, integration and system testing, necessary for validating safety-critical embedded systems.

The newest release includes stubbing of functions that is dynamically controlled on a per-test-case basis, built-in change-based testing functionality for a quick and easy assessment of the impact of a source code change, code coverage analysis to gauge the effectiveness of tests and four versions of the Ada language standard: Ada 83, Ada 95, Ada 2005 and Ada 2012.

"Organizations developing safety-critical applications require tools that help them improve time-to-market and reduce development and verification costs through structural code coverage analysis," said John Paliotta, Vector Software's CTO.

www.vectorcast.com



ULTRA-LOW IQ BUCK REGULATOR FOR AUTOMOTIVE INFOTAINMENT

The new A8591 from Allegro MicroSystems Europe is a buck regulator IC designed to meet the power supply requirements of the latest automotive infotainment systems. It is available in fixed 5V or 3.3V regulated output voltage configurations.

The new AEC-Q100 qualified device provides all the control and protection circuitry of a 2A regulator circuit with ±1% output voltage accuracy; an ultra-low-IQ mode employs pulse-frequency modulation (PFM) to draw less than 33µA from a 12V input while supplying a 5V/40µA output, making the A8591 ideal for automotive battery-powered "keep-alive" applications. A "sleep" feature is included which reduces the standby current down to 5µA.

The A8591 operates to at least 3.6V input to accommodate idle-stop battery input requirements. The regulator PWM switching frequency can be set between 300kHz and 2.4MHz and "dithered" or synchronised to an external clock.

www.allegromicro.com

HIGH-PERFORMANCE UNCOOLED THERMAL CAMERA CORE

FLIR Systems announced Boson, its smallest, lightest and least power-consuming, high-performance uncooled thermal camera for OEMs. Sized between FLIR's Tau and Lepton camera cores, Boson is the first thermal camera core to incorporate a sophisticated, low-power multi-core vision processor based on the FLIR XIR expandable infrared video processing architecture.

Boson features a high-sensitivity 12-micron pixel pitch detector that provides high-resolution thermal imaging in a small, low power, lightweight, turnkey package. It also offers several levels of video processing with inputs, and processing for other sensors including visible CMOS imaging sensors, Global Positioning Systems (GPSs) and Inertial Measurement Units (IMUs). Additionally, FLIR XIR offers a suite of advanced image processing features including super resolution algorithms, sophisticated noise reduction filters, local area contrast enhancement and image blending.

www.flir.com

RED PRICE THRESHOLD FOR 64-BIT X86 COMPUTING

Congatec has introduced new and highly cost-effective versions of its existing COM Express and Qseven modules as well as Mini-ITX boards. They are all equipped with the strategically low-priced, long-term available Intel Atom x5-E8000 processor. This 64-bit quadcore processor significantly lowers the entry threshold of powerful x86 computing and, now also in terms of price, offers developers a true alternative to competing platforms based on ARM technology.

Target applications of the new price-breaking embedded computers for x86 technology are very diverse and range from embedded mobile devices, industrial gateways, terminal, ticket and cash register systems in the retail segment to gaming machines and digital signage systems. Other fields of applications can also be found in compact industrial PCs as well as medical devices and systems in the transport sector.

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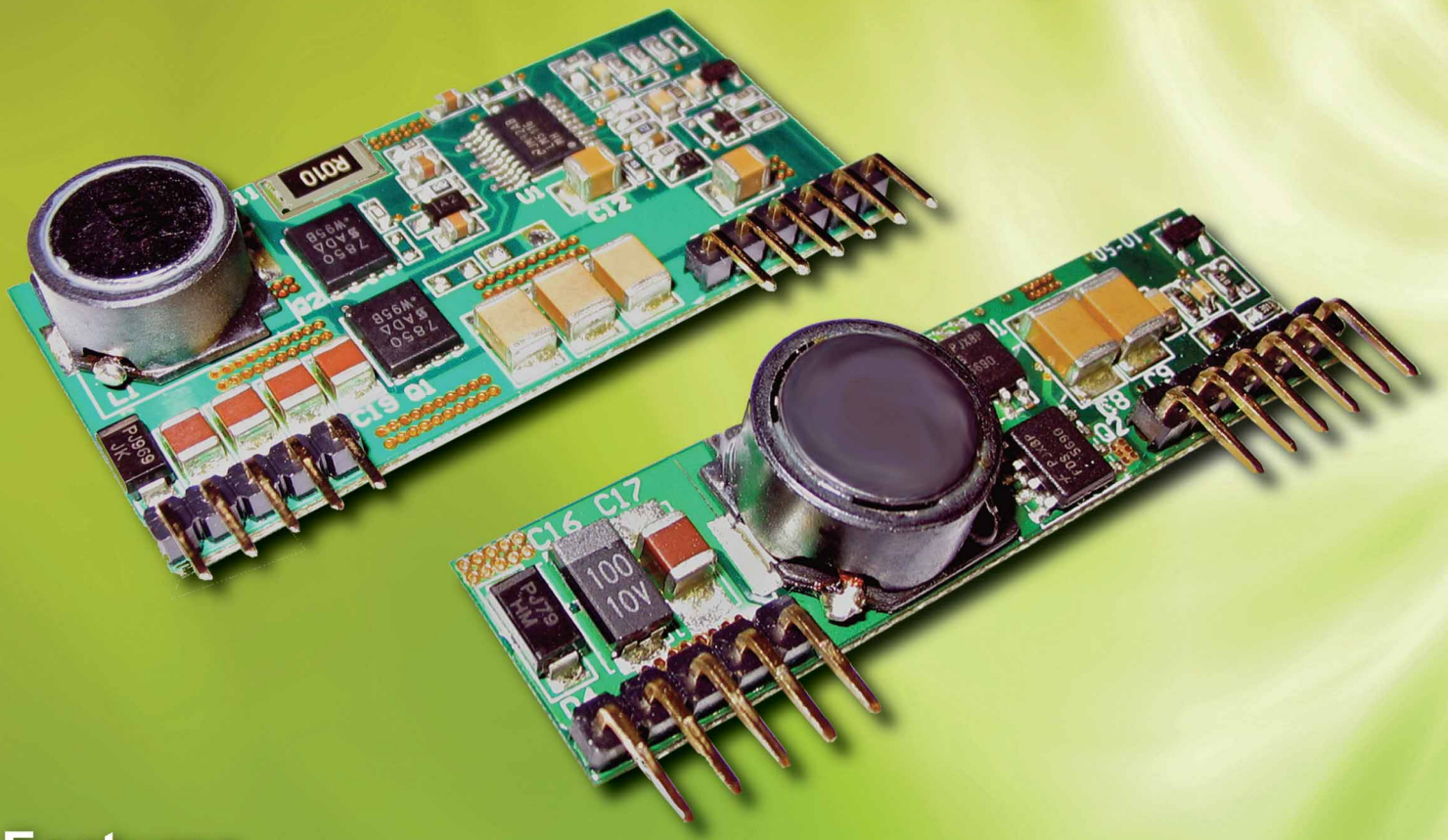

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