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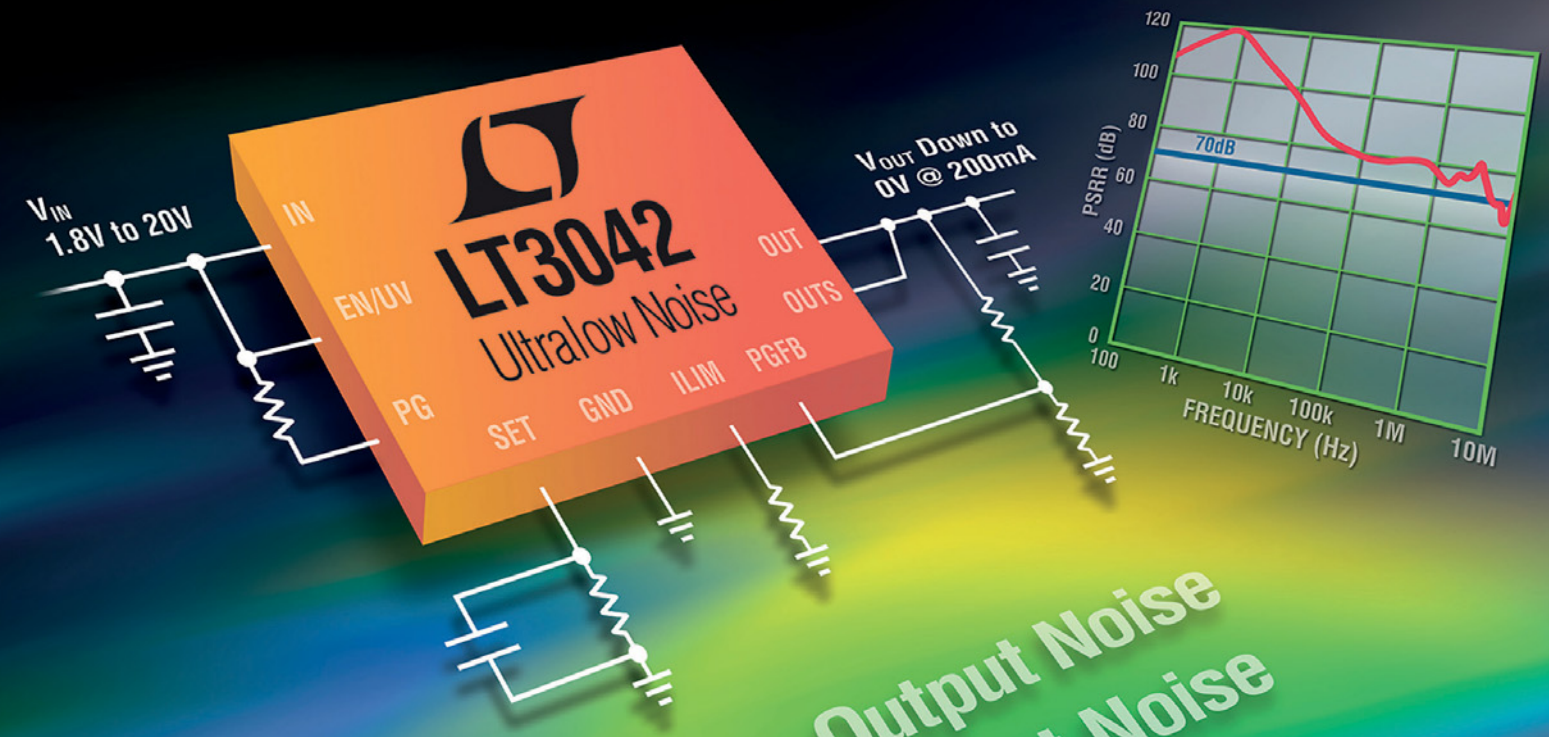
THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Powering Noise-Sensitive Analog/RF Applications

by Linear Technology



0.8μVRMS Output Noise

2nV/√Hz Spot Noise

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- Parasitics
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Whiter than white – a new generation of LEDs

NEW Regular column:
Embedded design

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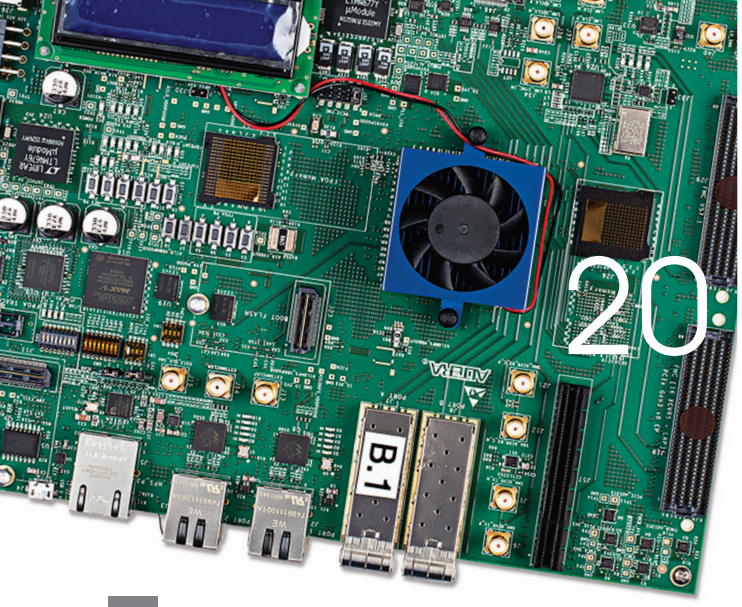
Latest generation of oscilloscopes and 'scope features



REGULARS

Cover supplied by LINEAR TECHNOLOGY
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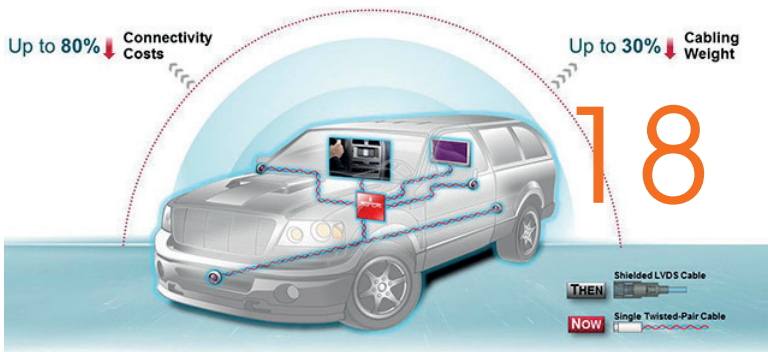
FEATURES



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PS12MK-12	12VDC 1.0A	PS20MK-12	12VDC 1.5A	PS36MK-12	12VDC 3A
PS12MK-15	15VDC 0.8A	PS20MK-15	15VDC 1.2A	PS36MK-15	15VDC 2.4A
PS12MK-24	24VDC 0.5A	PS20MK-24	24VDC 0.83A	PS36MK-24	24VDC 1.5A

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DISRUPTIVE TECHNOLOGIES DRIVE AUTOMOTIVE LIGHTING INDUSTRY GROWTH

> Automotive OEMs not only have to remain focused on their core competencies but they also have to develop new ones to remain competitive

The car is not just a simple mode of transport any more. In addition to security and autonomous driving features, car manufacturers are considering more and more functionalities to promote vehicles as custom and fashion items.

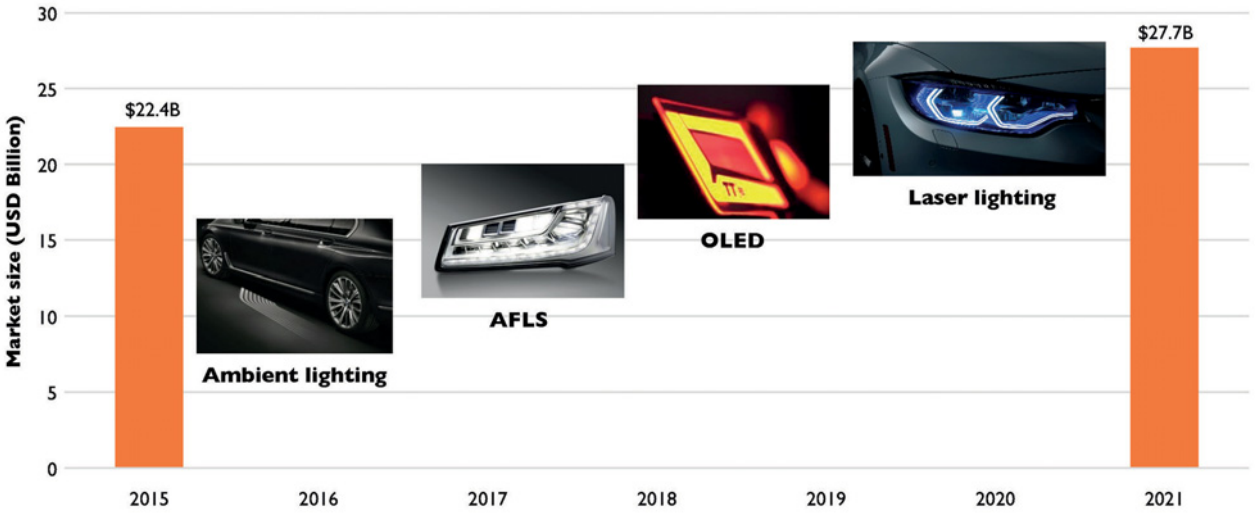
During the last few years, the progress of electronic, optoelectronic, software and various digital technologies, along with social changes, have added additional pressure on car manufacturers to transform their offerings and business models faster than ever before. In this context, automotive OEMs not only have to remain focused on their core competencies, but also develop new ones to remain competitive. One field where they might be requiring specific expertise is automotive lighting.

The lighting market for automotive applications will reach a compound annual growth rate (CAGR) of 23.7% by 2021, becoming nearly a $28bn market, according to French analysis house Yole Développement, that prepared a report on this subject, called *"Automotive Lighting: Technology, Industry and Market trends"*.

The growing role of design in automotive lighting and the introduction of new functionalities such as ambient, rear, fog, turn signal, parking, low/high beam and day-running lights are seen as the main reasons for their success.

In its report, Yole discusses the companies behind this growth, type of lighting technologies available – LEDs, OLEDs, halogen lighting, etc., and their impact on the supply chain, but also which one of these are likely to address market needs the most.

Automotive lighting market size 2015-2021



Yole Développement is an industry analysis house based in Lyon, France (www.yole.fr)

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DECADES-OLD LED COLOUR CONSISTENCY PROBLEM SOLVED BY EYE 'CONES' RESEARCH

Osram Opto Semiconductors has applied the latest findings of physiological research into how the human eyes perceive colour to solve an 85-year-old challenge of why the same light from two different LED light sources measured to be exactly the same can still appear different.

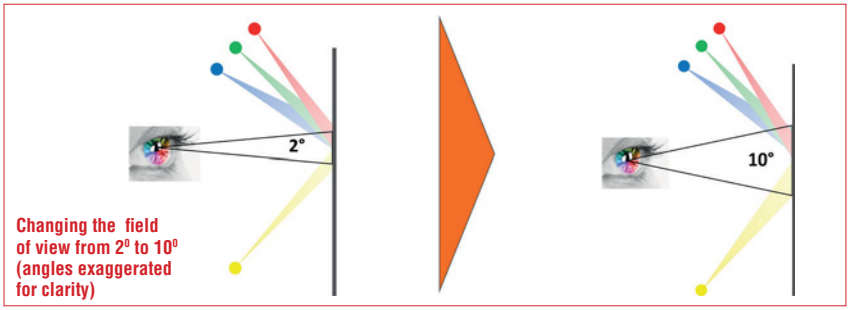
The phenomenon of colour perception versus reality colour measurement of different light sources has been well-known to scientists for decades. In general lighting, this occurs when there are several LED white light sources in the same space, such as spotlights, wallwashers and downlights.

In 2015 the International Commission of Illumination (CIE 170-2:2015) published a new colour space based on extensive research. Beside the physiological meaningful axis of the colour space, the most important improvement is the definition for a 10° observer view. Osram has applied these findings to the general lighting market with significant success.

"Colour coordinates in general lighting are typically measured with the CIE 1931 2° colour space. It is assumed that the blue, green and red cones that are responsible for colour perception in our eyes are evenly distributed and that the colour perception over viewing angle is constant. In reality this is not the case, and pigment density varies significantly over the field of view's size," said Alexander Wilm, Applications Manager at Osram Opto Semiconductors. "Most people have had this peculiar experience without realising, and it has a big impact on many markets. In retail and museum applications, for example, colour inconsistency is not an option and is often unpleasant, as it doesn't show an object in the best possible and consistent illumination. The world's greatest modern artists also want their work to be viewed as they had originally intended."

Osram solved the problem by complementing the CIE 1931 2° xy colour space with the CIE 2015 10° u'v'. By assessing the colour consistency not only at 2° field of view but also at a significantly larger 10° field of view, the measurement and binning – when LEDs' variety of factors are measured for each individual component under the exact same conditions regarding temperature voltage, etc – provides a more accurate assessment of colour discrepancies under realistic observation conditions.

The resulting TEN° binning feature has already been implemented in Osram's new Soleriq S 13 LED type, achieving unprecedented colour consistency under LED lighting.



Changing the field of view from 2^0 to 10^0 (angles exaggerated for clarity)

GOOGLE ATAP AND INFINEON ADVANCE THEIR PARTNERSHIP IN "SOLI" RADAR TECHNOLOGY

Gesture-controlled smartwatch and wireless speaker were demonstrated at "Google I/O" for the first time in May in Mountain View, California. Both devices use technologies from Infineon Technologies and Google ATAP to recognize gestures that completely replace switches and buttons.

"Gesture sensing offers a new opportunity to revolutionize the human-machine interface by enabling mobile and fixed devices with a third dimension of interaction," said Ivan Poupyrev, Technical Project Lead at Google ATAP. "This will fill the existing gap with a convenient alternative to touch- and voice-controlled interaction."

Infineon and Google ATAP believe gesture-controlled devices are a perfect fit for home entertainment, mobile devices and the Internet of Things (IoT). The jointly developed 'Soli' technology uses radar chips from Infineon and Google ATAP's software and interaction protocols.

"Sophisticated haptic algorithms combined with highly integrated and miniaturized radar chips can foster a huge variety of applications," said Andreas Urschitz, President of the Power Management and Multimarket division at Infineon. "Our goal is to create a new market standard with compelling performance and new user experience, developing a core technology to enable augmented reality and IoT."

Infineon and Google ATAP are addressing the home entertainment, mobile devices and Internet of Things (IoT) markets with the "Soli" gesture-recognition technology

Whilst virtual reality technologies could already visualize new realities, users could not interact with these realities. The 60GHz radar application developed by Google and Infineon bridges that gap, acting as the technology at the heart of the new-generation augmented reality.

"Since mankind started using tools over two million years ago, this is the first time in history that tools adapt to their users, rather than the other way round," added Urschitz.

POWERING NOISE-SENSITIVE ANALOG/RF APPLICATIONS

By Amit Patel, Senior Design Engineer, Power Products, Linear Technology Corporation

When it comes to powering noise-sensitive analog/RF applications, low dropout (LDO) linear regulators are generally preferred over their switching counterparts. Low-noise LDOs power a wide range of analog/RF designs, including frequency synthesizers (PLLs/VCOs), RF mixers and modulators, high-speed and high-resolution data converters (ADCs and DACs) and precision sensors. Nevertheless, these applications have reached capabilities and sensitivities that are testing the limits of conventional low-noise LDOs.

For instance, in many high-end VCOs, power supply noise directly affects the VCO output phase noise (jitter). Moreover, to meet overall system efficiency requirements, the LDO usually post-regulates the output of a relatively noisy switching converter, so the high-frequency power supply rejection ratio (PSRR) performance of the LDO becomes paramount.

With its ultralow output noise and ultrahigh PSRR performance, the LT3042 can directly power some of most noise-sensitive applications while post-regulating the output of a switching converter, without requiring bulky filtering.

Performance, Robustness & Simplicity

The LT3042 is a high-performance low-dropout linear regulator featuring Linear Technology's ultralow noise and ultrahigh PSRR architecture for powering noise-sensitive applications. Even with its high performance, the LT3042 maintains simplicity and robustness. Figure 1 is a typical application and Figure 2 shows a complete demonstration circuit. The LT3042's tiny 3mm × 3mm DFN package and minimal component requirements keep overall solution size small.

Designed as a precision current reference followed by a high performance voltage buffer, the LT3042 is easily paralleled to increase output current, spread heat on the PCB and further reduce noise – output noise decreases by the square-root of the number of devices in parallel. Its current-reference-based architecture offers wide output voltage range (0V to 15V) while maintaining unity-gain operation, thereby providing virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage.

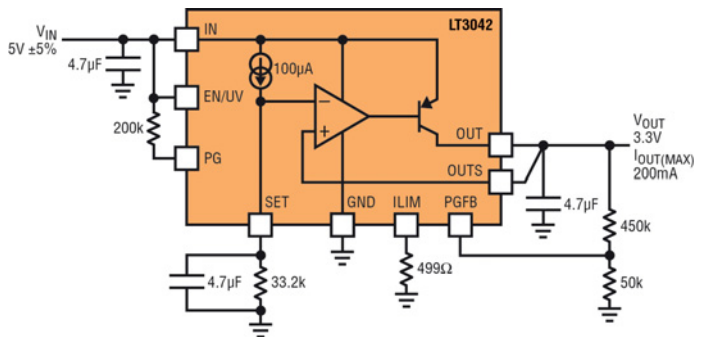


Figure 1: Typical LT3042 application

In addition to offering ultralow noise and ultrahigh PSRR performance, the LT3042 includes features desired in modern systems, such as programmable current limit, programmable power good threshold and fast start-up capability. Furthermore, the LT3042 incorporates protection features for battery-powered systems. Its reverse input protection circuitry tolerates negative voltages at the input without damaging the IC or developing negative voltages at the output – essentially acting as if an ideal diode is connected in series with the input. In battery backup systems where the output can be held higher than the input, the LT3042's reverse output-to-input protection circuitry prevents reverse current flow to the input supply. The LT3042 includes internal foldback current limit, as well as thermal limit with hysteresis for safe-operating-area protection.

Ultralow Output Noise

With its 0.8µVRMS output noise in 10Hz-100kHz bandwidth, the LT3042 is the industry's first sub-1µVRMS noise regulator. This opens up applications previously not possible, or otherwise required expensive and bulky filtering components.

The SET pin capacitor (CSET) bypasses the reference current noise, the base current noise (of the error amplifier's input stage) and the SET pin resistor's (RSET) inherent thermal noise. With a 22µF CSET, the output noise is under 20nV/√Hz at 10Hz. But, capacitors can also produce 1/f noise, particularly electrolytic capacitors. To minimize that, use ceramic, tantalum or film capacitors on the SET pin.

Actively driving the SET pin with either a battery or a lower noise voltage reference reduces noise below 10Hz. Doing so essentially eliminates the reference current noise at lower frequencies, leaving only the extremely low error amplifier noise. This ability to drive the SET pin is another advantage of the current-reference architecture. The integrated RMS noise also improves as the SET pin capacitance increases, dropping below 1µVRMS with just 2.2µF CSET.

Increasing SET pin bypass capacitance for lower output noise generally leads to increased start-up time, which is alleviated by the LT3042's fast start-up circuitry, easily configured using two resistors.

Ultrahigh PSRR Performance

LT3042's high PSRR is important when powering noise-sensitive applications. Unlike conventional LDOs, whose PSRR performance deteriorates into the 10s of dB as you approach dropout, the LT3042 maintains high PSRR at even low input-to-output differentials. LT3042 maintains 70dB PSRR up to 2MHz with only 1V input-to-output differential and almost 60dB PSRR up to 2MHz at a mere 600mV input-to-output differential. This capability allows the LT3042 to post-regulate switching converters at low input-to-output differentials – for high efficiency – while its PSRR performance satisfies the requirements of noise-sensitive applications.

Post-Regulating a Switcher

In applications where the LT3042 is post-regulating the output of a switching converter to achieve ultrahigh PSRR at high frequencies, care must be taken with the electromagnetic coupling from the switching converter to the output of the LT3042. In particular, while the "hot-loop" of the switching converter should be as small as possible, the "warm-loop" (with AC currents flowing at the switching frequency) formed by the switcher IC, output inductor and output capacitor (for a buck converter) should also be minimized, and it should either be shielded or placed a couple of inches away from ultralow noise devices like the LT3042 and its load. While the LT3042's orientation with respect to the warm-loop can be optimized for minimum magnetic coupling, in practice, it can be challenging to achieve 80dB of rejection simply with optimized orientation – multiple iterations of the PC board may be required.

Consider Figure 3, where the LT3042 is post-regulating the LT8614 Silent Switcher regulator running at 500kHz with an EMI filter at switching regulator input. With the LT3042 located just one to two inches from the switching converter and its external components, almost 80dB rejection at 500kHz is achieved without any shielding.

To achieve this performance, no additional capacitor – other than the 22µF at switcher's output – is placed at the input of the LT3042. However, even placing a small 4.7µF capacitor directly at the input of the LT3042 results in over 10× degradation in PSRR.

This is peculiarly counter-intuitive – adding input capacitance generally reduces output ripple – but at 80dB rejection, the magnetic coupling, which is usually insignificant, resulting from moderately high frequency (500kHz) switching currents flowing though this 4.7µF capacitor, significantly degrades output ripple. While changing the orientation of the 4.7µF input capacitor and the traces connecting the switcher's output to this capacitor help minimize magnetic coupling, it remains rather difficult to achieve nearly 80dB of rejection at these frequencies, not to mention the multiple PC board iterations it may require.

The relatively high input impedance of the LT3042 prevents high-frequency AC currents from flowing into its input terminal. Given that the LT3042 is stable without an input capacitor if located within three inches of the pre-regulating switching power supply's output capacitor, to achieve best PSRR performance, we recommend not placing a capacitor at the LT3042's input, or minimizing it.

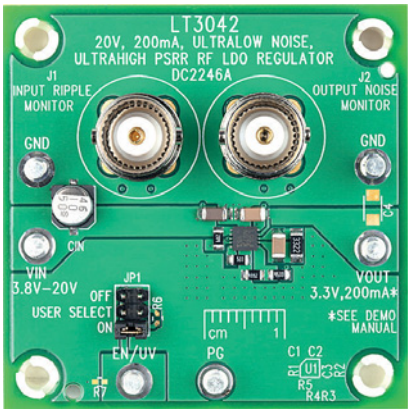


Figure 2: LT3042 demonstration circuit

A couple of inches of trace inductance connecting the LT8614 to the LT3042 input significantly attenuates the very high frequency power switch transition spikes. Some spikes still propagate to the output due to magnetic coupling from the LT8614's hot-loop. Optimizing the LT3042 board orientation reduces the remaining spikes.

For perspective, trying to achieve 80dB rejection at 500kHz without using the ultrahigh PSRR LT3042 LDO is a tall order. Alternatives don't measure up. For instance, an LC filter would require nearly 40µH of inductance and 40µF of capacitance to achieve 80dB rejection at 500kHz, adding large, expensive components. Costs and board real estate aside, the LC can resonate if not properly damped, adding complexity. Using an RC filter is untenable, requiring impractical resistance to achieve 80dB rejection. Similarly, using conventional LDOs require cascading at least two of them to achieve 80dB rejection at 500kHz, which requires additional components and cost, and degrades the dropout voltage. Additionally, these alternatives also require attention to magnetic field couplings; in particular, high-frequency AC currents must be minimized.

Owing to its ultrahigh PSRR over a wide frequency range, the LT3042 allows lower frequency operation of the upstream switching converter – for improved efficiency and EMI – without requiring any increase in filter component size for powering noise-sensitive applications.

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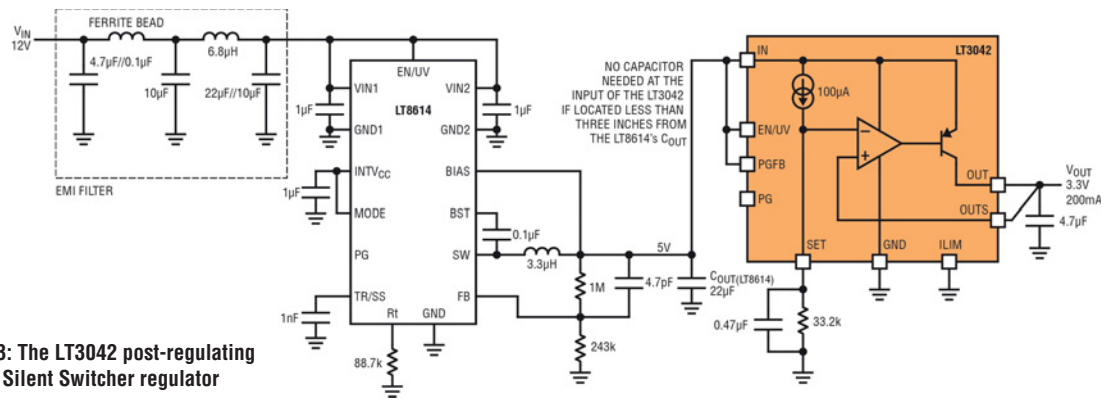


Figure 3: The LT3042 post-regulating LT8614 Silent Switcher regulator

Simplifying Capacitive Touch Sensing

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

Over the past ten years the progress in capacitive touch technology has been nothing short of spectacular. The technology is now a common requirement for many consumer, home appliances and automotive applications.

Whilst projective capacitive sensing is used in small and large (2D input) surfaces, and advanced DSP techniques are used to provide gesture recognition (3D input), the vast majority of capacitive sensing applications still revolve around much simpler solutions to replace a few buttons in a user interface, possibly with a slider (1D) or two. Here, despite the apparent simplicity, there seems to be an infinite appetite for customization defying any attempt by silicon manufacturers to standardize solutions around a few fixed-function devices.

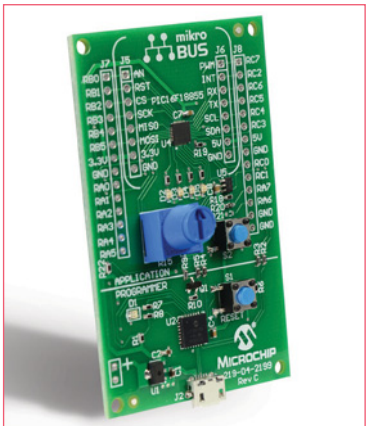


Figure 1: MPLAB Xpress Evaluation Board

Microcontrollers are used extensively to provide the required flexibility but the technology, whilst widely understood in its basic physics principles, is far from trivial in practice. Further, the precise nature of measurements and timings make capacitive sensing a rather core-/performance-intensive task.

This article will explore a novel approach to the problem using the Core Independent peripherals of modern microcontrollers to reduce the core workload and make the application not only simpler but also more accurate and responsive. We will use the MPLAB Xpress cloud toolchain (to avoid lengthy installations), the MPLAB Xpress evaluation board for rapid prototyping and the MPLAB Code Configurator (MCC) for a quick configuration of all required microcontroller peripherals.

Capacitive Sensing

When it comes to measuring accurately a (very small) capacitive value with a low-cost microcontroller, there are a number of techniques possible but, whilst most have been explored over the past decade, only a few have survived. The Capacitive Voltage Divider (or CVD) is the most prominent, used extensively and with excellent results by developers worldwide.

The physical principle at the root is the "conservation of charge". A reference capacitor of known value (C_o) is charged by applying a given voltage (V_o) to its plates. Laws of physics state that the charge Q present on its plates is now proportional to the product of the capacity C_o and applied voltage V_o.

$$\mathbf{Q = C_o * V_o}$$

A capacitor of unknown value (C_x) can first be discharged completely and later connected in parallel to the reference capacitor. Since charge is not destroyed or created in the process, the resulting parallel circuit will settle to a voltage proportional to the sum of the two capacitors $C_o + C_x$.

$$\mathbf{Q = (C_o + C_x) * V_x}$$

By measuring V_x we can deduce the value of the capacitor under measure:

$$\mathbf{C_x = C_o * (V_o/V_x - 1)}$$

In touch-sensing applications we are actually interested in the relative value of the capacitance measured rather than its absolute value, so the exact value of C_o is not critical as long as it is reasonably constant over time and temperature. If the charging voltage is simply V_{dd} (3V or 5V) then the voltage measurements can be performed using an analogue-to-digital converter (ADC) peripheral commonly found on any microcontroller.

Capacitive Sensing With A Microcontroller

In practical implementations, the sensing capacitor (C_x) is realized with a small pad (the approximate size of a fingertip) on the printed circuit board, and its value depends both on the area and the material (air) dielectric characteristic as it couples with a reference ground plate. When a finger is pressed against the surface (or in its proximity), the dielectric characteristic is changed (our body is 90% water), resulting in a more or less pronounced change in capacitance.

This would seem trivial to measure if it wasn't for the fact that

the capacitance values involved are minuscule. A typical sensor capacitance is in the order of ten picoFarads (10pF) or less, the same order of magnitude of most parasitic effects (couplings) between traces on a PCB. The capacitiance changes in the vicinity of a finger are only a fraction of that value. It follows that there is a seemingly infinite number of ways noise can get injected into such measurements and wreak havoc.

Many embedded developers who tried to hack together a capacitive sensor found a quick and exhilarating success when testing it on their bench for the first time, only to spend months – if not years – to turn that prototype into a repeatable (manufacturable) and robust embedded application.

Expert touch-sensing developers have distilled a set of rules over the years for optimal PCB layout design (a fundamental step in every touch design) and filtering techniques that enhance the noise immunity of the system. These techniques are all based on the need for a large number of measurements in the shortest possible time.

Since each measurement is composed of a complete sequence (charge, discharge, connect in parallel, convert), even when a fast ADC is used there is still a considerable amount of work that needs to be coordinated and precisely timed by the microcontroller. It is here that smart Core Independent peripherals can make a considerable difference.

ADC With Computation

In the latest PIC16F18855 family (featured on the MPLAB Xpress Evaluation board) we find a new type of ADC module enhanced specifically to relieve the core from some trivial but otherwise time-consuming tasks that are commonly found in most embedded applications.

The new module adds two post-processing stages to the conversion front-end. First, each conversion result can be accumulated (signed 16-bit math) for a given number of times; the result can then be compared against a pair of threshold values so that an event (or an interrupt) is generated only when a specific condition is identified – a value inside/outside the given window.

Further, conversions can be triggered automatically (based on a number of internal or external events), and a "pre-charging" mechanism has been specifically designed to support the CVD technique so the ADC module sample-and-hold capacitor can be used as reference capacitor (C_o) for a completely automatic and fully-integrated sequence.

The use of the new ADCC module results in a massive reduction in the core workload during capacitive-sensing acquisition. Once the input channel is selected, by connecting the ADCC input multiplexer to the desired pin/pad, the module will operate independently for milliseconds before returning an averaged output value ready to be used by the detection algorithms to implement the button or slider functionality desired. This can result in the ability to support a larger number of buttons/inputs, an increase in resolution for proximity detection applications or, even more importantly, a considerable reduction in power-consumption.

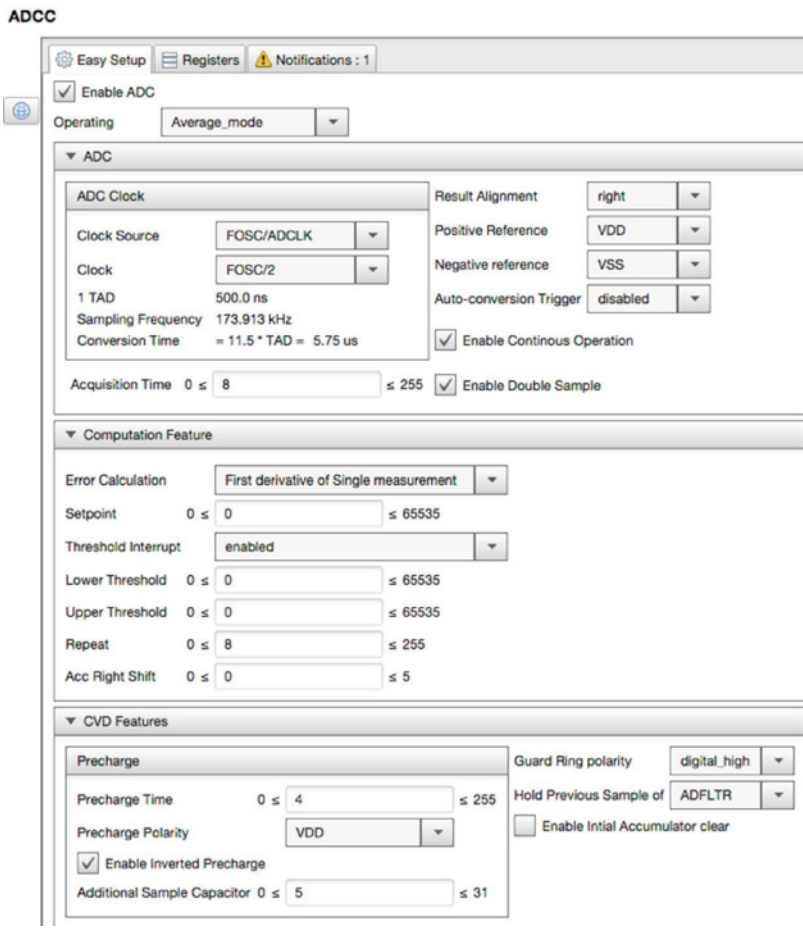


Figure 2: MPLAB Xpress ADCC configuration

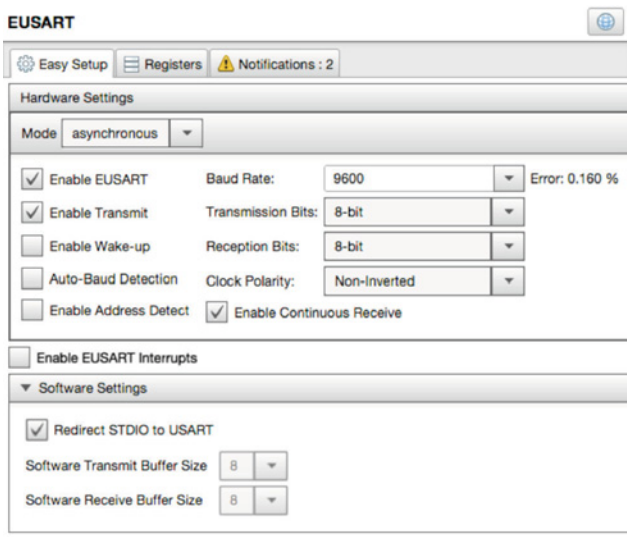


Figure 3: USART configuration

Figure 4: mTouch evaluation kit – 8 pads board

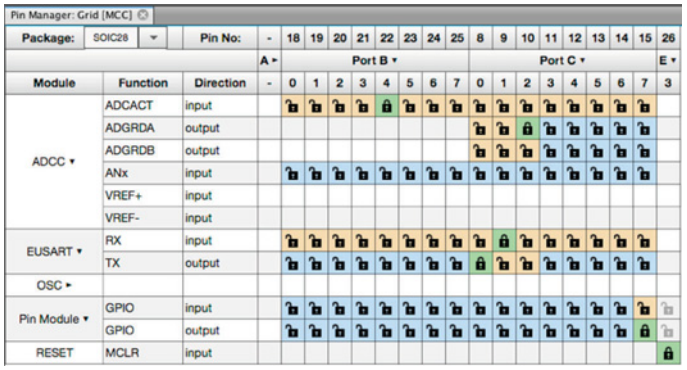


Figure 5: Pin Manager grid

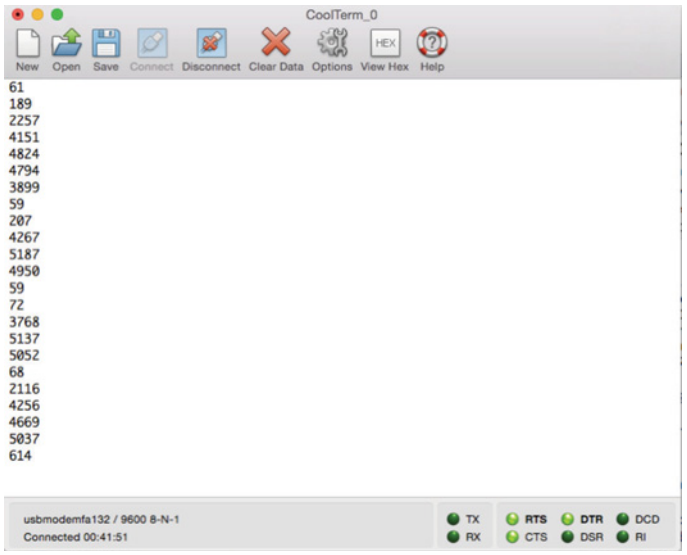


Figure 6: Terminal screen capture

Touch Express

Using the MPLAB Xpress cloud tool chain and the MPLAB Xpress little evaluation board we can test the effectiveness of the ADCC module in just minutes to get a feel for the performance achievable.

- After logging into your own myMicrochip account, create a new project for the PIC16F18855 device and launch the MPLAB Code Configurator.
- Select the ADCC module, then select the following options (see Figure 2).
- Choose the Averaging mode.
- Select the internal oscillator (FOSC/2) as the clock source.
- Select the right-hand alignment of the conversion results and make V_{dd} and V_{ss} the positive and negative internal references.
- Enable Continuous operation so the ADCC will perform rapid bursts of conversions as fast as possible.
- Enable the Double Conversion Sample mode, activating a differential CVD sampling technique.

By swapping (alternating) the role of the two capacitors (precharging the external unknown first and discharging it on an empty reference capacitor), it is possible to obtain a *differential* measurement, effectively cancelling out a number of noise sources and increasing measurement resolution substantially.

Expanding the Computation Features section of the configuration window, select the following options:

- Make the error calculation the First Derivative of Single Measurement (also part of the differential technique described above).
- Enable the Interrupt threshold.
- Set the repeat count to 8 (larger values are possible, but won't be needed, as we will soon see).
- Expand the CVD Features section of the configuration window and select the following options:
- Set the precharge time to 4 (clock ticks).
- Set the precharge polarity to VDD (first).
- Enable Inverted precharge.
- Set the guard ring polarity to digital high.
- Set the additional Sample Capacitor to 5(nF); you might try with different values to optimize resolution depending on the size of the sensing pad.
- Add the EUSART module to the project and configure it for the desired baud rate (see Figure 3).

Wiring Up The Demo

For demo purposes any size and shape capacitive touchpad will do, but since the little Xpress evaluation board has none of its own, you will need to either clip on a small metal plate to the RC7 pin or recycle one (for example, I had an old mTouch evaluation kit DM183026, so I simply re-cycled the little daughter board with 8 square pads – see Figure 4 – for my own convenience.)

Next, enter the Pin Manager window (grid, see Figure 5) and select the desired I/O pins to connect:

- sensor input to RC7 (a convenient pin positioned at the top right corner of the Xpress evaluation board).
- ADGRDA output to pin RC2 (this will be connected to the terminals marked GND or similar layer on the sensor board PCB, if available).

Note that both the RC7 and RC2 pins must be configured as analogue inputs with digital output functions so the ADCC module can automatically perform the correct CVD pre-charge sequence.

Finally let's configure the UART (TX) output to RC_o, conveniently connected internally to the serial to USB bridge on board.

In 10 Lines Of Code

With a click of the "Generate" button, the MPLAB Code Configurator

will produce the configuration files and place them in the project sources. We are now ready to start focusing on the core of our demo application.

```
#define TOUCH 0x17 // pin RC7

void main(void)
{
 SYSTEM_Initialize();
 ADCON3bits.ADSOI = 1; // stop sampling after interrupt

 ADCC_StartConversion(TOUCH); // select channel
 __delay_ms(500);
 int base = ADACC; // detect base value

 while (1)
 {
 ADCC_StartConversion(TOUCH); // select channel
 __delay_ms(100);
 printf("%d\n", base - ADACC);
 }
}
```

Listing 1: Automatic CVD Conversion

The ADCC configuration we obtained with the MPLAB Code Configurator is already providing all that's required to perform a burst of 8 (pairs of differential) conversions, each composed of the complete CVD precharge, discharge, parallel and A/D conversion steps with the correct timing. So all that's left for our main application (as seen in Listing 1) is to select the desired input channel and invoke repeatedly the ADCC_StartConversion() function.

Reading the output on your terminal application (see Figure 6) will give you a rough idea of the kind of resolution achievable with the suggested configuration.

The values captured whilst I repeatedly touched the sensor (larger values) clearly show a remarkable dynamic range of more than 10 bits. This gives us the confidence that following filtering and event detection logic we might want to turn this demo into a real touch application, with more than sufficient resolution to operate reliably and with large noise margins.

In Closing

The MPLAB Code Configurator and the flexibility of the Core Independent Peripherals (ADCC) make it easy for us to completely automate the most core-intensive part of the capacitive touch sensing technology (CVD). Whilst we still need to use the greatest care in designing a proper board layout and add the desired touch detection logic, we have considerably simplified the task at hand and can now focus all our resources and efforts on the development of the actual end application. ●

Light sensors

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

It is important to be able to measure and adjust the ambient light for visual comfort in everyday activities, such as whilst using a computer, reading a book, watching television, cooking, eating and so on.

Light has a very wide spectrum, although in this article we are only interested in visible light in the wavelength range of 390nm (violet) to 700nm (red), all that is necessary in everyday life.

Figure 1 shows the definition of some of the commonly used SI light units. The amount of light being given off in all directions by a light source is known as 'luminous flux', measured in units of lumens. Table 1 gives the light outputs of some commonly used incandescent light bulbs in lumens. For example, a 60W incandescent light bulb emits about 800 lumens. In 2010, European Union legislation took effect, requiring that all light bulbs must be labelled in terms of their luminous flux outputs (in lumens) instead of electric power (watts).

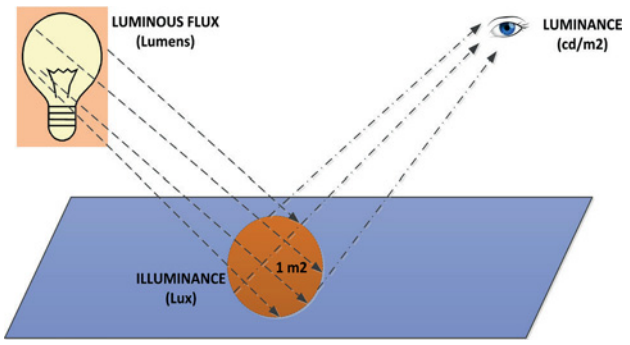


Figure 1: Some commonly used light units

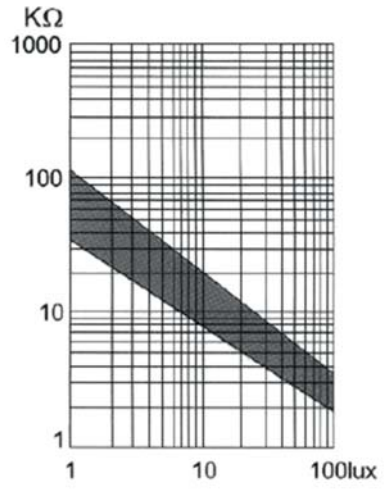


Figure 2: LDR light levels versus resistance

Incandescent bulb (watts)	Minimum output (lumens)
40	450
60	800
75	1100
100	1600
200	3100
300	4000

Table 1: Light output of incandescent light bulbs

The amount of light incident on a surface is known as 'illuminance' and is measured in units of lux, where lux is the number of lumens falling on a square meter of surface, which in numerical terms is 1 lux = 1 lumen/m^2. One-candela (1cd) light-source produces 1 lux of light at one meter distance. Lux is the unit used commonly when measuring and specifying the visual comfort levels in an area.

Luminance is measured in cd/m^2 and indicates how bright a surface appears when looking at it; basically, it is the reflection from a flat diffuse surface. For example, the brightness of a computer display is measured by its luminance.

Illumination from the sky varies at different times of day and at different seasons, as shown in Table 2 in lux.

Sky condition	Illumination (lux)
Full daylight	10700
Overcast	1050
Dark day	105
Twilight	10
Full moon	0.2
Quarter moon	0.02

Table 2: Illumination from the sky

Although natural illumination from the sky can be bright, it is not usually available inside a building. It is the design engineer's task to make sure that right level of light reaches inside a

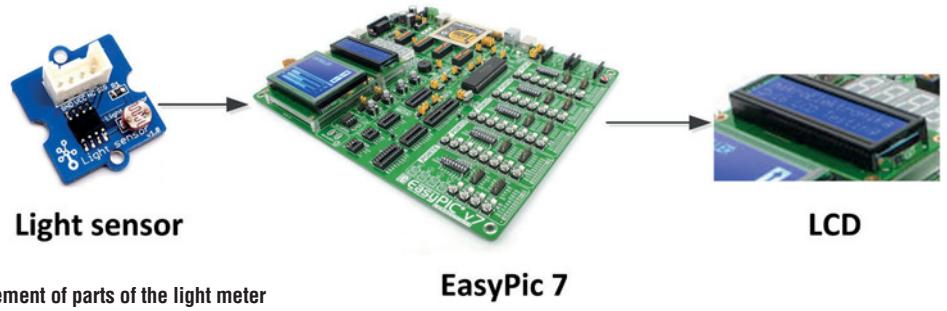


Figure 3: Arrangement of parts of the light meter

building for visual comfort of the occupants. The amount of light required inside a building depends on what tasks are performed there. For example, a watchmaker or a place where electronic components are assembled requires much brighter light than a supermarket. Table 3 gives a list of the recommended illumination levels for different activities. Notice that where possible the actual illumination level is measured on a surface where work is carried out.

Activity	Minimum illuminance (lux)
Watch making and jewellery	1500-2000
Electronics assembly	1000
General computer work, reading/writing	500
Libraries, lecture theatres	300
Restaurants, warehouses	200
Corridors, changing rooms	100-150
Tunnels, night time parks	50

Table 3: Recommended illumination levels inside a building

Light Sensors

A light sensor detects the presence of light (usually visible light) and provides some kind of output of a value proportional to the measured ambient light. Although there are some light sensors with digital outputs, most are simple resistors, also known as a light dependent resistor (LDR), whose resistance changes depending on the light intensity striking the surface of the sensor.

Light sensors are used in embedded applications such as light meters designed to measure light levels inside a building (e.g. an office or a factory), light-sensitive switches and alarms, and so on. In this article we will focus on low-cost analogue light sensors in microcontroller-based embedded applications.

Digital Sensors

Digital light sensors are accurate devices allowing exact light measurements, usually in the range 0.1-40,000 lux. Most are sensitive to both visible and infrared light sources. Some sensors (e.g. TSL2561) have built-in ADC converters, enabling them to be interfaced with any microcontroller, even if the microcontroller has no ADC converters. Depending on the

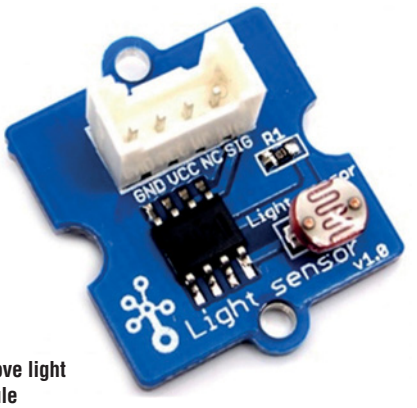


Figure 4: Grove light sensor module

type, the operating voltage can be 3.3V or 3-5V, with current consumption of around 0.5mA when active. Some digital light sensors give square-wave outputs where the frequency is proportional to the measured light level. TSL2561 is a 6-pin active device with I2C-type output where the measured light level can be read by addressing the device via the I2C interface.

Analogue Sensors

An LDR has the property that in the dark its resistance is very high, usually in the range of mega-ohms, but when exposed to light the resistance drops sharply to a few kΩ, or even lower, depending on device intensity of the light source and sensitivity.

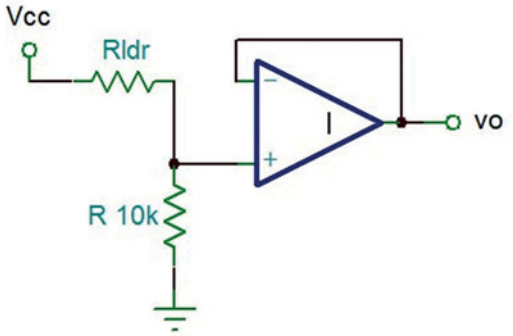


Figure 5: Circuit diagram of the Grove light sensor module

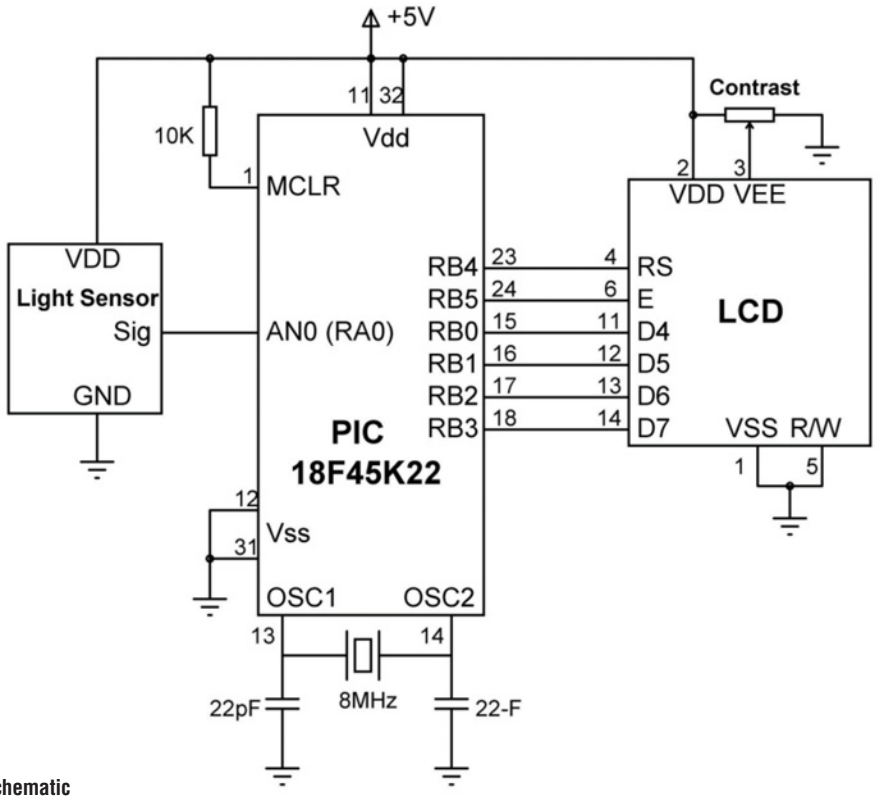


Figure 6: Light meter schematic

The main advantages of LDRs are their very low cost and ease of use in embedded applications.

Figure 2 plots the light level against resistance of a typical LDR.

Designing A Simple Light Meter

Here we present the design of a simple microcontroller-based light meter for measuring ambient light and displaying it on an LCD in lux. The meter has a limited range and gives only approximate results, i.e. it's not meant to be a professional-grade device. For more accurate results, a photodiode or a digital light sensor is recommended.

Figure 3 shows the arrangement of the example system. The ambient light level is sensed using a Grove light sensor module (available at www.seeedstudio.com), which provides an analogue output voltage proportional to the measured light level. The ADC channel AN0 of a PIC microcontroller receives this voltage and, after some processing, displays the actual light level in lux.

This light meter can also be used in an embedded circuit as a light-dependent switch, to be activated at a predefined level of ambient light.

The Grove Light Sensor Module

This is a low-cost small module with GL5528 LDR light sensor on board (see Figure 4). As shown in Figure 5, a unity-gain operational amplifier buffer provides the module's output voltage. The relationship between output voltage and measured light level can be derived as follows:

Because of the voltage-divider resistors at the positive input of the op-amp, the op-amp's output voltage is simply given by:

$$V_o = \frac{V_{CC}R}{R + R_{LDR}} \quad (1)$$

or,

$$R_{LDR} = \frac{R(V_{CC} - V_o)}{V_o} \quad (2)$$

Assuming a 10-bit ADC with 1023 quantization levels and reference voltage V_{CC}, the relationship between the output voltage V_o and its digital value r read by the microcontroller is given by:

$$V_o = \frac{rV_{CC}}{1023} \quad (3)$$

Substituting in Equation 2 we have,

$$R_{LDR} = \frac{R(1023 - r)}{r} \quad (4)$$

But, since R is 10k, the value of the LDR in kΩ is found with Equation 5. Notice that the power supply voltage V_{CC} is eliminated from the equation, whose solution depends only on the digital value read from the ADC and the value of the voltage

divider resistor R used:

$$R_{LDR} = \frac{10 \times (1023 - r)}{r} \quad (5)$$

After finding the value of the LDR (in kΩ), we can calculate the light level:

$$Lux = \frac{120}{R_{LDR}} \quad (6)$$

Thus, we use Equation 5 initially to determine the LDR resistance, and Equation 6 to calculate and display the light level in lux.

Figure 6 shows the schematic diagram of the light meter. The EasyPIC V7 development board is used in the design (performance is not an important factor in this design, and any other microcontroller can be used as long as there is at least one ADC channel and a digital port with at least 6 pins to connect the LCD). This development board is equipped with a PIC18F45K22 medium-performance PIC microcontroller, with an 8MHz crystal. In addition, the board contains rich features that make it an ideal development board for those wishing to learn and experiment with PIC microcontrollers.

The light-sensor module is connected to analogue input AN0 (port RA0) of the PIC18F45K22 and is powered from the +5V supply of the development board. The 2x16 character LCD is connected to the microcontroller's PORTB to display the light level in real time, its contrast being adjusted with a potentiometer. The LCD is operated in 4-bit mode to minimize I/O port pin-count.

The Software

Listing 1 shows the software for the light meter. The program was written using the mikroC Pro for PIC language and the integrated development environment (IDE). At the beginning of the program the connections of the LCD to PORTB are defined. The main program starts by configuring PORTB as a digital port (ANSELB = 0) and then initializing the LCD library. The main program is then executed in an endless loop formed using a while statement. Inside this loop the output of the light sensor is read through analogue input channel AN0 using statement ADC_Read(0) and the digital value read is then converted into physical units of lux using Equations 5 and 6. Notice that for accuracy the calculation is done using floating point arithmetic. The value is then converted into a string variable (Txt) using statement FloatToStr so it can be displayed on an LCD. Any leading spaces are removed from this variable using statement Ltrim, and statement Lcd_Out is called to display the light level starting from the LCD's first row and first column, followed by text "LUX". This process is repeated endlessly at one-second intervals, and is only terminated if stopped by the user. ●

```
// LCD module connections
sbit LCD_RS at RB4_bit;
sbit LCD_EN at RB5_bit;
sbit LCD_D4 at RB0_bit;
sbit LCD_D5 at RB1_bit;
sbit LCD_D6 at RB2_bit;
sbit LCD_D7 at RB3_bit;

sbit LCD_RS_Direction at TRISB4_bit;
sbit LCD_EN_Direction at TRISB5_bit;
sbit LCD_D4_Direction at TRISB0_bit;
sbit LCD_D5_Direction at TRISB1_bit;
sbit LCD_D6_Direction at TRISB2_bit;
sbit LCD_D7_Direction at TRISB3_bit;
// End LCD module connections

void main()
{
        unsigned int r;
        float RLDR, LUX;
        unsigned char Txt[14];
        ANSELB = 0;
        LCD_Init();

        while(1)
        {
        r = ADC_Read(0);
                // Read from analogue AN0
        RLDR = 10.0*(1023.0 - r) / r;
                // Calculate the LDR resistance
        LUX = 120.0 / RLDR;
                // Calculate the LUX value
        LCD_Cmd(_LCD_CLEAR);
                // Clear LCD
        FloatToStr(LUX, Txt);
                // convert into string
        LTrim(Txt);
                // Remove leading spaces
        Lcd_Out(1,1,Txt);
                // Display result
        Lcd_Out_Cp("LUX");
                // Display the unit
        Delay_Ms(1000);
                // Wait 1 second
                 }
}
```

Listing 1: Program listing of the light meter

THE FUTURE OF ETHERNET

BY **RON WILSON**, TECHNICAL WRITER, INTEL PROGRAMMABLE SOLUTIONS GROUP

Ethernet is spreading far beyond its original intended use as a local area network for workstations, into scenarios as diverse as chip-to-chip interconnect, automotive data buses and data centres. The reason behind this is three-fold: Ethernet's culture of standardization and interoperability; the rapid evolution of foundational signalling technology that this culture makes possible; and the lower price of components enabled by the resultant economies of scale.

Ethernet was developed at Xerox's Palo Alto Research Center (PARC) to replace an earlier network with a shared co-axial cable on which all devices were peers. The key enabler of its wider success was the decision to submit Ethernet to the Institute of Electrical and Electronics Engineers (IEEE) standards process. Each development since has drawn on a methodical process of convening a task group, defining requirements and organizing development, with the outputs being proven in interoperability testing workshops. This gives Ethernet a huge advantage in emerging applications.

IEEE 802.3 Ethernet standards define the bottom two layers of the network protocol stack: layer 2, the media access control (MAC); and layer 1, the sub-layers that are together known as the physical layer (PHY). Other networking layers above Ethernet (IP, TCP, etc) are specified and standardized independently. Once a standards working group defines a new combination of medium and data rate, all the protocol layers implemented above Ethernet become available for use in the new applications area.

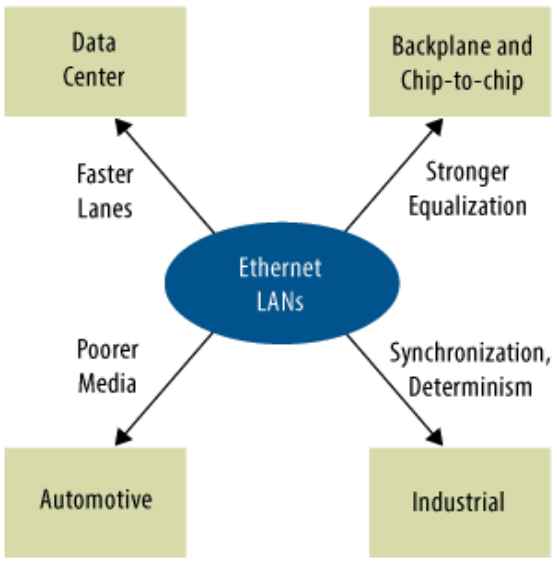


Figure 1: Ethernet's evolution is driven by the demands of new applications [Source: Altera]

PHY

New applications tend to demand new approaches to implementing the physical layer. Channel negotiation, signalling methods and transmitter/receiver equalization all need to be updated to squeeze more information per second through current and new communication channels.

One example of this process at work is the development of a standard for 10Gbit/s backplane interconnects, known as 10GBASE-KR. Here the attraction of Ethernet is to reduce the number of signals crossing a backplane, standardize the PHY hardware and use standard protocols to set up channels and move data.

The challenge of implementing 10GBASE-KR is to achieve 10Gbit/s data rates not over a finely-tuned medium such as high-quality co-ax, but over a channel composed of a mix of circuit-board traces, vias, connectors and backplane runs of differing lengths and electrical characteristics. In this environment, each transmitter and receiver must adjust its equalization independently, demanding many tap-adaptive receiver equalizers and new channel-training sequences.

The technology behind 10GBASE-KR is also being used for chip-to-chip connections on circuit boards, to replace multiple parallel connections with fewer, faster serial links, thus reducing pin count, board congestion and failure rate. In advanced system-on-a-chip (SoCs), the extra die area to support the extra transceivers may be less expensive than implementing the many pins of a parallel connection.

Faster Ethernet

The use of Ethernet in data centres, which need much greater bandwidths between server racks, is driving the development of faster version of the standard. The idea is to increase the maximum speed of a single Ethernet lane from 10Gbit/s to 25Gbit/s, and then to 50Gbit/s and 100Gbit/s, using binary or multi-level modulation signalling. This will require better transceivers and new generations of test equipment. The 25Gbit/s lanes will enable data centres to upgrade their existing top-of-rack cabling from 10Gbit/s to 25Gbit/s, or from 10/40Gbit/s to 50/100Gbit/s.

Vehicle Ethernet

Cars now have so much electronic interconnect that cabling has become an important part of vehicle cost, weight and reliability. This makes the promise of Ethernet – one shared medium and protocol for all data – extremely attractive.

The challenge here is that the best bearer medium in most cars is unshielded twisted pair (UTP), with all its issues of uniformity, impedance and noise-susceptibility. Automotive designers already face these issues in low-speed CAN buses, which is why the Open

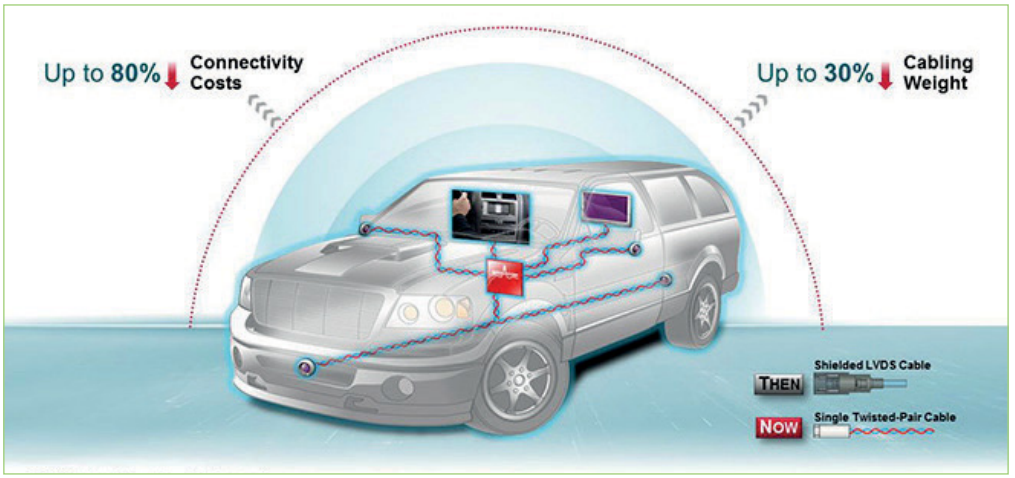


Figure 2: BroadR-Reach promises a single, lightweight and inexpensive network on which all the disparate systems in a car can converge [Source: Broadcom]

Alliance has launched the BroadR-Reach standard to run 100Mbit/s Ethernet over UTP.

Using BroadR-Reach PHYs and standard 100Mbit/s Ethernet switch chips, automotive designers hope to concentrate all the interconnect for engine, brake, steering, chassis, lighting, safety, convenience, infotainment and driver-assistance electronics in a few networks (Figure 2). They will then move toward a single, partitioned network architecture and, perhaps eventually, to one network per vehicle.

Automotive Ethernet means linking engine, brake and chassis controllers, which introduces three requirements that Ethernet doesn't fully address yet: synchronicity, frame delay determinism and security.

These relatively tightly-coupled systems often need to synchronize everything on the network to one clock, so that, for example, the order in which events were sensed or commands given can be preserved. This has to happen despite the fact that the communications medium is a best-effort frame-transmission network without a shared real-time clock or quality-of-service guarantee.

These issues are, up to a point, solvable in the Ethernet stack, especially in closed, short networks such as those in a car, and standards groups have also added other solutions to the Ethernet protocol stack.

Synchronicity is addressed in the IEEE 1588-v2 (2008) Precision Time Protocol (PTP) standard, which distributes time-synchronization PTP packets across Ethernet, so that every interface on the network agrees on the time, down to millisecond or even tens-of-nanosecond levels of accuracy.

The 1588 protocol requires time stamping of PTP packets sent periodically between a 1588 master clock generator and all the 1588 network nodes at the Ethernet entry and exit ports. It can be implemented in the upper protocol layers, above the Ethernet MAC, with standard Ethernet PHY devices. For applications that need micro-second accuracy, the Ethernet MAC or PHY devices must be altered to improve their time-stamping.

A separate IEEE working group, on Time-Sensitive Networking (TSN), is addressing the frame-deterministic latency issues. TSN will reduce both the latency and uncertainty in the movement of packets over Ethernet by providing 1588-based standards for precise time synchronization at layer 2 (just above the PHY), reserving resources in the network and managing the scheduling and pre-emption of packets.

In some cases, TSN may even make the network provably deterministic. Eventually, measures such as TSN will have to face the stringent functional safety demands of industrial and transportation applications. A formally provable – or at least formally traceable – system may be possible in some cases.

Security

Security is another issue Ethernet must face as it evolves, not only in functional-safety situations but in cloud data centres. It will become increasingly important that nodes on the network not be able to monitor the network traffic without permission, and that nodes cannot spoof the identity of another device to send commands.

The privacy issue is partially covered by the fact that Ethernet PHYs scramble data as part of their data-coding algorithms. There are also standards for security in the MAC, IP and application protocol layers, although these are vulnerable to attack. In the long run, Ethernet will need more powerful authentication and encryption.

Power

Finally, work is underway to increase Ethernet's ability to deliver power over an active connection and the data rate supported when it is doing so. There are moves to provide up to 100W for industrial applications over a four-pair connection. Speeds will also rise for single-pair, power-over-data-line technology.

These developments reflect the reasons for Ethernet's success to date. Improving signalling, channel modelling and transceiver design enables Ethernet to reach new data rates over a wider range of media. This opens up new applications, whose implementers can build on everything that has gone before and help add new functions to the protocol stack. Some of these increase bandwidth demands even further, while others need new features in the PHY. This virtuous circle, built on an initial decision to open up PARC technology to the wider design community, helps ensure a steadily broadening horizon for Ethernet.

POWER MANAGEMENT FOR FPGA, GPU AND ASIC SYSTEMS

BY **AFSHIN ODABAEE**, BUSINESS MANAGER FOR μMODULE POWER PRODUCTS AT LINEAR TECHNOLOGY

There are only a few power-management-related design challenges on system boards controlled by FPGAs, GPUs or ASICs, but these challenges can seriously delay release of a system due to repetitive debugging. However, many power and DC/DC regulation issues can be prevented if the same or similar design is verified by the suppliers of power products and the FPGA, GPU and ASIC manufacturers.

The burden is often on the shoulders of system designers to analyze the problem, then find a solution. These engineers are already immersed in configuring the complex digital portions of the design. Tackling the analogue and power portion becomes a major challenge, since power is not the simple task many designers expect.

A Challenging Task

Every design task is initially challenging, including power management for a complicated system that may include transceivers, memory modules, sensors, line connectors, a mesh of PCB traces and layers of PCB planes. But haphazardly addressing power management with DC/DC regulators, capacitors, inductors, heat removal and heat sinks, plus component layout, can lead to later design problems. Hasty decisions by the system designer or choosing inferior solutions will at some point inhibit progress, especially at the debugging stage.

The design of any power management circuit can be done with confidence in a systematic and thoughtful way. In other words, it can be simplified if the analysis is accurate and addresses power management related design challenges before PCB assembly.

Figure 1: Arria 10 GX FPGA development kit board

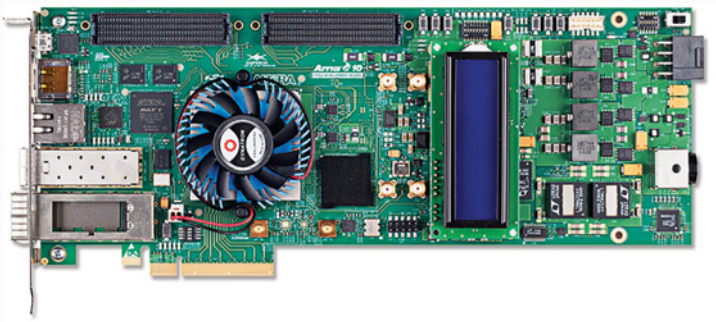
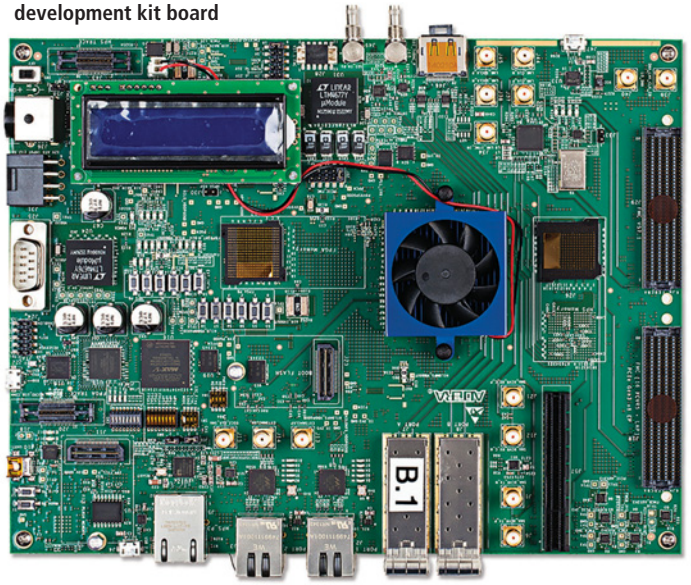


Figure 2: Arria 10 SoC development kit board



Moreover, a power management guide is already tested and verified to meet the requirements of the FPGAs, ASICs, GPUs and microprocessors, and the systems that use these and other digital components.

Mapping power management with proven solutions will ensure that the project is initiated with high confidence. Spending less time on debugging power is an important step in quickly turning a design around, from prototype to production.

Example: Powering Arria 10 FPGA And SoC

FPGA development kits enable system developers to evaluate the logic without having to design a complete system. Figures 1 and 2 show Altera's new 20nm Arria 10 FPGA and SoC (system-on-chip) development boards, tested and verified by Altera, demonstrating best design practices in layout, signal integrity and power management.

A well-thoughtout power management design can reduce PCB size, weight and complexity, as well as lead to lower power consumption and cooling costs, all essential to achieve optimal system performance. For example, the 0.95V at 105A, supplied by the 12V DC/DC regulator powering the Arria 10 GX FPGA core, has several features that complement the power-saving schemes

of the SoC. This includes the DC/DC regulator's integrated 6-bit parallel VID interface used by the Arria 10's SmartVID to control the regulator and reduce FPGA power consumption during both static and dynamic states.

The DC/DC regulator's very low value DC resistance (DCR) current sensing improves efficiency by minimizing power loss in the inductor. Temperature compensation maintains the accuracy or the DCR value at higher inductor temperature.

Customizing The Power Tree

What if the design's power requirements differ from those of the development kit? In this case, use the LTpowerPlanner PC-based design tool to personalize and optimize a system's power tree.

Start with the suggestions given in the development kit, then easily reorganize power blocks, alter power ratings, compute efficiency and power loss, simulate each power block, select DC/DC regulator part numbers and authenticate a customized solution.

LTpowerPlanner was used to generate the power tree (Figure 3) for the Arria 10 development kit's FPGA and system requirements, and is available within the more encompassing LTpowerCAD design tool (free download from www.linear.com/ltpowercad).

The LTpowerCAD enables users to select specific Linear Technology DC/DC regulators to match a given power specification, select appropriate components such as inductors, resistors and capacitors, optimize efficiency and power loss, optimize regulator loop stability, output impedance and load transient response, export the design to LTspice, and so on.

This methodical and proven approach simplifies assigning and managing blocks of power in a system with complex multi-voltage rail requirements, needed from the start of a project.

But, what about the more refined, intricate, details? What other power-related topics should a system designer note ahead of time to avoid debugging, spinning the board or, worst case, starting over? Here is a brief discussion of a few of the subjects that typically occupy the time of an engineering team.

Capacitors, Transient Response And Output Voltage Ripple

Any load such as a GPU, FPGA or a processor may be subject to randomly high data traffic, experiencing a surge of current that quickly disrupts its steady-state power consumption. This transient in current (or power) consumption affects the output voltage of the DC/DC regulator responsible for powering and regulating the voltage to the load. The output voltage of the regulator droops as it fights to supply the current needed by the device's core, for example, whilst regulating its core voltage.

If the regulator is unable to keep up with the demand while supplying the load current, this raises several questions:

- Can the loop response of the regulator be compensated by adjusting the phase margin and bandwidth of the regulator's feedback loop?
- Is a more powerful regulator circuit required?
- Will the addition of more output capacitors remedy the problem? (Capacitors hold charge and help the regulator during load transients.)

To address these questions is time consuming. These aspects also impact cost and size. There are several power supply design tools that can assist even the inexperienced system engineers. Development boards for FPGAs and supporting engineering materials reduce time spent assessing performance of power management, such as optimizing the transient response and minimizing the number of capacitors needed (Figure 4).

Sequencing And Tracking Multi-Voltage Rails

With multiple voltage rails in a system, there is inevitably the question of order. The reverse is also true during system shutdown: which rail is turned off first and which last? The reason is the need for sequential timing between different digital segments of a system, each tasked to perform a job that may

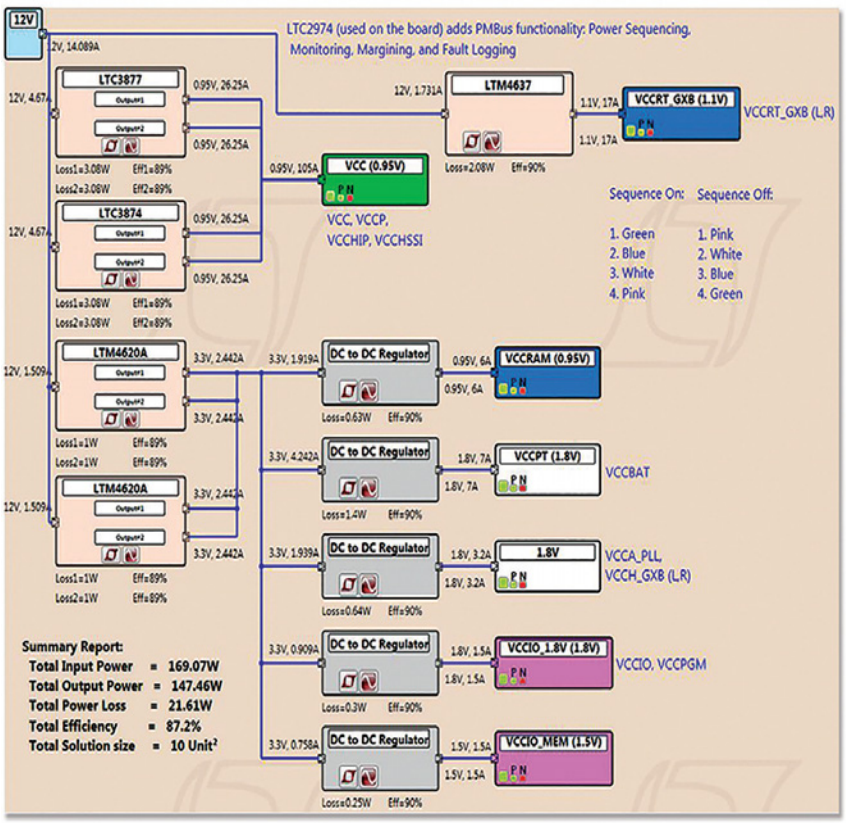


Figure 3: Power tree for Arria 10 GX FPGA board, designed in LTpowerPlanner

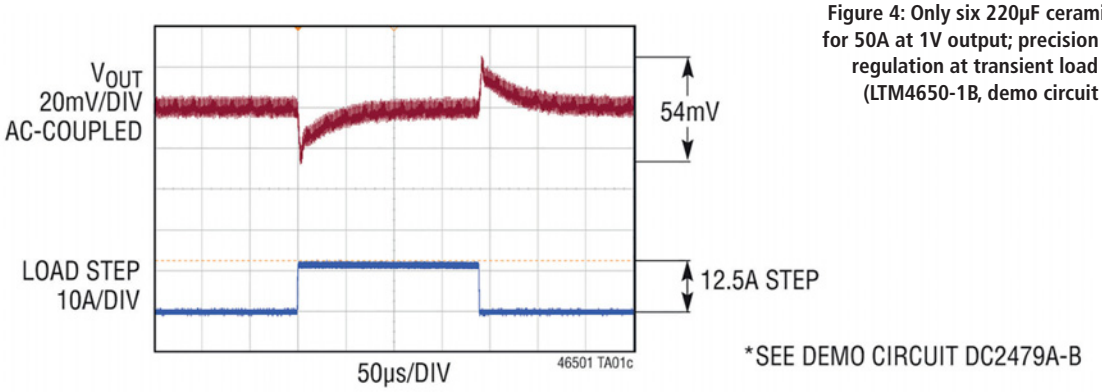


Figure 4: Only six 220µF ceramic capacitors for 50A at 1V output; precision ±3% output regulation at transient load step of 25% (LTM4650-1B, demo circuit DC2479A-B)

depend on the status and "health" of another segment (see Figure 5). For example, should the core voltage be in regulation first, followed by the I/O and then the transceivers? How to ensure one segment does not accidentally start too early or too late and prevent the system from powering up?

Sequencing of power-up is recommended by digital chip suppliers such as Xilinx, Intel (Altera), NXP (Freescale) and others, as is well-known to system engineers. How, then, to best enforce proper sequencing of power for multiple voltage rails?

This task is relatively simple and most DC/DC regulators have this function, sometimes referred to as 'tracking a voltage'. However, knowing how to set up the sequence early in the design and simulate it is most important. It saves retracing PCB layouts or swapping capacitors and resistors later to fix the power-up and power-down timing of the regulators. Performing this exercise early on will enable first-try power-up of a complex multi-rail system.

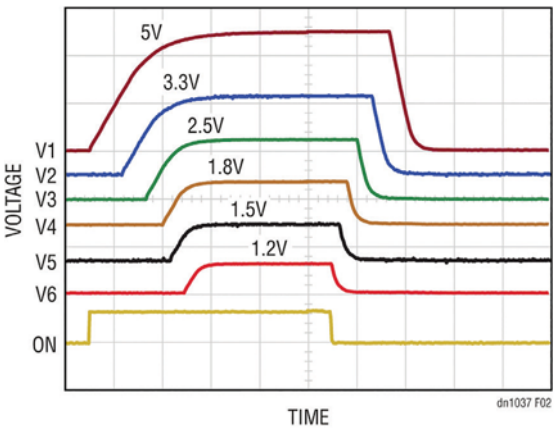


Figure 5: An example of sequencing or tracking six voltage rails: 5V rail starts up and regulates first, 1.2V last

Scaling Power

At some point during prototyping most system designers suspect the regulator is unmatched to the load and feature requirements of the system. As a result, most designers over-design, using bigger and more powerful regulators, which occupy more PC board area and cost more, or the load's (FPGA, ASIC, etc) power consumption may be under-reported. A 10A load may suddenly require 30A due to factors such as the number of transceivers in use, faster timing, flow of firmware and algorithms, etc. Is there a way to map the power management, choose the part numbers and do the layout, with assurance that if power requirements change, the change to the power circuit design is simple or at least not overwhelming?

There is a concept of scaling power-up or power-down by adding or removing blocks of regulators. These blocks are pin-compatible, so the layout can be a matter of copying and pasting the same footprint and same part number or device. For example, a power block (or power module) that is capable of delivering 30A per device can have five devices share a current to deliver 150A (5 x 30A) to a 1V load. The key is to make sure that these power blocks share the current accurately so that no one device is over- or under-used. An over-used device will experience higher temperature rise, possible hot spots and may reach its end of life sooner due to higher thermal stress.

Pin-compatibility is also important because once the layout and pin routing of the device is confirmed, it can be repeated. To ease the prototyping process, using the example of a 150A regulator of 30A per block, a designer can start with all five layouts, populate them and build the board. If board characterization confirms that a lower current, say 115A, is sufficient then instead of five devices, one device for 120A can be removed and prototyping continued.

Or, if after starting with 110A with four devices in mind, you want to build in some insurance, then lay out a fifth socket, leaving it empty and then testing the board. If later during the board evaluation 120A is needed with board at its full usage, then it's simple enough to assemble the fifth power block on to the empty spot without changing the layout and delaying progress. ●

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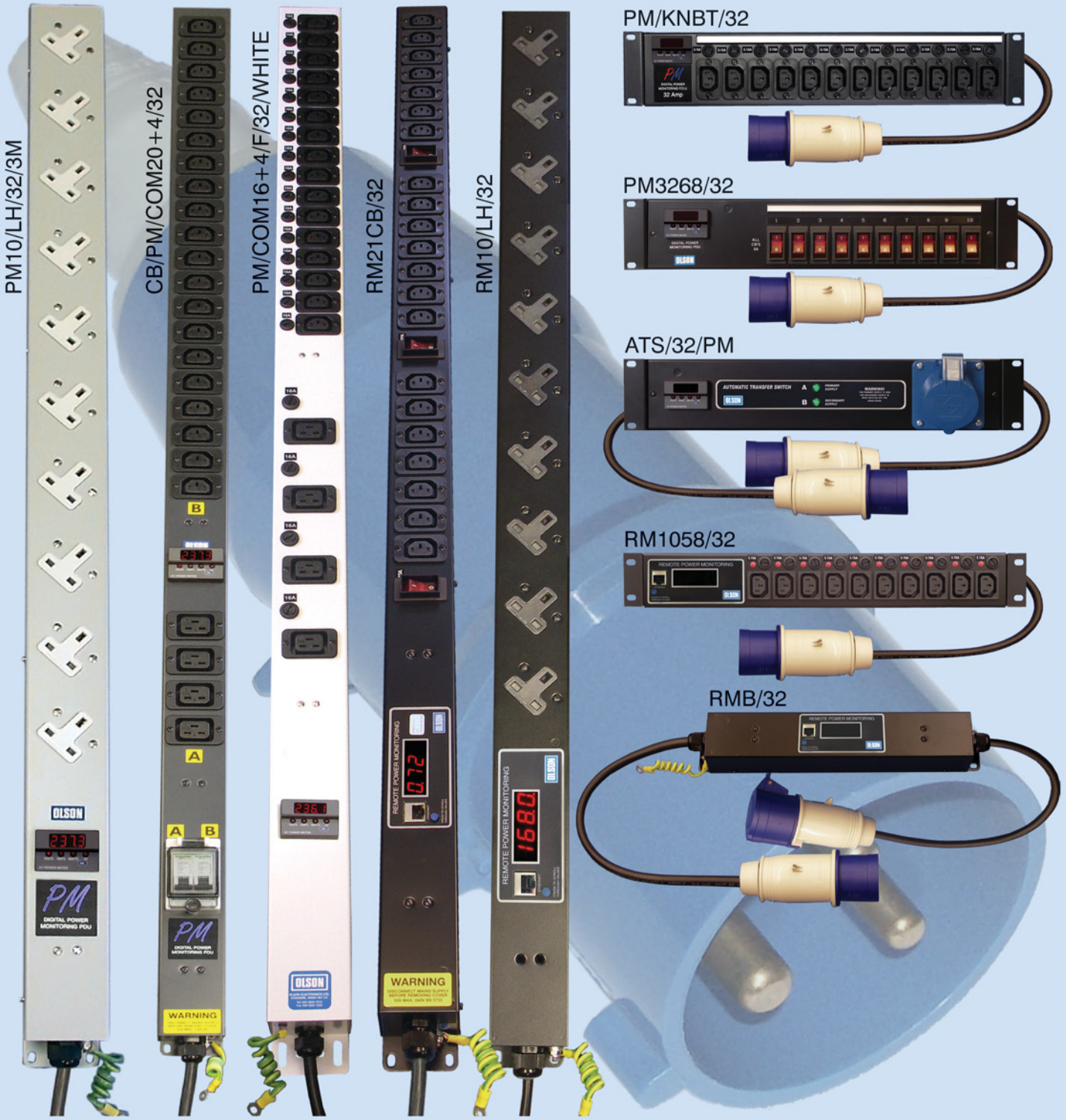

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ESTIMATION OF PARASITIC PARAMETERS AND EMI IMPROVEMENT OF A FULL-BRIDGE PWM CONVERTER SYSTEM IN THE ELECTRIC VEHICLE

BY **QUANDI WANG** AND **QINGSONG LIU** FROM CHONGQING UNIVERSITY, CHINA

Research into electric vehicles has rapidly developed in recent years. Compared to traditional, petrol-based vehicles, electric vehicles contain many high-power devices, including power converters and electric motor drive systems, all of which are a new source of electromagnetic interference (EMI), affecting system operation. Many countries and international committees have already introduced standards relating to electromagnetic compatibility (EMC) of such devices, so EMI cannot be ignored.

Tackling EMI

Methods for suppressing power-device-caused EMI can be classified into several categories: soft-switch based to decrease conducted noise (e.g. buck, boost, flyback, etc); modulation techniques, such as frequency-conversion PWM or random PWM (RPWM); optimizing the PCB design and using a common filter, or improved filter performance based on cancellation of its parasitic parameters. For example, introducing negative inductance in the capacitance path could eliminate the capacitance-equivalent series inductance (ESL).

The first two methods are well-developed and widely applied; the last one is most common right now, but adding filters brings drawbacks such as increased product size, weight and cost.

EMI Transmission Factors

Depending on the various transmission paths in the system, noise can be classified as two types: common mode (CM) and differential mode (DM). CM noise usually flows between ground and the power circuits, whilst DM noise usually refers to the noise that only flows within the power delivery paths. Basically, the main difference between them is whether or not the noise flows through the ground line.

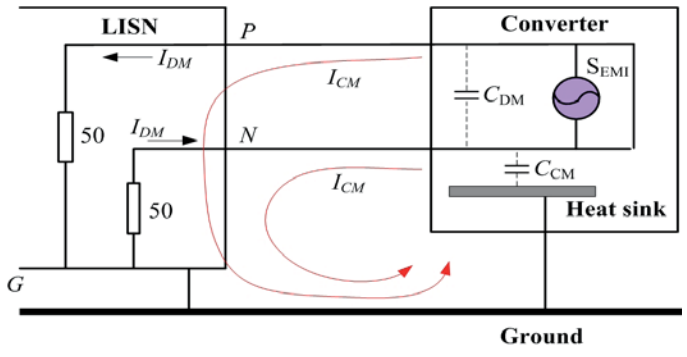


Figure 1: EMI transmission path of a power converter

A simplified EMI transmission path of a power converter is shown in Figure 1. It can be seen that both DM parasitic parameters (C_{DM}) and CM parasitic parameters (C_{CM}) will affect the impedance of the noise transmission loop; DM and CM loops' equivalent circuits are shown in Figure 2.

In Figure 2a, S_{DM} is the DM noise source, Z_{line1} is line impedance, Z_{line2} the impedance of other components in the circuit and Z_{DM} the impedance of parasitic capacitance between power components. In Figure 2b, S_{CM} is the CM noise source, Z_{line1} is the line impedance and Z_{DM} the impedance of parasitic capacitance between the power components and heat sinks.

According to Ohm's Law, the voltage-current relation of the DM loop is:

$$V_{DM} = I_{DM} \cdot \left(Z_{line1} + \frac{Z_{DM} \cdot Z_{line2}}{Z_{DM} + Z_{line2}} \right) \quad (1)$$

and its impedance is:

$$Z_{loop-DM} = Z_{line1} + \frac{Z_{DM} \cdot Z_{line2}}{Z_{DM} + Z_{line2}} = Z_{line1} + \frac{Z_{line2}}{1 + \frac{Z_{line2}}{Z_{DM}}} \quad (2)$$

If the impedance of parasitic parameters in the DM loop increases, the impedance of the whole loop will also increase. With a certain noise source, the DM current in the loop will drop and so will the voltage value extracted from one point in the loop. For that reason, the voltage-current relation of CM loop is given by:

$$V_{CM} = I_{CM} \cdot \left(Z_{line} + Z_{CM} \right) \quad (3)$$

The impedance increment of parasitic parameters in the CM loop will contribute to a decrease in CM current. This analysis leads to the conclusion that the impedance of DM and CM parasitic parameters can affect the amplitudes and distribution of electromagnetic interference in the system.

Parasitic Parameters Calculation

The converter's power components are usually bound to the heat sink with adhesives, and there is a parasitic capacitance between the metal heat-conducting plates of the power modules and the heat sink. When the converter is working at high frequency the parasitic capacitance is the main path of CM current. Also, if the power modules are close to each other, there will also be parasitic capacitance between them, the main transmission path for DM current.

The distribution of parasitic capacitance is shown in Figure 3.

The system, which consists of heat-conducting plates, thermal conductive adhesive, insulating backing and heat sink, we can regard

as a parallel-plate capacitor; see Figure 3a. In addition, the metal heat-conducting plates can be described as several such capacitors, with air dielectric. Meanwhile, the power components and heat sink make up a multi-capacitor system.

Our study focuses on a six-conductor system, comprising five conductors and ground (Figure 3c), with the conductors representing the heat-conducting plates of the power components, and ground (as reference potential) representing the heat sink.

EMI Optimum Method

Theoretically, one part of the high-frequency noise current flows through the parasitic capacitance to ground, constituting CM noise, whilst the other part forms a current loop between the power components as DM noise.

The CM parasitic parameter distribution in the converter is shown in Figure 6. The parasitic impedance of the CM path consists of the parallel connections between the four MOSFET parasitic capacitances to ground and the silicon stack parasitic capacitance to ground. The voltage difference between the power component's drain terminal (D) and heat sink is the CM noise voltage source of this system (Figure 6).

In Figure 6, C_{10}, C_{20}, C_{30}, C_{40} and C_{50} respectively represent CM parasitic capacitance to ground of the five power components. The current-voltage relation in the CM loop is:

$$I_{CM} = \frac{V_{CM}}{Z_{line} + Z_{CM-MOSFET\ \&\ Diode}} \quad (4)$$

Impedance caused by parasitic parameters in the CM loop can be described as:

$$Z_{CM-MOSFET\ \&\ Diode} = \frac{1}{j\omega}\left(\frac{1}{C_{10} + C_{20} + C_{30} + C_{40} + C_{50}}\right) \quad (5)$$

where

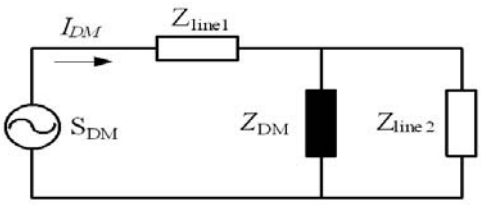
$$Z_{CM-MOSFET\ \&\ Diode} \propto \frac{d}{j\omega\varepsilon S} \quad (6)$$

In Equation 6, d is the thickness of the thermally-conductive adhesive, ε is its permittivity, S is the power component's heat-conducting plate area, and $Z_{CM\text{-}MOSFET\ \&\ Diode}$ is CM impedance caused by the power component's parasitic capacitance. Therefore, modifying these parameters can change the impedance in the CM noise loop and decrease system CM noise current.

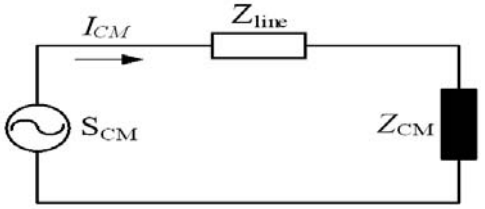
The DM parasitic parameter distribution in the converter is shown in Figure 7. All parasitic capacitances C_{12}, C_{24}, C_{14}, C_{23} and C_{34} add to the DM noise loop. C_{14} and C_{34} are in parallel, and so are C_{12} and C_{23}, whereas C_{24} sits between the legs of the bridge circuit. The DM noise sources in this system are the threshold voltage and pinch-off voltage of the switching devices (MOSFETs). As shown in Figure 7, the voltage V_{DM} can reflect working voltages of the four MOSFETs at any time.

Since the dielectric in the gap of the heat-conducting plates is air and the plates are separated, the calculated results for DM parasitic capacitances are much smaller than the CM parasitic capacitance, meaning that the impedance of the DM parasitic capacitance is much greater than that of the CM parasitic capacitance.

With Equation 2 we determine that when the impedance of the DM parasitic capacitance is very large, it will contribute less to the impedance of the DM loop. Therefore, we can theoretically change

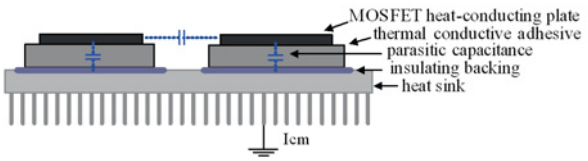


(a) DM noise loop

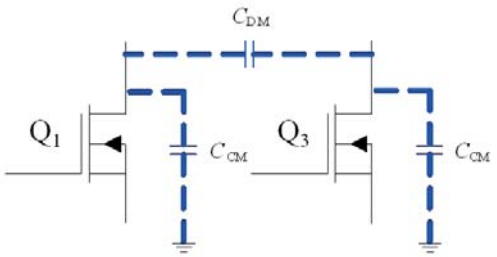


(b) CM noise loop

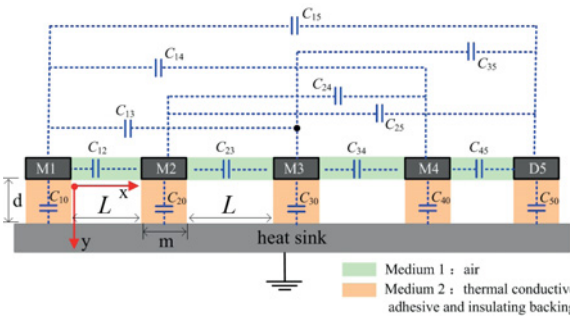
Figure 2: Equivalent-circuit model of EMI paths



(a) physical model



(b) circuit model



(c) multiple conductor parasitic capacitance model

Figure 3: The distribution of parasitic capacitance

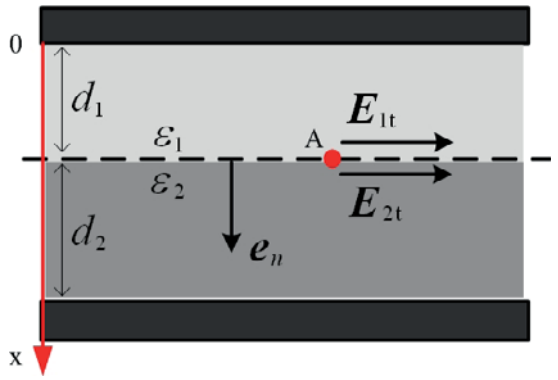
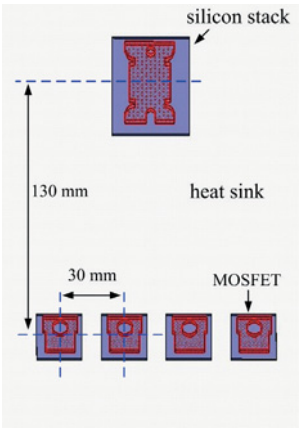
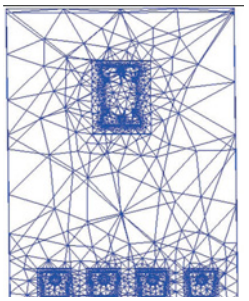


Figure 4: Computation model for parasitic capacitance

(a) FEM model



(b) mesh subdivision



(c) section drawing

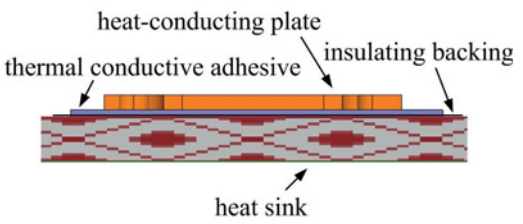


Figure 5: Computation model for parasitic capacitance

the positions of the components to reduce DM parasitic capacitance and hence reduce DM noise current in the system.

From our analysis, the value of conducted noise in the system is determined by the permittivity and filling thickness of the thermally-conductive adhesive between the plates and heat sink, as well as the geometric shape and spatial position of the power modules' plates. These four parameters directly influence the value of DM and CM noise.

Unfortunately, the improvement in EMI suppression performance cannot easily be verified by changing the area of the heat-conducting plates, which are determined by the manufacturers. Also, if we want to verify the effect of different positions of the power components, new PCBs are needed. Therefore, this article mainly concentrates on changing the permittivity and thickness of the thermally-conductive adhesive to analyze these measures' influences on noise.

Simulation And Verification

The thickness of the adhesive is 3mm, permittivity of the insulating backing is about 3, and the area of the MOSFET's plates is 233.65mm^2 and that of the diodes 758.4mm^2. We selected nine permittivity values for the thermally-conductive adhesive: ε=1.0, 1.5, 2.1, 2.8, 3.6, 4.2, 5.0, 6.0 and 7.0. The simulation results are shown in Figures 8 and 9, where we have given the value of 0.5Ω to the component impedances.

Figure 8 shows that differences in permittivity of the adhesive don't affect the impedance of the DM equivalent loop, indicating that associated parasitic parameters do not exist in the DM path. As shown in Figure 9, with increase in adhesive permittivity, the impedance of the CM noise loop will significantly decrease in the frequency range up to 10MHz. However, in the high-frequency range (over 10MHz) the amplitude of CM impedance in the system will decrease dramatically due to capacitive effects of the parasitic parameters, thus providing a main transmission path for CM noise. Therefore, changing the permittivity of the thermally-conductive adhesive can theoretically improve the EMI performance of the system in the low-frequency range, although not so in the high-frequency range. This effect can be calculated through circuit simulations; see Figure 10.

In Figure 10a, the CM current waveforms are shown in the time domain, when permittivity ε is 1 and 7, respectively. The corresponding spectrum amplitude of the noise will also increase accordingly, as shown in Figure 10b.

In the experiment, two types of 3mm-thick thermally-conductive adhesive with permittivity of 4 and 8 were chosen for the gap between the heat-conducting plates of the power components and heat sink, with the rest of the parameters unchanged.

The frequency spectrum of the CM current is measured with a current probe, coaxial cable and spectrum analyzer, and the time-domain measurements use a current clamp and an oscilloscope. When the permittivity values of the adhesive vary, the values of CM current on the power line are as shown in Figure 11.

The experimental result of Figure 11a shows that when the CM noise is within the frequency range of 150kHz-10MHz, for a lower adhesive permittivity, the spectrum amplitude of conducted noise current on the converter system's power lines is lower. Figure 11b shows the waveforms' cutoff as sections of time-domain noise current.

The value for the measurement time sweep is 10us/div, and

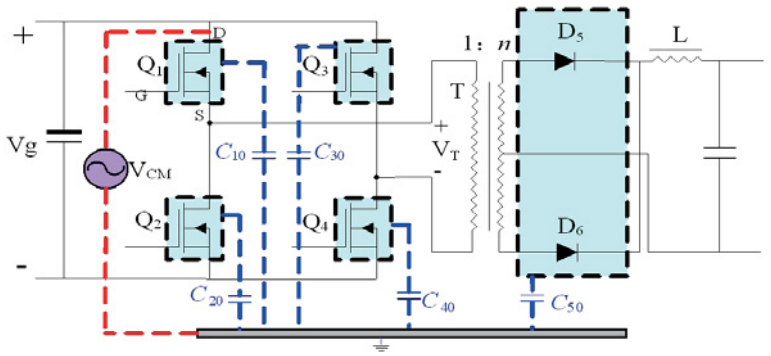


Figure 6: CM parasitic parameter distribution

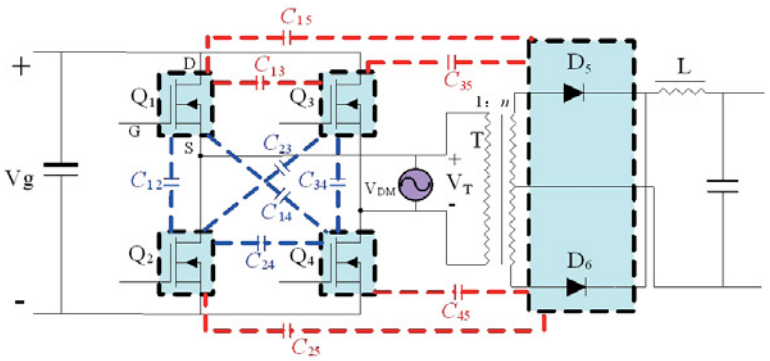


Figure 7: DM parasitic parameter distribution

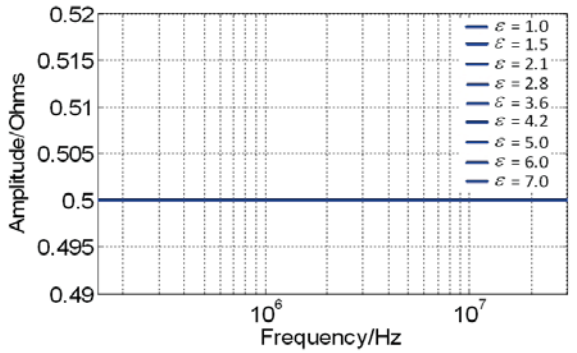


Figure 8: Frequency-impedance characteristic for DM equivalent loop

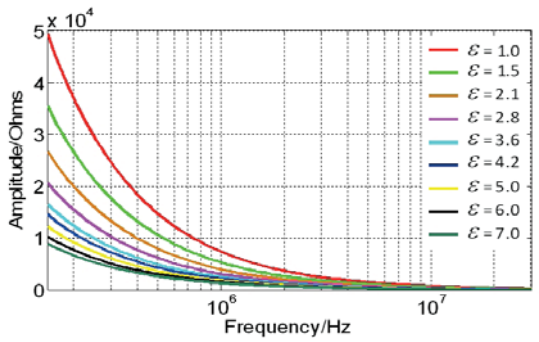
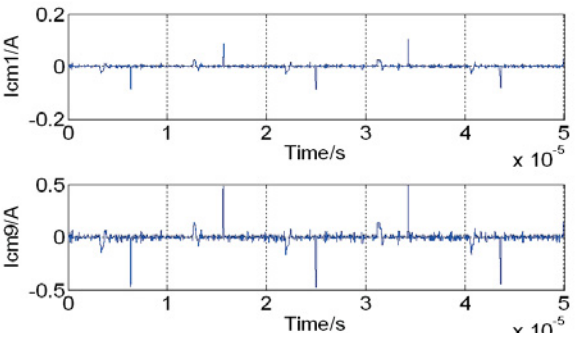


Figure 9: Frequency-impedance characteristic for CM equivalent loop

(a) Current waveforms in time domain



(b) frequency-domain

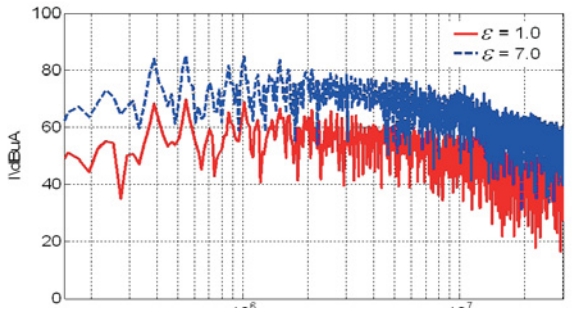


Figure 10: The simulation comparison of CM current, when $^{\varepsilon}$=1 and $^{\varepsilon}$=7

amplitude sweep 500mA/div. The average peak-to-peak values of CM current noise are 232.09mA and 301.69mA respectively. Both frequency-domain and time-domain results match the theoretical analysis, proving that electromagnetic interference can be reduced in the system in practice by decreasing the permittivity of the adhesive between power components and heat sink.

Adhesive Thickness Modification

When the thickness of the adhesive varies between 0.5mm and 1.5mm (choosing six typical values of d = 0.5mm, 0.7mm, 0.9mm, 1.1mm, 1.3mm, 1.5mm), we can calculate the CM parasitic capacitance with simulation. The frequency-impedance characteristic for the common-model loop is shown in Figure 12.

Simulation results show that adhesive thickness has different effects on the CM loop impedance. In the low-frequency range (up to 10MHz), with increased thickness the parasitic capacitances decrease and the CM noise loop impedance gradually increases – a significant change. So, by changing the adhesive thickness, system EMI performance in the low frequency range can theoretically be improved, but not in the high frequencies.

The calculation model for CM current is based on Figure 12, and its circuit simulation results are shown in Figure 13.

Thus we find that with increased thickness d, the CM current amplitude decreases significantly.

Using a power converter system of an electric vehicle as an experimental subject, we can verify that the thickness of the thermally-conductive adhesive does influence the conducted CM current in the input power line of the DC-DC converter. In the experiment, the thickness of the adhesive ($\varepsilon = 8$) is 0.1mm and 2.0mm respectively, filling the gap between the MOSFET's heat-conducting plates and diode silicon stack and the converter's heat sink. All other conditions remain the same; see Figure 14.

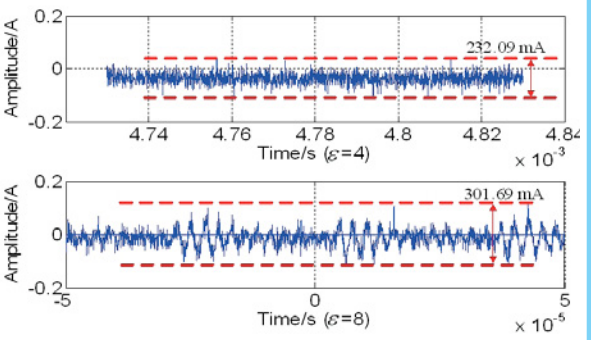
In Figure 14a, the top graph shows the waveforms of the time-domain CM current when the thickness of the adhesive is 0.1mm, whilst the bottom graph is for thickness of 2.0mm. The scanning time is 10us/div and scanning amplitude 500mA/div.

We determined that in the low frequency range (up to 10MHz), when the thermally-conductive adhesive is thicker, the CM current amplitude of the converter system's power lines is smaller. In the high-frequency range (over 10MHz) however, the EMI suppression effect is not significantly improved when the thickness of the adhesive varies. These results match the theoretical analysis for Figures 12 and 13. So, in practice, low-frequency electromagnetic interference can be reduced in a system by appropriately increasing the thickness of the thermally-conductive adhesive between the power components and heat sink.

Upshot

Through theoretical analysis and experiments we verified that by either increasing the thickness of the thermally-conductive adhesive that fills the gap between the heat-conducting plates of the power components and heat sink, or decreasing its permittivity, low-frequency conducted electromagnetic interference on the power line of the converter system can be significantly reduced. In addition, either method decreases the weight and size of the converter and does not require additional costs for design and materials, also significantly reducing filter costs. ●

(a) Current waveforms in time domain



(b) frequency-domain

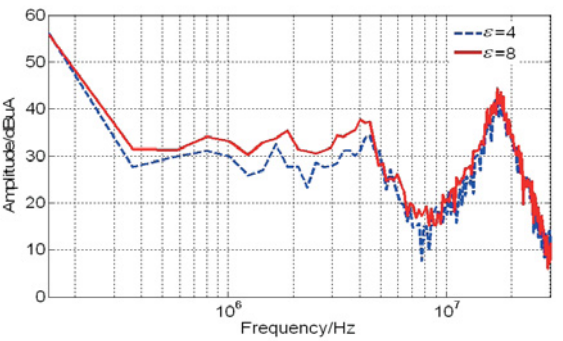


Figure 11: Comparison between measured CM currents on the power line

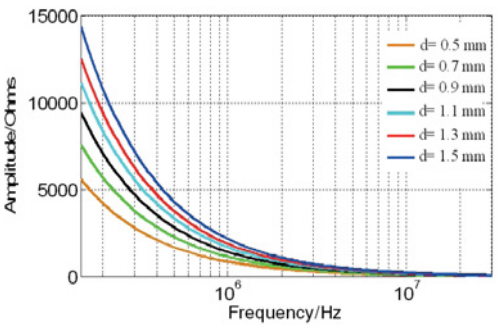


Figure 12: Frequency-impedance characteristic for the common-model loop

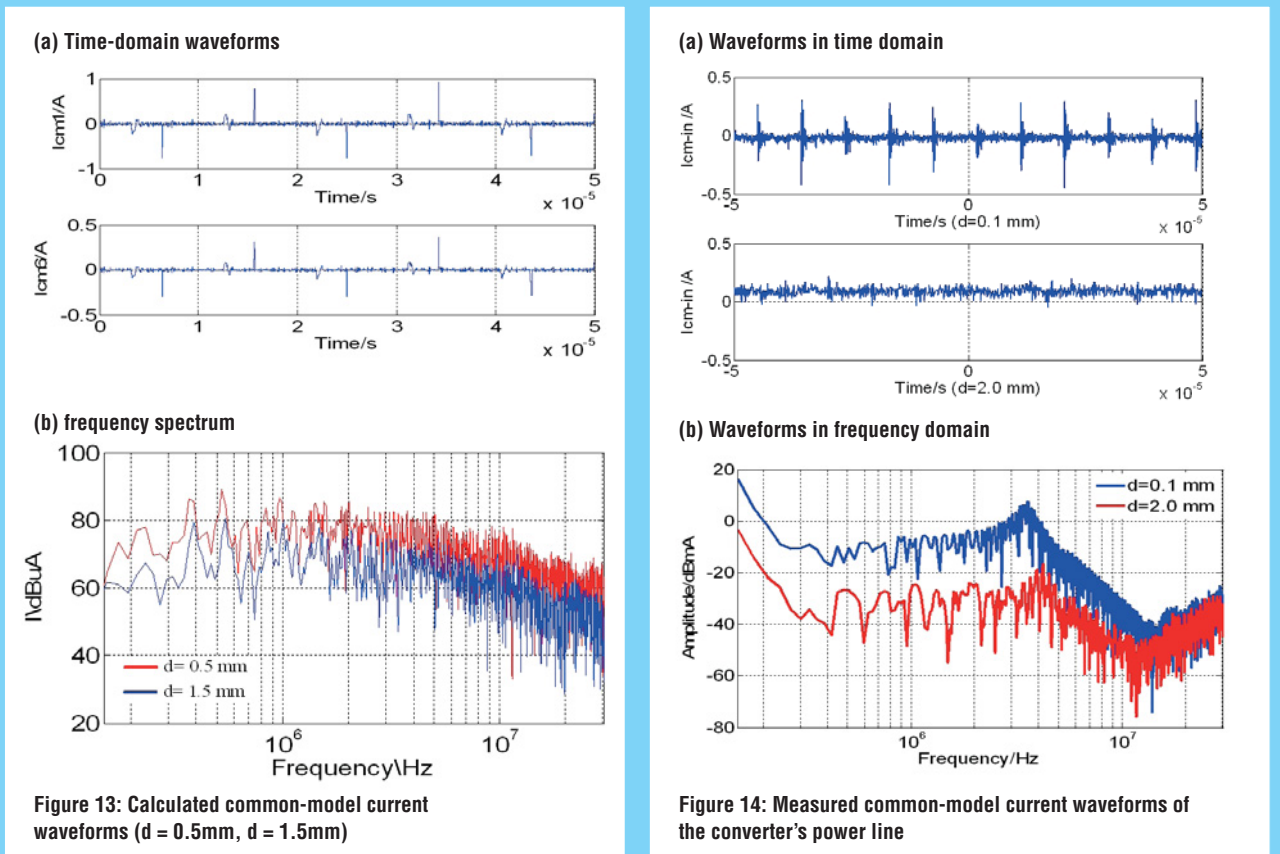


Figure 13: Calculated common-model current waveforms (d = 0.5mm, d = 1.5mm)

Figure 14: Measured common-model current waveforms of the converter's power line

OUTPUT CABLE VOLTAGE DROP COMPENSATION CIRCUIT WITH STATE MACHINE

LING-FENG SHI, SEN CHEN AND **XIU-JIE HU** OF XIDIAN UNIVERSITY, CHINA, PRESENT NOVEL OUTPUT CABLE VOLTAGE DROP COMPENSATION CIRCUITS

Power applications often suffer from output cable voltage drop. Taking a power adaptor as an example, the voltage drop is difficult to handle. Since the resistance of the cable is not part of the feedback loop circuit, for a long cable the voltage drop will be large and the consequent demand on output current too big. The output voltage drop will adversely affect system efficiency and stability.

Traditional Methods

To ensure system stability, it is necessary to use a cable-voltage-drop compensation circuit. One traditional method is with discrete components, where a feedback loop circuit is used to stabilize the output voltage, see Figure 1. Output voltage V_o is expressed as:

$$V_o = \left(1 + \frac{R_2}{R_3}\right)V_{REF} + \frac{IR_dR_2}{R_3} - IR_{lo} \quad (1)$$

where I is the load current.

Assuming the ratio of feedback resistor R_d to cable resistance R_{lo} is:

$$R_d = \frac{R_{lo}R_3}{R_2} \quad (2)$$

then the cable voltage drop must be properly compensated for when the converter load increases from no load to its peak, which leads to the fact that the output voltage is proportional to the reference voltage. However, this traditional method suffers from two shortcomings. One is the use of discrete components which increases system cost and the printed circuit board (PCB) area; moreover, it leads to circuit temperature sensitivity too. Another issue is R_d being kept a constant, which leads to unsatisfactory compensation when the cable length or load is varied.

To address these issues, we propose a circuit that offers accurate compensation and low temperature coefficient, improving output voltage stability and operation in a wide temperature range, at low cost.

Proposed Method

To solve the problem of cable voltage drop in a switched-mode power supply (SMPS), we propose the circuit shown in Figure 2, where it can be seen that the FB pin's voltage increases when the output voltage increases. The switching frequency is adjusted as the FB pin voltage rises to provide a constant output current regulation.

The CC (constant current) circuit is completed by controlling the

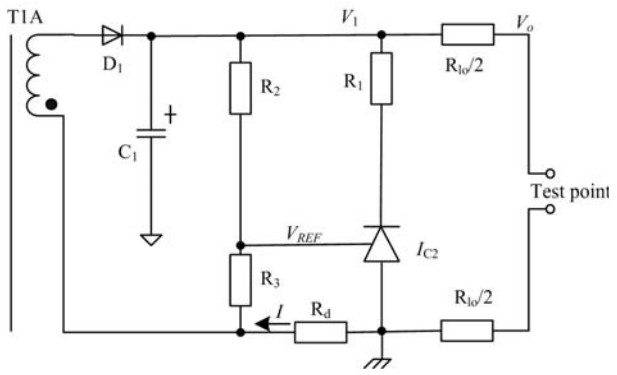


Figure 1: Traditional cable voltage drop compensation circuit

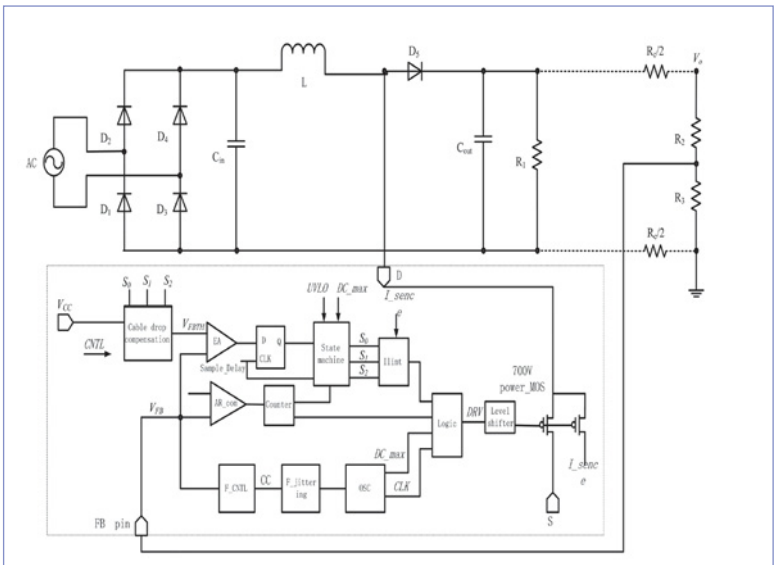


Figure 2: Topology of the cable voltage drop compensation circuit

frequency. As the FB pin approaches V_{FBTH} from the CC regulation mode, the power supply transitions into CV (constant voltage) operation. At this point the switching frequency is at its maximum, corresponding to the peak power point of the CCCV characteristic; see Figure 3.

Using a state machine the controller regulates the FB pin voltage to remain at V_{FBTH}. The FB pin voltage is sampled 2.5µs after the high-voltage switch turns off. In other words, *Sample_Delay* is a brief high voltage when the power MOSFET turns off after 2.5µs.

The cable output drop compensation provides a constant output voltage at the end of the cable over the entire load range in CV mode. As the converter load increases from no-load to the peak power (the transition point between CV and CC), the voltage drop introduced across the output cable is compensated for by increasing the FB pin reference voltage. Obviously, V_{FBTH} increase leads to output voltage increase; the controller determines the output load. Therefore, the correct degree of compensation is based on the output digital signals S_0-S_2 of the SM (State Machine).

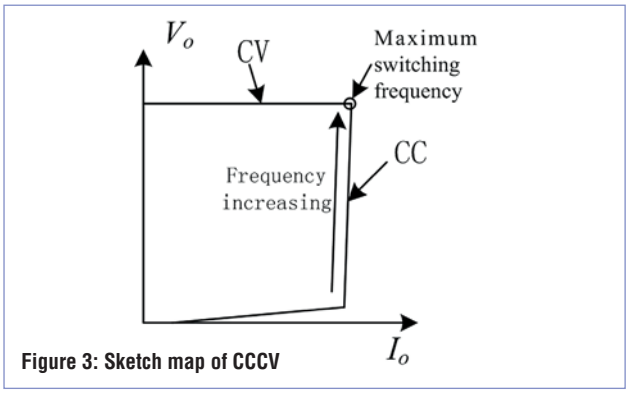


Figure 3: Sketch map of CCCV

SM Circuit

The SM circuit is used to skip periods when $V_{FB} > V_{FBTH}$ by controlling the logic module. In addition, it generates 3-bit digital signals S_0-S_2 representing load states.

DC_{max} is the maximum duty cycle, *Sample_Delay* is the brief high voltage after the power MOSFET turns off after 2.5µs, and *Comp* is the output of the EA (Error Amplifier).

The structure of the SM is shown in Figure 4. It consists of D trigger, 8-bit counter, 14-bit shift register, frequency divider and a data selector with a 1-bit output from 8-bit input.

When $V_{FB} > V_{FBTH}$, *Comp_Sample* is high and *XComp_Sample* is low. The 14-bit register generates a high level between two clocks, initially in Q_0, and shifts the high level right to Q_{13}; see the process in Figure 5. Similarly, when $V_{FB} < V_{FBTH}$, the 14-bit register produces a high between two clocks, initially in Q_{13}, and moves the high level to Q_0. During the chip start-up phase, V_{FB} is low so the high level first emerges in Q_{13} and is then shifted left, gradually.

As mentioned earlier, the SM circuit realizes a *XComp_Sample* signal to control the 14-bit shift register. Because the hold time of the *XComp_Sample* is related to load states, it follows that digital signals S_0-S_2 represent load states. The hold time of *XComp_Sample* varies with the load states; the relationship between S_0-S_2 and the load states is shown in Table 1.

The PSM (Period Skip Mode) logic is shown in Figure 6. *CLK*, triggered by the falling edge of *DCmax*, is a high-level pulse signal. *DRV* is controlled by *XComp_Sample* and *LB*21.

When *XComp_Sample* is high, *CLK* triggers RS by G_1. The power MOSFET will not skip any periods. While *XComp_Sample* is low, G_1 will block the *CLK* signal; *LB*21 determines whether *CLK* is passed by G_2 or not. If *LB*21 is low, *CLK* will not pass G_2 and this period will be skipped.

*LB*21 is generated by an 8-bit counter and data selector with 1-bit output from an 8-bit input; see Figure 4. The 8-bit counter is triggered on the rising edge of *DCmax*. Signals D_0-D_7 are selected by Q_0-Q_{13} (as shown in Table 2) as input signals to the data selector.

When Q_0 is high, D_0 will be selected and the SM circuit will skip one period. If Q_1 is high, D_1 will be selected and the skipping periods

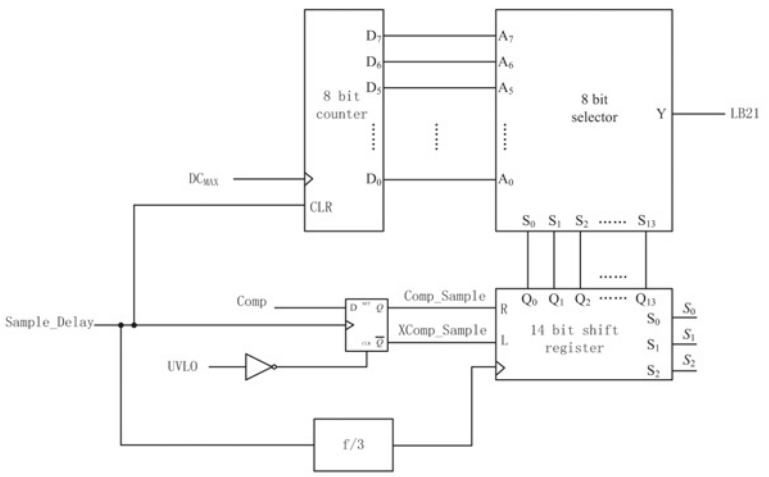


Figure 4: State machine (SM) equivalent structure

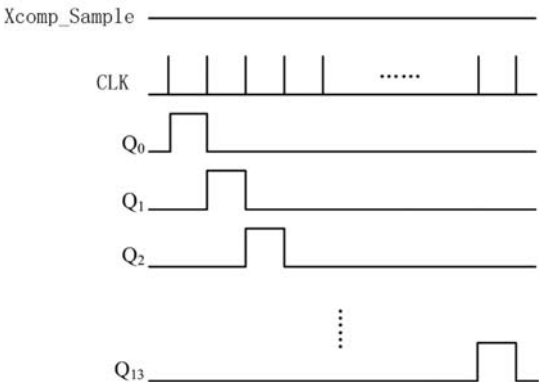


Figure 5: Shifting-right process

of SM will be divided by two frequencies of *DCmax*.

From Table 2, Q_0-Q_7 select D_0 and D_1. If V_{FB} is still larger than V_{FBTH} when S_0-S_2 becomes '000', the high level will be shifted right to select D_0-D_7, which means the circuit will skip 1, 2, 4, 8, 16, 32 and 64 periods.

The shift register's *CLK* is 3-frequency dividing *Smaple_Delay*. The power MOSFET conducts three times and the output of the shift register changes once. This means that the hold time of $V_{FB} > V_{FBTH}$ is

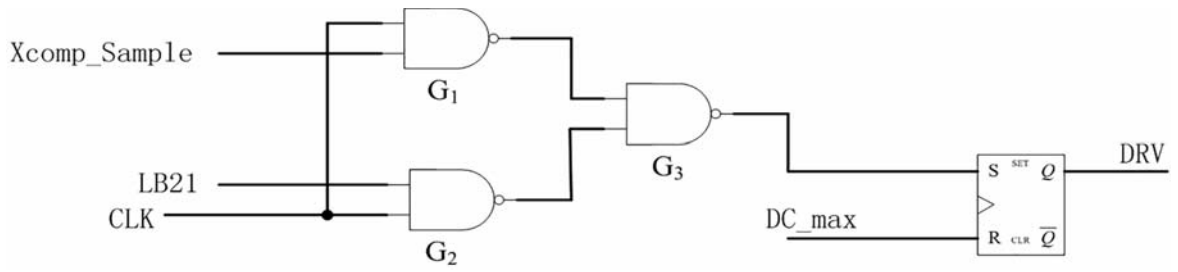


Figure 6: PSM logic module

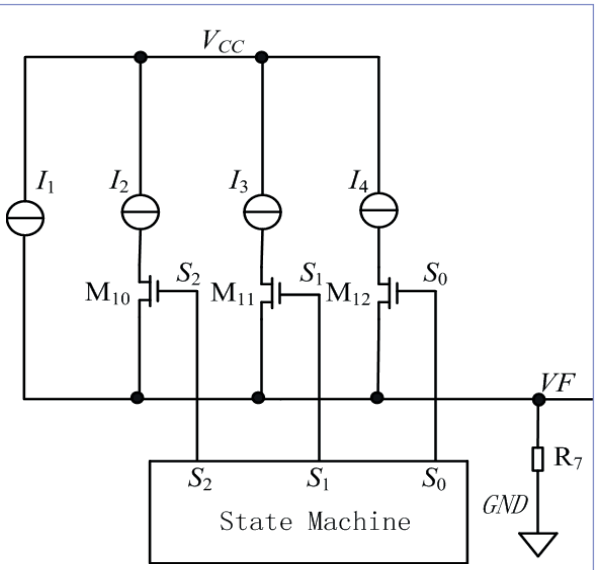


Figure 7: Voltage representing the load states circuit

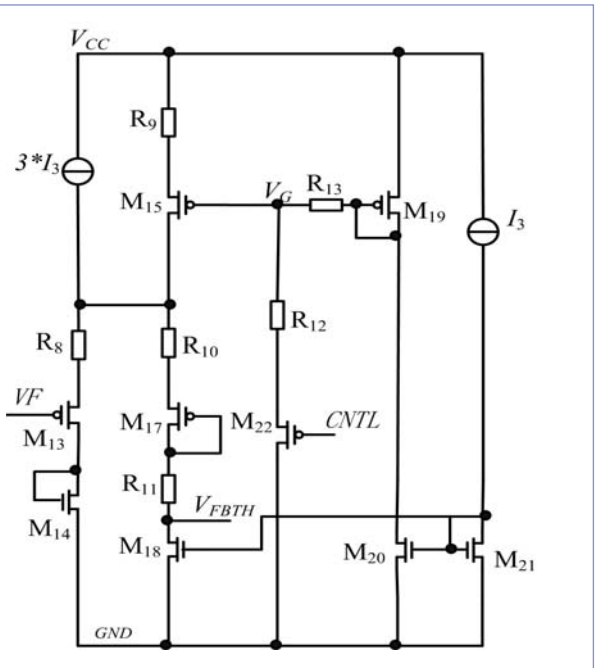


Figure 8: Cable voltage drop compensation and control circuit

equal to three periods of *Sample_Delay*, and the number of skipped periods will increase or decrease based on *Sample_Delay*. This method reduces the ripple of the output voltage, making the system more stable.

Load States Generating Circuit

As seen in Figure 7, the voltage *VF* representing the load-states-generating circuit has current of a low-temperature-coefficient reference flowing through R_7.

$$VF = (I_1 + M \times I_2)R_7 = V_{REF1}(M+1)(R_7/R_6) \quad (3)$$

where M is the number of currents I_2 - I_4 selected by S_0-S_2. The voltage *VF* is proportional to the reference voltage with a low temperature coefficient.

Control Circuit

The signal *VF* representing the load states generates V_{FBTH} with a level shifting circuit. However, V_{FBTH} is generated by the control signal *DRV*. Both signals are proportional to the reference voltage, with a low temperature coefficient and high independence from the power supply. The cable voltage drop needs to be compensated for, which is controlled by the high and low thresholds; see Figure 8.

The cable voltage drop compensation circuit comprises M_{13}, M_{17}, R_8, R_{10} and R_{11}; the threshold voltage can be obtained with:

$$V_{FBTH} = VF + V_{SG13} + I_{R8}R_8 - I_{R10}(R_{10} + R_{11}) - V_{SG17} \quad (4)$$

where $V_{SG13} = V_{SG17}$ because there is a small current through M_{13} and M_{17}. Assuming the ratio of M_{21} to M_{18} is 1:2, then:

$$I_{R8} = I_{R10}/2 = I_3 \quad (5)$$

Both I_1 and I_3 are made of a current mirror so that I_3 is a reference current with low temperature coefficient independent from the power supply. M_{16} is a trimming MOS which is always on to regulate the value of V_{FBTH}. I_{M16} is proportional to V_{SGM15} when M_{16} is on, and voltage V_G is obtained by the resistance voltage divider R_{12} and R_{13}:

$$V_G = (V_{CC} - V_{SGM19})R_{12}/(R_{12} + R_{13}) \quad (6)$$

The control circuit consists of *CNTL* and M_{22}. It controls the high

Load states	S_0	S_1	S_2
Light	0	0	0
Weight	0	0	1
High weight	0	1	1
Peak point	1	1	1

Table 1: The relationship between S_0-S_2 and the load states

Control terminal	Bit of counter	Control terminal	Bit of counter
Q_0, Q_2, Q_4, Q_6	D_0	Q_{10}	D_4
Q_1, Q_3, Q_5, Q_7	D_1	Q_{11}	D_5
Q_8	D_2	Q_{12}	D_6
Q_9	D_3	Q_{13}	D_7

Table 2: Scheme of selecting counter bit

and low threshold with the control signal *CNTL* to switch M_{22} on or off. When *CNTL* is high, due to M_{22} being off, the gate voltage V_G is not large enough to drive M_{15} because of R_9. The threshold voltage is defined as:

$$V_{FBTH-} = VF + I_3\left[R_8 - 2\left(R_{10} + R_{11}\right)\right] \quad (7)$$

However, when *CNTL* is low, M_{22} will be on and the gate voltage V_G will drive M_{15} to switch on. Then the threshold voltage is defined as V_{FBTH-} and current I_{M16} is expressed as:

$$I_{M16} = V_G / R_9 \quad (8)$$

Meanwhile:

$$I_{R8} + I_{10} = 3I_3 + I_{M16} \quad (9)$$

Then, substituting Equations 8 and 9 with Equations 6 and 10 obtains:

$$V_{FBTH} = VF + \left(I_3 + I_{M16}\right)R_8 - 2I_3\left(R_{10} + R_{11}\right) \quad (10)$$

Figure 9 shows how *CNTL* and the switching MOS's drive signal *DRV* control the change of the threshold from low to high.

When cycle skipping does not occur, *CNTL* will be low and M_{22} on, after the high voltage switches off following 2.5μs; then, the threshold voltage is V_{FBTH}. However, when V_{FB} is larger than V_{FBTH}, cycle skipping will occur and *CNTL* will be high, switching M_{22} off. Meanwhile, the threshold of the comparator is V_{FBTH-}. *CNTL* will become low at the rising edge of *DRV*, at which point the comparator threshold returns to V_{FBTH}, where it defines the cable voltage compensation factor as:

$$V_{FB} = \frac{V_{FBTH}}{V_{FBTH-}} \quad (11)$$

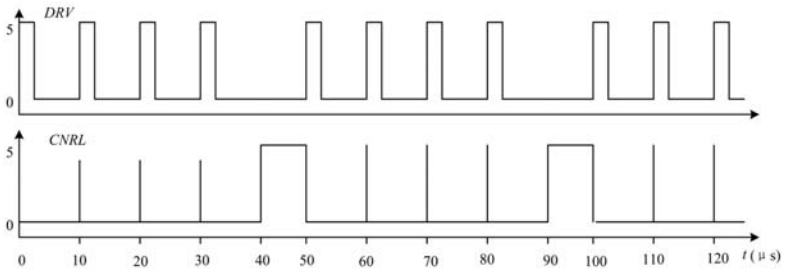


Figure 9: The relationship between CNTL and DRV

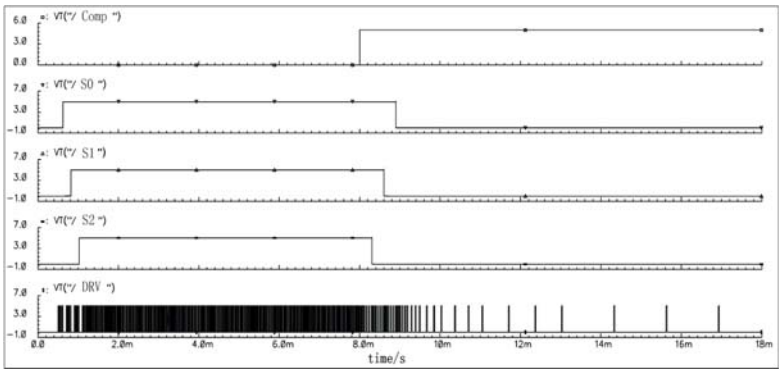


Figure 10: Simulated relationship between the skipping periods and S_0-S_2

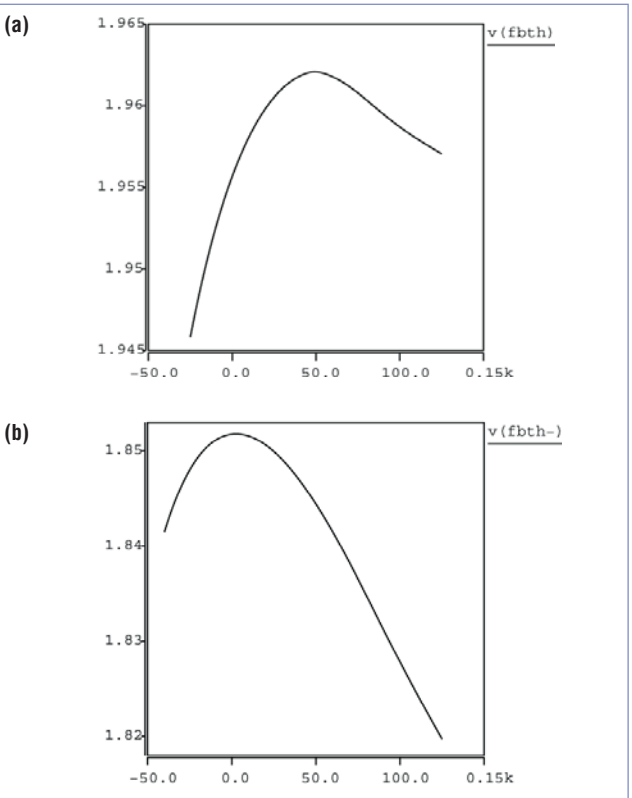


Figure 11: Simulated temperature characteristic for: (a) high threshold; (b) low threshold

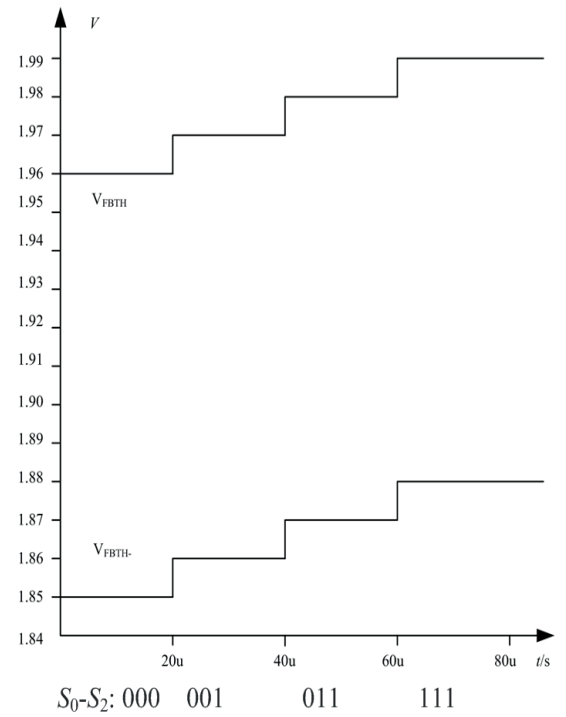


Figure 12: Simulated high and low thresholds with S_0-S_2

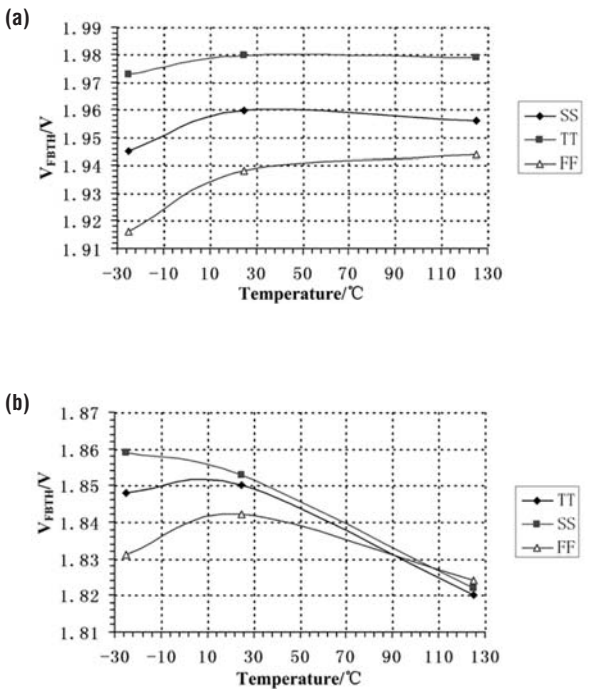


Figure 13: Corner simulation results of V_{FBTH} and V_{FBTH-} (a) V_{FBTH}; and (b) V_{FBTH-}

This confirms the circuit's ability to compensate the cable voltage drop.

Simulation Results

The proposed compensation circuit has been implemented in a 0.5μm BCD process. The temperature coefficient of the reference current is 26ppm/°C over a wide temperature range (-40°C ~ +125°C), which ensures the cable voltage drop compensation circuit works normally.

Figure 10 shows the relationship between the skipping periods and S_0-S_2. When *Comp* is low ($V_{FB} < V_{FBTH}$), S_0-S_2 change to '000-100-110-111'. In this mode all *CLK* pass and there are no skipping periods. While *Comp* is high ($V_{FB} > V_{FBTH}$), S_0-S_2 change to '111-110-100-000'; the number of skipped periods increases gradually.

Figure 11 shows the temperature characteristic of the high and low threshold levels. The high threshold voltage V_{FBTH} is 1.96V and the low threshold voltage V_{FBTH-} is 1.85V at room temperature. Using Equation 11, the cable voltage compensation factor is easily found to be 1.06.

Figure 12 shows how thresholds change with the load states: when the load changes from light to heavy, the threshold voltages of V_{FBTH} and V_{FBTH-} will increase in 0.01V steps.

Figure 13 shows the corner simulation results of V_{FBTH} and V_{FBTH-}. The maximum error of V_{FBTH} is 0.06V and V_{FBTH-} 0.03V.

Figure 14 shows the relationship between two skipped periods and different loads in CC mode. Obviously, the number of skipped periods is different for different loads.

Figure 15 shows the relationship between skipped periods and different loads in CV mode. V_{FBTH} and V_{FBTH-} vary with loads, which compensates for the cable voltage drop.

Figure 16 shows CC simulation results when the loads are 3.5Ω, 4Ω and 4.5Ω respectively. The output current is approximately 1A.

Figure 17 shows CV simulated results when the loads are 5Ω, 6Ω and 7Ω respectively. The output voltage is approximately 5V.

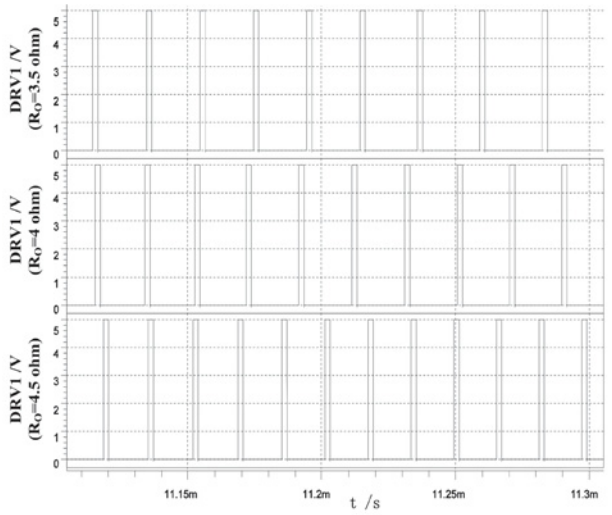


Figure 14: Simulated skipping periods when the load is 3.5Ω, 4Ω and 4.5Ω respectively

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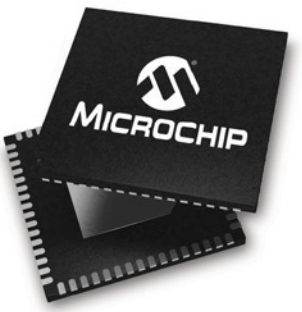

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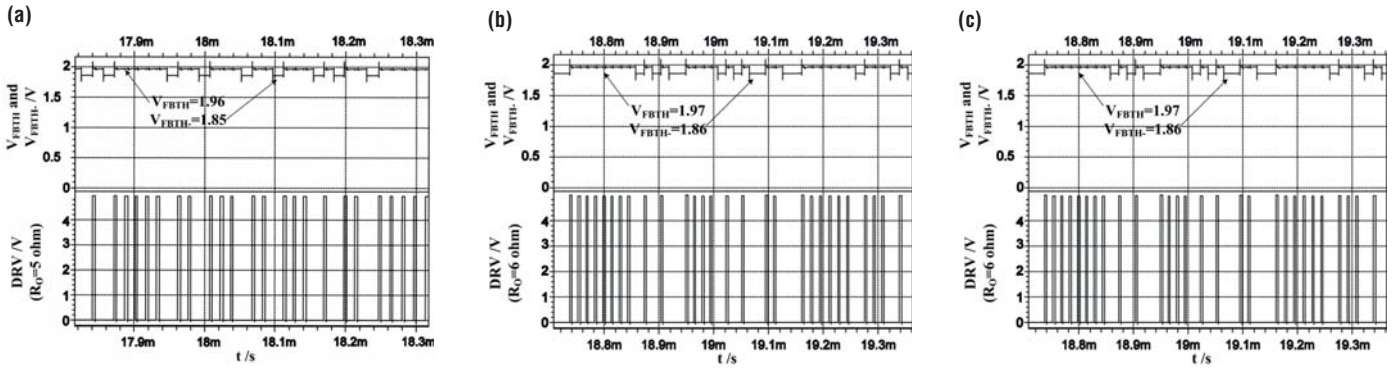


Figure 15: Simulated V_{FBTH} and V_{FBTH}- when the load is 5Ω, 6Ω and 7Ω respectively: (a) V_{FBTH} and V_{FBTH}- at 5Ω; (b) V_{FBTH} and V_{FBTH}- at 6Ω; (c) V_{FBTH} and V_{FBTH}- at 7Ω

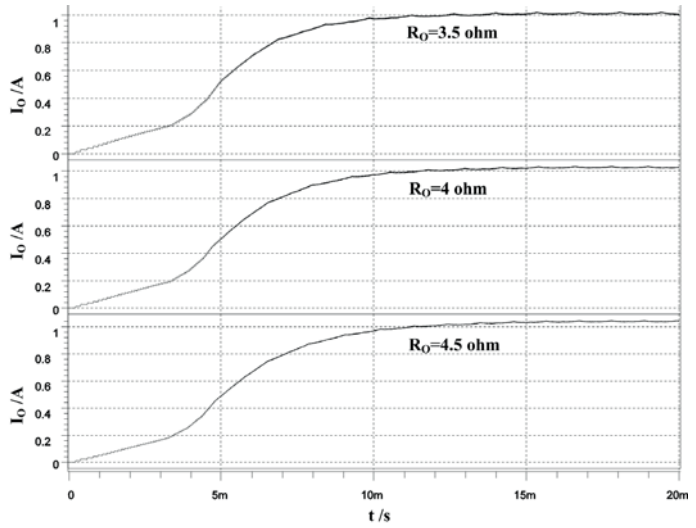


Figure 16: Simulated CC when the load is 3.5Ω, 4Ω and 4.5Ω respectively

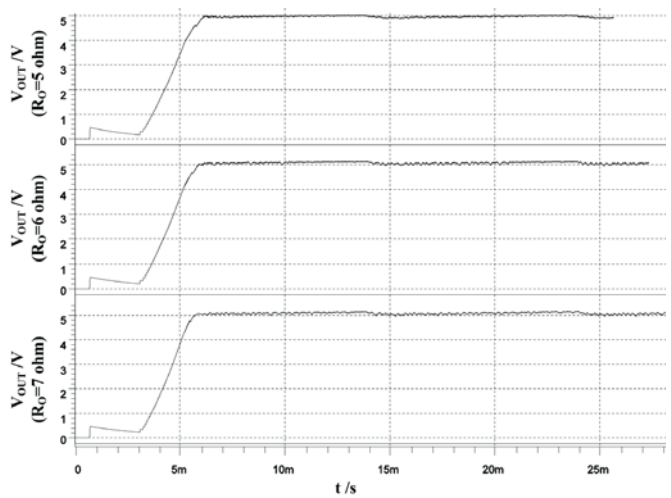
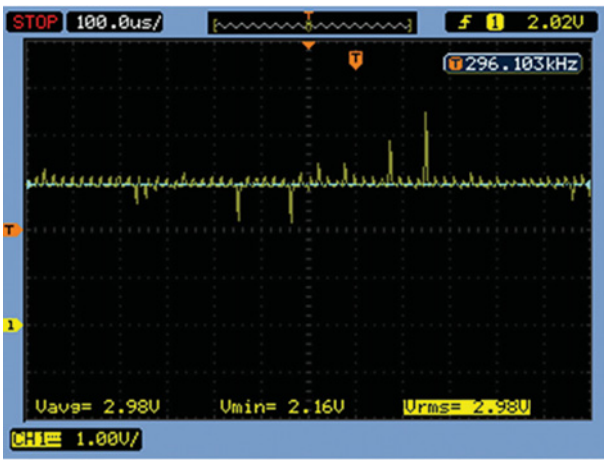


Figure 17: Simulated CV when the load is 5Ω, 6Ω and 7Ω respectively

(a)



(b)

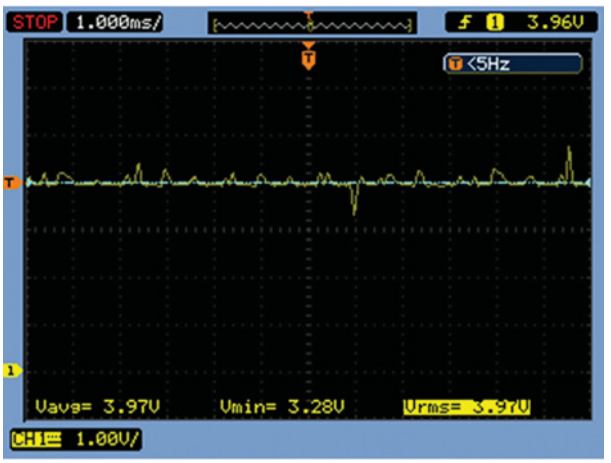


Figure 18: Test waveform of CC with cable volage drop compensation: (a) Output current at 3Ω; (b) Output current at 4Ω

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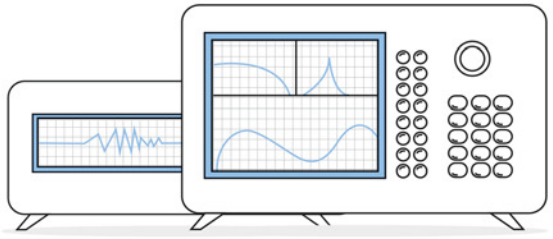

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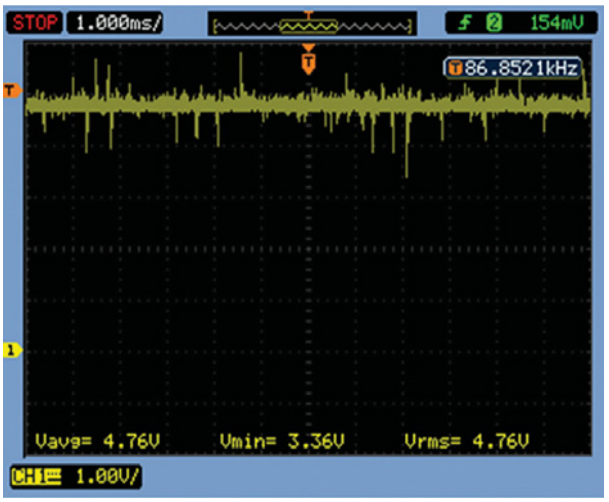
Test Results

To measure V_{FBTH}, the proper voltage across all pins has to be configured and the FB pin voltage raised until cycle skipping occurs at V_{out}. To measure V_{FBTH-}, the FB pin voltage needs to decrease until cycle skipping stops at V_{out}. V_{FBTH} is 1.97V and V_{FBTH-} is 1.87V at room temperature. The cable voltage drop compensation factor is 1.05 and the relative error is less than 1%.

As shown in Figure 18, the output current is 0.99A at the end of the 0.3Ω AWG cable of the example 5V 1A DC power supply with 3Ω and 4Ω loads respectively. In Figure 19, the output voltage without cable voltage drop compensation is 4.76V and 4.78V respectively, at the end of the 0.3Ω AWG cable of the example 5V 1A DC power supply with 5Ω and 7Ω loads respectively. However, as shown in Figure 20, with cable drop compensation the output voltages are 4.97V and 4.98V at the end of the 0.3Ω AWG cable of the designed 5V 1A DC power supply with 5Ω and 7Ω loads respectively. These results show that the proposed circuit compensates well for cable voltage drop. Table 3 shows the parameters for front and rear end of the cable compensation.

This circuit offers advantages over traditional methods, such as simple design that can conveniently be applied to a feedback circuit of a switched-mode power supply, including but not limited to flyback, forward, half-bridge and full-bridge converters. ●

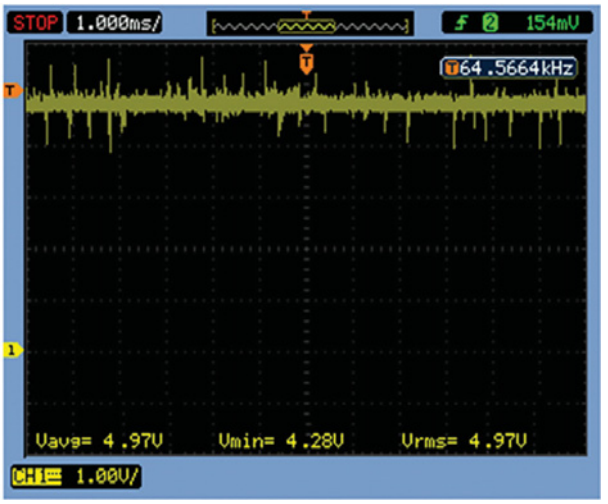
(a)



(b)

Figure 19: Test waveform of CV without cable voltage drop compensation: (a) Output voltage at 5Ω; (b) Output voltage at 7Ω

(a)



(b)

Figure 20: Test waveform of CV with cable voltage drop compensation: (a) Output voltage at 5Ω; (b) Output voltage at 7Ω

REVIEW OF MULTILEVEL INVERTER TOPOLOGIES, CONTROLS AND APPLICATIONS

BY **LU ZHENG, OUYANG HONGLIN** AND **XIAO MUXUAN** FROM HUNAN UNIVERSITY, CHINA

Middle-to-high-power AC motor speed adjustment systems are increasingly being used in various heavy industries including steel rolling, papermaking, cement plants, coal, railways and ship-building. Such a system not only conserves energy but improves process conditions, product quality and productivity.

Equally, using a middle-to-high-voltage, high-capacity, variable frequency speed control systems reduces exhaust emissions from city subways, high-speed rail, light rail and electric vehicles. This is one of the most direct and effective means of solving environmental pollution problems.

Because of the wide use of power electronics equipment and non-linear loads in power systems, reactive and harmonic pollution caused to the power grid are on the rise. The power grid's features such as its large scale, long distance and ultra-large capacity add to safety and stability issues.

Two methods that help overcome these problems are flexible AC transmission system (FACTS) and managing the reactive and harmonic pollution or, more specifically, unified power flow controller (UPFC) and active power filter (APF) based on high-voltage, high-capacity multilevel inverters. These methods have made the multilevel inverter a research hotspot for power electronics, along with its applications in middle- to high-frequency control and power systems.

Multilevel Inverter Topologies

The neutral point clamped three-level inverter was proposed by the Japanese scholar A. Nabae in 1980, followed by three other types of utility multilevel inverter topologies: diode-clamped, flying capacitor and cascaded H bridge; see Figure 1.

A diode-clamped multilevel inverter consists of diodes connected in series that crossover at the swings of the positive and negative bridge arms, clamping the output voltage. There is only one switch per arm at any one time, thus the inverter can output multilevel voltages. However, the disadvantage of this setup is that capacitor voltages are unbalanced.

Similarly, the flying capacitor multilevel inverter uses capacitor voltage for clamping. With the introduction of the capacitor, the options for synthesizing the voltages are increased and there are more flexible switching states. Disadvantages, however, include increased inverter size, cost and packaging.

The cascaded multilevel inverter consists of a number of H bridges in series, without any clamping diodes or capacitors, avoiding the issue

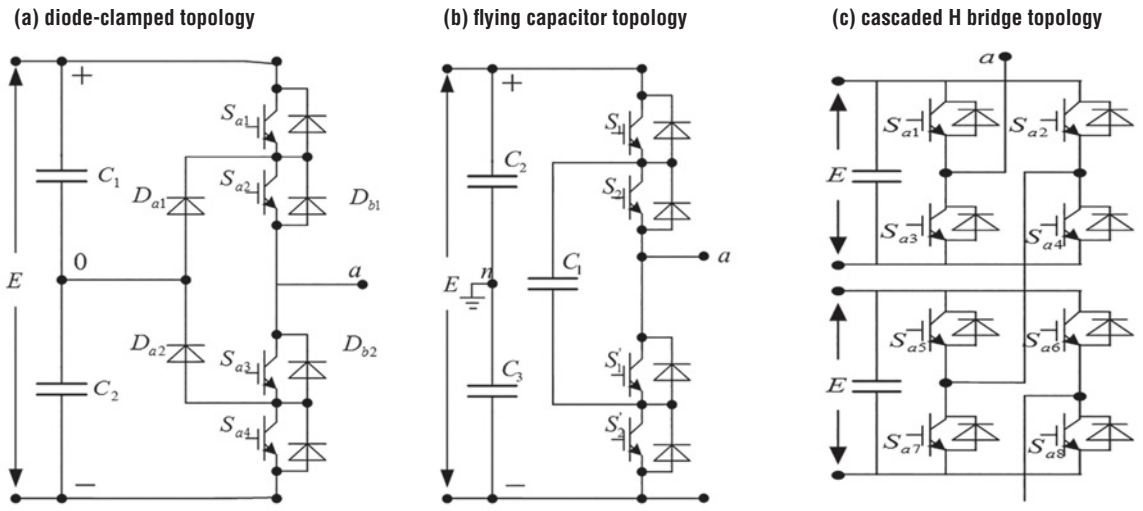


Figure 1: Three basic topology structures of a multilevel inverter

of unbalanced capacitor voltage. This topology requires the lowest number of components, it's easy to build and allows power device modularity and convenient maintenance. It also enhances the output voltage and reduces harmonic content. But among its disadvantages are the need for multiple independent DC sources and the fact that it can't realize a four-quadrant operation system drive.

Apart from the three traditional multilevel inverter topologies discussed here, there are many other improved topologies proposed in the literature. More recently, a new topology named modular multilevel converter (MMC) appeared in industrial applications, based on several two-level voltage source inverter arms (half-bridge converters) in series in a single phase. It is especially suitable for HVDC transmission systems.

In the last ten years, two-level pulse width modulation (PWM) methods have been extended to multilevel inverter designs. The most commonly used methods can be divided into three classes: carrier PWM (CPWM), selective harmonic elimination PWM (SHEPWM) and space vector PWM (SVPWM). Figure 2 shows the classification of modulation methods; the SHEPWM uses low switching frequency modulation, with the rest being high switching frequency modulation schemes.

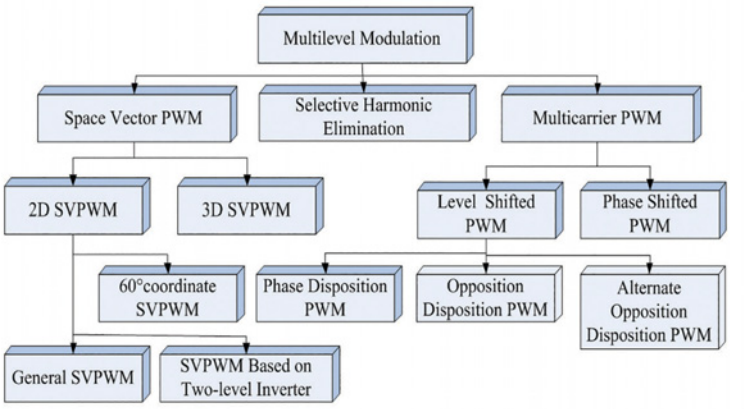


Figure 2: Multilevel inverter modulation classification

Applications

Diode-clamped multilevel inverters are widely used to drive traditional high-power AC motors, such as conveyors, pumps, fans and mills, providing effective solution in various industries including oil, gas, metals, power, mining, water, marine and chemistry.

Flying capacitor multilevel inverters are usually used in high-bandwidth, high-switching frequency applications, such as medium-voltage traction drives. Since cascaded H-bridge multilevel inverters are expandable, they are used in active filter and reactive power compensation applications, electric and hybrid vehicles, photovoltaic power conversion, uninterruptible power supplies and magnetic resonance imaging, among others.

Multilevel inverters occupy a certain market for medium- to high-power applications.

Future developments can be summarized as follows:

Power devices based on wide band-gap semiconductor materials

Compared to electronics devices made of silicon, devices made of wide band-gap semiconductor materials have higher voltage endurance, lower state resistance, better heat conductivity, better stability, greater radiation and high temperature tolerance, making them particularly suitable for high-voltage and high-temperature applications. Studies are focusing on SiC and GaN, which promise to significantly improve the performance of multilevel inverters.

Combination of multilevel inverter technology and polyphase machines

In the last decade, the polyphase machine has attracted a great deal of attention because of properties such as high reliability, high fault-tolerance, better torque performance and higher power densities. Such features are highly suitable for propulsion systems in ships. Even better would be devices that combine multilevel invert technology and polyphase machines. Studies have shown that increasing multilevel inverter output voltage levels can improve the performance of current and torque pulsations in polyphase machines.

Using multilevel inverters on distributed power generation systems

Distributed power generation systems are low cost, flexible, easily fitted into the environment, highly compatible with large power grids and, above all, have brought a huge change to the operation and control of modern power systems. Such technologies have become essential to the development of modern-day power systems.

However, in order to integrate and interconnect several power grids, an intelligent grid structure must be adopted. Such structures can now run on higher voltages and wider power ranges.

Universal flexible power management (UNIFLEX-PM) systems based on three-phase cascaded H-bridge multilevel converters offer the biggest opportunity for interconnecting different power grids. In addition, the new modular multilevel voltage source converter (MMVSC) that has emerged in recent years is also suitable for connecting distributed power generation systems to main grids. Modular construction not only benefits mass production, it also extends the capacity of converters.

Development toward fault diagnosis and intelligent, modular, systems

Making multilevel inverters modular also allows for simplified hardware, thanks to a combination of digital signal processors (DSPs) and microcontrollers (MCUs). Intelligent algorithms make controlling multilevel inverters easier, and complex control rules can readily be realized. Such advancements will make possible self-fault diagnostic capabilities and self-protect and self-monitor functions. So, the trend toward modular and more intelligent multilevel inverters will become even more important in the future.

IMPROVED POWER-FLOW CONTROL FOR A GRID-CONNECTED MICROGRID

AMIRREZA NADERIPOUR, ABDULLAH ASUHAIMI MOHD ZIN AND **MOHD HAFIZ BIN HABIBUDDIN** FROM UNIVERSITI TEKNOLOGI MALAYSIA PRESENT A DUAL-LOOP METHOD

Despite many advantages offered by traditional power systems, an increasing number of challenges face them, including depletion of fossil-fuel resources, poor energy efficiencies and environmental pollution.

Green generation technologies such as wind and solar power offer technical, environmental and economic benefits, making them suitable for generating power locally. However, the trend to generate power using renewable energy resources (RERs) has its own challenges, mainly related to reliability and secure operation.

More recently, industry has focused on implementing modular active distribution networks for flexible and intelligent operation in microgrids. A microgrid can be defined as a cluster of distributed generation (DG), loads, power electronic devices and energy storage systems. A microgrid can provide energy independence, choice of generation, energy cost control and other benefits to its owners and users. It can operate in both grid-connected and autonomous modes, and it can handle transitions between these two modes.

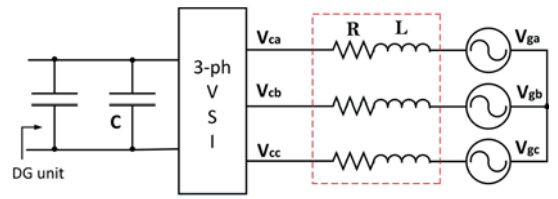


Figure 1: Grid-feeding power converter

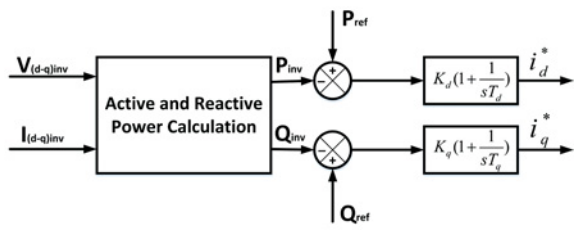


Figure 2: Outer power control loop

Microgrid Operation

Microgrids generate power from RERs locally, at distribution level, and they integrate RERs into the utility distribution network. RERs can be natural gas, bio-gas, solar photovoltaic (PV) cells, fuel cells, wind power, or heat and power systems combined. Power electronic converters are widely used to connect, control and integrate DG units into a microgrid. Microgrids operate intelligently in both grid-connected and island modes, so it is important they use proper control schemes for improved reliability and stability.

In grid-connected mode, the frequency and voltage of the microgrid are determined by the utility grid. In this mode, the main responsibility of the control unit is to regulate the active and reactive power generated by the distributed energy resource (DER) units. Any power deficit can be supported by the utility grid, whilst excess power generated within the microgrid can be transferred to the utility grid. This power exchange should be performed in a controlled manner.

On the other hand, the voltage and frequency of an autonomous microgrid should be controlled using DERs, because such variables are no longer supported by the utility grid. Moreover, island operation requires the implementation of appropriate load-sharing mechanisms to balance sudden active power mismatches.

For the purposes of this article, we considered power converters that operate as a high impedance current source connected to a utility grid. Commonly, these grid-feeding power converters deliver active and reactive power to an energized grid. Most RERs, such as PV or wind power, operate in grid-feeding mode, since they cannot independently form an autonomous mode. Voltage regulation of the power delivered to the utility grid is the main responsibility of the controller units in these power converters. It can be implemented using an inner current loop to regulate the current injected into the utility grid and an outer power loop to control the power delivered to the utility grid.

A considerable amount has been published on controlling the grid-connected microgrids such as the Newton-Rapshon repetitive iteration, the spatial repetitive controller, the

hysteresis controller and the proportional-resonant (PR) controller. Even though the PR controller is easy to implement, it has certain drawbacks, the main ones being its exponentially decaying response to step changes, great sensitivity and likelihood of phase shift instability in the sensed signals.

The hysteresis controller brings a fast response, but it suffers from variable switching frequency. The repetitive controller is also used with a pulse width modulation (PWM) rectifier to reduce high-frequency periodic components in the current-tracking error. Even though the method is effective, control algorithm complexity limits its applications range.

We designed a dual-loop control strategy based on the synchronous reference frame proportional-integral (SRFPI) approach to control the power flow in a grid-connected microgrid. The proposed controller contains an outer power loop and an inner current compensator to regulate the flow of active and reactive power and inject clean current into the utility grid. Furthermore, an effective method is applied to accurately synchronize the grid-feeding power converter with the utility grid. A phase-locked-loop (PLL) is also applied in the control scheme to detect the phases of the grid voltage.

Modeling The Inverter

The main purpose of this study is to improve control of the power delivered into the utility grid. To control the injected current, the power converter operates in grid-feeding mode. Since the inverter is assumed to be powered by a constant DC power source, no controller is required to adjust the DC link voltage.

The power circuit of the grid-feeding power converter and its filter are shown in Figure 1, where L and R are the filter's inductance and equivalent lumped resistance, respectively.

The proposed control strategy involves an outer power control loop, an inner current loop and a feed-forward voltage path. The purpose of the power control loop is to regulate the power flow between microgrid and utility grid, in case of injected active and reactive power to either the local load or the grid. Indeed, the outer loop is used to generate the reference current vectors for the inner loop in the synchronous reference frame. The inner current loop is also employed to ensure appropriate tracking and short transients of the inverter output current.

To allow the inverter voltage to match the grid voltage when the circuit breaker is off, a voltage feed-forward is added after the current controller in the abc reference frame; this can enhance the steady-state and dynamic performance of the control system.

Power Control Strategy

The types of DERs in a microgrid can be varied based on operating mode, type of power generation technology and system topology. Generally, DERs and conventional large generators differ considerably, not only in scale, but also in the way they generate electricity – traditional large generators are synchronous machines with a fixed frequency.

DERs, on the other hand, may be categorized into three main groups: variable frequency (e.g. wind turbines), high-speed frequency (e.g. small gas turbines) and direct energy conversion sources (e.g. PV arrays). These units can be further classified based on their controllability, whether they contain non-controllable and controllable units. The output of resources such as wind turbines and PV units is non-controllable; in contrast, battery energy storage systems (BESS)can be controlled fully. Normally, non-controllable units are suitable to operate in grid-connected mode. Here,

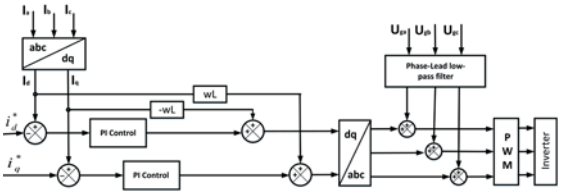


Figure 3: Current control loop

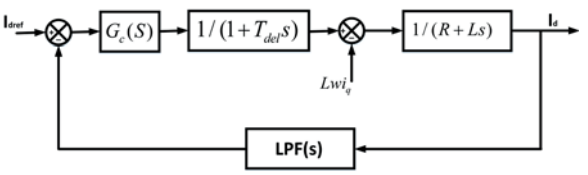


Figure 4: Closed-loop current controller for the d-axis

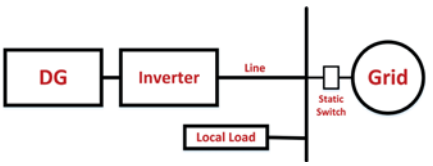


Figure 5: Microgrid test system

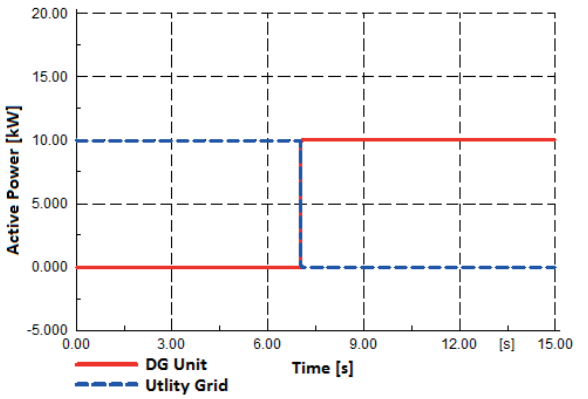


Figure 6: Output active powers of DG unit and the utility grid

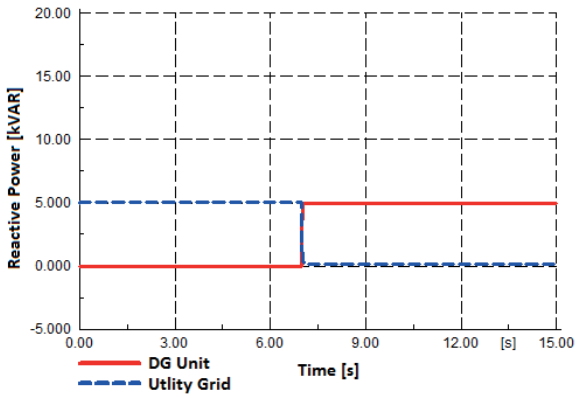


Figure 7: Output reactive powers of DG unit and the utility grid

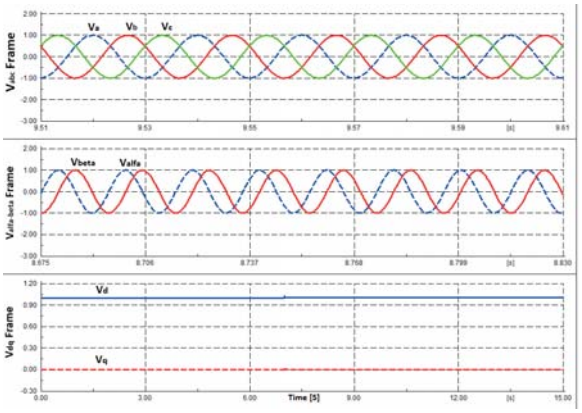


Figure 8: The output reactive powers of DG unit and utility grid

the inverter is controlled to inject preset active and reactive power values into the utility grid. These reference values can be determined either locally or using a central controller.

Figure 2 shows the proposed outer power control loop. The main objective of this loop is to manage the power flow between microgrid and utility grid. As can be seen that the outer loop is implemented using two independent proportional integral (PI) controllers to generate the reference current vectors for the inner current controller in the synchronous reference frame. First, the values of active and reactive power are measured using the active and reactive power calculation blocks. Then, two PI controllers are added in the dq frame in which control variables are no longer a function of time to regulate the active and reactive power of the inverter output independently, after comparison between measured values with preset active and reactive power values.

Current Control Strategy

The current control system shown in Figure 3 uses a separate controller for each component in the dq reference frame to ensure appropriate tracking and short output transients.

Two PI controllers are used to regulate I_d and I_q so that current injected into the utility grid can track the reference currents. As mentioned before, these reference currents are generated from the power control unit. The real and reactive powers exchanged with the utility grid are determined by I_d and I_q, respectively. To enhance performance, cross-coupling terms are also added to the system.

In order to detect the phase information of the grid voltage, a PLL is applied in the control scheme. When the reference currents generated from the power controller are zero, the generated voltage through the inverter must equal the grid voltage. In other words, the inverter must be synchronized with the utility grid in all circumstances. For this reason, the grid voltages are fed-forward to the current controller output through a low-pass filter. The filter has a gain of 1 and a phase lead at the fundamental frequency to improve the power quality of the microgrid. It also enhances the steady-state and dynamic performance.

A simplified block diagram of the closed-loop current controller for the d-axis is shown in Figure 4, where $G_c(s)$ is the transfer function of the current controller. The overall effect of the hardware anti-aliasing filter can be approximated by a low-pass filter block as:

$$LPF(s) = \frac{1}{1+T_{Fc}s} \quad (1)$$

where T_{Fc} is the time constant. PWM modulator delay and the sampling and calculation time of the discrete control system are included in this model as a pure time delay (T_{del}). The filter of the inverter is represented by (1/(R+Ls)).

Assuming a PI controller with gain k_c and integrating time constant T_c for $G_c(s)$, open current loop for the inner controller in d-axis can be approximated by:

$$H(s) = \frac{k_c(T_cs+1)}{T_cs} \frac{1}{1+(T_{Fc}+T_{del})s} \frac{1}{R+Ls} \quad (2)$$

In order to obtain the parameters of the open-loop transfer function, we apply the extended symmetrical optimum (ESO) approach. This method provides the maximum possible phase margin (PM) at a specific control crossover frequency, w_{cc}, by optimum shaping of the control loop bode plots. Therefore, the best choice of control parameters is:

$$T_c = \frac{b^2T\Delta}{1+m^2} \quad (3)$$

$$k_c = \frac{R\Delta}{bm} \quad (4)$$

$$W_{cc} = \frac{1}{b(T_{Fc}+T_{del})} \quad (5)$$

Based on these equations, and choosing an accurate PM to obtain a sufficient stability margin and fast dynamic response, b and consequently the parameters of the PI controller can be determined. In this study, the current controller parameters are calculated based on PM = 45°.

Simulation Results

To validate the performance of the suggested control scheme, the test system in Figure 5 is simulated in DIgSILENT Power Factory software. This microgrid contains a grid-feeding power converter and a sensitive load connected in parallel to the local bus, and connected to the utility grid through a static switch.

The grid-feeding power converter is equipped with the proposed control scheme; the local load type is resistive. Different simulation case studies under various scenarios were carried out to determine the effectiveness of the suggested control scheme.

At t = 7s, the grid-feeding power converter starts to operate in grid-connected mode. We want the local load to be shared based on the designed control mode of the DG unit. For this simulation, the control system is designed so 100% of the local load is powered by the DG unit. In other words, the grid-feeding power converter is capable of supplying the whole required active and reactive power of the local load. At this stage, the local load is set to 10kW active power and 5kVAR reactive power; so, the set-points of the active and reactive power for the power control unit are 0.2 per unit and -0.1 per unit, respectively.

The output active power flow for the grid-feeding power converter and utility grid are shown in Figure 6. The resulting controlled reactive power flow for the DG unit and utility grid is shown in Figure 7.

Although the DG unit is responsible for supplying the required reactive power of the local load after t = 7s, the utility grid still injects reactive power into the microgrid, due to the reactive losses across the series impedance between microgrid and utility grid.

The three-phase output voltage of the grid-feeding power converter in three different reference frames is shown in Figure 8. Figure 9 shows the behaviour of grid-feeding converter currents in the dq frame, after starting to supply the local load.

Load Change During Grid-Connected Mode

In this simulation, the local load is increased to 15kW active power and 7.5kVAR reactive power at t = 10s. Here, the set-points of the active and reactive power are changed from 0.2 per unit and -0.1 per unit to 0.1 per unit and -0.05 per unit at t = 5s, respectively.

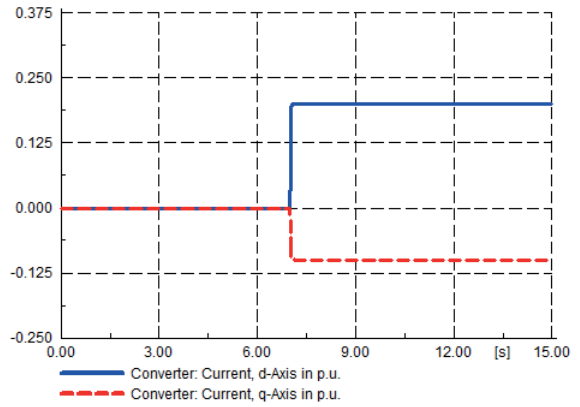


Figure 9: Currents of grid-feeding power converter in the dq frame

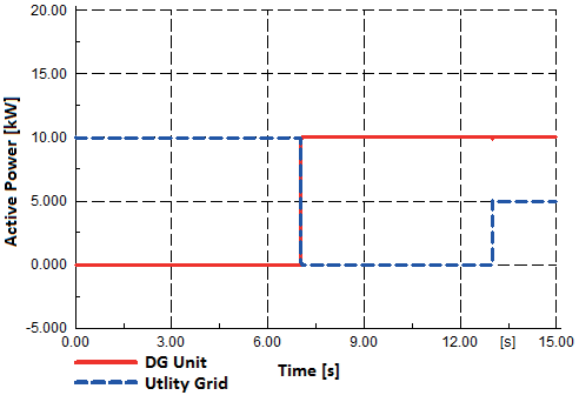


Figure 10: The output active power of DG unit and the utility grid

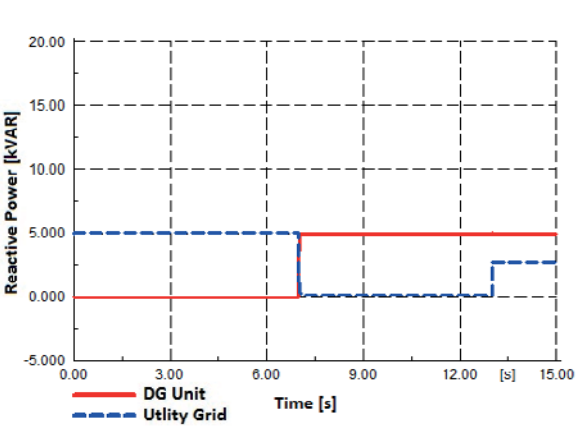


Figure 11: The output reactive power of DG unit and the utility grid

Figures 10 and 11 show the supplied active and reactive power by the grid-feeding power converter and utility grid, respectively. The simulation results show that the proposed control strategy based on a SRFPI controller is excellent at managing the power flow between microgrid and utility grid.

NOVEL RECHARGEABLE BATTERY CHARGE INDICATION CIRCUIT

LIN ZHIQI AND **ZHAO JIANGTUO** OF CHANGCHUN UNIVERSITY OF TECHNOLOGY IN CHINA

DESRIBE A TWO-STAGE CHARGE INDICATION CIRCUIT BASED ON THE CONSTANT CURRENT AND CONSTANT VOLTAGE METHOD

Portability of products has become one of the most desired aspects of modern electronics and with that the focus has shifted to the performance of batteries and how to best manage them.

When it comes to battery charging, currently there are four main types of charging circuit designs: constant-current, constant-voltage, constant current and constant voltage, and pulse charging.

The constant current and constant voltage (CC/CV) charging method is characterized by short time and high charging efficiency, and is widely used by most charging circuits; it is also the focus of this article.

After reading a large number of references about rechargeable batteries, we found that regardless of the charging mode there's a lack of good circuits to indicate charging status. So we designed a CC/CV charging circuit with an LED as a reference.

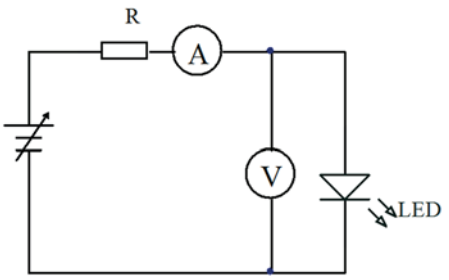


Figure 1: LED volt-ampere characteristics measuring circuit

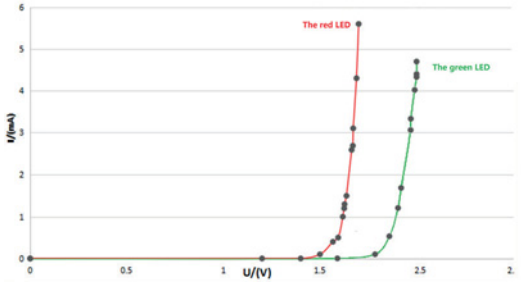


Figure 2: Curves of the positive volt-ampere characteristics of the red and the green LED

CC/CV Principle

The CC/CV charging method provides fast charging; see the curve of a lithium battery charging in Figure 1. In normal circumstances the method uses a large constant current to charge the battery. However, if the battery's voltage is lower than the threshold voltage, it will be charged with a small constant current at first. When the battery voltage rises to a set value, the charging process enters the stage of constant current, where it is necessary to monitor the battery voltage to prevent overcharging.

When battery voltage reaches the battery's rated voltage, the circuit switches to constant-voltage charging mode until charging current drops to a set value or the battery voltage is reached (these values are set by the performance of the battery) and the charging process stops.

At present, the CC/CV charging circuit mode mainly uses a linear charging circuit and a switched-mode charging circuit. The linear charging circuit typically consists of an adjustment transistor, some control circuits (for example band-gap reference, charge control, battery voltage detection, temperature detection, restart and so on), resistors and capacitors. The input source is a DC supply with small current ripple. At the same time, the linear charging circuit itself has feedback-regulating functions that can lessen the current ripple of the power, removing the need for a filter, resulting in a simpler structure and lower cost than a switching charging circuit. However, the voltage difference between the input voltage of the linear charging circuit and the voltage of the lithium battery is applied to both ends of the adjustment transistor (source and drain). Thus, the biggest drawbacks of the linear charging circuit are its larger power consumption and lower efficiency.

The switched-mode charging circuit has lower power consumption and higher efficiency both in the wide input voltage range of its power source and the entire battery voltage range.

Typically, the switched-mode system consists of a constant current charging circuit and constant voltage charging circuit, compensation network, pulse width modulator, logic control circuit and other components. Its structure is more complex than that of the linear control system and there's been less research on switched-mode-based charging circuits.

LED Volt-Ampere Characteristics

Light emitting diodes (LEDs) are semiconductor devices that emit visible light when powered. They are energy-saving, with a very long life, so they are better for the environment, quite inexpensive, easy to make and so on.

Red LED			Green LED		
Order number	U/(V)	I/(mA)	Order number	U/(V)	I/(mA)
1	1.400	0.00	1	1.400	0.00
2	1.500	0.10	2	1.500	0.10
3	1.567	0.40	3	1.567	0.40
4	1.594	0.50	4	1.594	0.50
5	1.618	1.0	5	1.618	1.0
6	1.625	1.20	6	1.625	1.20
7	1.627	1.30	7	1.627	1.30
8	1.637	1.50	8	1.637	1.50
9	1.664	2.60	9	1.664	2.60
10	1.670	2.70	10	1.670	2.70
11	1.672	3.10	11	1.672	3.10
12	1.689	4.30	12	1.689	4.30

Table 1: Measured data of positive volt-ampere characteristics for red and green LEDs

We used LEDs as indicators in our circuit. To begin the design, through experiments we determined the volt-ampere characteristics of red and green LEDs; see Table 1. Figure 2 shows the volt-ampere characteristics for the two LEDs to determine the turn-on voltage for each. We found that the red LED turns on at around 1.7V and the green around 2V.

Circuit Design

Our circuit is shown in Figure 3.

We know that:

$$R_1 \bullet I_{VT1BE} + U_{VT1BE} = U_{VD1}$$

or

$$I_{VT1BE} = \frac{U_{VD1} - U_{VT1BE}}{R_1}$$

The input voltage powers the red LED through R2, turning VD1 on; see Figure 4. At this time, VD1 is about 1.7V and VT1's base-emitter voltage is 0.7V. When R_1 is 10Ω, the current flowing through it is 100mA and the battery begins to charge. When its value changes from 1Ω to 100Ω, the constant current charging current also changes from 1A to 100mA.

The battery's charging voltage is divided into two parts by the resistor R5, whose centre tap is connected to the base of VT3. Then:

$$U_{VT3B} = U_O \frac{R_{5b}}{R_5}$$

In R5, the upper part of the divider is R_{5a} and the lower part R_{5b}. So,

$$U_O = U_{VT3B} \frac{R_5}{R_{5b}}$$

The green LED VD2 turns on at 2V so $U_{VT3BE} = 0.7V$.

Then,

$$U_{VT3B}' = U_{VD2} + U_{VT3BE} = 2V + 0.7V = 2.7V$$

In summary,

$$U_O = 2.7V \times \frac{R_5}{R_{5b}}$$

It is clear that we can change U_o from 2.7V to 4.8V by adjusting R5.

At the beginning of charging, the voltage at VT3's base is $U_{VT3B}' = 2.7V$, which is lower than the green LED's turn-on voltage U_{VT3B}. At the same time, if VT3 is cut off, it makes the green LED turn off and VT2 turns on because of R3. Since $I_e \approx I_c$, the battery is charged by a constant 100mA. This time the circuit is working in charging mode and the red LED's VT1 is on, acting as the constant current indication; see Figure 4. In the meantime, the green LED VT2 is off.

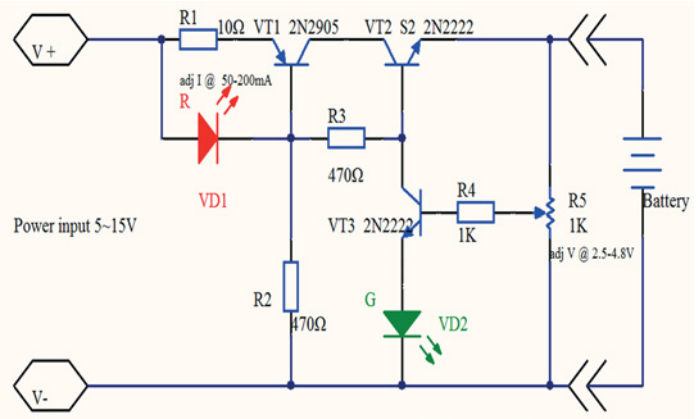


Figure 3: Constant current and constant voltage charging circuit

When the battery voltage reaches the constant voltage, the basic voltage of VT3 is higher than 2.7V, so VT3 turns on. At the same time, VD2, VT2 and VT3 turn into amplification state and they form a stabilized voltage power supply. The adjustment range of R5 is 2.7V.

When the base current of VT3 is negligible, the voltage of the battery is constant. At this time, the green LED VD2 is on (see Figure 5), indicating a constant voltage state. After reaching this state, the sum of R1's voltage drop and emitter junction voltage is lower than 1.7V and the red LED VT1 turns off. The red LED VD1 acts as a basic indicator of constant-current. Similarly, the green LED VD2 acts as a basic indicator of constant voltage charging and indication.

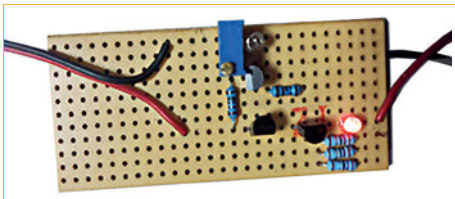


Figure 4: VD1 on

When at the stage of constant current charging, the red LED VD1 is on and the green LED VD2 is off. When constant-voltage charging, red LED VD1 is off and green LED VD2 is on, unmistakable indications of each state.

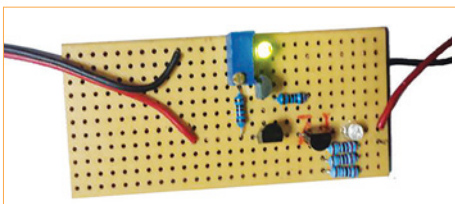


Figure 5: VD2 on

Implementation

Through experiments our circuit has proven very stable. We can change the charging current from 10mA to 1A by changing the resistance R1. We change the constant voltage by adjusting the variable resistor R5 from 2.7V to 4.8V.

Our circuit charges lithium ion or lithium polymer batteries safely, efficiently and conveniently.

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As a problem-solving connector manufacturer, ODU enjoys single-source status with over one hundred of the world's top manufacturing companies. Why is that? Because, not only does it have expertise, but it works hard at being a flexible and innovative supplier.

In the UK, ODU is probably best known for its miniature military push-pull connectors.

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ODU will be at several exhibitions this year so, if you are faced with a connector or packaging problem, then why not come and talk to its representatives, or get in touch now:

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Apacer's DRAM module technology development is focused on vertically integrating know-how in the semiconductor industry, manufacturing memory modules that satisfy the requirements of quality, performance and, yet, can be easily integrated into various platforms.

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SERIAL STANDARDS TESTING ON DPO70000SX OSCILLOSCOPES EXPANDED

Tektronix is bringing support for serial bus standards testing to the new DPO70000SX family of ultra-high performance oscilloscopes. Featuring patented Asynchronous Time Interleaving (ATI) signal acquisition technology, the DPO70000SX platform offers industry-best signal fidelity and performance, coupled with a scalable architecture that offers future upgrades as signal speeds continue to increase.

As engineering teams prepare for next-generation standards in the rapidly growing cloud computing and mobile segments, they need a measurement platform with extremely consistent and precise measurement of high-data-rate signalling schemes. To meet this need, Tektronix is enabling serial bus test support for 4th generation standards, including USB3.1, Thunderbolt over USB Type-C, PCIe Gen4 and DDR4 on the DPO70000SX Series. This new oscilloscope family offers incredible signal fidelity enabling precise margin analysis on 4th generation serial data rates beyond 10Gb/s.

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SCHOTT OFFERS THE BROADEST PORTFOLIO OF GLASS WAFERS

Special-glass expert Schott is one of the leading suppliers of thin and ultra-thin glass wafers and sheets for the semiconductor and optoelectronics industries meeting the industry standard requirements. At the international Electronic Components and Technology Conference (ECTC) from May 31-June 6 in Las Vegas, the company will present a variety of examples of products based on different materials and processing technologies (Booth 220).

Based on over 130 years of experience in developing and manufacturing specialty glass, Schott has the broadest portfolio of glass wafers and substrates. These are produced with proprietary processes, and are available in different sizes (wafer diameters up to 12˝; sheet sizes up to 510 x 510mm²) and thicknesses (from 1.1mm to ultra-thin 25µm).

Schott serves emerging industry trends in the fields of IC packaging, radio frequency (RF) components and micro-electromechanical systems (MEMS).

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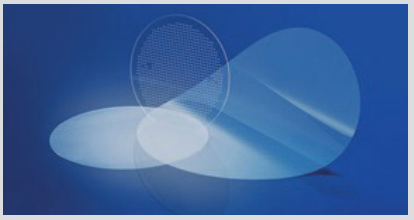

EYE DIAGRAMS ADDED TO SERIAL TRIGGER AND DECODE SOLUTIONS

Teledyne LeCroy has further expanded the serial data analysis capabilities for its oscilloscope solutions by introducing eye diagram capabilities in the new TDME serial bus options – a first on the market. Teledyne LeCroy today is offering the widest range of trigger (T), decode (D), measure/graph (M or G) and eye diagram and physical layer (E or P) options, which are nearly universally available across its entire oscilloscope product line.

An engineer can isolate events using the serial bus trigger and view colour-coded protocol information on top of analogue or digital waveforms. Timing and bus measurements allow quick and easy characterization of a serial data system. Measurement data can be graphed to monitor system performance over time and physical layer anomalies can be identified with eye diagram mask testing and mask failure locator.

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µMODULE POWER PRODUCTS WITH TIN-LEAD BGA PACKAGES

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These µModule products are available in four DC/DC converter categories: step-down or buck converters with single and multiple outputs, buck-boost converters, isolated converters and converters with PMBus digital telemetry with READ and WRITE data capability.

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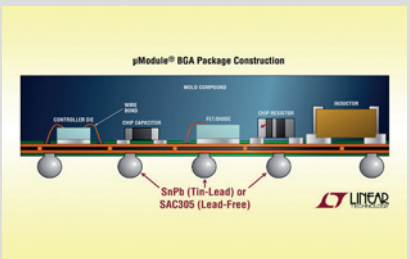

NEW 1MHZ BANDWIDTH, INTEGRATED HALL-EFFECT-BASED CURRENT SENSOR IC

Allegro MicroSystems Europe announced its first 1MHz bandwidth Hall-effect current sensor IC with a 210ns response time – the ACS730 provides an economical and precise solution for AC or DC current sensing.

The device is targeted at industrial, commercial and communications systems. Typical applications include motor control, load detection and management, switched-mode power supplies, and over-current fault protection.

The IC consists of a precise, low-offset, linear Hall-sensor circuit with a copper conduction path located near the die's surface. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimised through the close proximity of the magnetic field to the Hall transducer. A precise, proportional voltage is provided by the Hall IC, which is programmed for accuracy after packaging.

www.allegromicro.com

NXP'S INTEGRATED SINGLE-CHIP QI TRANSMITTER NOW AT MOUSER

Mouser Electronics is stocking the NXQ1TXH5 one-chip 5V Qi wireless transmitter from NXP. The NXQ1TXH5 is a fully integrated, single-chip controller and driver IC that enables engineers design a WPC 1.2 Qi-compliant low-power wireless charger with Foreign Object Detection (FOD). It includes a 5V full-bridge power stage and efficiently integrates all the functions required to control the power transfer with a Qi-compliant receiver. The NXQ1TXH5 delivers up to 8W continuous power into a Qi-compliant type A5, A11, A12, or A16 transmitter coil, and requires minimal external components, reducing application costs and enabling a simple PCB design for wireless power chargers and transmitters.

The Qi transmitter uses dedicated analogue ping circuitry to detect devices, achieving an extremely low standby power consumption of 10mW. It also provides reliable, dual-channel amplitude shift keying (ASK) communication among others.

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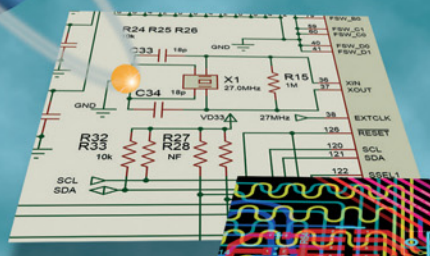

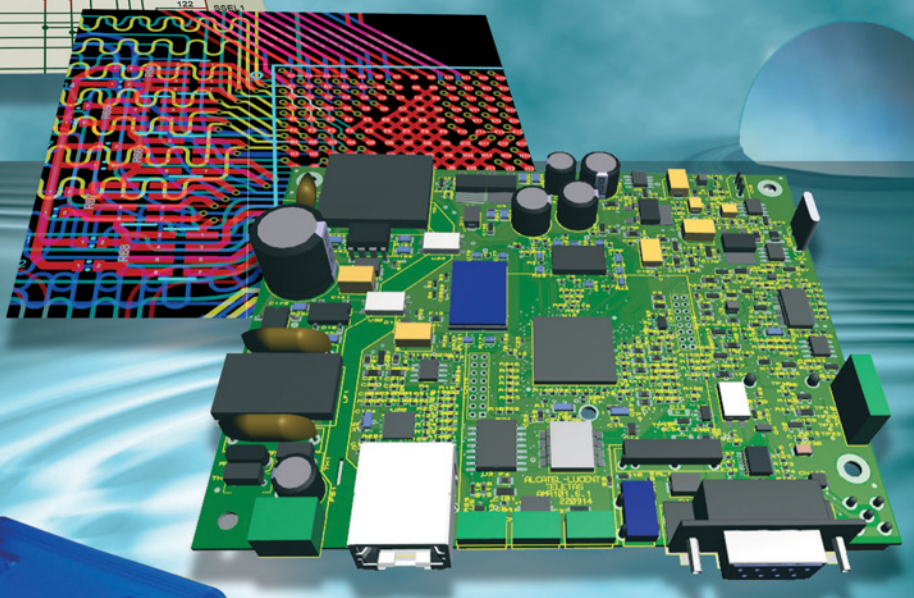

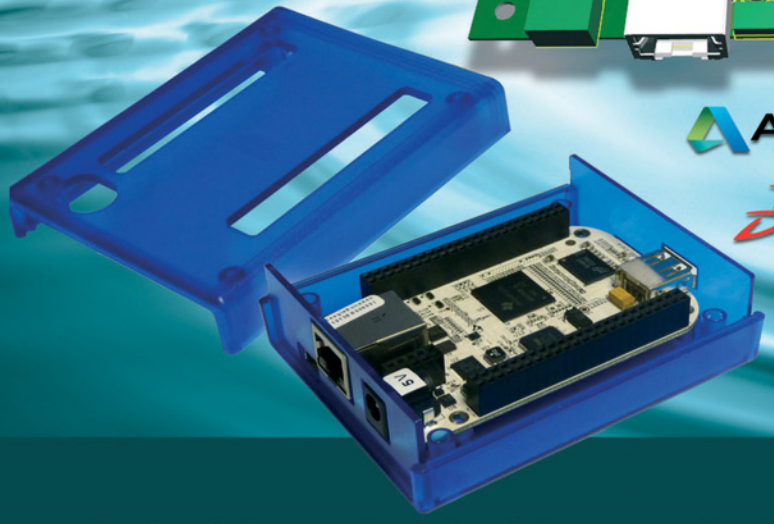

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