Electronics WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

High-Performance Mixer for 5G MIMO Receivers
by Linear Technology

5G

MIMO

LINEAR TECHNOLOGY

LTC5593

LO

SPECIAL REPORT
COMMUNICATIONS

▮ Passive Optical Networks
▮ Satellite Communications
▮ UWB Antenna Design

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Regular column
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- Meets ROHS requirements

Features

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- Will charge most devices powered by standard USB 5VDC chargers
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- Full International Safety Approvals & CE marked
- Compact Desk Top Enclosure
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FEWER ROAD ACCIDENTS SEEN AS BIGGEST BENEFIT OF DRIVERLESS CARS

More than a quarter of UK adults polled in the UK Robotics Week survey, held at the end of June, believe that the biggest benefit of driverless cars will be fewer road accidents.

 Over 26% of respondents in the survey commissioned by the EPSRC UK-RAS Network think the biggest benefit of autonomous vehicles – such as the Google Self-Driving Car – will be a reduction in the number of road accidents, and around 21% said they think road rage instances would decrease.

"While widespread advent of fully autonomous, 'never-need-a-driving-wheel' cars is some time away, the possibilities for safety, economy and efficiency is breathtaking," said Professor Paul Newman, who is leading Oxford University's Mobile Robotics Group which develops self-driving cars and related technologies.

Other key findings of the research into public attitudes to robotics advances include drivers' optimism that autonomous driving will have a positive impact on everyday commuting.

A further research into how people perceive robotics found that the automotive sector is expected to deliver the greatest benefits in the next 10 years, followed by medicine.

The research unveiled people's 'dream' roles for robots, such as more intelligent helping-hand robots for tackling chores around the house (vacuuming, ironing, cooking, etc.), but also for companionship.

The survey numbers reveal some surprising and interesting perceptions around robotics technology as the UK prepares to shine a major spotlight on the nation's innovation and leadership in robotics and autonomous systems. Of those surveyed, 43% believe robots will be able to perform surgical operations in the next 25 years and over a third (35%) think robots will be able to talk and have a conversation.

Commenting on the release of the survey results, Professor Guang-Zhong Yang, Chair of the EPSRC UK-RAS Network,

> Advances in technology will inevitably change the nature of workforce, replacing certain types of jobs whilst creating new opportunities in the process

said: "Advances in technology will inevitably change the nature of workforce, replacing certain types of jobs whilst creating new opportunities in the process. A national level engagement is essential to ensure the general public has a clear understanding of current and future development of robotics and artificial intelligence and their positive impact on UK jobs and economic growth. At the same time we need to be open and prepared for the changes in workforce structure and shift in the skills base by developing a national programme to address the digital skills gap."

UK Robotics Week is held annually during the last week of June, and is a good opportunity to learn about the current state-of-the-art robotics technologies, discuss the role of robots and artificial intelligence, and to inspire the next generation of designers and engineers.

UK Robotics Week culminates in a celebratory international showcase event in London, which brings together the latest research from the UK and from around the world, offering talks and demonstrations from leading robotics nations including Japan, the United States, South Korea, China, Italy, Switzerland and United Arab Emirates.

The event also includes an awards ceremony for the four robotics challenges – 'School Robot', 'Autonomous Driving', 'Surgical Robot' and 'Field Robotics'.

For information about UK Robotics Week visit www.roboticsweek.uk

CASTOR BEANS MAY BE AT THE HEART OF NEW-GENERATION MATERIALS FOR ELECTRONIC DEVICES

Science-based company Royal DSM has extended its range of high-temperature-resistant bio-based polymers with ForTii Eco — a new family of high-performance polyamide 4T materials, partially produced from renewable resources. The new materials fit the growing need for faster, thinner and more sustainable devices in the electronics industry.

On average, smart phones are getting 12% thinner every year, whilst speed and functionality continue to increase, and yet there is a growing demand for more sustainable devices. DSM's entire portfolio for the electronics industry is already free of halogens and red phosphorous, materials typically found in cables, connectors, frames and antennas of electronic devices.

DSM's products are mainly based on two materials, a thermoplastic elastomer and polyamide 410, which are partially or fully derived from renewable resources, such as castor beans. The company's new ForTii Eco grades provide increased performance compared to alternative mineral oil-based solutions, and meet more stringent requirements on properties like flow, mechanical and dielectric strength.

The ForTii Eco LDS62 grade is highly suitable for producing mobile electronics antennas, as it makes possible very fine and precise electrical circuitry through highly cost-effective laser direct structuring. Other applications include surface-mount technology (SMT) connectors — such as the new USB-C, audio jacks, RFID security casings and switches found in many portable electronic devices.

Are castor beans the new material for electronic devices?

DEMO OF 3D 'BLACK BOX' TECHNOLOGY FOR VEHICLES

UK-based Roke Manor Research demonstrated the world's first viable 3D 'black box' technology for vehicles this July.

Fitted to an autonomous Toyota Prius, Roke demonstrated how data captured from a single dashboard camera, combined with image processing algorithms, can be used to provide a precise 3D reconstruction following a road incident.

"Unlike current dashcams, the technology we tested today uses computer vision algorithms to determine the precise position and orientation of any vehicle – car, bike, lorry. This allows for near-perfect 3D reconstruction of any accident to be created even if the vehicle loses complete control," said Dr James Revell, Roke Consultant Engineer.

The black box will offer insurers and drivers, not to mention autonomous vehicle manufacturers, independent evidence related to an incident. This will not just lead to safer vehicles but also help to build public trust in driverless vehicles.
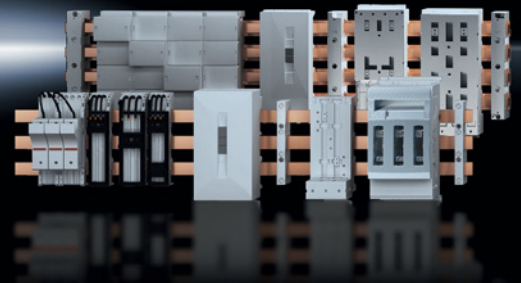
Early iterations of this technology were first developed by Roke for soldiers, in research undertaken for the UK government's Defence Science and Technology Laboratory.

COOLING GRAPHENE-BASED FILM CLOSE TO PRODUCTION

Researchers at Sweden-based Chalmers University of Technology have developed an efficient way of cooling electronics using functionalized graphene nanoflakes.

"Essentially, we have found a golden key with which to achieve improved heat transport in electronics and other power devices using graphene nanoflake-based film," said Johan Liu, Professor of Electronics Production at Chalmers. "This opens up potential uses of this film in broad areas, and we are getting closer to pilot-scale production based on this discovery."

The researchers studied the heat transfer enhancement of the film with different functionalized amino-based and azide-based silane molecules, and found that the heat transfer efficiency of the film can be improved more than 76% by introducing functionalization molecules, compared to a reference system without the functional layer. This is mainly because the contact resistance was drastically reduced by introducing the functionalization molecules.

Meanwhile, molecular dynamic simulations reveal that the functional layer constrains the cross-plane scattering of low-frequency phonons, which in turn enhances in-plane heat-conduction
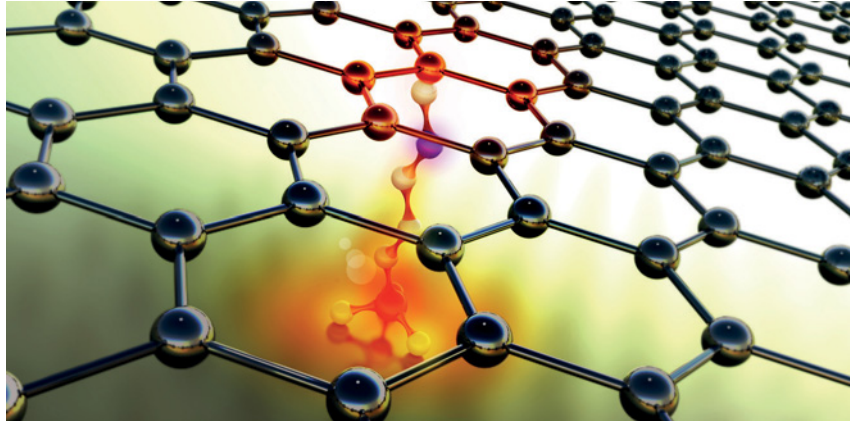
Heat transport of graphene nanoflakes
[Photo source: Johan Liu; Credit: Philip Krantz, Krantz Nanoart]

of the bonded film by recovering the long flexural phonon lifetime. The results suggested potential thermal management solutions for electronic devices.

Heat dissipation in electronics and optoelectronics is a severe bottleneck in the further development of systems in these fields, so the results of the research at Chalmers are seen as very promising.

MOLECULES FUNCTIONALIZATION
Functionalization is the process of adding new functions, features, capabilities or properties to a material by changing its surface chemistry. Functionalization is performed by attaching molecules or nanoparticles to the surface of the material, sometimes with a chemical bond or adsorption, where the particles stick to the surface without forming a covalent or ionic bond.
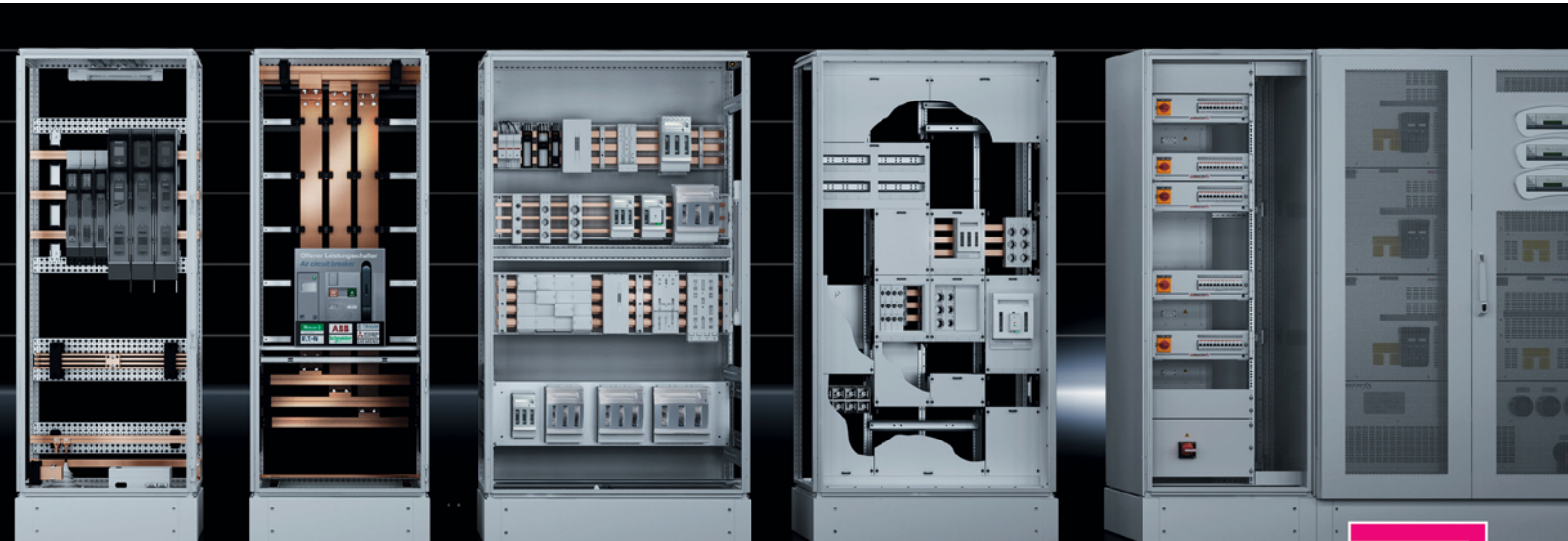
HIGH-PERFORMANCE MIXER FOR 5G MIMO RECEIVERS

By Bill Beckwith, Staff Scientist, Xudong Wang, Senior RFIC Design Engineer, and Tom Schiltz, RFIC Design Manager, all at Linear Technology

Global demand for ever-increasing data rates has pushed the limit of the current 4G wireless networks capacity. Next generation 5G networks will need to increase the capacity by more than 10-fold to keep up with future demand. Even though the 5G standard has not been finalized, most – if not all – market participants have concluded that bandwidth needs to increase to at least 100MHz (from the current 20MHz spectrum), or potentially even 200MHz. Doing so will push the frequency spectrum upward of 3.6GHz.

To address this need, Linear Technology's LTC5593 dual passive downconverting mixer provides excellent linearity and dynamic range performance at 3.6GHz, while supporting more than 200MHz flat signal bandwidth that makes for a superbly robust MIMO (Multiple-Input Multiple-Output) receiver. MIMO technology has demonstrated its usefulness by markedly boosting net data rate throughput and reception in systems such as Wi-Fi and 4G networks in times of limited spectrum bandwidth. As 5G systems migrate to higher frequencies, the LTC5593 provides continuous 50Ω matched from 2.3GHz to 4.5GHz, supporting multiband receivers at 2.6GHz and 3.6GHz bands.

For lower bands, other pin-compatible mixers include the LTC5590, LTC5591 and LTC5592, which cover all other LTE receivers. The frequency coverage and typical 3.3V performance of each mixer is shown in Table 1. These mixers deliver high conversion gain, low noise figure (NF) and high linearity with low DC power consumption. Typical power conversion gain is 8dB with an input 3rd order intercept point (IIP3) of 26dBm, 10dB of noise figure and 1.3W power consumption.

The LTC5593 family of dual high-performance mixers is ideal for wireless infrastructure MIMO receivers, such as in a RRH (Remote Radio Head). Such systems are extremely compact and are in self-contained, weather-sealed casing, posing challenges in small size and thermal management from the large content of electronics. The dual-channel solution reduces parts count, simplifies routing of LO signals and reduces board area. Additionally, each LTC5593 incorporates integrated RF and LO baluns, double-balanced mixers, LO buffer amplifiers and differential IF amplifiers, further reducing overall solution size, complexity and cost.

Mixer Description

The simplified block diagram in Figure 1 shows the dual-mixer topology, which uses passive double-balanced mixer cores driving IF output amplifiers. The mixer cores are switched-MOSFET quads, which typically have about 7dB of conversion loss. However, in this case the loss is more than compensated by the gain of the subsequent on-chip IF amplifiers, resulting in overall power gain of about 8dB. The differential IF output has been optimized for a standard 200Ω interface, which can drive directly differential IF filters and variable gain amplifiers, minimizing the number of external components.

The LO path uses a shared balun to convert the single-ended input to a differential LO, which then drives independent buffer amplifiers for each channel. This separate LO drive topology preserves the phase coherency of the LO signal to both mixers while providing excellent channel isolation. Additionally, to prevent unwanted load-pulling or disturbance to the VCO, a constant 50Ω LO input impedance matching is maintained in all operating modes, even when one or both mixer stages are turned on and off. A 50Ω impedance match from 2.1GHz to 3.4GHz is realized by adding a 1.5pF external series capacitor, C2. This capacitor is also needed for DC blocking.

For the higher 3.6GHz band, adding a shunt inductor of 10nH on the source side of the capacitor provides good return loss at the LO. Figure 2 shows the LO input return loss of the LTC5593, under various operating conditions. This feature eliminates the need for an external LO buffer stage.

Traditional basestations maintain a temperature-controlled environment and require that components work up to +85°C. Smaller cells and remote radio heads, however, present a harsher environment for components, requiring operation up to +105°C. The LTC5593 mixers have been designed for and tested at +105°C to meet this demand.

To minimize solution size, the LTC5593 family of mixers is assembled in a small 5mm x 5mm 24-lead QFN package. The small package size is only part of the total solution size reduction, however. The high integration level reduces the number of required external components to about 19, minimizing board area, complexity and cost.

Receiver Application

The functional diagram of an LTC5593 mixer in a two-channel receiver is shown in Figure 3. Single-ended RF signals are amplified and filtered before being applied to the mixer inputs. In this example, differential IF signal paths are shown, eliminating the need for an IF balun. The SAW filter, IF amplifier and lumped-element bandpass filter are all differential. With the circuit component values as shown, this example receiver supports

Part #	RF RANGE(GHz)	LO RANGE(GHz)	GAIN(dB)	IIP3(dBm)	NF(dB)
LTC5590	0.6 – 1.7	0.7 – 1.5	8.7	26.0	9.7
LTC5591	1.3 – 2.3	1.4 – 2.1	8.5	26.2	9.9
LTC5592	1.6 – 2.7	1.7 – 2.5	8.3	27.3	9.8
LTC5593(3.6GHz)	2.3 – 4.5	2.1 – 4.2	7.6	26.0	11.3

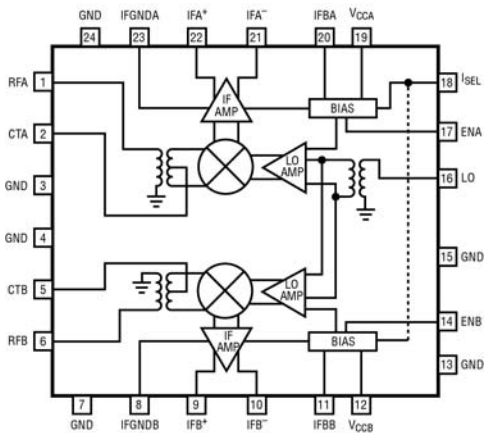Table 1: LTC559x Frequency Coverage and 3.3V Performance Summary

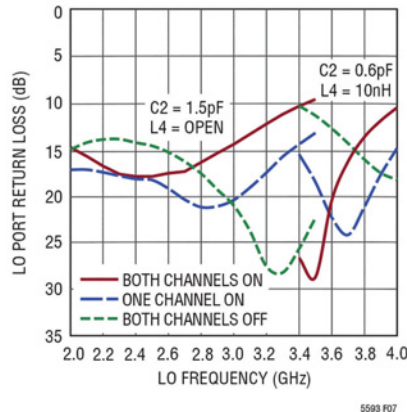**Figure 1: Block Diagram of Dual-Channel Mixer**

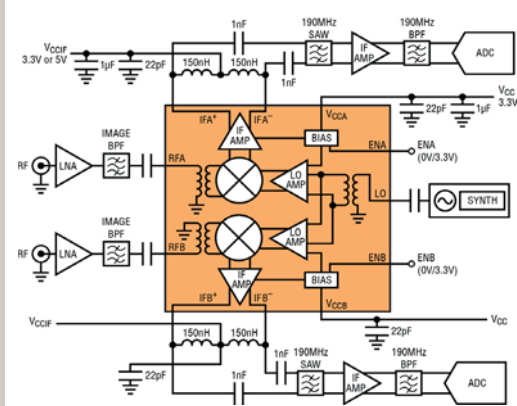**Figure 2: LTC5593 LO Return Loss for Different Operating States**

Figure 3: LTC5593 Dual Passive Mixer in a Receiver Application

150MHz IF bandwidth. Higher bandwidth can be achieved by lowering the resistance across the differential pins – with a slight reduction in gain.

High-selectivity SAW filters are used in many MIMO receivers to block unwanted spurs and noise at the mixer output. The mixers' 8dB of conversion gain compensates for the high insertion loss of these filters and reduces their impact on the system noise floor. The overall mixer performance allows the filter loss to be accommodated while enabling the receiver to meet sensitivity and spurious requirements.

Another important performance target for multichannel receivers is the channel-to-channel isolation, which is the IF level at the undriven channel's output relative to the IF level at the driven channel's output. This parameter is usually specified to be 10dB better than the antenna-to-antenna isolation to avoid degrading system performance. Based on its precise IC design, the LTC5593 achieves 44dB of channel-to-channel isolation at 3.6GHz, and 52dB at 2.6GHz, which satisfies many multichannel application requirements.

Power Consumption and Solution Size

With the maturing of multiband/multimode basestation topologies and a more refined system definition migrating from 4G to the future 5G networks, wireless infrastructure systems are moving toward platform configurations that allow implementation of various band or mode requirements with minimal hardware and software changes. The LTC559x family of dual mixers all share a common pinout, making it easy to use the same board layout for all bands.

The continued growth of wireless communications has also spurred the use of smaller cells such as picocells and femtocells. The need for smaller cells and more of them, plus the increased use of remote radio heads, has placed additional constraints on infrastructure systems, demanding higher integration and smaller solution size.

As the number of cells grows, power consumption has also become increasingly important as energy costs go up proportionally. In remote radio heads, on the other hand, thermal stress is a major concern due to reliance on passive cooling. Simply reducing the solution size is not sufficient, as reduced system size would result in higher power density, higher junction temperatures and potentially reduced component reliability. Thus, it is necessary to simultaneously reduce system power consumption and size. This goal is challenging, because the RF performance must not be compromised.

In the past, combining two individual mixers on one chip would result in total power consumption of 2 watts. To reduce power consumption, the LTC5593 family of mixers has been designed for 3.3V operation instead of 5V. Low-voltage circuit design techniques reduce power dissipation without impacting conversion gain, IIP3 or noise figure performance. The only parameter affected by the lower supply voltage is the output P1dB performance, which is approximately 10.4dBm. The P1dB is limited by the output voltage swing at the open collectors of the IF amplifiers when driving the 200Ω load impedance. For applications where higher P1dB is necessary, the mixers have been specifically designed to allow the use of a 5V supply on the IF amplifier. The higher voltage improves the P1dB to 13.7dBm.

As shown in Table 1, the dual-mixers achieve excellent performance while using just over 1.3W of power, with both channels enabled. For additional power savings, each channel can be independently shut down as desired by using the independent enable controls. In instances where reduced linearity requirements are acceptable, the ISEL pin allows the user to switch to low current mode and further decrease DC power consumption.

Conclusion

The LTC5593 dual passive downconverting mixer delivers the high performance needed to meet the demanding requirements of emerging 5G multichannel infrastructure receivers, pushing higher frequencies and wider bandwidth. The mixer's combination of high conversion gain, low NF and high linearity improves overall system performance, and low power consumption and small solution size meet the more stringent needs of ever-smaller basestations and remote radio heads.

Improving Communication And Application Robustness

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

I am quite conscious that bringing up the subject of robustness in an embedded control column is like opening the proverbial Pandora's box.

Robustness is often defined as the ability of tolerating perturbations (noise) that could affect a system. In embedded systems, including a microcontroller, there are so many ways noise can affect an application; but, in the following, I will try to focus the conversation on just two of the many facets of this problem. Specifically, this will include where noise affects communication and where it affects the reading of Flash memory content – when individual instructions are fetched for execution. Top priority in both cases is identifying errors before corrupt data is used by the application, or incorrect commands are executed. Cyclic Redundancy Check (CRC) algorithms are commonly employed for the purpose but, whilst these can be executed as software tasks, the additional workload imposed on the processor core can be significant.

As we will see, a dedicated set of core-independent peripherals can help reduce or eliminate altogether this workload, increase application responsiveness and reduce power consumption. Needless to say, we are going to use the MPLAB Xpress cloud toolchain (to avoid lengthy installations), the Curiosity demonstration board for rapid prototyping and MPLAB Code Configurator (MCC) for a quick configuration of all required microcontroller peripherals.

Brief Introduction To CRC Algorithms

As the name suggests, the idea is to perform a check on the integrity of an arbitrary block of raw data, communicated over a medium or stored in a memory, by attaching to it (hence the redundancy) a particular control code. This is obtained by applying a cyclic code – a mathematical function (polynomial division) to detect single and multiple bit errors.

The size (number of bits) of the control code is typically limited (much smaller than the block of data) to keep the communication/storage overhead low. It follows that the ability of a given CRC algorithm to detect errors is never absolute. Typically, an n-bit CRC applied to a data block of arbitrary length will detect any single error burst not longer than n bits and will detect a fraction $1 - 2-n$ of all longer error bursts.

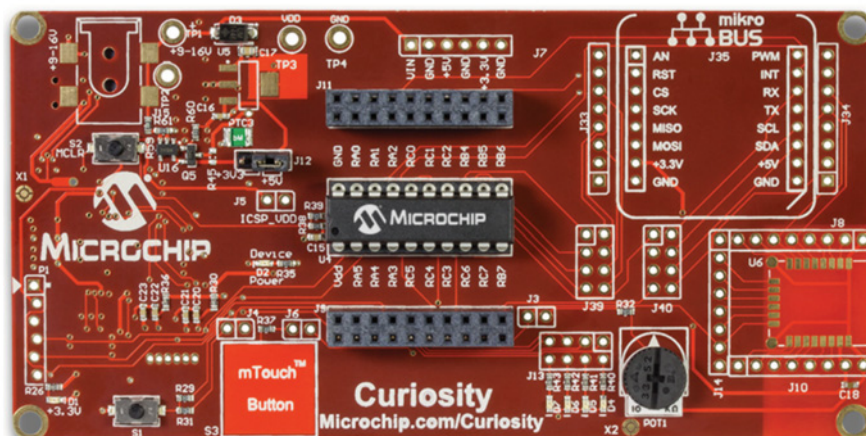Despite the complexity of the underlying mathematical theory,

> The top priority cases is identifying errors before corrupt data is used by the application, or incorrect commands are executed

Figure 1: MPLAB Xpress evaluation board

the practical implementation in digital logic is often quite trivial, at most involving a shift register of appropriate length and a (small) number of XOR operations.

CRC Peripheral

A CRC algorithm can be implemented in a few lines of C code, but this is actually one of those few areas where you will still find assembly code being used today. The cyclic nature of the algorithm imposes that the entire polynomial expression be evaluated for each bit of the data block, so hand-optimized assembly implementations can provide a significant boost by focusing on the most efficient coding possible of the innermost loop.

Whilst dedicated networking and communication devices tend to incorporate hardware implementations of the specific CRC algorithm required, and CRC peripherals are featured on high-end (16- and 32-bit) microcontrollers, the low-cost general-purpose microcontrollers users have so far been left on their own. Even a simple parity check (which is eventually nothing more than a 1-bit CRC) for the most common UART peripheral is usually left as an exercise for the 8-bit embedded developer.

But, following on the commitment to provide even the smallest 8-bit microcontroller with an efficient set of peripherals to relieve the core from menial, repetitive workloads, Microchip has recently began offering a new CRC peripheral, capable of polynomials up to 17-bit in size, in devices as small as 8-pin and with as little as 1.5kbytes of Flash memory.

One such device, part of the PIC16F161x family (8/14/20-pin), featured on the Curiosity demonstration board launched in spring 2015. More recently, the XPRESS evaluation board has featured a similarly equipped device part of the PIC16F188xx family (28/40-pin), soon to be joined by the recently-announced PIC18xxK40 family to complete the gamut of options up to 128kbytes of Flash and up to 64 pins.

Testing The CRC-16-CCITT Polynomial

Using the MPLAB Xpress cloud tool-chain and the Curiosity demonstration board (or the Xpress evaluation board) we can test the effectiveness of the CRC module in just a few minutes to get a feel for the ease of use and performance achievable.

● First, launch the MPLAB Xpress online IDE. After logging into your own myMicrochip account, create a new project for the PIC16F1619 (or PIC16F18855 if using the Xpress Evaluation board instead) and launch the MPLAB Code Configurator.
● Select the CRC module and proceed to select the following options in the 'Polynomial' panel (as in Figure 2):
● Check the 'Predefined Polynomial's checkbox.
● Select the CRC-16-CCITT option – this will pre-set the following three options including Seed, Seed Method and Shift direction with the correct values.
● Select the "data augmented with 0s" option.
● Set the shift direction to left as per above.
● Set the data word width to 8-bit.
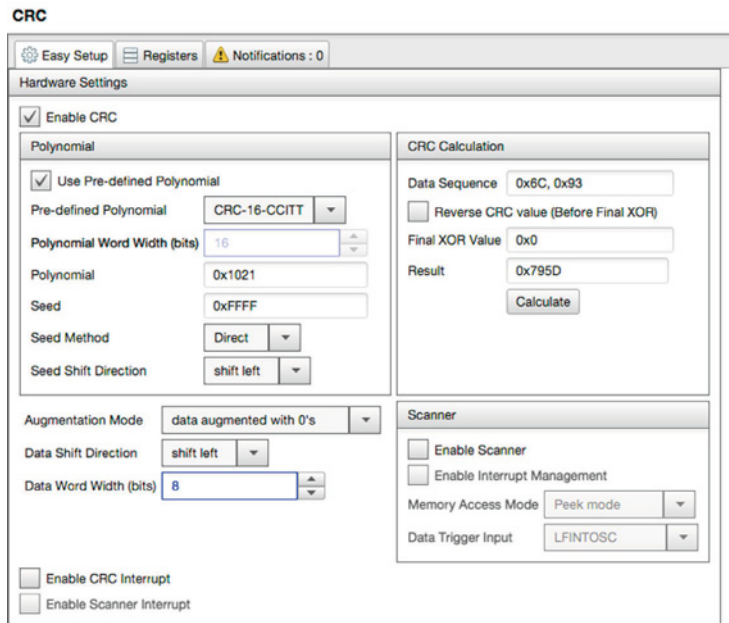For this test project we will also use the EUSART module to

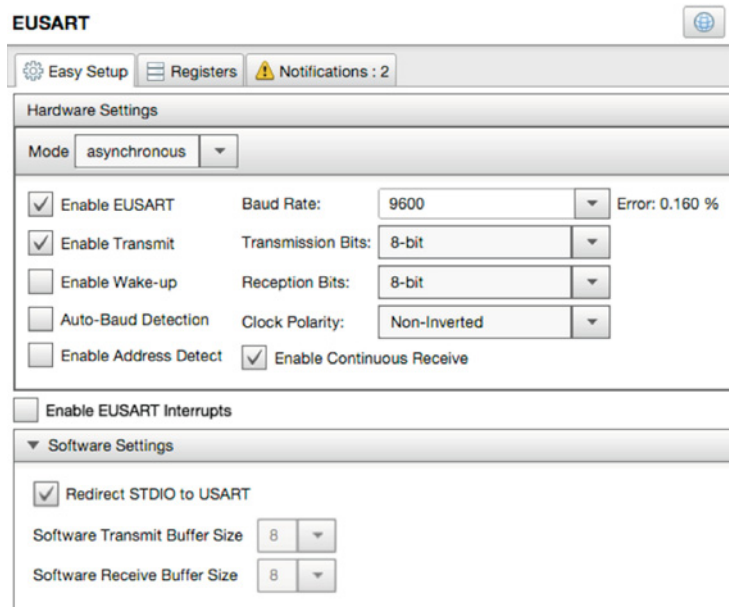
Figure 2: MPLAB Xpress ADCC configuration

Figure 3: USART configuration

connect to a USB Click board (if using the Curiosity board) or to communicate directly to the on-board USB bridge (if using the XPRESS evaluation board).

Proceed to add the EUSART module to the project and configure it for the desired baud rate; see Figure 3.

In 10 Lines Of Code

With a click of the 'Generate' button, the MPLAB Code Configurator will produce configuration files and place them in the project sources. We are now ready to start focusing on the core of the demo application.
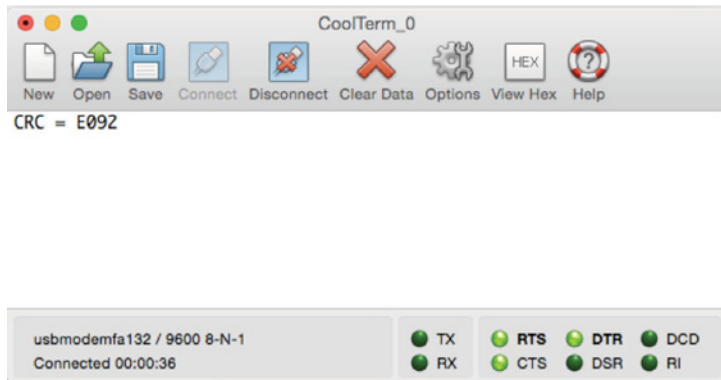
Figure 4: Terminal screen capture

```
#include "mcc_generated_files/mcc.h"

void main(void)
{
// initialize the device
SYSTEM_Initialize();

CRC_Start();
CRC_8BitDataWrite(0x6C);
while(CRC_IsBusy());
CRC_8BitDataWrite(0x93);
while(CRC_IsBusy());
printf ("CRC = %04X \n", CRC_
CalculatedResultGet(false, 0));

while (1)
{
}
}
```

Listing 1: Testing the CRC-CCITT polynomial

After the usual call to SYSTEM_Initialize(), where both the CRC module and UART are configured, we can make the CRC peripheral ready to serialize data with a call to CRC_Start() and begin immediately feeding it with input test data using the CRC_8BitDataWrite() function.

We can use the CRC_IsBusy() function to test for the completion of the CRC calculation and proceed to retrieve the results and print them out to the serial port. Note that the CRC_CalculatedResultGet() function is ready to reverse the bit order of the result or perform a XOR with an expected value (as necessary in some legacy applications), although this is not used here.

In our example using:
● the test data sequence: 0x6C, 0x93;
● for a (direct) Seed value of 0xFFFF;
● no reversing required (passing False as the first parameter);
● expecting a XOR value of 0 (passed as the second parameter); we will obtain a value of 0xE092 as seen in the Terminal screen capture of Figure 4.

Nowadays it is very easy to find online calculators that can provide reference values for the most popular polynomials. The Lammertbies website offers one of such free tool: http://www.lammertbies.nl/comm/info/crc-calculation.html.

By applying the same inputs you will soon be able to verify that the value we obtained is indeed the correct one.

Even More Core Independent CRC-SCAN

This simple demo application has barely scratched the surface of what's possible with the new CRC module. In fact, for those cases when the CRC module is used to test the integrity of a device Flash memory, an additional important piece of functionality has been added to the module to make its operation even more core-independent. Whilst the small PIC16 and PIC18 microcontrollers featured do not have a proper Direct Memory Access (DMA) mechanism, the CRC module has been given one ad hoc. To avoid any confusion, this has been named SCAN function since it is dedicated to the exclusive use of the CRC module and it can only provide a read-from-memory (Flash) functionality.

The SCAN function can be further configured to operate in one of four possible modes:
● Burst mode, where the SCAN function takes absolute control of the microcontroller's Flash memory (stalling the core execution pipeline) but performing the fastest possible computation of the chosen CRC algorithm over the contents of an assigned memory range.
● Concurrent mode, where the CRC function is allowed to fetch, alternating with the core.
● Triggered mode, where the CRC function is allowed to fetch from memory when specific events are triggered. Typically, a timer period match event is used to provide a desired rate of execution.
● Peek mode, where the core has the highest priority of access over the Flash memory and the CRC function is relegated to use only "free" bus cycles. Whilst providing a slower CRC computation, this mode effectively makes the CRC function completely transparent to the application (zero impact on the core performance).

Different application needs will dictate the mode of choice, balancing core performance vs CRC computation speed.

Applications that need to conform to the Class B (IEC60730) or UL98 specifications, for example, might choose to perform a Burst mode check upon power-up and, later, periodically repeat the same check in Peek mode or Triggered mode for continuous functional safety coverage.

In Closing

The MPLAB Code Configurator and the flexibility of the Core Independent Peripherals (CRC-SCAN) can make it really easy to automate the most core-intensive part of communication and application integrity checking. The flexibility of a programmable CRC polynomial is available now, even in very small and inexpensive microcontrollers, without the workload and complexity of traditional firmware implementations. ●

Using text-to-speech processors in intelligent embedded designs

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

A speech synthesizer is a computer system that artificially produces human speech. These are complex systems requiring fast digital signal processors (DSPs), and are normally implemented in both hardware and software.

The basic idea for speech synthesis started in the 18th century, when Russian professor Christian Kratzenstein created an apparatus based on the human vocal tract to demonstrate the physiological differences in producing five long vowel sounds. Today the speech synthesis is an advanced mature field of DSP.

A text-to-speech (TTS) processor (or text-to-speech converter) receives language in text form and converts it into speech that can be heard on suitable audio output devices, such as speakers or headphones. TTS systems are used in many embedded intelligent applications to convert text into speech.

PC-Type TTS Software

There are many versions of TTS software available for personal computers (PCs), including:

● **Balabolka:** freeware TTS software based on the Microsoft Speech API (SAPI), allowing voice parameters such as rate and pitch to be configured. Balabolka offers 25 languages, including Arabic, Japanese, Russian, German and Turkish.
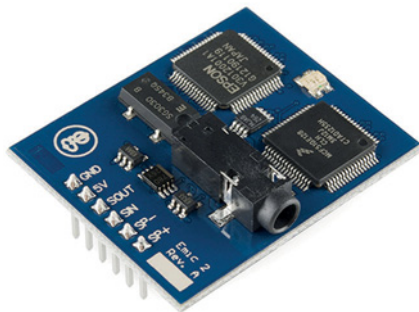

Figure 1: Emic 2 TTS module

Figure 2: Speech synthesis shield for Arduino

Figure 3: V8600A TTS module
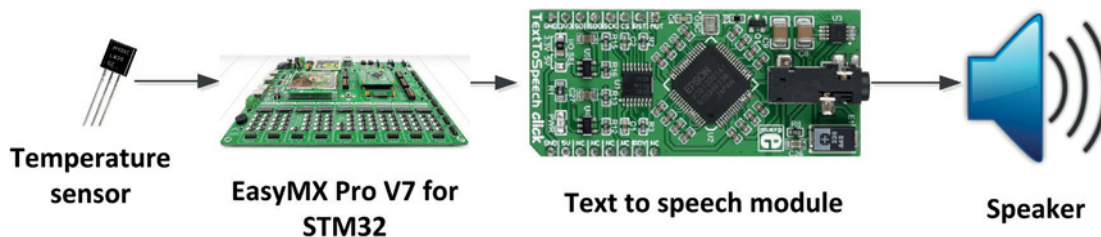

Figure 4: V-Stamp TTS module

Figure 5: The designed system

- **NaturalReader:** powerful TTS software that can listen to various files including PDF, web pages, e-books and even printed books. This software is also widely used to learn languages. NaturalReader includes many features that help people with disabilities, including large fonts, text highlighted during reading, spellcheck, colour interface and word prediction.
- **WordTalk:** free TTS plug-in for the Microsoft word processor, available only for Windows-based PCs. The software speaks the word document, highlights the words during speech, has a talking dictionary and with variable speed of reading.
- **PowerTalk:** free software used with Microsoft PowerPoint presentations; the software speaks even the text embedded in images. The program waits for the text to be displayed and any animations to play before the words are spoken.
- **ClaroRead:** there are several versions of this professional software that reads text files in many different formats. The program is available in 80 different languages. Text written by the user can be read back to improve writing, reading and listening skills. Thesaurus is also included.

TTS In Embedded Applications

TTS software is used on PCs, tablets and mobile phones without the need of additional hardware. There are also many microcontroller-based embedded applications where TTS may be required and, in such applications, a TTS processor hardware module is normally used.

The features of some of the TTS modules which can be used in embedded designs are described here briefly. Emic 2, available at **www.parallax.com** (Figure 1), is an easy to use TTS module, operating with serial text data at 9600 baud and requiring an external speaker with an on-board audio amplifier. The module operates at +5V (30mA idle, 46-220mA active) and is connected to a UART output of the host processor.

Speech synthesis shield for Arduino module (Figure 2) has been specifically developed for Arduino and compatible microcontroller development boards, but it can be used with other microcontrollers too. The module can speak
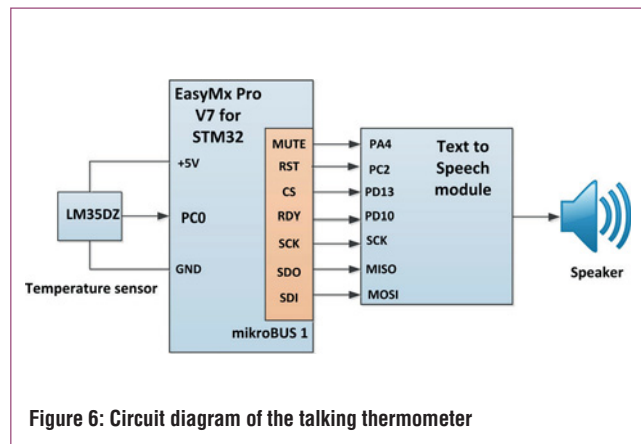

Figure 6: Circuit diagram of the talking thermometer

both English and Chinese, and communicates with the host processor through the UART. The module offers baud rates in the 4800-115200 range, can operate with 11 different speech speeds and supports male, female and child voices. Its operating voltage is +5V.

V8600A (Figure 3) is based on the RC8650 chipset and it converts plain-text English into male voice. The module requires +5V power supply and an external speaker for its operation. The host interface is through parallel I/O pins, although an optional RS-232 interface is also available for interface to a host UART.

V-Stamp (Figure 4) is a sound synthesizer and recorder. It includes several features such as text-to-speech converter, audio recording and playback, musical tone generation, telephone dialler and 4-channel, general-purpose, ADC converter. The module operates from +3.3V or +5V and includes a power amplifier that can generate sound at 1W. Interface to the host is through standard serial logic levels.

Example TTS System – Talking Thermometer

Our example system is a talking thermometer where ambient temperature is sensed and sent to a speaker as voice. The system diagram is shown in Figure 5; it is based on the mikroElektronika text-to-speech click board, a small mikroBUS-compatible board

with the following features:

- Epson S1V30120 speech synthesis IC;
- Fonix DECtalk speech synthesis engine;
- US English, Castilian and Latin-America Spanish speech;
- Control of quality, pitch and intonation of synthesized speech;
- 11.025kHz audio sampling rate;
- Communication with the target processor via SPI (MISO, MOSI, SCK, CS) interface;
- +3.3V or +5V power supply.

The S1V30120 speech synthesizer IC contains all the required analogue codecs, memory and EPSON-supplied embedded algorithms, and is controlled over a single SPI, allowing control from a wide range of hosts.

DECtalk is the world's most intelligible TTS synthesizer with the most natural sounding voice. It also has the smallest memory footprint in the industry for a full featured, multi-language voice synthesizer, thus being an excellent embedded solution.

An EasyMX Pro V7 for STM32 ARM Cortex-M3 microcontroller development board is used in this design for simplicity. This development board has the following basic features:

- STM32F107VGT6 Cortex-M3 72MHz microcontroller;
- 256kbytes flash memory;
- 64kbytes RAM;
- 80 I/O ports;
- 2 x 16 channel 12-bit ADCs;
- 2 x 12-bit DACs;
- 2 x mikroBUS sockets;
- 67 LEDs and push-button switches;
- USB and CAN bus support;
- TFT display.

Figure 6 shows the circuit diagram of the designed TTS system. The temperature is sensed using an LM35DZ type analogue temperature sensor chip, connected to the analogue input PC0 (AN10) of the microcontroller. The ADC is 12-bits wide, with 4096 quantization levels and a reference voltage of 1.8V. The output voltage of the sensor chip is directly proportional to the measured temperature and is given by $V_0 = 10mV/^\circ C$. Thus, for example at 30°C, the output voltage is 300mV, and so on.

The text-to-speech module is controlled using the microcontroller's SPI interface. In addition, the RST, CS, MUTE and RDY pins of the module are connected to the I/O pins of the microcontroller. In this design, the text-to-speech module is connected to mikroBUS socket 1 of the development board, powered by the on-board +3.3V supply.

The interface between the microcontroller and text-to-speech module are as follows: (notice that the SCK, MISO and MOSI are the SPI bus signals). In this design SPI3 module of the development board is used.

Text-to-speech pin	Microcontroller pin
MUTE	PA4
RST	PC2
CS	PD13
SCK	SCK of SPI
SDO	MISO of SPI
SDI	MOSI of SPI
RDY	PD10

The output of the text-to-speech module is connected to a speaker through the 3.5mm on-board audio jack connector. It has two working modes: boot and run. The device boot mode is entered on hardware reset and the initialization data is downloaded whilst in this mode. After this, the loaded image must be executed and the TTS interface must be tested before the module enters run mode, where it is configured for the required operational parameters.

The Software

The software of this design is developed using the mikroC Pro for ARM language and IDE. Figure 7 shows the complete software listing.

The mikroElektronika text-to-speech library is used in the software for simplicity. The library includes module-configuration functions by selecting output types, speed and sampling frequency to set the volume, mute and unmute, as well as other functions.

At the beginning of the program, the text-to-speech module library is included and the interface between the microcontroller and text-to-speech module defined. Inside the main program, function system_init is called to configure the I/O port directions and to initialize the SPI bus. Notice that by default, the SPI3 pins are at port pins PC10, PC11 and PC12. Function tts_setup initializes and configures the TTS module; the ADC channel 10 is then initialized. The remainder of the program is executed in an endless loop, where temperature is read at analogue channel 10 and converted into a string in variable Txt. Finally, function tts_speak is called to output the temperature on the speaker as voice in the form *'The temperature is nn degrees Centigrade'*. This process is repeated endlessly after a 10-second delay. ●

```
#include "text_to_speech.h"
#include "text_to_speech_img.h"
sbit TTS_RST at GPIOC_ODR.B2;
sbit TTS_CS at GPIOD_ODR.B13;
sbit TTS_MUTE at GPIOA_ODR.B4;
sbit TTS_RDY at GPIOD_IDR.B10;

void system_init()
{
 GPIO_Digital_Output(&GPIOC_ODR, _GPIO_
PINMASK_2 );
```

```
                                    >
 GPIO_Digital_Output(&GPIOD_ODR, _GPIO_
PINMASK_13 );
 GPIO_Digital_Output(&GPIOA_ODR, _GPIO_
PINMASK_4 );
 GPIO_Digital_Input( GPIOD_IDR, _GPIO_
PINMASK_10 );

 SPI3_Init_Advanced(_SPI_FPCLK_DIV128, _SPI_
MASTER | _SPI_8_BIT |
 _SPI_CLK_IDLE_HIGH | _SPI_SECOND_CLK_
EDGE_TRANSITION |
 _SPI_MSB_FIRST | _SPI_SS_DISABLE | _SPI_SSM_
ENABLE |
 _SPI_SSI_1, &_GPIO_MODULE_SPI3_PC10_11_12 );
}

void tts_setup()
{
 tts_image_load((uint8_t* )TTS_INIT_DATA,
sizeof(TTS_INIT_DATA));
 tts_image_exec();
 tts_interface_test();
 tts_audio_default_config();
 tts_default_config();
}
```

```
void main()
{
 float mV;
 unsigned int voltage;
 unsigned char Temperature,Txt[50]="The
temperature is ";
 system_init();
 tts_init();
 tts_setup();
 ADC1_Init();
 ADC_Set_Input_Channel(_ADC_CHANNEL_10);

 while(1)
 {
 voltage = ADC1_Get_Sample(10);
 mV = voltage*1800.0/4096.0;
 Temperature = mV / 10;
 ByteToStr(Temperature, Txt+19);
 strcat(Txt,"Degrees Centigrade");
 tts_speak(Txt);
 delay_ms(10000);
 }
}
```

Figure 7: Software listing

DESIGN OF A PRINTED MONOPOLE ANTENNA FOR UWB COMMUNICATIONS

BY **MOHAMMAD JAKIR HOSSAIN** AND **MOHAMMAD RASHED IQBAL FARUQUE** FROM THE MALAYSIAN SPACE SCIENCE CENTER (ANGKASA) AND **MOHAMMAD TARIQUL ISLAM** FROM UNIVERSITI KEBANGSAN, MALAYSIA

Industry is always on the lookout for best performance technologies, and this is also the case with ultra-wideband (UWB) communications – especially after the US Federal Communication Commission (FCC) allocated the unlicensed frequency band 3.1-10.6GHz to its use.

Due to its high data rates and better spectral power density it offers, the UWB system is one of the most favoured in the industry at the moment. However, designing a suitable small yet super-efficient antenna is still a challenge.

The planar microstrip patch antenna is commonly used in wireless communication systems because of its simple structure, compact size, low profile, low weight, constant gain, stable radiation patterns and ease of manufacture.

In this article we review a new version – a compact, planar, monopole, printed antenna of high performance, sufficient impedance bandwidth and stable radiation pattern.
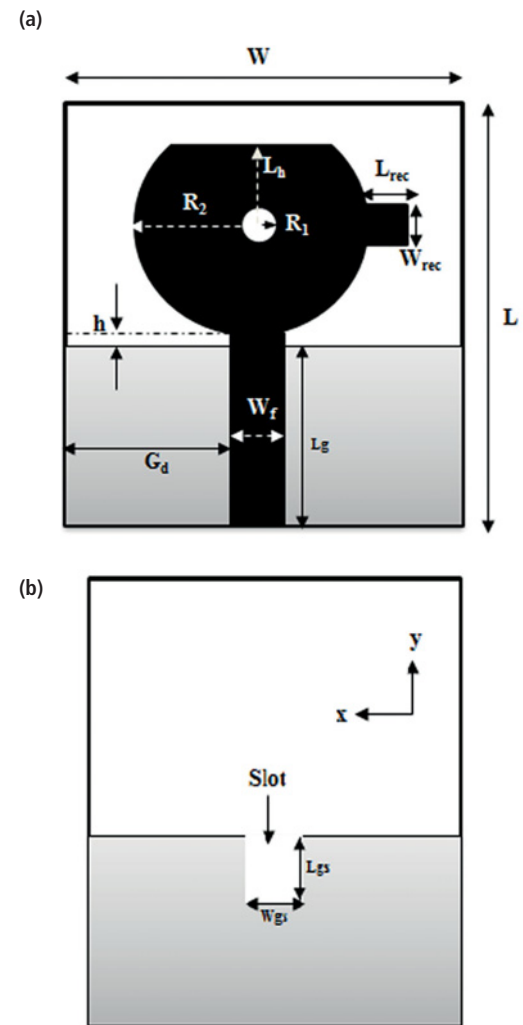

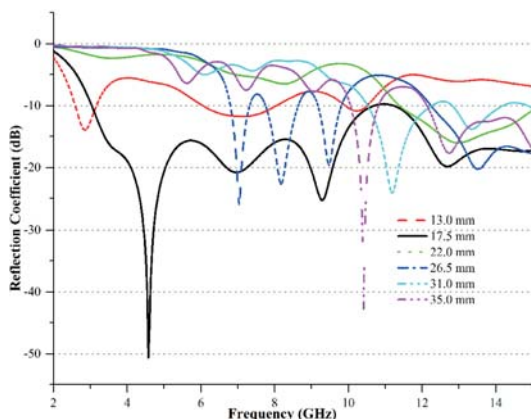Figure 1 (a, b): Top and bottom of the proposed monopole antenna

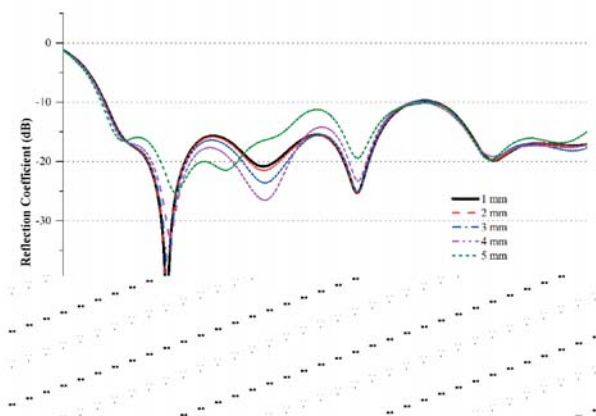Figure 2 (a): Simulated reflection coefficient for various L_g values

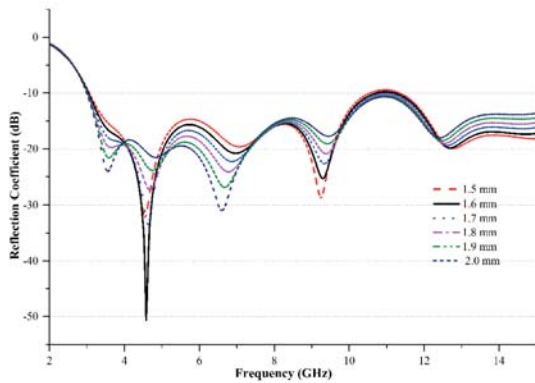Figure 2 (b): Simulated reflection coefficient for various R1 values

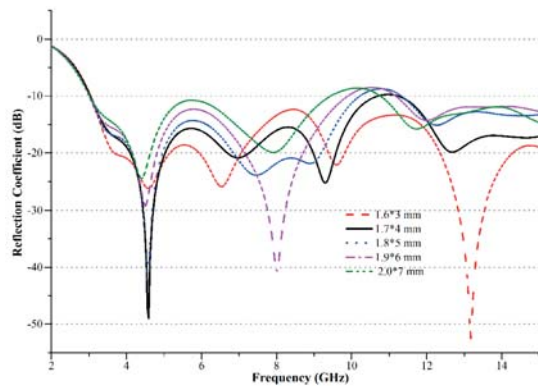**Figure 2 (c): Simulated reflection coefficient for various W$_f$ values**

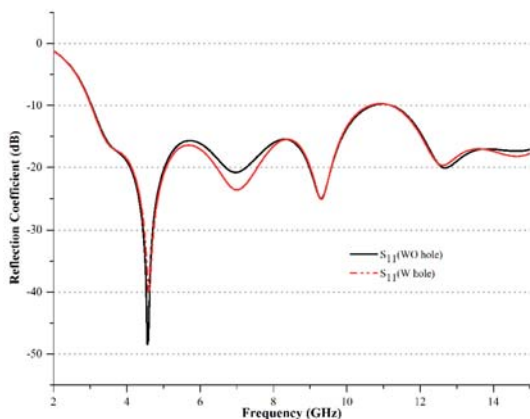**Figure 2 (d): Simulated reflection coefficient for various slot values**

Figure 2 (e): Simulated reflection coefficient with and without a hole in the radiating patch
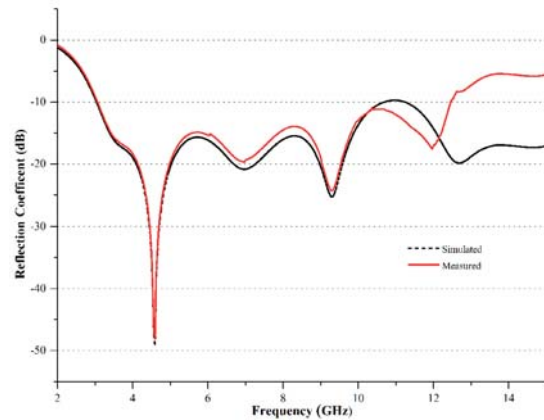

Figure 2 (f): Measured and simulated reflection coefficient for the proposed planar antenna
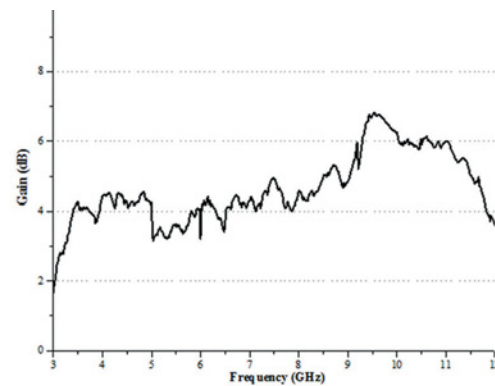
Figure 2 (g): Measured peak gain of the proposed antenna

The configuration of the proposed patch antenna is shown in Figure 1. The antenna is ring-shaped with a 3mm × 2.5mm rectangular slot on top and a 17.5mm-long ground plane with a 4mm × 3.4mm slot. Because of the antenna's shape, it easily achieves impedance bandwidth of 3.088-12.497GHz for UWB applications.

The antenna's overall size is compact (35mm × 24mm) and it's printed on the surface of a 1.6mm-thick FR4 substrate with relative permittivity of 4.4 and loss tangent of 0.02. The radiator is a microstrip feed line, with a subminiature version A (SMA) connector attached.

A study was performed to observe the effects of varied antenna parameters for best matched impedance and bandwidth. These included the inner radius of the radiating patch (R$_i$), ground plane length (L$_g$) and feed line width (W$_f$).

Impedance Bandwidth
The ground plane's dimensions play an important role in the design of a UWB antenna, affecting its impedance bandwidth. We verified through simulation that an increase or decrease in

the ground plane size takes its coverage outside UWB: for a 2mm decrease the antenna's frequency range is 2.80GHz-7.4GHz with one stop band; with a 2mm increase the impedance bandwidth shifts to 12.51GHz.

The simulated reflection coefficients for various ground-plane widths are shown in Figure 2a, whereas Figure 2b shows the simulated reflection coefficient for different radius values for the inner gap of the radiating patch (R_1 = 1, 2, 3, 4 and 5mm). It has been shown that a 17.5mm-long ground plane maintains a good impedance bandwidth for the lowest reflection coefficient values. It can be noted that small changes in the gap size have little effect on impedance bandwidth; however, bigger changes have a greater impact. Our study concluded that the antenna's radius should be 1mm.

The simulated reflection coefficients for different feed line values (W_f = 1.5, 1.6, 1.7, 1.8, 1.9 and 2.0mm) are shown in Figure 2c; all other parameters remain the same. It can be seen that shrinking or widening the feed line changes the reflection coefficient and helps tune the antenna's input impedance, which in turn affects operating bandwidth.

Figure 2d shows the simulated reflection coefficient for varied ground-plane slot area which influences impedance matching. Figure 2e shows the effects on impedance matching if a hole is added in the middle of the radiating patch, where a small hole has little effect on operating bandwidth.

New Antenna Capabilities

The capability of the proposed printed antenna was verified and optimized with a CST & HFSS simulator. Then a SATIMO Starlab anechoic chamber of 0.6-18GHz was used in this experiment, conducted at the microwave laboratory of the Space Science Centre (ANGKASA) institute in Malaysia. The setup was used to measure the antenna's peak gain, radiation pattern and efficiency. We used an Agilent E8362C vector analyzer to measure the input impedance characteristics of the antenna.

We applied near-field measurement techniques in the test, which helped determine the antenna's electromagnetic fields. Using its far-field radiation pattern, antenna efficiency and gain were easily measured.

Figure 2f shows the curve of the reflection coefficient for the proposed patch antenna, which shows that for the 3.088-12.497GHz range, the measured impedance bandwidth is below or equal to -10dB. The measured results are similar to the simulation results; any discrepancy may be due to fabrication errors.

We thus showed that despite the antenna's small size, it can be adjusted over a wide bandwidth (3.1-10.6GHz), suitable for UWB applications.

Figure 2g shows the measured peak gain of the printed patch antenna for 3-12GHz. It can be seen that 4.2dB is achieved at the first resonance of 4.5GHz, 4.22dB at the second resonance of 7.0GHz and 6.8dB at the third resonance of 9.5GHz. Moreover, the gain for frequencies below the tested band is lower than that for above-band.

Antenna gain and efficiency can be further enhanced by using better microwave substrates, instead of the lower-quality FR4.
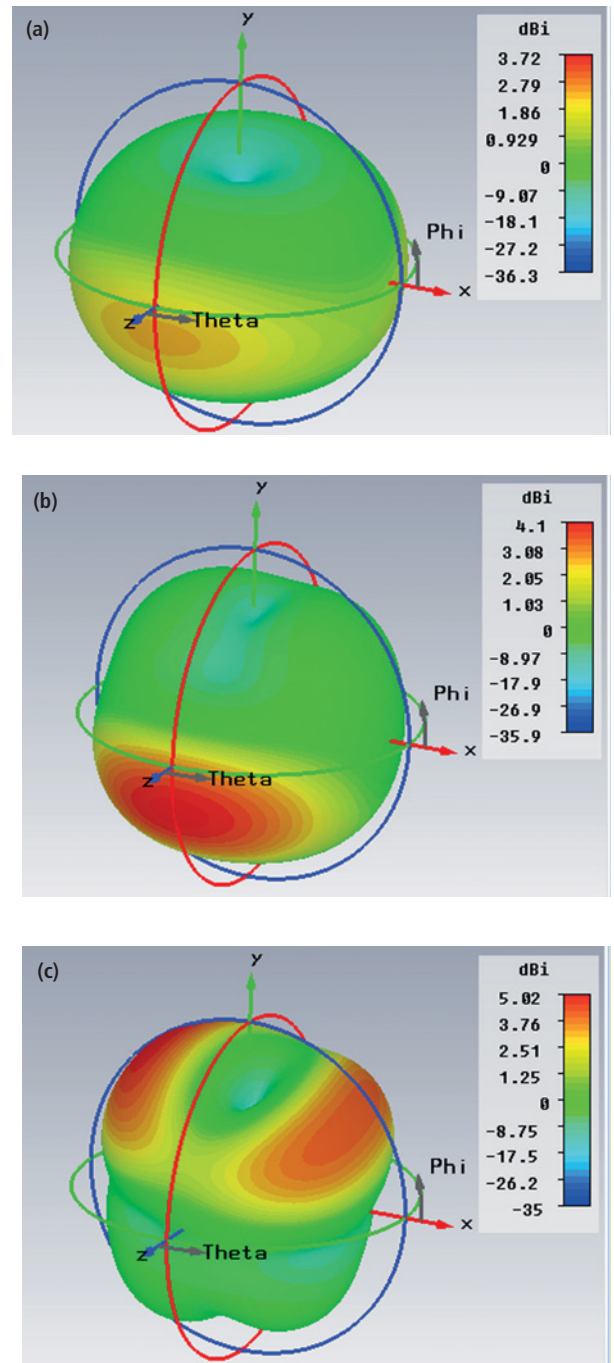
Figure 3 (a, b, c): Simulated 3D radiation patterns for 4.5GHz, 7.0GHz and 9.5GHz

Figure 3 shows the 3D plot for the radiation of the proposed monopole printed antenna, where the E and H plane fields exhibit near omnidirectional patterns. On the other hand, these radiation patterns degrade severely at higher frequencies.

To receive signals from all directions, the proposed patch antenna has a perfect omnidirectional pattern. In addition, symmetrical and stable omnidirectional radiation patterns have been achieved along both H and E planes. ●

COST MINIMIZATION OF PASSIVE OPTICAL NETWORKS USING EVOLUTIONARY ALGORITHMS

BY **JOYCE JACOB** FROM ANNA UNIVERSITY AND **SWARNALATHA ALAGALA**, ASSOCIATE PROFESSOR AT THE ST. JOSEPH'S COLLEGE OF ENGINEERING, BOTH IN CHENNAI, INDIA

Existing broadband communication networks are expected to be replaced in the near future with Passive Optical Networks (PON). Therefore, it is essential that PON deployment is planned properly to reduce the overall cost of the network.

A PON is a single point to multipoint telecommunications network, a fusion of larger systems, say a neighbourhood, building, or home Ethernet network on coaxial cable. PONs are becoming popular because of their higher bandwidth, smaller size and low power consumption.

In a PON, optical fibre cabling carries data and signals. The network is terminated either at the curb or in the building and, based on this, the system is fibre-to-the-curb (FTTC), fibre-to-the-building (FTTB) or fibre-to-the-home (FTTH).

A PON uses wavelength division multiplexing (WDM), where one wavelength is used for downstream traffic and another for upstream in a single-mode fibre.

There are two important types of PONs: Ethernet-based (EPONs) and gigabit-speed passive optical networks (GPONs). EPON offers a bandwidth capacity of 1Gb/s both upstream and downstream, at distances up to 20km. GPON is based on the traditional Asynchronous Transfer Mode (ATM) technique, supporting higher bandwidth (up to 2.5Gb/s) in both directions. GPON also works at longer distances, up to 60km. Portions of this bandwidth can be allocated to multiple users.

Bandwidth Allocation

There are many studies focusing on PON bandwidth allocation and quality-of-service (QoS), but not many covering network planning and cost minimization. PON planning involves determining the number of splitters, their locations and the assignment of optical network units (ONUs) to each. Subtractive clustering algorithms help determine the number of splitters and their locations, whereas evolutionary optimization

Figure 1: Double star architecture
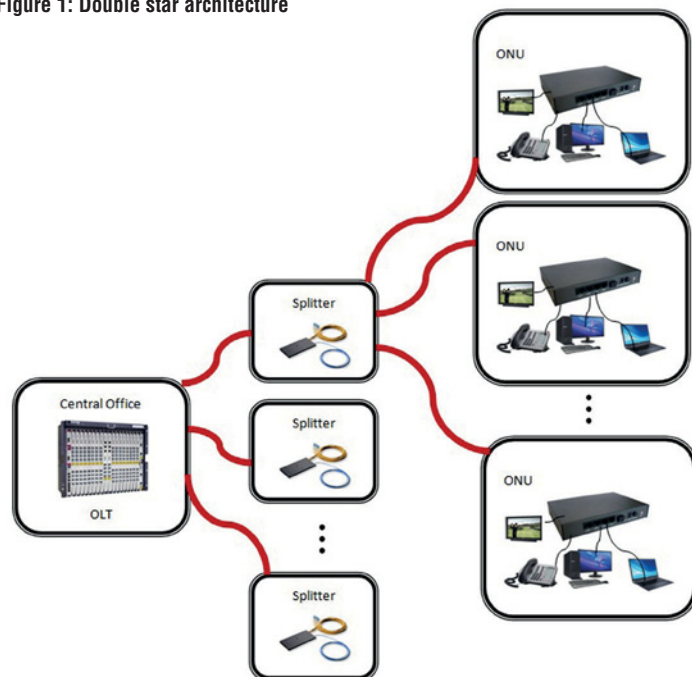
Figure 2: Evolutionary optimization flow chart
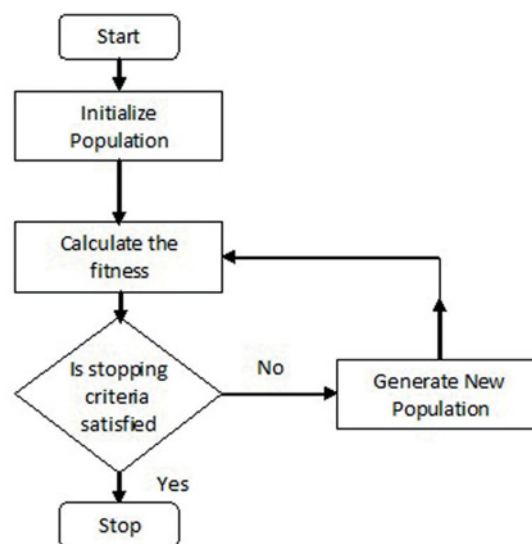
Figure 3: Gravitational search algorithm flow chart

Figure 4: Gravitational search algorithm flow chart
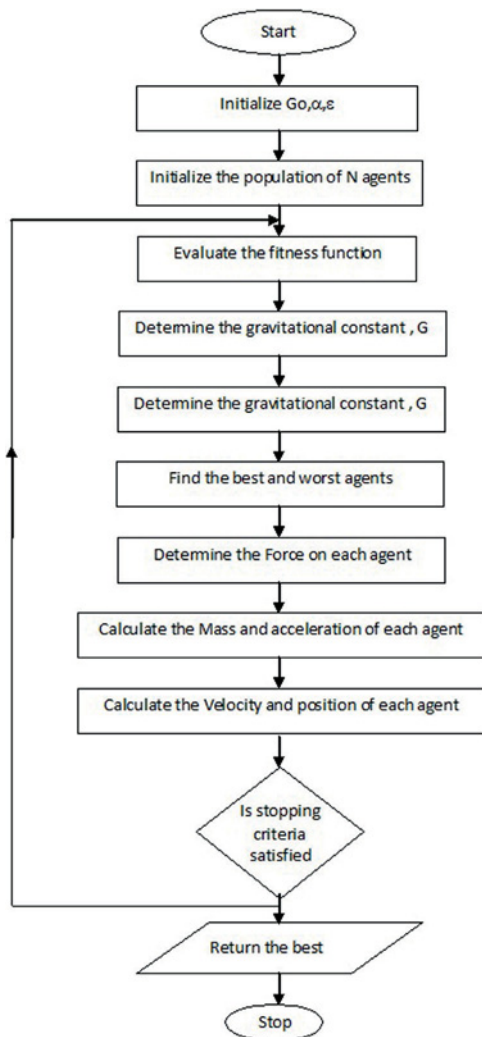
algorithms are used to assign ONUs to splitters.

A PON consists of an Optical Line Termination (OLT) at the communication central office and a number of ONUs or Optical Network Terminals (ONTs) near the end users. In the PON, the optical transmission path requires no power or active electronic parts to pass signal through the network.

A double star architecture, shown in Figure 1, is considered for cost minimization planning of the passive network. In this architecture, the signal from an OLT at the central office is sent to optical splitters, with many ONUs connected to each splitter.

> The number of ONUs connected to a splitter depends on the split ratio – another important factor in minmizing costs

The distances between optical splitters and ONUs, as well as between OLTs and optical splitters, determine the cost of the fibre and its installation. So, if these distances are minimized then the cost will be lower, too. The location of the splitter is also important, because if closer to many ONUs then distances are reduced.

The number of ONUs connected to a splitter depends on the split ratio – another important factor in minmizing costs. For example, if 1:8 is the split ratio, no more than eight ONUs can be connected to one splitter.

The objective function for cost minimization is:

$$(1)$$

$$f(x) = \sum_{i=1}^{nt} \sum_{j=1}^{sp} C_{ts}(i,j)\, x(i,j) + \sum_{j=1}^{sp} C_{sl}(j) y(j)$$

where n is the number of ONUs, sp the number of splitters, $C_{ts}(i,j)$ the cost of laying fibre between the ith ONU and the jth splitter, $C_{sl}(j)$ is the cost of laying fibre between the jth splitter and OLT, X is the connection matrix between ONUs and splitters,

---

Figure 5: Deployment of 100 nodes, 8 splitters and OLT
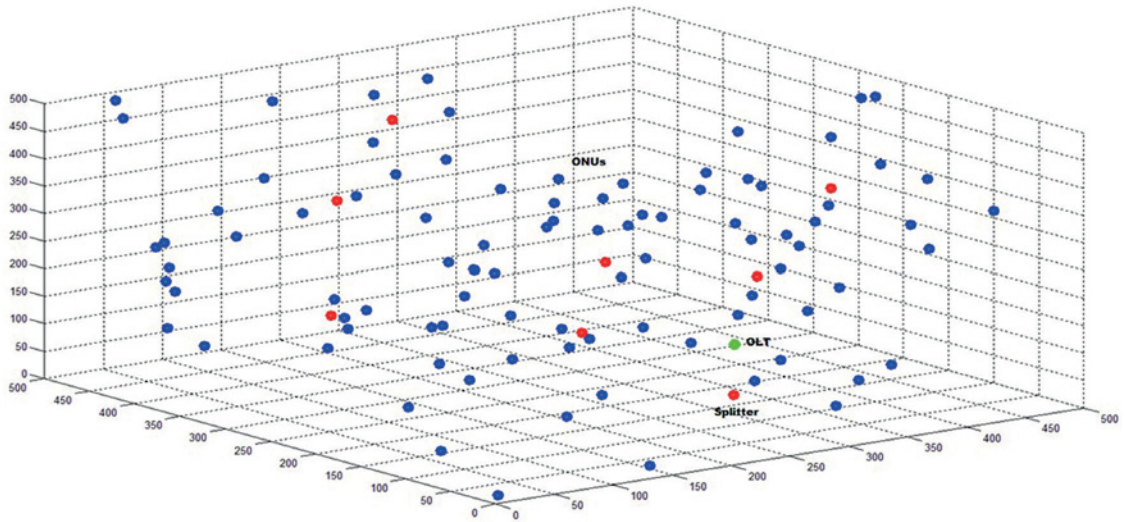
Figure 6: Deployment of 20 nodes, 4 splitters and OLT
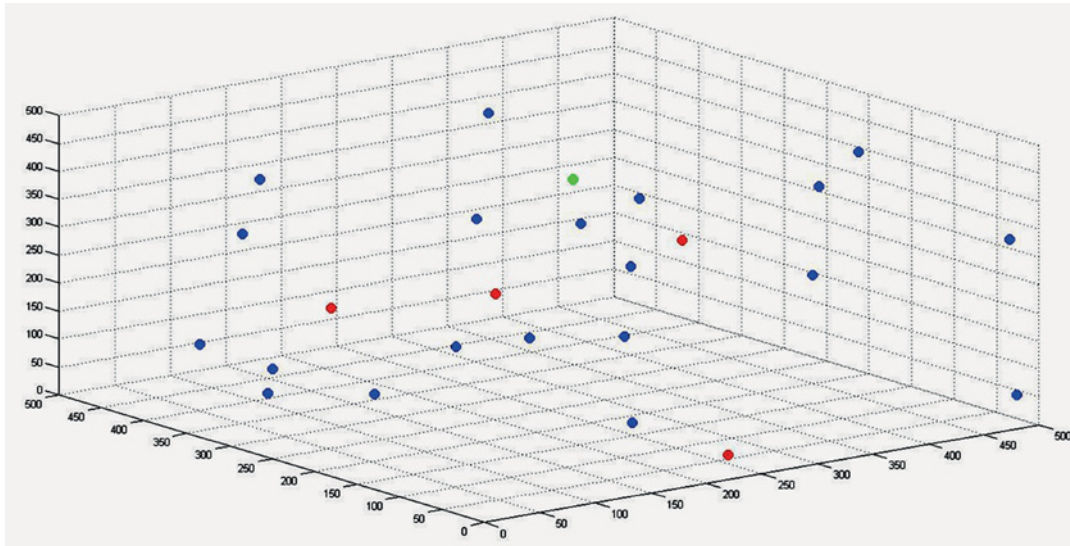
Y is the connection vector between splitters and OLT, and x(i,j) determines the connection between the ith ONU and the jth splitter. This last parameter is normally 1 if there is a connection between the ith ONU and the jth splitter, otherwise it is zero.

It is assumed that there is always a connection between every splitter and the OLT, i.e. Y is assumed to be a unit vector. C_{ts} matrix values depend on the distance between ONUs and splitters, whereas C_{sl} matrix values depend on the distance between splitters and the OLT.

When planning a passive optical network, we assume that OLT and ONU locations are known. Planning is then realized as follows:

● Initialize the number of ONUs, their locations and that of the OLT.
● Determine the number of splitters and their locations using the subtractive clustering algorithm.
● Determine the cost matrices C_{ts} and C_{sl} according to distances.
● Randomly initialize the connection matrix.
● Optimize the objective function using evolutionary optimization techniques.
● Assign the ONUs to respective splitters according to the optimized connection matrix X.
● Determine the cost.

Figure 7: Communication between ONUs and splitters by GSA
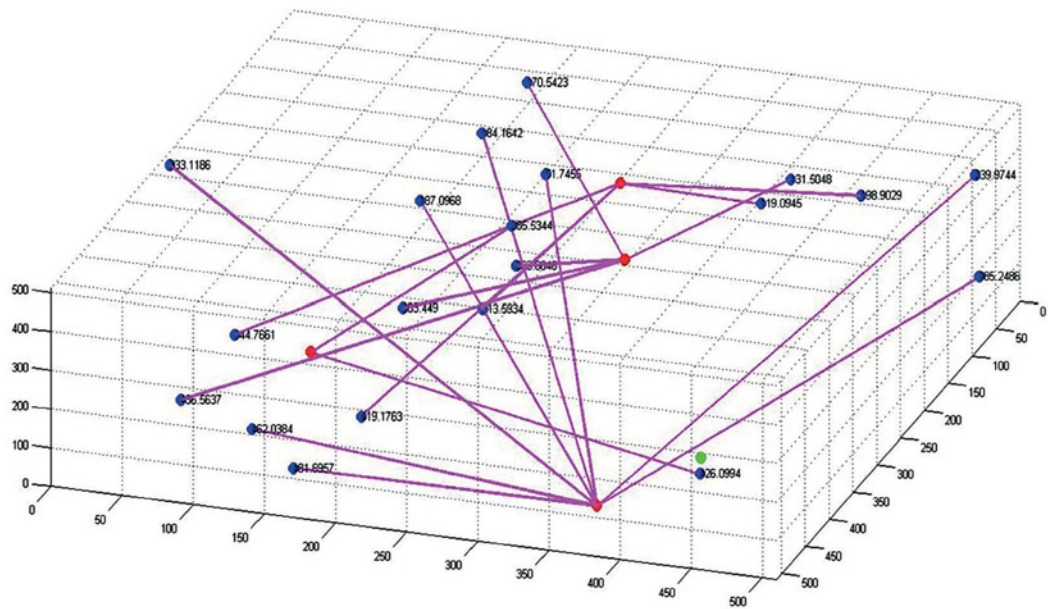
Performance Measures

The OLT and ONU locations are plotted in 3D space. Figure 5 shows 100 ONUs with eight splitters, where ONUs are shown as blue dots, splitters are red and the OLT green.

Figure 6 shows the locations of 20 ONUs and four splitters. The communication between ONUs and the splitter they are assigned to by the Gravitational Search Algorithm (GSA) is shown in Figure 7 and communication between splitters and OLT in Figure 8. The communication between ONUs and the splitter they are assigned to by the Cuckoo Search Algorithm (CSA) is shown in Figure 9, whereas the communication

Number of Nodes	Number of Splitters	Cost		% Occupancy Ratio		Convergence Time	
		GSA	CSA	GSA	CSA	GSA	CSA
20	4	80190.16	67292.64	66.6667	66.6667	4.305699	0.558279
40	3	164195.2	143035.5	41.6667	45.4545	4.11837	0.774385
40	6	128190.1	126681.6	76.9231	41.6667	5.14762	1.495392
60	4	267824.8	258366.8	37.5000	40.5405	4.614752	1.590409
60	8	206074.9	156665.4	83.3333	50.0000	6.107117	3.560550
80	4	294460.1	253515.4	38.4615	57.1429	4.763835	2.283722
80	8	282507.1	265077.8	76.9231	58.8235	15.16558	5.675149
80	12	288785.1	274258.4	80.0000	41.2371	8.205845	10.21604
100	4	344879.7	308713.5	39.0625	67.5676	18.55819	3.342195
100	8	358155.8	331221.3	46.2963	50.0000	19.76811	8.204022
100	14	367076.5	355866.2	73.5294	50.5051	9.729635	19.18824
200	4	914431.7	868002.5	78.1250	62.5000	5.60984	9.79058
200	8	699396.0	604015.2	39.0625	67.5676	10.0999	26.81052
200	14	540443.2	457920.9	48.0769	66.6667	22.49658	68.43026
200	26	860370.6	820700.5	74.6270	54.9450	25.1153	204.4300
400	4	1842667	1611515	78.1250	78.1250	12.63073	34.40538
400	8	1429820	1177189	78.1250	84.0336	10.94371	102.0944
400	14	1545258	1517491	44.6429	50.0000	24.01324	268.5810
400	26	1840707	1631113	45.045	61.9195	33.75229	847.8329

Table 1: Performance analysis of optimization algorithms

Figure 8: Communication between splitters and OLT by GSA
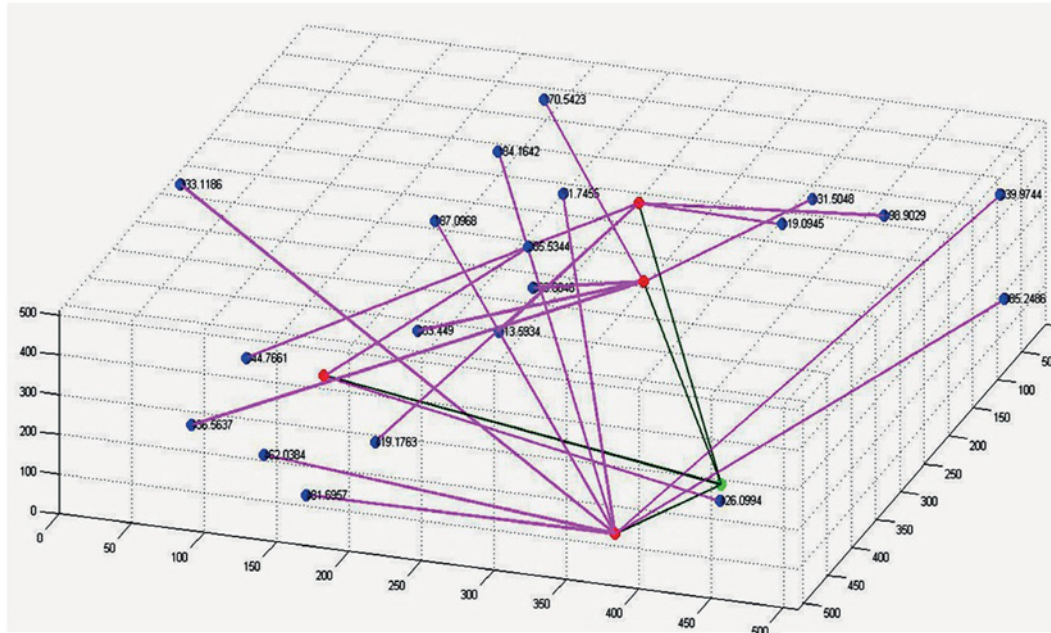
Figure 9: Communication between ONUs and splitters by CSA
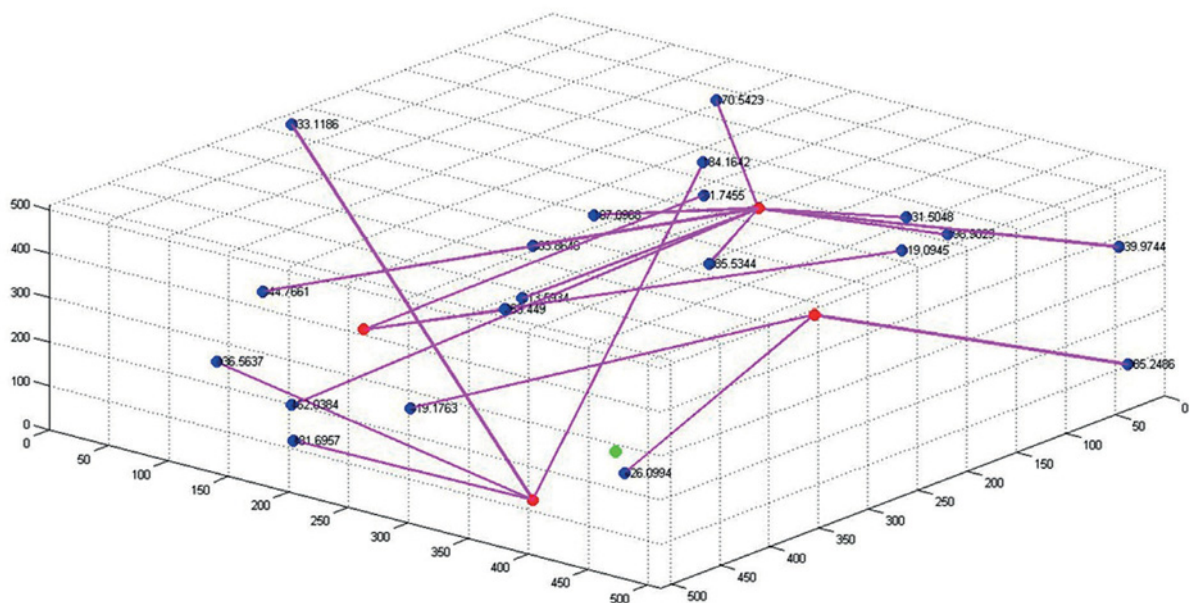
between splitters and OLT by CSA is shown in Figure 10.

Three performance metrics are chosen for comparing the evolutionary optimization algorithms: cost estimation of PON planning, occupancy ratio and convergence time.

The subtractive clustering algorithm determines the number of splitters and their locations. The evolutionary optimization algorithms allocate the ONUs to their respective splitters, and the cost of the PON planning is determined by Equation 2.

In optical splitters the ratio of number of output ports to input ports is known as the split ratio, which is usually in the order of $1:2^k$, where k is an integer. Optical splitters are available with split ratios of 1:2, 1:4, 1:8, 1:32, 1:64 and so on.

The split ratio of the splitters is determined by the number of ONUs allocated to them by the algorithm. Occupancy ratio is the measure of occupation of the optical splitter, defined as:

$$Occupancy\ Ratio = \frac{\sum_{j=1}^{sp} al(j)}{\sum_{j=1}^{sp} ca(j)} \qquad (2)$$

where sp is the total number of splitters, al(j) the number of ONUs allotted to jth splitter by the algorithm, and ca(j) is the capacity of the jth splitter.

The percentage occupation ratio is given by:

$$\% Occupancy\ Ratio = $$
$$Occupation\ ratio \times 100 = \frac{\sum_{j=1}^{sp} al(j)}{\sum_{j=1}^{sp} ca(j)} \times 100 \quad (3)$$

The optimum value of percentage occupation ratio is 100.

Convergence time is a measure of how fast evolutionary optimization algorithms can reach the state of convergence.

PON network planning is performed using two of the latest evolutionary optimization algorithms, i.e. the GSA and CSA. Table 1 shows the results of PON cost minimization, the number of ONUs and their locations, as well as the number of splitters for the two evolutionary algorithms. For both algorithms, the convergence time keeps increasing with the number of splitters and the node products (nd×sp); for example, if the product increases, then the convergence time also increases for the evolutionary optimization algorithms.

When (nd×sp) is low, the convergence time of the CSA is slower than GSA; and if (nd×sp) is higher, then the convergence of GSA is faster than CSA.

From Table 1 it can easily be seen that irrespective of the (nd×sp) value, the cost of PON planning is lower for CSA than GSA and the occupancy ratio of CSA is greater than GSA. As the number of splitters increases, for the same number of ONUs the occupation ratio of both algorithms increases too. The rate of increase in case of CSA is also greater than that of GSA.

It can be concluded that for cost minimization and occupancy ratio, CSA results in the optimal solution. These results are found to be consistent for almost all combinations, making CSA best suited to cost minimization in PON planning. ●

Figure 10: Communication between splitters and OLT by GSA
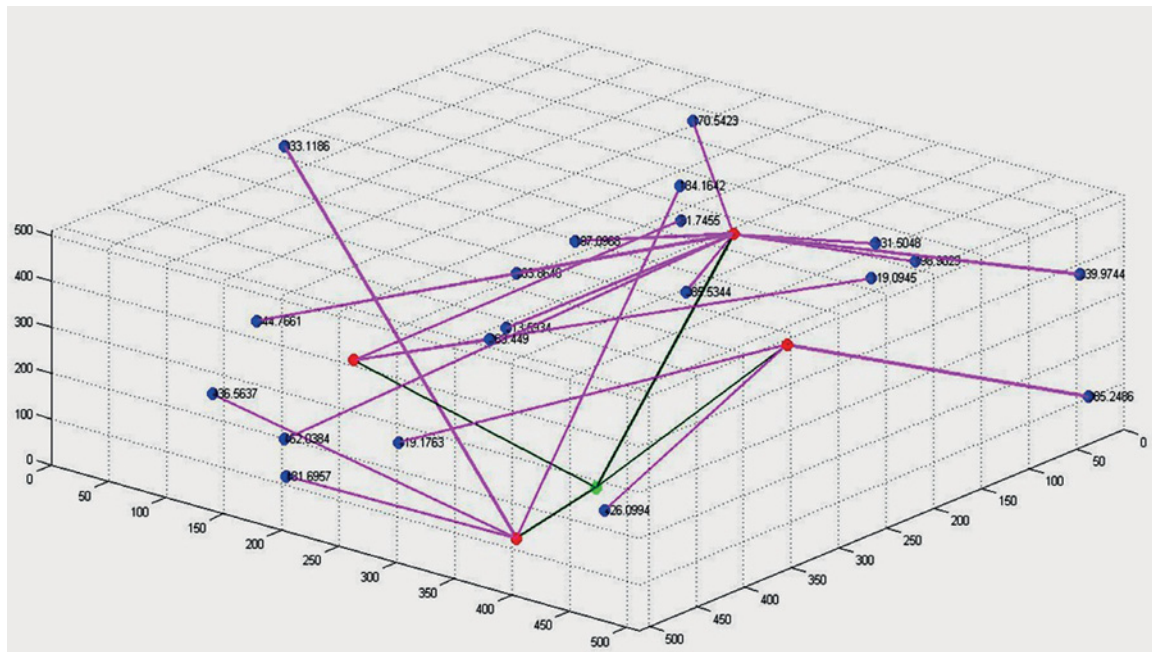
THERMAL DESIGN OF A GEOSTATIONARY ORBIT COMMUNICATIONS SATELLITE

BY **MURAT BULUT**, PHD, AND ASSOCIATE **PROFESSOR NEDIM SOZBI**, BOTH FROM SAKARYA UNIVERSITY IN TURKEY

One of the major technical challenges facing designers of a satellite in geostationary orbit is its thermal control subsystem (TCS). To ensure its equipment temperatures are maintained within limits, the satellite must be accurately modelled during its preliminary design phases.

In this instance, the use of the satellite's north and south panels as radiative areas was considered, as well as its payload, and we applied lumped-parameter network solver and generic model-builder software called ThermXL, a very flexible and easy to use tool.

Satellites

A geostationary (GEO) communications satellite has two main subsystems: payload and platform; the payload ensures the communications mission and the platform the mission control and stability. The payload includes a repeater and antenna, and telemetry, command and ranging (TCR) subsystems. The platform consists of the unified propulsion system (UPS), solar array, thermal control, harness and mechanical subsystems.

A satellite's operational life is at least 15 years. It normally uses a three-axis stabilized platform, with two main modules: for communications (CM) and service (SM), see Figure 2.

Figure 1 shows the configuration of a satellite in orbit, with its payload and platform equipment and constant conductance heat pipes (CCHP) that carry heat from the onboard equipment. The payload equipment can be located on the north and south sides of the satellite, as shown in Figure 3. The external surfaces of these panels are covered with an optical solar reflector (OSR) as a radiating area.

In the model, the 16 Ku-band and 4 C-band channels are in full operation. The location of 10 Ku-band and three C-band for the north panel are shown in Figure 4. Only eight Ku-band and two C-band channels are in full operation.

Figure 1: Configuration of a satellite in orbit
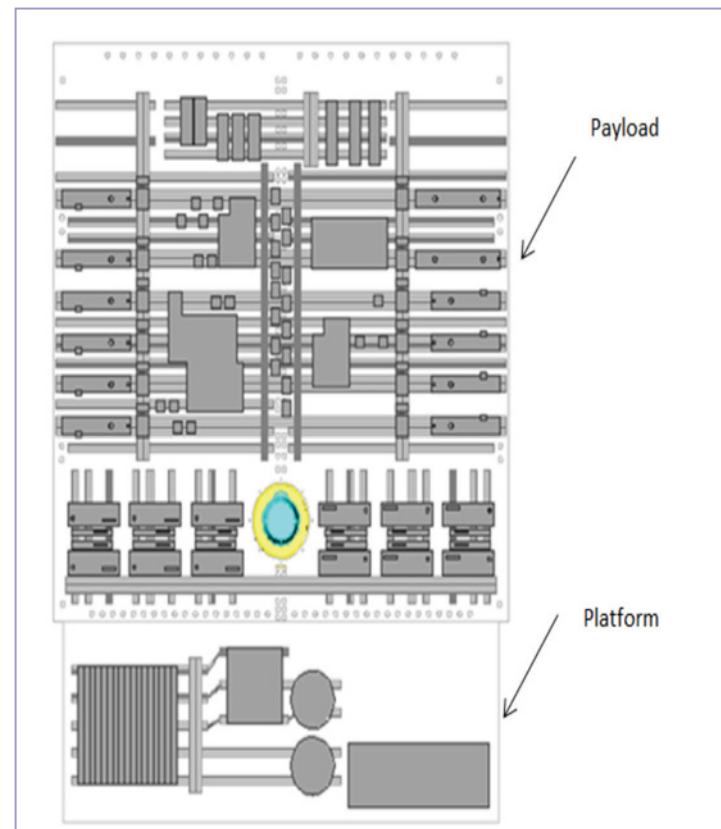
Figure 2: South panel payload and platform layout
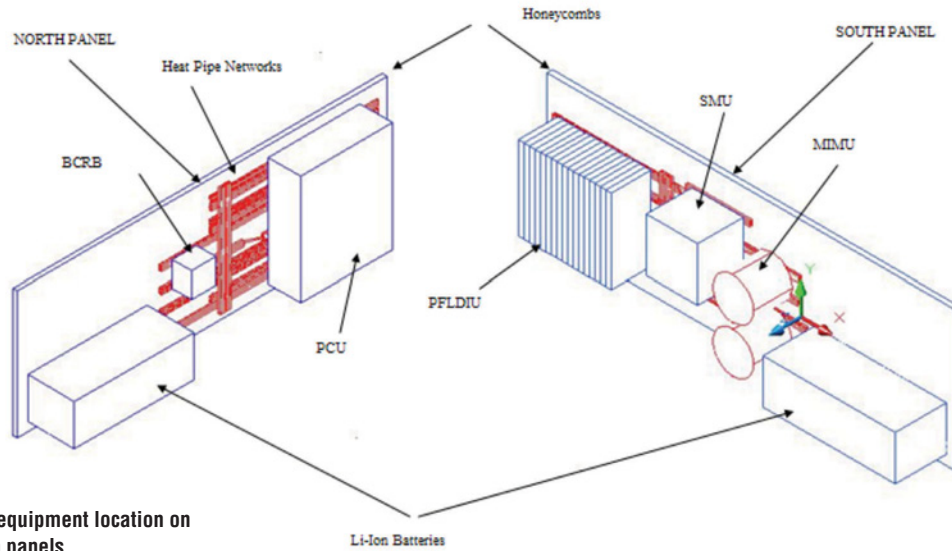
Figure 3: Platform equipment location on the south and north panels

The location of 10 Ku-band and two C-band for the south panel are shown in Figure 5. Only eight Ku-band and two C-band channels are in full operation.

Thermal Mathematical Model

Thermal models of a satellite are usually developed using a lumped-parameter network formulation, which involves dividing the object being analyzed into a network of discrete nodes, connected by thermal conductors. Each node is considered to be isothermal, i.e. a single temperature is associated with it. A thermal network is then drawn, connecting the nodes. A governing energy expression is written for each node:

$$(Mc)_i \frac{dT_i}{dt} = Q_i^d + (\alpha^s A^s q^s + \alpha^s A^A q^A + \varepsilon A^E q^E)_i - \sum_j \Im_{ij} A_i^r (\sigma T_i^4 - \sigma T_{jr}^4) - \sum_j K_{ij}(T_i - T_{jk}) \quad (1)$$
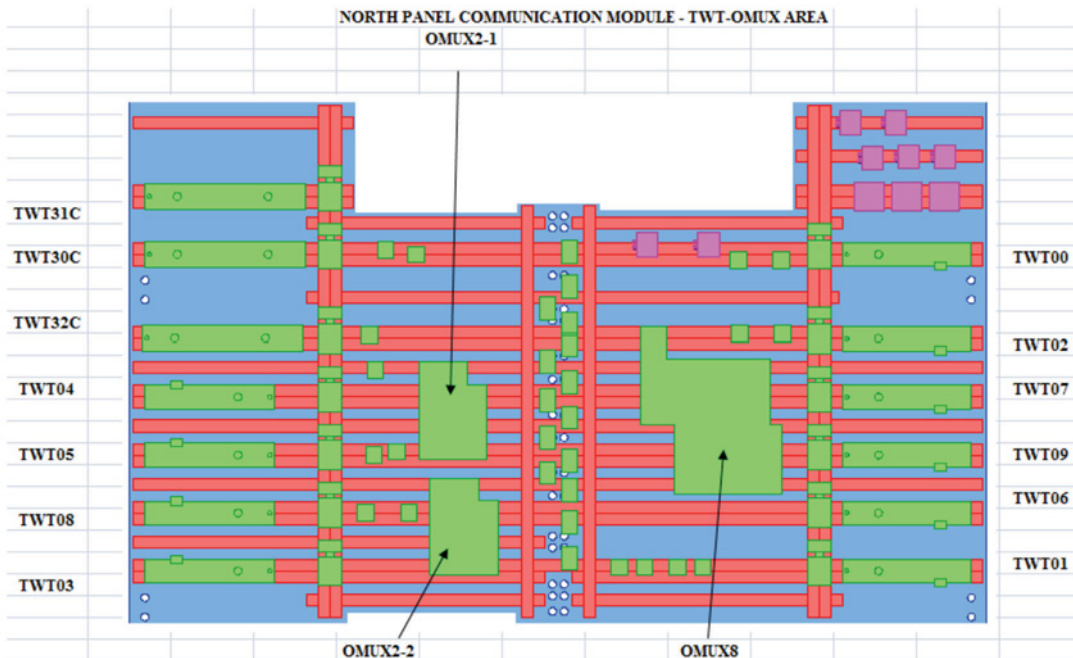
Figure 4: Payload equipment layout on the north panel
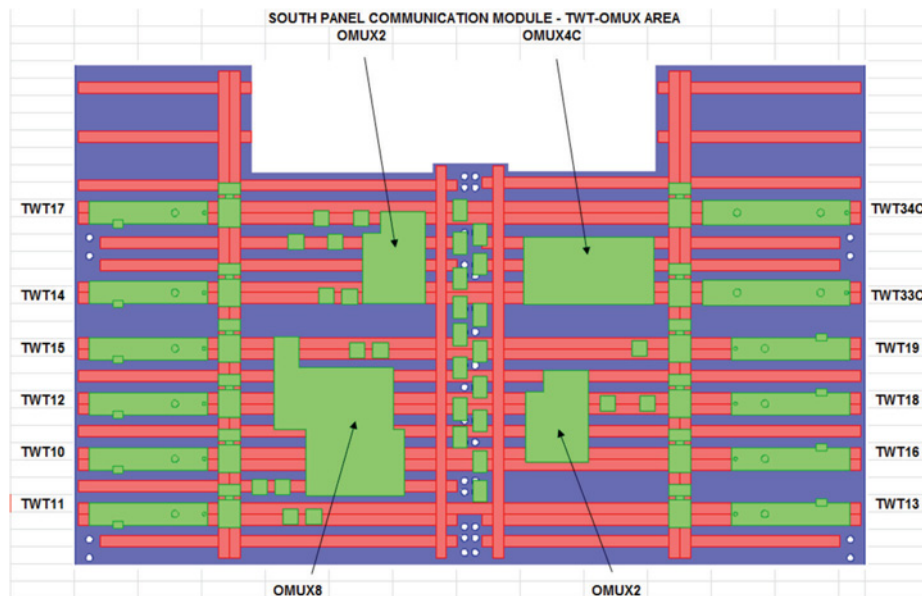
Figure 5: Payload equipment layout on the south panel

The equation consists of transient, conduction and radiation terms plus boundary conditions (solar, earth radiation, albedo – the proportion of incident light or radiation reflected by a surface) as a source term.

The left side of Equation 1 is the thermal capacitance of the structure's material. The righ side is the total operational heat load, Q_i^d, net absorbed external radiated heat flux, the total of net rejected radiation heat and internal heat conduction of each node.

To determine the steady-state (i.e. not time-dependent) total, a heat balance is applied to each node:

$$\sum Q = 0 \qquad (2)$$

All nodal temperatures are calculated by ThermXL.

To determine the transient (or time-dependent solution), a heat is applied to each node:

Figure 6: ThermXL nodes

$$\sum Q = (Mc)_i \frac{dT_i}{dt} \qquad (3)$$

where Q represents the heat input.

To determine the equipment temperature, the external heat fluxes and equipment heat dissipation must be known. These parameters are necessary for the ThermXL software to calculate the temperatures, thermal conductivity of the structure's material, infra-red emittance and solar absorption.

ThermXL Model Inputs

The number of nodes in our model is 392. The total conductively-coupled nodes and radiatively-coupled nodes are 963 and 75, respectively.

For our study we used a Traveling Waveguide Tube-Output Multiplexer (TWT-OMUX) area at the north panel communication module as an example.

In Figure 6, the total number of diffusion nodes (i.e. nodes to be calculated) is 82. There is also a boundary node (temperature between 0K and 4K), representing deep space. Diffusion nodes are calculated by the ThermXL software, and their number may
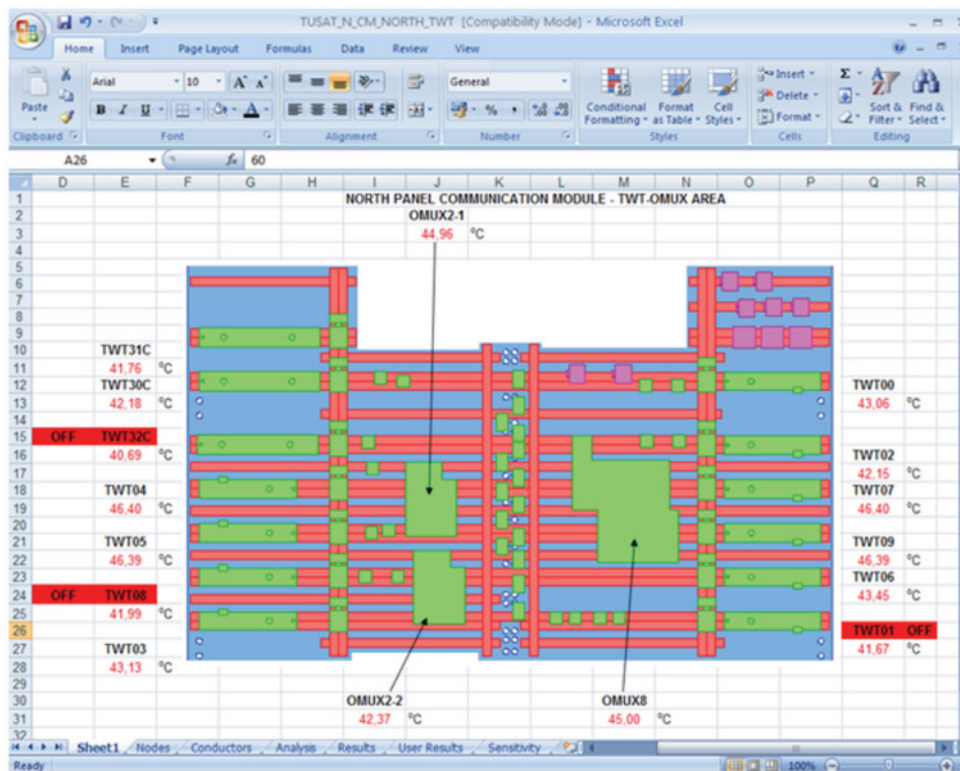
Figure 7: Temperature results on the north panel

Module	UNITS	Qualification Temperatures		Extreme Calculated Temperatures	
		Tmin(°C)	Tmax(°C)	Tmin(°C)	Tmax(°C)
	EPC	-15	65	-7,16	39,24
NORTH CM	CAMP	-15	65	-6,87	39,2
	TWT	-15	85	11,83	46,4
	OMUX	10	80	13,54	45
	TCR	-30	65	3,05	33,79
	EPC	-15	65	-7,01	37,83
SOUTH CM	CAMP	-15	65	-6,49	37,78
	TWT	-15	85	11,72	48,51
	OMUX	10	80	12,46	47,31
	Rx	-30	65	-0,18	35,02

Table 1: Payload equipment temperature predictions in GEO phase (cold case)

Module	UNITS	Qualification Temperatures		Extreme Calculated Temperatures	
		Tmin(°C)	Tmax(°C)	Tmin(°C)	Tmax(°C)
NORTH SM	Battery	0	40	9,4	27,3
	PCU	-30	70	5,8	36,5
SOUTH SM	Battery	0	40	9,2	26,3
	MIMU	-30	65	-5,1	39,8
	PFLDIU	-30	65	-8,2	40,2
	SMU	-30	65	-6,5	34,9

Table 2: Platform equipment temperature predictions in GEO phase (hot case)

vary depending on the accuracy we want to achieve.

We used 250 conductively-coupled nodes and 20 radiatively-coupled nodes for the north panel communications module. Any heat radiation between internal was neglected, but in the future we will use the ESARAD software (a thermal radiation analysis tool) to calculate radiation exchange factor.

Analysis cases are defined by determining the external thermal environment and operational conditions. Figure 6 shows how we've defined the nodes and changed the attributes of the existing ones for each case. All attributes can be changed apart from the temperature of the current and the thermal response time, which are calculated during the analysis. The attributes include group, number, label, type (boundary or diffusion), heat capacity (mC), solar absorption (α), infra-red emittance (ϵ), surface area (Area), absorbed solar power (Q_S), absorbed albedo power (Q_A), absorbed earthshine power (Q_E), internal power (Q_I), initial temperature (T_o), actual temperature (T) and thermal response time (RC).

Figures 7 and 8 show the ThermXL temperature results for the north and south panels, based on a steady-state solution. Tables 1 and 2 show calculated temperatures for the geostationary orbit for cold- and hot-case conditions.

In the cold-case condition, external heat loads are minimal; the satellite is operating with lowest heat dissipation and the thermal optical properties of the equipment coatings are not affected. In the hot-case condition, external heat radiation is at a maximum; the satellite is in operational mode with highest heat dissipation, and the optical properties of its coatings are reduced for the payload and platform panels. It can be seen that all unit temperatures remain inside the permitted range.

During the thermal analysis we used a passive thermal control system without a heater to control the temperature of the payload equipment, with multiple configurations. The analysis showed that the physical configuration of the equipment is one of the most important parameters to consider at an early stage of the design. ●
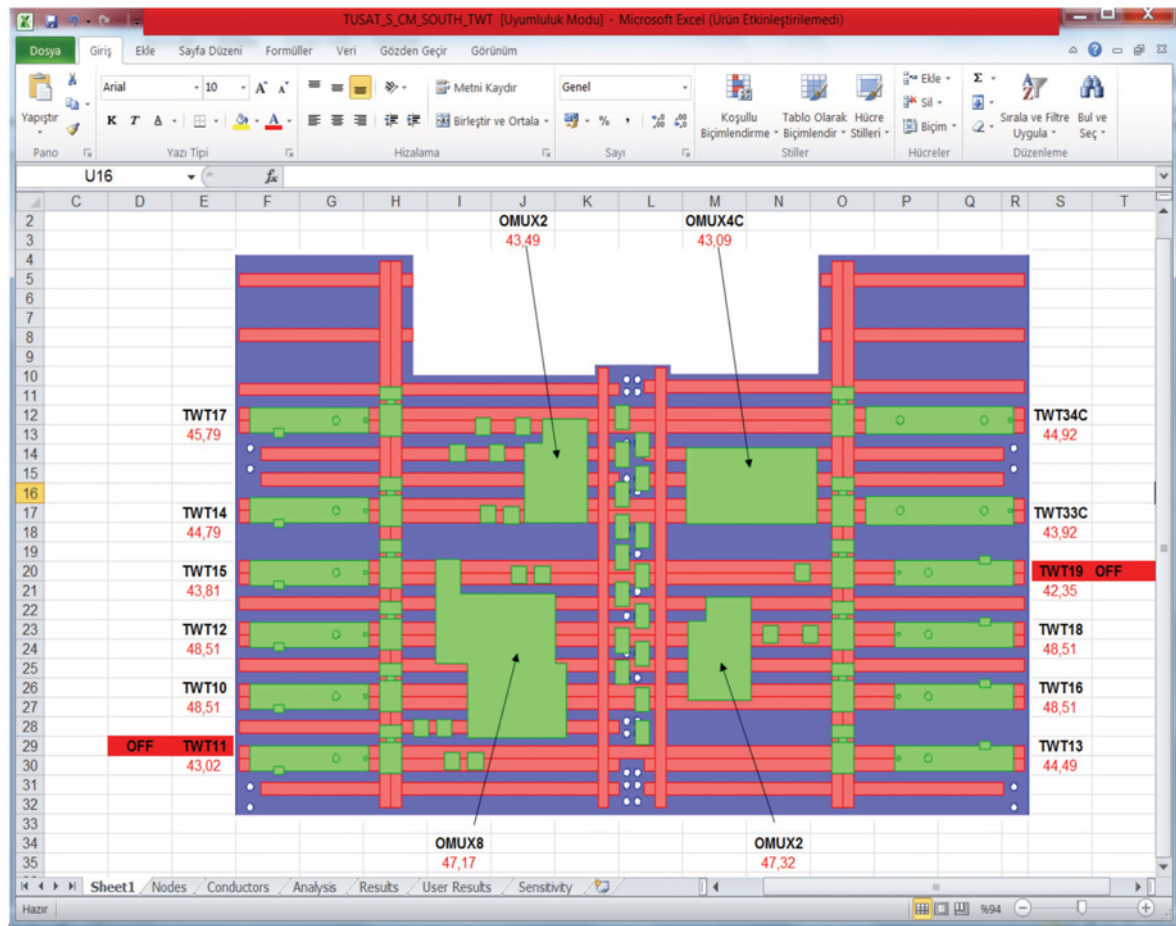
Figure 8: Temperature results on the south panel
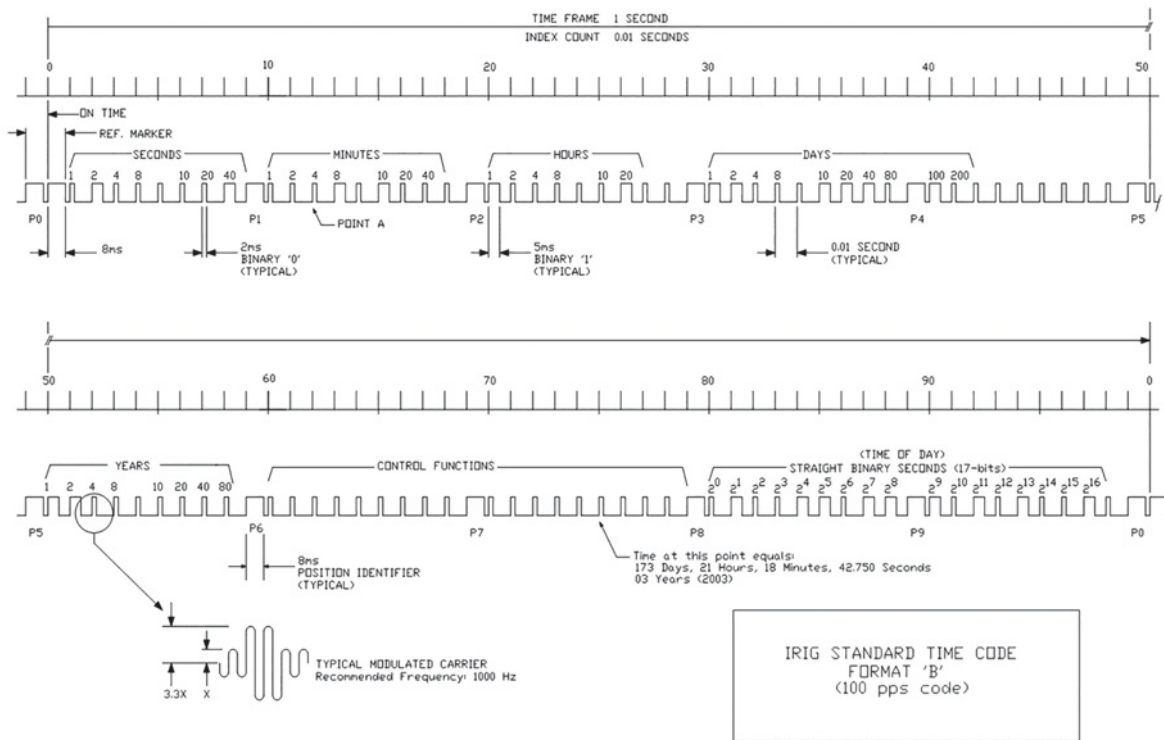
Figure 1: IRIG-B time code frame format

DESIGN AND IMPLEMENTATION OF IRIG-B TIME CODE DISPLAY

BY **SENOL GULGONUL**, TURKSAT SATELLITE COMMUNICATION AND CABLE TV ANKARA, TURKEY

Inter-Range Instrumentation Group (IRIG) codes are widely used in communications, data handling, missile tracking, telemetry and industrial automation systems for relaying timing information. The standard was developed by the Telecommunications Working Group of the US military's Inter-Range Instrumentation Group (IRIG), and first adopted in 1960.

The IRIG-B serial time code is 1kHz amplitude-modulated sinusoidal signal. Mark-to-space ratio is 10/3, and the sine wave carrier is amplitude-modulated by the time code bits synchronized to positive-going, zero-axis crossing. A single one-second frame duration consists of 1000 cycles of 1ms sine wave with three different types of signals – position identifier, binary zero and binary one, as shown in Figure 1.

The IRIG-B frame format (Figure 1) has 10 fields separated by position identifiers, each having 10 bits of binary decimal information, encoding seconds, minutes, hours, days, years, control functions and time of day.
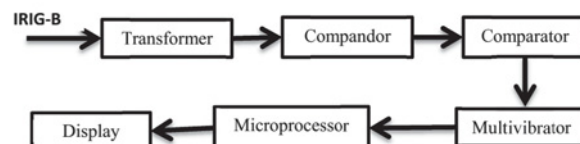
Figure 2: Block diagram of time code display
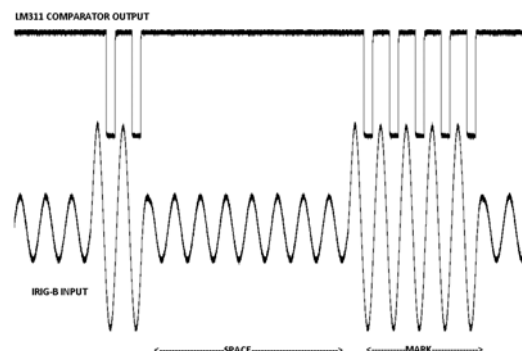
Figure 3: IRIG-B input and LM311 comparator output
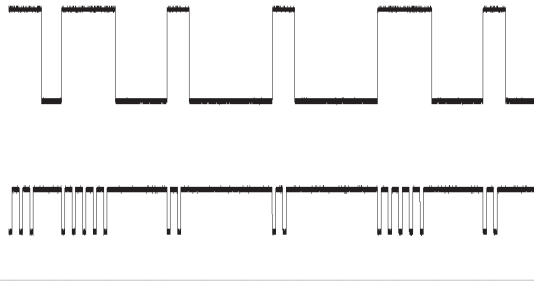
Figure 4: 74LS123 input and DC level shift modulated IRIG-B signal

```
while(true){
 switch(pulse_width){
  case 8: /*position identifier*/
    if this is consecutive position identifier reset hour, minutes and seconds.
    increment position identifier counter.
  case 5: /*binary one*/
    increment hours, minutes and seconds in accordance with format.
  case:2 /*binary zero*/
    display hours, minutes and seconds after 9th position identifier.
}}
```

Figure 5: Pseudo code of the PIC16F88 program

Figure 6: Time code display internal view
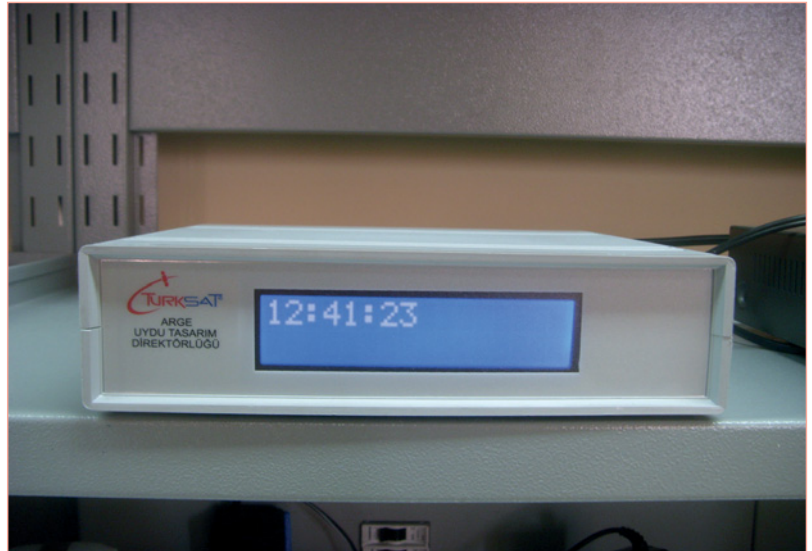
Figure 7: Final view of the time code display

IRIG-B time code displays are professional clock displays with hours, minutes and seconds found in satellite or missile control centres, TV studios, cockpits etc. A 1kHz IRIG-B signal is distributed from a master clock typically via coaxial or copper wire. The 1kHz signal is also suitable for transmission by short-wave radio stations, telephone lines and satellite TV audio channels.

We have designed a low-cost IRIG-B time code display using a single PIC16F88 microprocessor. IRIG-B signal is received at its 75-ohm BNC port, isolated, and the DC component is removed by a ETAL P1200 line-matching transformer. An NE571 compandor is used to sharpen the sine wave's zero crossings. The LM311 single comparator "catches" the negative peak mark bits of the sine IRIG-B signal by comparing them to the reference voltage (1.2V) of two diodes connected in series.

A remote trimming circuit with a 74LS123 retriggerable monostable multivibrator creates 10ms pulses with 80% (position identifier), 50% (binary one) or 20% (binary zero) duty cycles. The 74LS123 yields DC level shift modulated (DCLS) IRIG-B code. DCLS is a suitable format for the PIC16F88 to measure the input pulses' duty cycles.

DCLS modulated IRIG-B signal is connected to the Capture/Compare/PWM (CCP1) port of the PIC16F88. We can calculate the pulse widths by using rising-edge and falling-edge interrupts. The pulse width of the DCLS-modulated IRIG-B signal will be either 8ms (position identifier), 5ms (binary one) or 2ms (binary zero). Two consecutive 8ms pulses begin the frame and we can read each bit and increment hours, minutes and seconds at binary ones in accordance with BCD.

The time code display equipment uses 220VAC power, supplying +5VDC for the circuit. An UA741 operational amplifier supplies +12VDC and -12VDC for the LM311 comparator. We used a 16x2 monochrome LCD display to show hours, minutes and seconds in hh:mm:ss format.

If there is no signal at the IRIG-B port, the time code display uses its internal DS1302 timekeeping chip and displays a "*" after hh:mm:ss to alert to this condition. DS1302 is synchronized to IRIG-B time after each frame if there is a signal at the input port of the time code display. There are three buttons to adjust hours, minutes and seconds for standalone clock usage of the display without an IRIG-B signal. ●

Figure 8: Schematic of the time code display
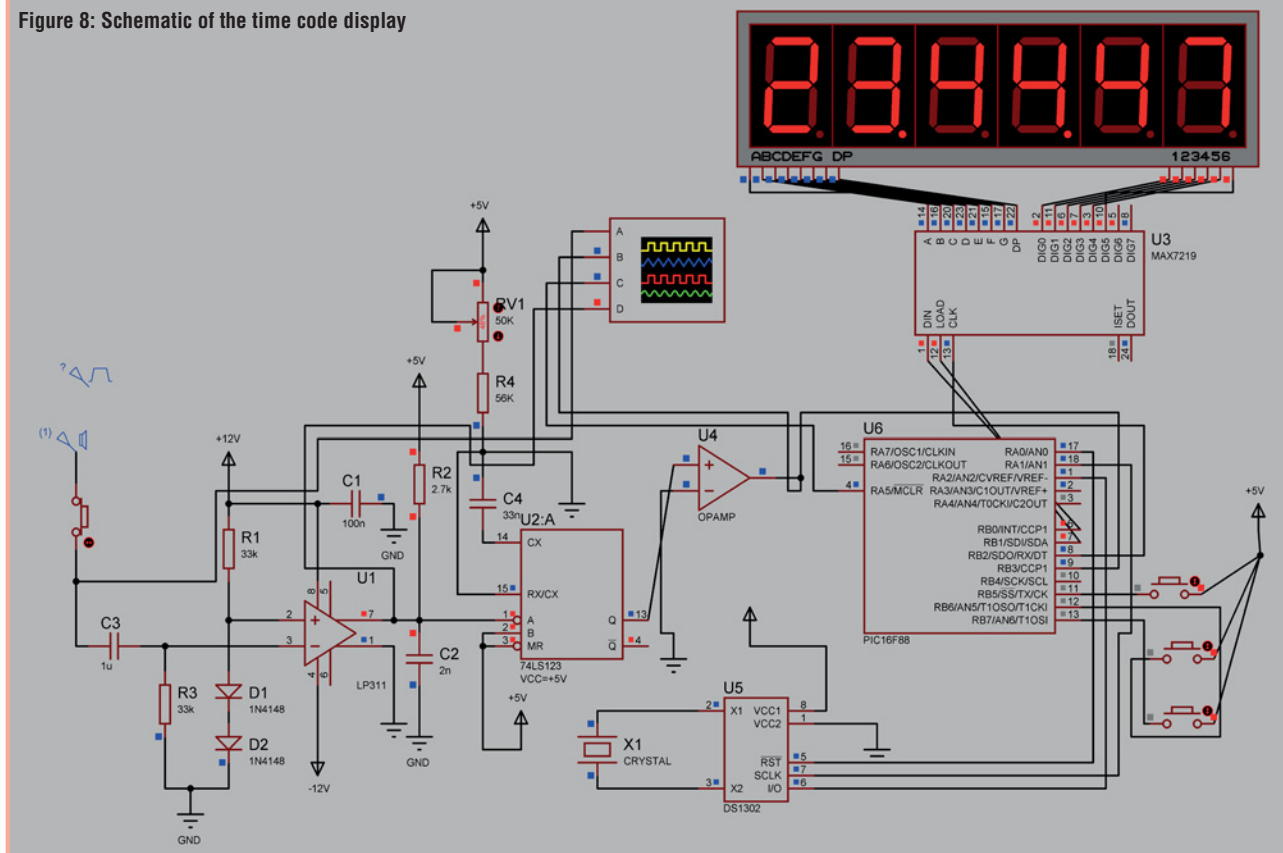
NEW OP-AMP DESIGN BASED ON MINIMUM-COMPONENT, CURRENT-FEEDBACK, SINUSOIDAL OSCILLATOR

BY **MUHAMMAD TAHER ABUELMA'ATTI** AND **NAYEF RADHYAN AL-MUTAIRI** OF THE KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS IN SAUDI ARABIA

S inusoidal oscillators are indispensible building blocks in many applications ranging from instrumentation and control to communication and other analogue signal processing systems. Over the years several sinusoidal oscillator circuits have been developed and reported in the literature using off-the-shelf integrated circuits like voltage-mode operational amplifiers (op-amps), operational transconductance amplifiers, plus-type second-generation current-conveyors and current-feedback operational amplifiers (CFOA). Of particular interest here are the CFOA-based realizations. This is due to the attractive features of the CFOA like its larger bandwidth and higher slew rate. Thus, sinusoidal oscillator circuits built around the CFOA are expected to work at higher frequencies than their counterpart using voltage-mode op-amps. Moreover,
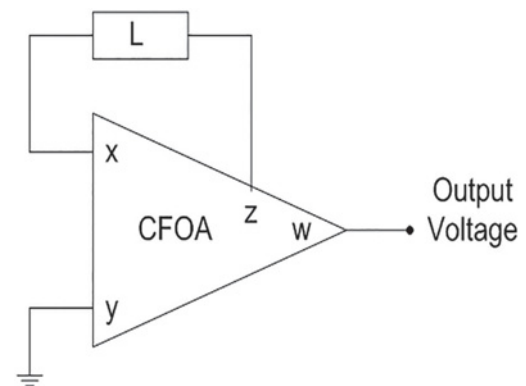
Figure 1: Proposed oscillator circuit using one CFOA and one inductor
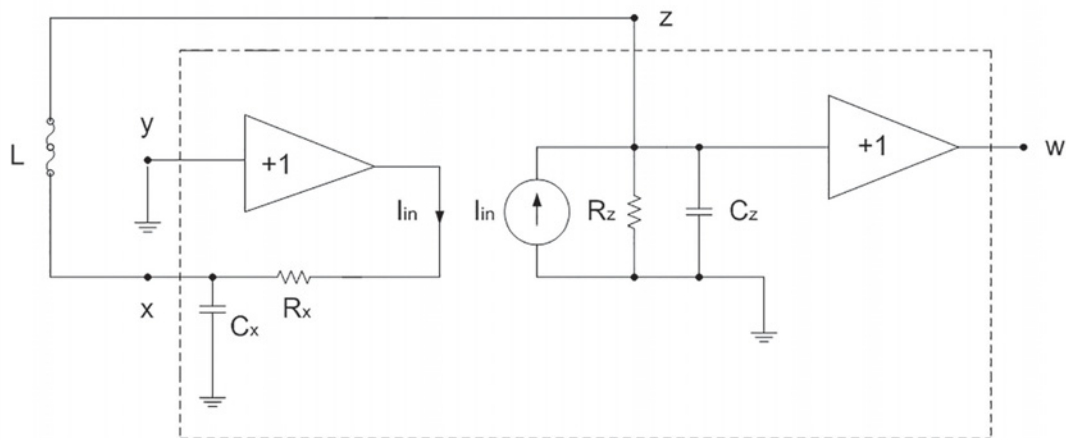
Figure 2: Equivalent circuit of the proposed oscillator circuit of Figure 1. The circuit in the dotted box is a simplified equivalent circuit for the CFOA

by exploiting the parasitic components of the CFOA, it is possible to further extend the operating frequency range of these oscillator circuits. Table 1 shows a comparison between some CFOA-based sinusoidal oscillators reported in the literature.

The maximum oscillation frequency reported by others is 40MHz, obtained using two CFOAs, three resistors and the parasitic components (internal poles) of the CFOAs. While using inductors is expected to result in higher oscillating frequencies, the maximum frequency of oscillation reported using a single CFOA, six passive components (one of which is an inductor) and the parasitic components of the CFOA is 10MHz. According to the Analog Devices data sheet of the AD844 CFOA, the bandwidth is 60MHz at gain = 1. Thus, it appears that the full bandwidth capability of the AD844 is not exploited to advantage yet. The major intention of this article is to describe a new CFOA-based sinusoidal oscillator using only one CFOA and one inductor that oscillates at frequencies up to 122.1MHz, exploiting the high-speed capability of the AD844 CFOA.

> The circuit produces sinusoidal signals with frequencies much higher than any previously reported using CFOA

Proposed Circuit

The proposed circuit is shown in Figure 1, where L is an externally-connected inductor and r its internal resistance. Its equivalent circuit is shown in Figure 2, where the dotted line represents a simplified equivalent circuit for the CFOA. Here, the capacitance C_x represents the parasitic capacitance at node x of the CFOA. Routine analysis of the circuit yields the characteristic equation of the oscillator circuit of Figure 1 that can be expressed as:

$$2R_z + s\left[C_x R_x R_z + L\right] + s^2\left[LC_z R_z + LC_x R_x\right] + s^3\left[LC_z C_x R_z R_x\right] = 0 \tag{1}$$

Applying the Barkhausen criterion (a mathematical model that helps determine when a linear electronic circuit will oscillate) to Equation 1, the oscillation frequency and oscillation condition of our circuit can be expressed as:

$$\omega_0^2 = \frac{1 + \dfrac{L}{C_x R_x R_z}}{LC_z} \tag{2}$$

and

$$L\left(\frac{C_z/C_x}{R_x} + \frac{1}{R_z}\right) + C_x R_x = C_z R_Z \tag{3}$$
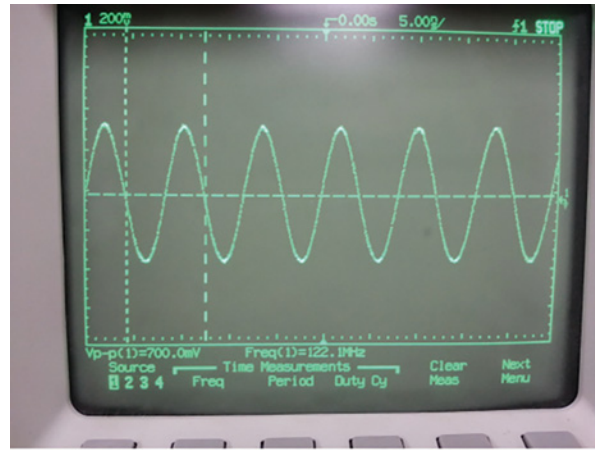
Figure 3: Typical output waveform at frequency of 122.1MHz obtained from the circuit in Figure 1 with externally-connected inductance L = 0.14μH
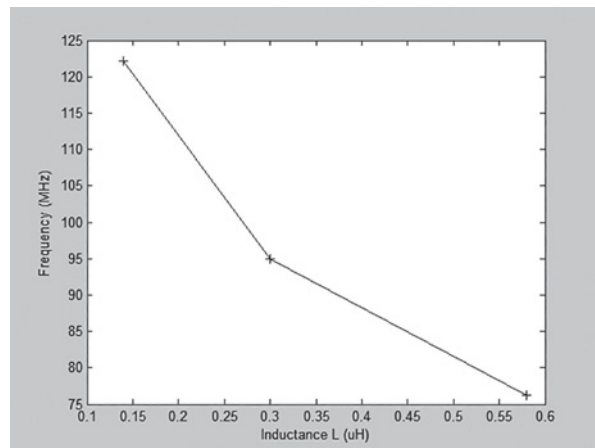
Figure 4: Variation of the frequency of oscillation with the externally-connected inductance L
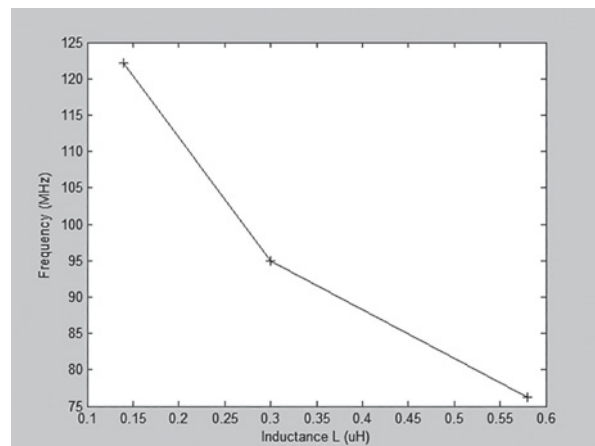
Figure 5: Variation of the peak-to-peak output voltage with the externally-connected inductance L

With $C_x = 5pF, C_z = 5.5pF, R_x = 50\Omega, R_z = 5M\Omega,$

where L is a few µH, Equations 2 and 3 reduce to:

$$\omega_0^2 \cong \frac{1}{LC_z} \qquad (4)$$

and

$$L \cong C_z R_x R_z \qquad (5)$$

It is worth noting here that extreme care must be taken when using Equations 2-5 obtained using the Barkhausen criterion. In fact, the results of this this criterion must be used as guidelines only.

Experimental Results

Our circuit was tested using the AD844 CFOA. A typical output waveform at 122.1MHz is shown in Figure 3. The variations in frequency of oscillation and the peak-to-peak amplitude with the value of the externally-connected inductance are shown in Figures 4 and 5. A comparison between the results shows that the frequency of oscillation obtained is the highest, showing that the circuit of Figure 1 can produce high frequencies using only one externally-connected inductor and exploiting the internal poles of the CFOA.

The circuit produces sinusoidal signals with frequencies much higher than any previously reported using CFOA. As expected from Equation 4, frequency of oscillation decreases as inductance increases.

It is worth mentioning that the proposed circuit was used to generate FM signals that were successfully received at a distance around 3 meters. The proposed circuit can, therefore, also be used as a simple FM generator. ●

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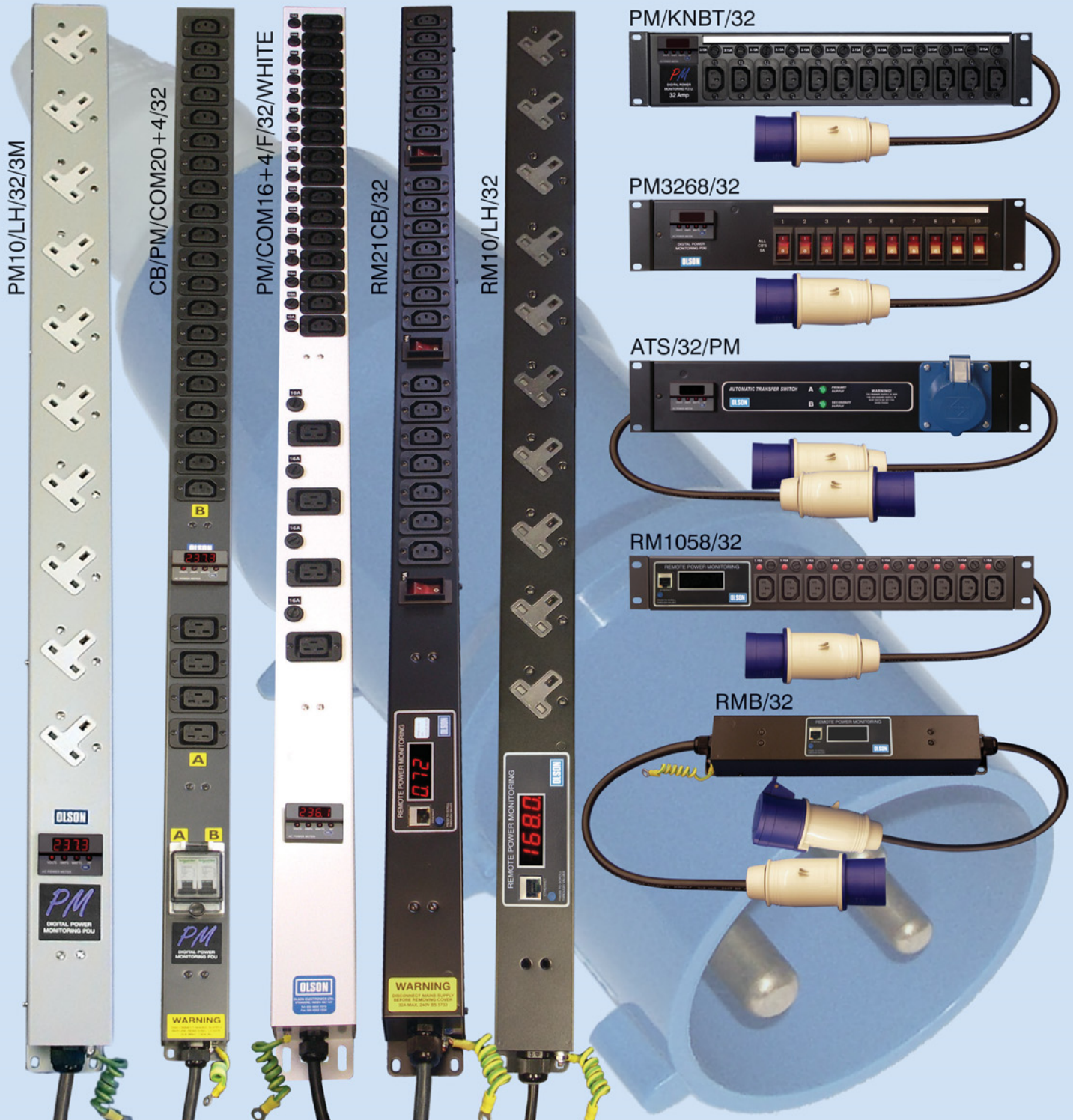
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CUSTOMIZING WET PROCESSING PARAMETERS

COMPANIES USING MICROFABRICATION CAN GAIN IMPORTANT BENEFITS BY USING WET PROCESSING EQUIPMENT DESIGNED TO HANDLE A VARIETY OF APPLICATION PARAMETERS. BY **ED SULLIVAN**, TECHNICAL WRITER BASED IN LOS ANGELES, CALIFORNIA

Since a burgeoning range of microelectronic devices have adopted the microfabrication techniques of semiconductors, there's increased attention on the design and selection of processing equipment that can make a significant difference in product quality and throughput.

Those potential gains exist for the vast range of applications that require microfabrication processes, including in the MEMS, biotech, photovoltaic, LED panel, sensor and other micro- and nano-technology industries. Products from all of these sectors depend on silicon and other semiconductor materials that undergo a variety of processes requiring specialized equipment, accessories and software.

The performance of that equipment and software (e.g., precision, throughput, flexibility) can be significantly improved though various types of optimization. Such is the case with the wet processing equipment used to etch silicon and other semiconductor materials used in microfabrication. A wide variety of equipment designs is available – both manual and automated – to accommodate the many different wet process requirements, which may vary in materials, throughput, size of products being processed and type of chemicals.

Essentially, manual processing equipment consists mainly of benches used for low-throughput applications in laboratories and production facilities with low volume requirement. Conversely, automated equipment is typically used for high-throughput, high-volume cleanroom applications, and is normally found within mass-production microfabrication environments. Usually having far greater complexities in terms of tooling and utilizing software, the automated wet processing equipment offers the highest potential benefits from some type of optimization.

Equipment Design

Fully automated process equipment for high-speed production often includes multiple stations or modules as well as robotics, sophisticated control, data logging and monitoring systems.

Since the design of many wet processing systems is proprietary, specifications are protected by the equipment manufacturers and

JST Manufacturing has an on-site applications laboratory where end users can develop their process with various chemistries and do tests on real equipment ranging from immersion and spray tools to dryers

users alike. Therefore, considering all possible design variables, it may be advisable for users in the market for an automated wet processing system to visit an equipment manufacturer with design capabilities and an application laboratory.

One of the prominent designers and builders of wet processing equipment, US-based JST Manufacturing has an on-site applications laboratory where end users can develop their process with various chemistries and do tests on real equipment, ranging from immersion and spray tools to dryers. The laboratory includes sophisticated metrology equipment, including a scanning electron microscope and a Tencor particle counter.

By visiting applications labs such as JST's, end users can "dial-in" on the optimization of their processes, and hence minimize the amount of chemicals required, and/or determine the tool features their applications need, saving on costs by eliminating features that are not needed.

Typical examples of automated systems include process modules for solvents, acid, bases, de-ionized water rinse and drying. Mechanical, ultrasonic or megasonic agitation and other processes may also be incorporated, if desired. Another consideration is safety, and there are many mandated requirements for items such as ventilation, fire suppression, chemical handling and explosion prevention.

Application-wise, systems designs may vary widely. In operation, there is quite a difference in the etching of silicone rods and the crystals used in nuclear sensors. One of the major differences may be the chemistry involved, its concentration and temperature. Chemical compatibility with the materials of construction is a must. Most solvents require stainless steel tanks and, in other cases, plastic tanks and baths may suffice.

Increased attention is being paid to the design and selection of processing equipment that can make a significant difference in product quality and throughput

Specific Approach

To facilitate the economical design and building of a wet processing equipment solution, many users insist on a standardized approach with customizable features that will best handle their applications parameters.

For example, JST utilizes standard products and standard methodologies to design and manufacture equipment. Using Solidworks's 3D-modeling software, minor changes and customizations can be made to meet the needs of each application. Also, the equipment is modular by design, allowing for easy changing and reconfiguration should a process or product requirements change.

Another powerful feature consists of each unit being designed with software capable of performing all tool functions, including those that are not required. With this, end users can create their own process, or recipes, with all sub-routines at their disposal.

"Customers have the added flexibility of programming their equipment to do everything it's capable of doing," said Louise Bertagnolli, JST president. "This enables them to get involved in applications, such as chemical concentrations. They can also turn various features on or off, depending on the process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful."

Optimizing Manual Applications

Specifying the design parameters for many manual benches may not be as involved as those of automated systems. However, soliciting the opinion of equipment manufacturers regarding equipment design may be highly beneficial.

Dennis Schweiger, Senior Director of Infrastructure at the University of Michigan's Lurie Nanofabrication Facility (LNF), feels that the right combination of user requirements and assistance from the equipment fabricator can make a significant difference in the design, layout and operation of a wet processing station.

The LNF is a world-class facility in all areas of semiconductor device and circuit fabrication, integrated microsystems and MEMS technologies, nanotechnology, nanoelectronics, nanophotonics and nanobiotechnology. The facility is based on open use with hundreds of users from various UM departments, as well as many other universities and businesses.

"Since we essentially rent lab space and equipment to our diverse users, it is important we provide them with benches that suit their purposes well, from those who are processing wafers to those who may be doing very advanced research or testing on non-wafer components," said Schweiger.

Schweiger explains that the original equipment design for the new lab areas wet processing benches was very specific, and determined by the LNF staff.

"We had looked at it in terms of process flow, from start to finish, not really taking into account the variety and variation of process samples that our user community might be working with; how we'd accommodate non-standard sample sizes, or what the impact might be in total cost of ownership with respect to chemical usage," he said.

Schweiger added that the some of the new benches had their decks reconfigured once the tools were installed. Several of the earlier benches, some of which were purchased over 20 years ago, were also modified to allow for more flexibility in meeting the process needs of the user community.

"In retrospect, our initial plan for the deck space and processing capability of the benches wasn't adaptable or flexible enough and we worked with JST to implement modifications so that the bench decks were simpler and could provide more working space," said Schweiger. ●

USING A COMPLEMENTARY WAVEFORM GENERATOR

MIKE GOMEZ, APPLICATION ENGINEER AT MICROCHIP TECHNOLOGY, EXPLAINS HOW A COMPLEMENTARY WAVEFORM GENERATOR FOUND IN 8-BIT MICROCONTROLLERS CAN HELP IN MOTOR DRIVE APPLICATIONS

A complementary waveform generator (CWG) can be handy when half-bridge and full-bridge control is needed, such as in motor drive applications, for example, and it's even better if the generator also has selectable input sources, polarity control, auto-shutdown and auto-recovery. These functions can be provided as a peripheral in some 8-bit microcontrollers with no processor overhead; Figure 1 shows a block diagram of such a peripheral.

Each block in Figure 1 represents a feature of the CWG, which generates a complementary output from one of several selectable inputs. The output can be modified in different modes of operation, such as push-pull, half bridge, full bridge and steering PWM.

The clock source can be selected and used to insert a dead-band delay between the pair of complementary output waveforms. Each output pin has individual output enable control, and the polarity of these pins can be controlled individually. The output can also be terminated immediately during a fault, and recovered when the fault is removed.

Selections

Input sources can be external inputs to the CWGxIN pin or outputs from other internal peripherals. The input source selection bits are used for selecting the input source. The input sources and bit selection settings may vary from device to device.

Some of the available peripherals that can be used as input sources are the comparator, capture compare PWM (CCP), numerically controlled oscillator (NCC) and configurable logic cell (CLC). First, the selected peripheral should be configured as the CWG's input. For devices that have peripheral pin select (PPS), the CWGxIN input pin can be moved to any other pin with the PPS input selection register (xxxPPS). By changing the "xxx" notation in the register name to CWGxIN, any available IO pin can be selected as CWGxIN.

The CWG output can be modified to operate in any of the following modes: half bridge, forward full bridge, reverse full bridge, push-pull and steering PWM. Mode selection is only available in some devices, where it can be selected by setting the mode selection bits. For example, Figure 2 shows the output of the CWG in different modes of operation for the Microchip PIC16F161X family.

In half-bridge mode, two output signals are generated as true and inverted versions of the input. In forward and reverse full-bridge modes, three outputs drive static values, while the fourth output replicates the input data signal. Toggling a bit in the register switches between forward and reverse mode.

In push-pull mode, the output signals generated are alternating copies of the input. In steering PWM mode, enabling the steering enable bits allows the input event signal to be replicated to any or all four CWG outputs. When steering enable bits are cleared, the CWG output signal is determined by the steering data bits. When using a synchronous steering mode, the next rising input event is required before the changes on the steering enable bits take effect. Whilst in the non-synchronous steering mode, changes on the steering enable bits take effect on the next instruction cycle.

The reference clock for the dead-band control can be selected from several different clock sources using the clock selection bits. As with the input sources, the available clock sources may vary from device to device.

Dead-Band Control

Dead-band control provides non-overlapping output signals during half-bridge mode, and direction changes during full-bridge mode. The signal prevents the cross conduction of external power switches. The selected clock source is used as a reference to create a delay.

A maximum of a 6-bit value can be placed in the rising and falling dead-band counter registers to indicate the count of clock delay periods. When CWGxB goes low, the rising edge dead-band starts to count and delays CWGxA for a ten-clock period before it goes high. Likewise, when CWGxA goes low, the falling edge dead-band starts to count and delays the CWGxB for a ten-clock period before it goes high.

Dead band is timed by counting the clock periods from zero up to the value in its respective count registers. There are instances when this time calculation may not be accurate, referred to as time uncertainty, as shown in Figure 3.

When the rising and falling sources that trigger the dead-band timer come from asynchronous inputs, such as the external input to the CWGxIN pin, it creates an uncertainty in the time.

Auto Shutdown

Auto shutdown – an active-low operation – can be triggered by a fault event source or by software execution. The fault event source can be selected using the auto-shutdown control register.

When the selected fault event goes low, the output pin will be in shutdown state. The output pin shutdown state can be selected as forced low, forced high, tri-state or inactive by selecting the auto-shutdown state control bits. Also, setting the shutdown bit of the auto-shutdown control register in software will force the output into shutdown state.

The shutdown state can be held until cleared by software or automatically, which requires enabling auto-restart using the auto-restart enable pin.
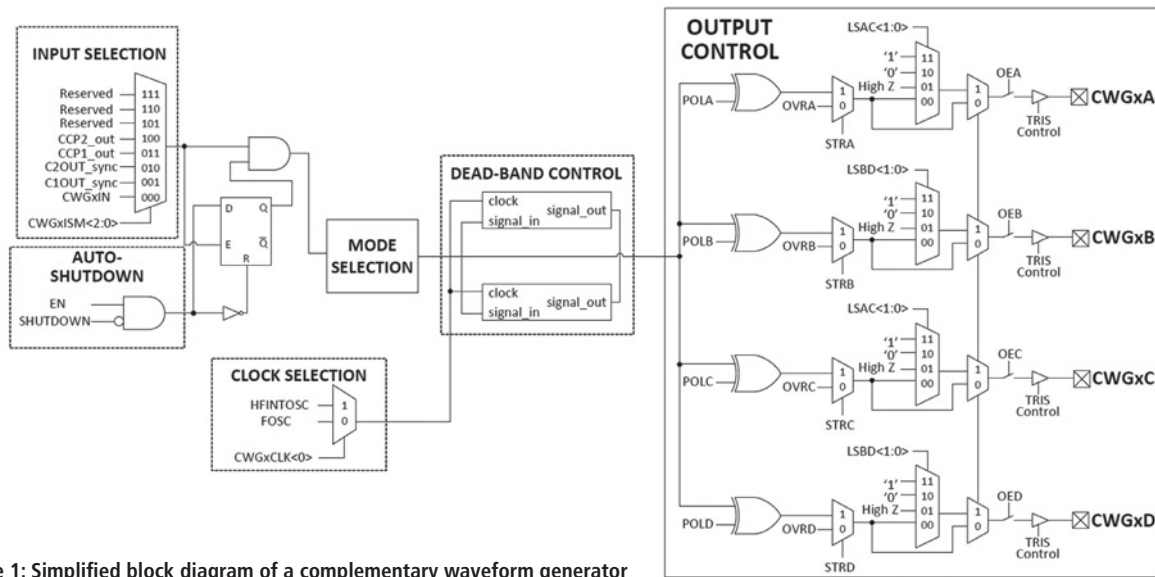
Figure 1: Simplified block diagram of a complementary waveform generator

Output Enable

Each CWG output pin has its own enable control. When an output pin enable bit is cleared, the CWG has no connection to the output pin. When the output enable is set, the override value or active waveform is applied to the pin as per the internal port priority selection.

Output control can be completely disabled by clearing the module enable bit. Output enables are selected in the CWG using the output enable bits; setting the bit enables the output. By default, the complementary drive is configured as inactive in output, whilst the complimentary drive is configured as active in output.

Some devices let the CWG output be moved from default pins to alternative pins using the alternate pin function. For devices that have PPS, there is no output control available. Instead, each device pin has an individual output selection controlled by the PPS register. When the output is not selected in the PPS register, the peripheral has no connection to the output pin.

Polarity Control

Polarity control can be set to invert the output signal, and the polarity of each CWG output can be selected independently. When the output polarity bit is set, the corresponding output will become active low. Clearing the output polarity bit configures the corresponding output as active high. Inverting the polarity of the output signal would allow two outputs to produce the exact same signal.

Configuration

Microchip's MPLAB code configurator (MCC) can be used to configure the CWG module. This user-friendly plug-in tool for the MPLAB X IDE generates drivers for controlling and driving peripherals of PIC microcontrollers based on settings and selections made in the GUI.

The complementary waveform generator found in Microchip's 8-bit microcontrollers provides precise half- and full-bridge control for motor drive applications. There are selectable input sources as well as dead-band and polarity control. It can also provide auto recovery and shutdown. ●
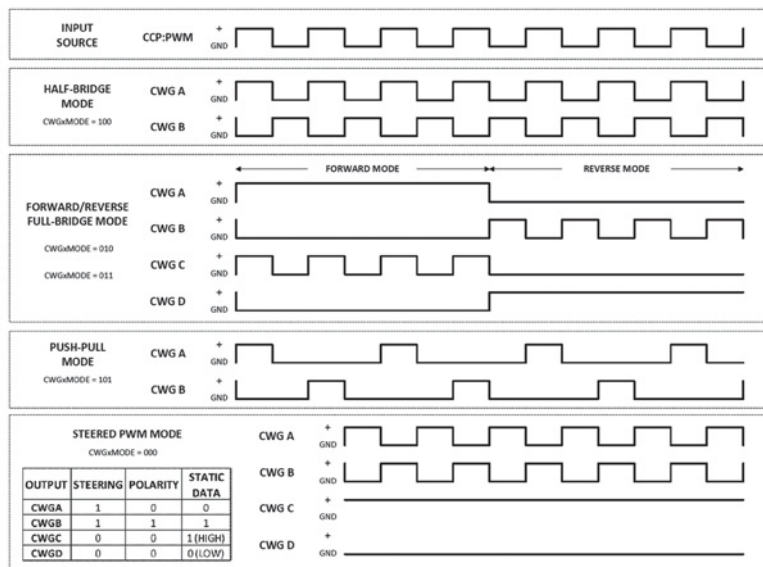

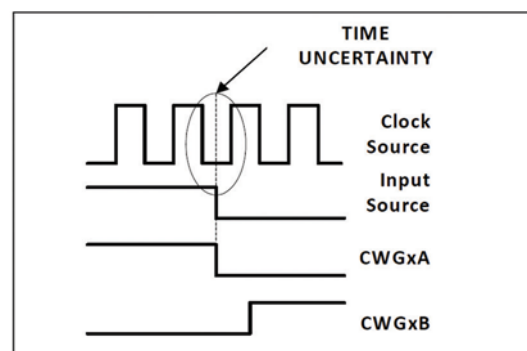**Figure 2: CWG modes of operation**

Figure 3: Time uncertainty

RS COMPONENTS INTRODUCES MICROCHIP LORA EVALUATION KITS

RS Components (RS) has added Microchip's new range of LoRa development kits to its portfolio of high-quality tools for Internet of Things (IoT) applications.

LoRa technology, driven by the LoRa Alliance, is for tracking and monitoring IoT applications with low data rates and a low-duty cycle for a variety of markets. Predominantly used for the uplink of sensor data, the bidirectional nature of the communications allows real-time acknowledgement of mission-critical data and downlink control of remote actuator nodes. The technology is capable of securely delivering two-way communication at data rates from 0.3-50kbps, and over distances of 2-5km in urban environments and up to 15km in suburban environments.

The Microchip kits provide all the required components necessary for a developer to create a low-power LoRaWAN network.

www.rs-online.com

RFID RANGE FOR WAREHOUSING AND LOGISTICS AT IMHX

Harting will be exhibiting its range of radio frequency identification (RFID) products at the IMHX show on 13th-16th September in Birmingham, stand UK14. Products will include the unique Ha-VIS LOCFIELD antenna and the new Ha-VIS RF-R300 UHF RFID reader, both designed to meet some of the toughest industrial RFID applications.

The stand will also feature live demonstrations to highlight how Harting's products help overcome the challenges of speed, location and environmental conditions. Tags of various design and specification, combined with a range of antenna designs and readers of appropriate power can be used to create solutions for almost every RFID requirement.

The Ha-VIS RF-R300 UHF RFID reader is of extremely robust construction allowing it to be placed in exposed and harsh environments.

www.harting.co.uk/harting-rfid

FAST AND EFFECTIVE TESTING OF ELECTRONIC MEDICAL EQUIPMENT

Rigel has introduced a new handheld safety analyser for routine electrical testing of basic medical and laboratory equipment.

The new Rigel SafeTest 60 is a compact, robust and reliable safety analyser suited particularly well to high-volume testing demands, with a simple colour-coded user interface, pushbutton operation and fast step-through of test routines.

The general purpose tester includes a range of safety tests for hospital and medical equipment such as medical beds and chairs, operating tables, hoists, infusion pumps and other similar equipment that does not require patient lead testing. As such, the SafeTest 60 is suitable for compliance testing with a range of international safety standards including IEC 60601, IEC 62353, IEC 61010 and NFPA-99. Also the unit can carry out insulation testing.

www.rigelmedical.com/safetest60

CONFIGURATION SOFTWARE STREAMLINES COMMISSIONING PROCESS

WAGO's new automation engineering suite of tools shortens development time for automation projects by bringing all tasks – including hardware configuration, programming, simulation and diagnostics all the way up to final commissioning – into one single platform. The e!COCKPIT software supports all CODESYS 3 languages, allowing engineers to spend less time learning the new system and more time using it.

An intuitive drag-and-drop interface means that even complex automation tasks can be engineered without the need for extensive training, allowing easy adoption by engineers. By using one single platform from end to end, machines can be brought online faster leading to increased productivity.

By merging mechanical, electrical and software components into the same system, e!COCKPIT offers shorter development cycles without compromising on functionality.

http://global.wago.com/uk

PROGRAMMABLE UNIPOLAR HALL-EFFECT SWITCH WITH BUILT-IN DIAGNOSTICS

Allegro MicroSystems Europe has announced a new unipolar Hall-effect switch with an externally-enabled diagnostic function and user-programmable switchpoints. Allegro's A1162 has on-chip electromagnetic coils used to implement self-test of the sensor's entire magnetic and electrical signal chain. It is designed for systems where precise magnet switchpoints and safety and/or reliability are critical, such as those designed to meet the requirements of ISO 26262.

In normal operating mode, the A1162 functions as a standard unipolar Hall-effect switch. The device output transistor turns on (output signal switches low) in the presence of sufficient magnetic field (> BOP max). The output transistor of the A1162 switches off (output signal switches high) when the magnetic field is removed (< BRP min).
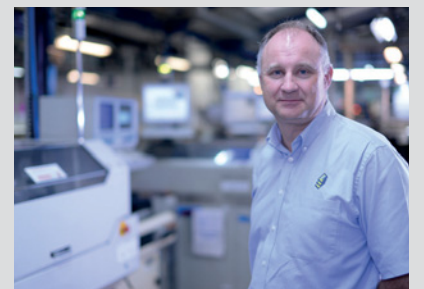
www.allegromicro.com

SPEEDBOARD ASSEMBLY SERVICES REPORTS TURNOVER INCREASE

Contract Electronics Manufacturer (CEM) Speedboard Assembly Services has closed its 2015-16 financial year with a turnover of £11.10m, up on the previous financial year by 20%, which was already a record year for growth at Speedboard, closing at £9.23m. Together, these growth figures represent an increase in turnover of 49% over a two-year period.

"We're delighted with this achievement, reflecting how we're outperforming most other CEMs," said Nick Fairhead (pictured), Speedboard's Sales & Marketing Director.

Reasons cited for Speedboard's continued growth are the company's new business wins as well as increased workload from existing customers, some of which have made Speedboard their 'virtual shop floor'.

www.speedboard.co.uk

Harmonic

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Geyer

Geyer Electronic eK was founded in 1964, selling electronic components from a small office in central Munich. 50 years on and Geyer is now well known as a manufacturer and supplier of high quality Frequency Control Products for the Automotive, Telecom, Medical and Security, Consumer/Multimedia and Industrial Electronics. With an international network of Sales Offices and distributors, factories in Taiwan, Japan and S Korean, and a Design and Test Center at its Headquarters in Germany, Geyer Electronic is able to offer dedicated support to their clients from design stage, through to volume production, manufacturing around 75 million parts per month to ISO9001, ISO 14001 and TS15949/AEC-Q200 standards

Geyer eK moved to their Headquarters in Gräfelfing, in the west of Munich, in 2002 where they were able to benefit from the access offered by the Autobahn routes, and opened a Design and Test Center in 2011 to develop the crystal products and to work with clients on custom-designed solutions for their applications. Since that time, the Design Center has been expanded and now offers a comprehensive consultation service from our team of five Application Engineers, providing design validation, custom samples and prototype devices, and 3D models of our components to help customers' engineers during

the design stages. We also offer the unique Y-Quartz App to help Design Engineers select the optimum crystal specifications to work in their system, supported by advice from our Application Engineers if requested.

Geyer Electronic UK Ltd, based at their office in Romsey Hampshire, supports customers in the UK and Ireland by working closely with their R&D teams, using the Munich sales support and Design Centre to help identify the optimum crystal, oscillator, SAW filter or resonator for their projects and supplying samples for evaluation and prototype builds.

Contact: sales@geyer-electronic.co.uk
or by phone on +44 (0)1794 329341

Stand: J6

Electroquartz

Euroquartz is the sole remaining UK quartz crystal manufacturer of high specification HC49U, UM1 and UM5 crystals, as well as a range of military clock oscillators and crystal filters.

Manufacturing, engineering and sales are situated in a custom-built modern facility in Crewkerne, Somerset, UK from where a comprehensive range of frequency control products is also offered. The recently upgraded facility enables Euroquartz to perform full military screening tests and qualification testing on all other products in the company's portfolio.

The test capabilities of the facility include accurate frequency measurement, temperature cycling, acceleration testing, gross leak, fine leak, filter characteristic testing as well as active burn-in routines. Custom crystal selection testing is also offered from the Euroquartz test facility.

Founded in 1982, the company has a wealth of experience and technical knowledge making it a leading specialist in the field of frequency products. Customer service and quality are the main driving forces behind the business, a fact clearly demonstrated by the company's AS9100 quality

certification awarded in 2015.

As a long-standing and well respected manufacturer in its own right, Euroquartz has access to many very specialised sources of supply that are not available from many of their competitors.

Euroquartz is a privately owned British-company providing a flexible and quality service unrivalled in the frequency control field.

Contact: Tel: +44 (0)1460 230000
info@euroquartz.co.uk

Stand: F2

EUROPEAN MICROWAVE WEEK   WWW.EUMWEEK.COM

Electro Rent

Since 1965, Electro Rent has been giving its customers alternative ways to acquire, implement and manage their test equipment resources. The company provides flexible equipment rental and leasing, new and used sales, and full service solutions. By offering this range of services Electro Rent ensures that its customers can get the equipment they need, when they need it and at a cost that's within their budget.

The inventory includes a comprehensive range of RF/Microwave, Power Systems, Communications and General Purpose test equipment used by companies operating in the aerospace and defense, semiconductor, telecommunications and electronics industries.

Electro Rent can supply equipment from over 200 suppliers, and has longstanding relationships with all of the major test equipment manufacturers, particularly because it buys its inventory pool new from those manufacturers. The company has the largest inventory of test equipment in the world and all of this equipment can be supplied on a rental or leasing basis. In addition because the inventory is turned over regularly there is always a selection of ex-inventory used equipment available for sale.

Electro Rent's global network of dedicated account managers and professional business specialists help you plan your procurement strategy. Internal technical professionals handle all requests efficiently and risk free: quote requests, availability, fast delivery and more.

Contact: www.electrorent.co.uk • sales.uk@electrorent.com

Stand: 171

ELECTRONICA   WWW.ELECTRONICA.DE

ODU: not your average connector company

As a problem-solving connector manufacturer, ODU enjoys single-source status with over one hundred of the world's top manufacturing companies. Why is that? Because, not only does it have expertise, but it works hard at being a flexible and innovative supplier.

In the UK, ODU is probably best known for its miniature military push-pull connectors.

Notably, since 2002, ODU has supplied more than 100,000 helmet connectors for use on the UK Bowman military communications programme, without a single reported connector failure.

The AMC (Advanced Military Connector) series was originally developed to meet the ever-demanding needs of the many international 'Future Soldier' programmes, intended to equip the average ground-based combat soldier with an integrated set of high-technology systems, linked to an array of battlefield information resources.

Now this range of rugged connectors has been expanded to offer high-performance data transmission, high bandwidth, high reliability and easy handling in any harsh environment and in sizes that are typically a third smaller and lighter than MIL-Std housings.

The AMC range includes numerous high-density signal configurations, with transfer rates up to 10Gbit, and versions for combined signal and power up to 15A, in a compact package.

Performance characteristics include 5,000 mating cycles, push-pull or break-away functions for maximum safety, watertight to IP68/IP69, optimised mechanical and colour coding, highly reliable 360° shielding, operating temperature of -51°C to +125°C, salt spray resistance and so on.

ODU will be at several exhibitions this year so, if you are faced with a connector or packaging problem, then why not come and talk to its representatives, or get in touch now:

Contact: miniaturemilitaryconnectors.co.uk

**Hall: B2
Stand: 143**

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Apacer: the most reliable storage for industrial and embedded applications

Apacer Technology Inc was founded in 1997 in Taiwan and positioned itself to be an agile supplier of DRAM whose primary operations focused on memory modules. By 1999 Apacer had become the world's fourth largest memory module manufacturer.

With an optimistic view on the flash market and as a response to the changes in the memory industry, Apacer developed its industrial memory line in the early years of 2000.

Today, Apacer offers a large portfolio of innovative Solid State Drive Solutions (SATA, PATA, Flash Cards and USB) and DRAM Solutions (desktop, notebook and server) for the industrial and embedded markets. More recently, Apacer developed a range of data security technologies by launching data security enhanced products and unique value added features.

One of our strengths lies in its customization capabilities: its industrial SSD line offers a wide range of different specifications in terms of size, angle, thickness and functions such as high capacities with strong performance, wide temperature support and shock- and vibration resistance for various industries: military, aerospace, networking, medical, automation, gaming etc.

Apacer's DRAM module technology development is focused on vertically integrating know-how in the semiconductor industry, manufacturing memory modules that satisfy the requirements of quality, performance and, yet, can be easily integrated into various platforms.

Contact: eu.apacer.com

**Hall: A6
Stand: 439**