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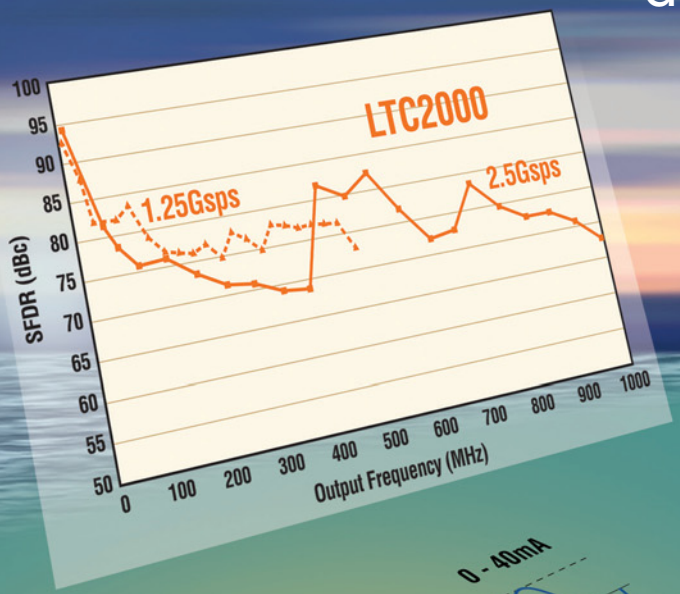
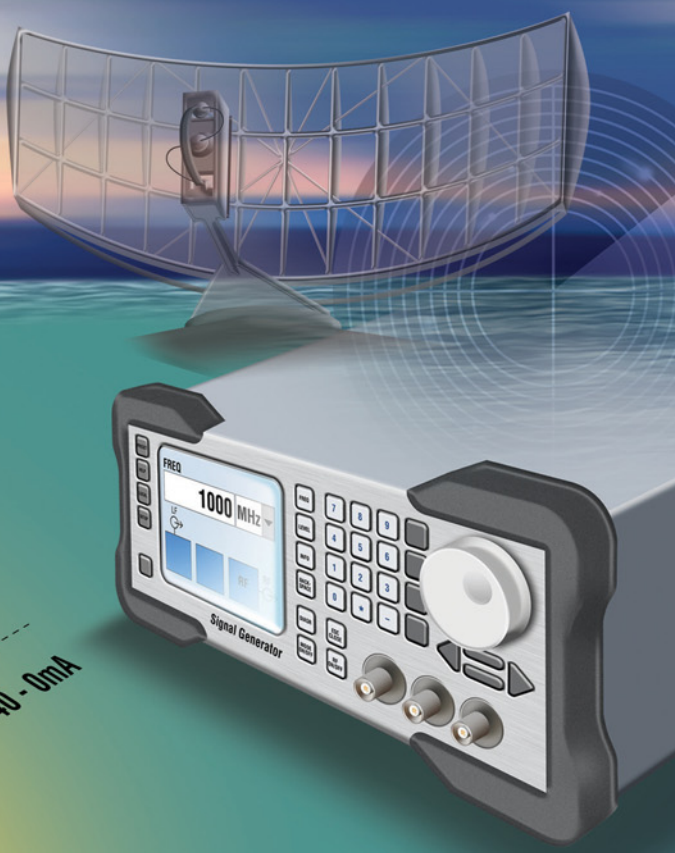
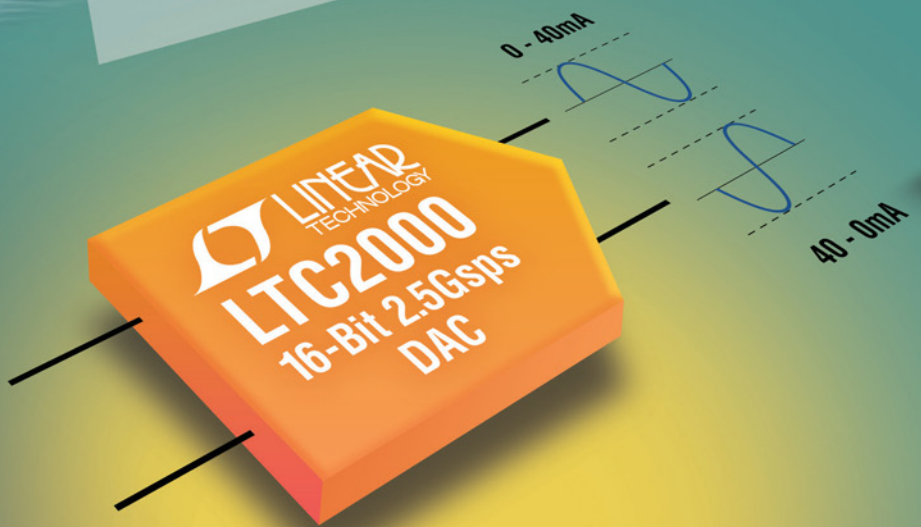
Critical Design Criteria In High-Speed Signal Generation

addressed by Linear Technology







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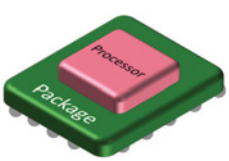

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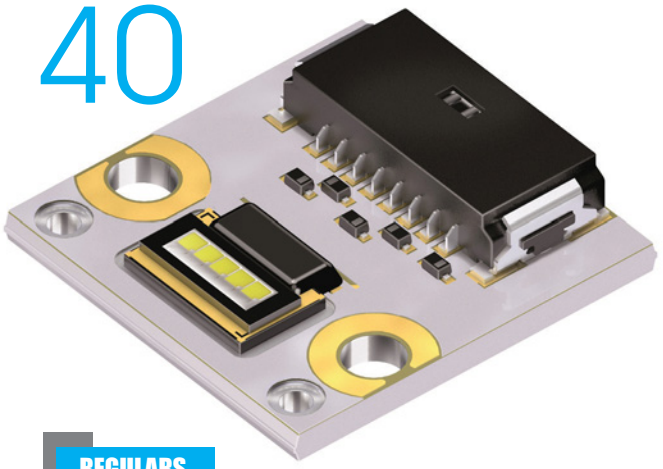

REGULARS

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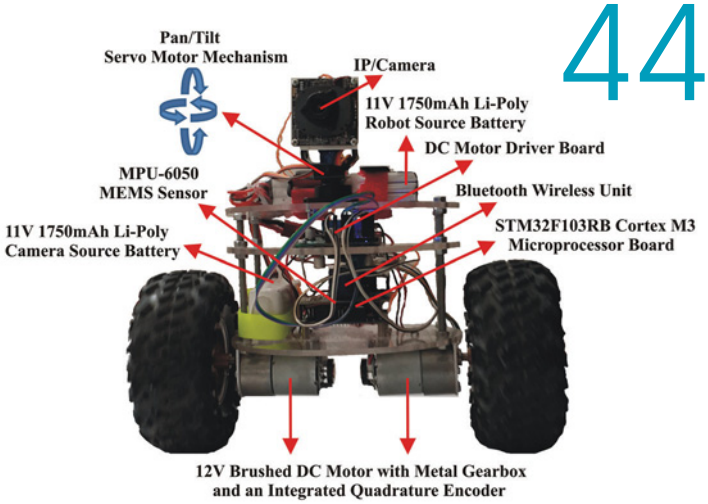

FEATURES

Isn't It About Time Your Design Got Connected?

Microchip is a leader in wireless solutions for embedded systems. With a broad portfolio of standards-based and proprietary wireless technologies, Microchip's wireless solutions are designed to be easy to use for fast prototypes, and even faster time to market. With our industry-leading ultra-low power Wi-Fi®, Bluetooth® Smart silicon and module solutions, short-range ZigBee®, MiWi™ Wireless Networking Protocol, Sub-GHz, and long-range LoRa™ technology, Microchip has the wireless solution for any application.

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FUTURE HIGHWAYS: APPS ARE CHANGING THE DRIVING EXPERIENCE

Today's cars would seem unrecognizable to a driver from 1886, when Karl Benz's petrol-powered automobile was introduced. As today's automotive manufacturers join force with technology companies to produce digital driverless cars, tomorrow's automobiles may seem just as unrecognizable to today's drivers.

A large part of the functionalities of today's vehicles is through apps, including weather reports, phone calls, alerts to road hazards, and entertainment. So to continue to provide the experience customers expect, brands must ensure that these technologies work seamlessly.

Cars are an emotional, brand-driven object: sports cars can make us feel cool; a 4×4 may make us feel rugged and adventurous; and a 4-door saloon reminds us of family and comfort. A luxury car may make us feel classy and, well, luxurious. The in-car experience is an extension of the brand and must be consistent with it if companies are to expect loyalty from their buyers.

A car marketed as a secure, dependable, family vehicle should have a telematics system that includes entertainment apps for children, as well as child safety apps such as automatic safety locking that parents can activate from their smartphones. For rugged, outdoor adventure vehicles, telematics systems will need to provide top-notch navigation and extreme weather warnings in remote locations.

Delivering a consistent digital experience to users through in-car apps can be a technical challenge, requiring the multi-tier architecture between mobile device and car to operate seamlessly. Apps must also work consistently across different car models and different smartphones, creating huge challenges for companies striving for a seamless, consistent experience.

As part of this challenge, ensuring swift response times is of particular significance for car makers when looking at the communication between apps and dashboard infrastructure. When commands pass from a smartphone to a remote server through to the dashboard, every millisecond counts.

Another technical challenge concerns release cycles. Auto manufacturers typically operate on a yearly release cycle, with a new model of each car introduced annually. However, mobility is changing the way manufacturers work. Due to the rise in digital products, auto makers will need to shift to more frequent updates of their apps, requiring shorter testing and development cycles for software rather than hardware.

Delivering a consistent digital experience to users through in-car apps can be a technical challenge as it requires the multi-tier architecture between mobile device and car to operate seamlessly

In meeting these challenges, testing is crucial to ensure that apps function consistently across disparate devices. Auto manufacturers need to know that their tests reflect users' real experiences, and need testing tools that guarantee this.

Testing systems should also be able to mirror the full user experience, including use of multiple apps at once. For example, auto makers need to know how a passenger will experience texting and using navigation apps at the same time.

Most car manufacturers today have global reach, which means they need to ensure their telematics systems and apps work seamlessly anywhere. For example, if an American company is selling cars in Japan, it needs to test the app experience of users in Japan accurately, including testing Japanese mobile phone networks.

But with the mobility inherent in a car's nature, manufacturers cannot test apps against only one location; they also need to compare experiences across disparate geographical locations and marketplaces.

As cars get smarter, automotive manufacturers that do not use branded telematics might miss a key market opportunity and risk falling short of consumer expectations. Businesses must therefore make sure that the in-vehicle digital experience they offer is consistent. To do so, manufacturers should use the right testing tools to ensure that apps are thoroughly tested and prepared for different conditions, geographies and networks, so that drivers have a seamless experience wherever the road may take them.

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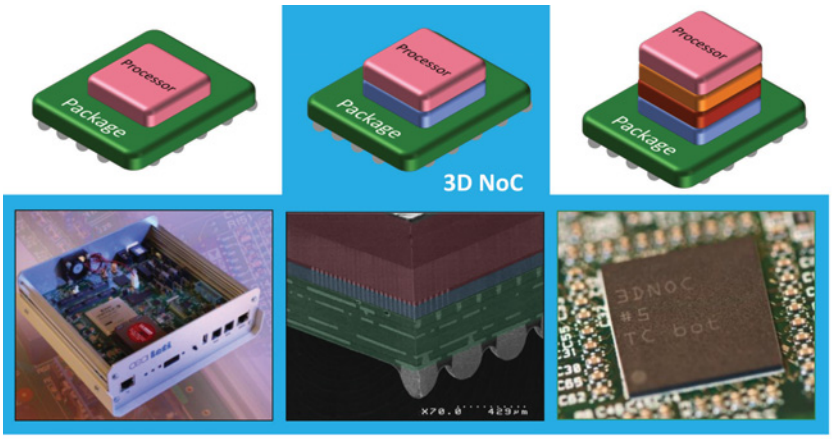
LETI DEVELOPS 3D NETWORK-ON-CHIP TO IMPROVE HIGH-PERFORMANCE COMPUTING

Leti, a CEA Tech institute, has developed a new on-chip communications system to improve high-performance computing (HPC), making it faster and more energy-efficient than current solutions and compatible with 3D architectures.

The structure was formed by stacking chips on top of each other in a single enclosure, or by placing them side by side on a silicon interposer. The chips, which have progressed from demonstrator to fabrication-ready, exchange data via a new communications network that is part of the network-on-chip (NoC) called 3D-NoC.

3D-NoC technology has been demonstrated with a homogeneous 3D circuit comprised of regular tiles assembled using a 4 x 4 x 2 NoCs. It also features robust and fault-tolerant asynchronous 3D links and provides 326MFlit/s @ 0.66pJ/bit. It was fabricated in a CMOS 65nm technology using 1,980 through-silicon vias in a Face2Back configuration.



3D-NoC structure formed by stacking chips in a single enclosure, or by placing them side by side on a silicon interposer

The 3D circuit, currently in foundry, combines a series of chiplets fabricated at the Fully Depleted Silicon On Insulator (FDSOI) 28nm node and co-integrated on a 65nm CMOS interposer. The active interposer embeds several lower-cost functions, such as communication through the NoC and system I/Os, power conversion, design for testability and integrated passive components. Moreover, the chip requires 20 times less energy for data transmission than chips placed on an electronic circuit board.

This new IP is compatible with standard remote direct memory access (DMA) software used for data transmission, and has likely industrial uses in virtual-server migration applications.

"The steady rise in the number of applications that require high-performance computing creates a demand for new hardware-plus-software communications solutions that improve both performance and energy consumption," said Denis Dutoit, Leti strategic marketing manager. "This new technology brick makes it possible to transfer data between processors via a network-on-chip delivering more powerful, energy-efficient computing."

LONDON RESEARCHERS DEVELOP ANTI-INTERFERENCE CONNECTOR FOR MOBILE NETWORKS

WaveWay connector promises to reduce PIM interference on communications networks

London South Bank University (LSBU) and Hughes Electronics have developed a connector called WaveWay that is less susceptible to interference on mobile networks than current designs.

There isn't a single mobile phone user not familiar with interference, most of it caused by passive intermodulation (PIM) – created when two or more interacting signals pass through cables and connectors. PIM is the leading culprit in the degradation of signal quality and strength. Metal connectors currently used by large telecom companies are particularly vulnerable to PIM, suffering from greater susceptibility to external signals and corrosion. In addition, common connector designs are poor, leading to longer installation times and signal loss.

Among other sources of PIM are humidity and temperature, and all these factors combined result in weaker signal strength, slower data speeds, increased buffering and overall poor performance on mobile devices. 4G is much more sensitive to PIM interference too, and with 65% of the world expected to be covered by 4G by 2019 that means the existing infrastructure cannot meet the future demands of mobile users.

"Passive intermodulation is a major headache in cellular networks. Mobile phone communication that we now depend on, such as 4G and the future 5G technology, suffer more from PIM than previous technologies, so it's vital that operators take action. We can't simply keep pumping more power," said Dr Sandra Dudley-McEvoy, Director of Research and Enterprise for the LSBU School of Engineering.

WaveWay is the first connector exclusively designed to tackle the sources of PIM. Its new, non-metal design, without any gaps for the signal to escape, is waterproof, easier to install and future-proof, i.e. compatible with 5G technology.

WaveWay is currently being tested by a top tier industry contractor in Ireland, with other big telecom companies expected to follow. The connector will be ready for market rollout in October this year.

CRITICAL REQUIREMENTS IN HIGH-SPEED SIGNAL GENERATION APPLICATIONS

By Clarence Mayott, Applications Engineer, Mixed Signal Products, Linear Technology

In high-speed signal generation applications bandwidth and resolution are the critical requirements. Modern signal generation applications use high-speed digital-to-analog converters (DACs) to produce various types of waveforms, from single tones to complex multichannel waveforms with several hundred megahertz of bandwidth. Such applications demand high-speed DACs that are fast enough to produce these waveforms without sacrificing analog performance. In many signal generation applications phase noise will limit the number of channels and the spacing of the channels that are possible.

Phase noise is traditionally set by the clock that is driving the DAC clock inputs, but any phase noise added by the DAC will show up in the output spectrum and can limit the signals that are possible to generate. The ideal DAC for any general purpose signal generation application should be as fast as possible, with low noise, high linearity and very low additive phase noise. If any one of these specifications is lacking, then the generated waveform will not be adequate to meet the application's needs.

Bandwidth

In any signal generation application the most important design aspect is bandwidth. The designer may need a certain amount of bandwidth for a particular signaling protocol or for a particular application. The bandwidth required can only be generated with a DAC that is at least twice as fast as the bandwidth of interest. This relationship between bandwidth and sample rate (f_s) was defined by Harry Nyquist and describes how signals behave in sampled systems.

While it is possible to generate a signal that spans from DC to the $f_s/2$, it is often not practical to do so due to the images of the generated signal that appear in the output spectrum. In practice, reconstruction filters are required to attenuate any images of the generated signal that may appear in the output spectrum. Even if the generated signal does not extend up to $f_s/2$ but closely approaches it, the images will be difficult to filter out due to constraints on the filter. The closer the bandwidth of the signal is to $f_s/2$ the higher order the filter must be to attenuate the images produced by the sampling process. This higher order filter requires more components, and will have more insertion loss and passband ripple.

By using a DAC with a faster sample rate, the usable bandwidth will increase, which will ease the requirements of the filter. The LTC2000, which is a high performance, 16-bit, 2.5Gsps high-speed DAC, for example, has a sample rate of 2.5Gsps, so the $f_s/2$ frequency is 1.25GHz. Thus, for a signal bandwidth of 800MHz there will be an image of the signal beginning at 1.7GHz. There will be 900MHz between the frequency band of interest and the image frequency. With 900MHz of guard band the image can easily be filtered out with a simple low-pass filter.

Another issue with generating a signal that extends out to $f_s/2$ is that with any DAC there will be a SINC (sin(x)/x) roll-off that will attenuate the generated signal as the frequency increases. For practical applications, about 60% of the Nyquist zone (DC to $f_s/2$) can be used without much SINC attenuation. If 0dB is the signal level at DC, then at 60% of Nyquist the signal level would be down by 6dB. Using a higher speed DAC will reduce the roll-off of the SINC function as the output frequency of the DAC increases.

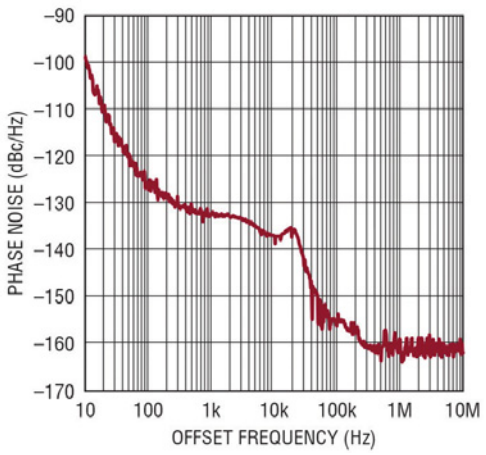


Figure 1: LTC2000 and LTC6946 phase noise F_{out} = 80MHz

Phase Noise

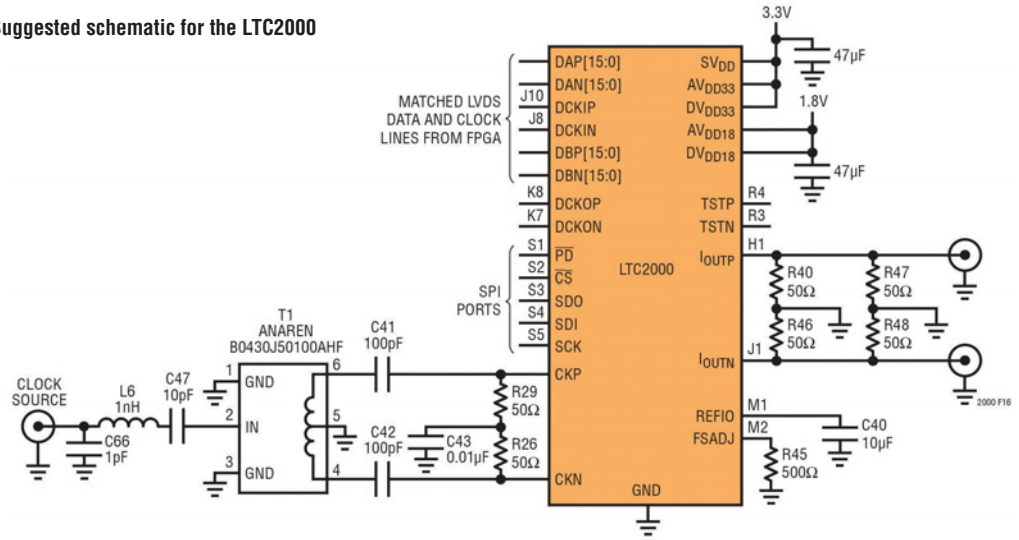
Another important consideration in signal generation applications is the phase noise of the output. The phase noise that is present on the output signals limits how closely the signals can be spaced and can limit the order of modulation that is possible to produce. The more phase noise that is added in the signal generation process the higher the bit error rate of the generated signal will be. If there are several tones closely spaced, the SNR of a tone can be degraded by the spectral leakage of its neighbors, which will reduce the bit error rate of the signal. This loss of signal integrity can be avoided by reducing the phase noise introduced into the generated signal.

A low phase noise clock will transpose less phase noise onto the generated signal. The LTC6946 is a frequency synthesizer that can produce signals from 370MHz up to 5.7GHz. When the LTC6946 is used to drive the LTC2000 high-speed DAC, the resulting phase noise is low enough for most demanding signal generation applications.

Figure 1 shows a plot of the phase noise of the LTC6946 and the LTC2000. The LTC2000 has an additive of -165dBc/rHz at a 1MHz offset when producing a 65MHz output tone. This ensures the phase noise of the clock will dominate the additive phase noise of the LTC2000 itself.

To avoid other noise degrading the output signals, care should be taken to use proper layout techniques in the analog output section.

Figure 2: Suggested schematic for the LTC2000



Proper RF Layout

The benefit of using high-performance DACs and clock sources will erode if proper design and layout rules are not used. Without proper symmetry, bypassing and barriers, the generated analog output waveform can be corrupted and noise and other spurs can be introduced.

Figure 2 shows a typical schematic for the LTC2000. The LTC2000 has a noise spectral density that is better than 158dBm/rHz for signals up to 500MHz, which keeps the signal-to-noise ratio high for a wide range of generated frequencies. It also has a spurious free dynamic range (SFDR) better than 68dB SFDR for output frequencies up to 1GHz.

The outputs from the DAC should be routed as symmetrically as possible. Any asymmetry in the output network can result in a voltage differential between the differential signals. This voltage differential will result in a common mode disturbance that will produce unwanted distortion and noise in the output spectrum.

Protecting the analog outputs from offensive signals can be achieved with symmetrically placed vias, along with good layout practices. Signal generation DACs have three ports that present layout challenges: the clock input, the analog output and the data inputs. If the data input is routed close to the output or the clock, it will couple into those signals, causing spurs to appear in the output spectrum. Likewise, if the clock couples into the analog output through poor layout, it will degrade the integrity of the generated signal.

Maximum DAC performance will be achieved by designing the board with proper barriers between the digital section, the clock signals and the analog output section. It is often appropriate to route digital signals, clock signals and the analog outputs on separate layers of the circuit board to minimize interaction between the signals.

Figure 3 shows the layout of the LTC2000, indicating how to isolate the digital signals, the clock and the analog outputs. In the figure the digital traces are routed on an interior layer of the board and only emerge through vias in the pads of the LTC2000. The clock trace is kept very short, is surrounded by vias to isolate the signal and is not routed by the digital traces or analog outputs. The output traces are kept as symmetrical as possible, and are surrounded by barriers which protect the analog outputs from offensive signals. With these layout guidelines and a clean sample clock, the LTC6946 and the LTC2000 will produce exceptionally clean waveforms that are suitable for most demanding signal generation applications.

Conclusion

Signal generation applications require high sample rates to push the images out further in frequency and reduce the complexity of the output filter. The high sample rate reduces the unavoidable SINC roll-off present in all DACs. Signal generation applications require clean, low phase noise sample clocks to allow for close spacing between adjacent tones. The LTC2000, clocked by the LTC6946, has excellent phase noise performance. With a proper layout and barriers around the critical signals of the LTC2000, the noise and spectral performance are ideal for most demanding signal generation applications. This allows signals to be generated without spurious content, requiring only minimal filtering. The LTC2000 has the sample rate and performance required to solve the issues that arise in modern signal generation applications.

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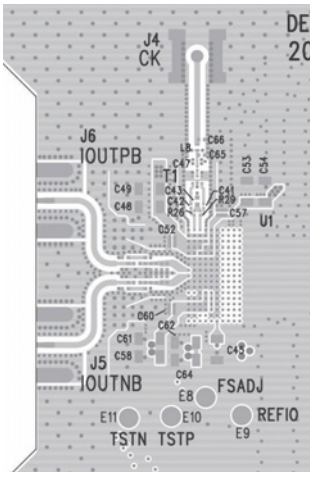

Figure 3: Suggested layout for the LTC2000

Two Clicks are better than one

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

For the past several months I have been working with the MPLAB XPRESS evaluation and Curiosity demonstration boards, interfacing with on-board sensors and actuators or with those on small daughterboards/shields, like the Mikroelektronika Click series. With this Serbian-based company committed to releasing a new Click every week, the portfolio of such little expansion boards has steadily reached a milestone of two hundred (200!) and will certainly have surpassed it by the time you read this.

Equally, my appetite for mikroBUS slots (the standard Click connector) has grown and I have found myself working on a number of versions to hack, share and stack various boards on top of each other to create more complex projects. The need for a second slot is perhaps less acute on the XPRESS evaluation board thanks to the virtual serial port (implemented by the USB programmer/interface chip) that provides an easy way to interact with the user via a standard terminal application. This is missing on the Curiosity board, replaced by an on-board debugger that, in my opinion, is less effective. A serial port can be used to print debugging messages; in fact, this is the oldest form of debugging, but a debugger cannot act as a console and provide a user interface.

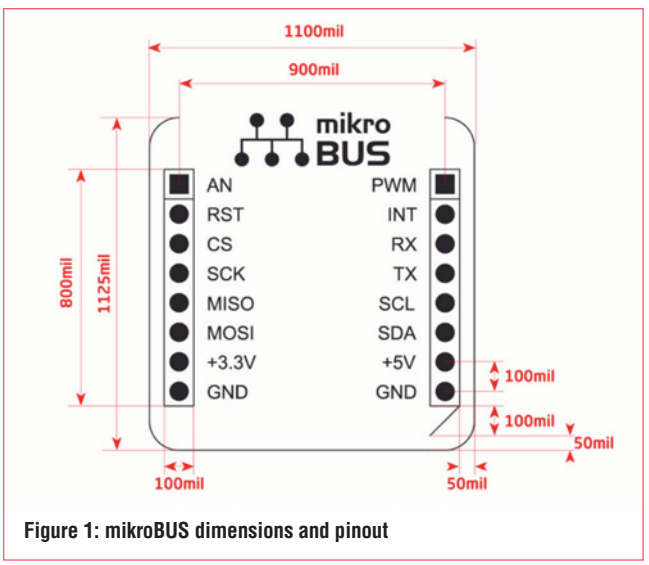

Figure 1: mikroBUS dimensions and pinout

Clearly, much like Arduino shields, Click boards can be stacked if being very careful about overlapping pin usage. A serial-to-USB Click using only the RX/TX pins for example could be mounted on top of an OLED display Click using only the SPI port and a couple of I/Os, and similar combinations are possible.

> Past the initial surprise, I realized this was a kind way of the C compiler to tell me how dumb I was, launching the microcontroller screaming at 48MHz only to have it loop endlessly to blink the LED at 1Hz

Just as I was getting ready to wire up a new prototype of my own, digging for a pre-perforated prototyping board under a stack of old development boards I (re-) discovered Clicker2! A board with same form-factor as the more-famous Mikromedia boards but without the fancy TFT display, it features a pair of mikroBUS slots connected to the pins of a fat PIC18 microcontroller. Bingo!

'Abusing' MCC To Set Up The Project

I have become reliant on MPLAB Code Configurator for all my projects, so I launched MPLAB X and immediately started the New Project wizard. However, my enthusiasm was short-lived as I realized that the PIC18F87J50 featured on the Clicker2 was not supported.

The MCC development team has so far been favouring parts with many core-independent peripherals and this particular PIC18 family has not made the cut – as yet! Nevertheless, I decided to work around it and cheat MPLAB Xpress into believing I was going to develop a project for PIC18F45K50 (with PIC18K devices being more recent and fully supported, featuring a common subset of peripherals).

With the intent of creating a board support package (BSP)

containing all the basic drivers I would need on Clicker2, I started adding an SPI port (MSSP1), an I2C port (MSSP2), a serial port (EUSART1), a timer (TMR2) and a PWM (ECCP1). A few clicks later, I had a fully-configured set of peripherals, ready to generate the code. At the push of a button, MCC did its magic and put all the drivers' source files and requested files in the newly-created *mcc_generated_file* folder.

I then closed the project, saving the MCC configuration (just in case), only to re-open it immediately, but from this point on without MCC. I proceeded to change the target device selection to the proper PIC18F87J50 model and started manually tuning the code. There were three areas that needed my immediate care: pinout definition, configuration bits settings and oscillator settings.

Pinout Definition

Replacing the 80-pin PIC18J with a 40-pin PIC18K model was bound to get all the wrong pin definitions, so I didn't bother setting up any of the I/Os. MCC generated a *pin_manager* file pair (.c/.h) containing just the scaffolding for me to insert the right definitions.

I set off to define a long list of macros (in *pin_manager.h*), following MCC traditional naming conventions, starting with all the GPIOs required to drive the mikroBUS control signals (RST, CS, PWM, INT) for each slot; see Figure 3 for the actual pin assignments for each mikroBUS slot.

I then added a minimum of macros to read the two user buttons (SW1, SW2) and to control the two LEDs on the board.

It took me a (long) while but the exercise was a good reminder of how much tedious work I had been spared by relying on MCC. It was not just the time spent, but the constant eye-crossing, mind-numbing effort required to get all the pins and port assignments right.

See Listing 1 for a few short examples of the resulting work.

```
#ifndef PIN_MANAGER_H
#define PIN_MANAGER_H
...
// mikroBUS slot 1
#define RST1_LAT LATD2
#define RST1_TRIS TRISD2
...
// user buttons definitions
#define SW1_Get() PORTD7
#define SW2_Get() PORTE7
...
// user LED definitions
#define LED1_SetHigh() LATD4=1;
#define LED1_SetLow() LATD4=0;
#define LED1_Set(x) LATD4=x;
#define LED1_Toggle() LATD4=1-LATD4;
```

Listing 1: Pin_manager.h – a snippet

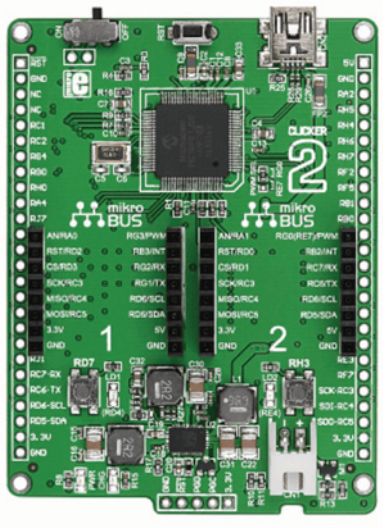

Figure 2: MikroElektronika Clicker2 for PIC18J

The *PIN_MANAGER_Initialize()* function (found in *pin_manager.c*) was much quicker to fix, and involved setting only a small batch of TRIS registers and disabling most/all of the analogue input settings.

Configuration Bits Fixing

For some reason, configuration bits definitions are almost always unique to each family of microcontrollers. MCC always places the list of *pragmas* at the top of the *mcc.c* module so it was easy to edit them out altogether. I used an MPLAB X tool (Window > PIC Memory Views > Configuration Bits) to select the correct values (*enums*) for each of the special configuration options available on this specific model. Then, I cut the output (text) of the tool and pasted it back into the *mcc.c* file.

```
// CONFIG1L
#pragma config WDTEN = OFF // Watchdog Timer
Enable bit (WDT disabled)
#pragma config PLLDIV = 2 // PLL Prescaler Selection bits
#pragma config STVREN = ON // Stack Overflow/
Underflow Reset Enable bit
#pragma config XINST = ON // Extended Instruction Set
Enable bit

// CONFIG1H
#pragma config CPUDIV = OSC1 // CPU System Clock
Postscaler
#pragma config CP0 = OFF // Code Protection bit

// CONFIG2L
#pragma config FOSC = HSPLL // Oscillator Selection bits
#pragma config FCMEN = ON // Fail-Safe Clock Monitor
Enable bit
#pragma config IESO = OFF // Two-Speed Start-up
...
```

Listing 2: Configuration bits pragmas, segment of mcc.c

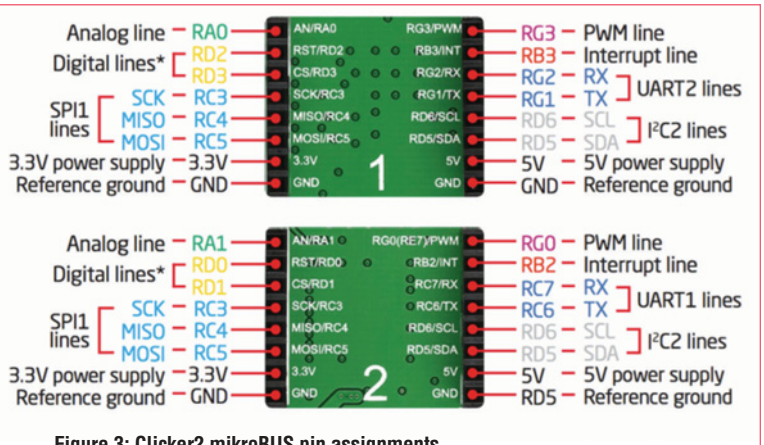

Figure 3: Clicker2 mikroBUS pin assignments

Oscillator Settings

The last parts to need my attention were the oscillator settings, also placed in the mcc.c file as the *OSCILLATOR_Initialize()* function.

The PIC18F87J50 has a full-speed USB interface module but, unlike the newer K50 family models, does not have the auto clock tuning (ACT) feature. It therefore is unable to use its internal oscillator with required accuracy and stability to support USB communication, so an external crystal oscillator must be used instead.

The Clicker2 board provides an 8MHz crystal that can be driven by the HS mode of the PIC external oscillator. This clock signal must be divided by two and fed into the internal PLL circuit, producing the 96MHz clock required for USB full-speed operation. The actual microcontroller core clock is then derived from this relatively fast clock by dividing it by an appropriate amount. Since I wanted to create a generic BSP but not arbitrarily limit the performance of my future applications, I decided for a divider of two (48MHz), which gives the PIC18 an actual instruction execution speed of 12MIPS. In practice, the selection of the proper external oscillator, clock divider and PLL feature was already taken care of by the configuration bits (see above). Eventually, the actual oscillator initialization code turned out to be quite simple, as there seemed to be only a single register (OSCON) to set.

Unbudgeted Learning Time

In theory this was it. The basic Clicker2 board support package was all there, so I decided to go for a test-run. I needed a simple *main()* function to blink the proverbial LED and I typed one fast out of pure habit; see Listing 3.

```
void main(void)
{
 // Initialize the device
 SYSTEM_Initialize();

 while (1)
 {
 LED1_Toggle();
 __delay_ms(500);
 }
```

Listing 3: Blinky, the embedded "Hello World"

What follows when hitting the 'build project' button on MPLAB X is a compressed recount of two additional and completely unbudgeted hours of typical embedded control development/learning time, as follows:

- At first, the built-in compiler macro providing the usual simple *__delay_ms()* blocking delay loop started 'complaining' not being able to take such a large delay amount in one gulp. After some fiddling I figured out that no more than 10ms at a time could be provided. Past the initial surprise, I realized this was a kind way of the C compiler to tell me how dumb I was, launching the microcontroller screaming at 48MHz only to have it loop endlessly to blink the LED at 1Hz. Point taken!
- Once that was fixed (building an additional loop around the 10ms loop, of course), the code compiled. The Clicker2 board brings the USB signals directly to the target PIC18, leaving two options for programming the device: a USB bootloader or an external programmer (a mikroProg or a PICKit3 via a small adapter). I chose the bootloader, which is a clever HID high-side bootloader that uses a protocol common to all Mikroelektronika boards. The advantage of high-side bootloaders is that they don't require the compiler to add any offset to the target application nor any re-direction of the interrupt vectors. It is only the reset vector that is intercepted (automatically) by the loader itself. Moreover, the Mikroelektronika implementation is quite transparent to the unaware end-user as the bootloader entry is purely time-based.
- After a device reset, the bootloader enumerates first as a HID device and awaits a host command for up to five seconds. Failing that, the device disconnects and the (target) application reset vector is launched.
- As it turns out, the Mikrelektronika HID bootloader is a Microsoft-Windows-only application, while I do have a Mac! This is a problem I had solved before, when writing the *"Graphics, Touch, Sound and USB"* book, using Mikromedia boards. I had created a simple Python script for the benefit of all Linux and Mac users (Windows users are welcome, too) and posted it on the Libstok repository. So I dug it up from my hard drive and tried to launch it.
- Fact is, in my laziness, I had covered only the PIC24 programming support, while now I needed the script to access a PIC18 hex file. This required some retouching of the address calculations, which went quickly. (PIC24 hex files differ from PIC18 and PIC32 hex files in the way they map their three-byte word in the memory address space).
- To add to the challenge, it turns out the Python *hidapi* library had changed quite a bit since my first (and last) use. The new revision included fixes for bugs that had previously required some creative workarounds, but also the protocol used to access a device had changed, just slightly. Of course this was barely documented – if at all, so I arrived at the correct sequence by a painful successive approximations process, posting the resulting script on Bitbucket.

Eventually I could program the board and see my Blinky application run – except the LED did not perform as expected!

It's The Little Details

It was blinking at an odd frequency, way too slow.

After much head scratching, I figured that it had to be the PLL failing to latch, or simply not working at all.

Following a very long and careful inspection of the datasheet topic chapters (oscillators, device configuration, electrical specification…), I stumbled into the key passage in the second paragraph of section 2.2.4:

"*The PLL can be enabled in HSPLL, ECPLL, INTOSCPLL and INTOSCPLLO Oscillator modes by setting the PLLEN bit (OSCTUNE<6>).* "

Contrary to my previous understanding, the HSPLL mode selected by the FOSC configuration bit (field) was a necessary but *not a sufficient* condition for the PLL to be enabled.

Hidden as bit 6 of the oscillator tuning register (OSCTUNE) there was the true PLL enable bit and it had to be set at run time.

OSCTUNEbits.PLLEN = 1;

The fix required only one line of code to be added to the *OSCILLATOR_Initialize()* function in mcc.c, but this painful experience reminded me once more how precious can be the service provided by code generation tools such as MCC. This, in fact, is exactly the kind of minute detail that we are sure to fail to notice or simply forget about when using a PIC18F87J50. Machines are good at repetitive tasks, and once such a detail is inserted into their databases, there is no forgetting!

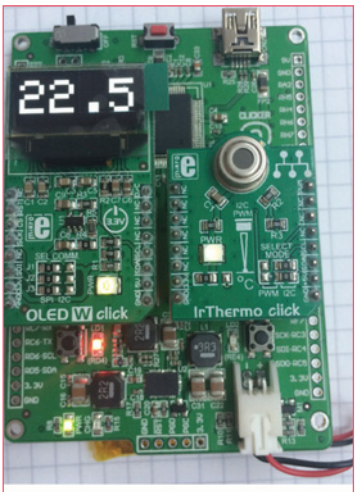

Figure 4: IrThermometer

Two Clicks At Work

With the confidence provided by Blinky, now successfully running at 1Hz, I finally set off to exercise two Click boards at once. The first use that came to mind was to combine the IrThermo Click, an infrared temperature sensor, with the OLED-W (display) Click to produce a small portable and accurate Ir Thermometer. I installed the OLED-W click in slot 1 and copied over the additional driver files (oled.c, oled.h)

I had developed and shared recently as an example project for the XPRESS board. This display board uses (by default) the SPI port and three GPIOs.

I then installed the IrThermo Click in slot 2 and copied over the SMBus read routine that I had developed for an EMC1001 sensor (featured in last month's column), taking care to modify the address to match that of the IR sensor, but also reading a 16-bit register value and converting it directly to a proper reading in degrees Celsius as illustrated in Listing 4.

```
bool IR_SensorRead(uint8_t reg, float * pTemp)
{
 int16_t data;
 I2C_MESSAGE_STATUS status = I2C_MESSAGE_
PENDING;
 static I2C_TRANSACTION_REQUEST_BLOCK trb[2];

 I2C_MasterWriteTRBBuild(&trb[0], &reg, 1, IR_
THERMO_ADDRESS);
 I2C_MasterReadTRBBuild(&trb[1], (uint8_t*)&data, 2,
IR_THERMO_ADDRESS);
 I2C_MasterTRBInsert(2, &trb[0], &status);

 while(status == I2C_MESSAGE_PENDING); // blocking
 *pTemp = ((float)(data) * 0.02) - 273.15; // convert to
deg C

 return (status == I2C_MESSAGE_COMPLETE);
}
```

Listing 4: SMB reading a 16-bit register value and converting it to degrees C

In 10 Lines Of Code – Or A Couple More

Finally, Listing 5 shows the complete application that ended up requiring just a few more lines of code.

```
void main(void)
{
 SYSTEM_Initialize();
 INTERRUPT_GlobalInterruptEnable();
 INTERRUPT_PeripheralInterruptEnable();
 OLED_Initialize();

 OLED_Clear();
 OLED_SetScale(4,4);
 while (1)
 {
 char s[6];
 float temp1, temp2;
 IR_SensorRead(OBJ_TEMP, &temp1);
 //IR_SensorRead(AMB_TEMP, &temp2);
 sprintf(s, "%2.1f", temp1);
 OLED_Puts(0,0, s);
 delay_ms(1000);
 }
}
```

Listing 5: An IR thermometer with OLED display

Figure 4 shows a view of the resulting prototype in action. Notice that the Clicker2 board also provides a connector for a Li-Ion battery (a regulator and charger circuit are included as well), making it a perfect solution for many portable, self-contained demos and makers projects.

Eventually the Clicker2 board met my wish for access to more sensors and actuators. The experience of writing its small BSP helped me understand how spoiled I had become relying on MPLAB Code Configurator for my routine project start and development needs. I am also quite happy with the newly-improved HID bootloader, although I know I will be missing the convenience of the virtual serial port provided on XPRESS and its drag-and-drop programmer. The next question is, how long before I might need a third or even a fourth slot? Stay tuned. ●

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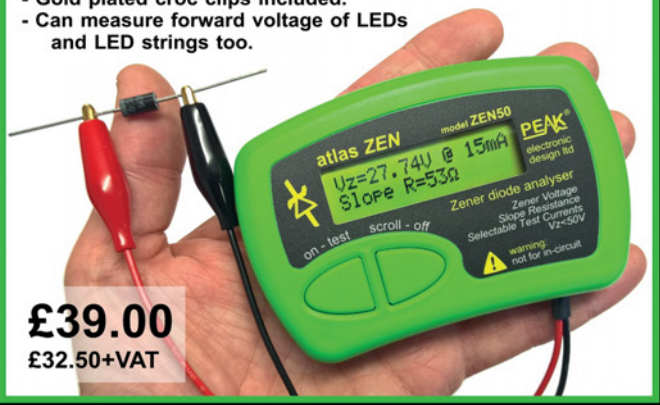

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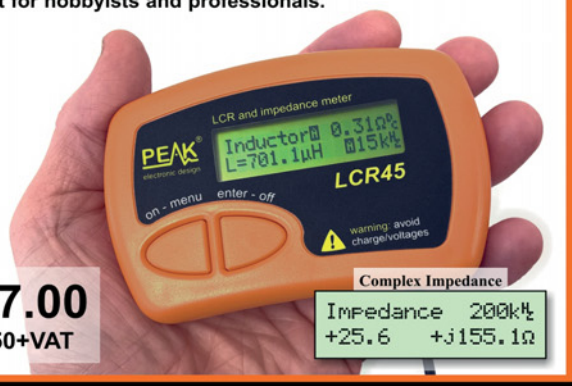

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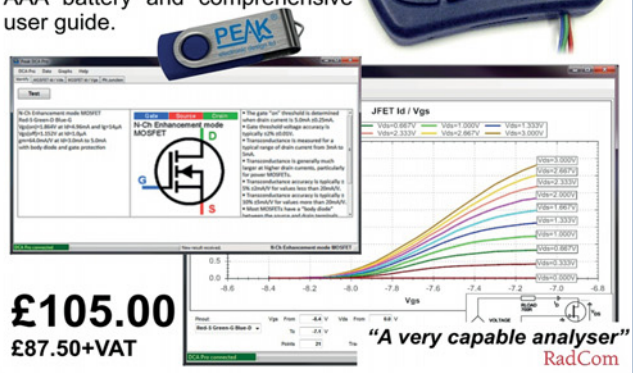

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Force sensors in embedded applications

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

Force sensors are found in many instrumentation applications such as robotics, domestic, commercial and industrial equipment, games, transportation safety systems, and others. Accurate and reliable measurement of force is important, especially in safety-critical systems, and it is necessary to use the correct measurement techniques to achieve solid results.

A force measurement system consists of a force sensor and associated instrumentation, and possibly a display to show the measured value. The force sensor produces electrical voltage or current related to the measured force. The instrumentation can be a simple dial gauge or a microcontroller-based system with memory and associated ADCs and DACs. The display can be a simple meter or a complex device such as an LCD.

Force Sensor Choices

There are many types of force transducers with varying complexities and costs that can be used in embedded applications. In designing a force measurement system it is vital that the accuracy required and overall cost are known or can be estimated in advance.

Most force sensors employ some kind of elastic load-bearing element which the application of even a very small force causes to deflect. This deflection is then converted into an electrical signal which is the output of the sensor. These types of force sensors are used to measure small-to-medium-level forces in the range 0.01N-50MN.

Piezoelectric is another type of force sensor where the sensor generates an electric charge proportional to the force applied to the surface of the piezoelectric material. This sensor's advantage is it can measure very small forces (e.g. 1.5mN), as well as very

Figure 1: Load cell working principle of a Loadstar sensor

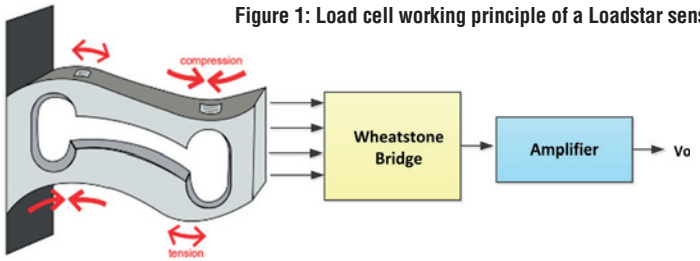


Figure 2: Force sensing resistors

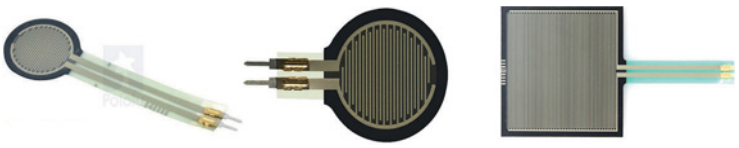


Figure 3: Block diagram of the designed system

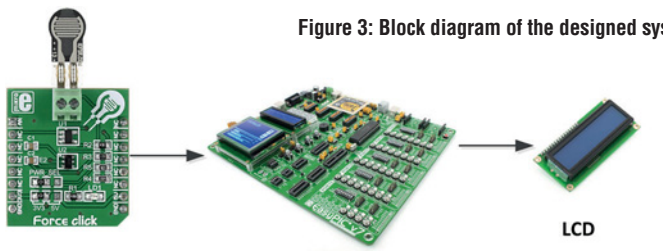
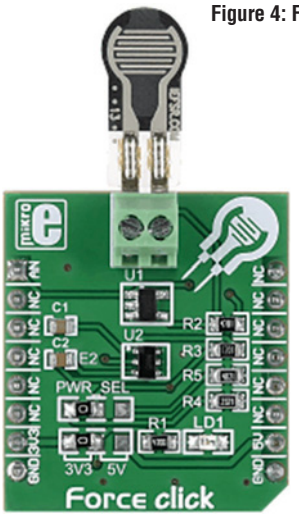


Figure 4: Force Click board



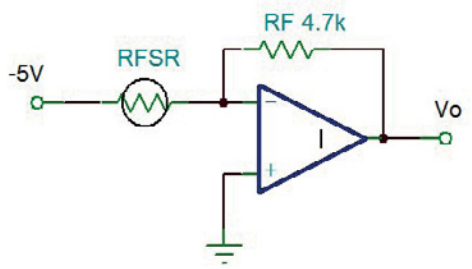


Figure 5: Circuit diagram of the Force Click board

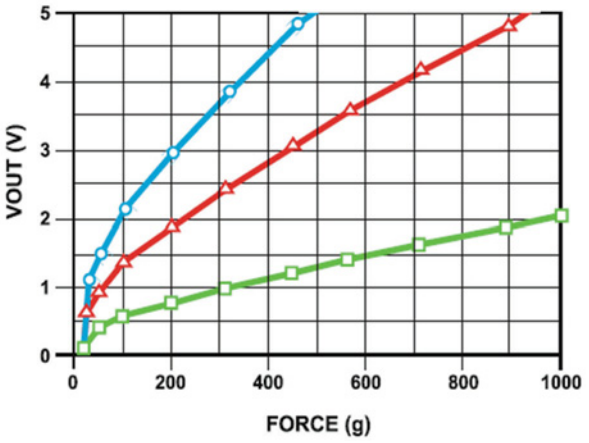


Figure 6: Output voltage versus applied force

high forces (e.g. up to 120MN). Hydraulic, pneumatic, capacitive and magnetic-based force sensors are also in common use, although they not as accurate as the elastic or piezoelectric sensors.

Strain Gauge Load Cells

Load cells are one of the most commonly used low-cost force sensors. A load cell is made up of an elastic material which is strong but highly repeatable. A number of strain gauges are attached to different parts of the load cell. An example load cell is shown in Figure 1, with two strain gauges at the top and two at the bottom. When force is applied on top of the cell, the elastic material deflects, causing the two top strain gauges to compress and the two on the bottom to stretch, or tense.

A Wheatstone bridge circuit is commonly used to produce a voltage when the load cell is deflected. The strain gauges are connected to the arms of a Wheatstone bridge. Normally the bridge is in balance and the output voltage is zero when no force is applied. When force is applied to the load cell, the resistance of one or more arms of the bridge change, causing the bridge to be unbalanced and produce a voltage. This voltage is usually very small (tens of millivolts) and is amplified to obtain a large enough voltage to measure accurately, or can be converted into digital form using an ADC. The resulting output voltage is calibrated and linearized to be directly proportional to the applied force.

Force Sensing Resistors

Force sensing resistors (FSRs) are used in applications where low cost and imprecise measurement of force is sufficient, commonly found in touch control devices. These are polymer thick film resistors (see Figure 2) whose resistances decrease in relation to the applied force.

FSRs are available in various sizes and shapes, and are flexible to fit the geometry of the application. Their sensitivity range is from 10g to over 50kg. Because FSRs have resistive characteristics, they are easily used in voltage or current divider circuits so that the output voltage or current changes when a force is applied on the sensor.

FSRs are also used in standard inverting or non-inverting operational amplifier circuits, either at the inputs or in the feedback loops. When used in inverting amplifier configurations the amplifier output voltage is linearly proportional to the change in the FSR resistance and hence the applied force. FSRs are low cost, lightweight, flexible, easy to use and durable.

Example Force Measurement System

This section covers an example of a microcontroller-based force measurement system (Figure 3), complete with hardware and software details. It consists of a Force Click board, an EasyPIC V7 microcontroller development board and a 2x16 character LCD.

Force Click (Figure 4) is a small mikroBUS compatible board (www.mikroe.com), which uses the Interlink FSR400 type circular force sensitive resistor as its sensor element. The board's basic features are screw terminal connection of the FSR, 3.3V or 5V operation, 0.2-20N force sensitivity range and a rise time of less than 3µs.

The Force Click board contains an on-board single-ended operational amplifier and a negative voltage converter chip. As shown in Figure 5, the op-amp is operated in standard negative feedback configuration as a current-to-voltage converter, where the FSR is connected to its negative terminal and a 4.7K resistor is used in the feedback loop. The board operates from a +5V supply derived from the development board. The other end of the FSR is connected to a -5V voltage using the ADM8828 switched capacitor voltage inverter chip. The output voltage of the board is therefore positive and is given by:

$$\mathbf{Vo = 5*R_G / R_{FSR}}$$

where R_G is the feedback resistor and R_{FSR} the resistance of the FSR sensor.

The relationship between the applied force and output voltage of the operational amplifier is shown in Figure 6. The red trace is

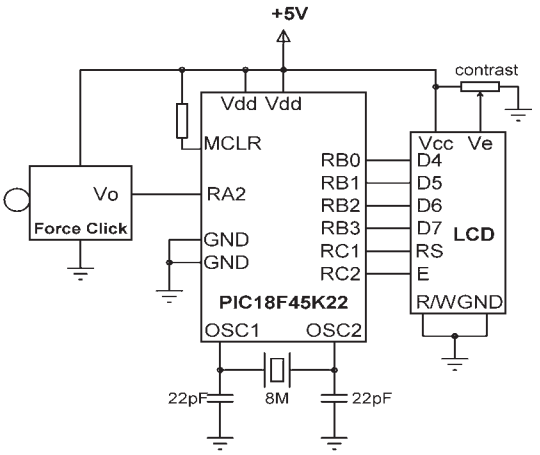


Figure 7: Circuit diagram of the force measurement system

the response when the feedback resistor R_G = 4.7K (see the Force Sensing Resistor Integration Guide, www.interlinkelectronics.com). Although the graph is non-linear for small forces, in this article for simplicity it is assumed to be linear. The relationship between the output voltage V_o and the applied force F (in g) is approximately given by (calibration of the system is required for accurate results):

$$V_o = 0.0042F + 1.15$$

The applied force is then determined with:

$$F = (V_o - 1.15) / 0.0042$$

Figure 7 shows the circuit diagram of our force measurement system. The EasyPIC V7 microcontroller development board is based on the medium-performance PIC18F45K22 microcontroller, operating with an 8MHz crystal. The on-board microcontroller is programmed via the mikroICD programmer interface from a PC.

This board has two mikroBUS sockets where the Force Click board is connected to socket 1. With this interface, the output of the Force Click board is connected to pin RA2 of the microcontroller. A standard 16x2-character text-based LCD is connected to PORTB of the microcontroller.

The Software

The mikroC Pro for PIC language and IDE are used in this design, consisting of a fully integrated C-language-based development environment that also includes a simulator and a hardware debugger. mikroC is one of the popular microcontroller system development languages, rich with many library functions, including support for advanced peripherals such as CAN bus, USB, SD card, SPI, I2C, UART, LCD and many others.

Listing 1 shows the complete program. The interface between LCD and microcontroller is defined at the start. Inside the main program PORTA is configured as an analogue input port, PORTB as a digital output port, and the LCD module initialized. The remainder of the program is executed in an endless loop, where the output voltage of the Force Click board is read and converted into voltage. The applied force is then determined as a floating point value by using the equations in this article. The program converts the force into text form and displays it on the LCD. The above process is repeated continuously at one-second intervals. ●

```
// LCD interface
sbit LCD_RS at RB4_bit;
sbit LCD_EN at RB5_bit;
sbit LCD_D4 at RB0_bit;
sbit LCD_D5 at RB1_bit;
sbit LCD_D6 at RB2_bit;
sbit LCD_D7 at RB3_bit;

sbit LCD_RS_Direction at TRISB4_bit;
sbit LCD_EN_Direction at TRISB5_bit;
sbit LCD_D4_Direction at TRISB0_bit;
sbit LCD_D5_Direction at TRISB1_bit;
sbit LCD_D6_Direction at TRISB2_bit;
sbit LCD_D7_Direction at TRISB3_bit;
// End LCD interface

void main()
{
 unsigned int temp;
 float V, Force;
 unsigned char Txt[14];

 ANSELA = 4;    // RA2 is analog
 ANSELB = 0;    // PORTB is digital
 TRISA2_bit = 1;            // RA2 is input
 LCD_Init();     // Initialise LCD
 LCD_Out(1,1,"Force");  // Display heading
 Delay_Ms(2000);          // Wait 2 seconds

 while(1)          // Do forever
 {
 temp = ADC_Read(2);   // Read force
 V = temp*5.0/1024.0; // Convert to voltage
 Force = (V - 1.15) / 0.0042;          // Calculate force
 if(Force < 0)Force = 0;
 FloatToStr(Force, Txt);               // Convert to string
 Ltrim(Txt);      // Remove leading spaces
 Lcd_Cmd(_LCD_CLEAR); // Clear LCD
 Lcd_Out(1,1,Txt);          // Display heading in degrees
 Delay_Ms(500);          // Wait 0.5 second
 }
}
```

Listing 1: The program

Understanding A Chip's Age

BY **OLIVER KING**, CHIEF TECHNOLOGY OFFICER OF MOORTEC

Semiconductor devices age over time, we all know, but what is often not well understood are the mechanisms behind it or the factors that cause a chip to fail. In addition, there is also a requirement for a minimum lifetime of a device, which largely depends on the application. For example, this could be two or three years for a consumer device and up to twenty-five years for a telecommunications device.

If that ageing process is better understood or better still monitored, then chip over-design can be reduced and we can potentially even create chips that react and adjust for the ageing effect or self-predict when they might fail.

The Mechanisms Of Ageing

There are a number of mechanisms that contribute to a chip's ageing process, the most notable ones being electromigration, hot carrier effects and bias temperature instability (BTI). Whilst some of these can be mitigated through design techniques, especially when involving dedicated CAD tools, these efforts can only go so far.

In the case of BTI, the mechanisms are not fully known. Whilst traditionally only negative bias temperature instability (NBTI) was considered an issue, now, with the introduction of high-k metal gates at 28nm, positive bias temperature instability (PBTI) is a problem too.

The result of BTI is to raise threshold voltages, and the effect is a close temperature dependency, so without a good model of device use, it is hard to predict and design for. In addition, by their nature ageing effects are hard to measure, because it takes a long time to get a device to end of life, even when using acceleration techniques such as high-temperature operating life (HTOL).

Ageing is complex and very dependent on the application and operating environment. In most modern applications neither of those is well known and often varies with time.

If we take the smartphone as an example, there will be modes when it is doing very little – the clock frequency is low and so is its power use. But, at the other extreme, the phone will be playing HD video, where the clock runs at high rates and the power demand will be correspondingly high. Obviously, if the device is mostly in low power state, it would age at a significantly lower rate than if in high power state. The trouble is, at the design stages a designer does not know what that ratio will be.

This is a rather simplified example because more often than not there will be more than two states, and the designer needs to make assumptions about time spent in each state and build in margins to cope with the unknowns.

Predicting Device Lifetime

There are on-chip monitors available that measure the ageing process of a device in the field. By having reference structures in addition to live structures, the two can be compared over time. Such applications are already in use today, alongside information of how to adjust the supply to bring the chip back to its required performance level.

By allowing the system to monitor ageing, potentially the dynamic voltage and frequency scaling (DVFS) schemes can be optimized too, helping predict chip and device lifetimes or perhaps even reign in certain modes to insure a particular lifetime goal is met. ●

IMPLEMENTING A CLASS D AUDIO AMPLIFIER

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Class D amplifiers have become popular as audio amplifier topology due to their high efficiency and low cost. The high-current output stage uses binary switches, resulting in low heat generation and power loss, allowing for smaller power supply, heat sink and overall physical size of the amplifier.

The typical efficiency of a class D amplifier is more than 90%, as opposed to 50% for a typical class AB amplifier. In an AB design, most of the inefficiency is a result of the output stage devices being required to operate in the linear region. As current flows though the devices, it is converted to heat instead of being delivered to the load.

A single-channel, full-bridge, push-pull class D amplifier can be made using only the analog features of a 16-bit microcontroller and a few external components, leaving the processor available for other applications.

Class D Topology

A class D audio amplifier is essentially a pulse width modulation (PWM) amplifier. The input audio signal is used as modulation reference for a PWM carrier. The resulting PWM signal drives a higher power output stage, and is filtered to recover the amplified audio. As Figure 1 shows, there are four main functions in such a device: triangle waveform generator, audio modulation comparator, switch controller and output stage, and lowpass filter.

Using a comparator, the analog audio signal is first compared with a high-frequency triangle wave to create a pulse waveform that is directly proportional to the instantaneous values of the audio signal, resulting in a digital representation that can drive the output devices, but only in on and off states. Additional logic produces the inverse of the digital signal to drive the complementary switch pair.

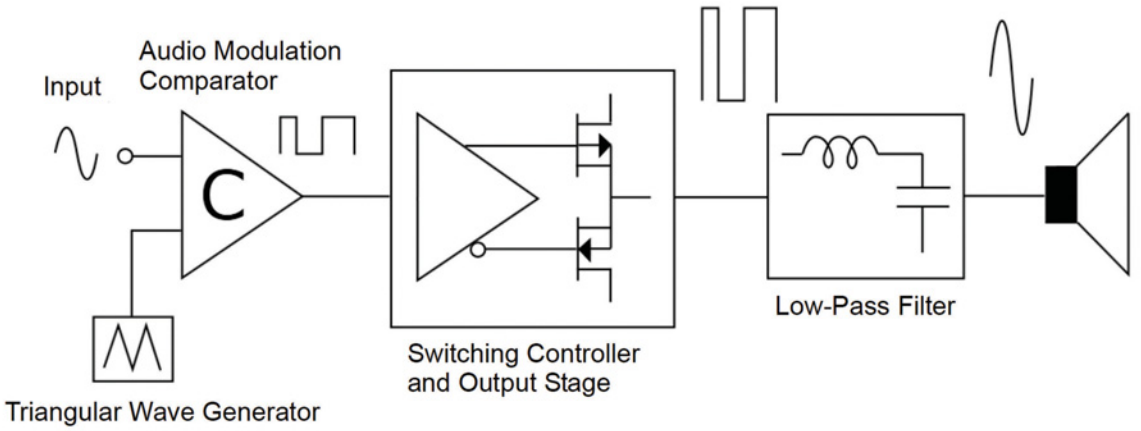
Next, a switch controller provides signal timing and gate drive voltages for the output devices. The output switches provide voltage gain proportional to the supply voltage and high current capability to drive the speaker coil. Finally, a lowpass filter removes the carrier frequency and recreates the analog audio signal.

Analog Input

The incoming audio signal needs to be conditioned and filtered before it is compared with the triangle wave. A lowpass filter can prevent aliasing, and the level should be limited to below that of the triangle wave. The amplitude of the audio signal may need to be attenuated or amplified to match that of the comparator supplies and triangle wave amplitude.

To improve signal-to-noise ratio, the peak level audio input should be as close to system full scale as possible. Depending on the application and loudspeaker to be driven, it may be beneficial to band limit the input signal. For example, if a small speaker is used that cannot produce tones below 100Hz, the input should

Figure 1: Block diagram of a class D amplifier



be highpass-filtered to reduce wasted energy and possible speaker damage.

Power Supply

A stable DC power supply is important as it plays a critical role in the performance of the amplifier, including gain, THD and noise. Class D amplifiers have little or no power supply noise rejection; any noise or voltage drops from loading will be passed on to the output.

Due to the digital nature of the class D design, the power supply has to deliver large current transients each time the output devices switch. The power supply can also be affected by the energy storage elements in the lowpass filter and loudspeaker coil.

Output Stage

Using a full bridge output stage, as shown in Figure 2, reduces the power supply's effect on performance degradation and can be implemented with a single rail design.

Some dead time is needed to prevent damaging current flow though the switches. Dead time is a delay in driving a switch high due to the capacitive settling effects of the output switch. This prevents both switches from being closed at the same time, effectively shorting V+ to GND.

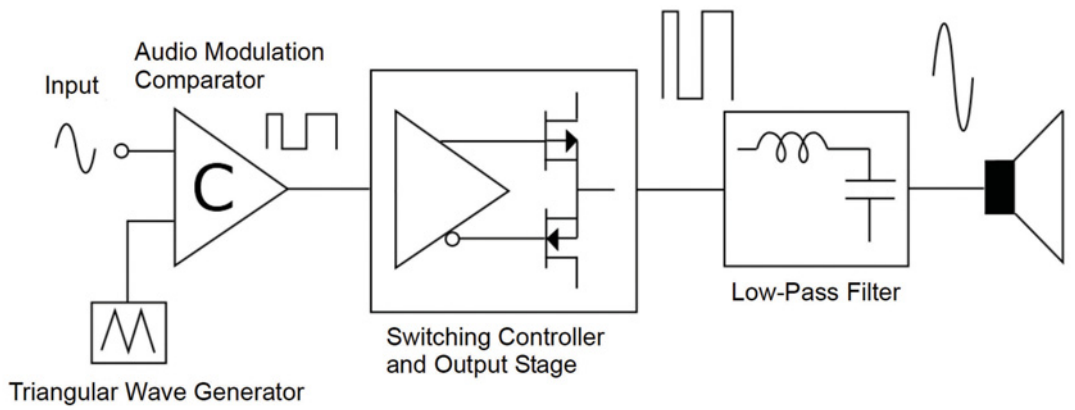
The amount of dead time depends on the switch's on-off delay, and will affect THD. A full-bridge topology has reduced offset and THD compared with a half bridge, and can be implemented without a feedback circuit. When idle, the PWM duty cycle is 50% and the average voltage on both ends of the speaker coil is V+/2.

Output Filter

A typical class D output filter is a second order L-C lowpass filter with no resistive components to waste power. The filter cutoff frequency should be at least four times lower than the switching frequency of the triangle generator. The application's speaker nominal impedance will guide the initial values of the inductors and capacitors. However, the speaker coil's own inductance and capacitance also interact with the filter elements and should be considered in the design.

The power level of the amplifier and resulting current delivered though the filter guides the power rating of the filter elements. Lastly, some designs may have restrictions on

Figure 2: Full-bridge output circuit diagram



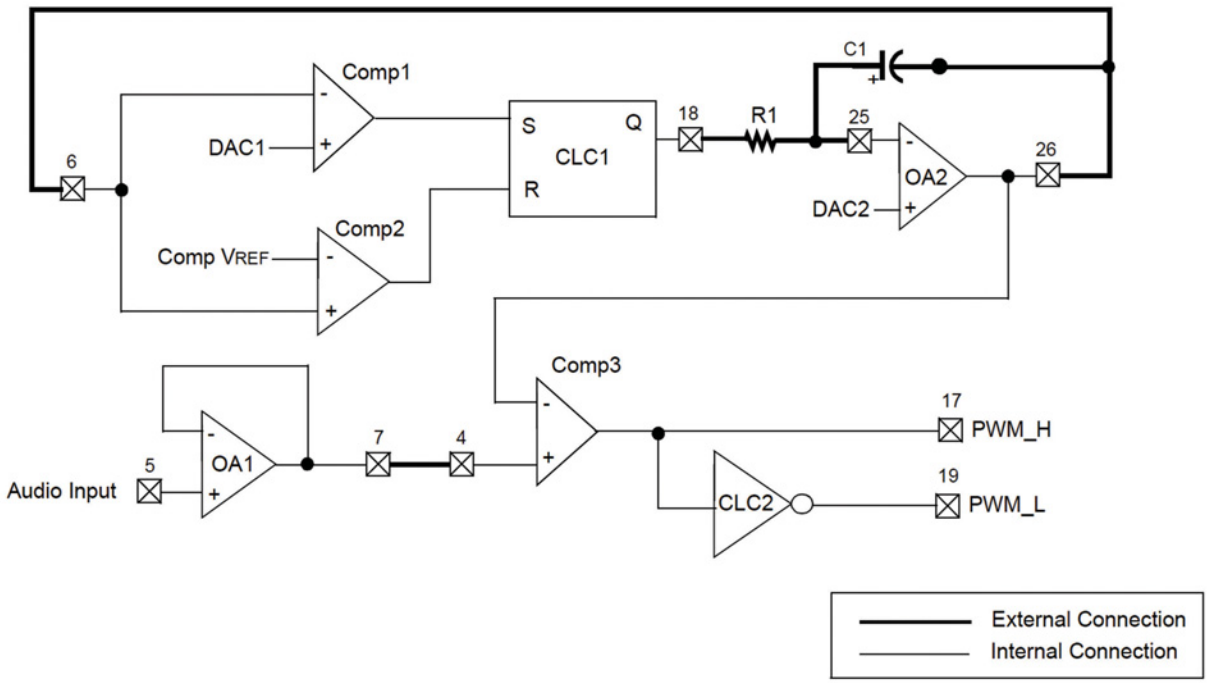


Figure 3: Peripheral connections for the PIC24FV16KM202 microcontroller

radiated emissions (EMI). The filter design, physical location and trace routing need to be considered for best performance.

Implementation

A 16-bit microcontroller, such as the PIC24FV16KM202 from Microchip, can have a wide range of analog and digital peripherals for creating an analog class D amplifier. The KM device also has configurable internal connections between the peripherals that reduce external PCB routing and free up IO pins for other uses. The FV variant of the family was chosen for its 5V operation, improving the signal-to-noise ratio of the system. Figure 3 shows the peripherals and connections used for the amplifier.

Op-amp OA1 is a buffer for the incoming audio signal. The triangle generator uses a pair of comparators, a configurable logic cell (CLC) module set up as an SR latch, and an op-amp configured as an integrator. The comparators are wired as a windowed comparator, with thresholds set by DAC1 and the comparator voltage reference. The windowed comparator's output is then converted to a square wave using the SR latch and, finally, a triangle wave via the integration function of OA1. The triangle wave is fed back to the window comparator completing the self-resonator circuit.

Comparator Comp3 creates the pulse waveform by comparing the triangle waveform with the audio input. CLC2 configured as an inverter provides the complement signal for the full-bridge topology.

Three comparators are used in the design. Comparators Comp1 and Comp2 function as windowed comparators using the comparator voltage reference and DAC1 to set the voltage threshold levels. Comparator Comp3 compares the audio signal with the triangle wave to create the digital PWM signal.

OA1 acts as a buffer for the incoming analog audio signal. It is set up as a voltage follower using the selectable internal connection from the output to the inverting input. Optionally, OA1 can be set up as a filter with or without gain. OA2 is used in the triangle generator as an integrator, with its output fed back to the window comparator to create an oscillator.

The digital-to-analog converters (DACs) are used in a static state to provide a programmable DC voltage level for the triangle generator. DAC1 is internally connected to Comp1's non-inverting input as the upper voltage threshold of the window comparator. DAC2 is internally connected to OA2's non-inverting input and used to set the DC bias level at 2.5V (V+/2).

The CLCs provide digital logic for the triangle wave generator and digital output. CLC1 is configured as an RS flip-flop to create a single square wave from the window comparator's outputs. CLC1's inputs are internally connected to the comparator outputs. CLC2 is set up as an inverter to create a complementary PWM signal for the low side switches.

Advantages

The microcontroller's wide range of analog and digital peripherals allows it to be used to create a complete class D amplifier. The internal connections between peripherals reduce the pin count needed for implementation, leaving the IO pins available for other uses.

Using the peripherals instead of discrete components to realize a Class D design reduces PCB area and overall cost. ●

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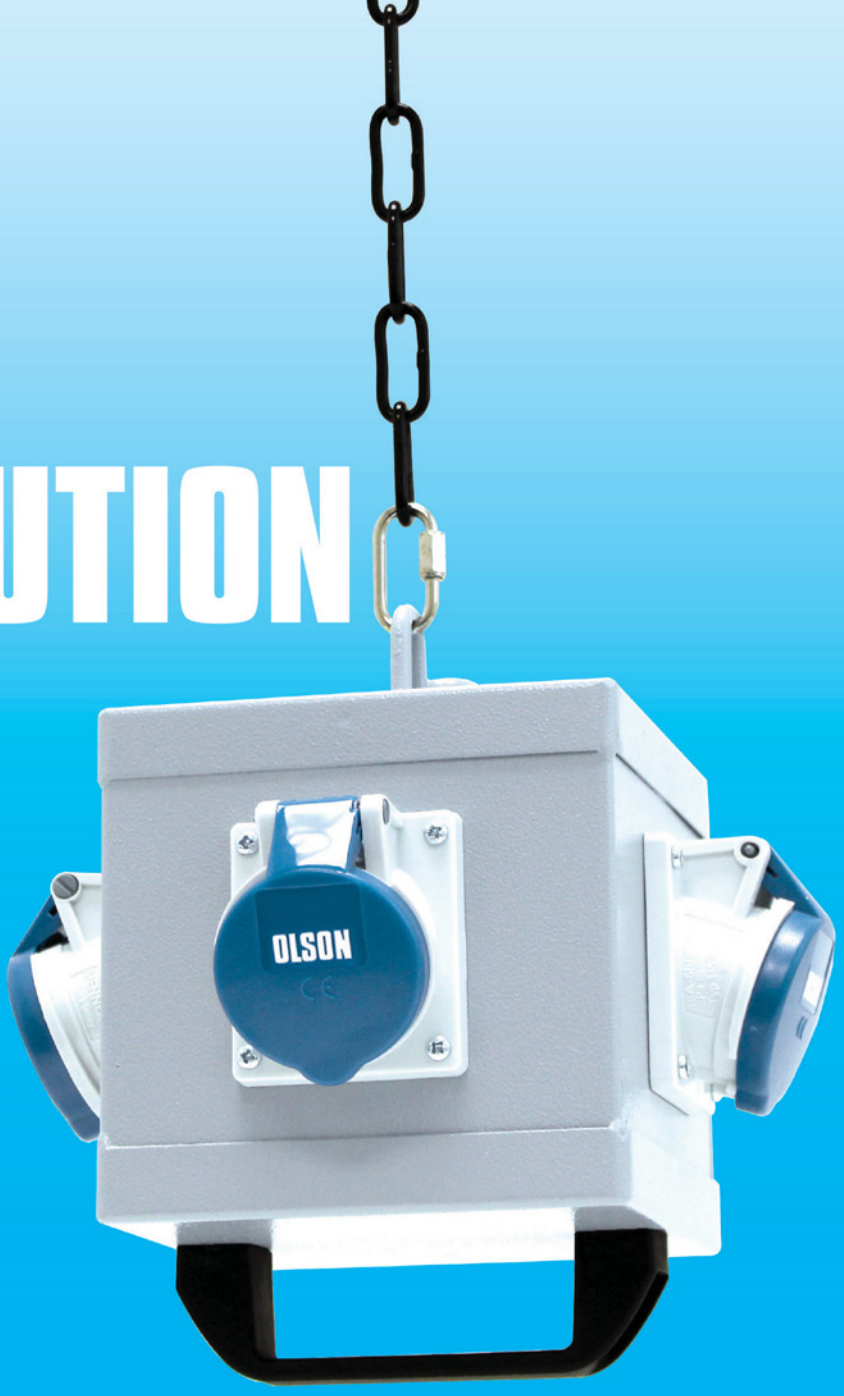

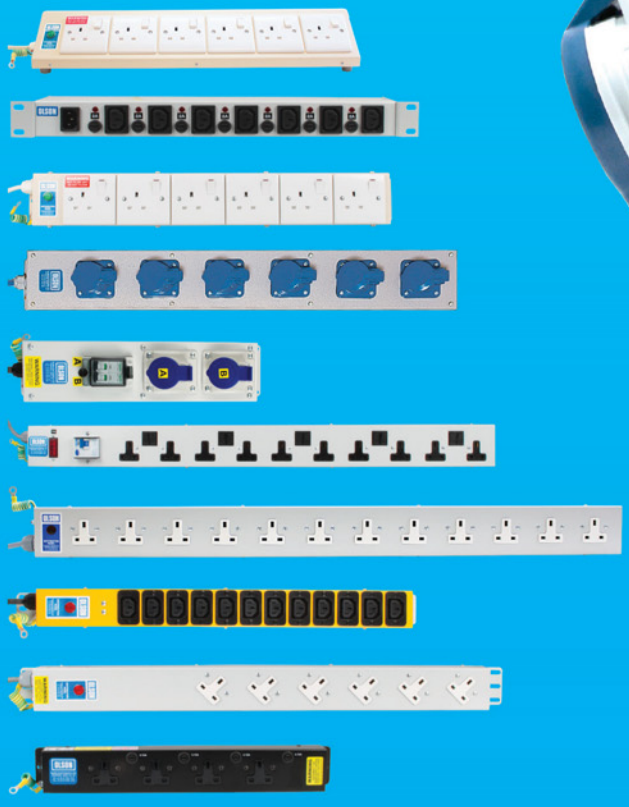

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555-TIMER-BASED ANALOG TIME-TO-VOLTAGE CONVERTER

MUHAMMAD TAHER ABUELMA'ATTI FROM THE KING FAHD UNIVERSITY OF PETROLEUM AND MINERALS IN SAUDI ARABIA PRESENTS A SIMPLE ANALOG TIME-TO-VOLTAGE CONVERTER, USING OFF-THE-SHELF COMPONENTS

Measurement of time intervals between two physical events is widely used in many instrumentation, control and communication applications, which fuels the continuous development of electronic circuits for time-to-voltage converters (TVCs) and time-to-digital converters (TDCs). In fact, a TDC can be easily built around a TVC followed by an analog-to-digital converter (ADC).

Over the years several circuits were developed for TVC and TDC; some convert pulse duration to a voltage, whilst others convert the time interval between two pulses to a voltage. In the latter circuits, some of the TVCs have two inputs, with two pulses generated on two separate wires; one applied to the START input of the TVC and the other to the STOP input. Alternatively, the START and STOP pulses may be applied to the same input. Moreover, while some of the TVCs or TDCs use digital circuits, others use analog circuits.

There's a circuit that uses two operational amplifiers and a number of switches to configure integrator and sample-and-hold stages that convert the duration of a single pulse to a DC voltage. Another circuit uses two op-amps, a 555 timer and a number of switches to convert a square wave input into a voltage proportional to the time between the edges (period) of the input signal, and thus its frequency. If the time between the pulse edges is decided by the START and STOP pulses, then both circuits can form a TVC.

There're also solutions that use a charge pump circuit to charge a capacitor with a constant reference current, whose voltage is then converted to a digital output using a dual-integrator circuit.

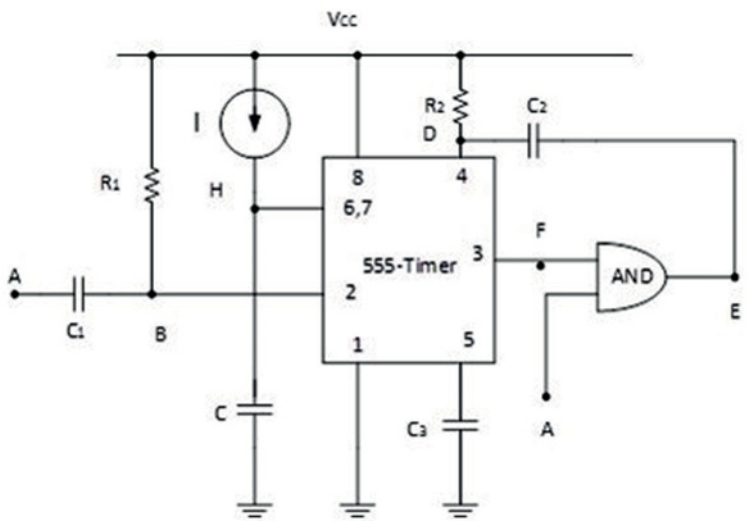

Figure 1: Proposed TVC

There are circuits that use a Vernier delay line formed of D-type flip-flops (FFs) for the TDC; and those that use a constant-current source and two switches to start and stop the charging of a capacitor, with the voltage across the capacitor measured via a voltage buffer. And so on.

Proposed Circuit

The circuit we propose here can operate as a time-to-voltage converter; see Figure 1. Its operation is as follows:

The differentiating circuit formed of R_1 and C_1 will differentiate the input START pulse A shown in Figure 2. The resulting output of the differentiator B will pull down the voltage at pin 2 of the 555 timer at the negative-going edge of START pulse A. When the timer is triggered, capacitor C will begin to charge via constant current source I, and the voltage at pin H will start increasing linearly with time, as shown in Figure 2.

In the meantime, the output voltage at pin 3 of the 555 timer (pin F of the AND gate) will be a pulse, whose duration will be limited by the arrival of the STOP pulse. The START pulse will also be applied to the AND gate, but as long as the output of the 555 timer is logic 0, the AND gate will be disabled and its output will also be logic 0.

The 555 timer will continue to be enabled by the voltage applied at pin 4. When the STOP pulse arrives, it will be differentiated by the R_1 C_1 differentiating circuit of Figure 1. The resulting output B of the differentiator, shown in Figure 2, will pull down pin 2 of the 555 timer, triggering it. However, this trigger will be ignored as the timer is already enabled and capacitor C will continue charging. The STOP pulse will also appear at the input of the AND gate.

With the other input of the AND gate connected to the output of the 555 timer, which is by now logic 1, the AND gate will be enabled and will produce an output corresponding to logic 1 in the form of a pulse. The duration of this pulse is equal to the duration of the STOP pulse. The output pulse of the AND gate will be applied to the differentiator circuit formed of R_2 and C_2 of Figure 1. The output of this differentiating circuit will pull down the voltage at pin 4 of the 555, disabling the timer, with the charging process of the capacitor C terminated.

The final value of the capacitor voltage will be given by

$$V_C = \frac{I}{C}T \qquad (1)$$

where T is the time interval between the START and the STOP pulses, as shown in Figure 2. This voltage represents the output of the TVC. A TDC can be obtained by applying the voltage across capacitor C to an ADC. During the charging process of capacitor C, the ADC will produce an output, which will not be available until a set of latches connected to the ADC are enabled by the negative-going edge of the STOP pulse.

It is worth mentioning here that for the TDC a fundamental trade-off between the dynamic range DR, that is the maximum time interval to be measured, and the number of bits N of the ADC is governed by Equation 2:

$$DR = 2^N T_{LSB} \qquad (2)$$

where T_{LSB} is the minimum time interval that can be resolved. This equation reveals that a long measuring interval will result in low resolution and vice versa.

Experimental Results

The functionality of the proposed circuit was tested using the LM555 timer, and a current source $I = 0.1mA$ obtained using a standard current-mirror formed of two transistors and a resistor. The values of the resistances R_1 and R_2 were chosen as $10.0k\Omega$. In fact, this value is not very critical since the resistors just provide the differentiation between the input pulses to trigger the LM555 timer.

The capacitors can be polypropylene, polystyrene or Teflon capacitors for C, C_1 and C_2 to minimize errors. The selected value for these capacitors is 0.01mF. The START and STOP pulses were obtained from another LM555 timer configured as a monostable multivibrator. Since the minimum pulse width obtainable from the LM555 timer is 10μs, the time interval between the START and STOP pulses was selected as 100μs. Thus, upon the arrival of the STOP pulse the voltage across the capacitor is 1V.

The experiment was repeated for different time intervals between the START and STOP pulses, and the voltage across the capacitors was monitored, with results in excellent agreement with the theoretical calculations.

It is worth mentioning here that faster 555 timers are available, which can provide shorter pulse widths than the LM555. This would allow the time interval between the START and STOP pulses to be reduced. One example of such a faster timer is the LMC555 from National Semiconductors (now Texas Instruments) which has a top speed of 3MHz. ●

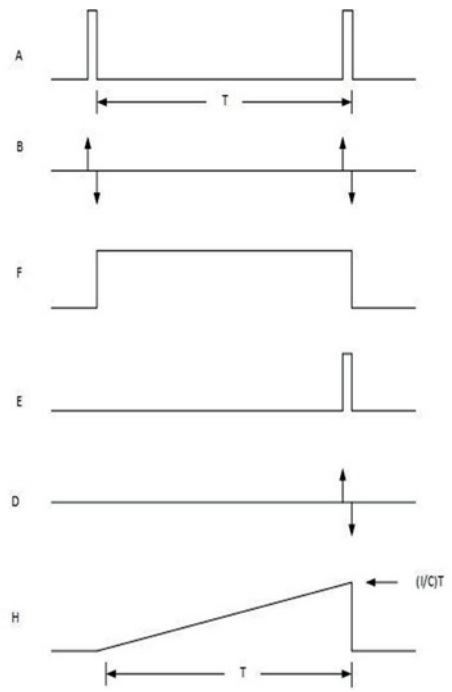

Figure 2: Waveforms at different nodes in the circuit of Figure 1

NOVEL DESIGN OF AN I-V CONVERTER FOR INFRARED RECEIVERS

YI-FAN SHI FROM THE BEIJING INSTITUTE OF TECHNOLOGY IN CHINA PRESENTS AN I-V CONVERTER FOR INFRARED COMMUNICATION, CONSISTING OF TRANSIMPEDANCE AMPLIFIER AND COMPENSATION STRUCTURES

Infrared (IR) communication technology possesses the advantages of low cost, low power and high speed among others that make it widely used in areas such as home appliances, remote control equipment and so on.

Figure 1 shows the functional block diagram of an IR receiver. The photodetector, generally a photodiode, transforms the optical signal into a current signal. An I-V converter amplifies input current signals and transforms them into voltage signals, which are then processed by a variable gain amplifier (VGA) and a bandpass filter (BPF). The VGA provides most of the gain in the system, which is adjusted according to the strength of the input signal. The BPF determines the selectivity of the receiver and limits its bandwidth. Its output signals are evaluated by a demodulator, consisting of a comparator, an integrator and a Schmitt trigger, which generates an envelope of the input signal without the carrier frequency for driving a transistor. The driven transistor provides a digital signal to a microcontroller or other device for further processing.

Conventional I-V Converter

The schematic diagram of a conventional I-V converter circuit is shown in Figure 2. The photodiode transforms IR signals into current signals, which are then converted into voltage signals by the transimpedance amplifier (TIA), whose transimpedance R_f can be expressed as Equation 1.

$$R_f = \frac{V_{out}}{I_{AC}} \quad (1)$$

In Figure 2, the purpose of M is to restrain the DC and low-frequency part of the input current, only allowing the signal at the frequencies of interest to be amplified by the TIA. When a DC current enters the TIA, its DC output voltage will deviate from the reference voltage V_{ref}. Moreover, an error voltage is generated by the error amplifier (EA), which controls the current source M to prevent more DC current at the input, regulating the TIA DC output voltage to V_{ref}.

The disadvantage of this circuit is obvious in Figure 2: the equivalent impedance of the current source M decreases as the input DC current increases, and the low impedance path will restrain parts of the signal at the frequencies of interest, with the sensitivity of the receiver reduced too. In this paper, a novel I-V converter with an AC compensation structure is proposed to improve the sensitivity of IR receivers.

Proposed I-V Converter

To fulfill the requirement of rejecting DC and low-frequency input current, and preserving the sensitivity of the receiver, two compensation structures are proposed; see Figure 3. The DC compensation circuit employs a variable resistance structure, whose equivalent resistance decreases as the input current increases. The AC compensation circuit is used to increase the resistance of the DC compensation circuit at

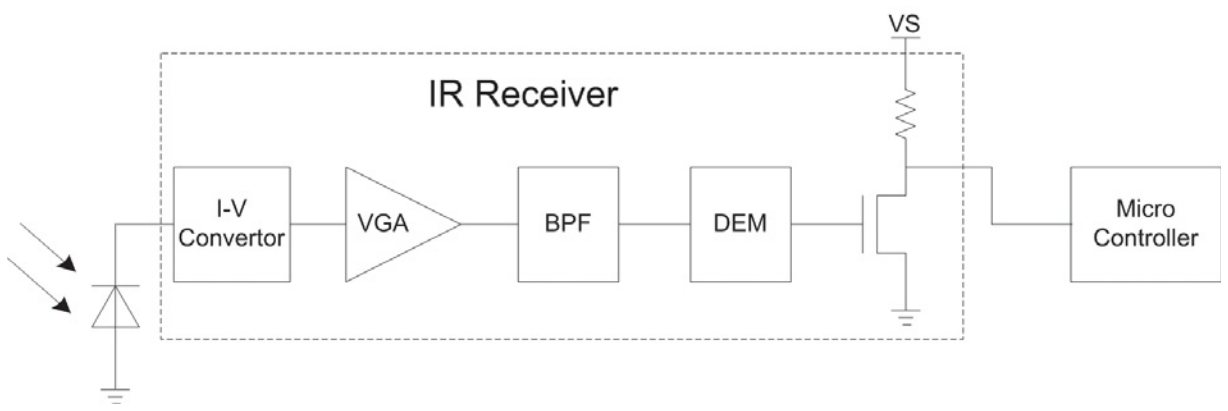

Figure 1: Functional block diagram of an IR receiver

signal frequency, preventing the useful signal from entering the DC compensation circuit, significantly improving receiver sensitivity.

The DC compensation circuit is shown in Figure 4.

$R_1 >> R_2 >> R_3$, and the emitter area ratio of Q_1 to Q_2 is 1:6. When I_{DC} is very small, both transistors turn off and the equivalent resistance of this circuit is:

$$R_{eq1} = \frac{V_{AB}}{I_{DC}} = R_1 + R_2 + R_3 \quad (2)$$

where V_{AB} is the voltage across R_1, R_2 and R_3.

As I_{DC} increases, Q_1 turns on first, so the equivalent resistance can be expressed as:

$$R_{eq2} = \frac{V_{AB}}{I_{DC}} = R_1 + R_2 + R_3 - \frac{I_{C1}}{I_{DC}} R_1 \quad (3)$$

where I_{C1} is the current flowing through Q_1.

When I_{DC} is very large, both Q_1 and Q_2 turn on, and the equivalent resistance is:

$$R_{eq3} = \frac{V_{AB}}{I_{DC}} = R_1 + R_2 + R_3 = -\frac{I_{C1} + I_{C2}}{I_{DC}} - \frac{I_{C2}}{I_{DC}} \quad (4)$$

where I_{C2} indicates the current in Q_2.

Equations 2-4 show that resistance decreases as I_{DC} increases, which means the circuit separates the DC and low frequency components from the useful signal by providing a low-impedance path to ground. Therefore, there are few DC and low frequency currents that can enter the TIA, and V_{out} does not saturate, even when there's large DC current entering the receiver.

AC Compensation Circuit Design

The structure of the AC compensation circuit is symmetrical; see Figure 3. The DC voltage level of the Q_6's base is:

$$V_{be6} = V_A = V_S - V_{BE} \quad (5)$$

where V_{BE} is the voltage across the emitter PN junction.

This circuit possesses a high-pass characteristic with a lower cutoff frequency ω_c:

$$\omega_c = \frac{1}{[r_{ce4} \| (r_{be6} + (1+\beta)R_5)]C} \quad (6)$$

where r_{ce4} is the small-signal equivalent-impedance between Q4's collector and emitter, and r_{be6} is the small-signal equivalent impedance between the base and emitter of Q_6; ω_c should be set at a frequency lower than the useful signal frequency.

When part of the signal enters the DC compensation circuit, it will cause a voltage drop ΔV_B at point B of Figure 4. After two source followers, there is a similar voltage drop ΔV_A at

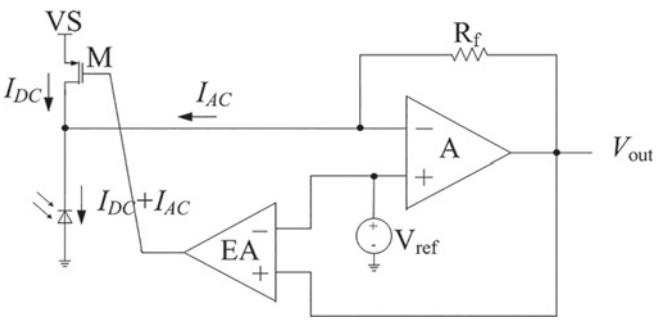

Figure 2: Schematic diagram of a conventional I-V converter

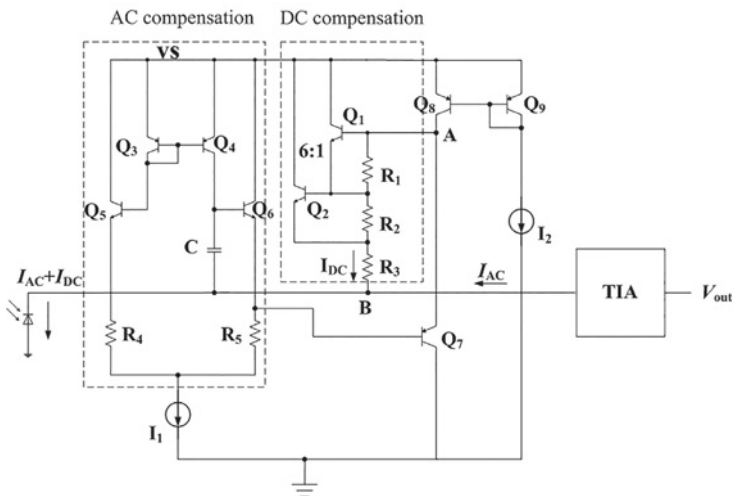

Figure 3: Circuit diagram of the proposed circuit

point A in Figure 4. So the equivalent impedance of the DC compensation circuit at the signal's frequency is then:

$$R = \frac{\Delta V_B - \Delta V_A}{\Delta I} \quad (7)$$

where ΔI is the signal current entering the DC compensation circuit. It can be determined that R is much larger than without compensation. Also, with fewer currents at signal frequency entering the DC compensation circuit, the receiver's sensitivity does not decline dramatically with a large DC input current.

TIA Circuit Design

Figure 5 shows the schematic of the TIA. There are two negative feedback loops; the DC negative feedback loop to set the common-mode level for the amplifier, and the AC negative feedback to amplify the signal. The DC negative feedback loop employs a V-I structure, with characteristic

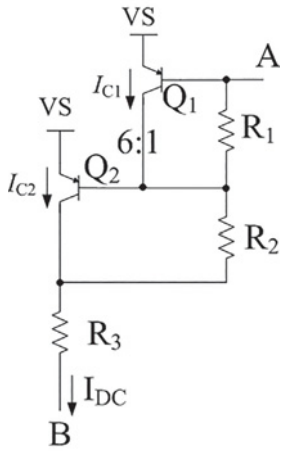

Figure 4: DC compensation circuit

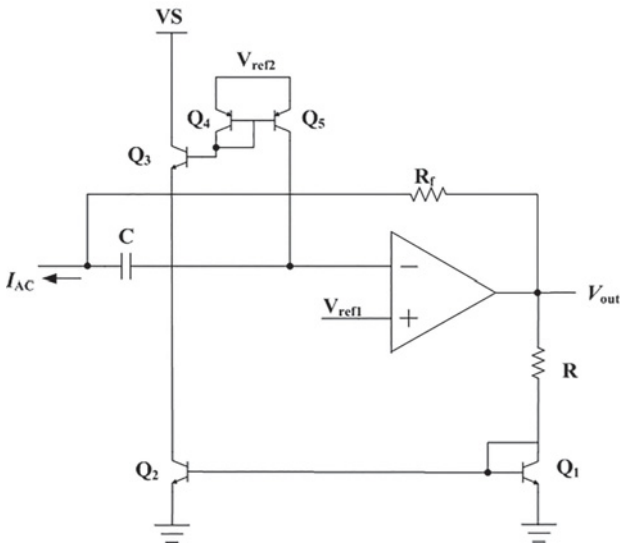

Figure 5: TIA schematic diagram

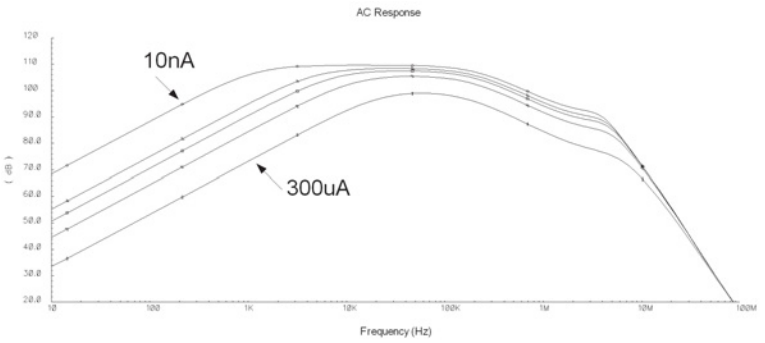

Figure 6: Transimpedance gain of the I-V converter without AC compensation under different DC input currents

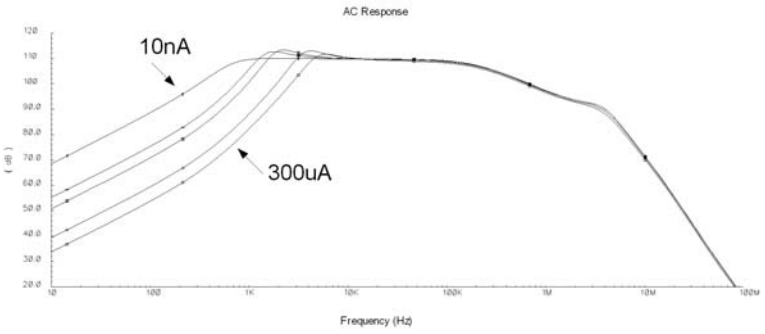

Figure 7: Transimpedance gain of the I-V converter with AC compensation under different DC input currents

high impedance at the non-inverting input of the amplifier. The V-I feedback structure has little influence on the AC feedback loop.

The purpose of employing two feedback loops is to increase the DC input impedance of the TIA and thus decrease the amount of DC current entering it.

Experimental Results

The I-V converter was implemented in the 0.6µm BiCMOS process. Figure 6 shows the transimpedance gain of the converter without AC compensation under different DC input currents. The converter achieves a gain of 109dBΩ with no DC input current, but the gain declines dramatically as the DC input current increases.

> The converter achieves a gain of 109dBΩ with no DC input current, but the gain declines dramatically as the DC input current increases

Figure 7 shows the gain of the I-V converter with AC compensation circuit under different DC input currents. The transimpedance gain stays at 109dBΩ for the signal frequency range 30kHz-60kHz, even if the DC input current is very large.

It is confirmed that the circuit achieves DC input current rejection while preserving the sensitivity of the receiver. The simulation results show that the circuit provides a transimpedance gain of 109dBΩ and can reject DC currents up to 300µA. Moreover, the circuits shown can be successfully used in IR products. ●

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Features

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ENHANCED DOUBLE-PI MODEL FOR ON-CHIP SPIRAL INDUCTORS

BY **MINGLIN MA, ZHIJUN LI** AND **XUE ZHANG** FROM XIANGTAN UNIVERSITY IN HUNAN, CHINA, **XIANGLIANG JIN** FROM HUNAN ENGINEERING LABORATORY FOR MICROELECTRONICS, OPTOELECTRONICS AND SYSTEM-ON-A-CHIP, AND **YICHUANG SUN** FROM THE UNIVERSITY OF HERTFORDSHIRE, HATFIELD, UK

Spiral inductors are extensively used in modern RFCMOS integrated circuits. Many studies have been done to capture their high-frequency behaviour, since an accurate model is crucial for reliable integrated circuit implementation and design optimization.

The single-PI and double-PI models are most popular, with the single-PI model offering advantages such as easy extraction of parameters, while the double-PI model is very accurate. Disadvantages, however, include a decrease in the effective series resistance (ESR), caused by substrate coupling at high frequency not accurately represented by the single-PI model, whereas in the double-PI, with its distributed nature, it is hard to extract its parameters.

Obviously we can get a more accurate double-PI model by converting a more accurate single-PI model. Joonho Gil

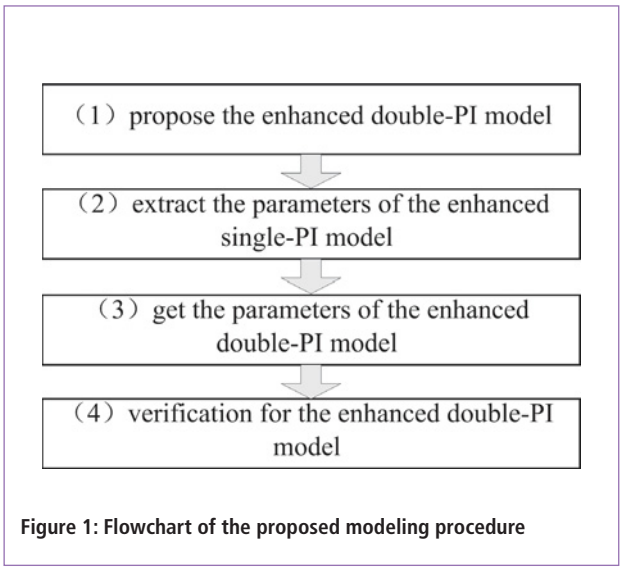


Figure 1: Flowchart of the proposed modeling procedure

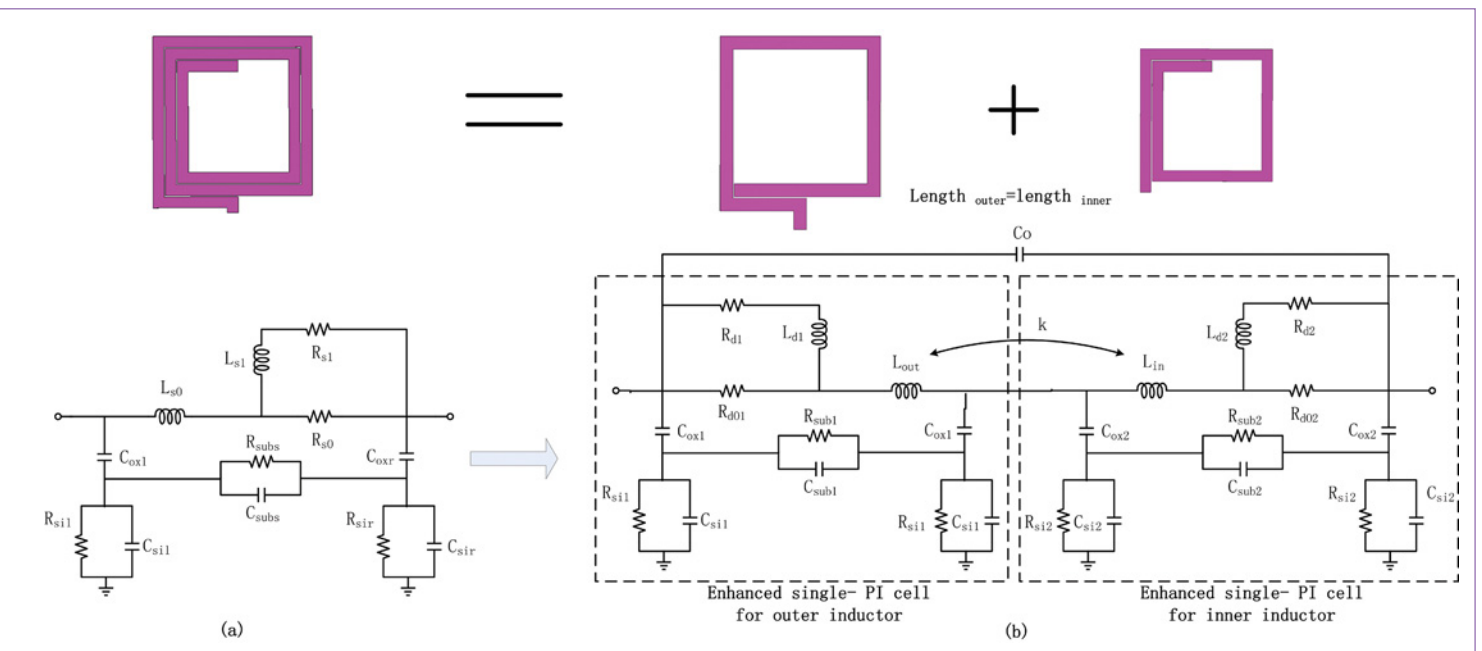


Figure 2: (a) Schematic of the spiral inductor and enhanced single-PI model; (b) The inductor is assumed to be divided into halves, which is an enhanced single-PI structure. There is coupling factor k between the inductances (L_{s1},L_{s2}) of the outer/inner inductors

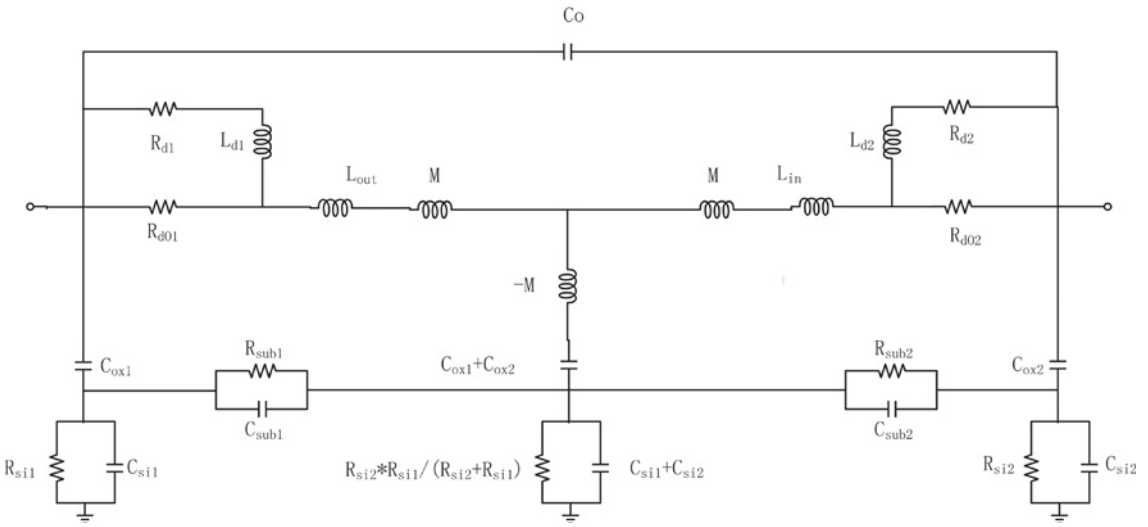


Figure 3: Enhanced double-PI model

presented an enhanced single-PI model, taking into account the substrate coupling too. Based on this enhanced single-PI model, we present an enhanced double-PI model, starting with a flowchart of the proposed modeling procedure; see Figure 1. Figure 2 shows the schematic of the spiral inductor, simulated in HFSS, and that of the corresponding enhanced double-PI model.

Enhanced Double-PI Model

We divided the spiral into inner and outer sections of the same length to reduce the number of unknown parameters; each partitioned inductor can then be modeled separately as an enhanced single-PI circuit, as shown in Figure 2b. To represent the lateral substrate coupling, R_{sub} and C_{sub} are introduced in the enhanced single-PI circuit. C_{ox} represents the oxide capacitance between inductor and substrate, and R_{si} and C_{si} are the substrate resistance and capacitance to ground respectively.

The LR ladder circuit formed by L_{s1} and R_{s1} in parallel to R_{s0} is used to capture the increase in series resistance due to both skin and proximity effects. A mutual coupling coefficient k between the outer and inner inductors was also introduced to produce the total inductance, which is larger than the sum of two self-inductances of the partitioned inductors.

The series capacitance (C_o) models the capacitive coupling between the input and output ports of the inductor.

We assume that the series inductances (L_{out}, L_{in}) of the inner and outer inductors are already known. The relation of all inductances can be expressed as:

$$L_{s0} = L_{out} + L_{in} + 2M = L_{out} + L_{in} + 2k\sqrt{L_{out}L_{in}} \quad (1)$$

where M is mutual inductance and k coupling coefficient. Considering the equivalent circuit for self-inductance and mutual inductance in the T-branch, we get the final enhanced double-PI model as shown in Figure 3.

Parameter Extraction

To verify the model, we simulated a 2.5-turn square inductor 2um thick and the partitioned out/inner inductors in HFSS.

Figure 2 shows the top views of these three inductors, where the line width (W), line spacing (S) and inner radius (R) are 15, 1.5 and 60um, respectively. The substrate resistivity is $10\,ohm\cdot cm$, and the thicknesses of the oxide dielectric, passivation and substrate are 9.8, 0.7 and 300um, respectively.

We used simulation results to extract the model parameters in ADS. To extract all elements of the enhanced single-PI model, it is split into several sub-circuits as shown in Figure 4. The parameter extraction process is shown in Figure 5.

In the low frequency band 0-1GHz, Y_{up} is approximately equal to Y_{HFSS}. We then use a set of equations to determine R_{s0}, R_{s1}, L_{s0} and L_{s1}. We find that we can ignore the effects of R_{subs} and C_{subs} to Y_{low} in the frequency band 3-6GHz. Then we can mathematically determine $C_{oxl,r}$, $R_{sil,r}$ and $C_{sil,r}$. According to Figure 6, the ABCD matrix of the 3rd sub-circuit $[T_{s3}]$ can be determined by:

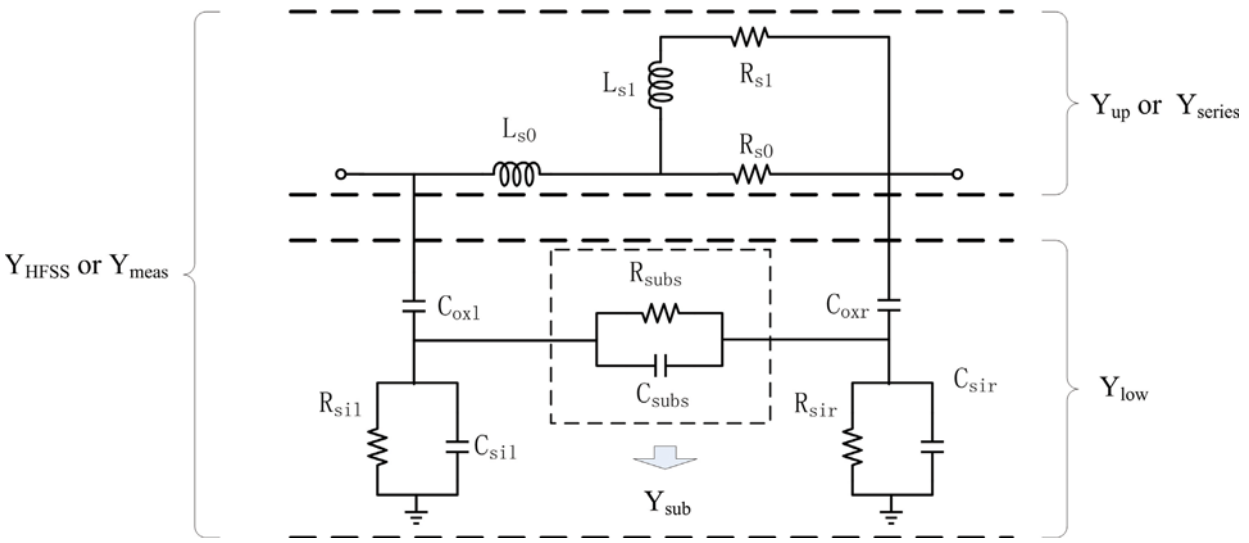


Figure 4: Y_{series}, Y_{up}, Y_{meas}, Y_{HFSS}, Y_{low}, Y_{sub} in the enhanced single-PI model

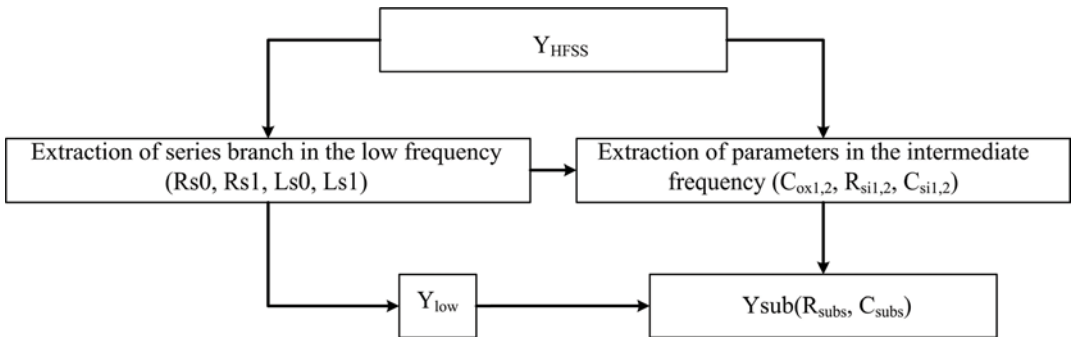


Figure 5: The parameter extraction process

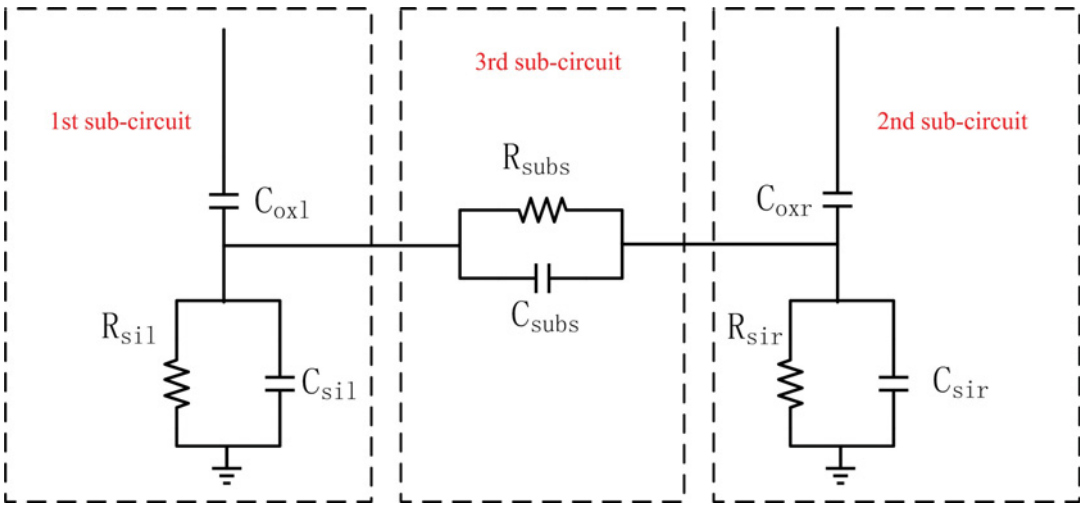


Figure 6: Lower part of the circuit of the enhanced single-Pi model

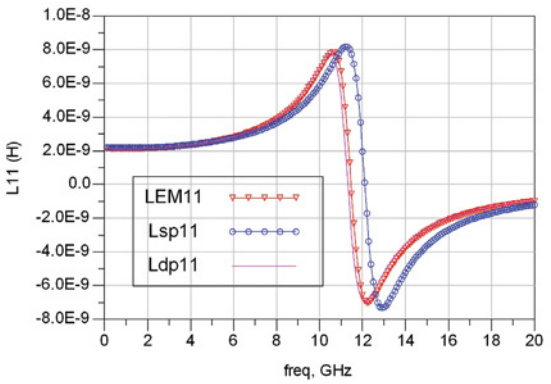


Figure 7a: Equivalent inductances seen from one port of the inductor, with the other port acting as AC-shorted

$$[T_{s3}] = \begin{bmatrix} A_{subs} & B_{subs} \\ C_{subs} & D_{subs} \end{bmatrix} = \begin{bmatrix} A_{s1} & B_{s1} \\ C_{s1} & D_{s1} \end{bmatrix}^{-1} \begin{bmatrix} A_L & B_L \\ C_L & D_L \end{bmatrix} \begin{bmatrix} A_{s2} & B_{s2} \\ C_{s2} & D_{s2} \end{bmatrix}^{-1} = [T_{s1}]^{-1}[T_L][T_{s2}]^{-1} \quad (2)$$

where $[T_L]$ is the ABCD matrix of the lower sub-circuit, which can be determined from the Y-matrix of the lower sub-circuit, or $Y_{low} = Y_{HFSS} - Y_{up}$. Also, $[T_{s1}]$ and $[T_{s2}]$ are the ABCD matrices of the first and second sub-circuits, determined by using $C_{oxl,r}$, $R_{Sil,r}$ and $C_{Sil,r}$. With the matrix $[T_{s3}]$, R_{sub} and C_{sub} can be determined using:

$$\frac{1}{R_{subs}} + j\omega C_{subs} = Y_{subs} = \frac{1}{B_{subs}} \quad (3)$$

All parameters of the whole inductor are shown in Table 1.

Single- To Double-PI Model Conversion

The inner and outer inductors' self-inductances (L_{out}, L_{in}) can be determined the same way as with the entire inductor.

To determine the substrate capacitances, we can refer to the elementary electromagnetic analysis result that the product of R_{sub} and C_{sub} is constant. For the same reason:

$$R_{sub1,2} = R_{sub} / 2 \quad (4)$$

and

$$C_{sub1,2} = 2 * C_{sub} \quad (5)$$

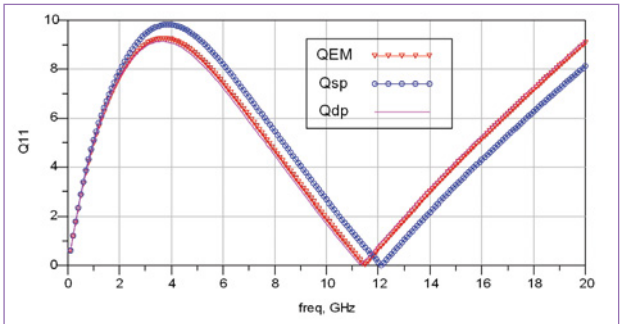


Figure 7b: The absolute value of the quality factors seen from one port of the inductor, with the other port acting as AC-shorted

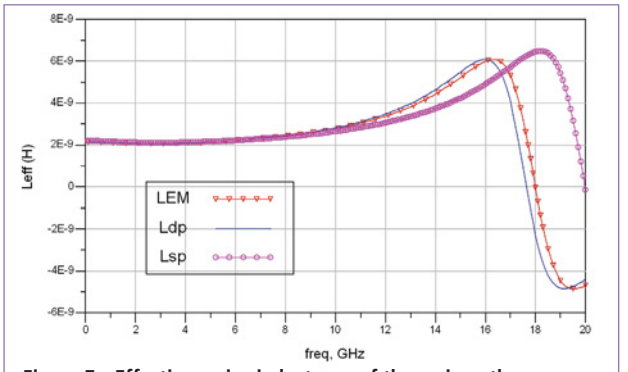


Figure 7c: Effective series inductance of the main path

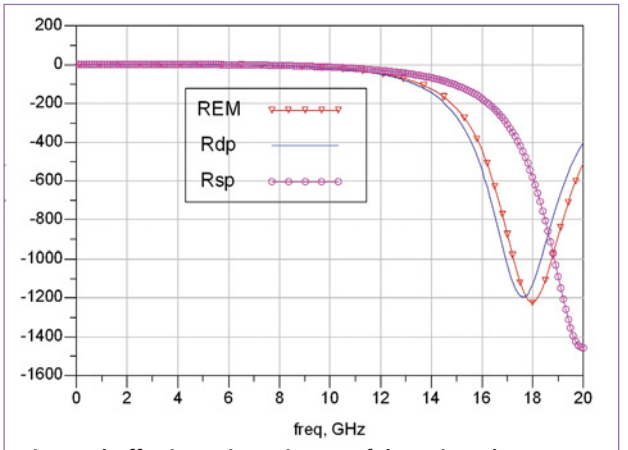


Figure 7d: Effective series resistance of the main path

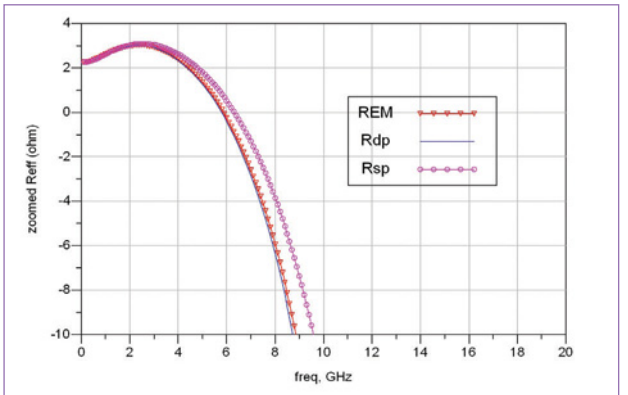


Figure 7e: Effective series resistance of the main path at low frequencies

Model parameters	value extracted	Model parameters	value extracted
L_{s0}(H)	2e-9	R_{si1}(ohm)	201
L_{s1}(H)	0.8122e-9	R_{si2}(ohm)	181.6
R_{s0}(ohm)	3.839	C_{si1}(fF)	77.8
R_{s1}(ohm)	5.445	C_{si2}(fF)	107.5
C_{ox1}(fF)	129	R_{subs}(ohm)	125
C_{ox2}(fF)	144.7	C_{subs}(fF)	253

Table 1: Enhanced single-PI model parameters for the inductor

C_o can be determined by optimization. All parameters of the enhanced double-PI model are shown in Table 2.

Model Verification

An on-chip spiral inductor is a two-port device and characterized by two-port S or Y parameters. There should be a constrain $S_{12} = S_{21}$ or $Y_{12} = Y_{21}$ for a linear passive network according to its reciprocal nature. Thus, Y parameters can be transformed into the following six independent quantities:

$$\begin{cases} L_{11} = \dfrac{1}{\omega} imag\left(\dfrac{1}{Y_{11}}\right) \\ L_{22} = \dfrac{1}{\omega} imag\left(\dfrac{1}{Y_{22}}\right) \\ Q_{11} = abs\left(imag\left(\dfrac{1}{Y_{11}}\right) / real\left(\dfrac{1}{Y_{11}}\right)\right) \\ Q_{22} = abs\left(imag\left(\dfrac{1}{Y_{22}}\right) / real\left(\dfrac{1}{Y_{22}}\right)\right) \\ L_{eff} = \dfrac{1}{\omega} imag\left(\dfrac{-2}{Y_{12} + Y_{21}}\right) \\ R_{eff} = real\left(\dfrac{-2}{Y_{12} + Y_{21}}\right) \end{cases} \quad (6)$$

L_{11} (shown in Figure 7a), L_{22}, Q_{11}(shown in Figure 7b) and Q_{22} are the equivalent inductances and absolute values of the quality factors seen from two ports of the inductor respectively, with the other port acting as if AC-shorted. L_{eff} (shown in Figure 7c) and R_{eff} (shown in Figure 7d and e) present the effective series inductance and resistance of the main path at low frequencies; both lack physical meanings when the frequency goes higher because R_{eff} will eventually become negative.

$$R_{DC} = R_{eff}\big|_{\omega \to 0} \quad (7)$$

$$L_{DC} = L_{eff}\big|_{\omega \to 0} \quad (8)$$

where R_{DC} is DC resistance and L_{DC} is the inductance when $\omega \to 0$. R_{eff} is equal to the DC resistance first, and then rises with frequency due to skin and proximity effects.

Eventually R_{eff} reaches a maximum at a certain frequency, after which it begins to drop until it reaches a negative value when the frequency is sufficiently high. This phenomenon is due to the distributed nature of capacitive substrate coupling that overrides the skin and proximity effects.

The values shown in Figure 7 indicate a better agreement between the enhanced double-PI model performance (Q_{11dp}, L_{11dp}, L_{effdp} and R_{effdp}) and EM simulation results (Q_{11EM}, L_{11EM}, L_{effEM} and R_{effEM}) over a wide frequency range than the performance of the enhanced single-PI model (Q_{11sp}, L_{11sp}, our method is to use simple single-PI model parameters to determine the double-PI model parameters, to accelerate the scalable modeling procedure with little loss in precision. ●

parameters	L_{out}(H)	L_{in}(H)	M (H)	$R_{d01,2}$(ohm)	$R_{d1,2}$(ohm)
values	0.514E-9	0.886e-9	0.3e-9	2.723	1.919
parameters	$L_{d1,2}$(H)	C_{ox1}(fF)	C_{ox2}(fF)	C_{ox3}(fF)	C_{si1}(fF)
values	0.4061E-9	47.85	89	136.85	32.9
parameters	C_{si2}(fF)	R_{si1}(ohm)	R_{si2}(ohm)	C_{si3}(fF)	R_{si3}(fF)
values	59.5	535	296	92.4	190.6

Table 2: The parameters of the enhanced double-PI model

SELF-POWERED AND BATTERY-POWERED IOT WIRELESS SENSOR CHALLENGES

BY **STEWART WILSON**, EMEAI PARAMETRIC TEST BUSINESS MANAGER AT KEYSIGHT TECHNOLOGIES

It is estimated that by 2020, the Internet of Things, or IoT, will connect 50 billion devices that transmit useful data and control information via sensor networks. Although it's possible for a network to use wired sensors, the wireless variety provides easier deployment and wider flexibility.

Wireless sensor networks will introduce significant changes to monitoring the environment to support wide-ranging applications, from smart power grids and intelligent transportation to fleet tracking, industrial control and home security. But, one factor that currently limits their use is the short time-span during which wireless sensors can do their job. If a wireless sensor depends fully on a battery and the battery is depleted the sensor becomes worthless.

The simplest way to increase battery life is to use a bigger battery. This however does not tie in well with customer expectations of sensors to be small, provide high performance, transmit large amounts of data and have local data processing capabilities. Instead of increasing battery size, a typical approach to conserving battery energy is to segment the wireless sensor operation into a series of activities, each with a specific power level and for a specified duration. Once the sensor performs a required activity, it then goes into a low-power mode, such as idle or sleep.

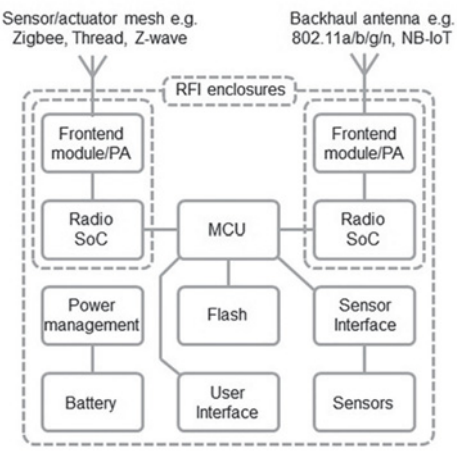


Figure 1: Typical components of an IoT gateway/sensor (e.g., a heating thermostat, smoke alarm, security alarm, or utility meter gateway)

As such, design engineers are expected to have in-depth knowledge of battery life, current drain and power consumption, ideally on each individual sensor's clock-cycle basis, a nigh on impossible task with traditional measurement techniques.

Assessing Actual Battery Life

A battery contains a defined amount of energy, specified in watt hours (Wh), with capacity in ampere hours (Ah). A battery's energy is the product of its voltage (V) and capacity (Ah), with the voltage rating typically taken at the midpoint of the battery's discharge curve. Based on this, battery life can also be estimated by using the following equation:

Battery life (hours) = Battery capacity (Ah)/Average current drain (A)

However, when a device operates in the real world, battery life is typically much shorter than the calculated number, primarily due to dynamic current drain.

Measuring Dynamic Current Drain

To conserve energy in battery-powered wireless sensors, engineers design the device's sub-circuits to be active only when necessary. Most of the time the device is in sleep mode with minimal current drain, with only the real-time clock operational. The unit wakes up periodically to perform measurements and transmit data to a receiver. To optimize battery life, device performance has to be characterized and its energy requirements in each mode properly understood. Its different operating modes result in a current drain that spans a wide dynamic range, typically from tens of nA in sleep mode to hundreds of mA during transmit mode. This equates to a dynamic current ratio of around 1:10,000,000.

MODE	CURRENT	DURATION
Transmission (TX)	20-300mA	1-100ms
Active	100µA - 10mA	10-100ms
Sleep	50nA - 50µA	100ms-minute

Table 1: Typical sensor current levels and time at those levels during measurement, transmission and sleep

Knowing how much energy is consumed in sending out a single packet of information is critical to optimizing battery life, and it helps with design questions such as: "Should information be sent

once every second, every five seconds or every ten seconds?". Accurate estimates of the impact of any firmware change on battery drain have to be validated in real time, and "in application" measurements are crucial.

Traditional Measurement Techniques

One well-known method for measuring current is with the ammeter function of a digital multimeter (DMM). Although the accuracy of these measurements seems sufficiently high, specifications are defined for fixed ranges and relatively static signal levels. Due to the dynamic current drain of a wireless sensor, especially whilst the sensor is transmitting, there may be reading instabilities. The DMM makes measurements by inserting a shunt in the circuit and measuring the voltage drop across it.

For low-current measurements, normally a low range based on a shunt with high resistance is selected, whereas for high currents, a high range based on a low-resistance shunt is selected. In each case there is a voltage drop in the shunt called burden voltage. Due to this voltage drop, not all the battery voltage reaches the wireless sensor. In practise most accurate low ranges for sleep current measurements result in large burden voltages during current peaks that can cause the device to reset. The practical solution is to use a high-current range that keeps the device operating during current peaks. This compromise enables handling of peak currents and measuring sleep currents. However, it comes at a price. As the offset error is specified at full scale, it heavily impacts measurements on low current levels.

Using Oscilloscopes

After measuring a sensor's low current level during sleep mode, the active and transmission current pulses need to be measured – this applies to both the current level and the time the sensor spends at that level. Oscilloscopes are excellent tools for measuring signals that change over time, where currents of tens of mA need to be measured.

Good clamp probes have noise of around 2.5mA rms with the zero compensation procedure repeated regularly, although this type probes are not suitable for measuring such levels due to their limited sensitivity and drift. Increasing current probe sensitivity is possible by passing the same wire multiple times through the probe to multiply the magnetic field. This results in a coil with greater sensitivity but lower bandwidth. Using this approach, the current pulse of the activity and the transmission time can be captured easily.

Within activity and transmission pulses, the current switches between high and low levels. To properly calculate the average current, export the waveform and integrate all the measured points to get the average value. Oscilloscopes capture a single burst well. However, the measurements become more complex if verification is needed of how many times a sensor activates during a time frame and how often it sends out a TX burst. Sensors may have operational cycles of minutes, hours or days, which are very challenging to capture and measure with an oscilloscope.

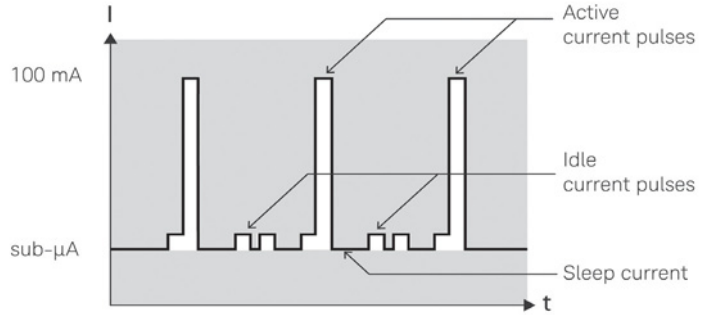


Figure 2: The Keysight N6781A SMU permits accurate measurements across dynamic current levels

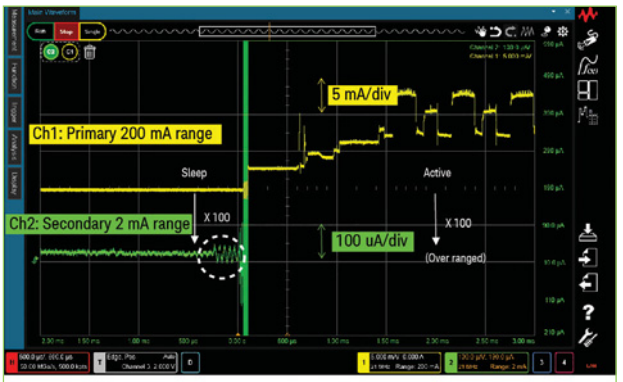


Figure 3: Current profile measurement example with CX1102A dual-channel current sensor

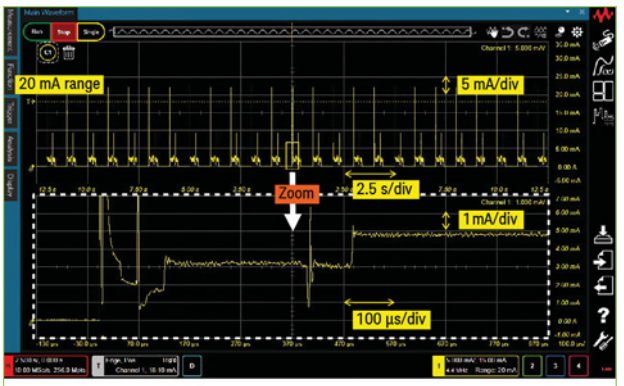


Figure 4: A long-term 25s measurement at 10MSps

New Measurement Solutions

The Keysight N6781A source/measure unit (SMU) for battery drain analysis and the CX3300A Device Current Waveform Analyser overcome these limitations of traditional measurements with two innovations. On the N6781A SMU it is seamless current ranging and long-term, gap-free data logging. On the CX3300A it is measurement sensitivity (100pA), with bandwidth of 200MHz at 1Gs/s and memory depth of 256Mpoints/channel respectively.

Seamless current ranging is a patented technology that enables the N6781A SMU to change the measurement range whilst keeping the output voltage stable without any dropouts. The CX3300A has a unique dual-channel sensor that allows 100dB of dynamic range, enabling seamless measurements of nA standby currents whilst instantaneously displaying peak transmit (Tx) current.

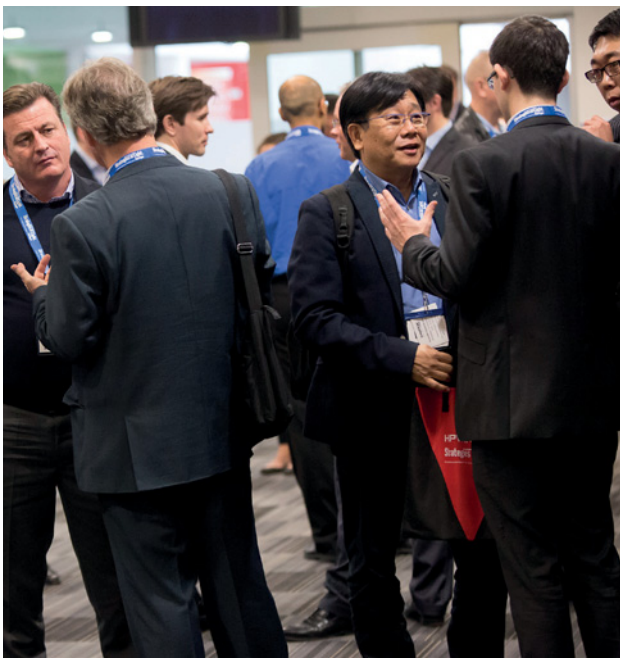
SEE THE FUTURE OF LIGHTING UNDER ONE ROOF

Philip Smallwood, Director of LED & Lighting Research, Strategies Unlimited and Conference chair for the forthcoming Strategies in Light Europe conference, provides his overview of what visitors and delegates can expect to see at the show this year.

This is the seventh iteration of Strategies in Light Europe, and my first as the Chair of the conference. Last year was the first time we co-located the show with LuxLive, one of the premier lighting trade shows in Europe, and I am very excited to keep up with the momentum of last year's successful partnership.

As you all know, the landscape of the industry is currently experiencing tremendous change. Not only have LED technologies made their way into the mainstream, but connected smart lighting technologies are the new "unknown" of the market that is causing shifts in not only how we perceive and think about light, but also how we go about the business of lighting. This new paradigm has required us to re-think the content of SIL Europe to keep the show at the forefront of the industry.

The Keynote and Plenary Sessions of the show will feature top executives from leading industry companies and organizations. The day will start with an exhilarating introductory keynote from OSRAM, Mr. Geert Van Der Meer, Senior Vice President & CEO of Business Unit Digital Systems will provide an exciting overview of what the path to mass adoption and monetization of lighting in the IOT might look like. He will be followed by Bill Rogers, Head of Strategy at The Green Investment Bank, who will go over how LED first changed the financing dynamics of the industry and how they are poised to continue changing with the increased usage of connected smart lighting. Our last keynote, Falk Meissner, Chief Strategy Officer of Lumileds will discuss how the evolution that continues within the packaged LED market is allowing for the creation of fixtures that are more than merely functional light, but provide for an exciting and immersive user experience.




Philip Smallwood

In order to keep up with these changes, the Advisory Board and I have overhauled the theme of the conference, which is divided into two sessions: "Dealing with A Disrupted Lighting Market", which will cover topics pertinent to the disruptive changes the industry is facing today. Presentations will revolve both around technological advancements and changing market dynamics. Discussions during this session will range from lasers used for lighting and data collection from smart connected lights to LED, lamp and luminaire forecasts presented by Strategies Unlimited's most up-to date market research reports. "The Future of Lighting" was designed to enhance the thinking of attendees as to provide a vision of what the market of the future might look like. Topics covered during these sessions will range from how lighting fits into the Internet of Things (IOT) and human centric lighting to new business practices being employed in the market.

- Keith Strickland, Chief Technology Officer, Plessey Semiconductirs Ltd, United Kingdom
- Joost Demarest, CFO & CTO, KNX, Belgium
- John Baekelmans, CTO, Cisco, United Kingdom
- Verena Rathjen, CEO Business Segment 'New Business' -Professional Luminaires / Smart Home, LEDVANCE, Germany
- Shane Cohen, Global Director of Lighting, Humanscale Corp, Israel
- Simon Coombes, CTO, GOOEE, United Kingdom
- Bianca van Der Zande, Senior Scientist, Philips Research, The Netherlands

I am very excited about SIL Europe this year and learning more about how our market continues to change. I look forward to seeing all of you in London!

For further information, please visit the event website, ***www.sileurope.com***

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LIGHT YEARS AHEAD: RAPID ADVANCES IN HIGH-PERFORMANCE AND MULTI-PIXEL LED TECHNOLOGY

BY **STEFAN GROETSCH**, SENIOR KEY EXPERT FOR APPLICATIONS, LED/AUTOMOTIVE, AT OSRAM OPTO SEMICONDUCTORS

Two of the biggest challenges for automotive manufacturers are how to maximize safety requirements whilst maintaining flexibility in design. A critical element toward solving these challenges is advances in lighting, from headlamps to interior aesthetics. The latest innovative types of LEDs deliver new possibilities in design; with compact dimensions, high luminance and individually controllable chips – all enabling flexibility in lamp construction.

In the past, the most common light source for headlamps was the halogen filament lamp. Its key advantage is low cost, and it is considered a technically robust solution. The fact that it is easily replaceable compensates for its limited service life. It does, however, have relatively high energy consumption and low efficiency, an average of 26 lumens per watt; and because the light is radiated in all directions, halogen filament lamps offer poorer illumination performance overall compared to the alternatives. At less than 3,000 kelvin, the colour is always in the spectrum of warm light, whilst cold light options are considered advantageous for night vision.

HID (high intensity discharge) lamps, on the other hand, offer a significantly better efficiency at typically 90 lumens per watt. However, when the covers of HID headlamps are obscured by dirt, this produces glare through scattering. Consequently, a cleaning system such as headlamp wipers is mandatory above a certain brightness, adding to design complexity and cost.

LEDs

Compared to these conventional light sources, LEDs offer many advantages. They are increasingly replacing incandescent light bulbs in automotive manufacture, particularly for signalling lamps such as brake lights or indicators. With brightness levels increasing, they are even becoming a good option for headlamps.

At some 100 lumens per watt today, they already provide a high level of energy efficiency, ensure good luminous efficacy, and are extremely robust and resistant to vibrations and environmental influences. In addition, they are durable enough that there is hardly any noticeable reduction in performance throughout the nominal 10,000 operating hours of a typical vehicle's life. This will become even more relevant for electric vehicles than for petrol or diesel cars.

At a colour temperature of 6,000 kelvin, LEDs also cover the full required wavelength distribution. Studies have shown the brightness of the LED spectrum perceived by the driver to be higher than that of alternative light sources by a factor of 1.3 to 1.5.

LEDs are already being used as a configuration option instead of HIDs in some sports cars and luxury vehicles. Further development work, such as simplified assembly methods, now aims at making the solutions even more energy-efficient and lower in cost so they are suitable for use in a mass market. At the same time, increasingly smaller LED lamps facilitate new design options and intelligent headlamp systems that are safer on the road.

The rapidly decreasing size of LED units (currently less than

Figure 1: A chip that enables LED ADB functions to be built with up to 25 pixels per headlamp (left). A more compact chip (right) enables more flexible designs, in addition facilitating AFS (Osram Ostar Headlamp Pro Mono (left), Oslon Compact (right)

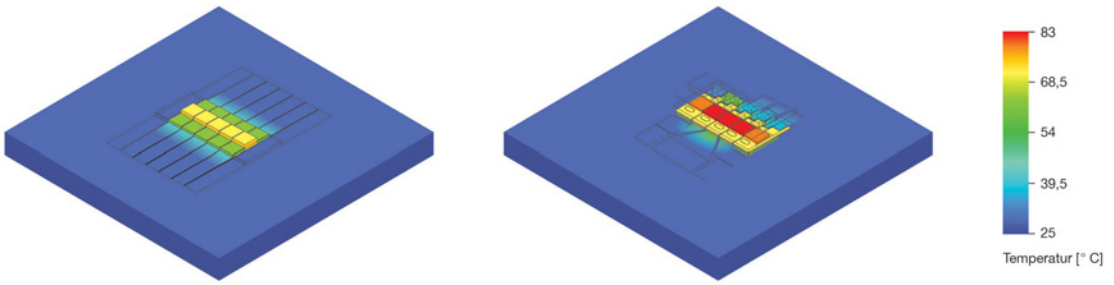

Figure 2: This diagram shows the improved thermal management of an individually controllable multi-chip LED (left), therefore reducing system cost (Oslon Black Flat S (left), predecessor version (right)

20mm x 21mm) offers much better scope for innovative light source design. Using surface mount technology (SMT) and UX:3 chip technology for powerful light emission of around 430mW at 500mA operating current will allow to pack up to 84 LEDs into a single, flexible unit. Arranging the units in tight arrays enables the use of fibre optic solutions for daytime driving or indicators.

Innovations

An Adaptive Front-lighting System (AFS) is one innovation made possible by these developments. It uses a dashboard camera to record the area in front of the vehicle, in conjunction with dedicated electronic control units to calculate the best lighting configuration in real time. This system controls a swivel mechanism for aiming the light beam – for example, when taking a corner, offering drivers the best possible visibility.

By illuminating the side of the road, or helping to protect oncoming traffic from glare through the Adaptive Driving Beam (ADB), AFS is helping decrease the risk of road traffic incidents.

For this mechanism to work inside the headlamp, it only requires individual chips to be switched on and off by an intelligent control system. This system uses several sensors to achieve a glare-free high beam by dynamically shutting off areas in the headlamp light distribution, for example to avoid blinding or dazzling other road users, or to illuminate potential obstacles along the road. Further, several LEDs on multiple individually-controllable chips could even use the anti-glare function for multiple road users whilst fully illuminating the area between them.

The use of SMT has also had a positive impact on the cost of developing LED lighting for automotive manufacture. Placing three to five UX:3 chips in one array at maximum dimensions of 7.9mm x 3.75mm x 0.5mm produces a headlamp assembly as a single light source, for both low and high beam. This can be turned off as required by electronic switches, producing a brightness of 2,000lm. Switching between lighting functions is achieved by means of a moving shutter. Thanks to the thermal optimisation of the SMT component, the headlamp could be designed to operate with passive cooling. At a current of 1A, a power loss of 12W and an ambient temperature of 25°C, the temperature at the central chips is only 69°C, which is a 44°C difference. Previously, the temperature difference achieved in the lab was 58°C.

The combination of high efficiency and good thermal interfacing reduces system cost considerably since it permits passive cooling, making LED solutions an interesting headlamp option for a wider market.

Further Developments

Despite its benefits, SMT poses greater challenges for assembly with respect to the precision required in positioning the optical headlamp components. The cost of providing cooling in the headlamp is indirectly proportional to the efficiency of the LEDs used. Consequently, work continues on improving efficiency, since an increase in the proportion of useful optical radiation goes hand in hand with a reduction in thermal power loss, which also means that less cooling is required.

There is also a lot of room to develop LED technology even further, providing new design scope for headlamp systems. For example, higher levels of luminance mean even smaller lamps. It is possible that a single LED chip emitting white light could produce luminous flux of 1,400 lumens. At just under 22W electrical power, this LED achieves a luminance of more than 200 megacandelas per square metre (Mcd/m^2). It thus offers three times the brightness of LEDs integrated in headlamps previously, which has ranged between 60 and 80Mcd/m^2. This can be achieved through tuning all the important components of the light source – from the central LED chip and a suitable ceramic converter for the additive mixing of white light, to heat management. In this situation, all components must also be optimised, from the design of the crystal layer of the indium gallium nitride (InGaN) semiconductor material, which is important for the light yield, to a specially-developed converter ceramic with a very high heat conductivity.

The metal contacts required for operation are embedded in the chip beneath the light-emitting p-n layers. This means the contact structures do not obscure any of the light generated by the LED. This UX:3 chip technology alone produced an increase in light yield of approximately 15%.

New Projects

While adaptive LED headlamps have operated in the past with individually-controllable chips for each beam section, a new project is now focusing on LED chips with many light

Figure 3: Prototype design of a combined low-beam/high-beam headlamp based on one high-luminance LED each and reflectors measuring just 30mm x 50mm

points, where each pixel can be switched on or off individually. The project called µAFS (pronounced "micro AFS"), comprises a group of German companies working to create the foundation for a new class of energy-efficient LED headlamps, as the basis for adaptive front-lighting systems. This kind of adaptive headlamp supports the driver even more effectively with additional intelligent functions. The most important function is better illumination of the road, as the light beam distribution adapts actively to the traffic conditions depending on the driving and traffic situation without dazzling other road users.

The key technology that makes all this possible involves the integration of microelectronics and optoelectronics. Light points are defined during chip processing itself, to enable them to be linked directly with the control system. An electronic driver chip is bonded with the LED pixel chip, allowing individual current control to each pixel with a typical current of 15mA. To complete the LED pixel unit, the chip surface is structured, and a converter solution for creating white light with an excellent contrast ratio is attached. This can then be placed upon electrical, mechanical and thermal interfaces to produce a light engine. Two key aspects here are intelligent control and appropriate interfacing to the vehicle bus for controlling the high-resolution headlamp light source.

Figure 4: The µAFS demonstrator shows 1024 pixels controlled individually with this LED chip

Light Source Of Choice

The advances in LED development demonstrate why it is quickly becoming the light source of choice among automotive manufacturers, who want to compromise less on aesthetics yet increase the safety ratings of their vehicles.

Aside from rapidly diminishing dimensions with the same or brighter luminance, offering freedom in design, LED technology is opening multiple doors to increased awareness and safety for everyday drivers.

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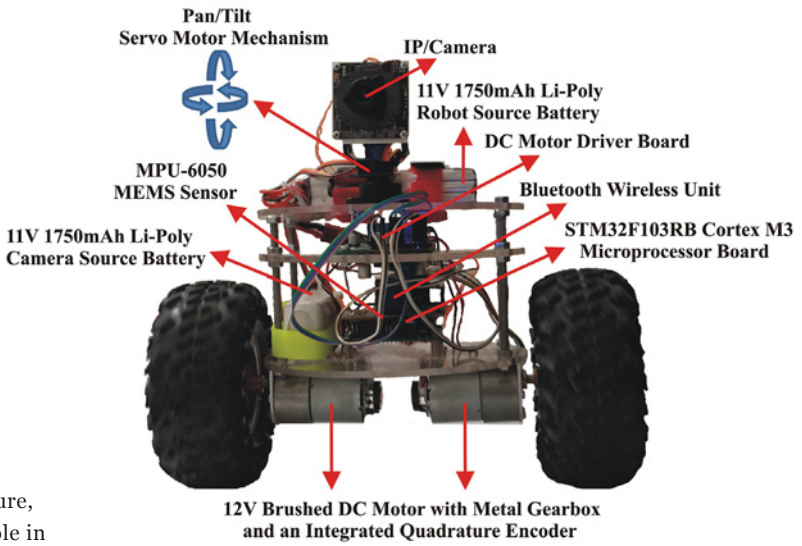
NOVEL MOBILE BALANCE ROBOT FOR ESTIMATING SURFACES

BY **ALI UNLUTURK** AND **OMER AYDOGDU**,
SELCUK UNIVERSITY, TURKEY

Figure 1: Two-wheeled MBR



Robot use is on the increase. In the near future, robots are expected to become indispensable in many fields, especially for helping people in the home, hospitals, offices, factories and so on.

One type of robot is the two-wheeled mobile balance robot (MBR), used by many researchers as a platform on which to develop software. A good mechanical design is a must for sensitive and stable balance control and motion planning in these robots, and carefully selecting the right balance sensor for its control is just as important. Gyroscopes and accelerometers are typically used, readily available on the market. However, their measurements also include noise, which can be minimized with sensor fusion algorithms such as simple, linear, extended or unextended Kalman filters.

The sensor used for balance control is of vital importance, and so is a high-speed microprocessor for overall robot control; see Figure 2.

Two-Wheeled MBR

MBRs are non-linear dynamic systems whose stable balance state and motion control algorithms are diffucult to develop.

A general-use MBR can operate many real-time control

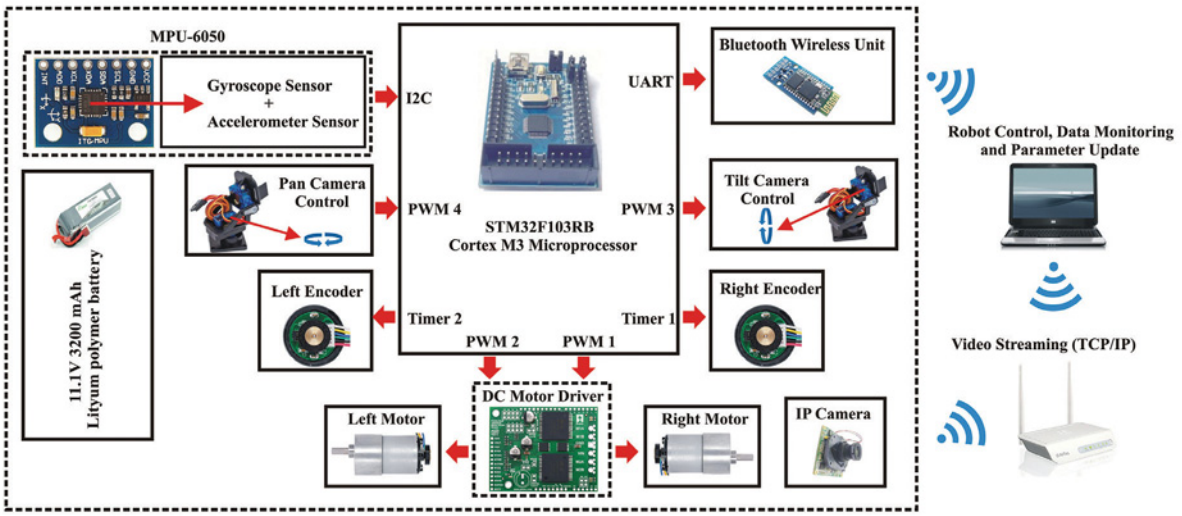


Figure 2: Block diagram of the control system

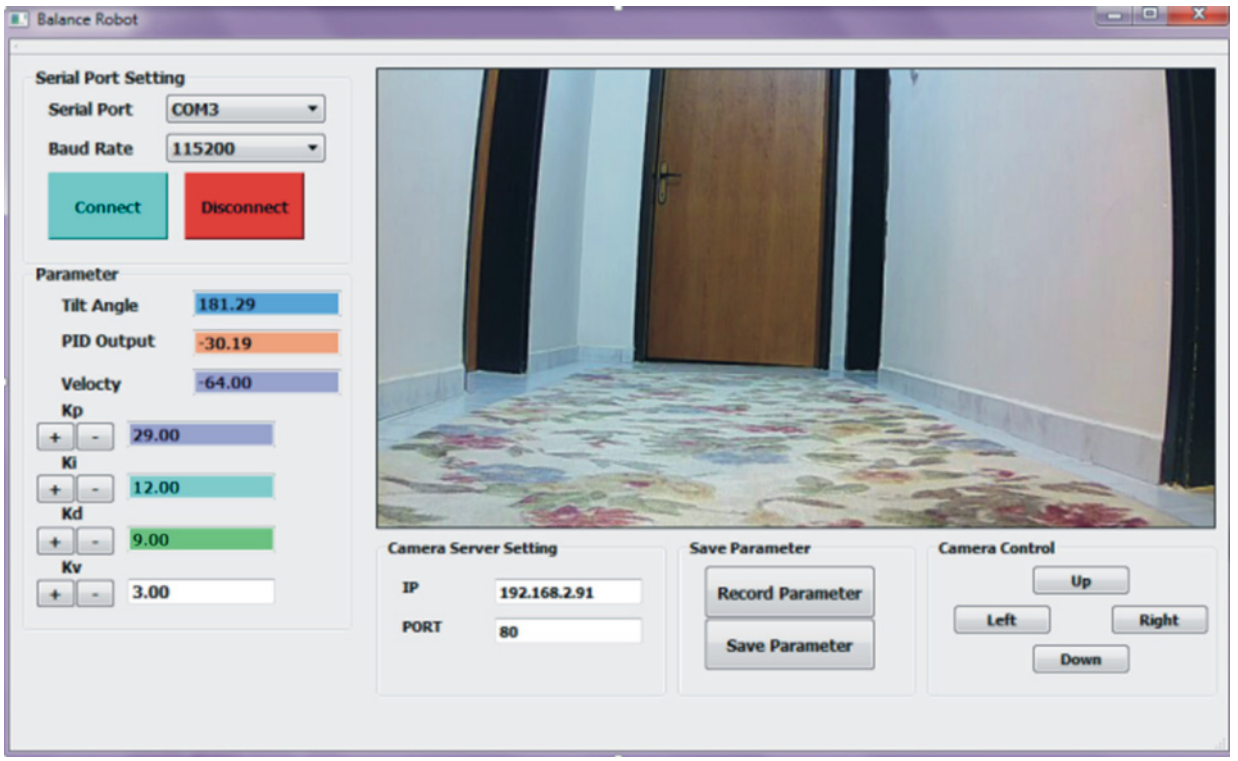


Figure 3: Control interface for balancing the robot

algorithms thanks to a well-developed control interface, including the classic Proportional (P), Proportional-Integral (PI), Proportional-Integral-Derivative (PID), Fuzzy Logic Control (FLC) and Sliding Mode Control (SMC) algorithms. However, there's always the opportunity to develop new control algorithms to further enhance the robot's control interface and its advanced hardware.

In this study, we've developed the robot control interface and surface estimation algorithm that will allow it to sense surfaces automatically using the feedback for autonomous motion control.

We started with the robot's mechanical design using 3D drawing programs. As seen in Figure 1, the MBR has three layers made of fibre glass material, with wheels and brush DC motors with gearbox on the bottom layer. There is also a Cortex-M3-based STM32F103RB microprocessor that controls the entire robot system, and a MEMS-based MPU 6050 sensor for balance control.

The second layer houses the dual-channel brush DC motor driver board and adjustable voltage regulator with 3.3V output. In the third layer there is 11.1V 3200mAh lithium polymer battery that provides power for the robot. There is also an IP-based camera that records video and transfers it to a PC via a real-time interface. The MBR's control system block diagram is shown in Figure 2.

PC-Based Robot Controller Interface

To control the system's balance effectively and compare the efficiency of the software algorithms, we use a well-known robot control interface, the classic PID control parameters. This will allow sensitive balance control, as some data needs to be observed in real time, such as the wheels' rotational speed, changes in robot tilt, its controller output and so on. Also, some controller parameters must be adjusted according to the robot controller algorithm.

All controller parameters can be changed even during the robot's operation. Wheel control and any changes in the robot's tilt are continuously observed and all data transferred to the PC, which records video via the IP camera. Motion control is done with the arrow keys on the PC. The video of this robot is available at https://www.youtube.com/watch?v=we37yBz9iys. The robot's control interface is shown in Figure 3.

Feedback Controller And Surface Estimation

MBR motion on different surfaces is rather difficult. It needs to sense the surface to control its own motion autonomously.

To sense different surfaces these robots need cameras, laser detection systems and/or radars. In this study we used an artificial neural network (ANN) based surface estimation algorithm for the robot to achieve its own surface identification. The more the robot uses this algorithm the better it gets at

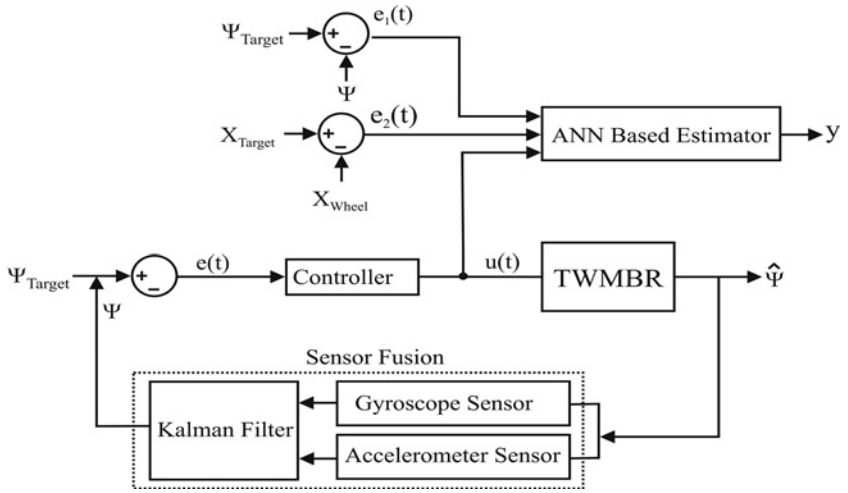


Figure 4: MBR's adaptive control block diagram with switching

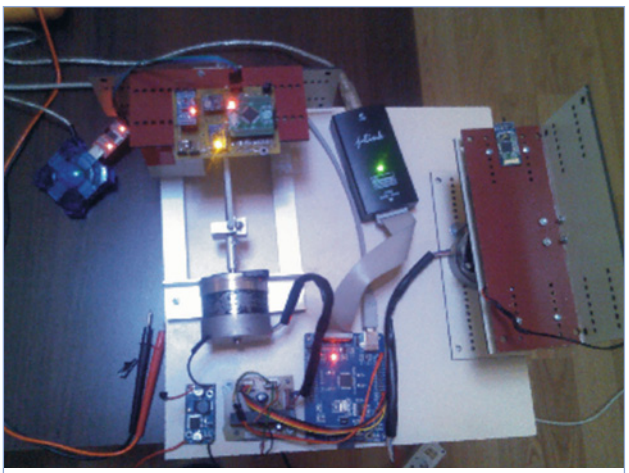


Figure 5: Sensor calibration mechanism

Figure 6: Surface estimation test platform

identifying/classifying the surface and adjusting its own motion, balance and stability. Figure 4 shows the robot's feedback controller structure.

In this figure, Ψ_{Target} (180°) expresses the target tilt angle, X_{Target} (0 cm) is the target linear displacement, $\hat{\Psi}$ is system output, Ψ defines the sensor fusion output, e(t) is the difference between Ψ_{Target} and Ψ, and y defines the ANN output.

The MPU-6050 balance sensor was used for the feedback structure, which also includes gyroscope and accelerometer sensors. The reason for using two different sensors is that they each have different advantages and disadvantages, and by comparing the two, the robot tilt angle can be estimated better. For example, the gyroscope sensor has a base drift value, which means that if we were to measure the system's stable motionless tilt angle (see Figure 5), the measurement will change with time. But, if we measured the structure's tilt angle with an accelerometer – which inherently suffers from noise – and changed the tilt angle by applying a bit disturbance on the system, then the accelerometer would interpret a tiny change as a big one.

For these reasons, we applied a linear Kalman filter as sensor fusion algorithm. There are different types of Kalman filter algorithms, such as extended, unexdended and quaternion. The Kalman filter draws the attention of many researchers due to its success in real-time applications, but it is also used actively for orientation measurement (yaw, pitch, roll) in the control of unmanned air vehichles.

As mentioned earlier, we used the classical PID controller algorithm to control the robot system. This is very easy to apply practically, but it's difficult to initially determine its parameters. For our system we determined the best PID parameters experimentally. We also ran various tests on uneven surfaces with a surface test platform, as shown in Figure 6. Robot balance

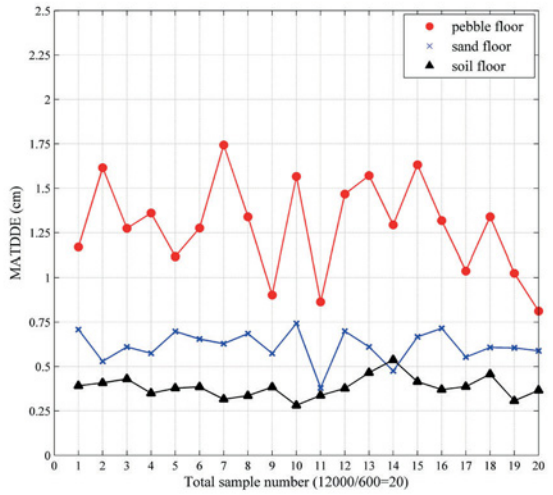


Figure 7: MATDDE range with respect to time on soil, pebble and sand surfaces

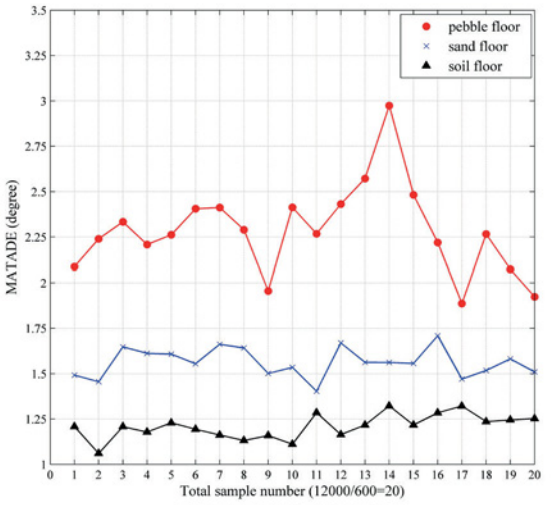


Figure 8: MATADE range with respect to time on soil, pebble and sand surfaces

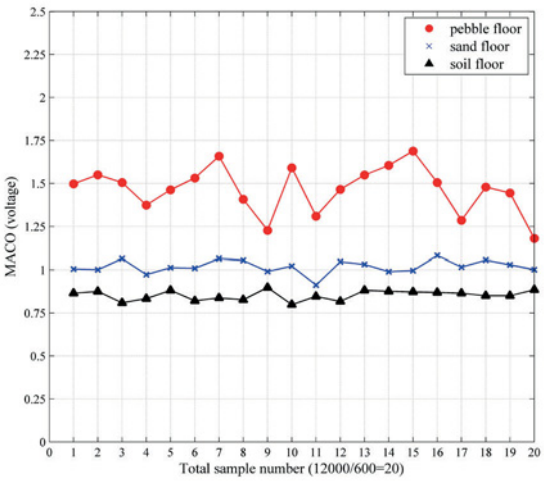


Figure 9: MACO range with respect to time

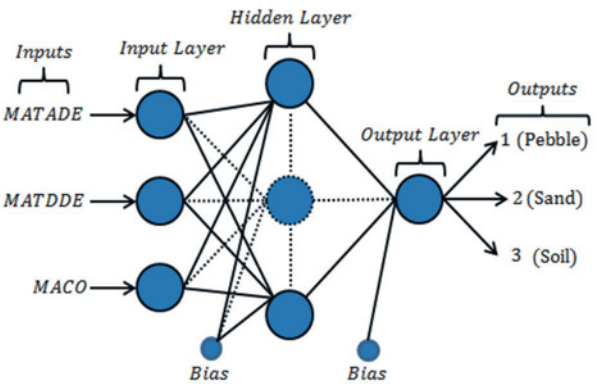


Figure 10: ANN model of the TWMBR control system

on each surface was tried individually with the same PID parameters, with each test lasting two minutes, withouth adding any additional disturbance to the robot.

In the first test we changed the robot's tilt angle, and established the distance and time it takes to adjust to the surface. To help with the surface estimation, we also used Mean Absolute Target Angle Deviation Error (MATADE), Mean Absolute Target Distance Deviation Error (MATDDE) and Mean Absolute Controller Output (MACO). Because of the robot's non-linear structure, N = 600 was chosen as a systematic sampling period for getting data from the robot. The MATADE, MATDDE and MACO equations are:

$$\mathrm{MATADE} = \frac{1}{N}\sum_{j=1}^{N}\left|\Psi_{\mathrm{Target}} - \Psi_{\mathrm{Output_j}}\right| \quad (1)$$

$$\mathrm{MATDDE} = \frac{1}{N}\sum_{j=1}^{N}\left|X_{\mathrm{Target}} - X_{\mathrm{Output_j}}\right| \quad (2)$$

$$\mathrm{MACO} = \frac{1}{N}\sum_{j=1}^{N}\left|U_j\right| \quad (3)$$

Therefore, we gained 20 meaningful data-points about the robot for each surface.

In Figures 7-9, the data (MATADE, MATDDE and MACO) was applied to the ANN's surface classifier structure. Following surface classification, prediction of the floor type is made by parameter adaptation mechanism. The model of the ANN structure used in this study is shown in Figure 10. So, autonomous balance and trajectory planning of the two-wheeled MBR in different environments was realized effectively.

POCKET IO PLC DEVELOPMENT PLATFORM FOR INDUSTRY 4.0

Maxim Integrated is launching the Pocket IO programmable logic controller (PLC) development platform for increased manufacturing productivity. The platform enables the smallest form-factor and highest power efficiency for next-generation PLC designs.

Lost productivity is a common concern for Industry 4.0 designers, who are challenged with keeping a manufacturing line running 24 hours a day, seven days a week. Without intelligent data available at their fingertips, factory operators do not have the insight to make informed, real-time decisions which can significantly improve uptime, revenue and gross margins. In addition to capturing real-time data, PLCs require fanless operation due to harsh industrial environments. As a result, highly efficient power solutions are required to minimize heat dissipation.

Maxim's Pocket IO PLC development platform provides real-time intelligence, fast data processing, adaptive manufacturing, distributed control and others.

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ELECTRO RENT EUROPE EXPANDS EMEA HEADQUARTERS BY 40%

Electro Rent Europe has expanded its headquarters in Mechelen, Belgium, as a direct result of its continued growth. Laboratory, warehousing and office space have been increased by 40% with more employees joining the company.

"As we are growing our business rapidly and more equipment is coming in, we need to be able to treat, inspect and ship equipment faster while maintaining a high level of quality," said Wouter Merckx, Operations Manager for Electro Rent Europe.

"We make sure our customers receive the best service and product possible. Our rental and used equipment is checked for functionality and completeness and calibrated in our A2LA accredited laboratory or by our approved vendors," he added.

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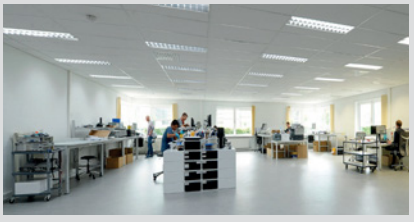

NEW BIPOLAR STEPPER AND HIGH-CURRENT DC MOTOR DRIVER IC

Allegro MicroSystems Europe has announced a new 40V motor driver IC capable of driving one stepper motor and one DC motor. The bipolar stepper driver outputs are rated up to 1.6A and the high-current DC driver at 3.2A.

Allegro's A5989 includes fixed off-time pulse width modulation (PWM) current regulators, along with 2-bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full, half, and quarter step modes.

This new device is targeted at the consumer, industrial and office automation markets with end applications that include point of sale, lottery, ticketing, laser, inkjet and label printers, copiers, vending and ATM machines.

The A5989 stepper driver PWM current regulator uses the Allegro patented mixed-decay mode for reduced audible motor noise, increased step accuracy and reduced power dissipation.

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Rittal now offers a new range of roof-mounted fans with superior efficiency, flexibility, protection and ease of use. Designed to reduce the costs associated with operation, installation and maintenance, the new fans are going to better protect the installed equipment with efficient cooling.

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NEW FLEXIBILITY IN SMD JUMPERS

Hitaltech has developed a range of PCB-to-PCB flexible SMD jumper cables that enable PCBs to connect at different angles. The new SMD jumpers are available in 0.5mm and 0.93mm pitch as standard, with increased pitch for higher power applications and improved co-planarity for reliable automatic pick and place and reflow soldering.

"Hitaltech is one of the first companies to develop a custom made SMD flexible jumper system," explains Hitaltech's MD, Andrew Fitzer. "That flexibility makes a huge difference to our customers. With mixed pitches and even custom lengths, we've found a way to give our customers greater power when connecting together their PCBs."

The new SMD jumper cables are aimed at high volume production for clients who might be using thousands or even a million+ pieces each year.

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Geyer eK moved to their Headquarters in Gräfelfing, in the west of Munich, in 2002 where they were able to benefit from the access offered by the Autobahn routes, and opened a Design and Test Center in 2011 to develop the crystal products and to work with clients on custom-designed solutions for their applications. Since that time, the Design Center has been expanded and now offers a comprehensive consultation service from our team of five Application Engineers, providing design validation, custom samples and prototype devices, and 3D models of our components to help customers' engineers during the design stages. We also offer the unique Y-Quartz App to help Design Engineers select the optimum crystal specifications to work in their system, supported by advice from our Application Engineers if requested.

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Manufacturing, engineering and sales are situated in a custom-built modern facility in Crewkerne, Somerset, UK from where a comprehensive range of frequency control products is also offered. The recently upgraded facility enables Euroquartz to perform full military screening tests and qualification testing on all other products in the company's portfolio.

The test capabilities of the facility include accurate frequency measurement, temperature cycling, acceleration testing, gross leak, fine leak, filter characteristic testing as well as active burn-in routines. Custom crystal selection testing is also offered from the Euroquartz test facility.

Founded in 1982, the company has a wealth of experience and technical knowledge making it a leading specialist in the field of frequency products. Customer service and quality are the main driving forces behind the business, a fact clearly demonstrated by the company's AS9100 quality certification awarded in 2015.

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Today, Apacer offers a large portfolio of innovative Solid State Drive Solutions (SATA, PATA, Flash Cards and USB) and DRAM Solutions (desktop, notebook and server) for the industrial and embedded markets. More recently, Apacer developed a range of data security technologies by launching data security enhanced products and unique value added features.

One of our strengths lies in its customization capabilities: its industrial SSD line offers a wide range of different specifications in terms of size, angle, thickness and functions such as high capacities with strong performance, wide temperature support and shock- and vibration resistance for various industries: military, aerospace, networking, medical, automation, gaming etc.

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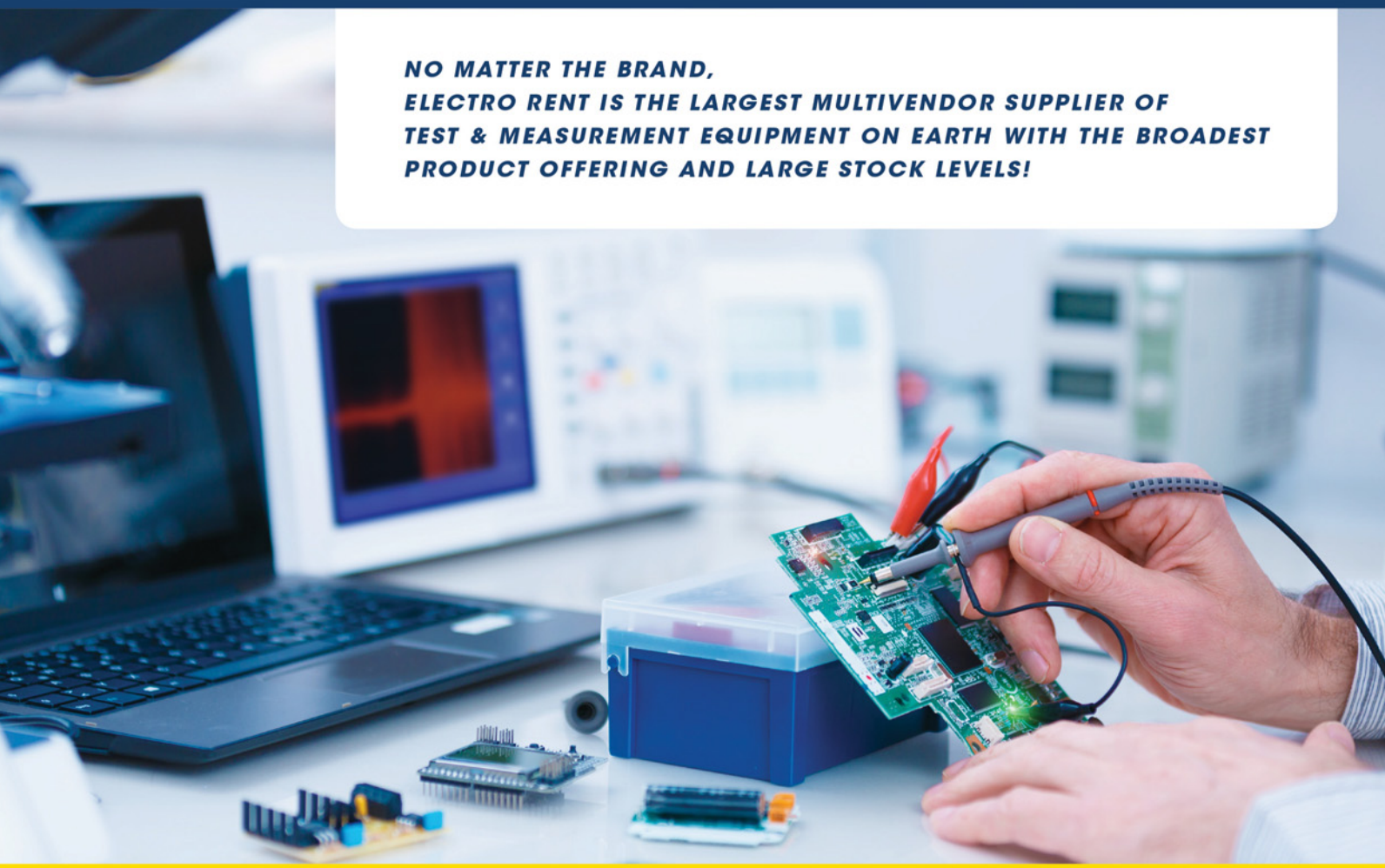

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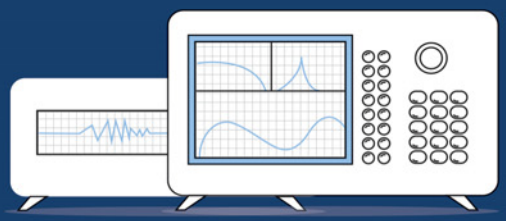

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