February 2017
Volume 123
Issue 1969
£5.90

www.electronicsworld.co.uk

Electronics WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

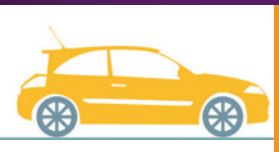
Complete Test and Analysis of Power Behaviour with One Instrument

from Teledyne LeCroy

TELEDYNE LECROY
Everywhereyoulook™

SPECIAL REPORT
DIGITAL ELECTRONICS

NEW REGULAR COLUMNS:
- Vision-Based System Design
- Inside Frequency Control



Technology
Fully autonomous driving is on its way

Semiconductors
Process detection and variability

Products
Hall sensors, LED light systems and Industry 4.0

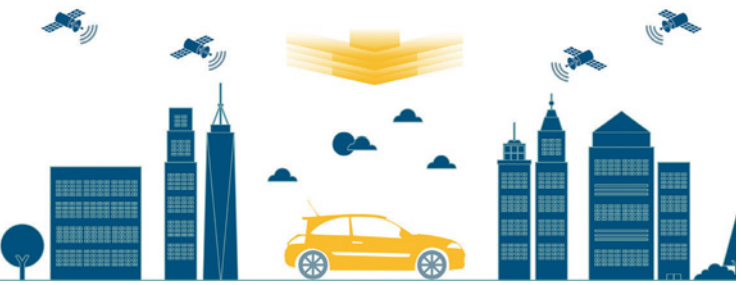
More new products **in stock** than any other distributor.

Order now at
mouser.co.uk

MOUSER ELECTRONICS

The Newest Products for Your Newest Designs®

08



Cover supplied by TELEDYNE LECROY
More on pages 10-11

REGULARS

FEATURES

Microchip Announces Ultra-low Power, Ultra-small MEMS Oscillators

Experience the Perfect Balance Between Power & Performance

Combining industry-leading low power consumption with exceptional frequency stability and jitter performance over temperature, in the smallest surface-mount packages, Microchip's DSC6000 MEMS oscillators excel as clock references in small, Battery-powered and industrial or automotive applications. The family achieves less than half the current consumption of the lowest-power quartz-based oscillators as well as withstanding 500x more shock and 5x more vibration. The extensive range of configurable performance parameters enable dynamic adjustment during operation and the family offers stability of 25ppm across an extended temperature range.

ClockWorks® CONFIGURATOR

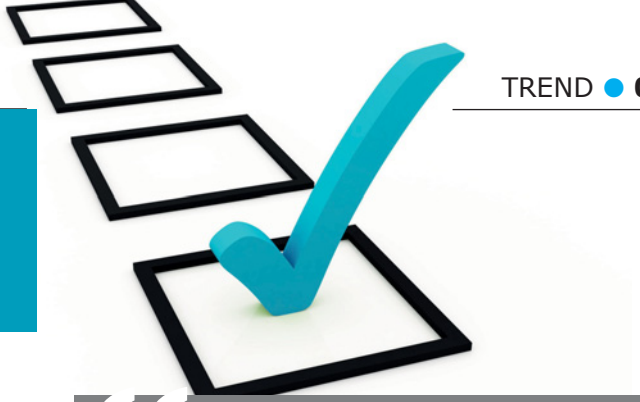
- 1.6 x 1.2 mm, 75% broad space saving
- 50% less power consumption than the lowest-power crystal oscillator
- High stability over a wide temperature range (±25 ppm over –40° to 85° C)
- AEC-Q100 qualified
- Online and field programmable

microchip DIRECT
www.microchipdirect.com

MICROCHIP

www.microchip.com/eudsc6000

2017 TELECOM TRENDS



In 2016 operators worldwide started to focus on network functions virtualization (NFV), as they hoped to drive efficiencies and move to a more flexible Internet Protocol (IP)-based communications model. In 2017, operators will realize the benefits of those network upgrades to serve specific purposes: we will see all-IP communications, such as Wi-Fi calls, become more prevalent as operators lay the foundations for mass-market rollout of VoLTE (voice over LTE).

Year 2017 will also bring more mergers and acquisitions, as operators look to acquire content providers. Mobile operators will offer unique content packages, as they make the shift to become multi-play businesses, able to provide content services at any time to subscribers anywhere.

Operators are now choosing to work with network equipment vendors, developing virtualized functions that are designed to run exclusively on their own NFV platforms to serve a specific vertical function, such as billing or firewalling, with robust network functionality being the primary driver. This approach could perhaps be described as network function 'verticalization'.

Meanwhile, at the service layer, where new real-time voice and video services are developed, we will see operators seeking to avoid vendor-locked NFV solutions. This is because such solutions engender service dependency on a single vendor, limit flexibility and tend to stifle further innovation. Therefore, at the service layer at least, there will be a more open approach to NFV, with operators selecting best-in-class solutions. With this approach we are likely to see a host of new voice and video services developed by operators.

In 2017 there will be more affordable VoLTE- and VoWiFi (voice over Wi-Fi)-enabled handsets, which will support services from any native operator in the region straight out-of-the-box, without the need for downloading firmware updates or activating a service. As a result, the mobile network will automatically direct users to the most applicable access network for their voice and video calls, whether it's Wi-Fi or LTE, with the process remaining transparent to the user. Subscribers will become accustomed to such ready access to rich voice and video services, which will increase service adoption.

Home security, self-regulating supply chains and autonomous vehicles are the main applications expected to drive IoT in 2017. Consequently, we can expect to see an increasing number of partnerships between operators and industry-specific IoT suppliers to address the requirements of these vertical sectors.

> Home security, self-regulating supply chains and autonomous vehicles are the main applications expected to drive IoT in 2017

In 2017, we will see software for these applications running over a virtualized service layer. Interoperability building-blocks and geographic coverage will be key drivers for such IoT/operator technology partnerships.

Service Agility

During 2016 we frequently heard the word 'agile' in the context of service development within telecoms operations. In 2017 we can expect conversations about 'agile service development' to move from R&D and into the boardroom, as operators start to adopt new business models for rapid development and monetization of their innovations.

Operators will introduce virtualized service development environments more flexible and open than traditional approaches, which were predicated on fixed hardware. These new environments will allow operators to gain the agility typified by Internet players, enabling them to empower their customers in new ways. This is especially important given the impact of Internet services on operator revenue streams. We can expect more 'Agile MNOs' challenging the traditional way operators have offered services to customers, with a wider range of differentiation.

Death Of The Dumb-Phone

In 2017 we are going to see the death of the dumb-phone as the market becomes flooded by entry-level smartphones supporting rich applications and services. We will also see more low-cost smartphones on the market, supported by services specific to demographics; for example, phones that support device-to-device money transactions in Africa. Such services will become key differentiators, and subscribers will make their purchases based on those unique set of services.

Chris Haddock is Head of Marketing at OpenCloud (www.opencloud.com)

EDITOR:
Svetlana Josifovska
Tel: +44 (0)1732 883392
Email: svetlanaj@sjpbusinessmedia.com

SALES:
James Corner
Tel: +44 (0)20 7933 8999 | Mobile: +45 93 86 42 65
Email: jamesc@electronicsworld.co.uk

Philip Woolley
Tel: +44 (0)20 7933 8989
Email: philipw@sjpbusinessmedia.com

DESIGN: Tania King

PUBLISHER: Wayne Darroch
ISSN: 1365-4675

SJP business media
2nd Floor,
52-54 Gracechurch Street,
London, EC3V 0EH

PRINTER: Buxton Press Ltd

SUBSCRIPTIONS:
Subscription rates:
UK - 1 year digital only £53.00+VAT
UK - 1 year print and digital sub £68.00
UK - 2 year print and digital sub £109.00
UK - 3 year print and digital sub £143.00
International - 1 year digital only £53.00
International - 1 year print and digital sub £164.00
International - 2 year print and digital sub £290.00
International - 3 year print and digital sub £409.00
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com
www.electronicsworld.co.uk/subscribe

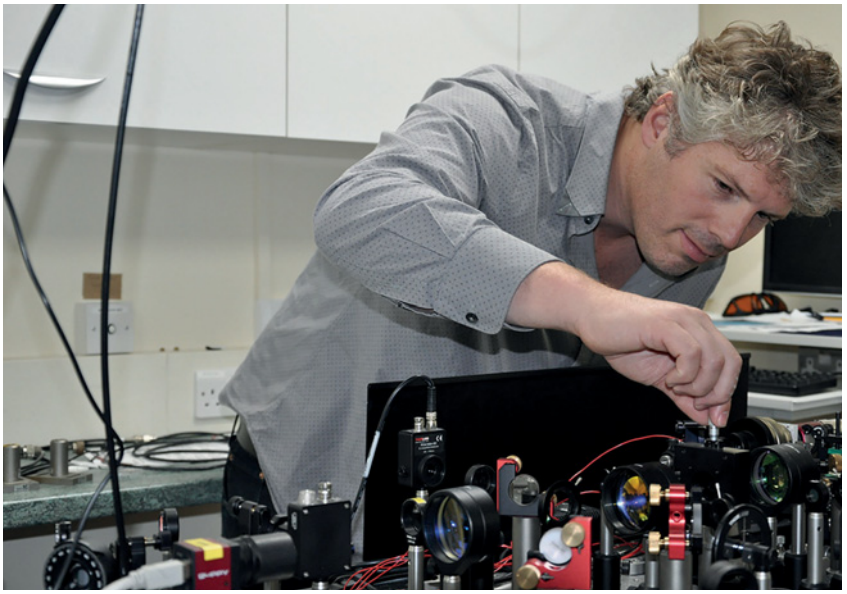
Follow us on Twitter @electrowo

Join us on LinkedIn

NANOANTENNA LIGHTING-ROD EFFECT PRODUCES FAST OPTICAL SWITCHES

A team of scientists led by the University of Southampton have produced a fast nanoscale optical transistor using gold-nanoantenna-assisted phase transition, opening up new directions in antenna-assisted switches and optical memory.

Small nanostructures that can interact strongly with light are of interest for a range of emerging new applications, including small optical circuits and metasurface flat optics. Nanoantennas are designed to have strong optical resonances where energy is concentrated well below the diffraction limit, the smallest scale possible using conventional optics. Such extreme concentration of light can be used to enhance various effects related to localised energy conversion and harvesting, coupling of light to small molecules and quantum dots, and generating new frequencies of light through nonlinear optics.



Next to the precise tuning of these antennas by design, an ability to further actively tune their properties is of great interest.

"If we are able to actively tune a nanoantenna using an electrical or optical signal, we could achieve transistor-type switches for light with nanometer-scale footprint for datacommunications," said Professor Otto Muskens of the University of Southampton.

The Southampton team used the properties of the antenna itself to achieve low-energy optical switching of a phase-change material. The theoretical modelling was done by a team from the University of the Basque Country in San Sebastian, Spain. Their detailed calculations revealed that the nanoantennas provided a new pathway by local absorption around the antenna. The antenna-assisted mechanism resulted in a much lower switching energy than other devices, corresponding to picojoule energies and a calculated efficiency of over 40%.

"We could achieve transistor-type switches for light with nanometer-scale footprint for datacommunications" – Professor Otto Muskens, University of Southampton (pictured)

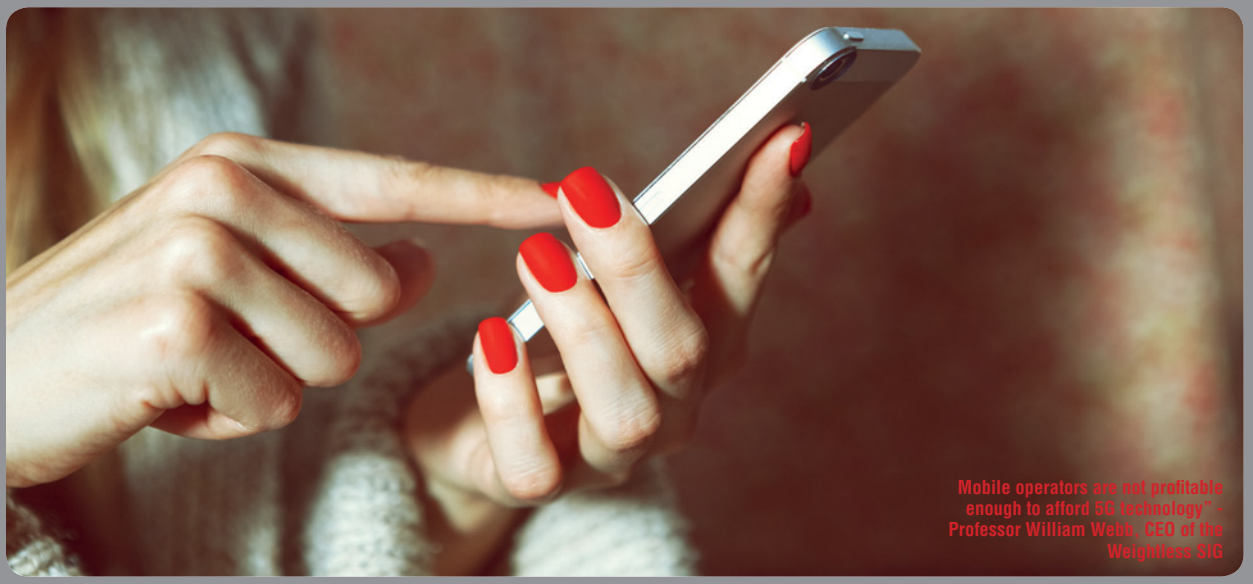
5G IS A MYTH, SAYS INDUSTRY LEADING PROFESSOR

"The 5G vision is flawed", says Professor William Webb, one of the world's leading wireless communications experts, deputy chair at Cambridge Wireless and CEO of the Weightless SIG.

In his book 'The 5G Myth', Professor Webb debunks the need and business case for 5G; he says that rather than heralding a huge advance in global connectivity, users will simply not value the higher data rates promised and won't need the higher capacity forecast. Equally, he argues that technological advances are insufficient to deliver 5G and mobile operators are not profitable enough to afford it.

"Despite the clearly flawed case for 5G, it is not in the interests of any stakeholder to point it out because they all benefit from the interest, funding and potential that 5G promises," said Professor Webb. "But there is an alternative vision where industry focuses on consistent connectivity everywhere rather than unnecessarily fast speeds in city centres."

Professor Webb has over 100 papers, 18 patents and 14 books under his belt. He led the design of the Weightless standard and helped form the associated standards body where he continues as CEO, authoring the UK Spectrum Framework Review whilst at Ofcom, designing the GSM-R technology for the European railways and inventing variable level modulation – a technique used in almost all radio systems today.



Mobile operators are not profitable enough to afford 5G technology" – Professor William Webb, CEO of the Weightless SIG

PROJECT 'ESCAPE' TO SET THE TONE FOR AUTONOMOUS DRIVING ON EUROPEAN ROADS

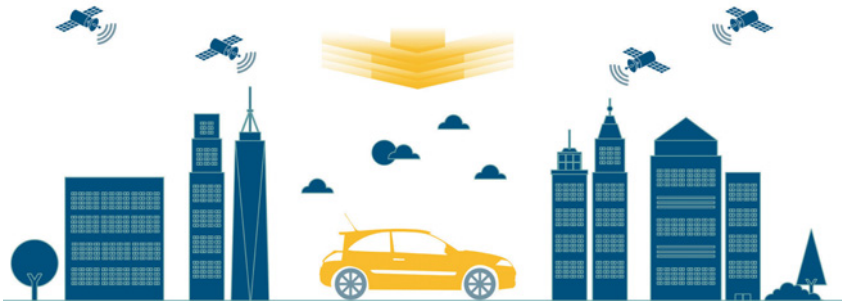
The European Agency for global navigation satellite systems (GSA) has launched ESCAPE, a three-year €5.4M project to use the European satellite navigation system Galileo for automated driving. ESCAPE (European Safety-Critical Applications Positioning Engine) will involve some of the most prominent companies and research institutions in Europe to create a positioning engine for road-safety critical applications in fully automated driving.

ESCAPE is led by the Spanish company Ficosa in collaboration with GMV from Spain, Renault and IFSSTAR from France, and STMicroelectronics and Istituto Superiore Mario Boella from Italy. By 2019 the consortium is expected to finish the development of an innovative positioning engine tailored to meet the paramount safety requirements for road transport applications that involve automation.

Key element of this innovative positioning device is the mass-market GPS+Galileo receiver chipset with multi-frequency capability tailored for the automotive sector. ESCAPE will enable a high-grade data fusion between different, numerous vehicle sensors and other technologies, such as the Precise Point Positioning (PPP) service and Galileo's ionospheric model, all fused by an integrity layer, to assess the degree of trust one can associate with the information provided by the device.

Using an integrity layer is crucial: in safety-critical applications it is often said to be more important to know whether information is reliable or not, than the precise information itself.

ESCAPE is expected to set a new trend in technologies for vehicle automation, since it is integrates multiple sources of positioning information, including satellite constellations, on-board sensors and maps, and high-accuracy services.



The ESCAPE setup will aid fully-autonomous driving by integrating multiple sources of positioning information, including satellite constellations, on-board sensors and maps, and high-accuracy services

AUGMENTED REALITY PLATFORMS COULD ADD £1BN TO UK'S RETAIL MARKET

The UK's retail market could benefit from up to £1bn per year, says research, if consumers were given access to visualisation technology that allowed them to see how products may look in their own homes before buying.

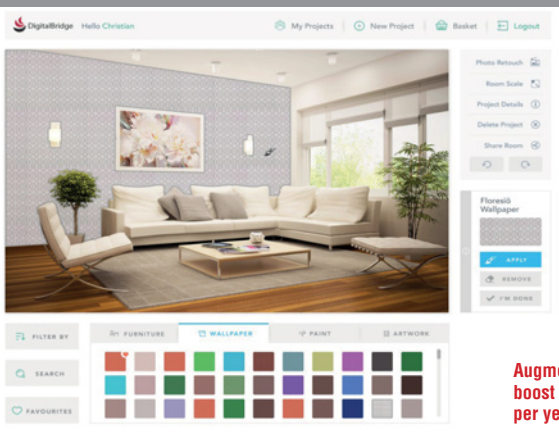
Virtual (VR) and augmented reality (AR) platforms are widely tipped to be the standout technologies of 2017 thanks to high-profile successes by the likes of Sony and Google.

New research commissioned by Manchester-based technology company DigitalBridge states that more than a third of consumers have walked away from making purchases in the last 12 months, just because they couldn't imagine what products such as furniture, wallpaper and new flooring would look like in their homes. This "imagination gap" has emerged as a serious concern for UK retailers, particularly those selling home interior products, with 56% of homeowners planning to make some kind of home upgrade in 2017 with budgets ranging from £500 to over £3,000 per project.

"With as much as £1bn of revenue up for grabs in the home décor market alone, retailers can no longer overlook the value of virtual and augmented reality as a commercial tool," said David Levine, CEO of DigitalBridge. "These types of visualisation tools could be the 'undo button' to home interiors that consumers have been calling for. Just imagine the benefits a customer would get from a retailer that allowed them to preview any product they wanted using nothing more than a picture taken on a smartphone."

VR and AR technologies are not just limited to the home interior market, they have potential to completely revolutionise all types of sectors, from fashion and architecture to real estate. UK's John Lewis and other major retailers are already investing in smaller start-ups that can help them bring AR platforms to market.

"With so much uncertainty already swirling around about the future of UK retail, businesses need every advantage they can get to remain competitive, especially those competing for attention on line," added Levine.



Augmented reality may boost UK retail by £1bn per year

PEAK® electronic design ltd

2 Year Warranty as standard

UK designed **and** manufactured

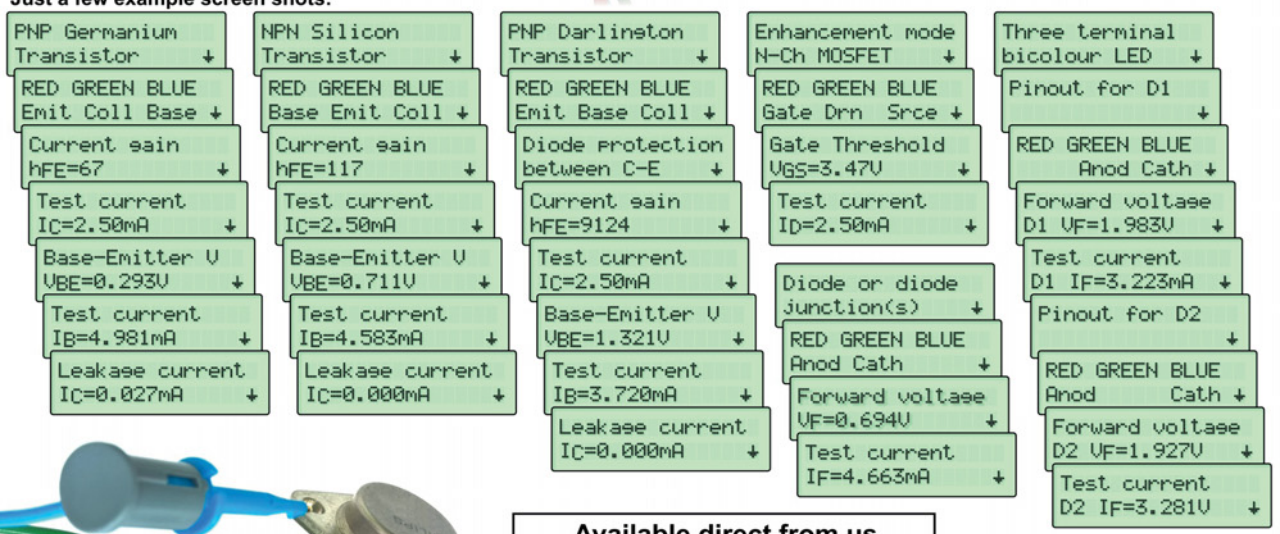
Atlas DCA - Semiconductor Analyser model DCA55

Now with backlit display and AAA battery!

- Connect any way round.
- Automatically identify component type.
- Automatically identify pinouts.
- Supports Transistors, MOSFETs, Diodes, LEDs and more.
- Measure transistor gain (h_{FE}).
- Measure V_{BE} (now 1mV resolution!)
- Measure leakage current.
- Measure MOSFET thresholds.
- Measure LED voltages.

Designed in the UK and made in the UK.

Just a few example screen shots:



Universal test clips for large and small components

Available direct from us and from our distributors:

RS · maplin (The electronics specialist) · Rapid electronics · Farnell

Peak Direct Price:

£48.00

(£40.00+VAT)

Peak's insured UK delivery £3.00 inc. VAT

It's only possible to show summary specifications here. Please ask if you'd like detailed data. Further information is also available on our website. Product price refunded if you're not happy.

E&OE

Tel. 01298 70012
www.peakelec.co.uk
sales@peakelec.co.uk

Atlas House, 2 Kiln Lane
Harpur Hill Business Park
Buxton, Derbyshire
SK17 9JL, UK

Follow us on twitter for tips, tricks and news.
@peakatlas

COMPLETE TEST AND ANALYSIS OF STATIC AND DYNAMIC POWER BEHAVIOR WITH ONE TEST INSTRUMENT

Motor Drive Analyzers provide complete three-phase power analysis from motor drive input through motor mechanical output, with results in a convenient Numeric table format. Motor speed, position, and torque integration are the most complete available. Long memory, per-cycle "synthesized" Waveforms and Zoom+Gate mode provide powerful dynamic drive and motor analysis. 8 analog input channels (MSO optional) with high resolution (12-bits), sample rate (up to 2.5 GS/s), bandwidth (up to 1 GHz) and memory (up to 250 Mpt/ch) provide unique capability to perform complete system debug on the motor drive power section, motor mechanical performance, and embedded drive control system operation.

Power electronics is one of the fastest growing electronics market segments, with growth driven by government mandates for motor efficiency, "green" (environmental) initiatives, and complex control requirements. Power electronics are commonly used in a variety of power conversion devices such as switch-mode power supplies, DC-DC converters, AC-AC drives, and DC-AC inverters. Higher power (1 kW) and/or three-phase power conversion devices typically utilize complex embedded control designs to regulate performance, and these complex embedded control systems can contain very high speed (100s of MHz) microprocessors with mixed-signal (analog, digital, serial data) interface architectures. Power Analyzers have been the tool of choice for measuring input/output system power consumption and efficiency, and oscilloscopes have been utilized for embedded control and system debug. However, several new developments are occurring that could change the existing test paradigms.

Image1: The Motor Drive Analyzer provides an extensive range of capabilities to allow you to debug your three-phase power electronics or motor drive design faster than ever before

Complete Drive System Debug

A complete drive system is a complex mix of three-phase power electronics, motor/mechanical analog and digital sensors, and embedded controls, with a complex variety of analog, digital, serial data and pulse-width modulated (PWM) signals. The HDO8000 oscilloscope with Motor Drive Power Analyzer software permits waveform captures from the drive power section, individual power transistors, and embedded control system, and performs coincident three-phase power analysis of the power section waveforms in one high-performance instrument, enabling debug and analysis of all aspects of the complete motor drive

Numeric Power Table

A user-configurable table is provided for display of a selection of power (real, apparent, reactive), power factor, phase angle, efficiency, voltage, current or motor mechanical parameters. Up to 120 values total may be displayed in 10 rows and 12 columns for any selection of input or output individual phase or total three-phase values, DC bus/link, or motor mechanical. Efficiency can be also be displayed. The Power Table values displayed are mean values from a statistical data set that is calculated on a "per-cycle" basis using a user-defined synchronization source signal. This display corresponds to what is normally provided by a power analyzer.

Per-cycle "Synthesized" Waveforms

A single averaged value "hides" dynamic behaviors. Simply "touch" the value in the Numerics table and a detailed percycle Waveform will be created from the complete per-cycle measurement set and then automatically displayed timecorrelated to the original acquisition or zoomed areas of the acquisition. Statistical values (min, max, number,

etc.) can also be displayed. Use this advanced capability to correlate complex drive behaviors to other control or power system waveforms, and to debug drive system problems. This capability is not provided in any Power Analyzer instrument.

Motor Mechanical Integration

The combination of analog and digital inputs on the HDO8000 series of mixed-signal oscilloscopes provides more motor integration capability than a power analyzer. For instance, not only can standard analog and digital (pulse) tachometers be integrated for speed sensing, but analog Resolvers, digital Quadrature Encoder Interface and Brushless DC Hall Sensors may also be used to provide speed, direction, and absolute position information, not normally possible with a power analyzer.

Zoom+Gate Mode

Enable Zoom+Gate mode to create zooms of all channel acquisitions and gate the numerics and statistics measurement tables to the zoomed area. Per-cycle displayed Waveforms will be zoomed and time-correlated to the other Zoomed waveforms. Change the zoom location and size and the data will instantly update. Scroll quickly through your measurement set to gain fast and deep insight into drive and control system behaviors.

Dynamic Drive Response

The long acquisition memory in the HDO8000 (up to 250 Mpts/Ch) provides unique capabilities for motor and drive dynamic response analysis. For example, 25 seconds of continuous acquisition capture is possible at a sample rate of 10 MS/s. This permits complete understanding of dynamic drive behaviors, such as startup, application of load, or fast changing load conditions, and correlation of drive response problems to control system instructions or power section failures

Flexible Setup Capability

The eight analog input channels provide capability for direct measurement of three voltage and three current signals from a drive input or output. However, support is provided for a two-wattmeter measurement method for three-phase power, which allows three-phase measurements to be made using two voltage and two current signals. Therefore, input/output efficiency measurements of a complete drive can be performed using the eight analog input channels. Support is also provided for a line-line to line-neutral voltage conversion so as to allow intuitive line-line probing with per-phase line-neutral reported results.

teledynelecroy.com

Image 2: This two second capture shows the drive output waveforms on the left and the Torque, Speed and Mechanical Power Waveform per-cycle values over time are shown to the right

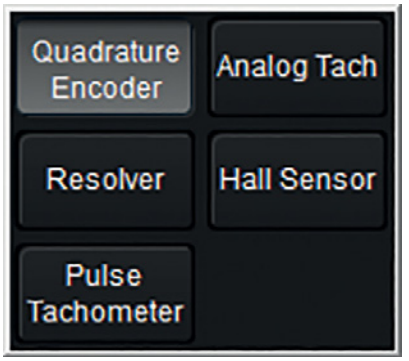


Image 3: Use sensors to provide speed, direction, and absolute position information

Image 4: This 480V drive has 10 second acquisitions for the AC Input and Drive Output (on the left) and on the right is shown power, efficiency and power factor Waveforms over time.

Electronica 2016: about new AVR and finding LoRa

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

I am writing this piece as the Electronica 2016 exhibition closes its doors. This bi-annual event has been held in Munich, Germany, for more than 50 years to become a mainstay of the electronics industry. I have been attending it for the past 15 years, presenting products to customers and press on behalf of Microchip. I thought this year the Microchip stand was busier than other year, and my belief is this is because of its recent, large acquisition...

Long Live AVR

Last year Microchip bought Atmel. This may have been Microchip's 17th acquisition in the last few years, but by all means it was the largest!

Much to the surprise of most Atmel aficionados, at Electronica Microchip already announced the immediate availability of a brand new generation of AVR devices – the tiny817 family, securing the future of the AVR architecture under its ownership. If the acquisition announcement made anybody worry about Microchip's intentions, the new silicon, tools and boards it presented at Electronica gave a pretty strong testimony of its continued commitment to the 8-bit market and the AVR product family.

Prior to the acquisition, most developers had noticed lack of new AVR (8-bit) announcements from Atmel, as the biggest spend was directed to its 32-bit portfolio. Microchip changed that, and we are now told that the number of designs dedicated to new AVR products has been more than tripled.

A more complete review of the innovative ideas introduced by the original design team of the AVR in Norway into the new tiny817 would take more space than I can afford here, but it should suffice to say that a lot was borrowed from the previous XMEGA generation and squeezed into a much smaller (14-/20-pin) package.

Xplained demo boards featuring the new tinyAVR are already available at most catalogues and distributors, and a new, rapid development tool called START, previously available only for 32-bit devices, has now been made available to the tinyAVR users. This is not too dissimilar from the PIC rapid development tool known as the MPLAB Code Configurator (MCC), so I promise a more in-depth review on this subject in the future.

Almost in parallel (a week prior to the show), and perhaps inevitably, Microchip had just launched yet another family of 8-bit PIC microcontrollers. This time it was the PIC18 architecture that received the Core Independent Peripheral "treatment" with the introduction of the PIC18F K40 series.

However, the novelty and excitement was simply all on the AVR side!

Finding LoRa

Among Electronica's 13 halls, packed with the latest and greatest products and solutions, there were definitely a few very recognizable trends. In automotive, for example, all lights where pointed at electric vehicles, with a great deal of focus on charging: faster, better, smarter and even wirelessly. Tesla cars were featured at more than one booth, but also a great number of new product announcements were targeting vehicle connectivity, where MOST and IP-based solutions are starting to merge.

Of course, the Internet of Things (IoT) hype was everywhere, and although some are already claiming we are past the peak – perhaps due to the recent news of hordes of baby monitors being hijacked and used to take down the Internet – judging from the show, one would have never guessed it.

Perhaps the one bright new star in this chaotic firmament was LoRa and its protocol. The LoRa Alliance is an open, non-profit association of industry partners focusing on IoT, with the mission to standardize Low Power Wide Area Networks (LPWAN). Whilst not exactly new, this long-range and low-power radio technology was introduced by Semtech at Electronica 2014, and it has now proven to be able to capture the attention, imagination and investment of a large portion of the embedded community – and rightly so!

Technically speaking, LoRa is based on a spread spectrum radio technology (previously an expensive option available only to military applications) that allows for extremely high receiver-sensitivities, up to 140dBm. Although there are several important technical

innovations involved, this unprecedented sensitivity alone is the reason for most of the excitement surrounding this technology. In fact, it enables long-range communication (in the order of kilometers) with power budgets typical of energy-harvesting systems or (very) short-range radios.

LoRa was very prominently featured at several semiconductor manufacturers' booths and almost every single one of the RF module/solutions exhibitors. So, finding LoRa at Electronica 2016 was not difficult.

My main concern with this technology is rather that I see already how a certain amount of hype is starting to build around it. As the customers' attention is easily captured by the promise of low power and long range in a license-free band, it is easy to lose sight of the fundamental laws of physics that even a clever spread-spectrum technology cannot circumvent.

In particular, as the transmitter power is reduced to conserve energy and the receiver is made powerfully sensitive to achieve range, something else has to give and, in this case, that "something else" is bandwidth!

Theoretically, a LoRa module can transmit short bursts of data at 250kbit/s, but the accent is on "short", since only a few bits/bytes can actually be (legally) sent every minute/hour to respect the FCC and EU duty-cycle limitations imposed on that same, free, radio band. Worse, a good amount of those bits will be eaten up by preambles (and other portions of the protocol), further reducing the actual data-payload size.

Such details are easily omitted/missed in much of the marketing messaging surrounding LoRa, and will invariably end up disappointing some prospective adopters, once they get past the hype.

More conscientious developers might instead discover the benefits of the clever LoRaWAN protocol that builds on top of the radio physical link layer and provides a sort of virtual MAC that takes advantages of the Internet infrastructure to provide a truly open and interoperable mechanism where LoRa gateways are not only allowed but encouraged to cooperate and share their resources/services. This openness is in stark contrast to the close and centralized nature of the (only) competing technology known as "sigfox".

The greatest champions of LoRa philosophy, and in my opinion the most powerful forces in this industry, is the gang known as 'The Things Network' or simply TTN. They have created partnerships with several semiconductor and radio equipment manufacturers, single-handedly deployed a network of gateways providing a free LoRaWAN infrastructure for all users (professional and amateur), galvanizing a huge community of hackers and developers all over Europe. Stay tuned for further information in the near future! ●

Wireless functional electronic stimulation device

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

Drop foot is a common problem caused by total or partial paralysis of the common peroneal nerve, which may be a result of stroke, multiple sclerosis, cerebral palsy, spinal cord injury, or spinal cord trauma. Drop foot is identified by the inability to lift the foot when it is brought forward during the gait swing cycle, causing a dragging foot when walking.

There is help however: Functional Electrical Stimulation (FES) is the application of electrical pulses to certain nerve points where functions have been partially or completely impaired. FES is an electronic device that generates pulses with correct amplitude, frequency and duration to stimulate the damaged nerves.

In a typical application, external electrodes energized by an electronic device are placed above the peroneal nerve. The pulses make the tibialis anterior muscle contract during the swing phase of the gait cycle, hence helping the patient lift the foot, preventing it from dragging.

Here we discuss the design of a microcontroller-based wireless stimulator device, called FootCorrect, for correcting drop foot. The system comprises foot sensors, microcontroller-controlled RF transmitter and receiver modules, a microcontroller stimulator and electrodes.

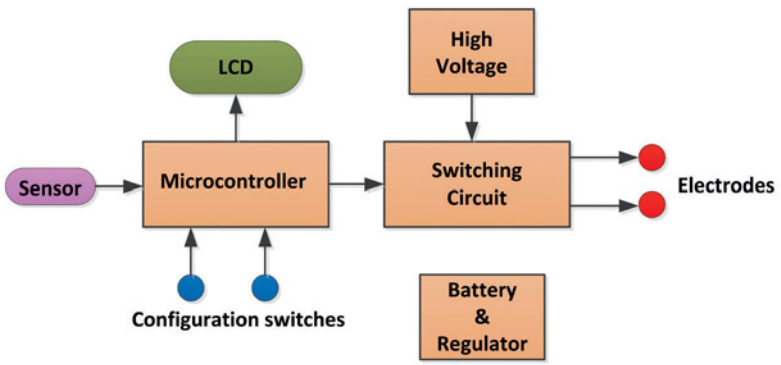


Figure 1: Typical modern FES device

FES Device Architecture

Most FES systems are based on manual, open-loop, or feedback control systems. In manual FES systems patients are required to devote their full attention to operating the device by activating a switch or similar sensor to generate pulses whenever required. Open-loop systems are more popular since they don't require any user interaction during operation. Here, a sensor detects when a heel lifts off the ground and then stimulates the ankle flexor muscles to help the patient walk. FES systems that use feedback are more complex since they can model and correct the gait movements and avoid disturbances during walking.

At present, there are a number of FES devices on the market, including ParaStep from Sigmedics, Compex Motion stimulator from Compex, and Free Hand system from Neurocontrol. Examples of open-loop systems are Odstock Drop foot Simulator by Odstock Medical Ltd, NESS L300 by Bioness and WalkAide from Innovative Neurotronics.

Sensors

All FES devices require an external sensor to determine the correct time when a pulse should be generated and when stimulus should be applied. Some commonly used sensor types include:

- Force Sensitive Resistor (FSR) sensors
- Tilt sensors
- Accelerometers
- Gyroscopes.

FSR sensors are simple and low-cost devices, which are desirable qualities in modern FES systems. FSR are round- or rectangular-shaped flexible resistive in-shoe sensors whose resistance changes with applied pressure. They produce on/off type outputs as the foot is lifted off the ground. When a heel rise is detected, the voltage state at the output of the FSR changes, which triggers the controller to apply stimulation to the peroneal nerve.

Tilt sensors have been used successfully in FES systems to detect when the lower leg of a drop foot patient tilts backwards. These sensors are usually based on the movement of liquid (e.g. mercury) to short circuit a pair of contacts when tilted.

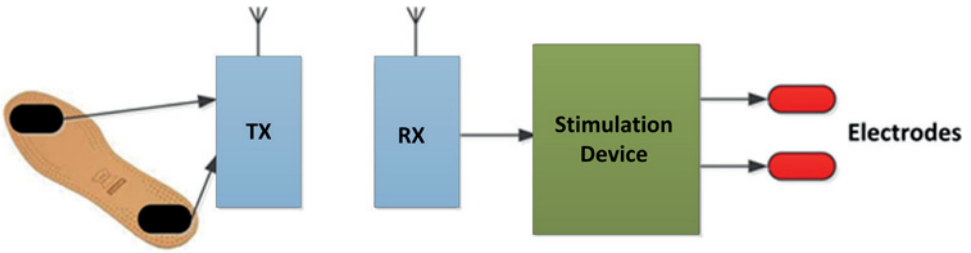


Figure 2: Block diagram of the FootCorrect device

Tilt sensors have advantages over in-shoe sensors as they do not suffer from reliability problems when used repeatedly.

Accelerometers are tiny electronic sensors used to measure velocity and acceleration. They are typically placed on the knee or waist to detect leg movements. Unlike in-shoe sensors, accelerometers are intelligent sensors and they do not suffer from repeatability problems.

Gyroscopes are used to measure angular velocity. Some researchers have reported successful use of gyroscopes as sensors in FES devices. Gyroscopes are usually used with other sensors, such as FSRs and accelerometers.

The Microcontroller

At the heart of all modern FES devices is a microcontroller whose function is basic gait detection and generation of pulses with specified pulse shape, duration and frequency. Low power consumption is the most important factor in selecting the right microcontroller for FES applications, since FES devices are portable, and long battery life is a desirable feature. Although the output pulses can be generated by software, it is easier to use a built-in microcontroller timer to generate accurate pulses with the required pulse shape, width and frequency.

Microcontroller speed or data length are not important and, in general, most 8-bit microcontrollers with around 4MHz clock will be sufficient in an FES system. Simple user interface, preferably with an LCD is also a requirement, thus enabling users to easily adjust the operational parameters.

High Voltage (Or Current) And Switching Circuit

The microcontroller output voltage needs amplification before it is fed to the electrodes. The switching circuit increases the amplitude of this voltage to the required level. This circuit usually consists of a DC/DC converter and a transformer where a low voltage (e.g. +9V) is converted into high voltage (e.g. +80V).

The output of FES devices can be either constant-voltage or constant-current. In a constant-voltage device, the pulse amplitude is around 80V and as the skin resistance increases the current reduces. Constant-current devices provide around 120mA current and these devices are less affected by skin resistance changes.

The output waveform from the FES devices is a pulse with shape that can be monophasic, consisting of positive pulses only, symmetric or asymmetric biphasic, where the pulses are both positive and negative with no gap in between, and symmetric biphasic with inter-pulse intervals. The pulse frequency in most devices can be varied between 1-100Hz, and its duration between 50µs and 1ms.

FootCorrect

The main task for the FootCorrect device is to satisfy the following requirements:

- Low-cost and low-power
- Portable
- Wireless
- Battery-operated
- Standalone with no external support.

The system's block diagram is shown in Figure 2. Two sensors are used inside the shoe: one operated by toe movements and the other by heel movements. The toe sensor applies when climbing up stairs for example, whereas the heel sensor during normal walking.

When the foot is lifted off the ground, a triggering signal is sent to the stimulation device via a pair of wireless XBee RF transmitter (TX) and receiver (RX) modules, both controlled with ATmega328 microcontrollers. The stimulation device then sends pulses to the patient's peroneal nerve via the electrodes.

The transmitter module is plugged into an Arduino Fio microcontroller development board and is then attached to the bottom part of the patient's leg. The receiver is plugged into an Arduino Uno type microcontroller development board which is then connected to the input of the FES controller device, worn around the waits or in a pocket. Lack of physical wires allows for patient comfort whilst walking.

Figure 3 shows a picture of FootCorrect, and the TX and RX modules are shown in Figure 4, with the entire system's circuit diagram in Figure 5.

The force sensitive resistors inside the shoe are connected to the TX module, also mounted in the shoe. The output of the RX module is connected to the input pin RC1 of the microcontroller. Two pushbutton switches named MODE and SET are connected to port inputs RB0 and RB1 respectively, used to configure the

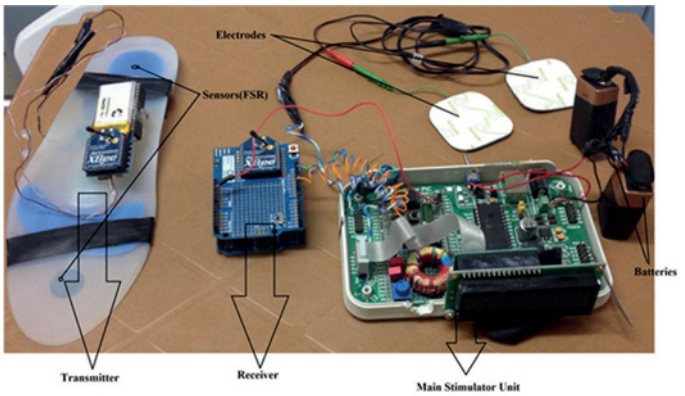


Figure 3: FootCorrect

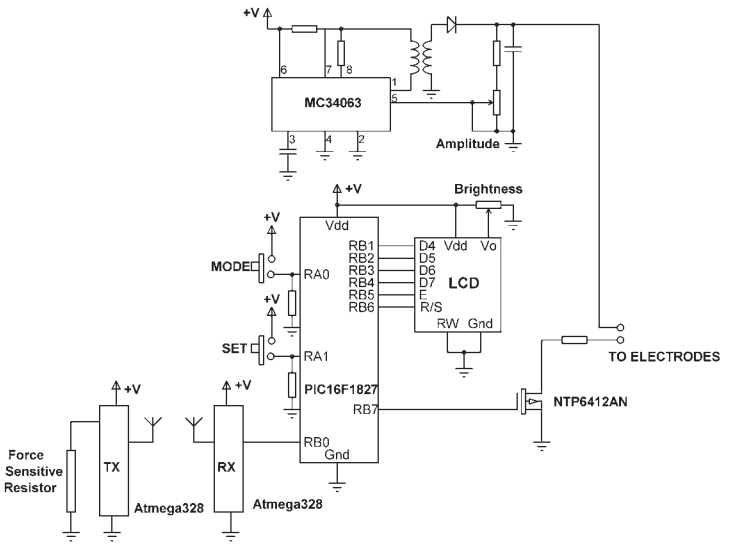


Figure 5: Circuit diagram of the FootCorrect FES device

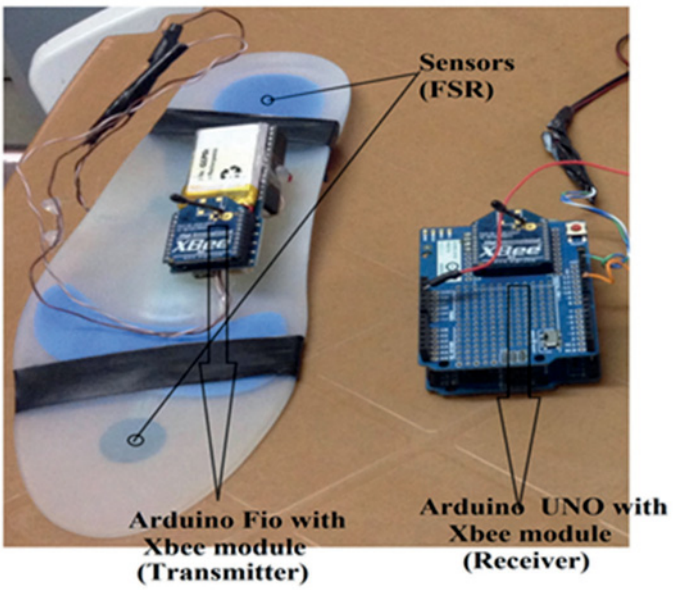


Figure 4: The TX/RX modules of the FootCorrect device

operational parameters, such as frequency, pulse-width and operation profile of the FES device.

The LCD, which is used for configuration only and removed during normal operation to conserve power, is connected to PORT D of the microcontroller. The device is configured with the help of the MODE and SET switches.

High voltage is obtained using a MC34063 type DC/DC converter. The amplitude of the output voltage can be adjusted up to 80V using a potentiometer. RB7 output pin of the microcontroller is used to turn on and off the output voltage through a NTP6412AN-type high-voltage MOSFET transistor switch.

Algorithm And Software

The X-CTU terminal program was used to set up the wireless communication between two TX/RX XBee radio communication modules. Although other terminal programs could be used, the X-CTU software was designed specifically for XBee, with terminal emulation functions and functions for saving, writing and reading data, and testing signal strength and state of the XBee modules.

The software of the stimulator microcontroller has been developed using the mikroC Pro for PIC language. Figure 6 shows the operation of the software in form of a program description language. If there is no activity for a pre-specified period of time, the processor is forced into Sleep mode where extremely low power is used. The processor comes out of this mode automatically when heel-rise is detected. ●

```
BEGIN
        Set stimulation OFF
        DO FOREVER
                IF Heel-rise THEN
                        Clear Timer
                        Set Stimulation ON
                ELSE
                        Increment Timer
                        Set Stimulation OFF
                ENDIF
                IF Timer overflow THEN
                        Sleep
                ENDIF
        ENDDO
END
```

Figure 6: Software operation

Process detection and variability

BY **OLIVER KING**, CHIEF TECHNOLOGY OFFICER OF MOORTEC

Process variation is a complex subject which covers a range of effects; broadly, however, we can consider that these effects are caused by imperfections in the manufacturing process. Examples are implant variations, mask misalignments and optical variations, among others. These all add up to give statistical variation on the ideal or "typical" transistor.

However, the mechanisms and causes of the variation are not particularly our concern. The reason we are interested in it is the ability to measure in a meaningful way where a particular piece of silicon is within the defined process space for its technology. Since, ultimately, process measurement helps optimise performance, we relate process to speed, so in advanced nodes this comes down to MOS device speed and the parasitics of the interconnect.

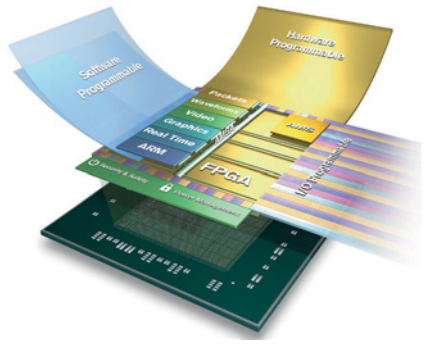
Process variability has always been an issue, and the design process normally accounts for it through designing for worst case. Whilst this is still possible, doing so erodes a larger proportion of the gains made by migrating to an advanced node, and when this is coupled with additional sensitivities to supply voltage (an effect of the dropping of core supplies), we are at a point now where process variation and, specifically, designing for worst case is too high.

Furthermore, with the advent of FinFET processes and the fabrication methods that allow for the high densities seen on current leading nodes, the process variation is manifesting itself in different ways. Due to limited availability of production data on these nodes, it is too early to say we fully understand process variation.

There is a range of applications for making use of process data, the first of which is using data performance optimisation. The simplest implementation of this is speed binning devices. A more detailed performance optimisation is to use this process data to optimise the die with a DVFS optimisation. This can either be once, to take the process into account, or over time to account for temperature and even ageing. It is possible, for example, to reduce power consumption to achieve a desired speed of operation. It is also possible to take process variation across a die into account, which is being done in large SoCs today.

Another application is in detecting chip ageing. This can be either part of performance optimisation, as described above, or through predicting device failure.

Ultimately, process, voltage and temperature are all interrelated because they all determine how fast a chip will work or how much power it will burn doing a given task. Having accurate measurements of all three allows SoC designers to take advantage of the performance which would otherwise be left as margin. ●



Vision-based system design – sensor selection

BY **AARON BEHMAN** AND **ADAM TAYLOR** OF XILINX

Visual sensing is widely used in tasks such as industrial inspection and security surveillance, and opportunities continue to expand in areas such as drones, robotics and augmented reality.

An embedded vision system encompasses the entire signal chain from the image sensor to the system output, which may comprise processed or unprocessed images or information extracted from images. The system architect must be familiar with concepts and techniques associated with the image sensor and the image-processing subsystem.

Choosing The Right Sensor

As far as sensor selection is concerned, CMOS image sensors are the most widely used today. On the other hand, Charge-Coupled Devices (CCDs) can deliver superior performance for high-end or specialist equipment.

When selecting either type of sensor, the first step is to determine the resolution required in terms of pixels per line and number of lines. For example, a scientific astronomy application may require a high resolution two-dimensional sensor, whereas an industrial inspection system may be best served using a line-scan approach.

Line-scan devices comprise one or several lines of pixels in the X direction. Typical applications include inspection or Optical Character Recognition (OCR), where the camera or target is moved to capture the image in the Y direction.

Time Domain Integration (TDI) line-scan sensors are also available, which have multiple lines in the X direction. As the target moves, the pixel value is accumulated from one to the next thereby increasing effective sensitivity to allow faster scan speed or greater low-light performance. Synchronization is required between the line transfer and movement of the target, to prevent smearing and image defects. Frame rates can be very high, as there are only a few lines to read out.

In a two-dimensional array containing a large number of lines, its size is one factor that determines the maximum frame rate. Some sensors allow pixels to be read in parallel for enhanced performance. 2D sensors can also perform windowing or 'region of interest' analysis, to read out pixels only from a particular area of the image. This can boost effective performance in applications where information of interest lies within a small area of the captured image, such as automotive Advanced Driver Assistance Systems (ADAS), or surveillance and scientific equipment.

Having determined the format of the imager and required resolution, pixel pitch is the next important consideration. The pitch defines the size of the pixel that's available to collect the charge created by incident photons. Pixels on a smaller pixel pitch collect less charge in a given time period and thus may require longer integration times to capture an image. This can impair performance in low-light conditions or with fast-moving objects.

Image-capture speed and performance under the expected lighting conditions are also governed by sensor technology and choice of either front-illuminated or back-illuminated type. The key parameter here is Quantum Efficiency (QE), which expresses the number of electrons produced relative to the number of photons striking the sensor. Typically, the chosen sensor's QE should be as high as possible across the spectrum of interest.

Absorption, reflection and transmission are the key criteria that influence the QE of a sensor. In a front-illuminated sensor, photons strike the front face but circuit features such as metallic lines or polysilicon gates can shield some pixels, resulting in lower QE. Rear-illuminated sensors are alternative type devices, back-thinned to receive photons on the back face, thereby avoiding such obstructions. These devices typically deliver superior QE.

Sensor Noise

The next consideration is the noise allowable within the image sensor. There are three main noise sources:

- Device noise is temporal in nature and includes shot noise and noise introduced by the output amplifiers and reset circuits.
- Fixed Pattern Noise (FPN) is spatial in nature and relates to the different responses of pixels when subjected to the same illumination intensity. One of the most popular techniques to compensate for FPN is correlated double sampling of the output signal.
- Dark current is caused by thermal noise within the image sensor, and is present even when there is no illumination. The impact of the

dark signal upon the final image quality is less significant at higher frame rates. It is also temperature related, and so may be reduced by cooling the sensor using a device such as a Peltier element.

Understanding the noise model helps determine the Signal to Noise Ratio (SNR) that can be achieved. Next, the required dynamic range can be determined. Dynamic range quantifies the ability of the sensor to capture images containing both highly illuminated areas and dark areas. It is usually expressed in dB or as ratio of the full-well capacity of the pixel (number of electrons the pixel can hold before saturating) to the sensor readout noise.

Dynamic range is often determined by performing a Photon Transfer Curve test, which plots noise against well capacity. If the device has a digital output, the dynamic range may also be influenced by the number of bits.

Remaining Criteria

Moreover, the I/O standard adopted for data, command and control connections is important, and can influence the effective frame rate. For instance, LVCMOS is not suitable for high frame-rates, but is acceptable for a simple monitoring camera. Dedicated high-speed serialised LVDS links are typically used where high frame-rates, resolution and bits per pixel are required.

In addition, sensors may be of colour or monochrome type. The requirements of the application will dominate the selection. A colour sensor requires using a Bayer-pattern filter on top of each pixel alternating red, green on one line and blue, green on the next. The bias towards green reflects the fact that the human eye is more sensitive to green wavelengths. The true colour of the pixel is determined by post-processing using results from surrounding pixels. This can reduce image resolution by up to 20%.

In a monochrome sensor each pixel receives all of the photons, as there is no Bayer pattern on top of the image array. This results in increased image sensitivity and allows for simpler readout of the image as the de-mosaicking required for colour reconstruction is not needed.

If the selection procedure suggests using a CMOS image sensor, these are in reality complex, dedicated SoC devices that provide designers with additional choices and design considerations. The integration time, for instance, must usually be configured by writing to a register via the command interface. In addition, various shutter modes are often available, such as global shutter mode that enhances capture of fast-moving targets at the expense of relatively high noise, or rolling shutter mode that reduces noise but also limits high-speed capability.

Next Time

This article has explored several key aspects of the image sensor as the first stage in the complex signal chain at the heart of a modern vision-based system. The next article in this series will look at post-sensor signal-processing requirements and potential solutions. ●

Professional 8, 10 & 20 ports USB 2.0 charge only or charge & sync hubs

The Powersolve 8, 10 and 20 port USB charge only, or charge & sync hubs offer the perfect solution to charge and sync several tablet PC's or other USB devices simultaneously. Also ideal for automated duplication tasks such as USB memory sticks etc, where data can be transferred to multiple devices at the same time. Ideal for use in schools, business or any application where multiple charging and or data transfer is required.

Model PLV60-USB 5V USB Hub
This charge only model has 10 output ports which are switchable for 10 x 1A or 5 x 2.4A 5V outputs. Integral power supply will operate from a 90-264VAC universal AC input.

Model PLV120-USB 5V USB Hub
This 10 port, charge only, model is available with 10 independent 5V 2.4A outputs. Features smart charging IC and can charge any device using USB charging technology. Integral power supply operates from 90-264VAC input.

New!

Model PSUSB-0824 5V charge & sync hub
Provides 8 output ports with up to 5V 1.5A (CDP mode) or 5V 2.4A (DCP mode) Supports iOS and Android devices.
Supports high speed 480 Mbps, full speed 12 Mbps and low speed 1.5 Mbps operation. Up to 8 units can be cascaded to increase output ports to 64. Housed in compact aluminium case measuring 170 x 80 x 30mm.
Powered by external 120W power supply with 90-264VAC input.

Model PSUSB-20CH charge & sync hub
Charges and syncs up to 20 devices. Charge current 1.1A per port in charge mode. Supports high speed 480 Mbps, full speed 12 Mbps and low speed 1.5 Mbps operation. Compatible with all USB compliant devices. 2 x 20 port hubs can be connected in cascade mode increasing number of ports to 40.
Housed in metal enclosure which measures 268 x 102 x 40mm
Powered by external 150W power supply with 90-264VAC input.

Models PSUSB-1024 & PSUSB-2024 10 & 20 port charge & sync hubs
Provides up to 1.5A (CDP mode) or 2.4A (DCP mode) Supports iOS and Android devices. Features Green Energy mode switch. The 10 & 20 Port hubs can be cascaded with another unit to double the number of ports. Supports high speed 480 Mbps, full speed 12 Mbps and low speed 1.5 Mbps operation. These models feature integral fan cooling via temperature controlled fans and will shutdown with over temperature. Compact metal housing measures 268 x 102 x 40mm
Powered by external 150W (10 ports) or 288W (20 ports) power supply with 90-264VAC input.

New!

www.powersolve.co.uk
Tel: 44-1635-521858 Email: sales@powersolve.co.uk

Breaking Down OCXOs – Performance

BY **TOMMY REED**, VP OF TECHNOLOGY AT BLILEY TECHNOLOGIES

Oven-controlled crystal (Xtal) oscillators, or OCXOs, are used in applications where a very high degree of frequency stability is required. Sometimes these oscillators may even be referred to as temperature-stabilized crystal oscillators, or just crystal ovens.

While crystal oscillators show a high degree of stability even when the outside temperature is varied over a significant range, some applications require even higher levels of temperature stability. These are the applications where OCXOs may provide the required solution.

Like many other crystal-based products, OCXOs come in a wide variety of packages and package styles, and just large a variety of performance levels and costs – all of which are crucial parameters to consider when choosing an OCXO for a specific project.

Temperature Effects On OCXOs

It is still sometimes necessary to ensure even better stability. This can be achieved by placing the crystal in a thermally-insulated container with a thermostatically-controlled heater. By heating the crystal to a temperature above the one it would encounter within the destined electronic equipment, its temperature can be maintained constant, resulting in far greater temperature stability. Additionally, the crystal in the OCXO will be cut to ensure that its temperature stability is optimized for the operating temperature.

Crystal ovens are commonly run at 75°C, thermostatically-controlled.

The typical specification for an OCXO might be ±5 x 10^{-8} per degree Celsius (0.05ppm), whereas a non-oven controlled oscillator may be from 10 to 100 times poorer. Since the oscillator assembly will also contain buffering circuitry and supply voltage regulation, the other characteristics of the oscillator should also be good. Typically, frequency stability might be expected to be around ±5 x 10^{-9} (0.005ppm) per day, ±5 x 10^{-7} (0.5ppm) per year and 1 x 10^{-7} for a 5% change in supply voltage – figures much better than that of simple crystal oscillators.

A periodic calibration of the OCXO may be required to ensure optimum accuracy is maintained, and this also helps fight the crystal's ageing processes too. Typical calibration periods may be on the order of six months to a year, but the actual period will depend on the OCXO itself and the requirements of its application.

OCXO Physical Considerations

OCXOs are physically much larger than a simple crystal oscillator. Not only do they need to contain the crystal oscillator itself, but also the heater, control circuitry and the thermal insulation around the crystal oscillator.

Typically, the heater is run from a different supply than the oscillator. It does not need the same level of regulation and, indeed, the oscillator is most likely to have its own regulator to remove any stray noise and RF that may appear on the supply line and thereby degrade the performance of the OCXO.

The supply for the heater in the OCXO may be quite current-hungry. Some units may require an Amp or so to warm up. This figure decreases as the temperature inside the OCXO rises and less heat is needed.

OCXO units are naturally more expensive than crystals by themselves, but the performance of an OCXO is considerably better than that of a simple crystal in an unregulated environment. They also consume much more power than a traditional crystal or non-oven oscillator, which is considered one of their main drawbacks, leading to the rise in a new class of low-power OCXOs that draw significantly less power than traditional ovens. ●

More on OCXOs in the next issue

EMULATING DATA EEPROMs

WILLEM J. SMIT, DESIGN ENGINEER AT MICROCHIP TECHNOLOGY

LOOKS AT THE EMULATION OF HIGH-ENDURANCE DATA EEPROMS ON 8-BIT MICROCONTROLLERS

No two families of microcontrollers are exactly the same in terms of features and specifications. One feature available only on some microcontrollers is to store user data internally in a non-volatile memory, such as internal EEPROM for example.

To keep costs down, some MCUs do not have internal EEPROMs but can read and write flash program memory (FPM) using self read-write. This allows users write and read data to and from any unused portion of the FPM in a non-volatile manner.

FPM is arranged in rows, consisting of a fixed number of 14-bit program memory words. For example, on the PIC10F322 8-bit microcontroller from Microchip Technology, the FPM is broken down into rows consisting of 16 14-bit words, accessible by an address of XX0h-XXFh.

The FPM can only be erased by a minimum of a row at a time; when erased, the contents are all set to 1, whereas when writing, only 0 can be written.

To use the PIC10F322 as an example, the minimum program flash memory cell endurance is 10k erase and write cycles from -40˚C to +85˚C. Each memory cell is 1-bit in the 14-bit FPM word, but software library routines can increase the minimum program FPM cell endurance to a theoretical minimum of 160k erase-and-write cycles when storing user data in the FPM in rolling-page format; 10k FPM cell endurance by 16 rows is 160k FPM cell endurance. Thus, the FPM is brought into the high-endurance range, which is specified as a minimum of 100k erase and write cycles.

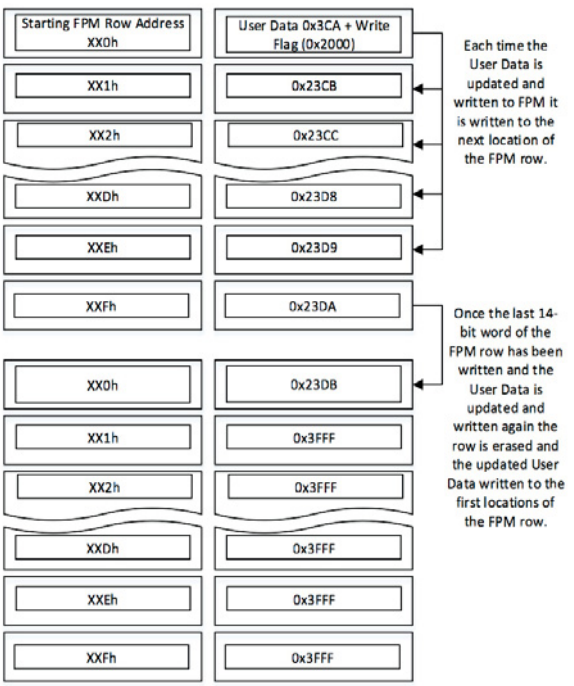


Figure 1: One row of FPM high-endurance write flow

Figure 1 shows a row of FPM high-endurance write flow.

The software library supplied with the device makes use of a minimum of one row of FPM to store one 12-bit user data value, which is continually updated, requiring a minimum endurance greater than 10k erase and write cycles. The increased endurance is achieved by incrementing the location of the 12-bit user data by one FPM address location in the row each time a write takes place. Once all 16 locations within a row have been filled and a new value written, the row is erased and the new value written to the first 14-bit word location of the same row.

Implementation

The software library consists of one main function routine:

uint16_t ReadWrite_HEFlash(uint8_trw, uint16_t data, uint8_t rowstartaddr)

Here, "rw" designates if the function will perform a read of the FPM or a write to the FPM. If "rw" is 1 then write to FPM, or if it's 0 then read FPM. "Data" is the 12-bit value written by the user, and "rowstartaddr" is the starting address of the FPM row being used.

A row's starting address can be determined by looking at the first nibble starting with the least significant bit (LSB) of the FPM addresses. The beginning row address always starts with the first nibble equal to 0x0. For example, 0xE0 to 0xEF is one row, with 0xE0 being the row start address. This function writes and reads 12-bit of user data to and from the FPM. A write is done by writing the next available or open FPM location (bits <11:0>). Bits <13:12> are used as flags, indicating if an FPM row location has been written or not, as follows:

Bits <13:12> = 0b11 = Open
Bits <13:12> = 0b10 = Written (Closed)

The write example is:

ReadWrite_HEFlash(1, 0x3CA, 0xF0)

The above function will write a value of 0x3CA to the next available or open FPM location within the row, which has a starting address of 0xF0. Figure 2 shows the high-endurance flash write flow-chart.

The read example is:

buffer = ReadWrite_HEFlash(0, 0x000, 0xF0)

The above function will return the last 12-bit value of user data written to the selected FPM row and place the value in the buffer. In case of a read, the data field is a "don't care" and will be ignored. If a read is performed and no user data has been written to the FPM, a value of 0xFFF will be returned. The flow chart for this is shown in Figure 3.

When selecting a row or rows to write, never attempt to write

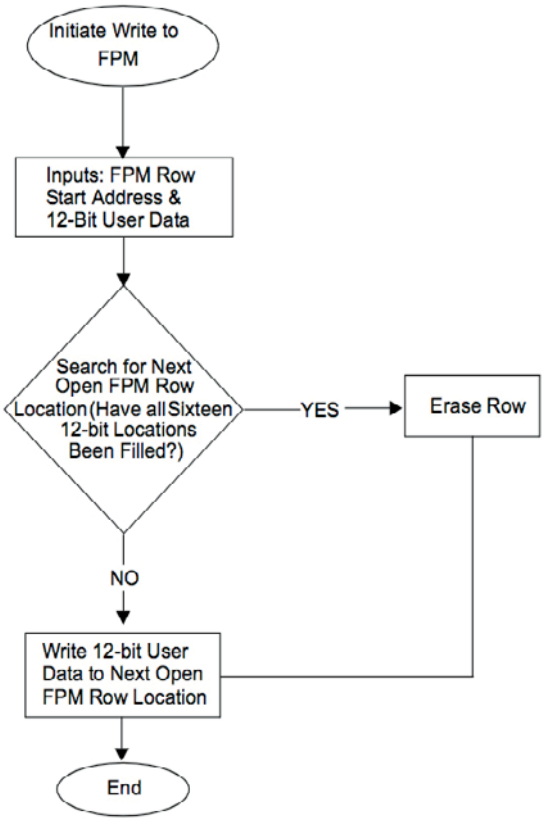


Figure 2: High-endurance flash write flow chart

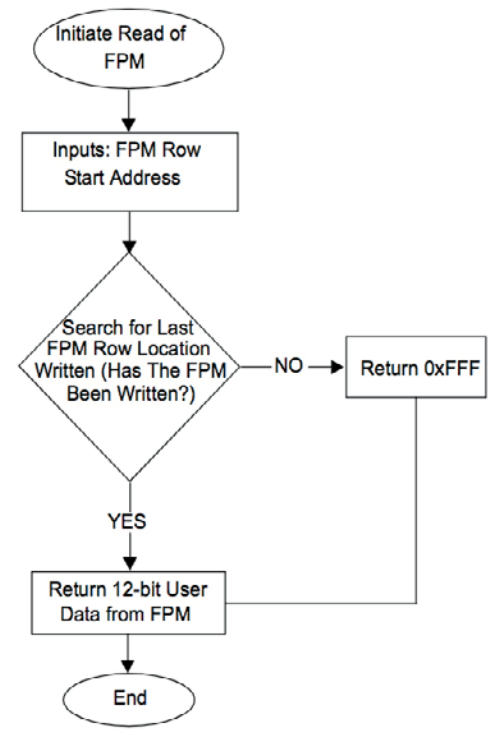


Figure 3: High-endurance flash read flow chart

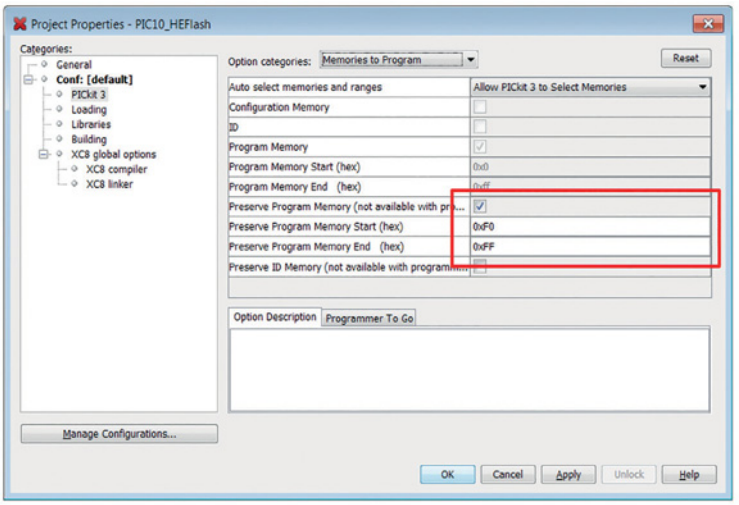


Figure 4: MPLab X FPM preservation

to a section of FPM occupied by the firmware. In addition, areas where the reset and interrupt vectors reside should always be avoided; these are usually located between FPM addresses 0x0000 and 0x0004.

The best way to select an applicable row or rows is to look at the program memory map in MPLAB X after doing a compile.

During program cycles, via MPLAB X by default, the whole FPM on the device is erased.

If a user requires data already written to FPM to be preserved during the programming cycle in MPLAB X, this can be done by opening project properties and selecting the programmer being used in the left hand column, for example PICkit 3, REAL ICE and ICD3. Then, check the preserve program memory box and enter the range of the rows selected for high-endurance flash emulation in the preserve program memory start and stop box. Figure 4 shows how to preserve FPM locations 0x0F to 0xFF.

Special attention should be paid if interrupts are used in the application. When interrupts are being used in the main user code, "save_INTERRUPT();" and "INTCON = SaveInt;" should be uncommented in LPC_HEFlash.C. This will cause the device to disable all interrupts during read and write high-endurance FPM cycles, as well as saving the state of the INTCON register before a read or write cycle and restoring it afterwards. The interrupts are disabled to avoid an interrupt occurring during a read or write cycle and resulting in FPM data corruption.

This shows how high-endurance data EEPROMs can be emulated using supplied software libraries. The PIC10F322 was used as an example, but the information is also valid for other PIC10 and PIC12 devices. ●

Realise your vision

We have all the parts you need to solve your technical challenges and bring your design projects to life.

Never get stuck again. Our extensive range of semiconductors, passives and interconnects has got you covered. With thousands of brands you know and trust, you can count on us for the best solution.

Find the right parts at

uk.rs-online.com

HIGH-SPEED, LOW-POWER, 8-BIT CARRY LOOK AHEAD ADDER WITH DUAL THRESHOLD VOLTAGE

BY ASSISTANT PROFESSOR **SHABBIR MAJEED CHAUDHRY**, **MUHAMMAD QASIM, S.IRFAN LATIF** AND **KAMRAN SALAHUDDIN** OF UNIVERSITY OF ENGINEERING AND TECHNOLOGY IN TAXILA, PAKISTAN

High-speed and low-power adders are widely used in arithmetic logic units (ALUs). Adders with low delays and smaller chip area include carry look-ahead, ripple carry, carry skip, carry select and conditional sum.

Typically, the ripple carry adder is one of the simplest to design and lay out because it uses n number of 1-bit full adders in series to implement an n-bit add operation. In these type adders, each stage has to wait for the carry term from the previous stage to compute the next sum term, which results in long delays. The other full adders (carry skip, carry select and conditional sum adders) use different techniques to reduce this delay, and this is why we use the ripple carry adder as a comparison for more sophisticated designs like the carry look-ahead adder.

The ripple carry adder has a long delay due to the number of gates in its path from the least significant bit (LSB) to the most significant bit (MSB). In a typical design, the long delay path for n-bit ripple carry adder is 2n+2 gates. So, for an 8-bit ripple carry adder the total is 18-gate-delay, which is a major impediment in high-speed designs.

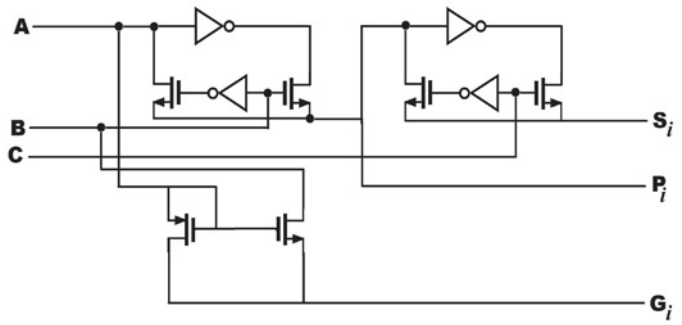


Figure 1: Schematic of the partial full adder (PFA)

For fast computational applications, the preference is to use carry look-ahead (CLA) adders. This type adder computes the final result in an n-bit add operation with shorter delays, solving the carry delay problem by calculating the signals in advance, based on the input signals. As a result, each stage of an n-bit CLA full adder need not wait for the carry signal from the previous stage, hence the shorter delay.

There are several 8-bit CLA adder types in the literature, but usually there are three main challenges that arise when designing n-bit full adders in system-on-chip (SOC) applications, which include power consumption, signal propagation delay and chip area.

New CLA Design

Our 8-bit carry look-ahead adder addresses these challenges based on the logic implementation approach, where we split part of the full adder (typically the main cause of signal propagation delay) by removing one AND gate and an OR gate from the full adder circuit. The end result is a partial full adder (PFA). This split not only reduces signal delays, but results in a lower transistor count, leading to smaller propagation delays and reduced chip area.

To reduce the adder's power consumption, we use dual threshold-voltage (V_{th}) transistor techniques to combat sub-threshold current leakage. Post-layout simulations in Cadence Virtuoso show that our proposed methodology results in lower power consumption and reduced power delay product (PDP) – a figure of merit correlated with the energy efficiency of a logic gate or family.

Ai	Bi	Ci	Pi	Gi	Sum
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	0	1	0
1	1	1	0	1	1

Table-1: Truth table of the partial full adder (PFA)

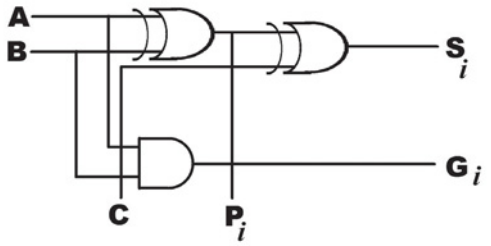


Figure 2: A partial full adder (PFA)

Other Work

The domino CMOS logic circuit design is widely used in high-performance ICs because of its better speed and area attributes, compared to the standard, fully-complimentary, static CMOS logic.

The main disadvantage of the domino dynamic logic technique is its large power dissipation due to transistor switching and clock load. This architecture's efficiency is also influenced by charge sharing and race hazard (the behaviour of electronics, software or other systems where the output is dependent on the sequence or timing of other uncontrollable events).

By using the dual threshold-voltage domino logic we achieved average power of 5.64mW at 1.8V, and a clock frequency of 100MHz. The transistor count is 882 for this circuit.

V_{TH} can be obtained with:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\phi_F| + V_{BS}} - \sqrt{|2\phi_F|}) \quad (1)$$

where V_{THo} is the zero bulk bias threshold voltage, V_{BS} is the bulk source bias, γ is the fabrication process parameter, Φ_F is the bulk potential and $2\Phi_F$ is the surface potential.

Another method to reduce the sub-threshold leakage current employed by researchers is to use a standby switch which offers significant power reduction and lower transistor count.

Proposed Design Methodology

There are two types of power consumption in CMOS circuits: static and dynamic. The static power consumption is generated by current leakage when the transistors are off, whereas the dynamic power consumption is due to transistor switching.

The MOS transistor works in two modes: active and standby. In active mode the leakage current is higher than in standby mode. But, from power reduction point of view, both modes are just as important, which poses a challenge for the designer when optimizing the circuit for low power consumption.

To overcome this problem we propose using high- and low-V_{th} pass transistor logic: low-V_{th} transistor in the main path of the signal reduces the switching power and controls the leakage current without affecting performance.

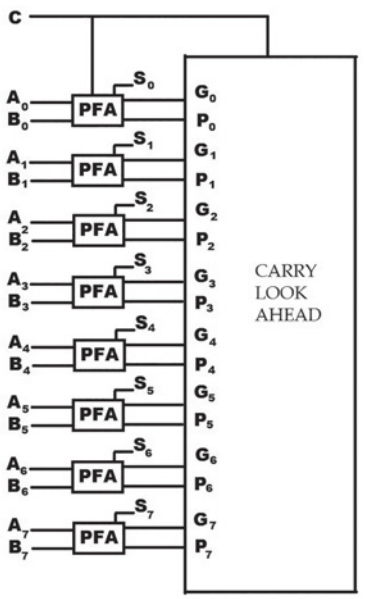


Figure 3: Block diagram of the 8-bit carry look-ahead (CLA) adder

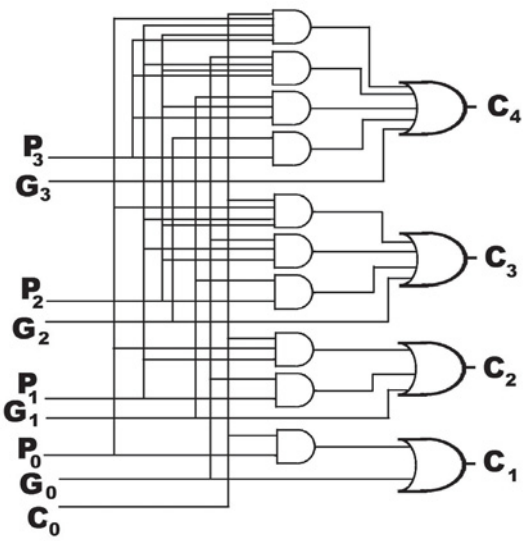


Figure 4: The 4-bit carry look-ahead generator

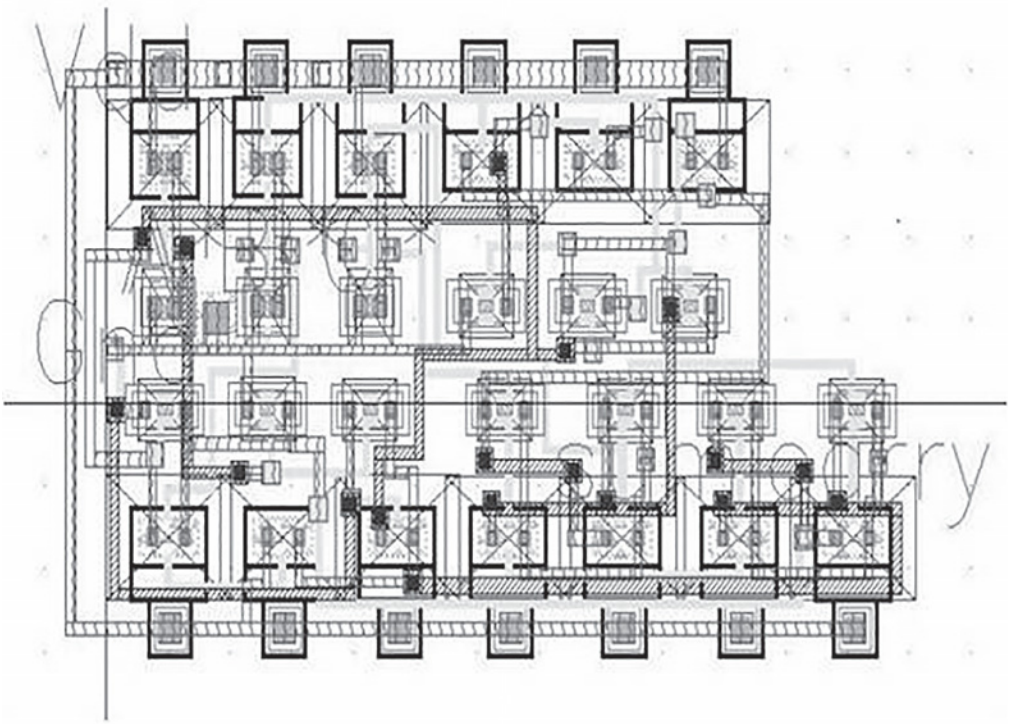


Figure 5: Layout of the proposed full adder

Our PFA Circuit

The schematic of our PFA circuit is shown in Figure 1, with the diagram at gate level in Figure 2. The circuit's truth table is shown in Table 1.

The proposed PFA circuit consists of one AND gate and two XOR gates. It has three inputs (A, B, C) and three outputs (Pi, Gi, SUM). Pi is the carry propagate function and Gi is the carry generate function.

It can be seen from Figure 1 that transistors n1 and n2 and inverters I1 and I2 perform the function of the XOR1 gate; transistors n5 and n6 and inverters I3 and I4 perform the function of the XOR2 gate; and transistors p5 and n9 perform the AND function. The output of XOR1 is Pi, the output of XOR2 is Si and the output of the AND gate is Gi.

CLA Adder Circuit

The speed of the CLA adder is based on parallel calculation of the carry bit. The CLA adder consists of two blocks: PFA and CLA generator. The PFA produces two signals: carry propagate signal (Pi) and carry generate signal (Gi). These are then applied to the CLA generator; a carry signal C is obtained by using the AND and OR gates; see Equations 2-5:

$$Pi = Ai + Bi \quad (2)$$

$$Gi = Ai + Bi \quad (3)$$

$$Sum = Pi + Ci \quad (4)$$

$$Ci+1 = Gi + (Pi \times Ci) \quad (5)$$

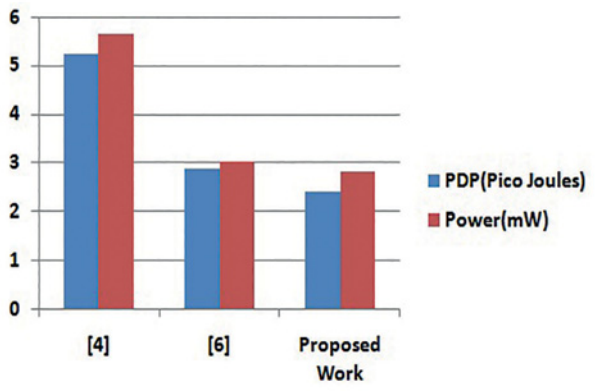


Figure 6: Comparison of power and Power Delay Product (PDP) with other designs

These equations perform the basic function of a CLA adder. Equation 5 determines the carry for the i+1 stage of the basic full adder. To determine it, we put values from i = 0-2, and we then obtain the following set of equations:

$$C1 = Go + Po.Co \quad (6)$$

$$C2 = G1 + P1.Go + P1.Po.Co \quad (7)$$

$$C3 = G2 + P2.G1 + P2.P1.Go + P2.P1.Po.Co \quad (8)$$

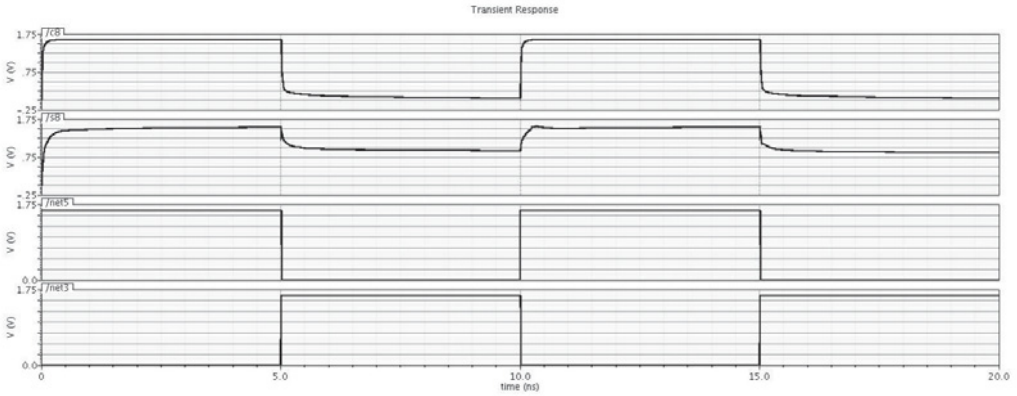


Figure 7: Input/output waveform

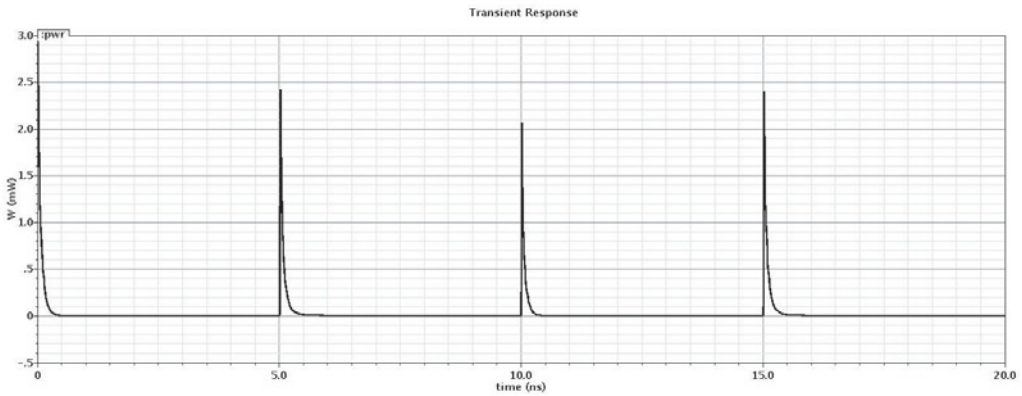


Figure 8: Power waveform

The schematic diagram was designed using Equations 6-8. The block diagram of the 8-bit CLA adder is shown in Figure 3, and the logic diagram of the 4-bit CLA generator, described by Equations 6-8, is shown in Figure 4.

Implementation

We implemented our design with the carry equations, each determining the fan-in of the AND and OR gates. The transistor count of the PFA for 8-bit is 14 x 8 = 112, with the carry block having 280 transistors. The transistor count for the 8-bit CLA adder is 392 with transistor size W/L= 0.22µm/0.18µm.

The CLA adder is implemented in 1P9M UMC 90nm standard CMOS process. The supply voltage is 1.8V with 200MHz operating frequency; the delay is 0.93ns and the consumed power is 2.8mW.

Comparisons of performance parameters between our circuit and other 8-bit CLA adders are shown in Table 2. Our design operates at higher frequency and, yet, has lower power consumption, lower leakage current, lower PDP and lower signal rise and fall times, compared to others.

We mentioned earlier that our 8-bit CLA adder was even able to operate at a maximum frequency of 1GHz, although with higher switching losses and higher PDP.

	Design 1	Design 2	Proposed
Clock Frequency	100MHz	100MHz	200MHz
Operand length	8-bit	8-bit	8-bit
VDD	1.8V	1.8V	1.8V
CMOS Process	1P6M0.18um	1P6M0.18 um	UMC 90nm
Average power(mw)	5.64	3.1	2.8
Transistor Count	882	588	392
Area (mm^2)	1.02 x 1.02	0.79 x 0.79	0.51 x 0.51
Power Delay Product	5.24pJ	2.88pJ	2.40pJ

Table 2: Comparison of our 8-bit CLA adder with other designs

The layout of the full adder is shown in Figure 5. It operates at a minimum voltage of 1V, whereas ours operates at 200MHz; see our circuit's performance in Figures 6-8.

The use of a PFA and CLA generator circuit resulted in an operating frequency increase of 100% and reduction of power consumption by 26%, PDP by 27%, chip area by 58% and transistor count by 66%, at twice the reported operating frequency of competing designs. We also found that our design is more reliable at high speeds too.

THE IMPACT OF DEVICE MISMATCH ON THE PERFORMANCE OF CORRELATED DOUBLE SAMPLING CIRCUITS IN CMOS IMAGE SENSORS

WEIHUI LIU, XIANGLIANG JIN, HONGJIAO YANG, LIZHEN TANG AND **JIA YANG** FROM THE HUNAN ENGINEERING LABORATORY FOR MICROELECTRONICS, OPTOELECTRONICS AND SYSTEM ON A CHIP IN CHINA

EXPLORE THE IMPACT OF DEVICE MISMATCH ON THE PERFORMANCE OF CORRELATED DOUBLE SAMPLING CIRCUITS AND QUANTITATIVE MODELS FOR THE PREDICTION OF COLUMN FIXED-PATTERN NOISE

Fixed-pattern noise (FPN) is one of the major disadvantages of CMOS image sensors compared to charge-coupled device (CCD) imagers. The major source of column FPN is believed to threshold voltage variations ΔV_{TH} and current factor differences $\Delta\beta$ ($\beta = \mu C_{OX} W/L$, where C_{OX} is the gate-oxide capacitance and μ is the low field mobility) between adjacent readout circuits.

Multiple circuit structures have been proposed to eliminate column FPN, and one way is to subtract the dark reference voltage from the signal. The reference voltage for each column is obtained from the last row of the pixels array, covered by light shield. This method can be implemented either on- or off-chip.

The second method to decrease column FPN is to adopt double delta sampling (DDS) circuits, implemented with column amplifiers. Here, the pixel is first reset and then sampled. A second sample is read after the integration period, and the corresponding output is then subtracted from the former sampled voltage. This process eliminates FPN in the column parallel readout structure. Nevertheless, offsets due to parameter changes in the column amplifier still affect image quality, and will require compensation.

Classical CDS Readout Architecture

The CMOS active pixel sensor readout circuit discussed in this article is shown in Figure 1a, with the timing for pinned photodiode type pixels in Figure 1b. This circuit includes an in-pixel NMOS buffer (M2) and a column circuitry consisting of two sampling capacitors (CR and CS) and two PMOS buffers. M1, M5 and M5' are source followers, whereas M3, M7 and M7 are load transistors and common to all pixels of a column. VLN, VLP1 and VLP2 sources determine the bias currents of the buffers; M2 and M6-M6' are pixel and column selection transistors respectively.

Circuit operation starts with enabling the row select transistor M2 of the sensor's first row. The floating diffusion node is then reset to V_{DD}, SHR is lowered and the reset signal sampled on CR. Note that this also stores the kT/C reset noise and FPN from the pixel readout onto CR. Then, TX is pulsed high and a charge from the pinned photodiode transferred to the floating diffusion node. After that, SHS is lowered, and the data signal, kT/C reset noise and pixel FPN sampled on CS, completing the first row's readout.

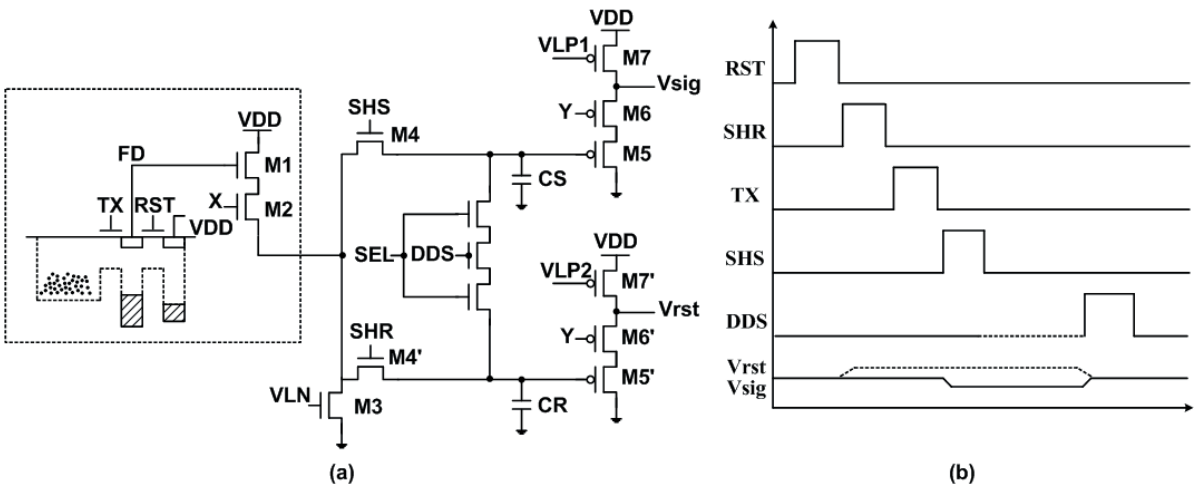


Figure 1: (a) CMOS-APS-pixel- and CDS-readout circuit; and (b) CDS-readout-circuit timing

Lastly, the decoder sequentially selects each column CDS circuit, with each simultaneously outputting the reset signal V_{rst} and data signal V_{sig}. After all CDS circuits are selected, the DDS is pulsed high and the voltage on the two sample capacitors is averaged. Afterwards, the second row is read out in a similar fashion, following with the rest of the rows until the frame is complete. This type operation is called "rolling shutter".

FPN Analysis

In classical CDS readout circuits, after a row has been selected, the signal present on each column pixel in that row is sampled (SHS) onto the holding capacitor CS. Next, each pixel in the row is reset (RST), followed by sampling the reset level (SHR) onto the holding capacitor CR. A simplified expression for the voltage of the reset branch of the column circuit is given by:

$$V_{rst} = (V_{rst,ptxel} - V_{th1} - \sqrt{\frac{2I_{D1}}{\mu_n C_{OX}(\frac{W}{L})_1}}) - |V_{th2,rst}| - (\sqrt{\frac{2I_{D5'}}{\mu_p C_{OX}(\frac{W}{L})_{5'}}})_{rst} \quad (1)$$

where $V_{rst,pixel}$ is the voltage on the floating diffusion node after reset, V_{th1} is the threshold voltage of the pixel source follower n-channel transistor M1, and $V_{th2,rst}$ is the threshold voltage of the column source follower p-channel transistor M5'.
Similarly, the output voltage of the signal branch of the column circuit is given by:

$$V_{sig} = (V_{sig,ptxel} - V_{th1} - \sqrt{\frac{2I_{D1}}{\mu_n C_{OX}(\frac{W}{L})_1}}) - |V_{th2,sig}| - (\sqrt{\frac{2I_{D5}}{\mu_p C_{OX}(\frac{W}{L})_5}})_{sig} \quad (2)$$

where $V_{sig,pixel}$ is the voltage on the floating diffusion node with the signal charge present, and $V_{th2,sig}$ is the threshold voltage of the column source follower p-channel transistor M5.
The subtraction output voltage of the CDS can be written as:

$$V_{OUT} = (V_{rst,ptxel} - V_{sig,ptxel}) - (|V_{th2,rst}| - |V_{th2,sig}|) - [(\sqrt{\frac{2I_{D5'}}{\mu_p C_{OX}(\frac{W}{L})_{5'}}})_{rst} - (\sqrt{\frac{2I_{D5}}{\mu_p C_{OX}(\frac{W}{L})_5}})_{sig}] \quad (3)$$

In its parallel readout structure, FPN is dominated by column-to-column device mismatches. There are three main groups of device mismatches in the CDS circuit of Figure 2, which are sample circuits, source followers and load transistors.

These random differences have a normal distribution with zero mean and a variance dependent on the device area W x L:

$$\sigma^2(\Delta V_{TH}) = \frac{A_{VT}^2}{W \cdot L} \quad (4)$$

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 = \frac{A_\beta^2}{W \cdot L} \quad (5)$$

where W and L are channel width and length, and the proportionality constants A_{VT} and A_β are CMOS-process dependent. Although A_{VT} and A_β have some common process parameter dependencies, experimental data further shows a low correlation between A_{VT} and A_β, so the assumption that they can be modelled as independent random variables is generally accepted.

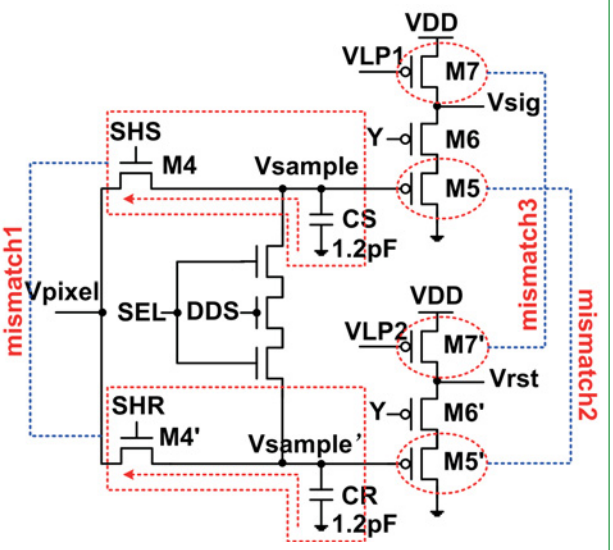


Figure 2: Column offset is caused by CDS circuit mismatches

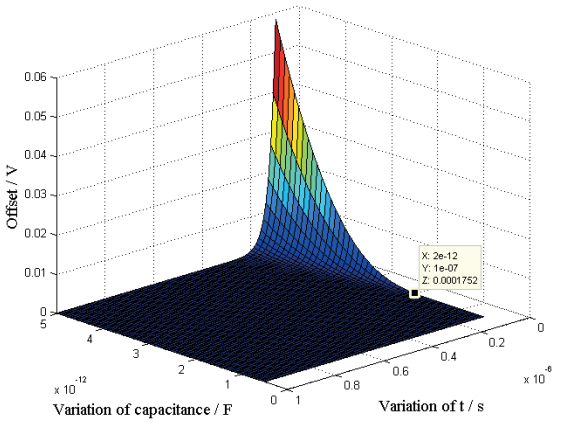


Figure 3: Column offset is caused by deviation of capacitance and sampling time t

The proportionality constants for several industrial CMOS processes are summarized in open literature. This works are based on 0.18μm CMOS process, so A_{VT}= 5.49$mV\mu m$ (PMOS) and A_β= 0.99%μm (PMOS).

Sample Circuit Mismatch

Capacitors CR and CS are combined with M4' and M4 into a simple sample circuit, as shown in Figure 2. According to the relationship between capacitor voltage and charge current, the Equation 6 is obtained (neglecting second-order effects):

$$C\frac{dV_{sample}}{dt} = I_D = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)\left[2\left(V_{DD} - V_{sample} - V_{th}\right)\left(V_{pixel} - V_{sample}\right) - \left(V_{pixel} - V_{sample}\right)^2\right] \quad (6)$$

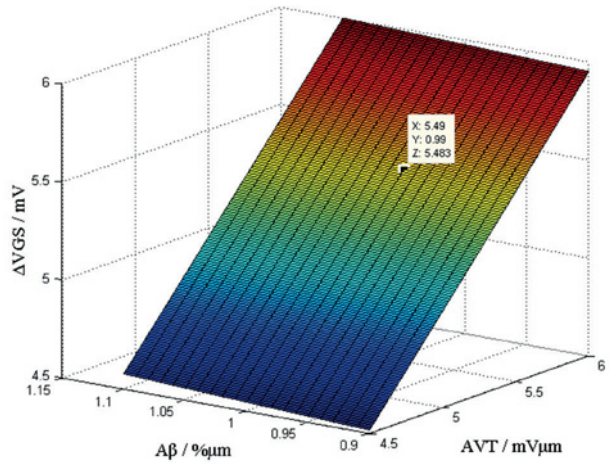


Figure 4: Column offset is caused by mismatch of ΔVTH and Δβ of the source follower

The sampling voltage is influenced by variation in capacitance and sampling time, and so the equation then becomes:

$$V_{sample} = \frac{\left(2V_{DD} - 2V_{th} - V_{pixel}\right) - V_{pixel}\exp\left[\left(V_{DD} - V_{th} - V_{pixel}\right)\mu_n \frac{C_{OX}}{C}\left(\frac{W}{L}\right)t\right]}{1 - \exp\left[\left(V_{DD} - V_{th} - V_{pixel}\right)\mu_n \frac{C_{OX}}{C}\left(\frac{W}{L}\right)t\right]} \quad (7)$$

where V_{pixel} is the input voltage, V_{th} is the threshold voltage of the switch M4-M4', V_{sample} is sample voltage of the sample capacitor CS or CR, C ($1.2pF$) is the capacitance of CS or CR, and t is sampling time.

Column offset is caused by deviation of capacitance and sample time t in the sample circuit, as shown in Figure 3. It was noticed that the column offset is below 1mV, capacitance change is from 0.5-2pF, and sampling time longer than 100ns. Therefore, when the sampling time is 400ns, the mismatch of capacitance has little effect on column offset (< $1\mu V$).

Source Follower Mismatch

As shown in Figure 2, the main column-wise FPN is believed to be mismatch between a pair of adjacent p-channel source-follower input transistors (M5-M5'), comprising a random difference ΔV_{TH} and $\Delta\beta$. The output of source follower can be expressed as:

$$V_{out} = \sqrt{\frac{2I_{DS}}{\mu_p C_{OX}\left(\frac{W}{L}\right)_5}} + V_{sample} + \left|V_{th,p}\right|_5 + \sigma\left(\Delta V_{GS}\right) \quad (8)$$

$$\sigma^2\left(\Delta V_{GS}\right) = \sigma^2\left(\Delta V_{TH}\right) + \frac{\left(V_{GS} - V_{TH}\right)^2}{4}\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 \quad (9)$$

where V_{out} is the output voltage of the source follower, $V_{th,p}$ is the threshold voltage of the source follower M5 or M5', V_{sample} is the sample voltage of sample capacitor CS or CR, and ΔV_{GS} is the gate-source voltage error.

Equations 8 and 9 combined with Equations 4 and 5 provide a first order model, sufficient for tradeoff analysis. Figure 4 shows that for analyzing the implications of device mismatch on a small value of V_{GS}-V_{TH}, the relative effect of the V_{TH} mismatch dominates over the β mismatch, and that the β mismatch effect can often be neglected for MOS transistors.

Since $A_{VT} = 5.49mV\mu m$ (PMOS) and $A_\beta = 0.99\%\mu m$ (PMOS), the column offset will be $5.483mV$. Consequently, the threshold voltage mismatch ΔV_{TH} of the source follower input transistors M5-M5' is the main source of column FPN.

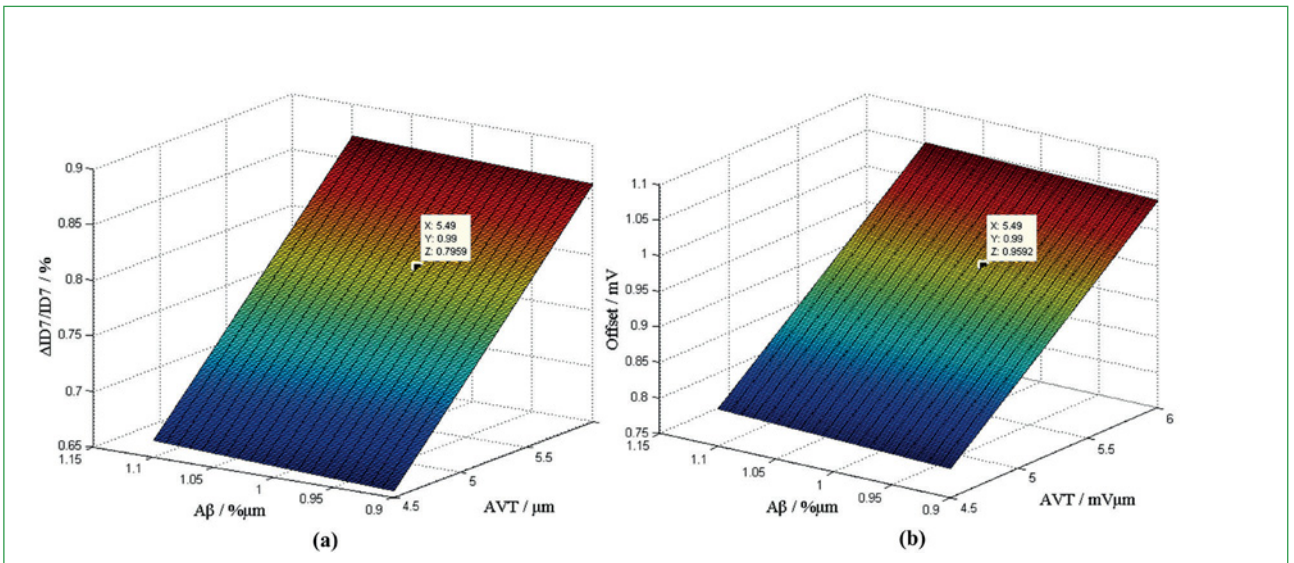


Figure 5: Fig. 5 (a) Percentage of column current variation and (b) column offset are caused by mismatch of ΔVTH and Δβ of load transistor

Load Transistor Mismatch

The mismatch between load transistors M7-M7' is another source of column FPN; see Figure 2. This mismatch directly affects the mirror current, which causes the output voltage of the source follower to introduce column offset:

$$V_{out} = \sqrt{\frac{2\left(\sigma\left(\Delta I_{D7}\right)+I_{D7}\right)}{\mu_p C_{OX}\left(\frac{W}{L}\right)_5}} + V_{sample} + \left|V_{th,P}\right|_7 \qquad (10)$$

$$\left(\frac{\sigma\left(\Delta I_{D7}\right)}{I_{D7}}\right)^2 = \left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2 + \frac{4}{\left(V_{GS}-V_{TH}\right)^2}\sigma^2\left(\Delta V_{TH}\right) \qquad (11)$$

where V_{out} is the source follower output voltage, $V_{th,p}$ is the threshold voltage of load transistor M7 or M7', V_{sample} is the sample voltage of sample capacitor CS or CR, and ΔI_{D7} is the drain-source current error of load transistors M7-M7' ($I_{D7} = I_{D5}$). Figure 5 shows that the percentages of column drain current variation and column offset are caused by mismatch ΔV_{TH} and $\Delta\beta$ of the load transistor. Therefore, if the device has a large value of V_{GS}-V_{TH}, the relative effect of the V_{TH} mismatch dominates over the β mismatch, and the effect of β mismatch for MOS transistors can often be neglected.

Since $A_{VT} = 5.49mV\mu m$ (PMOS) and $A_\beta = 0.99\%\mu m$ (PMOS), current mismatch and column offset will reach 0.7959% and $0.9592mV$, respectively. Consequently, the mismatch of load transistors M7-M7' has relatively lower impact on column offset.

Adding it all up, FPN is dominated by column-to-column mismatches that involve sample circuits, source followers and load transistors. From the analysis it can be concluded that the main source of column FPN is threshold voltage variations ΔV_{TH} between a pair of adjacent p-channel source-follower circuits in CDS; the column offset can reach $6.4422mV$ or $4.5308mV$, and $-6.4422mV$ or $-4.5308mV$ with $A_{VT} = 5.49mV\mu m$ (PMOS) and $A_\beta = 0.99\%\mu m$ (PMOS). However, the final mismatch of circuits depends completely on the deviation of the CMOS process.

Monte Carlo analysis provides information on circuit performance versus process variations and mismatch, so we assumed the SPICE parameters to have statistical distribution. The column offset distribution is shown in Figure 6, for a mismatch. The results for temperatures set at 27°C, -40°C and 120°C are shown in Figures 6a-c. They show standard variation of $4.08983mV$ around $511.521\mu V$, $4.10249mV$ around $526.157\mu V$, and $4.05191mV$ around $486.717\mu V$. Accordingly, the probability for specific ranges of standard variation ($-4mV$ to $4mV$) of column offset is about 68%.

Experimental Results

The designed chip was fabricated in a standard $0.18\mu m$ 1P4M CMOS process with additional steps for the pinned photodiode; see Figure 7. The CMOS image sensor consists of 128×128 pixel arrays, a CDS circuit, and row and column decoders. The pixel size is $4.4\mu m \times 4.4\mu m$ and the chip area occupies $3.5mm^2$; the supply voltage is $3.3V$.

As device mismatches cannot be predicted accurately during the design phase, and they also depend on the device's size, a

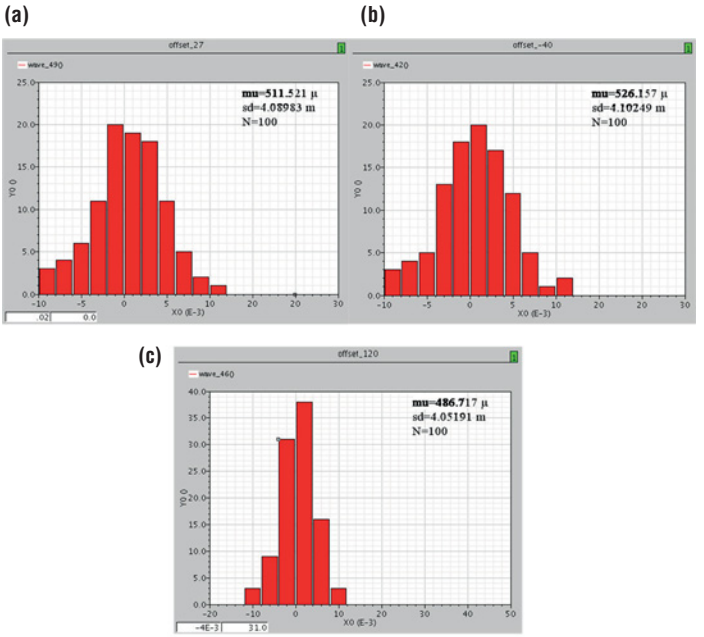


Figure 6: Column offset distribution with Monte Carlo mismatch variation, (a) T = 27°C; (b) T = -40°C; (c) T = 120°C

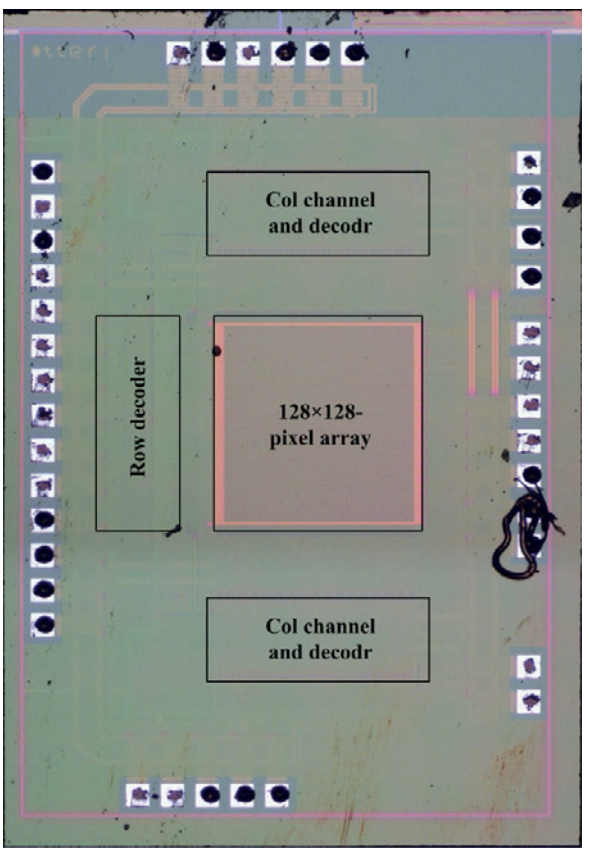


Figure 7: Chip micrograph

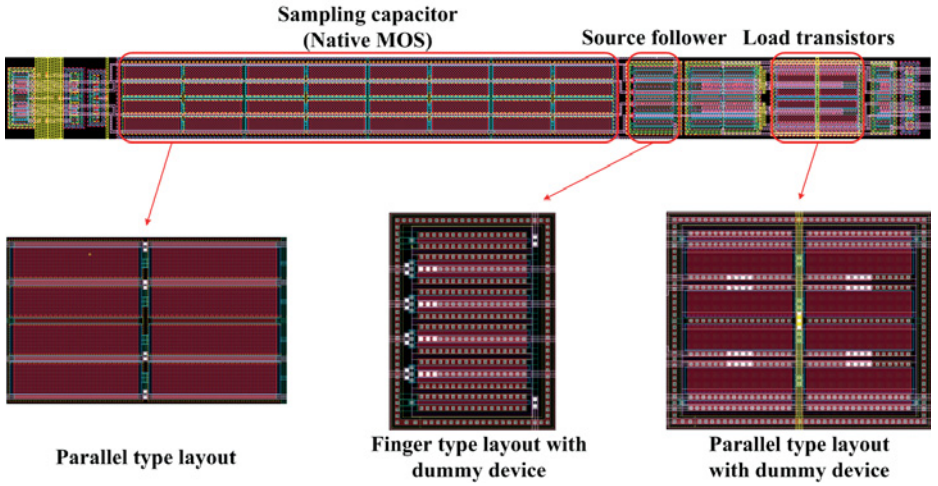


Figure 8: CDS layout with matched technology

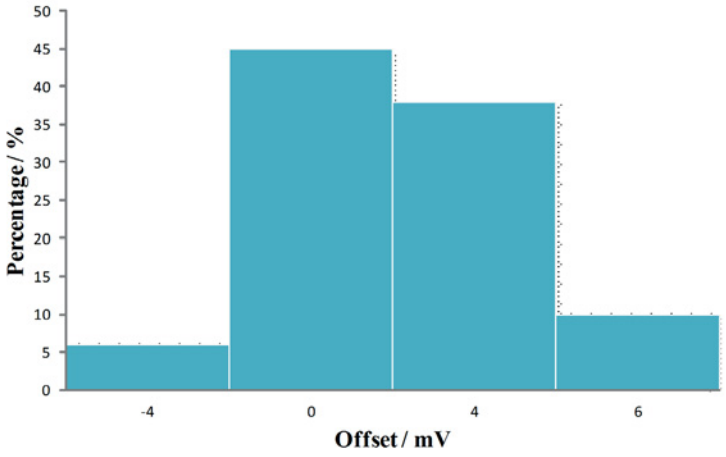


Figure 9: Experimental results of column output offset

circuit designer can use its dimensions (area, width and length), layout and bias point to control the matching. Therefore, good analogue layout practices include using dummy devices, maintaining the same current direction, using symmetrical layouts to cancel processing gradients – for example common-centroid layouts, avoiding metal coverage and maintaining identical metal fill patterns around the device.

Packaging-induced stress can also introduce systematic device mismatches. This can be avoided by changing the circuits' locations on the die.

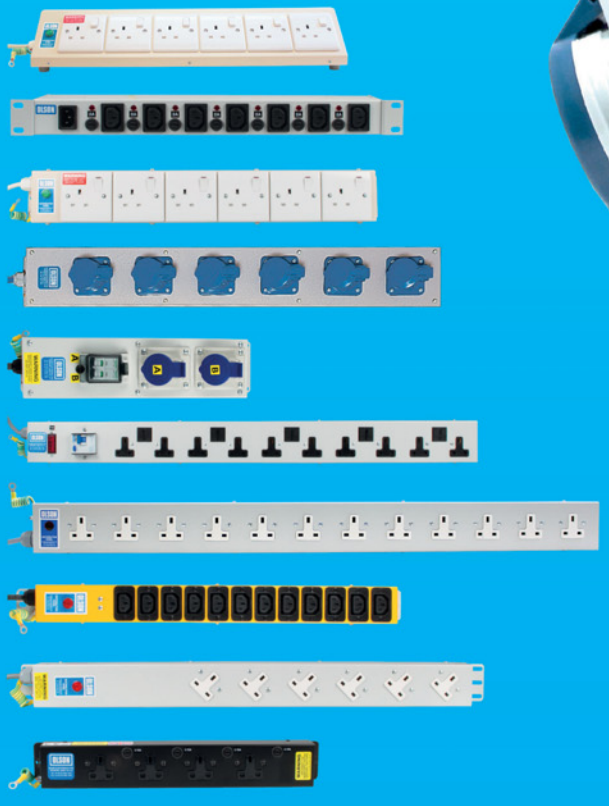
We designed a matched layout of CDS as per Figure 8. Measurements were first taken with conventional equipment, and then with CPLD (complex programmable logic device) controlled boards. Figure 9 shows the results of the FPN of a column CDS circuit taken at maximum speed of 78.125kfps in a laboratory with fixed reset control of pixels, which shows that all probability for specific ranges (-4mV to 4mV) of column offset is about 90%.

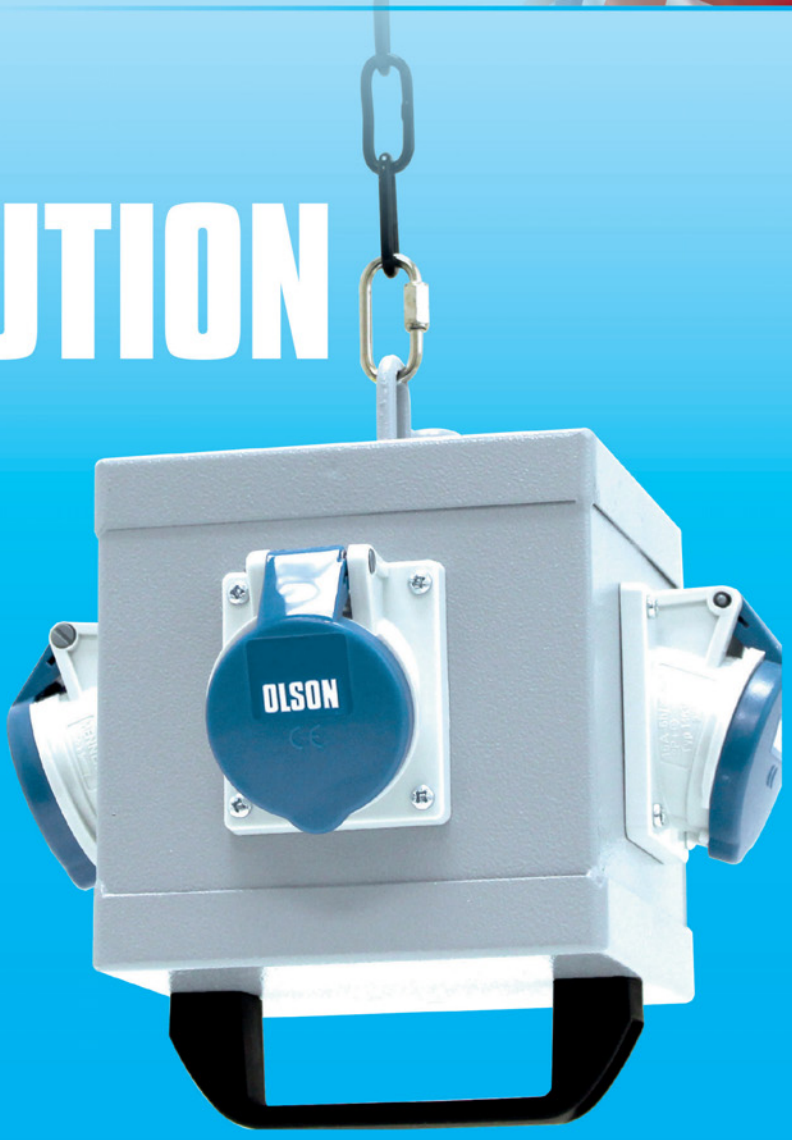
Experimental results show that the main offset values are -4mV, 4mV and 6mV, which are in good agreement with the forecasts of theoretical analysis. Reasons for deviations between experimental results and simulations are due to noise coupling inequality on the internal power supply's output. ●

OLSON®

CELEBRATING 55 YEARS
OF BRITISH MANUFACTURING

POWER DISTRIBUTION UNITS





THE NUMBER ONE CHOICE
FOR BESPOKE POWER SOLUTIONS

- Rated at 13A, 16A and 32A
- Metal construction
- Vertical / horizontal mounting
- Availability from stock
- Colour variants available
- 24 hour delivery

SINCE 1961

Manufactured in the UK

OLSON®

+44 (0)20 8905 7273 | sales@olson.co.uk | www.olson.co.uk

HYBRID CHANNEL-PERFORMANCE-OPTIMIZED ADVANCED MULTI-BAND-EXCITATION VOICE CODEC

SIGNAL FADING, INTERFERENCE AND POOR DECODING QUALITY AFFECT SATELLITE MOBILE COMMUNICATIONS, SAY **WENLIANG LIN, ZHONGLIANG DENG, XUEMING LI, NING LI** AND **WEN LIU** FROM BEIJING UNIVERSITY OF POSTS AND TELECOMMUNICATIONS, AND **QIN FANG** FROM BEIJING SYLINCOM TECHNOLOGY

Space-based networks require satellite mobile communications to be set up as wide area networks. Although VR (virtual reality), high-definition video broadcasting and real-time multi-party communications are becoming new growth areas, there is still a need for low-bit-rate and high-quality voice services (Figure 1).

The 2.4kbps voice services offer reliable communications in satellite channels but with large power attenuation, which has attracted the attention of researchers. Some advanced voice coding algorithms enhance the performance of the Mean Objective Score (MOS), which represents the objective sensation quality for people in ground mobile communications networks such as AMBE (Advanced Multi-Band Excitation), MELP (Mixed Excitation Linear Prediction), ACELP (Algebraic Code Excited Linear Prediction) and others.

In this article we propose a novel Hybrid Channel performance-optimized Advanced Multi-Band Excitation voice codec (HC-AMBE), which combines channel performance with the voice signal envelope to enhance the coding framework. The voice frame structure is optimized by vector compression, where the loud part of the voice remains unchanged, but the quietest part is compressed with Line Spectrum Frequency, or LSF (LSF is a Fourier transform of linear predictive coding for voice). HC-AMBE effectively promotes coding overheads and decreases the bit rate of voice coding throughput. Simulations and tests show it improves speech MOS RMSE (Root Mean Square Error).

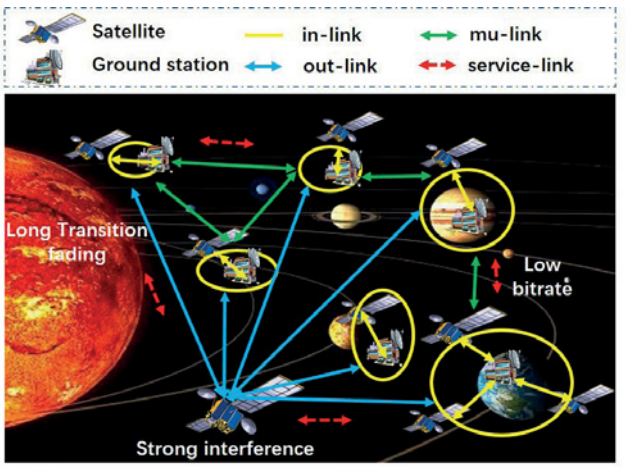


Figure 1: Low bit-rate voice service in deep space communications

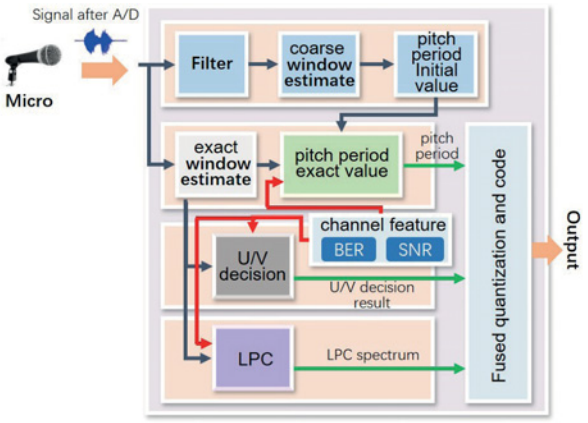


Figure 2: HC-AMBE voice coding framework

HC-AMBE Voice Coding Framework

Our proposed framework consists of voice signal de-noising pre-processing module, pitch period predicting module, V/U (unvoiced/voiced) judgment module, linear predictive coding module, and combined channel performance and voice signal envelope error controller; see Figure 2. The pitch period predicting module extracts the pitch period frequency from voice signals, which is the vocal cord vibration period during speech.

We performed voice coding vector quantization in two continuous speech frames, based on 8-bit quantization of the pitch period

frequency, and the number of quantization bits for parameters such as noise gain and V/U judgement. After using CRC (Cyclic Redundancy Check) for groups of quantization bits, a stream of 2.4kbps voice data is generated.

Improving Voice Quality

To improve the quality of voice from the codec, our solution decreases the total number of quantization bits and improves the coding overhead and redundancy.

Traditional 2.4kbps voice algorithms use 8kHz sample rate and 180 sample points; each voice frame lasts 22.5ms and has output of 54 bits. We allocated 25, 8, 8, 7, 4, 1, 0, 1 bits respectively for the LSF vector quantization for noise gain, residual harmonic spectrum (different vocal sounds made during speech), pitch period frequency, V/U judgment, period sign, CRC and quasi-synchronization.

Simulations demonstrate that different allocations of vector quantization bits take up different times. Tests show LSF takes up the most time and bits for quantization bits' matrix operations. Assuming the total number of vector quantization is 54 bits, decreasing the bit number in the LSF vector quantization will not deteriorate voice quality. Therefore, sensation-optimized voice frame structure and adaptive sparse vector quantization are used to control the coding redundancy and quality, as shown in Figure 3.

The new algorithm not only enhances the voice coding with the same quantization bits, it also focuses on the potential compressed features, such as LSF. The vector quantization number of LSF is designed to reduce from 25 to 19 bits, where 19 bits are extracted from multi-band input signal pulses, which limit the lengths (or range of periods) of the pitch to keep the voice signal's envelope features.

Meanwhile, we make CRC 9 bits for 19 bits LSF. HC-AMBE performs CRC for the total vector quantization data. Superposition of two CRC error correction layers can compensate for any decoding errors from channel fading, and recover missed data, which obtains acceptable voice quality in poor satellite channels.

Sensation Voice Coding And Decoding

A parallel coding and decoding sensation voice codec is also designed, optimized with an AMBE speech algorithm, as shown in Figure 4.

Jitter and link loss degrade the quality of decoded voice, so the HC-AMBE codec provides a stable and sparse coding structure. A duplex vocoder-chip codes and decodes voice data to realize a hybrid channel performance optimized framework and generate an optimized structure for the voice's main features and adaptive sparse vector quantization compression.

A microphone and a speaker are used as voice input and output. We used TL C32046 as our analogue-to-digital converter (ADC), CSP 1027 as voice pre-processing module and STC10F08XE as the main microcontroller.

Continuous voice is captured from the microphone; TL C32046 converts it into a digital signal and CSP 1027 modifies it by low-pass filtering, amplification, wave sampling, scalar quantization and PCM (Pulse Code Modulation). Each voice frame is extracted at 20ms intervals.

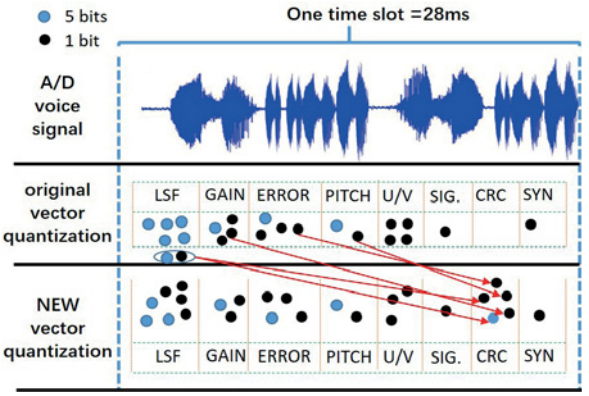


Figure 3: Adaptive sparse vector quantization

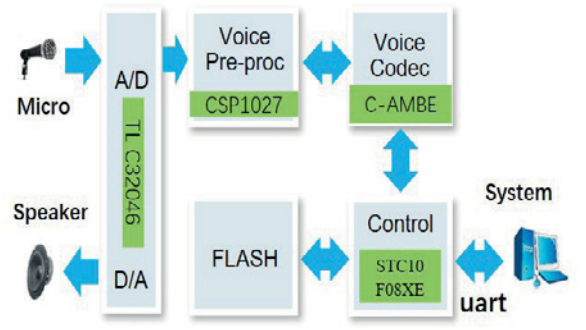


Figure 4: Parallel sensation voice coding and decoding

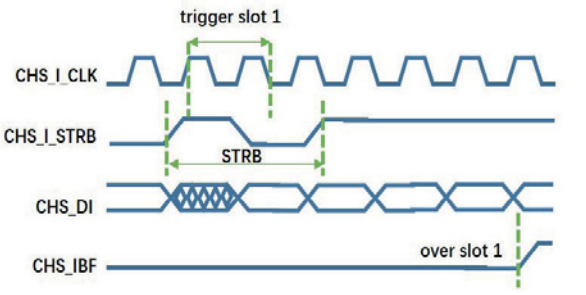


Figure 5: Sequential waveform figure of HC-AMBE

Voice signals coding bits are generated by streaming parameter vector bits. Streaming voice signals bits are uploaded to the host computer, which simulates channel degradation and test signal quality. In the decoding stage, duplex HC-AMBE chip codes receive the coded streaming vector bits, recover the source-audio serial bits and perform a digital-to-analogue conversion, low-pass filtering and amplification.

A sequential waveform from the HC-AMBE voice encoder is shown in Figure 5.

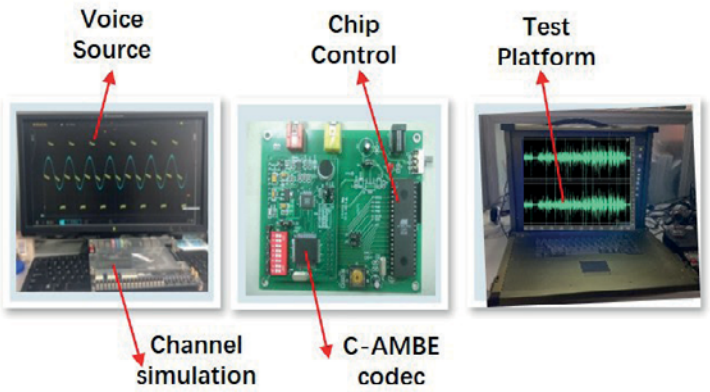


Figure 6: Satellite mobile communication voice-quality testing simulation environment

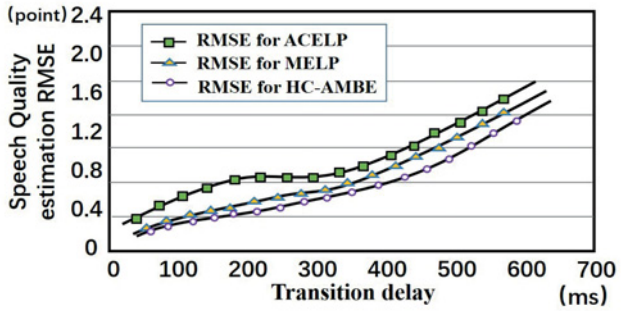


Figure 7: RMSE voice quality estimation for different transition-delay-testing simulation environments

Test And Simulation

We built a satellite mobile communication voice-quality testing simulation environment, consisting of tested voice sources, voice coding algorithms, voice transmission channels, voice quality evaluation algorithms and test results analysis module, as shown in Figure 6.

The target analogue voice source was a 10-segment male voice of two seconds, selected from the ITU-T B series international standard voice database. So we can simulate the actual effect of satellite mobile terminal speakers, the voice was filtered by an IRS (Intermediate Reference System) to generate a signal that matches the amplitude and frequency of a satellite mobile communications voice.

We chose MELP and ACELP as voice coding algorithms, and a channel model similar to the Lognormal-Rayleigh model, modified by large power attenuation for multi-path fading probability distribution. Experimental data was processed by the Monte Carlo method, and the MOS RMSE of subjective speech quality analyzed. The test results are shown in Figures 7 and 8.

Figure 7 shows the RMSE results of voice quality estimation by different voice coding algorithms and with different transition delays. The voice signal encoding and data processing delays are set at 50ms and 30ms respectively. With increase in transition delay, the subjective speech sensation quality RMSE of all voice coding algorithms rises. At the case of 0-100ms, three voice coding algorithms have a low-level MOS RMSE of below 0.4. The tested, recovered, decoded voices are heard clear and continuous, which shows high quality. However, when the transition delays increase to 100-300ms, the voice signal appears broken and noisy.

It was determined that the voice quality RMSE with the HC-AMBE algorithm is 13.3% lower than MELP and ACELP. If the transition delay is above 600ms, the loudspeaker voice signals cannot be distinguished because of their poor quality. The RMSE threshold of failure HC-AMBE decoding is then 0.65, with 352ms mapping for the transition delay. RMSE results for voice quality estimation for different voice coding algorithms and with different coding delays are shown in Figure 8.

Voice signal transition and data processing delays are configured at 250ms and 30ms. In the case of a 0-20ms voice-coding delay, HC-AMBE, MELP and ACELP have a low-level MOS RMSE of below 0.056. Clear and continuous voice can be heard from the speakers, which indicates a satisfactory voice quality.

As the voice coding delay increases to 20-60ms, the voice quality RMSE of MELP and ACELP show obvious performance deterioration, including signal discontinuities and noise. Whilst HC-AMBE remains below 0.2 RMSE with acceptable listening clarity, because of the LSF bits' compression of the quietest parts, it is determined that the RMSE threshold of failure for HC-AMBE decoding is 8.6% higher than that of MELP and ACELP. Therefore, HC-AMBE effectively improves the coding overheads and decreases the voice-coding bit rates throughput. We used an FPGA-based system to simulate, test and verify our method, and results show that it improves speech MOS RMSE by 13.3% and raises the failure threshold to 8.6%. ●

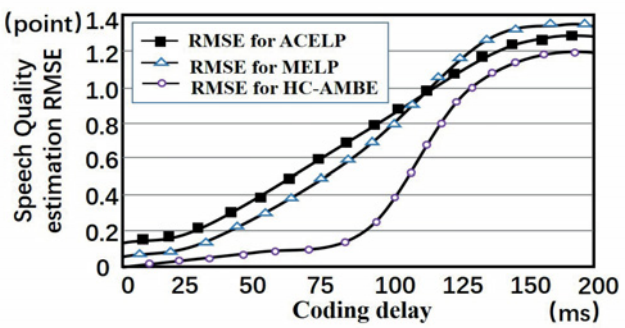


Figure 8: RMSE voice quality estimation for different coding delays

Worldline

XJTAG Boundary Scan Wins the Trust of e-Payment Solutions Leader

"e-payment solutions provider Worldline has chosen XJTAG boundary scan over its previous solution as part of a test strategy created to ensure absolute trust in the technology supporting its services. Aided by XJTAG's test-development expertise, Worldline is benefiting from 30% higher test coverage, 60% lower test hardware costs and 50% faster test cycle time."

Worldline, an Atos company, is a leader in electronic payment solutions, and offers a complete end-to-end service that includes all the technology from the payment terminal to the secure network used for validation, and the servers that verify the transactions. Worldline payment solutions are in action every day, around the globe.

Worldline is highly regarded throughout the banking industry for excellent security. To protect this reputation, the company's engineers have created a robust test regime for equipment such as its payment terminals, which feature built-in tamper checking that protects the unit's secure memory to prevent hackers accessing any useful data. Working with Logic Technology, an embedded development consultant and XJTAG distributor in Benelux, Worldline engineers selected XJTAG's XJRunner system to test this critically important aspect of the terminal's functionality.

XJRunner is used on the production line at Worldline's manufacturing partner, and also for in-house test and repair. In addition, Worldline is extending the use of the system throughout its global Value Added Reseller (VAR) network. This gives the VARs flexibility to test or re-flash boards locally and so save the time and costs of returning boards to Belgium. Over 40 systems are currently deployed worldwide, with many more planned for the future.

XJTAG is supporting Worldline with test-development and maintenance services that enable engineers to access the latest versions of boundary scan tests. The XJTAG partnership allows Worldline to focus on its core technology and benefit from the latest developments in test while reducing overall deployment costs. "The service from XJTAG is competitively priced and offers outstanding flexibility and competencies that support our test requirements," explains Leone Alfano, Industrialization Test Specialist at Worldline.

XJRunner is a run-time boundary scan environment optimised for production-line use. It provides layout and schematic viewers to aid fault finding. XJRunner can test multiple boards simultaneously, and is compatible with commonly used serial-numbering systems.

Worldline has integrated XJRunner into a custom test station based on National Instruments' LabVIEW™, taking advantage of the XJTAG .NET API and Virtual Instruments (VIs) to complete the integration quickly and efficiently. "The support provided to facilitate integration with LabVIEW makes XJTAG really stand out against other systems," confirms Leone Alfano. By integrating XJRunner so successfully with LabVIEW, Worldline has been able to take advantage of XJTAG boundary scan to verify power-supply voltages and also to automate the testing of RF circuitry. The RF test routine uses XJRunner to enable the board's transmitter output, allowing the test station to automatically verify the RF carrier signal using a digital oscilloscope. XJRunner then disables the transmitter to terminate the test.

Leone Alfano quantifies some of the advantages Worldline has achieved by choosing XJTAG: "We are using XJTAG at every stage of the product lifecycle. Since introducing it, we have increased test coverage by at least 30% while halving test cycle time and saving 60% of test hardware costs. We are very pleased with the results."

opinion

Leone Alfano
Industrialization Test Specialist
Worldline

"The service from XJTAG is competitively priced and offers outstanding flexibility and competencies."

"The support provided to facilitate integration with LabVIEW makes XJTAG really stand out against other systems."

"We are using XJTAG at every stage of the product lifecycle. Since introducing it, we have increased test coverage by at least 30% while halving test cycle time and saving 60% of test hardware costs. We are very pleased with the results."

Data Bank

worldline
e-payment services

Company	Worldline, an Atos company
Nature of business	European leader in business and payment transactional services, 40 years experience in payments
Main products	Design and provide innovative, end-to-end vertical B2C solutions: Merchant Services & Terminals, Mobility & e-Transactional Services, Financial Processing
Customers	B2B2C industries
Location	Operates in 17 countries; over 80% of turnover in Europe
Employees	7,200 worldwide
Web site	www.worldline.com

DESIGNING FRACTIONAL ORDER PID CONTROLLERS WITH ARTIFICIAL INTELLIGENT OPTIMIZATION TECHNIQUES

BY **MEHMET KORKMAZ** AND **OMER AYDOGDU** FROM SELCUK UNIVERSITY IN TURKEY

With advancing technologies in the industrial space, various systems require apt techniques to control them effectively. This has brought about a new wave of controllers based on fuzzy logic, nonlinear PID (Proportional Integral Derivative) and predictive control methodologies.

The PID or IO-PID (Integer Order – Proportional-Integral-Derivative) is an important controller, used widely in industrial applications and academic studies.

In this article we will discuss Fractional Order PID (FO-PID) controllers, which are no different to the traditional PID controllers but have additional fractional order integer and derivative terms.

Fractional Calculus

Fractional calculus (see Box, right) is a branch of mathematics that deals with derivatives and integral terms in non-integer order; in other words, it is a generalization of traditional calculus.

Up until recently, its heavy calculation process has impeded the fractional calculus from being used in many applications. But, advanced computers and new methods and software have made it more widely accepted.

Fractional terms are used as a tool for describing systems, from bio-engineering to control applications. In control, fractional calculus extends the classical PID scheme by adding non-integer terms, an improvement that ensures more precise design and control. However, the key question is how to accurately determine the parameters of a fractional PID controller and apply them to a system.

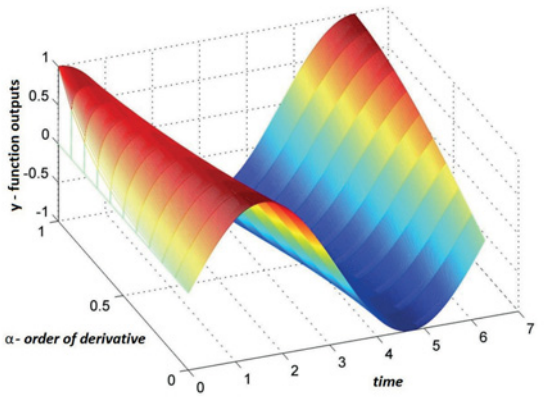


Figure 1: Fractional derivative of sin(t) signal

FRACTIONAL CALCULUS

Fractional calculus is a branch of mathematical analysis, and is as old as integer order calculus.

Fractional calculus was first mentioned in the correspondences of G.W. Leibniz (1646-1716) and G. l'Hôpital (1661-1704), in the late 17th century. Leibniz wrote a letter to G. l'Hôpital asking:"Can the meaning of derivatives with integer order be generalized to derivatives with non-integer orders?" to which L'Hôpital's replied: "What if the order will be ½?"

Leibniz quickly retorted: "It will lead to a paradox, from which one day useful consequences will be drawn." This letter was dated 30 September 1695, a date now considered the birthday of fractional calculus.

This prediction by Leibniz is only now showing its importance, confirming that next centuries' calculus will be fractional. For example, what is the half order derivative of the sinus signal (in Figure 1) or is it still zero if taking the fractional derivative of a constant? These are the hot topics of fractional calculus occupying academics and engineers nowadays.

The differintegral operator is D in the equation below, in which derivative and integral terms are represented as follows:

$$ {}_aD_t^{\alpha} = \begin{cases} \frac{d^{\alpha}}{dt^{\alpha}}, & \Re(\alpha) > 0 \\ 1, & \Re(\alpha) = 0 \\ \int_a^t (d\tau)^{-\alpha}, & \Re(\alpha) < 0 \end{cases} $$

where a is initial condition and α is fractional order. The negative terms of α refer to the fractional integral as opposed to the positive numbers of α representing the fractional derivative.

The Controller System

To control a system effectively, the controller's parameters have to be optimal, otherwise the system response will be skewed or the system operation unstable. Many methods have been developed to determine the optimal parameters for traditional PID controllers, including Ziegler-Nichols, Cohen-Coon, Tyreus-Luyben, artificial intelligence methods and so on. These compare to not so many methods for fractional systems.

In recent years, artificial intelligence (AI) techniques have emerged as alternative to optimally designing fractional controllers. One such method is Artificial Immune Systems (AIS), an algorithm that uses learning and memory characteristics of the vertebrate immune system to search for a solution in the computational parameter space. When the foreign body, called antigen (Ag), penetrates a system, the immune system immediately accesses its memory to find a suitable protection cell, called an antibody (Ab). If no appropriate matches are found, the system obtains the second best Ab for that Ag, based on their affinity. This specialty of AIS is used to get optimal parameters for the controllers in our approach.

Other two algorithms we involved in the study are differential evolution (DE) and the genetic algorithm (GA). Both are based on Darwin's evolution theory, with GA especially being a very popular tool among researchers and engineers.

GA is based on the principle of survival of the fittest, where the "fittest" may mean healthiest, strongest or most intelligent individual. First of all, the algorithm starts with randomly selecting individuals and then applying a crossover process, where chromosome exchange occurs between those individuals (parents). Following that, a mutation process provides diversity of individuals. The same processes repeat until a limit of iterations is reached or a specific function requested.

Another similar method is particle swarm optimization (PSO), a population-based algorithm inspired by social behaviour of animals like flock of birds, school of fish, a herd, and so on. The meaning of social behaviour relates to a job of the group, such as searching for food, hiding from a predator, and so on. For example, a flock of birds will circle over a region looking for food, and as soon as one of them finds or gets closer to a source of food, it informs the rest, which then group together around it. This process continues until the group reaches the food.

From algorithm standpoint, these birds are individuals, also known as particles, with their own velocities and positions that change with each iteration. Positions of particles are expressed as vector $x_i = (x_1, x_2,...)$, with their velocities vector $v_i = (v_1, v_2,...)$. These have their best positions, named p_{best}, and that vector set is $p_{besti} = (p_{best1}, p_{best2},...)$.

Similarly, global best positions, g_{best}, are stored as a vector $g_{besti} = (g_{best1}, g_{best2},...)$. The particles aim to approach the global best position with the best fitness value. The velocity and position of particles are updated with each iteration:

$$v_i^{k+1} = w.v_i^k + c_1.rand^k.\left(pbest_i^k - x_i^k\right) + c_2.rand^k.\left(gbest_i^k - x_i^k\right) \quad (1)$$

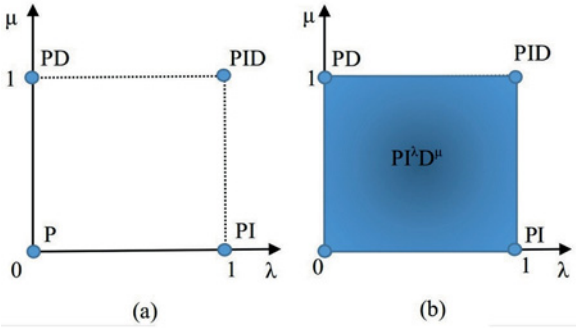


Figure 2: Controllers in the λ - μ plain

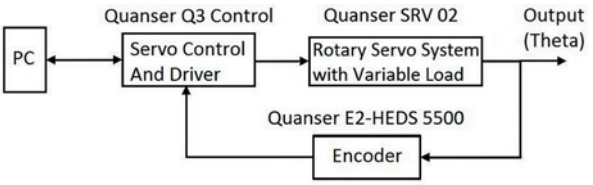


Figure 3 : The plant block diagram

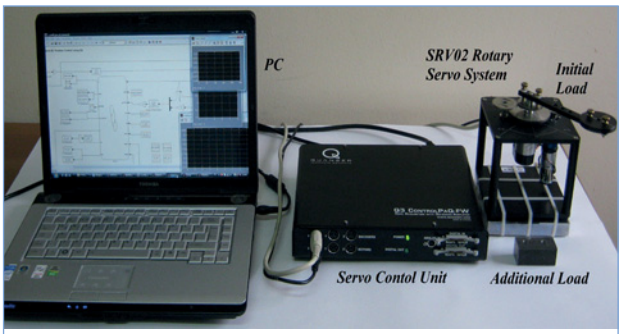


Figure 4: Applied experiments

$$x_i^{k+1} = x_i^k + v_i^{k+1} \quad (2)$$

where c_1, c_2 and w are coefficients related to acceleration and inertia weights.

Optimizing Controllers

The algorithms mentioned in this article have the common aim of determining optimal parameters for a system. Equally, all these algorithms are in need of an objective function, described as a multi-variable, together with error and control inputs:

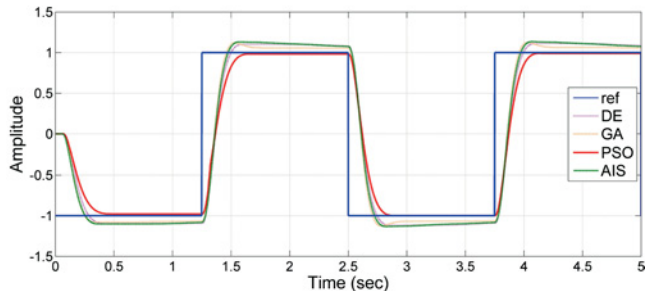


Figure 5: IO-PID controller output curves to square input

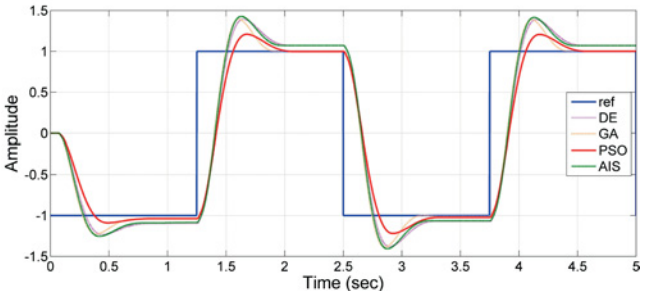


Figure 7: IO-PID controller output curves to square input with additional load disturbance

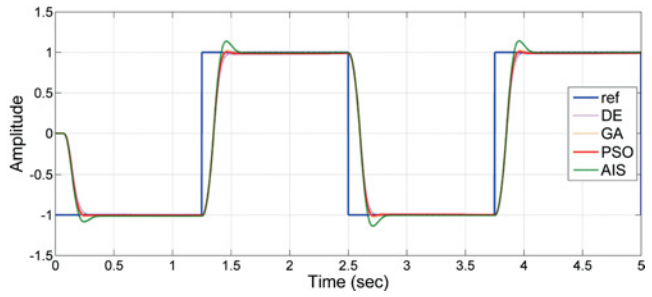


Figure 6: FO-PID controller output curves to square input

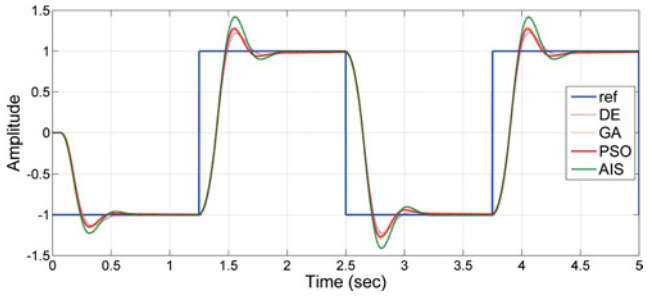


Figure 8: FO-PID controller output curves to square input with additional load disturbancewith additional load disturbance

SYMBOL	DEFINITION	VALUE
V	Nominal voltage of the DC motor	6 Volt
R	Motor armature resistance	2.6 ohm
L	Motor armature inductance	0.18 mH
kt	Motor torque constant	0.00767 N.m / A
kb	Motor back-EMF constant	0.00767 Volt /(rad/sec)
Ng	Total gear ratio (N2/N1)	70
ng	Gearbox efficiency	0.90
Jm	Motor inertia	4.6 x 10-7 kg.m2
Bm	Motor viscous damping coefficient	≅0 (negligible)
J l_in	Initial load and gearbox moment of inertia	4.83 x 10-7 kg.m2
J l_sub	Additional load and gearbox moment of inertia	4.83 x 10-6 kg.m2
Bl_in	Initial load viscous damping coefficient	4.41 x 10-6 Nm/(rad/sec)
Bl_sub	Additional load viscous damping coefficient	3.41x 10-5 Nm/(rad/sec)

Table 1: Parameters of the used load and rotary servo system

Controller Type	IAE	ISE	J	Controller Parameters				
				Kp	Ki	Kd	λ	μ
AIS based IO-PID	1.680	1.764	1.684	1.5726	1.0613	0.0204	-	-
DE based IO-PID	1.713	1.787	1.715	1.3716	0.8583	0.0141	-	-
GA based IO-PID	1.406	1.609	1.409	1.6965	0.5798	0.0125	-	-
PSO based IO-PID	1.435	1.686	1.435	1.0787	1.99e-4	9.67e-5	-	-
AIS based FO-PID	1.267	1.538	1.284	1.1344	1.4855	0.7759	0.2448	0.3016
DE based FO-PID	1.204	1.503	1.216	0.9840	0.8687	0.9665	0.6073	0.2719
GA based FO-PID	1.204	1.506	1.226	1.0089	1.9479	0.6902	0.2165	0.4276
PSO based FO-PID	1.190	1.492	1.212	1.6815	1.3055	0.6558	0.2997	0.4315

Table 2: Different algorithms based controller parameters and output values for square input in the loaded conditions

$$J = \int_0^t (w_1|e(t)| + w_2 u^2(t))dt \quad (3)$$

where e(t) is error, u(t) is time-dependent control input, and w_1 and w_2 are coefficients of error and control input.

For all the algorithms in our study we chose the iteration number to be 50, and the lower and upper limits of controller parameters are selected as K_p = [0-2], K_i = [0-2], K_d = [0-1], λ = [0-1], and μ = [0-1], where λ and μ are the order of integral and derivative terms, respectively.

For experiments we used the Quanser SRV02 rotary system; see Table 1 and Figure 3.

First of the experiments used initial load, and optimized IO-PID and FO-PID results are observed under the given square wave input (see Figure 5). It was seen that the system controlled by FO-PID has better results compared to IO-PID (see Figures 5 and 7). This means that from all optimization algorithms the best response is provided by the PSO algorithm.

Then the system was tested under variable load conditions (see Figures 6 and 7), to show the controllers' robustness. It was seen that the FO-PID controlled system has better results and the PSO algorithm gives the best controller parameters (see Figure 7).

Table 2 shows the loaded condition experiment results according to different performance indices. The lowest function value is provided by FO-PID, determined by the PSO algorithm.

Future Trends

It is found that fractional integral and derivative terms provide users with good design opportunities for controlling and modelling systems. We expect fractional calculus to be widely implemented in the future due to its flexibility and robustness.

The fractional controller is very helpful for advanced control in particular. If a system requires a high-level control structure, fractional controllers are best suited. On the other hand, it is very important to obtain this controller's parameters properly, and although not many methods exist to design fractional controllers, we suggest using optimization algorithms. Of these, the PSO method showed the most promise in terms of speed, effectiveness and simplicity, compared to other techniques. ●

Pickering PXI Switching & Simulation

We Already Have Your Solution.

Designed for Today's Most Demanding Electronic Test & Verification Applications

- **Huge range** of choices ranging from **low level DC to 1000 V, RF/Microwave to 65 GHz**
- **High-quality solutions** for most test applications including Aerospace & Defense, Automotive, Medical, Sensor Emulation, Hardware-in-the-Loop and Semiconductor
- Typical 15 to 20 year full product support
- All modules plug into any PXI chassis and also in our Ethernet controlled LXI Modular Switching chassis with a choice of 18 and 7 slots, plus our new 2-slot USB/LXI chassis
- Full range of supporting cable and connector solutions plus new on-line Cable Design Tool
- **18+ years** in PXI with a strong worldwide customer base
- Learn more at **pickeringtest.com/pxi**

3 Year Warranty — We stand behind our products with a standard three year warranty.

Switching | Programmable Resistors | Instrumentation | Custom Design | Connectivity & Cables

Scan this QR Code or go to
pickeringtest.com/pxi
01255 687900 | uksales@pickeringtest.com

pickering — Pickering Interfaces

AUTOMATION SYSTEM MANAGEMENT WITH PROGRAMMABLE LOGIC CONTROLLERS

BY **RUSTU GÜNTÜRKÜN**, ASSOCIATE PROFESSOR AT DUMLUPINAR UNIVERSITY, AND **ERHAN GÜNGÖR** FROM THE SIMAV TECHNICAL AND INDUSTRIAL SCHOOL FOR ELECTRONICS, KÜTAHYA, TURKEY

The development of low-cost computing has brought on the revolution of the Programmable Logic Controllers (PLCs), now widely used in analog and digital control systems in various sectors, from industrial and robotics to automotive – one of the largest users of PLCs.

The PLC was initially destined to be an electronic replacement for hard-wired relay systems. In 1968, an engineer called Dick Morley was working on a project, where he effectively created the first PLC. Nowadays, the PLC is a small computer with a built-in operating system. A soft PLC can run on a desktop computer and interface with industrial I/O hardware whilst executing programs within a version of commercial operating systems adapted for process control needs.

PLC Structure

PLCs are equipped with special input-output units suitable for direct use in automation systems. Inputs are typically connected to sensors loaded with information about levels, pressure, temperature and other parameters, whereas outputs are typically connected to drive components of remote circuit units, such as solenoid valves, for example.

PLCs are designed to be operated with little knowledge of computers and computer languages, and their programming can be managed by handheld, portable and desktop devices or computers.

PLCs are widely used in industry to control, monitor and operate technical and manufacturing processes. A need has been identified in industry for automating layered manufacturing systems, where processes are pre-defined to make them fully automated, similar to many Computer Numerical Control (CNC) systems. CNCs are expensive, physically large and difficult to program, making PLCs more accessible, as they are easily programmed, they communicate with other systems (PLCs, computers and portable devices) and are competitive in both cost and the space they occupy.

Typically, a computer converts a design produced by Computer Aided Design (CAD) software into data and then on to manufacture.

A New Model

We developed a loading and storage system based around a PLC. Our model is created to engage minimum labour in manufacturing, as it requires only one operator. In our system each step is observable on a panel.

Our model can be used for different purposes, such as cargo loading or indeed in academia, where students can learn about PLCs programming. Cargo handling is widely used in so many fields and, in the case of our model, the only change necessary is to re-program the PLC to handle various loads or processes. In case of a breakdown, the PLC helps pinpoint and fix the fault.

Our load-handling and storage model comprises a three-axis

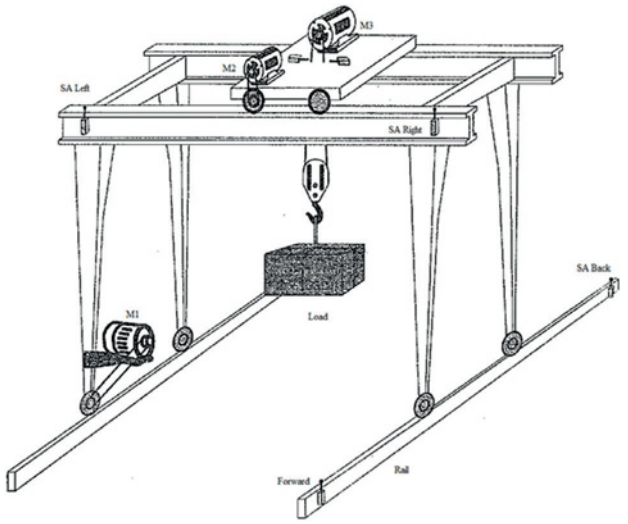


Figure 1: The loading system setup

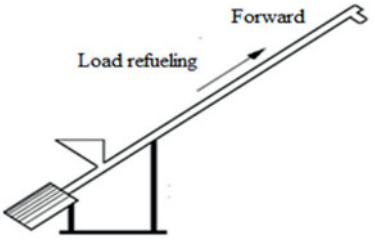


Figure 2: Spring setup

Mobile has become fundamental to our everyday lives. It has inextricably changed how we communicate, interact, work and play as individuals. It is transforming entire industries, bringing new levels of productivity and efficiency to enterprises.

Over three decades, mobile has evolved from an emerging communications technology to a phenomenon that is now at the foundation of everything we do. How can we describe the role of mobile in today's world?

Elemental.

Mobile is revolutionary, dynamic, ever adapting. It's the force behind every emerging innovation, every forward-thinking enterprise. Join us in Barcelona for Mobile World Congress 2017, where the world comes together to showcase, celebrate and advance mobile.

GSMA MOBILE™ WORLD CONGRESS

BARCELONA 27 FEB - 2 MAR 2017

#MWC17

WWW.MOBILEWORLDCONGRESS.COM

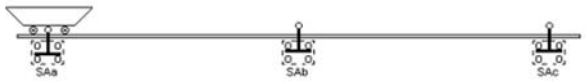


Figure 3: Cart setup

crane, a transportation cart, loading spring, five asynchronous motors, a PLC and TD 200 operator panel. The main platform located in the crane system (see Figure 1) moves on the forwards-backwards axis, right to left, and the rope (iron cable that moves the crane's hook whilst carrying the load) moves on the up-down axis.

The main platform consists of two keys, used to stop the system if there is a problem, whereas the top platform consists of three keys and a rope-carrying system. When the crane hook is lifted, the crane cable whips into the socket adjacent to the hoisting engine. To prevent the hoisting engine from locking up, a breakpoint switch is used.

> In our system, all machinery and motor parts are controlled by a PLC, making the whole setup flexible through programming

The Control Flow

Our system operates in a cycle; see Figure 2. The path consists of collecting, filling, feeding, classification and re-collecting the load. The system is controlled by a Siemens s7 200 PLC with the 224 CPU (see Figure 3). The CPU controls the conveyor, spring, pneumatic valve and three-axis crane and communicates with the TD 200 operator panel. All actions are transmitted to the operator via messages on the TD 200 panel.

If needed, memory units for each phase of the loading and storing can be added to the system, but this will require additional software and external commands.

The system can handle more than one load and differentiate between them. For example, if wheat arrives to the wheat silo by a transporter (container, train, truck, ship etc.), only the "wheat" button will be pressed and the storage process will continue until no wheat is left on the transporter. If, say, wheat and beans come with two transporters, there are functions representing each grain and storage of both products will be carried out seamlessly.

In our system, all machinery and motor parts are controlled by a PLC, making the whole setup flexible through programming. Classical control systems require a lot of cables, which is expensive, and their management complex. In a PLC-based system there are no cables and therefore no opportunity for a mix-up, which is always present in classical control systems. ●

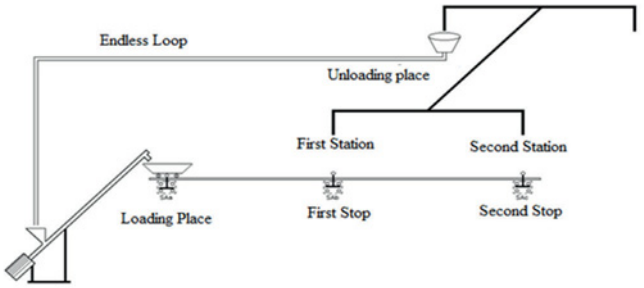


Figure 4: The system's flow setup

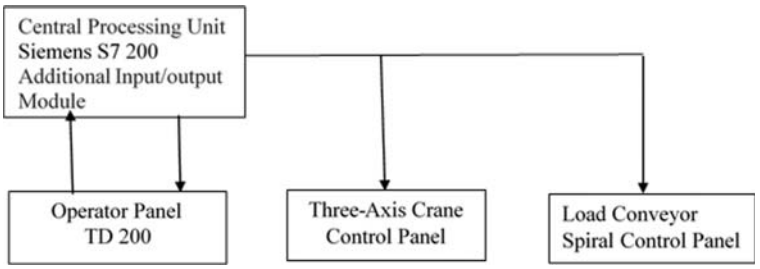
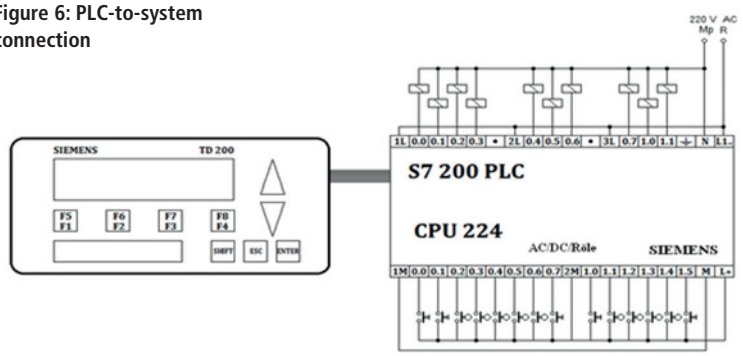


Figure 5: The system is controlled by Siemens S7 200 PLC 224 CPU

Figure 6: PLC-to-system connection



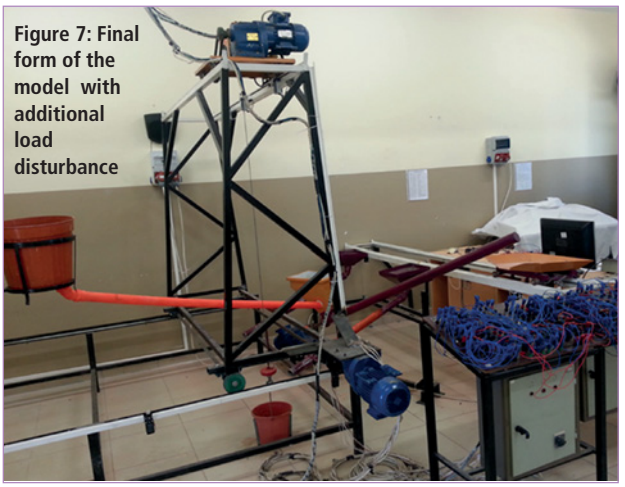


Figure 7: Final form of the model with additional load disturbance

WHAT'S NEW IN ELECTRONICS LIVE!

incorporating The PXI Show | EMC UK 2017

Bringing the World of Electronics Together

9 – 10 May 2017 NEC Birmingham

Register Free @ www.wnie.co.uk/live

What's New in Electronics Live - the only completely dedicated UK Electronics event. WNIE LIVE is the meeting place for the entire UK electronics industry to showcase the latest technologies, exchange ideas, educate, network and re-connect.

Joined this year by EMC Live and The PXI Show don't miss out on being part of WNIE Live

With live features, conferences, seminars and technical forums. Book the 9th - 10th May into your diary.

Networking has never been easier

Delivering unrivalled visitor engagement

Keep the conversation going 24/7 at wnie.co.uk

THE INDUSTRY HUB
FOR EVERYTHING ELECTRONICS

www.wnie.co.uk/live

Email: info@wnie.co.uk Call: + 44 1428 609 382

FREE ENTRY
FREE PARKING
FREE WIFI

THE WORLD OF ELECTRONICS ON YOUR DOORSTEP

Southern Manufacturing and Electronics 2017 returns to FIVE, Farnborough, from March 21st to 23rd. This UK engineering technology show ends its second decade with a move to new dates in early spring. More convenient timing, combined with significant infrastructure developments to improve access and facilities at the show's site alongside Farnborough Airport, are expected to encourage visitors in record numbers this year.

The Southern Manufacturing and Electronics Show has for many long been the most significant national electronics show in the UK. Its extension to a three-day tenure two years ago helped it raise its international profile significantly, with the result that the event now attracts not only an impressive cross-section of the UK electronics industry but quite a few major overseas exhibitors as well, many of whom will be exhibiting for the first time in 2017.

www.industrysouth.co.uk

BOSCH REXROTH ANNOUNCED AS HEADLINE SPONSOR OF INDUSTRY 4.0 SUMMIT

The rapidly increasing numbers of connected people and objects are beginning to transform many aspects of industry, having a fundamental impact on value creation in manufacturing. The concept of Industry 4.0 is opening up new potential for productivity, quality and efficiency. As such the Industry 4.0 Summit will address these issues this year, when Bosch Rexroth will also sponsor the Summit.

"This is a great opportunity to meet, listen and network with other key players in the industry," said Sean Kilgallen, Marketing Manager at Bosch Rexroth. "Bosch Rexroth is in a unique position to help drive the next industrial revolution, as both a lead operator and lead supplier of Industry 4.0 solutions. We are compiling real-life experience in outfitting our plants with Industry 4.0 technology."

www.industry40summit.com/register/

RITTAL LAUNCHES TWO NEW VERSIONS OF LED SYSTEM LIGHTS

Rittal's series of specially-designed lights will include 600 and 400 lumens of light output (luminous flux) to add to the current 1200- and 900-lumen versions. This means that Rittal can now offer lighting solutions to suit all size enclosures, from small housings right up to large systems.

The new lights are designed to enable control and switchgear manufacturers to provide lower light output for smaller enclosures. The 600-lumen version meets the standard requirement for the large TS 8 enclosure while the 400-lumen lights are suited to wall-mounted enclosures, such as the Rittal AE compact enclosure series.

An optical cover made of transparent plastic, in which a Fresnel structure is integrated, provides optimal illumination, focusing the light so that the entire enclosure can be illuminated.

www.rittal.co.uk

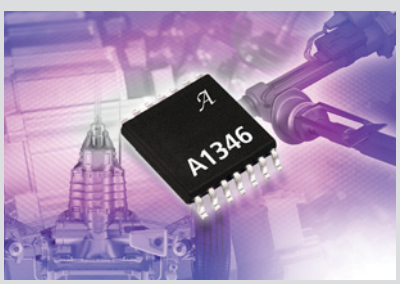
DUAL-DIE HIGHLY PROGRAMMABLE LINEAR HALL SENSOR IC FOR SAFETY-CRITICAL APPLICATIONS

The new A1346 from Allegro MicroSystems Europe is a dual-die, highly-programmable linear Hall sensor IC that is an ideal solution for safety-critical applications.

The A1346 incorporates full die redundancy with the added benefits of full diagnostics. The combination of these two features allows for a higher level of diagnostics without interruption to the application (where diagnostics would otherwise render a die temporarily unresponsive), and that the controller knows which die to trust when outputs don't agree.

The new device incorporates dual high-precision, programmable Hall-effect linear sensor integrated circuits with open-drain outputs, for both automotive and non-automotive applications. The signal paths in the A1346 provide flexibility through external programming that allows the generation of accurate and customised outputs from an input magnetic signal.

www.allegromicro.com



WURTH ELECTRONICS MIDCOM ANNOUNCES NEW DESIGN CONTEST

Now open to the public, Wurth Electronics Midcom announces the "Off The Clock Design Challenge", the premiere design challenge built for those who like to tinker. Participants will be designing a wireless-charging end-product using the new 15W wireless charging kit developed with ROHM Semiconductor.

Contenders chosen to design during the contest, and who meet the requirements, will receive a 3Doodler pen and accessories, valued at $150, and have the chance to win an XYZPrinting 3D printer, valued at $499, or a Hakko FX 951 soldering station with Chisel Tip pack, valued at $295. Contenders will be judged on social media exposure, blog postings, innovation and creativity.

Applications for the "Off The Clock Design Challenge" are due by February 17th, 2017, and designing starts March 10, 2017.

www.we-online.com/offtheclock

RTI FUSES CONTROL WITH BLUOS MULTI-ROOM MUSIC APP

RTI, control and automation manufacturer for residential and commercial settings, announced a new two-way driver for the full portfolio of BluOS-enabled devices from Bluesound and NAD Electronics, the leaders in wireless high-resolution, multi-room music systems. Developed by Lenbrook, the parent company of Bluesound and NAD, the new driver seamlessly incorporates the BluOS sonic streaming experience into RTI's powerful automation and control ecosystem.

BluOS is the operating system that powers select NAD devices and all Bluesound players. The proprietary system allows any BluOS-enabled device to connect to a home Wi-Fi network to access many popular streaming music services or a networked library of music. The music can then be streamed to one or many BluOS devices, even if the devices are located in different rooms of a home.

www.rticorp.com

ANDREAS SCHNEIDER BECOMES THE NEW CEO OF ENOCEAN

EnOcean announced that Andreas Schneider, the co-founder and Chief Marketing Officer of EnOcean, is the company's new Chief Executive Officer (CEO) as of January 1, 2017. In this position, Schneider is expected to further expand EnOcean's business in line with its long-term strategy in the self-powered IoT for the core markets of building automation, smart homes, LED light control and industrial automation. He replaces Dr Wald Siskens, who left the company to join Apple.

As the co-founder and CMO of EnOcean, Schneider has been responsible for market positioning and the sales strategies for energy harvesting wireless technology since 2001. He played a key role in strengthening the company's position as leading supplier of energy-harvesting wireless technology for maintenance-free applications in the Internet of Things.

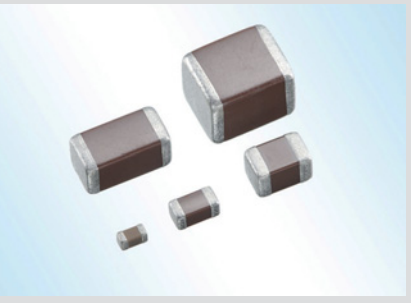
www.enocean.com

EXPANDED LINE-UP OF AUTOMOTIVE-GRADE MLCCS FROM TDK

TDK has expanded its CGA series of automotive-grade multilayer ceramic chip capacitors (MLCCs) for high-temperature applications, featuring X8L temperature characteristics and extended X8R types. This brings the new TDK line-up of X8L and X8R MLCCs to an unrivalled high capacitance range of up to 22µF, high reliability at temperatures from -55°C to +150°C, and capacitance drift of just ±15% for the X8R types and +15/-40% for the X8L types.

Automotive electronic control units are increasingly being located in the engine ompartments or near other structural parts, where the electronic components must be able to withstand high temperatures and offer high reliability and performance. The new high-temperature MLCCs were made possible by the development of a new dielectric material that maintains excellent reliability in such extreme environments.

www.global.tdk.com

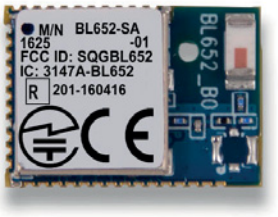


LAIRD BL652 BLUETOOTH AND NFC MODULE FOR EIOT NOW AT ALPHA MICRO

Alpha Micro Components has begun distributing a new secure, certified Bluetooth Low Energy (BLE) v4.2 and Near Field Communication (NFC) module – the Laird BL652. The standalone module is compact, energy-efficient and powerful. Its tiny footprint offers multiple interfaces and an easy-to-use application development environment for secure connectivity into Enterprise Internet of Things (EioT) devices without impacting power budgets or space limitations.

The BL652 already features hardware to incorporate the speed and range offered by Bluetooth 5, pending ratification. The BL652 series is claimed to be the most complete solution for adding Bluetooth Low Energy and NFC support to EioT devices, from development and integration to future support – including upcoming support for Bluetooth 5, when the BT 5 specification is published.

www.alphamicro.net



XP POWER'S 18-36W DESKTOP POWER SUPPLIES MEET LATEST ENERGY STANDARDS

XP Power introduced four new series of external/desktop power supplies that meet the latest level VI and CoC Tier 2 green standards. The single-output power supplies are perfect for applications needing low-power, external, 18, 24, 30 or 36W power source to meet current legislation aimed at increasing energy efficiency and reducing no-load power consumption.

The VET18, VET24 , VET30 and VET36 ranges feature a high average efficiency of up to 87% typical, measured at 25, 50, 75 and 100% load conditions. Accordingly, they meet the requirements from the Department of Energy (DoE) in the US and the Code of Conduct (CoC) Tier 2 in the EU.

The new legislation requirement lowers the no-load power to less than 0.075W for the 6-36W output power level, which the VET series power supplies now meet.

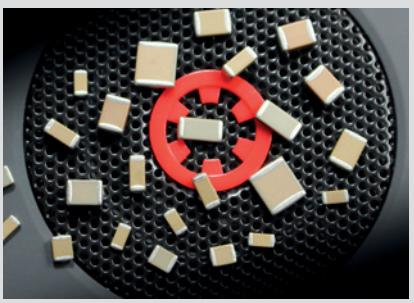
www.xppower.com

KNOWLES X8R MLCCS ARE NOW LEAD-FREE

Knowles Capacitors has qualified its X8R dielectric material to be Lead (Pb) free. Knowles is committed to developing more environmentally-friendly materials, as well as ensuring continued compliance to existing requirements along with potential future changes to the EU RoHS directive.

This new dielectric material will replace the company's current X8R materials that contain Lead (Pb), though these remain available on request. The new material will be used for standard X8R Multilayer Ceramic capacitors (MLCCs) and AECQ200 MLCC X8R Multilayer Ceramic Capacitors for all voltage ratings (50V-3kV) and capacitance values 100pF-2.2uF. Case sizes range from 0805 to 2225.

www.knowlescapacitors.com



PHOTOIC COUPLER FOR HIGH-SPEED COMMUNICATION

Panasonic's components spectrum is now extended by a PhotoIC coupler, a device that allows high-speed signal transmission combined with an optical isolation between input and output. Main applications are in the field of measurement equipment and factory automation.

The built-in light-receiving IC allows communication speeds of 50Mbps (typical) and a guaranteed performance at temperatures of -40°C to 105°C. With a CMTI of min. 15kV/µs, the PhotoIC coupler offers high resistance against noise on the transmitted signal. These features are combined in a small package size of 4.4mm x 4.3mm x 2.1mm (SO6 5 pin). Signals can be transmitted via a variety of communication standards, from Fieldbus and Ethernet to RF and so on.

www.panasonic-electric-works.co.uk

SOUTHERN 17 Manufacturing & Electronics

FIVE | Farnborough | Hants | GU14 6XL

21st – 23rd March 2017
9.30am – 4.30pm (3.30pm close Thurs)

Incorporating The Subcontract Engineering Exhibition
AUTOAERO
FIVE FARNBOROUGH • 21-23 MARCH 2017

FREE SEMINARS
FREE PARKING

The UK's top Manufacturing and Industrial Technology Exhibition

Meet over 800 national and international suppliers under one roof in Farnborough this March at Southern Manufacturing & Electronics (inc AutoAero) 2017.

See live demonstrations and new product launches of machine tools & tooling, electronics, factory & process automation, packaging & handling, labelling & marking, 3D printing, test & measurement, materials & adhesives, rapid prototyping, ICT, drives & controls and laboratory equipment.

Free industry seminar programme online @ **www.industrysouth.co.uk**

The exhibition is **free** to attend, **free** to park and easy to get to. Doors open at 9.30am on Tuesday 21st March.

Pre-register online now for your free entry badge and show preview at **www.industrysouth.co.uk**

SOUTHERN MANUFACTURING & ELECTRONICS
is an ETES event organised by
European Trade & Exhibition Services Ltd

Tel 01784 880890 · email philv@etes.co.uk

etes Regional Manufacturing Exhibitions

Register here with your smartphone