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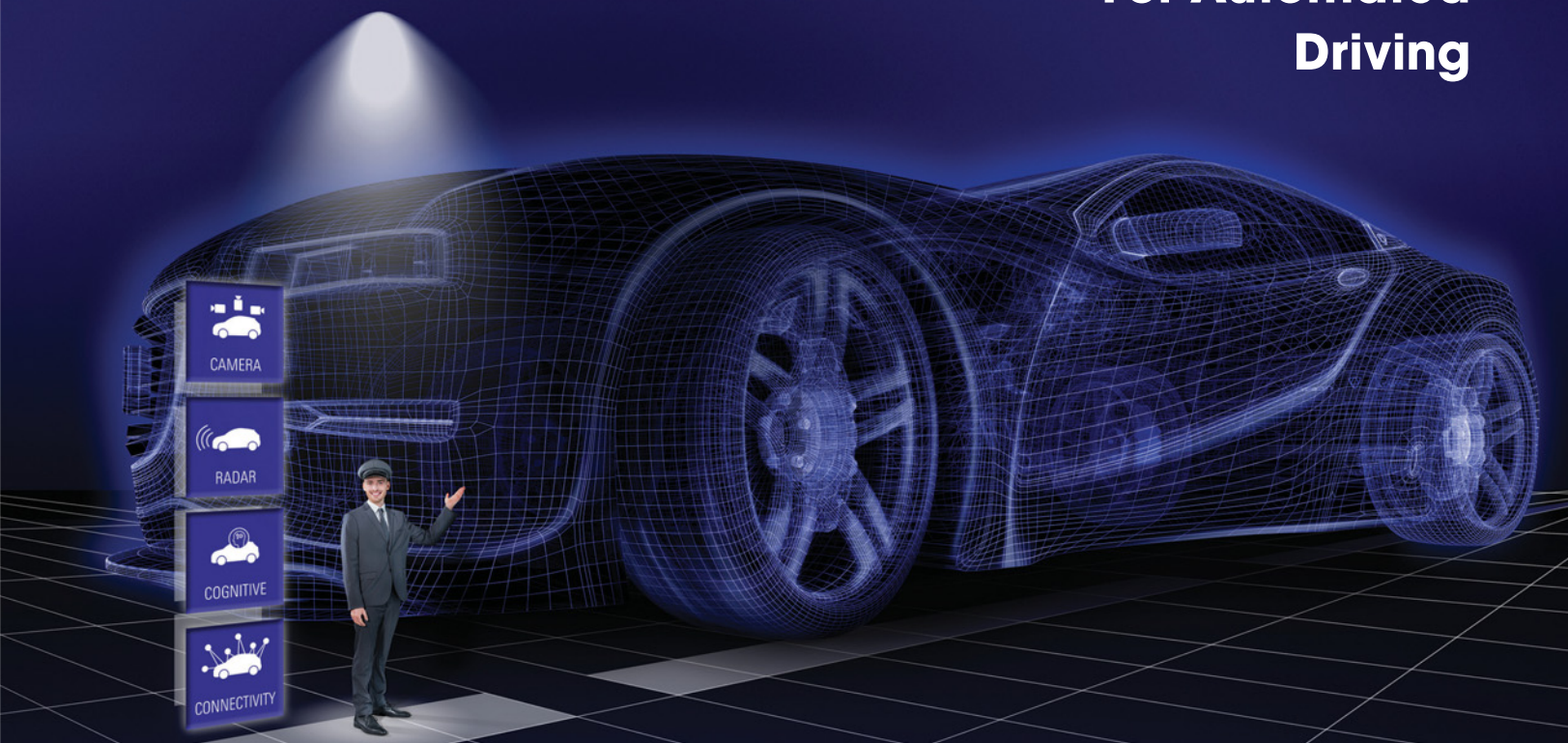

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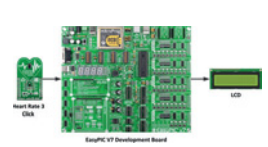

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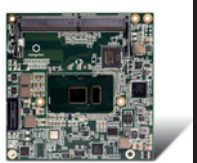

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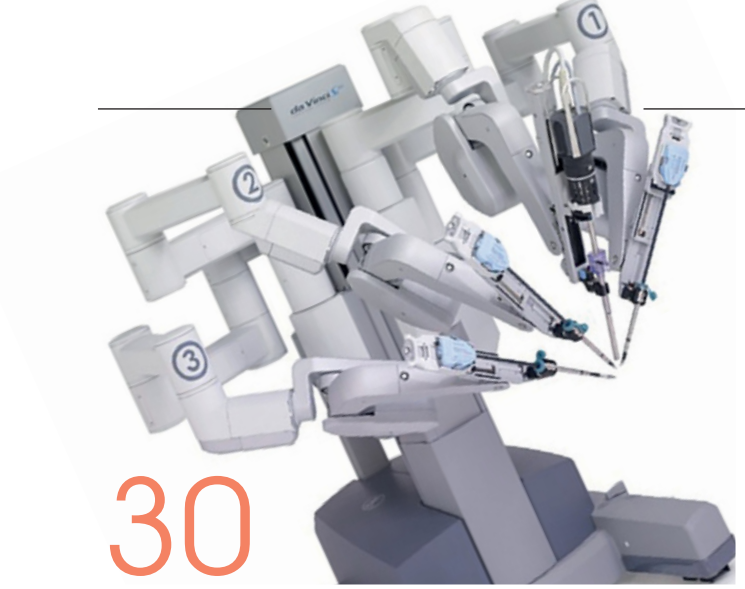

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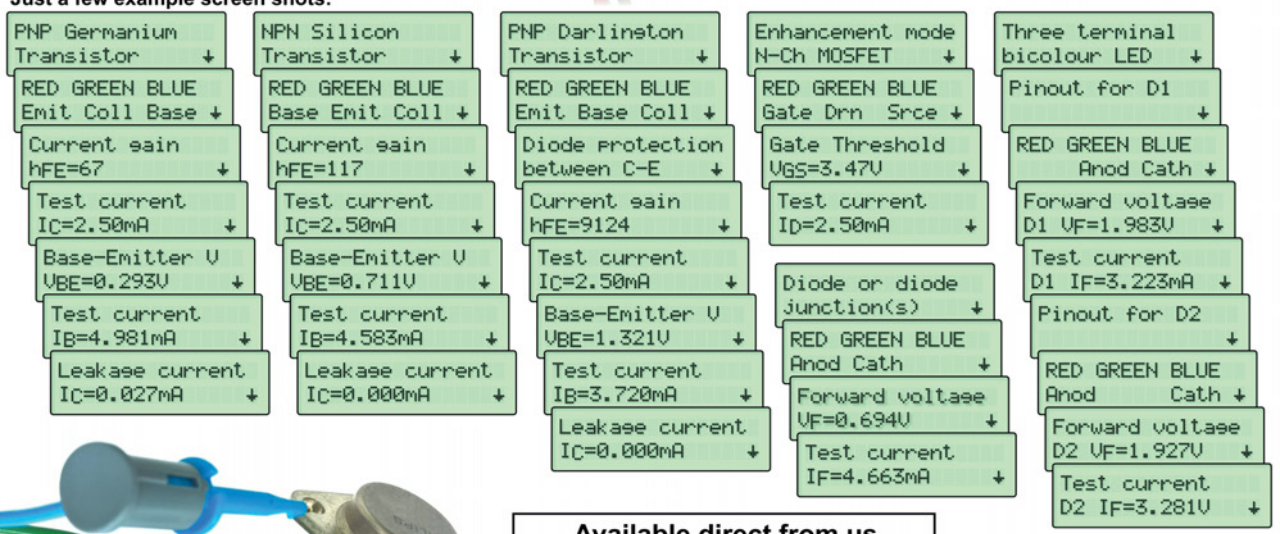

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UK UNIVERSITIES FAIL TECH BUSINESSES, RESEARCH SHOWS

> The survey highlights the immense value of internships, which must be encouraged

Over 40% of UK graduates fail to get a graduate-level job after leaving university, according to research by Intern Tech, a UK-based organisation that creates bespoke, international and national internships for young adults.

University students finding suitable placement is so poor that over five million of them regret the time and money spent on their degree. Some 48% of UK graduates don't know how to secure the country's most sought-after jobs within the technology sector and other industries.

Nearly 30% of the survey participants believe their degree courses are outdated in the present-day job market, and some 45% say internships and work placements have been more valuable to them in their professional life than degrees. The findings come at a time when 93% of UK technology firms complain of a shortage of skilled workers, holding their businesses back.

Over a third (35%) of the university graduates surveyed have paid for the training required for further qualifications in the skills they need to pursue their chosen jobs, leaving them with a post-course average debt of £44,000.

Areas Of Concern

One main area of concern listed in the research is the lack of knowledge and understanding surrounding the UK's technology jobs. When presented with a list of the country's most sought-after roles in the tech industry – such as data scientist, cyber security specialist and app developer – nearly half of graduates said they don't know what these jobs entail or how to secure one.

"The research has illustrated that universities are failing to equip graduates with the skills and experience they need in the professional world. Consequently, a vast number of degree holders in the UK are left regretting the debt they have been burdened with from university as they are still forced to take jobs below graduate-level or must complete further qualifications to get ahead. Meanwhile, the country's innovative high-growth companies are being held back by an inability to find the skilled workers they need – clearly something must be done," said Aaron Wilson, Managing Director of Intern Tech.

"In the Spring Budget the UK government signalled its intent to address the skills gap through T-level qualifications and additional funding for STEM subjects. However, this survey highlights the immense value of internships, which must be encouraged – they provide young people with vital insight and experience into the jobs and industries they wish to work in."

"With university education criticised as outdated, it is essential that students and graduates are encouraged to get hands-on work experience, in turn enabling companies to find potential employees with the culture, attitude and core skills they require," added Wilson.

Intern Tech creates bespoke, international and national internships for young adults, university students and career changers around the globe (www.intern-tech.com)

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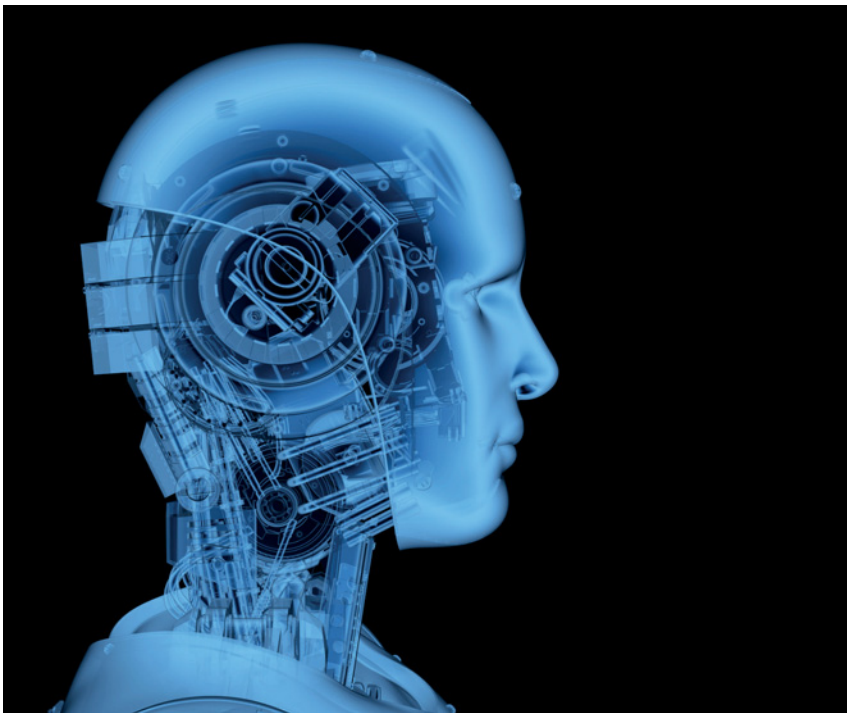
TECHNOLOGY FIRMS MUST RESIST HYPE AS THE UK GOVERNMENT ANNOUNCES £500M INVESTMENT

The UK government announced an additional £500m in funding to science, technology and innovation in its spring budget. Particular support will go toward electric vehicles, robotics and artificial intelligence (AI), but investment will also include 5G mobile technology and broadband networks.

"It's fantastic to see this recognition that technologies such as robotics and AI are essential components of the UK's economy," said Ben Boswell, UK and Ireland Director of World Wide Technology. "But since it's such an exciting time in the market with this extra investment, there is an associated risk that certain technologies can become overhyped. Businesses trying to take advantage of multiple new technologies can end up leaping without looking."



Boswell encourages decision makers to think hard about the full process of technology integration from idea to outcome, which can easily be neglected in the race against time, to ensure the UK is at the forefront of global innovation and competitiveness.

"The problems that consumers and businesses are trying to solve must be at the heart of new technologies," said Boswell. "We must ensure that heady days like this one, when the industry is enjoying the prospect of such investment, lead to outcomes that deliver real value for the country."

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MATTER WAVE GYROSCOPE COULD OFFER PRECISE DIRECTION IN ABSENCE OF A GPS SIGNAL

Researchers in the US have developed a protocol for a highly sensitive and compact gyroscope, capable of measuring very small changes in rotation. The design could form part of an inertial navigation system and offer directional information in the absence of GPS signals.

The proposed detection boost arises from the use of matter waves supported by an ion trap, but the operating principle is similar to fibre-optic gyroscopes available today. Rotation is detected as a shift in the interference pattern generated inside the device.

"The matter wave will make many repeated round trips in the ion trap, just like the light waves in a coil of fibre," said Wes Campbell of UCLA. "This is the key to shrinking down the device size."

Matter waves – a description referring to the wave-like behaviour of atoms and other charged particles – allow extremely precise measurements of rotation, but typically only when the interferometer track is spread over a relatively large area.

What's more, while gyroscopes based on photons (light) can have paths that loop around many times, there are fewer ways to achieve this with matter waves. But thanks to the use of an ion trap, which allows particles to bounce repeatedly back and forth, the scientists believe the concept could be made to fit inside vehicles, spacecraft and other systems.

DISRUPTIVE ARCHITECTURAL BREAKTHROUGH FOR 5G UNVEILED

Xilinx has made a 5G wireless breakthrough by integrating RF-class analogue technology into its 16nm All Programmable MPSoCs. The new All Programmable RFSoCs eliminate data converters, providing a reduction of 50-75% in power consumption and footprint, suitable for 5G massive-MIMO and millimetre-wave wireless backhaul applications.

"Integrating RF signal processing into All Programmable SoCs enables our customers to dramatically change their systems' architectures," said Liam Madden, Corporate VP at Xilinx.

The integrated 16nm-based RF data conversion technology includes direct RF sampling for simplified analogue design and greater accuracy; 12-bit ADCs at up to 4GSPS, with high channel-count and digital down-conversion; and 14-bit DACs that run at up to 6.4GSPS, also with high channel-count, with digital up-conversion.

"The shift to FinFET technology blends high integration density with improvements in analogue device performance characteristics," said Boris Murmann, Professor of Electrical Engineering at Stanford University. "This enables the integration of leading-edge analogue/RF macros using a digitally-assisted analogue design approach."

RENESAS AUTONOMY™ – THE OPEN PLATFORM FOR AUTOMATED DRIVING

By Raed El Makhour, Staff Engineer for Radar at the Global ADAS Centre

All studies, which have been collected worldwide, show the same results: Most of the traffic accidents are due to human error, misbehavior or misjudgment by the vehicle drivers. At an early stage passive safety devices such as safety belt and airbag were introduced to at least minimize the impact of accidents to the occupants, but their capabilities are limited. Therefore, the automotive industry was looking for new ways to minimize the number and severity of driving errors. As a result driver assistance systems to assist the driver with the safety aspects – for himself and equally so for other mobile and pedestrian traffic participants. Next to this, ADAS is supposed to enhance the driving comfort for the driver and finally yet importantly improve the economic as well as the environmental balance.

Renesas has declared that ADAS and AD, as a next step, is a key focus segment within the automotive market. ADAS and AD applications need high-end computing power of SOCs (System on Chips) to analyse the car's surroundings and for cognitive computing, as well as high-performance control functions running on MCUs to steer the car safely and comfortably.

Renesas has been in the last decades the globally leading MCU and SOC supplier to the automotive segment. In 2016, Renesas shipped over 1 billion of those processing engines, with a high quality rate of less than 0.1ppm, serving nearly all key automotive players worldwide. Thus ADAS and AS is a natural field for Renesas. To better support this globally, Renesas inaugurated the Global ADAS Centre in 2014 and defined the Renesas autonomy solution platform.

Renesas autonomy combines the best of SOCs and MCUs with software and hardware solutions of Renesas and its ecosystem – not just for today's ADAS applications, but also for future autonomous driving solutions.

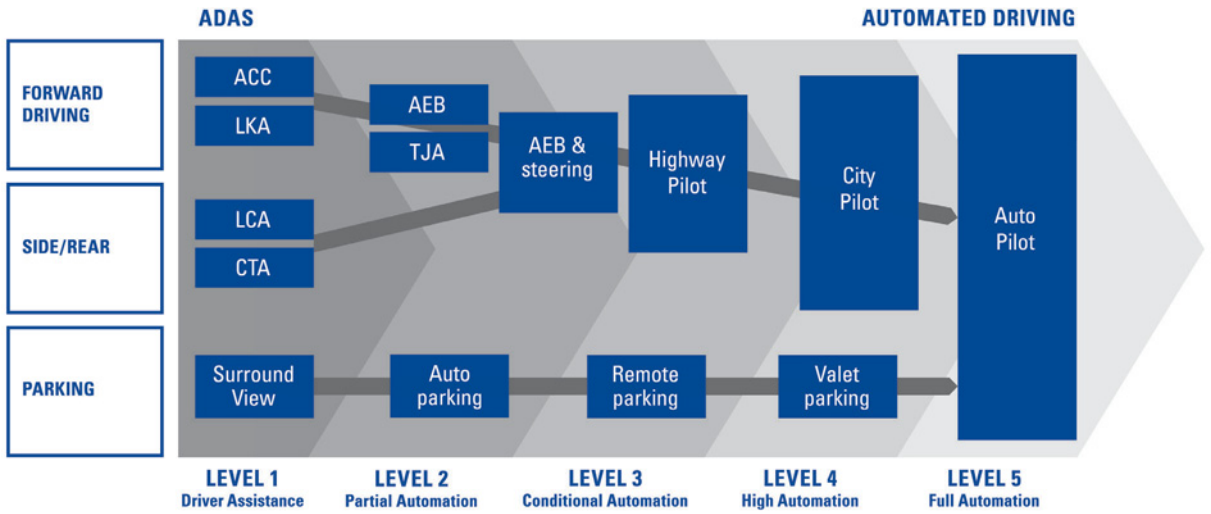
Key segments covered by Renesas autonomy initially are cameras and radar for sensing, cognitive for sensor fusion and decision making and V2x for communication.

Most advanced driver assistance systems assist the driver in his driving task by informing him or warning him, in some cases they are actively interfering in driving. But the next steps are already in development or in research. Already today, not only piloted driving on motorways is in discussion, but there has been running test drives for some time. And even if the piloted driving in the city is much more complex than on the motorway, the industry is also already working on it. The long-term goal of all these development efforts is the fully autonomous driving, in which the vehicle can handle all situations automatically and a driver is concentrating on something else.

In comparison to other sensor systems such as camera, ultrasound or LIDAR, radar sensors have some decisive advantages: radar sensors can measure precisely distances, speed and angles and easily detect multiple targets, e.g. vehicles, or persons, and track their movement. Typical Radar applications are blind spot detection, cross traffic detection, adaptive cruise control and automated emergency braking.

Adding those features will help the driver in having a safer and more comfortable journey. With increased market acceptance for driver assistance systems and autonomous drive evolving, car manufacturers are seeking to provide these features to differentiate their cars by enabling future driver assistance functions or gain higher ratings in public programmes such as the New Car Assessment Programs. The requirements for radar sensors in terms of range resolution, separation of objects and precision in measurement of velocity are also evolving.

While optical systems, such as infrared, LIDAR or camera, rely on good viewing conditions, radar sensors are more or



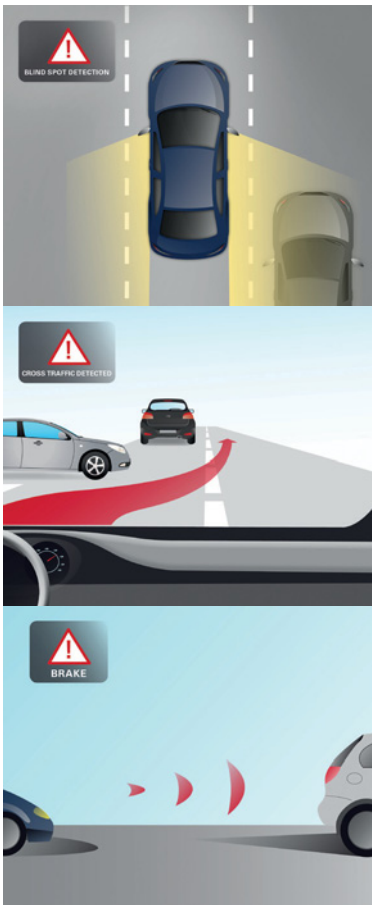
less unaffected by poor visibility conditions. Radar sensors use electromagnetic waves to detect objects - almost unrestrained by darkness, rain, snow, fog or dirt. Also fast changing light conditions, e.g. when traveling through a tunnel, are not an obstacle for radar systems. Moreover it is possible to mount radar sensors behind EM-transparent material such as bumpers or holographic car logos.

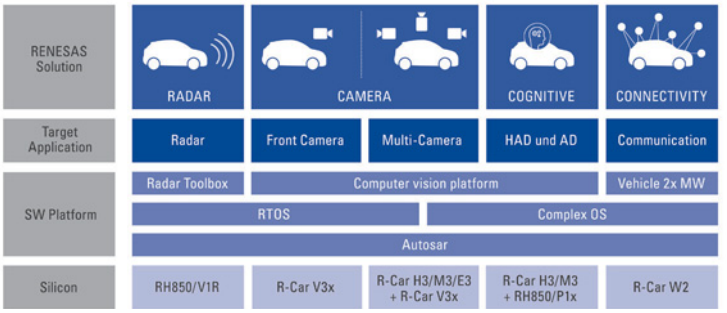
Renesas Radar Offer

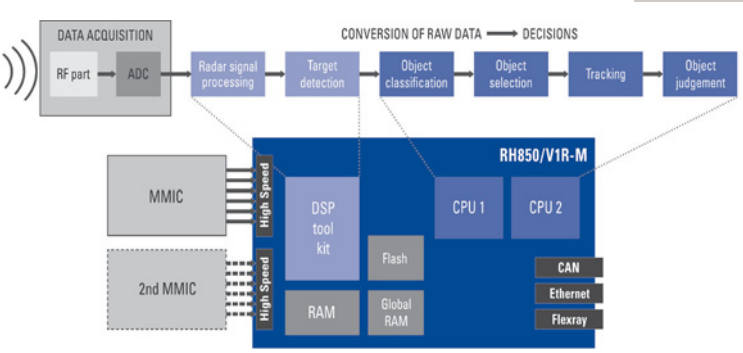
Renesas offers the RH850/V1R-M series a dedicated controller family, optimized for radar applications. RH850/V1R-M consists of 32-bit single-chip microcontroller with multiple CPUs, Code Flash, Data Flash and RAM. For the Radar function it incorporates a DSP toolkit (DSPSS) with additional RAM and has a high speed differential interface. This chip is compliant with the functional safety standard required in the automotive applications (ISO26262).

The high-performance DSP provides flexible programmability for improved radar signal processing performance and increased sensing accuracy. The optimized DSP allows the system developers to process the raw data into target objects efficiently, separately from the safety relevant classification and tracking done in the CPUs. Renesas' high performance DSP performs radar specific algorithms such as fast fourier transforms (FFTs), beamforming, windowing, channel calibration, peak search, at high speed and with low power consumption. The DSP offers high flexible programmability and Renesas specifically developed a DSP math library for automotive radar sensors to support system developers in their algorithm development.

Renesas low-power technology and embedded flash for more compact and low-cost radar sensors - The RH850/V1R-M is developed using Renesas' world leading 40nm embedded flash (eFlash) process technology, which has a proven track record in terms of re-write cycles, the industry's fastest random access operation speeds and high reliability. It also has the merit of low power consumption as the transistors are smaller lowering parasitic capacitances. The 40 nm technology has already been qualified in TSMC since March 2015. The principle advantage of SG-MONOS is the high reliability, because the charge trapping cells keep the charge even with oxide defects. This enabled the company to achieve zero defects though more than 700 million devices were already shipped. The process specification of RH850/V1R-M also fulfills the highest temperature requirements in the industry (T-junction 150°C). The embedded flash brings advantage to the system designer by offering higher integration using less PCB space and better real time behavior.







Dual core at 320MHz high performance, integrated 2MB large capacity RAM, 2MB highest speed flash and highest temperature requirements - the new RH850/V1R-M features two G3MH CPU cores operating at 320 MHz and are the highest performance cores among the RH850 Family. The G3MH is a superscalar RISC architecture with two 7-stage integer pipelines, which allows execution of two different instructions at the same time. Each G3MH core achieves the performance of 3.2 DMIPS/MHz. The RH850/V1R-M also includes 2MB industry-highest speed flash based on Renesas automotive 40nm embedded flash technology. By incorporating a large 2MB capacity RAM, the RH850/V1R-M handles all specific calculations on radar cube data such as range and velocity FFTs, digital beam forming, constant false alarm rate (CFAR) and peak detection.

A flexible programmable complete toolchain with C/C++ compiler, debugger, simulation models and detailed performance profiling tools will also be available.

Renesas also offers an evaluation board for the RH850/V1R-M quipped with all the necessary interfaces such as MIPI CSI2 and Aurora.

This complete offering becomes available to customers under Renesas autonomy platform, with the promise that the customer can decide what the future of driving will look like, using Renesas' solution for Radar. ●

Recommendations for the new (embedded) software developer

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

As mentioned in the previous column, after attending the recent Embedded World show in Nuremberg, I returned home with the stronger than ever before impression that "software was eating the (embedded) world!".

The last few weeks I have been thinking about this, wondering if it was time to re-consider how microcontrollers are being designed today and how to present them to a new, growing group: the software developers.

Ubiquitous

Microcontrollers are simply found everywhere, so we can't expect only (electronic) engineers to support the embedded development projects. We must acknowledge and embrace the much larger group of developers that exists, one that comes from a varied spectrum of backgrounds – from computer science graduates to the (often self-taught) Javascript/web developers. Hobbyists, hackers and DYI project makers are a part of the embedded world and use the same tools available to the embedded community, but perhaps without the complexity or the steep learning curves that go with them. I am referring to the proliferation of communities such as that of the Arduino.

Software Explosion

There's a school of thought that if embedded software is too hard, more software will help.

"More layers of abstraction (indirection) can help us solve any problem," said David Wheeler, the world first PhD in Computer Science.

Unfortunately, the result can be million lines of code (Linux) executed at blazing speed (1GHz) on a 64-bit processor, only to flip a single relay switch, as in one Raspberry Pi project (http://www.instructables.com/id/Raspberry-Pi-Garage-Door-Opener/).

I love the little board, but when it comes to controlling things in real time, all those layers of "indirection" get in the way. To get things done, they all end up bowing to "truer" embedded control solutions by means of 'hats' or 'shields', incorporating a leaner and inevitably harder solution, and often including a humble 8-bit microcontroller (https://www.raspberrypi.org/documentation/hardware/sense-hat/)!

New Perspective On Choosing Hardware

So, if the supremacy of software is inevitable, let's acknowledge it and let's see how modern microcontroller technology can best serve it.

What kind of hardware features would we recommend to new software developers to keep those many layers of abstraction to a minimum?

Below is my proposed list, next to some of the features that I have seen implemented in more recent microcontroller generations.

Pin Assignments

Probably nothing surprises or even annoys the software developer more than discovering the complexity behind a microcontroller's pin-assignment table. The more powerful the microcontroller (more peripherals), the more complex the problem becomes of selecting the right pin for a given function.

This is an easy one: I'd suggest looking for microcontrollers with Peripheral Pin Select (PPS), which multiplex *any* digital I/O on *any* pin.

In Listing 1 there's an example of pins RB6 and RB7 being assigned to the UART peripheral:

```
RB6PPS = PPS_FN_UART1_TX; // RB6 <- UART1:TX1 output

U1RXPPSbits.U1RXPPS = PPS_PIN_RB7; // UART1:RX1 <- RB7 input
```

Listing 1: Assigning two I/Os to the serial port (UART) of a PIC18F25K42

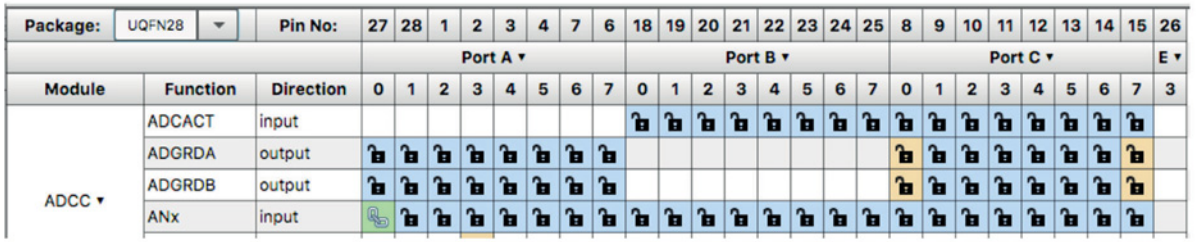


Figure 1: I/O selection grid for the PIC16F18855

Analogue Pin Assignment

Similarly, correctly identifying pins available as analogue inputs can be a problem. As an example, in the early Arduino days, only a small selection of pins (5) was available, clearly partitioned on the board. This limitation has mostly been removed in recent years and, today, most new microcontroller families offer many options.

Figure 1 shows how as many as 24 out of the 25 I/O pins of the PIC16F18855 microcontroller are available as analogue inputs (ANx row).

However, although true for ADC inputs, it is not necessarily so for op-amps' inputs and more delicate analogue features (V_{ref}, analogue comparators, etc.).

A/D And D/A

In the analogue world, handling analogue inputs and outputs should be as easy as handling digital quantities. Making ADC and DAC peripherals available is not sufficient, if capturing each single "sample" requires a complex state machine and precise timing of events handled in software.

Fortunately, both the resolution and automation of ADC modules have been greatly improved. Look for ADCC modules in most modern microcontrollers, where the second C stands for "computation". This is the ability of the peripheral to perform not only automatic, precisely-timed sampling of analogue inputs, but also to pre-process the data, automatically extracting averages, filtering and detecting thresholds.

Programmable Logic

Often, the time-critical path of an embedded application can be identified in a small section of the application logic. There is a small set of precious events (input signals, faults) that must be processed very quickly to avoid any consequences. The typical software developer will resort to demanding a faster processor, but that can be a trap. Faster processors come with higher power consumption and cost. A better solution is to use configurable logic cells (CLC), to turn those time-critical functions (code) into nanosecond-fast digital logic without breaking a sweat. You will find configurable logic cells in many low-cost 8- and 32-bit microcontrollers today.

Re-Arranging Internal Peripherals Connections

Similarly, at times, the software developer is confronted with a lack of the "perfect" peripheral. Software flexibility is often employed to "patch-up" things and make the best of what is available among the limited resources of an embedded processor. But, the same configurable logic (CLC) can be used to re-wire the internal peripheral set available to create a better hardware match to the problem at hand. This capability is found in the most recent microcontroller families featuring the so-called CIPs (Core Independent Peripherals) or the Event System.

Robustness

The smaller the geometry and the larger the number of gates available, the more delicate/susceptible the device appears to be. In the fastest processors, preferred by the software developers, internal power supply voltages drop to the sub-volt range and with that goes the ability to control directly high input/output voltages and currents.

But larger geometries have not been abandoned, though. Small microcontrollers are not only naturally more robust, but now also offer some seriously robust features. Look for CRC/SCAN, Windowed Watchdogs and Fail Safe Clock monitors, which simply take the pain out of securing the application to run the correct code and be properly reset if needed.

Speed Vs Low Power

It is interesting to note how the world of embedded applications differs in the interpretation of the term "low power". There is a difference of several orders of magnitude in power consumption between a microcontroller and a Raspberry Pi (nA vs mA), and the level of granularity in controlling power. Look for microcontrollers that include technologies such as Power

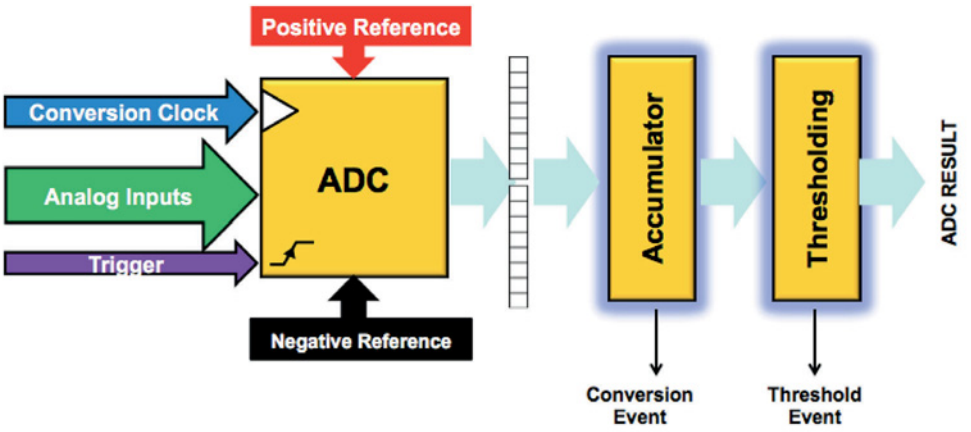


Figure 2: An ADCC adds 16-bit computation and thresholding

Module Disable (PMD), which disables individual hardware peripherals, and DOZE modes, where the processor can be made to run slower for intervals of time while its peripherals work at nominal speed, only to speed up again, automatically, when needed.

```
CPUDOZE = DOZE_1_16;
                        // set DOZE ratio to 1:16

CPUDOZEbits.DOI = ENABLE;
                        // interrupts at full speed

CPUDOZEbits.DOZEN = ENABLE;
                        // enable DOZE mode
```

Listing 2: Configuring a PIC16F15355 for DOZE mode

Assisted Configuration

All the suggestions discussed here would be wasted if the software developer needs to consult datasheets that run to the thousands of pages for each new device, and keep getting longer and more complex.

It is true here that software can, and successfully does, come to the rescue of software developers. Rapid development tools such as MPLAB Code Configurator and/or AVR START can turn the hours (or days) of research required to create the proper device configuration and that of all its peripherals into minutes of interactive exploration. In fact, all the code examples and figures presented in this column were not derived from the device datasheet but obtained from MPLAB Code Configurator GUI, a code that was generated automatically after a few clicks of a mouse. ●

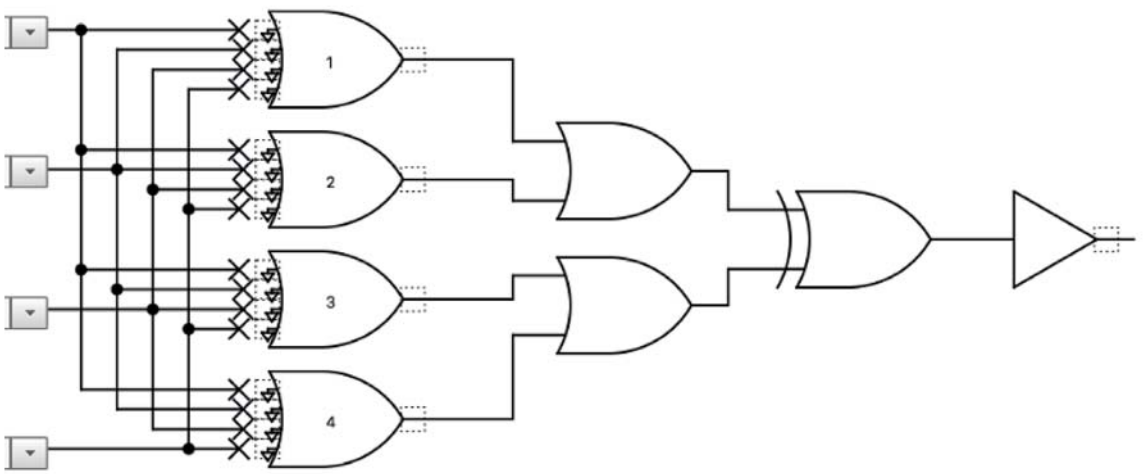


Figure 3: A configurable logic cell (CLC) can perform logic functions in nanoseconds

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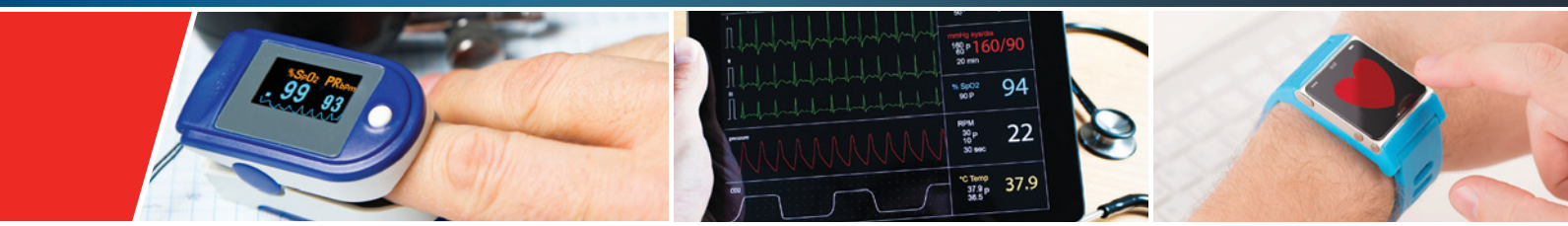

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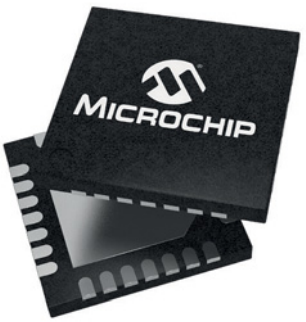

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Heart rate monitoring

BY **DR DOGAN IBRAHIM**, PROFESSOR AT THE NEAR EAST UNIVERSITY, CYPRUS

The use of technology in healthcare continues to grow, especially with each new generation of fast, low-power and low-cost processors. In cardiovascular applications, measurement of heart rate and pulse oximetry are two important parameters.

Heart rate varies significantly between individuals based on age, genetics, fitness levels, body temperature and various chemicals in the blood stream. For example, increased calcium, thyroid hormone or caffeine, or decreased sodium levels increase the heart rate. Each person has a maximum allowable heart rate, which is the highest from stress and exercise that doesn't cause problems. This rate decreases with age or illness.

Heart Rate Measurement

Heart rate is traditionally and simply measured by placing the thumb over the subject's arterial pulsation (usually at the wrist or radial artery), feeling the heartbeats and timing and counting the pulses for a given time. The heart rate is then obtained by multiplying this number by two, a simple method but not accurate, giving errors if the beats are weak or the rate very high.

More accurate methods use electronic techniques, including electro-cardiograms (ECG). Although accurate, ECG is rather expensive, and its use to measure just the heart rate is not economically justified.

UK hospitals and clinics use integrated medical devices with large displays to measure several parameters, including heart rate, saturated blood oxygen level, blood pressure and temperature. But, these are way too expensive for individual use.

Here, I describe the design of a low-cost, microcontroller-based heart-rate measuring device, which can be programmed to display various parameters, such as the average, maximum and minimum rates over a given period, and so on.

Measurement Details

Most heart rate measurement devices use optical sensors, placed on a finger or earlobe. As blood is pushed into the arteries, it propagates throughout the body to the capillaries of the finger, detected as a surge in blood volume. For example, if a light is shone through a finger, more of it will be absorbed when the blood's volume increases. Each change in this absorption can be counted as a pulse.

Two methods are commonly used: transmittance and reflectance. With transmittance (Figure 1), an infrared LED transmitter/light-detector pair is clipped on a finger or earlobe. The LED emits infrared light that's detected by the sensor on the other side, and the change of blood volume through the artery is measured. This signal, in the form of pulses, is then amplified, filtered and displayed as a count.

With the reflectance method, the light detector is on the same side as the LED transmitter (Figure 2) to detect light reflected

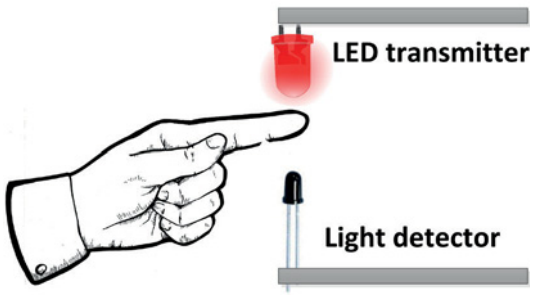


Figure 1: Transmittance method

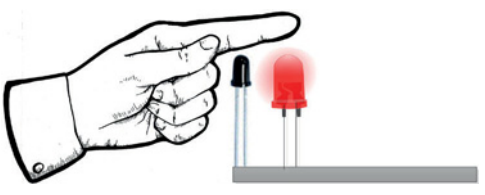


Figure 2: Reflectance method

Figure 3: Some commercially available heart-rate monitoring devices

by the tissue. This method works best if the artery is close to the skin's surface.

After counting the pulses in a certain period, the heart rate in beats per minute (bpm) is calculated as follows:

Heart rate = 60 x N / T

where N is the number of pulses counted in period T, and T is the period in seconds.

Commercially Available Devices

There are many commercially-available heart-rate measuring devices, most in the form of wristwatches or smartphone apps; see Figure 3 for some examples. Polar RS100 is a heart rate monitor and stopwatch. The device can be used as a personal trainer; it measures the average and maximum heart rates, as well as the heart rate as percentage of the maximum, and the number of calories expended during exercise.

The Huawei Fit Smart Fitness watch is a heart rate measuring and sleep monitoring device, as well as a personal trainer, step and calorie counter and smart alarm generator.

Ovente's BHS7000 is a heart-rate monitoring device with a stopwatch. It can be worn as a wristwatch or on the chest with a chest strap.

The Fitbit Charge 2 is a heart-rate monitoring device as well as a step and calorie counter, sleep monitor and an electronic reminder.

Facelake FL series of devices can measure blood oxygen saturation as well as heart rate. The device is clamped on a finger, and an LED display shows both the oxygen saturation level as a percentage and the heartbeats in bpm.

Heart-Rate Measuring Device Design

Figure 4 shows the block diagram of one version. A mikroBUS-compatible Heart Rate 3 Click board is used as sensor. This board contains a SFH7050 multichip package with three LEDs (infrared, red and green) and one photodiode, separated by a light barrier to prevent optical crosstalk.

The analogue readings from the SFH7050 are forwarded to the AFE4404 bio-sending IC. Current from the photodiode is converted into voltage by the transimpedance amplifier and digitised using an ADC; the ADC code can then be read out with an I2C interface.

The Hardware

The circuit diagram of the heart rate 3 Click board is shown in Figure 5. The interface is a standard I2C bus with additional signal for RDY. In this example the board is plugged into mikroBUS socket 1 of an Easy PIC V7 microcontroller development board. This board contains a 2x16-character text LCD in addition to many LEDs, pushbutton switches and a 4-digit, 7-segment display. The development board is shipped and a PIC18F45K22 microcontroller on board with an 8MHz external crystal for timing.

The Heart Rate 3 Click Board has the following mikroBUS connections of interest:

PIN NO	SIGNAL
2	RST
7	+3.3V
8	GND
9	GND
10	+5V
11	SCL (I2C)
12	SDA (I2C)
15	RDY

When connected, SCL and SDA signals are driven from the microcontroller I2C pins RC3 and RC4 respectively, and pins RST and RDY are driven from microcontroller pins RE1 and RB0 respectively. The LCD is connected to PORTB of the microcontroller. Figure 6 shows the circuit diagram of the system.

The Software

The software was developed using the mikroC Pro for PIC language compiler and IDE. The compiler provides a heart rate 3 library to configure the device and read heart-rate samples. This simplifies the programming tasks considerably.

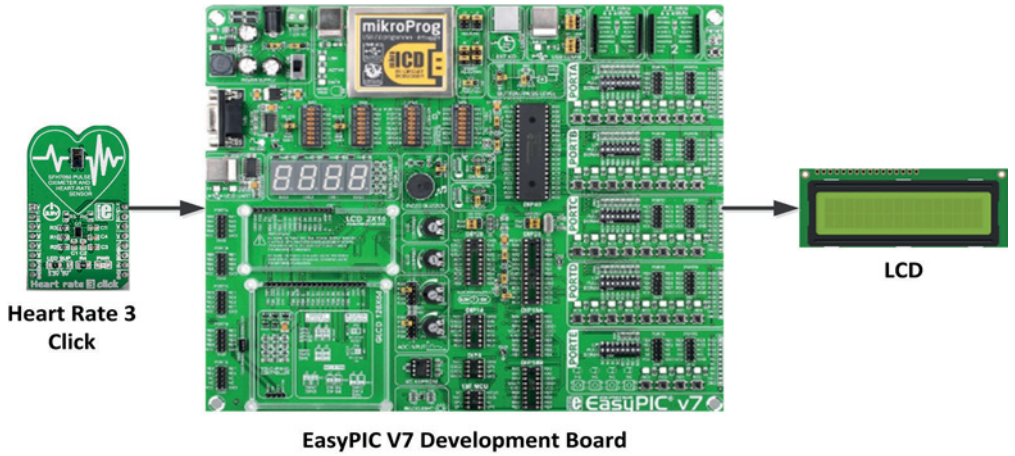


Figure 4: Block diagram of the example system

The complete program is shown in Listing 1. At the beginning of the program the interface between the LCD and the microcontroller PORTD is defined. Inside the main program, function Setup is called to configure PORTB, PORTC, PORTD and PORTE as digital I/O and, then, the heart rate sensor Click board is initialised by defining its dynamic parameters and calling to function hr3_init; the LCD is also initialised, and so is the I2C bus.

An external interrupt service routine is set up on the microcontroller pin RB0 that's activated when a sample is ready (when the Heart Rate 3 Click board pin RDY sends a short pulse).

The remainder of the program is executed in an endless loop. Inside this loop, the heart rate is read into an integer variable rate by calling the library function hr3_get_heartrate. This integer value is then converted into a string character array text using built-in function IntToStr, and displayed on the LCD. ●

```
#include "heartrate_3.h"
// LCD pinout settings
sbit LCD_RS at RD4_bit;
sbit LCD_EN at RD5_bit;
sbit LCD_D7 at RD3_bit;
sbit LCD_D6 at RD2_bit;
sbit LCD_D5 at RD1_bit;
sbit LCD_D4 at RD0_bit;
// LCD pin direction
sbit LCD_RS_Direction at TRISD4_bit;
sbit LCD_EN_Direction at TRISD5_bit;
sbit LCD_D7_Direction at TRISD3_bit;
sbit LCD_D6_Direction at TRISD2_bit;
sbit LCD_D5_Direction at TRISD1_bit;
sbit LCD_D4_Direction at TRISD0_bit;
// Heart rate sensor pins
```

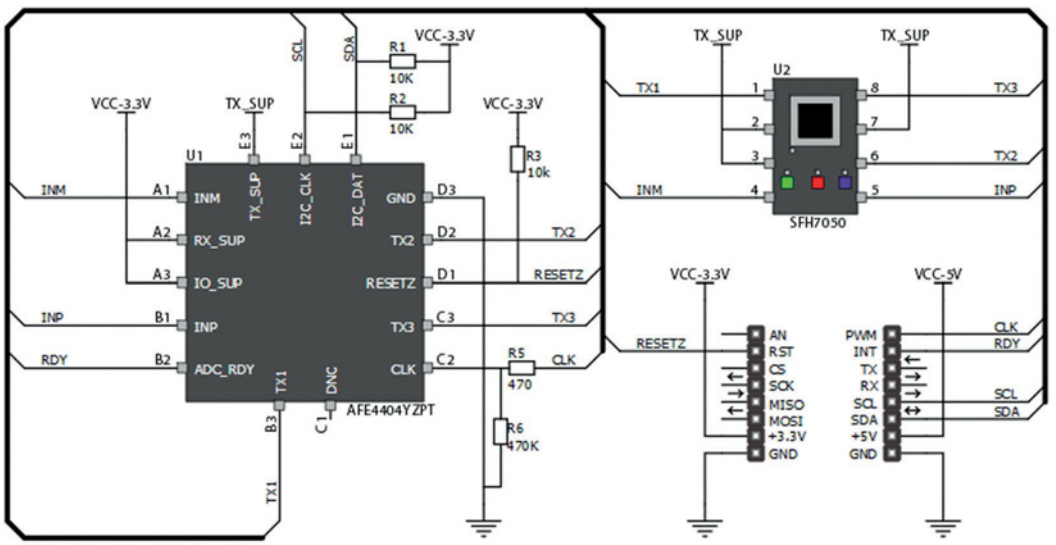


Figure 5: Circuit diagram of the heart rate 3 Click board

```
sbit RST at RE1_bit;
sbit RST_DIR at TRISE1_bit;

char Text[7];
char int_flag = 0;
char timer_count = 0;
uint16_t rate = 0;
//
// This function initializes the heart rate click
//
void Setup()
{
 dynamic_modes_t dynamic;
 uint8_t address = 0x58;
 LCD_Init();
 dynamic.transmit = trans_dis;
 dynamic.curr_range = led_double;
 dynamic.adc_power = adc_on;
 dynamic.clk_mode = osc_mode;
 dynamic.tia_power = tia_off;
 dynamic.rest_of_adc = rest_of_adc_off;
 dynamic.afe_rx_mode = afe_rx_normal;
 dynamic.afe_mode = afe_normal;

 LCD_Init();                    // Initialize LCD
 RST_DIR = 0;                   // Toggle RESET pin
 RST = 0;
 Delay_Ms(50);
 RST = 1;
 I2C1_Init(100000);             // Initialize I2C library
 Delay_Ms(150);
 hr3_init(address, &dynamic);   // initialize Heart
rate click
 initStatHRM();                 // Initializes values to 0
}

void Init_ExtInt()              // Setup external interrupt
{
 GIEL_bit = 1;
 INT0IF_bit = 0;
 INT0IE_bit = 1;
 GIE_bit = 1;
}

void interrupt()                // External interrupt service
routine
{
 INT0IF_bit = 0;


 int_flag = 1;
}
```

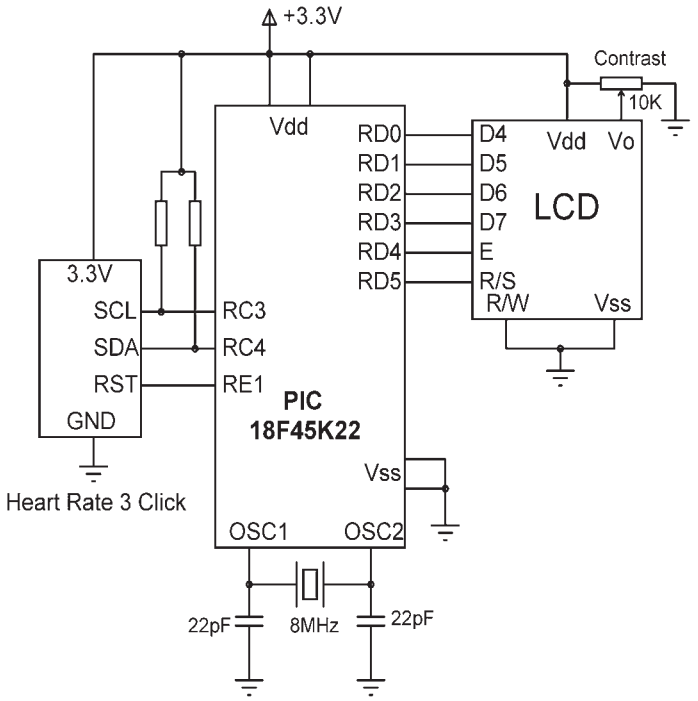
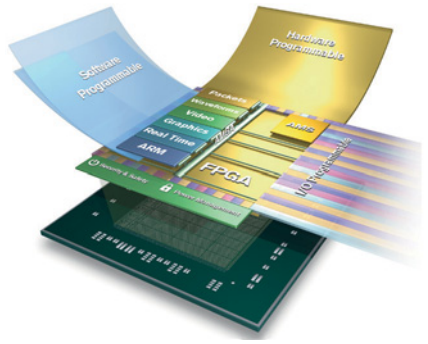


Figure 6: Circuit diagram of the system

```
void main()
{
 ANSELB = 0; // Set ports as digital
 ANSELC = 0;
 ANSELD = 0;
 ANSELE = 0;
 Setup();               // Initialize heart rate sensor
 Init_ExtInt();                 // Initialize external
interrupt

 while(1)
 {
 if(int_flag == 1)
 {
 statHRMAlgo( hr3_get_led1_amb1_val() );
 int_flag = 0;
 }
 rate = hr3_get_heartrate();                    // Get heart
rate
 IntToStr(rate, Text);                  // Convert to string
 LCD_Out(1,1, Text);                    // Display heart rate
 }
}
```

Listing 1: System program



Designing safety and security into an embedded vision system

BY **GILES PECKHAM** AND **ADAM TAYLOR** OF XILINX

So far, this series has examined techniques and devices for implementing the functions of an embedded vision (EV) system. This article will describe tools and techniques to ensure the system meets applicable safety and security requirements.

A suitable design methodology should include risk assessment to understand the likelihood of technical failure, accident or incorrect operation, and the possible consequences. Medical imaging equipment, industrial vision systems and automotive applications such as the Advanced Driver Assistance System (ADAS) typically require formalised assessment, referencing standards such as ISO 14971 for medical systems. In any case, teams should be able to demonstrate that safety has been given due consideration.

The results of risk assessment may call for functional safety measures, active systems designed to prevent dangerous failures. The IEC 61508 series are general international standards governing electrical/electronic and programmable functional-safety systems. Other application-specific safety standards include ISO 26262 for automotive applications, IEC 62061 for machinery, or DO178/DO254 for flight applications. Each defines several safety integrity or assurance levels according to the time to failure of the safety system; the longest time to failure represents the highest safety assurance.

Safety-related design decisions can be evaluated and documented by following an engineering lifecycle and agreed standards. The engineering life cycle (Figure 1) will be determined by the end application and the resultant certification required. Within this life cycle, the engineering review gates, which control the progress of the project, can be defined. During these reviews, independent technical experts will examine requirements, designs, technical reports and test results to allow the design to progress to the next stage, or demand further work to achieve the desired standard of evidence.

The engineering plan will also outline the verification and validation process at every level, to gain the body of evidence to achieve compliance with the applicable standard. This may

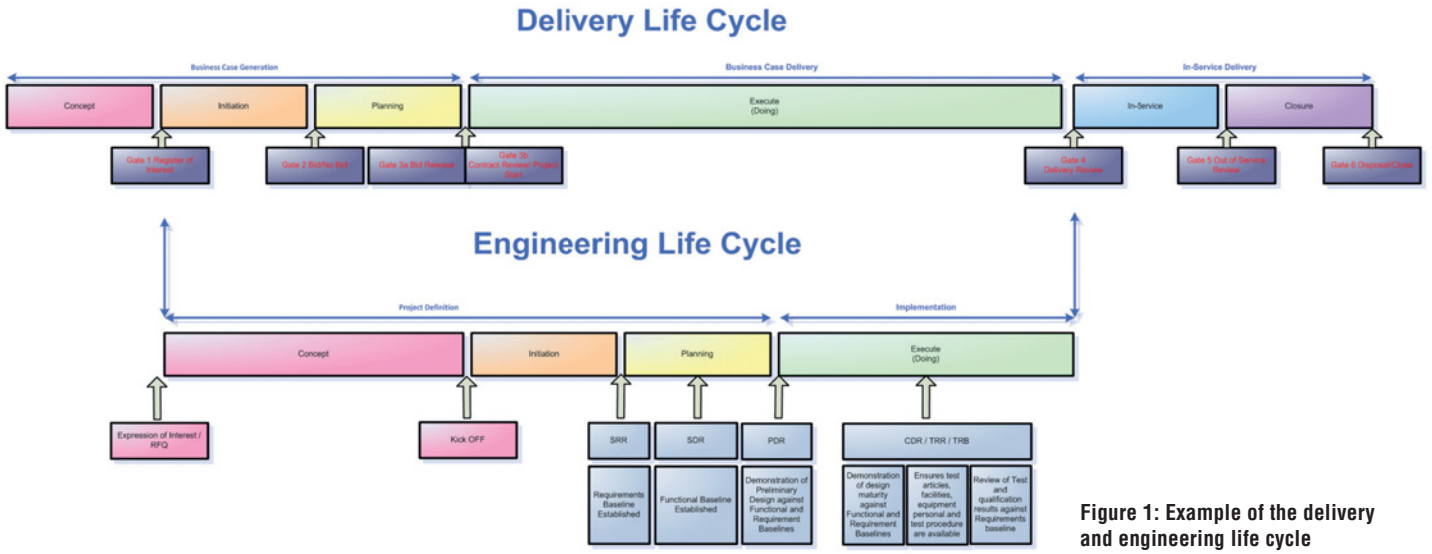


Figure 1: Example of the delivery and engineering life cycle

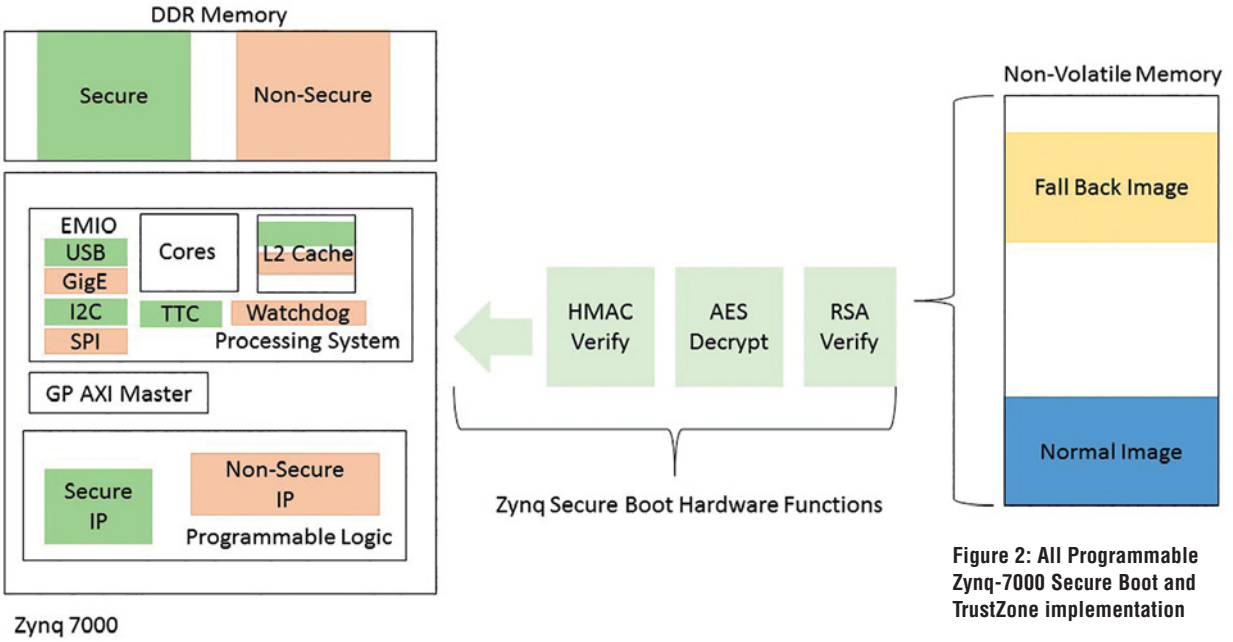


Figure 2: All Programmable Zynq-7000 Secure Boot and TrustZone implementation

require testing of the EV system across environmental operating ranges, dynamic vibration and shock. Accelerated life testing may also be necessary, to ensure the specified operating life of the system can be achieved.

Security-Conscious Design

As far as security is concerned, the high-level issues engineers deal with include the following:

- Competitors reverse-engineering the design;
- Unauthorised modification of the design;
- Unauthorised access to data within the design;
- Unauthorised control or manipulation of the end application;

There are several ways to address these challenges. Access to the design and manufacturing files can be controlled. Encrypting bit streams can prevent spoofing attacks or theft of data by eavesdropping. The physical design can be protected by limiting access to JTAG ports in the final product, and by implementing software security measures depending on the architecture of the device chosen.

The heart of any EV system is the image-processing pipeline, which combines high-bandwidth processing with supervisory and control capability. By enabling a more tightly-integrated architecture than is achieved using a processor and logic implemented in a separate FPGA, the All Programmable Zynq-7000 not only allows for a better SWaP-C solution (discussed in part 2 of this series), but also provides for a more secure system because data passing between the processor and logic fabric is not presented at external pins where it can be intercepted or monitored.

Moreover, the Zynq device provides an embedded security architecture that can be used to support secure configuration. A three-stage process can be used within the Processor System (PS) and the Programmable Logic (PL) to secure the system partitions. This comprises a Hashed Message Authentication Code (HMAC), Advanced Encryption Standard (AES) decryption and RSA Authentication. Both the AES and HMAC use 256-bit private keys while the RSA uses 2048-bit keys. The security architecture of the Zynq device also allows for JTAG access to be enabled or disabled.

These security features are enabled when generating the boot file and the configuration partitions for the non-volatile boot media. It is also possible to define a fall-back partition. In this case, should the initial first-stage boot loader fail to load its application, it will fall back to another copy of the application stored at a different memory location.

Creating A Trusted Environment

Once the device is successfully up and running, ARM TrustZone hardware-based security supported in the Zynq device can be used to divide the system into secure and non-secure worlds. TrustZone technology implements secure and non-secure virtual cores on the Cortex-A9 processor, and encompasses memory, L2 cache, software, bus transactions, interrupts and peripherals. Hardware logic partitions the secure and non-secure worlds, and a software-based secure monitor manages switching between the two. This creates a Trusted Execution Environment (TEE) comprising TrustZone-based hardware isolation, trusted boot and a trusted OS. Applications that need to be trusted can be run in the TEE.

When it comes to implementing the image-processing pipeline within the All Programmable Zynq-7000 programmable logic fabric, TrustZone can also be used to provide secure or non-secure access to IP cores embedded in the fabric. These may be either custom-developed modules or from the IP library. Securing access to critical aspects of the image-processing chain helps prevent unauthorised changes to the configuration.

Isolation Design Flow

Some safety and security implementations, such as IEC61508, may require certain elements of the system to be isolated from each other. This may be needed to achieve modular redundancy or to support different safety areas and test functions. Xilinx's Isolation Design Flow (IDF) helps designers enforce physical separation between the identified zones (Figure 3). This is supported for the Zynq device when used with Vivado Design Suite.

The IDF is similar to the conventional Zynq design flow, and enables users to implement a secure or safety-critical solution using familiar design techniques and coding styles. Engineers should, however, consider floor planning earlier in the design project to ensure proper isolation of elements such as logic, routing and I/O buffers. One important difference in the development flow is that partitions are used to isolate functions, which can simplify modification of isolated partitions when design changes are needed.

To implement the design, several device and tool-specific implementations are available. The end application and overall engineering management plan will help determine which of these techniques should be used:

- Use of Error Detecting and Correcting (EDAC) codes on memories. If necessary, this can be combined with a scrubbing function which periodically reads and corrects the data in memory.
- Exploiting the Hamming difference when defining control words. Increasing the Hamming distance between command words while requiring more bits to implement can help with the reliability of the design.
- For critical commands use the "arm and fire" approach which requires two separate commands to action critical functions.
- Use of EDAC codes on external communication interfaces.
- Built-In Test (BIT) capability. The Zynq XADC can support BIT by monitoring the device voltages and temperatures, as well as by capturing external signals.

Essential Management Plan

Identifying the applicable safety standards and establishing a suitable engineering management plan are essential to ensure the product achieves the required certifications. Important components, tools and development methodologies are available to designers of all programmable SoC devices, to help achieve the required standards for functional safety and security. ●

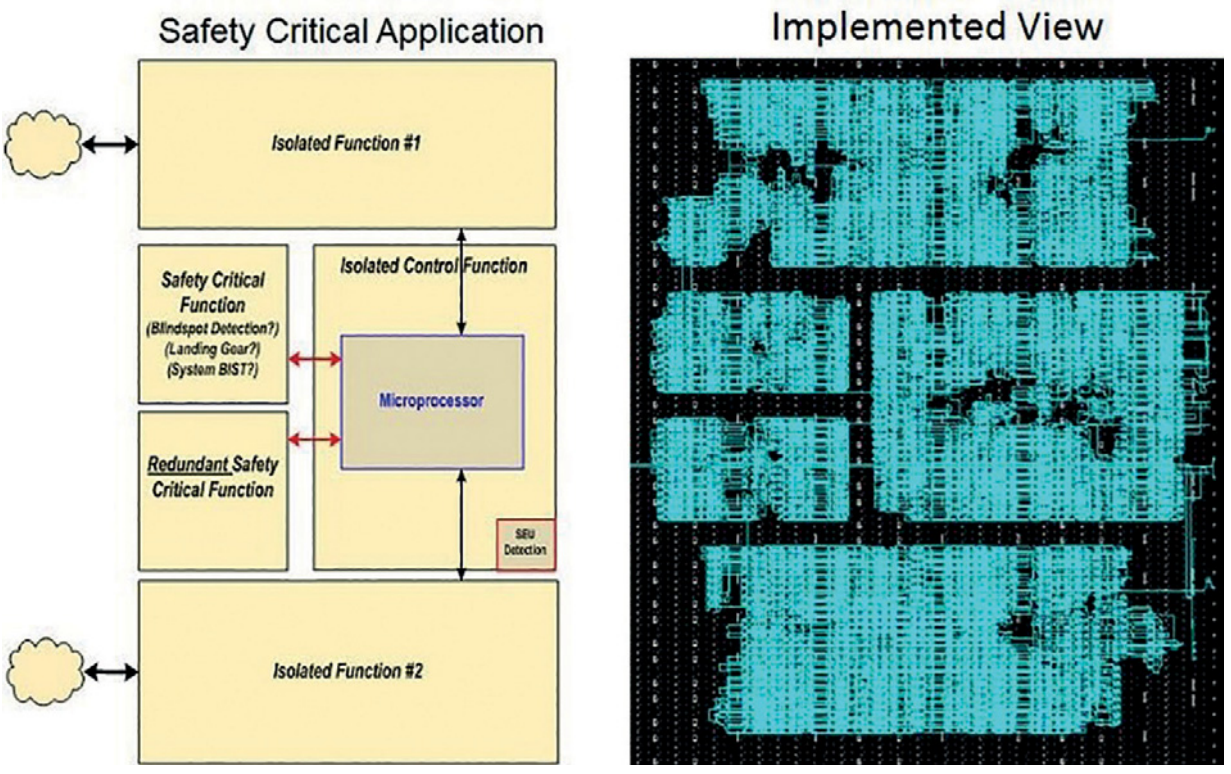


Figure 3: IDF enforced policy for a safety-critical FPGA

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E-PAPER AND RFID/NFC – A PERFECT PARTNERSHIP TO REVOLUTIONSE MEDICAL LOGISTICS

BY **SCOTT SOONG**, CEO OF PERVASIVE DISPLAYS

Radio frequency identification (RFID) and near-field communications (NFC) have revolutionised the logistics field. Wireless tags using these technologies can track individual items of stock and reduce fulfilment errors.

But, there are some logistics applications where these tags haven't been as widely adopted as in other markets; in these cases, paper labels and barcodes remain the preferred tracking media.

One major sticking point for wireless tag adoption has been the demand for scannable barcodes in some applications, alongside detailed information that can easily be read and edited. With an RFID/NFC tag, additional equipment is necessary to read the data. There have been attempts to engineer wireless tags with such capabilities, but the main roadblock has been excessive power consumption. This is likely to change however, since increased demand for human-readable and human-writable wireless tags is such that efforts are on-going to overcome the power problem.

Vaccine Storage Information

Changes to legislation around vaccines in the US are a perfect example of where a tag with a display would be useful. The new legislation requires direct visual access to detailed storage temperature information for vaccines, every 24 hours, in order to track changes in refrigeration that could damage the efficacy of the vaccine.

It doesn't take much imagination to come up with a solution: a wireless tag with a built-in display. This would enable people to instantly view the relevant information, as well as send data to and receive data from the tag using RFID/NFC. So far, however, this has proved almost impossible. If designers are to change that, they need to change a key part of their strategy.

Power Consumption

Traditional TFT LCDs are inherently power-hungry for two main reasons. First, they require a backlight to make the image on the screen visible, and, second, they need

constant refreshing, usually fifty or sixty times per second. Both operations vastly increase the power the display requires, making TFT LCDs unsuitable for power-limited applications.

An answer may be e-paper displays (EPDs), a technology growing in popularity, widely seen in e-book readers. EPDs don't require backlighting, and they need refreshing only when the displayed data changes. While the displayed information remains the same, there's no need to refresh and, hence, no power use. This allows an EPD to run for several years on a single coin-cell battery, compared to a TFT display which would use hundreds of similar batteries in the same time.

> Increasing demand for human-readable and human-writable wireless tags is such that efforts are on-going to overcome the power problem

In fact, for many applications, EPD uses so little energy that solutions built around the technology can often be implemented using energy harvested from the environment. This extremely low power usage means designers can include displays in applications where TFT technology would otherwise rule them out.

An EPD implementation for the vaccine example would enable a worker to check the status of the drug without using specialised equipment, since data can be read from a wireless tag without a display.

EPD Technology Workings

EPD technology uses two arrays of electrodes to operate. The top array is transparent. The 'pixels' in the display are micro-capsules between the two electrode arrays. To maximise the display's resolution, the micro-capsules can be as small as 0.2mm in diameter.

Each micro-capsule contains spherical pigment particles that are electrically charged, the white positively charged and the black negatively charged.

If the transparent electrode on the top layer of the display goes negative, it will attract the positively-charged white particles to the top and that part of the display will show white. Conversely, if the top electrode is positive, then the negatively-charged black particles will rise into view. By manipulating voltages across the array, text and images can be displayed, including various shades of grey.

Moreover, because ambient light reflects off physical pigment particles, the contents of an EPD remain readable in bright sunlight, unlike a TFT display.

Because of the way they are built, and especially since they don't need backlight, EPDs are thinner and lighter. It is also possible to manufacture flexible EPDs.

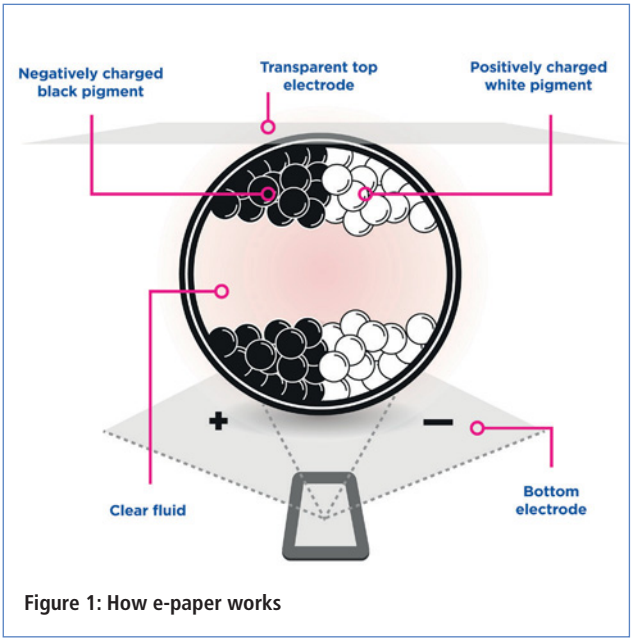

Figure 1: How e-paper works

EPDs In Healthcare

Aside from the vaccine example, there are many other healthcare applications where EPDs can be valuable, especially when used with wireless technology. For example, combining an EPD with a wireless location-tracking module would enable hospital staff to identify and locate a patient, know where the patient should be taken and what treatment has been prescribed.

The same combination of technologies can also be used to track other items that move around the hospital, such as transplant organs. By knowing where a patient, organ or other item is, medical staff can ensure they're ready when things arrive. The EPD can then be used to positively confirm the patient's identity, as well as any specific instructions.

Healthcare facilities also typically own expensive lab and test equipment. A good asset-management system, based around EPDs and wireless tags, would help ensure equipment is where should be, and enable users to check its calibration and maintenance status. To safeguard equipment records, you could restrict some personnel the ability to update information on the EPD.

Of course, there is an installation cost to consider when implementing an asset-management system, like the one outlined here. However, since the system is designed to prevent scenarios like incorrect patient identification, incidents can have a heavy financial impact on hospitals in legal fees, payouts to claimants, and so on. Therefore, the benefits of better tracking and managing patients, equipment and medication will quickly outweigh the initial investment. ●

ECG CIRCUIT REDESIGN BASED ON CCII+ STRUCTURES

BY **ŞÜKRÜ KITIŞ** FROM SAKARYA UNIVERSITY, AND **RÜŞTÜ GÜNTÜRKÜN** AND **HASBI APAYDIN** FROM DUMLUPINAR UNIVERSITY IN TURKEY

Electrocardiogram (ECG) measurements are typically used to detect heart and brain disorders. Since the heart and the brain emit electric signals, these can be picked up by an ECG; however, their low strength requires amplification to at least millivolt levels and filtering to remove noise.

At The Heart

The heart consists of four chambers, operating in a double circulatory system, where the right ventricle pumps blood into the pulmonary circulation of the lungs, and the left ventricle pumps blood into the systemic circulation through the aorta to the rest of the body. The signals the ECG system picks up are complex waves, representing to the trained eye each stage of the heart's operation.

Each cardiac cycle forms three important ECG waveforms – the so-called P, QRS and T. The P wave represents relaxation of the atrium; typically, atrial disorders show in this wave.

The QRS wave represents relaxation of the heart's ventricle, so, ventricular disorders show here; this is also the waveform that confirms a heart attack.

The T wave represents contraction of the ventricle. It's typically used to identify hypopotassemia (lack of potassium in the blood) and hypocalcemia (lack of calcium in the blood).

ECG Systems

There are many ECG systems on the market, but here we introduce a design very small in size (5cm x 5cm), low in price (the $200-250 range), yet with a significantly large measurement bandwith.

ECG measurement systems typically use op-amps; however, we found that current conveyors (CCII) show greater linearity, input voltage range and frequency performance and are, therefore, very suited to this application. In fact, designs with CCII+ structure (the positive type) are already widespread in amplifier, integrator, filter and differentiation circuits.

A CCII+ has two inputs (x, y) and an output. It can be designed with a BC237 – an NPN epitaxial silicon transistor for switching, and an amplifier (Figure 2), such as the AD844 high-speed monolithic op-amp.

In our study, the ECG circuit includes low-pass, high-pass and inverting amplifier sections, and then it is realised with a CCII+ structure (Figure 1).

Here, V1, V2 and V3 are inputs and V_{out} is the output. The system can be used as low-pass filter when V1 is zero, high-pass filter when V2 is zero, or band-pass filter when V3 is zero (see Table 1). Table 2 shows the characteristics of the ECG circuits with and without CCII+ structures in this study, as well as findings of previous studies and their

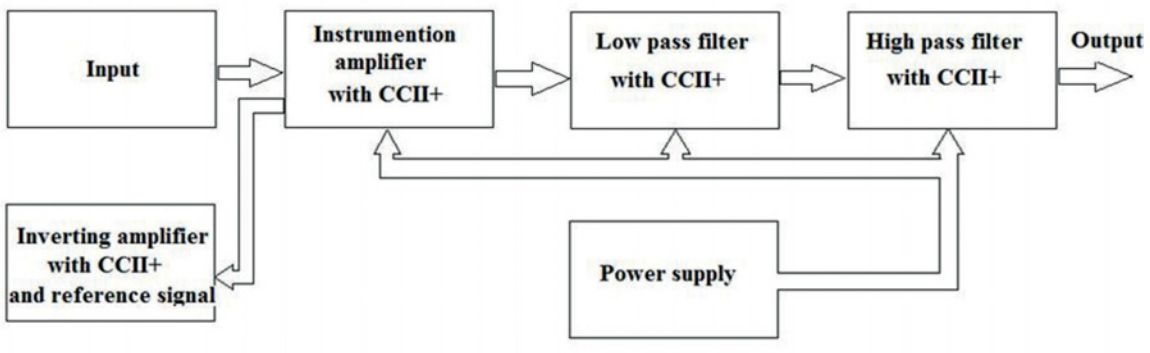

Figure 1: Redesign of an ECG circuit with CCII+ structures

	V_1	V_2	V_3	Feature	V_o/V_{in}
LPF	0	V_i	V_i	$R_1=R_2=R$	$\frac{V_o}{V_{in}}=\frac{1}{R^2C_1C_2s^2+RC_1s+1}$
HPF	V_i	0	V_i	$C_1=C_2=C$	$\frac{V_o}{V_{in}}=\frac{R_1R_2C^2s^2}{R_1R_2C^2s^2+R_2Cs+1}$
BPF	V_i	V_i	0	$C_1=C_2=C$ $R_1=R_2=R$	$\frac{V_o}{V_{in}}=\frac{-RCs}{R^2C^2s^2+RCs+1}$

Table 1: CCII+ filter options

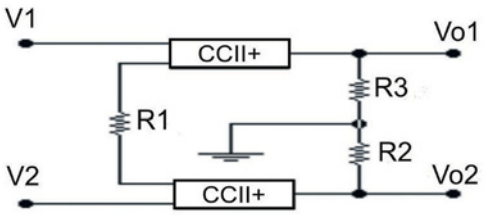

Figure 2: Instrumentation amplifier circuit realised with a CCII+ circuit

	1 (1998)	2 (2003)	3 (2008)	4 (2013)	ECG without CCII+	ECG with CCII+
Type	CBIA	OTA	CBIA	DDA	UAF42/AD624	AD844
CMRR(dB)	99	86	120	102	60	92
μV_{rms}	(0,3-150) Hz	(0,5-50) kHz	(0,5-100) Hz	(0,3-100) Hz	(0,3-50) kHz	(0,3-50) kHz
Imped.(ohm)	None	None	>1M	>1M	1 to 200M	1 to 200M
Power source (V)	9	± 2,5	3	1,8	± 5	± 5
Input noise interval (μV)	1,4	2,2	0,59	0,36	0,2	0,65

Table 2: ECG circuits comparison

characteristics. As shown in Table 2, CCII+ based ECG circuits have an advantage over other circuits, in terms of CMRR ratio, frequency range, gain and ease of implementation. While there is more interference in non-CCII+ based ECG measurements, such noise is reduced to a minimum in CCII+ based circuits, and ECG measurements can be made more accurately. In addition, this circuit can work from a single 5V DC supply. ●

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3D ELECTRONIC BRAIN ATLAS MODEL FOR THE DETECTION OF NEUROLOGICAL DISORDERS

OLD AGE BRINGS NEUROLOGICAL DISEASES SUCH AS ALZEHEIMER'S AND PARKINSON'S. NEW TOOLS ARE BADLY NEEDED FOR THEIR EARLY DETECTION AND TREATMENT. **MUHAMMET ÜSAME ÖZIÇ** AND **SERAL ÖZŞEN** FROM SELCUK UNIVERSITY IN KONYA, TURKEY, PRESENT A NEW ANALYTICAL MODEL

The human brain consists of many functional centres, some of which degenerate due to neurological disorders. High-resolution 3D structural magnetic resonance (MRI) images are used to monitor the degeneration, with the images usually measured manually by radiologists.

Manual methods can give relatively accurate measurements of anomalies such as tumours and lesions that can be separated from the background in the MRI images, but other neurological diseases such as Alzheimer's, Parkinson's or frontotemporal dementia, for example, are very difficult to distinguish.

To overcome this deficiency, 3D electronic brain atlases are used, developed to international standards and proven reliable. Pre-processed images from the atlas and the MRI are superimposed to find corresponding regions and thus assess the state of the brain.

There are several studies in the literature showing how to use the electronic brain atlas, so in this article we present a study of volume differences in brain lobes between Alzheimer's and normal MRI images, calculated using a 3D electronic brain atlas. For the purpose, we've developed a technique called "atlas-based volume measurement".

Magnetic Resonance Imaging

MRI is a medical imaging technique that shows soft tissues inside the human body in high resolution. It is a relatively inexpensive technique compared to other imaging techniques often used to monitor diseases.

With MRI scanning, the patient lies in a machine with a high magnetic field; see Figure 1. Radio frequency (RF) waves are sent to the area to be imaged. Hydrogen atoms in water and fat of the body absorb these waves, and as the RF wave is interrupted, energy absorbed by the hydrogen atoms is released. The returning signals are picked up by the scanner, digitised by an analogue-to-digital converter (ADC) and stored in a graphical matrix called k-domain. The MRI image is then obtained by performing a two-dimensional Fourier transformation.

Figure 1: MRI scanner

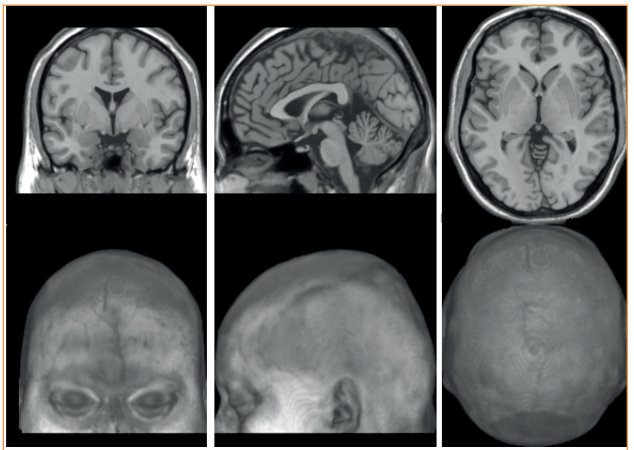


Figure 2: (a) A single slice from the coronal axis and a 3D model of all coronal slices; (b) A single slice from the sagittal axis and a 3D model of all sagittal slices; (c) A single slice from the axial axis and a 3D model of all axial slices – all created by the MRIcro program

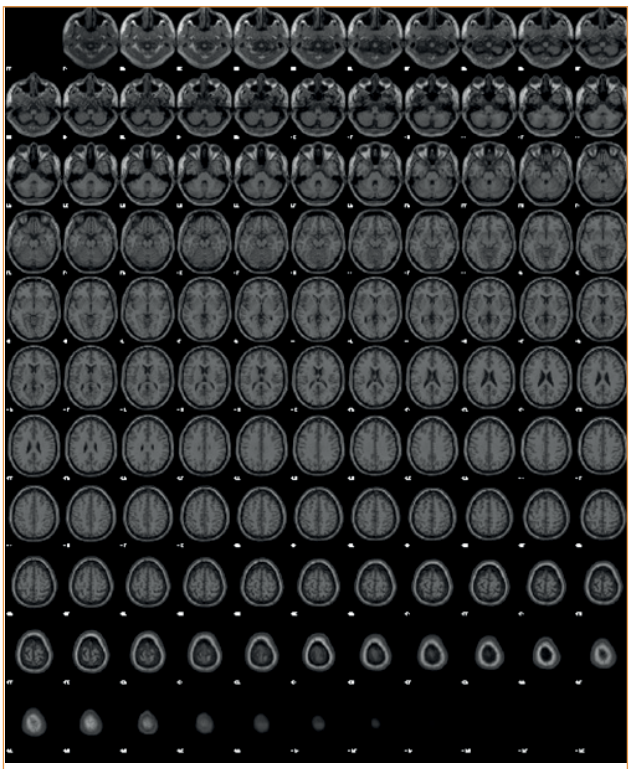


Figure 3: Each image is 121 x 145 pixels large, with a total of 121 axial slices. The smallest unit in 3D is 1.5 x 1.5 x 1.5 voxels, or the smallest part of a cube

Three-dimensional MRI images consist of 'slices', taken along three axes – axial, coronal and sagittal. Images taken from one side of the head are on the sagittal axis; those taken from the top of the head are on the axial axis; and images taken from the front of the face to the back of the head are on the coronal axis. Figure 2a shows a single slice from the coronal axis and a 3D model of all the coronal slices; (b) a single slice from the sagittal axis and a 3D model of all sagittal slices; and (c) a single slice from the axial axis and a 3D model of all axial slices.

Each slice has a thickness and image matrix size; the smallest unit in the 3D MRI space is the voxel, so there are two basic definitions for each 3D MRI image, namely a matrix size and a voxel size; see Figure 3.

Alzheimer's Disease

Alzheimer's is a neurological condition associated with old age, and is not reversible. There is no known cause and treatment for the disease. However, if diagnosed at an early stage, there are some treatments that lessen its effects.

Alzheimer's starts with simple forgetfulness, which intensifies over time. Over 65 is a risk factor for the disease, and as the world population ages, the costs of medicine and care bring economic burdens to all countries.

The disease first begins in the memory regions of the brain and spreads elsewhere as it progresses. This typically shows as loss of volume in the memory parts of the brain such as the hippocampus, amygdala and limbic system regions. At the same time, proteins called neurofibrillary tangles and senile plaque spread to all parts of the brain, causing tissue deterioration. MRI images clearly show the regions Alzheimer's affects in the brain and the progression of the disease.

For our study we used the Open Access Series of Imaging Studies (OASIS), a 3D MRI database developed by the Washington University Alzheimer' s Disease Research Center (http://www.oasis-brains.org); see Table 1.

Brain Regions

The brain has three parts: grey matter (GM), white matter (WM) and cerebrospinal fluid (CSF). The GM is a region of functional centres, WM provides communication between the grey matter and body functions, CSF is a liquid that surrounds GM and WM and protects the brain.

The main functional centres are located in the GM, which is further divided into six regions: frontal lobe, parietal lobe, limbic lobe, occipital lobe, temporal lobe and cerebellum. The basic tasks of these regions are as follows:

- **Frontal lobe:** Moral judgment, planning, analytical thinking;
- **Parietal lobe:** Right and left discrimination, reading, writing and arithmetic skills;
- **Occipital lobe:** Visual stimuli and interpretation of information;
- **Temporal lobe:** The perception of sound and smell, the processing of complex stimuli such as faces and space, speech, memory and hearing (distinguishing voices);
- **Limbic lobe:** Long-term memory formation, emotion, learning and memory skills, memory formation and storage, motivation, pain and pleasure;
- **Cerebellum:** Balance, coordination of muscles.

Figure 4 (left) shows these basic regions. The limbic system is inside the brain. It is itself subdivided into thalamus, cingulate gyrus, fornix, amygdala, hippocampus and parahippocampal gyrus. Figure 4 (right) shows the limbic system and subcortical regions.

In Alzheimer's, volumetric losses start in the grey matter in which the functional centres are located. Here, volumetric losses occur in the temporal lobe and limbic lobe regions, especially the memory and language regions. The boundaries of these lobe regions are not clearly visible in MRI images.

Volume measurements vary from person to person and from experience to experience, which frequently leads to misinterpretation of results and delay in treatment.

Analysis Programs

There are several brain analysis programs that automatically analyse 3D MRI images, such as the Linux-based Freesurfer (https://surfer.nmr.mgh.harvard.edu/) and FSL (https://fsl.fmrib.ox.ac.uk/fsl/fslwiki) and MATLAB-based (PM8(http://www.fil.ion.ucl.ac.uk/spm/software/spm8/). Freesurfer and FSL can perform automatic volume analyses of some subcortical regions. However,

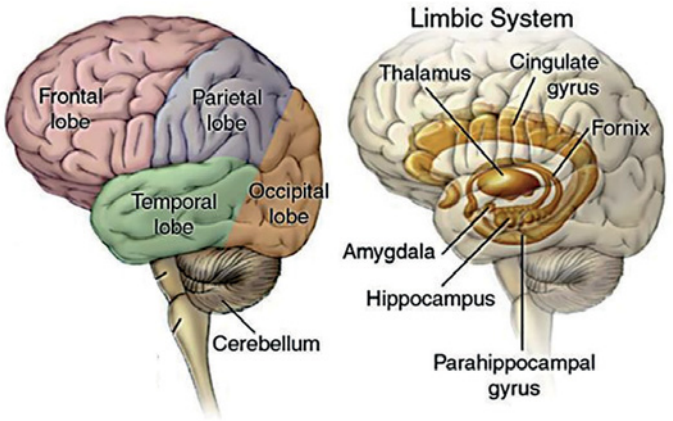


Figure 4: Brain lobes (left) and limbic lobes (right) with subcortical regions

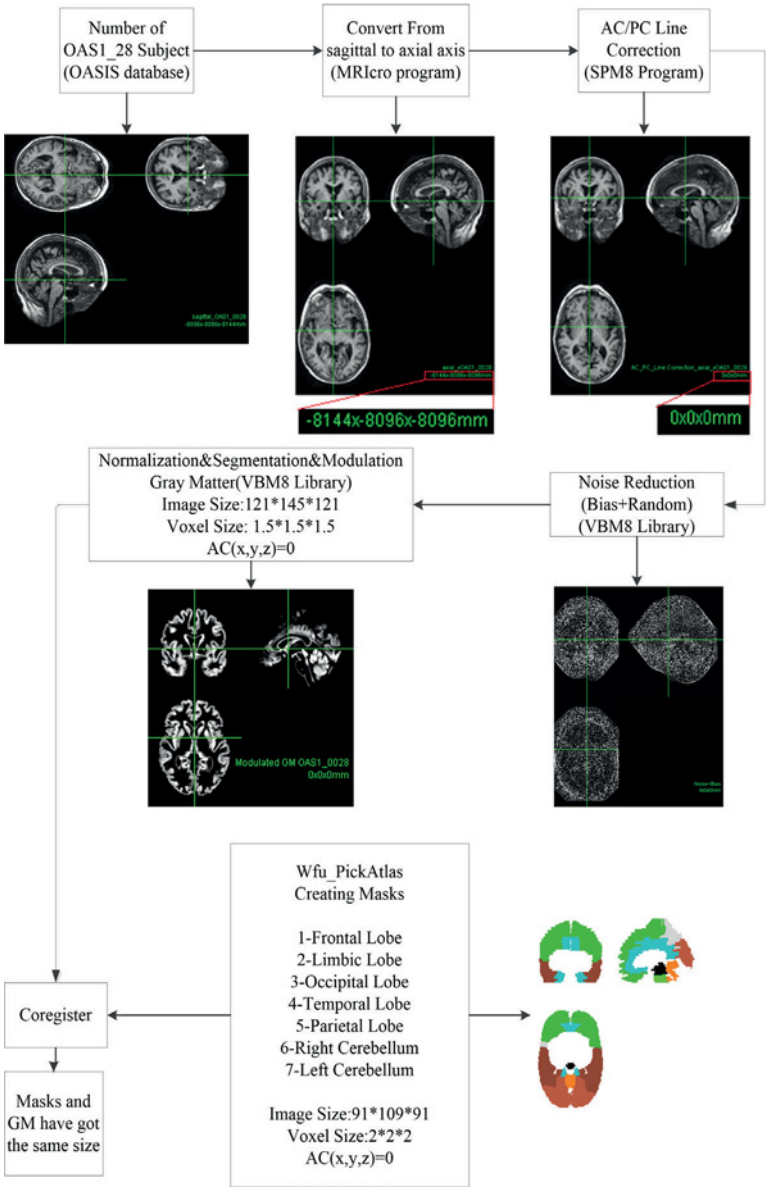


Figure 5: Pre-processing techniques shown as a flow diagram

analysis time can be long; for example, 3D MRI image analysis with the Freesurfer program can take 30 hours. Whereas the FSL program does volume analysis of only 15 subcortical regions it takes longer for analysis. Since these two programs have some disadvantages we set out to develop an atlas-based volume measurement model, based on a MATLAB SPM8 program.

SPM8 can automatically segment the GM, WM and CSF regions by using a coordinate system on the 3D MRI images. It can perform MRI image analysis as well as fMRI and EEG analysis. Using this program's libraries, researchers can create new tools.

One popular tool developed for MRI analysis is the VBM8 library (http://dbm.neuro.uni-jena.de/vbm8/), which performs noise reduction, normalisation and segmentation operations simultaneously. For our study we used this library, customised for structural brain MRI analysis.

In 1988, Talairach and Tourneux devised the so-called Talairach coordinate system and the Talairach space, although some find it not truly representative of the entire population. This atlas, as well as others, such as the AAL and Broadmann digital electronic brain atlases, can be obtained as binary masks from the MATLAB-based WFU Pick Atlas (http://fmri.wfubmc.edu/software/pickatlas) program developed by Wake Forest University. We used Talairach atlas masks for our study.

However, during our study we found some inconsistencies between raw MRI images and Alzheimer's lobes binary masks, raising the following questions:

1) How to best correspond 3D electronic brain masks and raw 3D MRI images? Both raw images and masks have different voxel sizes and image dimensions. How can these differences be reconciled?
2) Everyone's head size is different, meaning the size of the raw MRI images will differ too. How can these differences be smoothed out?
3) Which image pre-processing methods can be used on the raw MRI images?
4) How will the volume calculations be performed?

We used the SPM8, VBM8 and MRIcro programs on these problems. The pre-processing steps are as follows:

- **Conversion from sagittal to axial axis:** A process required for the SPM8 program, perfomed with the MRIcro program.
- **AC/PC line correction:** A necessary pre-processing of images in the VBM8 library. The raw 3D MR images were shifted in the 3D space with the SPM8 re-orientation tool to make the AC point x, y, z = 0 (the assumed centre of the brain). In this sequence, images will not lose any content, since they are only moved and/or rotated.
- **Noise reduction:** Removal of noise from the MRI machine and environmental factors during MRI imaging.
- **Normalisation and segmentation:** All 3D MRI images are placed in MNI space (the Montreal Neurological Institution's general population coordinate system). For

NC

Age Gr.	Numb.	M\F	Mean Age	Mean MMSE	CDR
60s	9	3\6	68.00±1.11	28.77±1.64	0
70s	32	8\24	73.37±2.44	29.15±0.91	0
80s	22	6\16	83.40±3.27	28.77±1.26	0
90s	7	1\6	91.14±1.67	28.57±1.71	0
Total	70	18\52	77.61±7.48	28.92± 1.21	0

AD

Age Gr.	Numb.	M\F	Mean Age	Mean MMSE	CDR
60s	7	3\4	67.85± 1.21	23.42± 4.85	5\2\0
70s	35	14\21	74.42±2.61	24.54±4.21	23\11\1
80s	23	11\12	82.69± 2.61	24.47 ±4.06	16\6\1
90s	5	2\3	92.00± 2.44	23.80±1.92	4\1\0
Total	70	30\40	77.74 ±6.66	24.35 ±4.05	48\20\2

*MMSE: Mini Mental State Examination (Another neuropsychological test)

Table 1: Data set used in this study

this operation, the raw MRI images are superimposed on a previously-generated reference image. Thus, differences between the raw MRI images are eliminated by normalisation. All images are analysed in a single space. GM, WM, CSF are segmented by this process. Images were segmented in the MNI space, and the GM region was taken.

- **Modulation:** After the segmentation process, two different normalised images are obtained:
  - An unmodulated normalised image, preserving tissue information prior to normalisation;
  - And, a modulated normalised image, preserving volume information prior to normalisation.

In this study, modulated normalised GM imaging was used for volume analysis.

- **Coregister:** This is a pre-processing stage to resolve size inconsistencies between GM and the atlas. The GM as a reference image and atlas masks as source image were used to perform this step. Atlas masks were re-sliced to bring them to the same dimensions as GM.

Figure 5 shows the flow diagram of the pre-processing methods in a 3D MRI image. These operations were done for each MRI image. After resolving the size inconsistency between the mask and GM, the overlapped images are shown in Figure 6.

Following this stage, the images are run through a MATLAB script named "get_totals.m", code developed by Ged Ridgway. Modulated images and overlapping masks make it possible to determine the volume of the underlying regions.

The operations for 70 AD and 70 NC images were handled one at a time, allowing to calculate the volumes for the six basic lobes; the volumetric mean value and standard deviation values within the group were calculated. As shown in Table 2, there is a statistically significant difference in the limbic lobe and temporal lobe in which Alzheimer's basic volumetric losses begin. These regions are primarily responsible for memory and language abilities. The resultant volume differences are consistent with volume losses found in the literature.

With this atlas-based volume measurement model, not only Alzheimer's, but also other neuro-degenerative diseases can be analysed. In cross-sectional and longitudinal MRI imaging, volume analysis is important for the early detection of disease and the early application of treatments. Similar studies can be done with AAL and Talairach atlases for subcortical regions to make more precise volume measurements. So, practical manual measurement difficulties can be overcome with these techniques. ●

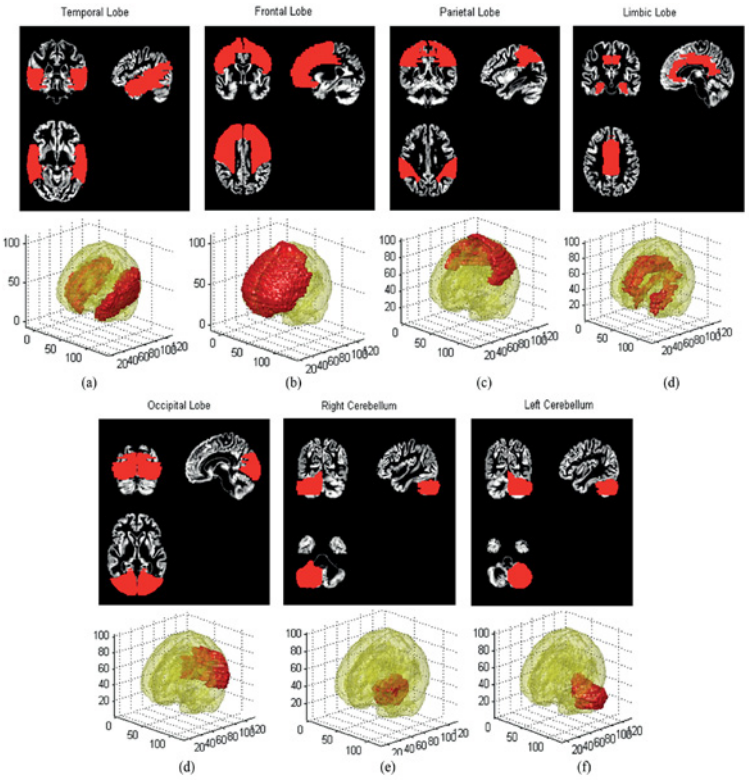


Figure 6: Overlapping normalised modulated GM and coregistered masks; (a) Temporal lobe and its 3D model; (b) Frontal lobe and its 3D model; (c) Parietal lobe and its 3D model; (d) Limbic lobe and its 3D model; (e) Occipital lobe and its 3D model; (f) Right cerebellum and its 3D model; (g) Left cerebellum and its 3D model

	AD		NC		Stats
	Mean	Std	Mean	Std	p
Frontal Lobe	147.73	15.96	149.5	13.56	0.47
Limbic Lobe	52.924	6.069	56.04	5.166	0.001
Occipital Lobe	55.071	7.504	55.75	7.087	0.581
Parietal Lobe	67.215	8.706	69.04	6.667	0.165
Temporal Lobe	84.335	10.12	89.81	8.122	6E-04
Left Cerebrum	225.18	24.17	231.7	19.87	0.084
Right Cerebrum	226.7	24.2	233.2	19.79	0.085

Table 2: Results of our tests

ELECTRONICS IN HEALTHCARE: THE GREATEST INNOVATIONS

BY **ANDREW FLAXMAN**, UK AND EUROPEAN PATENT ATTORNEY, AND **OLIVIA MURPHY**, UK PATENT ATTORNEY, BOTH AT INTELLECTUAL PROPERTY FIRM HASELTINE LAKE

Each year on the 26th of April we celebrate the role of intellectual property (IP) in driving innovation; this year, World IP Day focused on innovations that have improved lives in the areas of health, safety and comfort. Here are some of the most notable electronic medical device innovations to date:

Virtual Reality In Healthcare

Virtual reality (VR) is becoming increasingly commonplace in many areas of healthcare, from training junior doctors in a safe environment, to helping cure phobias and post-traumatic stress disorder (PTSD), and for pain management.

The real step forward comes in the use of VR to visualise parts of the body from every possible angle without having to cut it open. One incredible story tells of Dr Redmond Burke, who performed heart surgery on a baby after using Google Cardboard to visualise her heart before the surgery. Every moment wasted on the operating table increases patient risk, but by viewing the heart beforehand, Dr Burke greatly reduced the time needed in surgery.

Google Cardboard is a VR device made entirely from cardboard, designed as a head-mount for a smartphone. Cardboard-compatible apps run on the smartphone for a VR experience.

The design was initially conceived with gaming in mind – it's not clear whether the Google inventing team ever thought it would be used to save lives!

A US design patent US D750,074 was granted to Google in 2016.

Medical Imaging

Computed tomography (CT) scans make use of a series of x-ray images, taken over a range of angles and combined to generate a cross-sectional image of a target.

The idea of imaging a slice of the body on a radiographic film was first proposed in the 1930s by a Genovese radiologist called Alessandro Vallebona. The theory developed for decades, until in 1971 Sir Godfrey Hounsfield and Dr Allan Cormack presented the first commercially-viable CT scanner, for which they won the Novel Prize in Physiology for Medicine in 1979.

The original concept for magnetic resonance imaging (MRI) was developed by an American, Dr Raymond Vahan Damadian, in 1969. When a strong magnetic field is applied across a target to be examined, hydrogen atoms that are present in water and fat of all living beings are caused to generate a radio-frequency signal that can

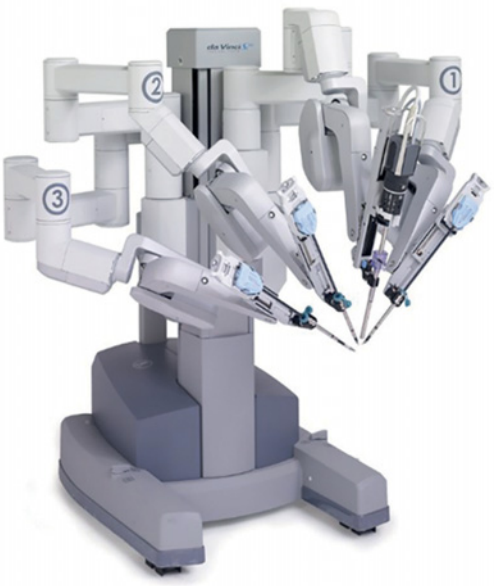


Figure 1: Da Vinci surgical system

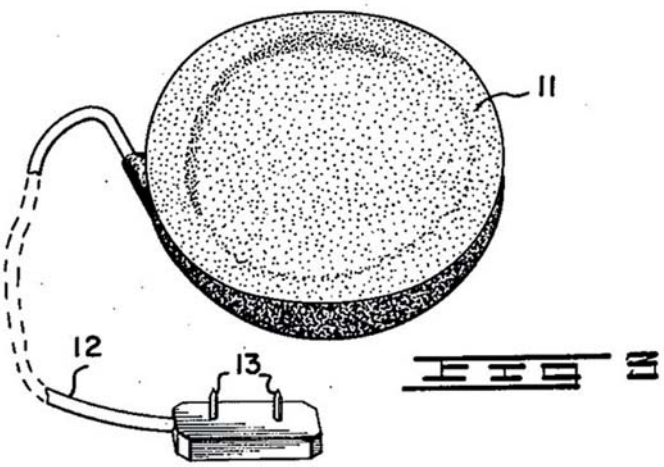


Figure 2: Dr C. Walton Lillehei pacemaker

be detected by a nearby antenna. Therefore, an MRI scan essentially provides a map of water and fat within the target.

The first MRI scanner was constructed and tested in 1977 and, since then, thousands of patent applications have been filed relating to the field of MRI scanning, with some 20,000 MRI scanners now in use all around the world.

Robotic/A.I. Surgery

In 1992, the first pure robotic surgery was performed by Dr Senthil Nathan using the PROBOT, which was developed at Imperial College London. The PROBOT was specifically designed for transurethral resection of the prostate.

While PROBOT was being developed, ROBODOC, a robotic system designed to assist hip replacement surgeries, was the first surgical robot approved by the US's Food and Drug Administration (FDA).

Further development of robotic systems was carried out by SRI International and Intuitive Surgical, who introduced the 'da Vinci surgical system' (Figure 1). Although the telesurgical robot was originally intended to facilitate remotely-performed surgery in battlefields and other difficult-to-access environments, it turned out also to be more useful for minimally-invasive routine surgery.

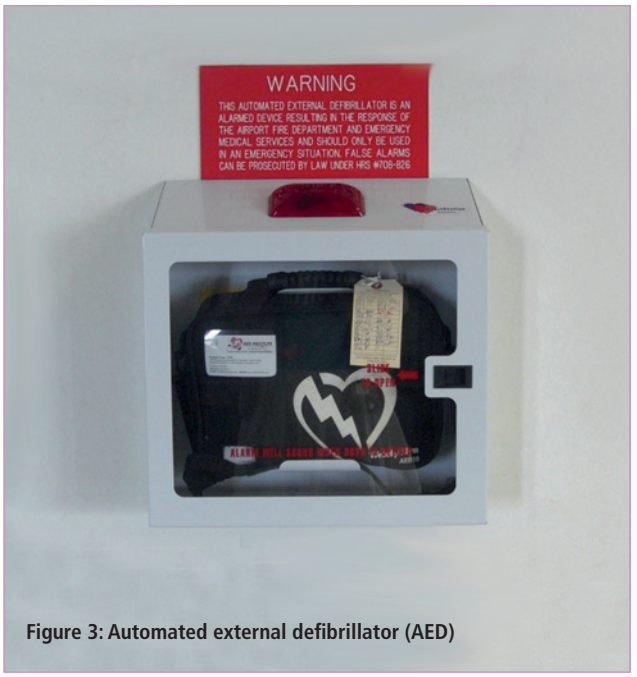


Figure 3: Automated external defibrillator (AED)

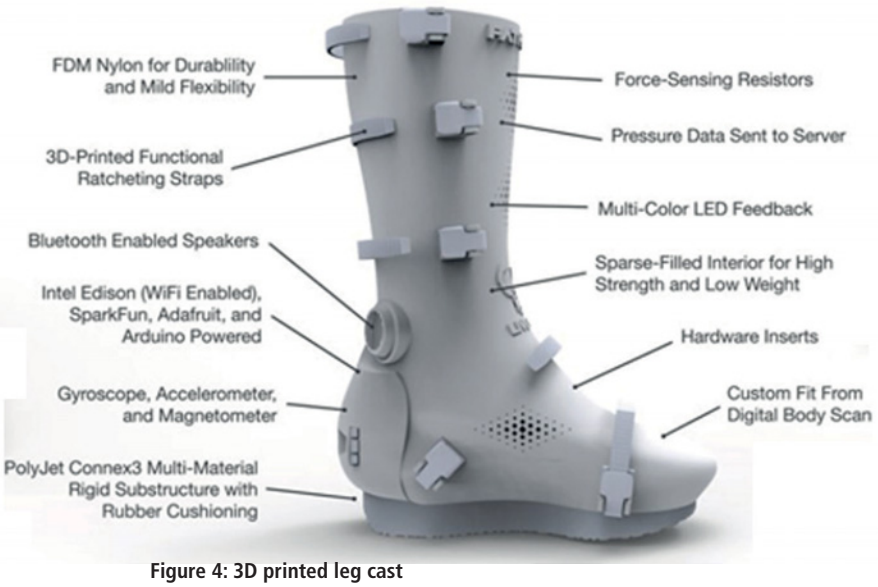


Figure 4: 3D printed leg cast

The da Vinci system senses the surgeon's hand movements and electronically translates them into scaled-down micro-movements to control the instruments. It also detects and filters out any tremors in the surgeon's hand movements, so that are not duplicated robotically.

The camera used in the system provides a true stereoscopic picture transmitted to the surgeon's console.

Milestones of the da Vinci system include the first robotically-assisted heart bypass in 1998, and the first all-robotic-assisted kidney transplant, performed in 2009.

Interestingly, several core patents relating to the da Vinci robotic design expired in 2015 and 2016, particularly patents covering some of the basic robotic concepts implemented in the company's products, including control of robotic arms and tools with a remote controller, and imaging functionality provided by the surgical robot. The expiration of these patents may potentially open up the field for more innovation in the near future.

Pacemaker

The theory behind electrically stimulating the heart was known as far back as the early 1900s. So, in the 1950s came Medtronic, the company where considerable progress was made in the development of the pacemaker.

Dr C. Walton Lillehei was a 1950s American open-heart surgeon who applied mains-powered pacemakers to patients during surgery, but regular power outages made the mains-powered devices unreliable.

Around that time, Earl Bakken, who co-founded Medtronic, was visiting Lillehei's hospital and witnessed the problems with the existing pacemakers. He was asked to design an improved device, to which he agreed, and Medtronic's external battery-powered pacemaker was born; see Figure 2.

Over a decade later, electrical engineer William Greatbatch worked with a small team of doctors to develop the first viable implantable pacemaker. US patent number 3,057,356 was granted to Greatbatch in 1962 for his invention. Since then, pacemaker designs have greatly improved, with the latest versions being as small as a pill and directly implantable in the heart.

Defibrillator

Defibrillators are used to deliver a jolt of electric current to the heart, which can be used to alter or restart a person's heartbeat, for example during cardiopulmonary resuscitation (CPR).

External defibrillators apply shocks to a patient's heart through paddles applied to the patient's chest on either side of the heart. The development of the external defibrillator began near the end of the 19th century, when it was demonstrated that small electric shocks could change heartbeat patterns.

Implantable cardioverter-defibrillators (ICDs) are smaller devices into a patient's body to correct life-threatening cardiac dysrhythmias (irregular heartbeats). The ICD was developed in the late 1960s, and US patent number 3,614,954 ("Electronic Standby Defibrillator") was granted in October 1971. The first device was implanted in 1980 and, since then, ICDs have been implanted in millions of people… and at least two dogs!

The development of defibrillation devices in recent years had extended to automated external defibrillators (AEDs; Figure 3) – suitable for use without medical training – being made available in many public areas.

3D Printed Leg Cast

3D printers are at the forefront of modern technology. So, it's perhaps unsurprising that someone has taken 3D printing power into the medical world.

The 3D printed leg cast shown in Figure 4 is known as the BOOMcast; it's fitted with embedded electronics that allow a doctor to monitor the leg's physical state from anywhere in the world. It also has pressure sensors, Bluetooth speakers, LED lights, a gyroscope, an accelerometer and WiFi-enabled Intel Edison – more gadgets than the average phone.

Since it is 3D printed, each BOOMcast can be made as a custom fit from a digital body scan.

Health-Monitoring Wearable Devices

In this day and age you'd be hard-pressed to find someone who's never heard of some sort of fitness tracker, be that in an Apple Watch, a Fitbit, Garmin, TomTom, Jawbone and so on. This type of tracker has also made its way into the medical field, to measure vital signs and overall patient welfare.

Imec has not only produced a remote electrocardiogram (ECG) patch to keep tabs on a patient's heart activity, but has extended the wearable devices to a headset with electroencephalographic (EEG) capabilities, to monitor a patient's brain activity continuously and remotely.

This is our list of the most impressive electronics medical innovations to date; but radical innovations never stop; who knows what we'll discuss on World IP Day next year. ●

www.electronicsworld.co.uk

June 2017

Electronics WORLD

T&M supplement

CONTENTS

2-Slot LXI/USB Modular Chassis

from Pickering Interfaces

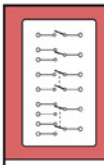
pickeringtest.com

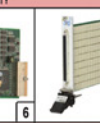
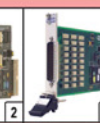
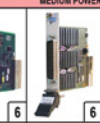
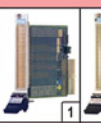
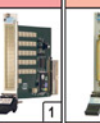
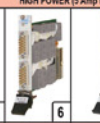
Pickering Interfaces

pickering

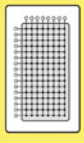
Pickering PXI Mo

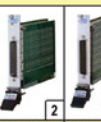
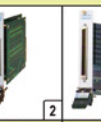
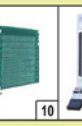
General Purpose Switches



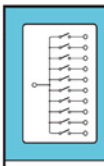
	LOW DENSITY (<50 Relays)		HIGH DENSITY						MEDIUM POWER (2 Amp to 5 Amp)						HIGH POWER (5 Amp to 40 Amp)								
	 6		 NEW 2016 1	 6	 11				 2	 6	 6	 3	 1	 1	 4	 3	 6	 8		
Features	• Low Cost General Purpose • Uses High Reliability Pickering Reed Relays		• Very High Density Electro-Mechanical Relay Module	• Highest Density Reed Relay PXI Modules • Pin Compatible With 40-145/6/8		• Pin Compatible With 40-140A/141/143 • 60W Maximum Power			• Medium Power Relays	• Low Cost Relay Module For Medium Power Switching Applications		• Power Ruthenium Reed Relays	• High Density Power Relays	• High Density • Highly Versatile Mixed Relay Configurations	• High Density • Low Cost Version of 40-138	• High Power • DPST and SPDT options		• High Power • SPST and DPST options		• High Density • High Current	• Very High Power • Suitable For Automotive Test			• 50A Peak Current
Model Family	40-110	40-115	40-100	40-140A	40-141	40-143	40-145	40-146	40-130	40-131	40-132	40-136	40-137	40-138	40-139	40-150/151	40-155/156	40-160		40-161	40-170	40-180	40-181	40-182
Configurations	16 or 32 x SPDT	16 or 32 x SPST	16 or 24 x DPST	83 x SPDT	50, 75 or 100 x SPST	50 x DPST	48 or 64 x SPDT	50, 75 or 100 x SPST (NO or NC)	25 or 50 x DPST	32, 48 or 64 x SPDT	8 or 13 x DPDT	16 or 26 x SPDT	16 or 32 x SPST	16 or 19 x DPST	16, 25 or 32 x SPST	12, 16 or 19 x DPST	16 x SPST	32 or 39 x SPST	Module accepts mix of SPST, DPST, SPDT & DPDT Relays	Up to 80 x SPST, 40 x DPST, 52 x SPDT or 26 x DPDT	8 or 12 x DPDT	8 or 16 x SPDT	10 or 20 x SPST	10 x DPST	10, 12, 16 x SPST or 6, 12 x SPDT	2 x SPST or 2 x DPDT	2 or 4 x SPST	2 x SPDT	3 or 6 x SPST
Relay Type	Pickering Instrumentation Reed		Electro-mechanical	Pickering Instrumentation Reed			Electro-mechanical		Electro-mechanical			Pickering Instrumentation Reed	Electro-mechanical											
Max Switch Voltage	150VDC/100VAC		200VDC/140VAC	150VDC/100VAC					220VDC/ 125VAC	300VDC/250VAC		200V	110VDC/250VAC	300VDC/250VAC		125VDC/ 250VAC	35VDC/ 250VAC	125VDC/250VAC		300VDC/ 250VAC	30VDC/ 250VAC	14VDC or 28VDC		200VDC/ AC peak
Max Switch/Carry Current	0.25A/1A	1A/1.2A	2A	1A		0.25A/1A	1A		2A			1A/2.5A or 1A/2A	5A	2A		5A		10A	8A	16A	30A	40A or 20A	10A	
Max Switch Power	3W	20W	60W	20W		3W	60W		60W			40W	150W	90W	60W	175W/125VA		300W/2500VA	240W/2000VA	480W/4000VA	900W/7500VA	560W	2000W	
Typical Operate Time	0.5ms		3ms	0.5ms			3ms		3ms			0.5ms	10ms	3ms		5ms		10ms			30ms	15ms	20µs	
Connector Type	96-pin Micro-D		500-pin SEARAY	200-pin LFH					50 or 78-pin D-type	78-pin D-type		50 or 78-pin D-type	37-pin D-type	78-pin D-type	160-pin DIN 41612	37 or 50-pin D-type		20-pin GMCT			8-pin Power D		
Width (PXI-1, PXI-hybrid)	1-Slot		1-Slot						1-Slot							1-Slot				2-Slot			1 or 2-Slot
Mating Connectors and Cabling Datasheet	90-016D		90-021D	90-002D					90-005D (50) 90-006D (78)	90-006D		90-005D (50) 90-006D (78)	90-007D	90-006D	90-001D	90-007D (37) 90-005D (50)		90-014D			90-012D		
Spare Relay Kits	91-100-017/045/058/061/074		91-100-001	91-100-005/011/015/025			91-100-001		91-100-037	91-100-001		91-100-036/051	91-100-020	91-100-001		91-100-049/052		91-100-071/052			--			

Mat



	LOW DENSITY (<128 Crosspoints)		MEDIUM DENSITY (128 to 256 Crosspoints)																						
	 12	 3	 5				 NEW 2016 2	 18	 8	 2	 3	 2	 NEW 2016 1	 4	 10		
Features	• Reed Relay Matrix	• 2-Amp • 2-Pole	• 2A Matrix With up to 224 Crosspoints				BiRST		• Reed Relay Matrix				• Signal Insertion & Monitor Matrix	• 2A Matrix • 128 Crosspoints BiRST		• Fast Operate Time • Long Service Life		• Ultra High Density	BiRST	• Ultra High Density				
Model Family	40-510/511/512/513	40-515/516/517	40-505	40-506	40-507	40-508	40-509	40-518A/518A	40-520	40-521	40-522	40-523/524	40-525A	40-527	40-528A	40-500	40-501	40-530	40-533B	40-531/532	40-534A	40-538		
Configurations	Single 12x4, 12x8, 24x4 or Dual 12x4, 1 or 2-Pole or 1-Pole Shielded	Single 8x8, 16x4 or Dual 8x4, 2-Pole	Single 42x4, 1-Pole	Single 32x6, 1-Pole	Single 25x8, 1-Pole	Single 18x12, 1-Pole	Single 14x16, 1-Pole	Single 16x8 or 32x4, 2-Pole	1-Pole Matrices Between 16x16 & 32x2	Single 24x8, 1 or 2-Pole	Dual 12x8, 1 or 2-Pole	Single 44x4, 1-Pole, 2-Pole, 1-Pole Shielded or 46x1, 1-Pole	34x4, or 16x4, with Switched Loop-Thru	Single 64x2, 1-Pole	Single 32x4 1-Pole	Single 16x8, 1-Pole	Single 64x4, 1-Pole		Single 32x8, 1-Pole	Single 64x4 or 64x2, 1-Pole or 2-Pole	Single 32x8 or Dual 16x8, 1, 2-Pole or 1-Pole Shielded	Dual 32x4, 1, 2-Pole or Shielded	Single 55x8, 1-Pole	Single 44x8	
Relay Type	Pickering Instrumentation Reed	Electro-mechanical	Electro-mechanical						Pickering Instrumentation Reed				Electro-mechanical			Solid State		Pickering Instrumentation Reed						
Max Switch Voltage	150VDC/100VAC	300VDC/ 250VAC	300VDC/250VAC						150VDC/100VAC				220VDC/ 150VAC	300VDC/250VAC		±60VDC/AC peak	±100VDC/AC peak	150VDC/100VAC						
Max Switch/Carry Current	1A/1.2A	2A	2A						1A/1.2A	0.5A/1A	1A/ 1.25A		2A			0.5A	0.15A	1A						0.5A
Max Switch Power	20W	60W	60W						15W	10W	20W		60W			30W	15W	20W	15W					10W
Typical Operate Time	0.5ms	3ms	6.5ms				3ms		0.5ms				3ms			400µs		0.5ms						
Connector Type	68-pin Micro-D	50-pin D-type	160-pin DIN 41612	78-pin D-type	78-pin D-type	50-pin D-type	50-pin D-type	78-pin D-type	50-pin D-type	96-pin Micro-D			78-pin D-type	50-pin D-type	37-pin D-type	78-pin D-type		96-pin Micro-D	200-pin LFH	96-pin Micro-D	200-pin LFH	96-pin Mi		
Width (PXI-1, PXI-hybrid)	1-Slot		1-Slot																					
Mating Connectors and Cabling Datasheet	90-015D	90-005D	90-001D	90-006D	90-006D	90-005D	90-005D	90-006D	90-005D	90-016D			90-006D	90-005D	90-007D	90-006D		90-016D	90-002D	90-016D	90-002D	90-01		
Spare Relay Kits	91-100-003/008/011	91-100-001	91-100-001						91-100-097	91-100-012 /016/018	91-100-003 /008/011	91-100-003/ 008/011/030	91-100-001			--		91-100-019	91-100-012 /018	91-100-012/016/018		91-100-004/009		

Multip



	LOW DENSITY MUX			HIGH DENSITY MUX																					
	 8	 1	 18	 16	 18	 8	 3	 2	 2	11	6	2	1	1	NEW 2016 20	29		
Features	• Low Density, Low Cost • Single and Dual Configurations	• Differential Thermal Offset <1.5µV	• Low Cost • 2A Switching	• Very High Density • Wide Range of Configurations		• Multiple Configurations • High Speed, Long Life	• Configurable • Equivalent to 40-612		• Configurable with inter-bank relays		• High Density	• Wide Range of Configurations	• High Density • Low Cost		• Versatile - Many Possible Configurations • Software Configurable		• Low Cost • Wide Range of Configurations		• High Density MUX in Pickering BRIC format		• Power	
Model Family	40-630	40-632	40-620	40-610	40-615	40-680	40-681	40-682	40-683	40-616	40-617	40-640	40-670A	40-675	40-611	40-612	40-613	40-614		40-670				
Configurations	Single 64:1 or Dual 32:1 1-Pole, Single 32:1 or Dual 16:1 2-Pole, Single 16:1 4-Pole	Single 48:1 1-Pole, Dual 24:1 1-Pole, Single 24:1 2-Pole	Single 23:1 1-Pole Low Thermal EMF MUX	Between Single 128:1 1-Pole & 8-Bank 8:1 2-Pole (1-pole shielded reed available)	Between Single 160:1 1-Pole & 20-Bank 4:1 2-Pole	Between Single 160:1 1-Pole & 20-Bank 8:1 1-Pole	Between Single 128:1 1-Pole & 8-Bank 8:1 2-Pole			16-Bank 5:1, 1-Pole	18-Bank 3:1, 1-Pole	Single 94:1 1-Pole or 47:1 2-Pole	Between Single 158:1 1-Pole & Single 5:1 32-Pole	Between Single 158:1 1-Pole & Single 5:1 32-Pole	Single 158:1 1-Pole or Single 79:1 2-Pole	8 Basic Configurations from Single 128:1 1-Pole to 8-Bank 8:1 2-Pole	5 Basic Configurations from Single 64:1 2-Pole to 16-Bank 4:1 2-Pole	20 Configurations: 1 to 16 Banks, 4 to 128 Channels, 1 to 32 Poles		Max configurations between 6:1 160-Pole & 96:1 10-Pole with switched loop-thru		Max co between 8-4 with	
Relay Type	Pickering Instrumentation Reed		Electro-mechanical	Pickering Instrumentation Reed		Solid State				Pickering Instrumentation Reed						Electro-mechanical								
Max Switch Voltage	150VDC/100VAC	100V	300VDC/250VAC	150VDC/100VAC		±15V	±60V	±40V	±100V	100V	150VDC/100VAC					300VDC/250VAC		200VDC/140VAC		100VDC/100VAC peak				
Max Switch/Carry Current	1A/1.2A	0.5A/1A	2A	1A/1.2A		20mA	350mA	250mA	125mA	1A	0.5A/1.2A	0.5A	1A			2A				1A				
Max Switch Power	20W		60W	20W		3W	21W	10W	12.5W	20W		10W				60W								
Typical Operate Time	0.5ms		3ms	0.5ms		200µs	80µs	500µs		0.5ms						3ms								
Connector Type	68-pin Micro-D	96-pin Micro-D	78-pin D-type	200-pin LFH		160-pin DIN 41612				96-pin Micro-D		200-pin LFH				160-pin DIN 41612								50-
Width (PXI-1, PXI-hybrid)	1-Slot			1-Slot																	8-Slot			
Mating Connectors and Cabling Datasheet	90-015D	90-016D	90-006D	90-002D		90-001D				90-016D		90-002D				90-001D								
Spare Relay Kits	91-100-003/005/011	91-100-043	91-100-001	91-100-003/008/011/015		--				91-100-003	91-100-005/011	91-100-013/018				91-100-001								91

RF & Microw

	RF SPDT SWITCH				RF MATRIX																				
	4	8	7	4	1	8	2	3	4	12	2	4	2	12	4	2	12	4				
Features	• 6GHz Bandwidth • Terminated Channels • High Performance	• High Performance • Low Cost	• Multiple Connector Options	• High Density • High Performance • Low Cost	• 6GHz Bandwidth • High Performance • Compact	• Expandable • High Performance	• Expandable	• X and Y Isolation Switching	• Expandable • Easy Y-Axis Loop-Thru	• Low Loss Expansion Options: 24x8, 32x8, 40x8, 48x8.... • X and Y Isolation Switching						• 6GHz Bandwidth • Terminated Channels • High Performance			• 3GHz Bandwidth • High Performance • Low Cost		• 3GHz Bandwidth • Terminated Channels		• 3GHz Bandwidth • Term	
Model Family	40-880	40-870	40-830	40-710	40-854	40-877	40-837	40-750	40-725	40-726A	40-727	40-728	40-729			40-881	40-882	40-883		40-872	40-832	40-873		
Impedance	50Ω	75Ω	50Ω	75Ω	50Ω	75Ω	50Ω	75Ω	50Ω	75Ω	50Ω	75Ω	50Ω	75Ω		50Ω				75Ω				
Configurations	Dual, Quad, Hex or Octal SPDT	Triple or Hex SPDT	Quad SPDT		9 or 17 x SPDT	Single 4x4	Single or Dual 2x2	8x2	8x9	12x8	16x4	16x2	8x4			Single or Dual SP6T Terminated	Single, Dual, Triple or Quad SP4T Terminated	Single SP8T Terminated	Single SP8T Terminated	Single/Dual/ Quad SP4T		Single or Dual SP4T Terminated			
Max Frequency	6GHz	3GHz	2.7GHz	1GHz to 2.5GHz	1GHz to 2GHz	6GHz	2.5GHz	1.5GHz	500 MHz	250 MHz	300 MHz	250 MHz	300 MHz / 100 MHz	300 MHz / 100 MHz	300 MHz / 100 MHz	6GHz								
Insertion Loss	<3dB	<0.5dB	<0.9dB	<3dB	<0.75dB	<0.6dB	<5dB	<1.4dB	<1.6dB	<3dB						<4.7dB	<4.5dB	<5dB	<6dB	<1dB	<1.6dB	<1dB		
VSWR	<1.65:1	<1.25:1	<1.6:1	<2.0:1	<2.2:1	<1.5:1	<1.5:1	<1.8:1	<3:1	Path Dependent						<1.5:1	<1.45:1	<1.5:1	<1.65:1	<1.25:1	<1.6:1	<1.3:1		
Max Power	+30dBm	10W				+30dBm	10W									+30dBm		10W		1W Terminated				2W
Typical Operate Time	50µs	3ms	10ms	3ms		50µs	3ms	5ms	0.5ms	5ms						50µs								
Relay Type	Solid State	Electro-mechanical				Solid State	Electro-mechanical		Instrumentation Reed	Reed & Electro-mechanical						Solid State								
Connector Type	SMA	SMB, MCX	BNC, SMB, SMA	BNC, SMZ, 1.0/2.3 SMB	SMB	SMA	SMB, MCX	SMA, SMB	SMB	SMB or MS-M RF						SMA								
Width (PXI-1, PXI-hybrid)	1, 2 or 3-Slot	1-Slot	1 or 2-Slot		2-Slot	1-Slot	3-Slot	1-Slot								1 or 2-Slot	1, 2 or 3-Slot	2 or 3-Slot						

odule Map - 2017

BRIC Large Matrices

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HIGH VOLTAGE

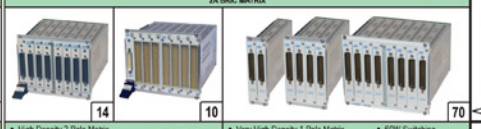
			3	4
			• 120A Peak Current	• 90A Peak Current
			40-183	40-184
			6 x SPST	3 or 6 x SPST
			Solid State	
			40VDC/ AC peak	100VDC/ AC peak
			40A	25A
			1600W	2500W
			250µs	
			type	
			1-Slot	1 or 2-Slot

2	3		
• High Voltage Reed Relays	• High Voltage Power Relays		
40-310	40-330		
8 or 16 x SPST	12, 18 or 24 x SPST		
Pickering Rhodium Reed	Electro-mechanical		
1000VDC/1000VAC peak			
0.5A	5A		
10W	150W/1250VA		
0.5ms	10ms		
37-pin High Voltage D-type	50-pin High Voltage D-type		
1-Slot			
90-007D	90-005D		
91-100-033	91-100-020		

190+

HIGH DENSITY BRIC MATRIX

2A BRIC MATRIX



Number shows the quantity of modules in a particular range

Features																
	• Integrated PXI Matrix With Built In High Performance Analog Bus • Highest Quality Reed Relays				• Available as 2, 4 or 8 Slot 3U PXI Modules • x4, x8, x16 & x32 Options • Built-In Self Test				100+	• High Density 2-Pole Matrix • 60W Switching • Built-In Self Test		14	• Very High Density 1-Pole Matrix • x4, x6, x8, x12 & x16 Options • Electro-mechanical Relays		10	• 60W Switching • Available as 2, 4 or 8 Slot 3U PXI Modules	70	Features
Model Family	40-560A			40-561A			40-562A				40-563A	40-565B	40-566A	40-568	40-596	40-567	40-597	40-598	Model Family
Configurations	From 184x4 to 1104x4, 1-Pole	From 92x8 to 552x8, 1-Pole	From 46x16 to 276x16, 1-Pole	From 60x8 to 360x8, 1 or 2-Pole	From 30x16 to 180x16, 1 or 2-Pole		From 88x4 to 528x4, 1 or 2-Pole	From 44x8 to 264x8, 1 or 2-Pole	From 22x16 to 132x16, 1 or 2-Pole	From 10x32 to 60x32, 1-Pole	From 64x8 to 384x8, 1-Pole	From 29x8 to 232x8, 2-Pole	From 55x4 to 385x4, 2-Pole	From 75x4 to 600x4, 1-Pole	From 58x6 to 464x6, 1-Pole	From 44x8 to 352x8, 1-Pole	From 32x12 to 256x12, 1-Pole	From 24x16 to 192x16, 1-Pole	Configurations
Relay Type	Pickering Instrumentation Reed										Solid State	Electro-mechanical							Relay Type
Max Switch Voltage	150VDC/100VAC										±40V	150VDC/100VAC		200VDC /140VAC	150VDC /100VAC	100VDC/70VAC			Max Switch Voltage
Max Switch/Carry Current	0.5A			1A/1.2A							0.25A	2A							Max Switch/Carry Current
Max Switch Power	10W			20W							10W	60W							Max Switch Power
Typical Operate Time	1ms										20µs	3ms		6.5ms					Typical Operate Time
Connector Type	96-pin Micro-D	68-pin Micro-D		68-pin & 96-pin Micro-D	68-pin Micro-D	96-pin Micro-D	68-pin Micro-D					78-pin D-type	160-pin DIN 41612 & 25-pin D-type	78-pin D-type		50-pin D-type	37-pin D-type	25-pin D-type	Connector Type
Width (PXI-1, PXI-hybrid)	2, 4 or 8-Slot											2, 4 or 8-Slot							Width (PXI-1, PXI-hybrid)
Mating Connectors and Cabling Datasheet	90-016D	90-015D		90-015D & 90-016D	90-015D	90-016D	90-015D					90-006D	90-001D & 90-008D	90-006D		90-005D	90-007D	90-008D	Mating Connectors and Cabling Datasheet
Spare Relay Kits	91-100-010			91-100-022			91-100-003/005/011				–	91-100-001							Spare Relay Kits

rices

112

HIGH DENSITY (256 to 528 Crosspoints)

	3	3	5	1	1	1	1	4												
	• Highest Density in 1-Slot • 528 Crosspoints		• Highest Density Single Slot 3U 2 Amp Matrices • Up To 448 Crosspoints		• Ultra High Density			• Highest Density 1-Slot 2 Amp Matrices												
-535/536/537	40-540	40-541	40-542	40-575	40-576	40-577	40-578	40-579	40-580	40-581	40-582	40-583	40-584	40-585	40-586A	40-587A				
le 92x4, Single 8 or Dual 44x4, 1-Pole	Single 132x4, 1-Pole	Single 66x8, 1-Pole	Single 33x16, 1-Pole	Single 85x4, 1-Pole	Single 66x8, 1-Pole	Single 50x8, 1-Pole	Single 36x12, 1-Pole	Single 28x16, 1-Pole	Single 32x8, 2-Pole	Single 33x8, 2-Pole	Single 16x16, 2-Pole	Single 64x4, 2-Pole	Single 128x2, 1-Pole	Single 64x4, 1-Pole	Single 32x8, 1-Pole	Single 16x16, 1-Pole				
	Electro-mechanical																			
	300VDC/250VAC			150VDC/ 100VAC				300VDC/250VAC												
	2A			1A	2A															
	60W																			
	6.5ms			3ms																
Micro-D	200-pin LFH	96-pin micro-D	68-pin micro-D	160-pin DIN 41612	78-pin D-type	78-pin D-type	50-pin D-type	50-pin D-type	160-pin DIN 41612	96-pin micro-D	78-pin D-type	160-pin DIN 41612	78-pin D-type	50-pin D-type	37-pin D-type					
	1-Slot																			
6D	90-002D	90-016D	90-015D	90-001D	90-006D	90-006D	90-005D	90-005D	90-001D	90-016D	90-006D	90-001D	90-006D	90-005D	90-007D					
91-100-004 /006/009	91-100-006			91-100-001																

HIGH POWER (2 Amp to 40 Amp)

4	4	2	4	4	4	3		
• High Density • 2 Amp	• High Density • 5 Amp	• 2-Pole • 5 Amp	• High Density • 10 Amp	• High Density • 16 Amp	• High Speed, Long Service Life • High Inrush Current			
40-545/546/547/548	40-549	40-550	40-551	40-552	40-553	40-554	40-555	
Single 10x1, 10x8, 20x4 or Dual 10x4, 1-Pole	Single 16x4, 8x8, 8x4 or Dual 8x4, 1-Pole	Single 8x4, 2-Pole	Single 8x4, 8x2 or 4x4 1-Pole (8x4 loop-thru option)	Single 4x4 or 8x2 1-Pole with loop-thru option	Single 6x2, 1-Pole		Single 8x2, 1-Pole	
Electro-mechanical					Solid State			
110VDC/250VAC		125VDC/250VAC		400VDC/ 250VAC	±200VDC/ AC peak		±40VDC/ AC peak	
2A	5A		10A	16A	10A		40A	
90W/500VA	150W/1250VA		300W/2500VA	448W/4000VA	2000W		1600W	
6ms	10ms				120µs		250µs	
37-pin D-type	25-pin D-type	37-pin D or 20-pin GMCT	20-pin GMCT		8-pin Power D-type			
1-Slot					2-Slot			
90-007D	90-008D	90-007D (37) 90-014D (20)	90-014D		90-012D			
91-100-020		91-100-032	91-100-071	91-100-092	–			

HIGH VOLTAGE

3	2
	• High Voltage Power Matrix
	40-332
	Single 12x2 or 6x4, 1-Pole
	Electro-mechanical
	1000VDC/ 1000VAC peak
	5A
	150W/1250VA
	10ms
	37-pin High Voltage D-type
	1-Slot
	90-007D
	91-100-020

Number shows the quantity of modules in a particular range

Features
Model Family
Configurations
Relay Type
Max Switch Voltage
Max Switch/Carry Current
Max Switch Power
Typical Operate Time
Connector Type
Width (PXI-1, PXI-hybrid)
Mating Connectors and Cabling Datasheet
Spare Relay Kits

plexers

232

HIGH POWER MUX

29	1	12	4	1	1	4	1	1	3	8	7	2	4							
MUX in Pickering ormat	• 5A Power MUX	• 5A MUX - Multiple Configurations	• High Speed • Long Life	• Configurable • 2-Pole Switching	• High Density • 2-Pole Switching	• High Density • 1-Pole Switching	• Power & Sense MUX	• High Density • 2-Pole Switching	• 1 or 2-Pole Power MUX • 10A or 8A Current Handling		• High Density • 10A Switching	• High Density • 16A Switching	• Suitable For Automotive Test	• High Speed, Long Life • High Inrush Current						
40-571	40-650	40-651	40-652	40-655	40-656	40-657	40-658	40-659	40-660	40-665	40-661	40-662	40-664	40-666	40-667				
configurations en 6:1 48-Pole 8:1 6-Pole h loop-thru	Single 16:1, 2-Pole	1-Bank 48:1, 2-Bank 24:1, 4-Bank 11:1 or 8-Bank 5:1 1-Pole	Single 48:1 1-pole, Dual 24:1 1-pole, Single 24:1 2-pole or Single 24:1 1-Pole	7-Bank 4:1, 2-Pole	Single 38:1, 2-Pole	8-Bank 8:1, 4-Bank 16:1, 2-Bank 32:1 or Single 64:1, 1-Pole	Dual 18:1, 2-Pole	8-Bank 8:1, 2-Pole	Single 10:1, 2-Pole	Single 10:1, 1-Pole / Single 18:1, 1-Pole	8-Bank 4:1, 4-Bank 8:1, Dual 16:1, Single 32:1, 5-Bank 6:1, 4 Bank 4:1, Dual 8:1, Single 16:1	Quad 4:1, Quad 6:1, Dual 8:1, Dual 4:1, Single 16:1, Single 12:1 or Single 8:1	Single 4:1, 1-Pole	Single 6:1 or Dual 3:1, 1-Pole						
	Electro-mechanical		Solid State	Electro-mechanical			Instrumentation Reed	Electro-mechanical						Solid State						
k	125VDC/250VAC	110VDC/250VAC	±100V	220VDC/125VAC		110VDC/250VAC	200VDC/240VAC (Power) & 200VDC (Sense)	300VDC/250VAC	125VDC/250VAC			300VDC/250VAC	14VDC or 28VDC	±200VDC/ AC peak	±40VDC/ AC peak					
3A	5A			2A			1A/2A (Power), 1A/1.2A (Sense)	2A	8A	10A		16A	40A or 20A	10A	40A					
105W	175W/1250VA	150W/1250VA	500W	60W		90W/500VA	40W (Power), 20W (Sense)	60W	240W/2000VA	300W/2500VA		448W/4000VA	560W	2000W	1600W					
10ms	10ms		85µs	3ms		6ms	0.5ms	3ms	10ms				15ms	120µs	250µs					
-pin D-type	37-pin D-type	9 & 50-pin D-type	50-pin D-type	78-pin D-type				160-pin DIN 41612	20-pin GMCT				8-pin Power D-type							
	1-Slot												2-Slot							
90-005D	90-007D	90-003D (9) 90-005D (50)	90-005D	90-006D				90-001D	90-014D				90-012D							
1-100-032	91-100-052	91-100-020	–	91-100-037		91-100-020	91-100-034/051	91-100-001	91-100-052	91-100-071		91-100-092	–							

HIGH VOLTAGE

2	6
• High Voltage • Hot Switch 750V	• High Voltage • 1-Pole Power MUX
40-320	40-331
Single 12:1 or 24:1 1-Pole	Single 24:1, Dual 12:1, Quad 6:1, Hex 4:1, Octal 3:1 or Twelve 2:1
Rhodium Reed	Electro-mechanical
1000VDC/1000VAC peak	
0.5A	5A
10W	150W/1250VA
0.5ms	10ms
37-pin High Voltage D-type	
1-Slot	
90-007D	
91-100-033	91-100-020

Number shows the quantity of modules in a particular range

Features
Model Family
Configurations
Relay Type
Max Switch Voltage
Max Switch/Carry Current
Max Switch Power
Typical Operate Time
Connector Type
Width (PXI-1, PXI-hybrid)
Mating Connectors and Cabling Datasheet
Spare Relay Kits

vave Switches

242

RF MULTIPLEXER

6	8	4	18	4	4	4	4		18											
z Bandwidth inated Common	• 3GHz Bandwidth • High Performance • Low Cost		• Up to 2GHz Bandwidth • Wider Choice of Connector Types	• 1GHz Bandwidth • Wider Choice of Connector Types		• Wider Choice of Connector Types		• Very High Density • High Performance • Low Cost	• Low Cost • Unterminated	• Low Cost • Terminated Channels										
40-876	40-874	40-834	40-675	40-835	40-740	40-745	40-746	40-747		40-748		40-749		40-755	40-760/2/4/6	40-761/3/5/7				
0Ω	75Ω	50Ω	75Ω		50Ω or 75Ω			50Ω	75Ω	50Ω	75Ω	50Ω	75Ω	50Ω		50Ω				
le, Dual or Quad 4T Terminated	Single or Dual SP8T		Single SP16T		SP4T Terminated	SP4T or SP8T	Dual SP4T	Single SP16T		Dual SP8T		Quad SP4T		4 or 10 off SP4T	5 or 10 off SP4T	Dual, Quad, Octal SP4T, Single, Dual, Quad SP8T, Single, Dual SP16T or Single SP32T				
3GHz					1GHz to 2GHz			1GHz	2GHz	1GHz	1.3GHz	1GHz	1.8GHz	500MHz						
<1.3dB	<1.2dB	<2.1dB	<1.3dB	<1.9dB	<3dB			<1.6dB	<2.9dB	<2.6dB	<1.9dB	<1.5dB	<1.25dB	<1.3dB	<1dB	<3dB				
<1.5:1	<1.2:1	<1.5:1	<1.4:1	<1.6:1	<1.8:1			<1.9:1	<1.92:1	<1.95:1	<1.65:1	<1.85:1	<2.0:1	<1.6:1	<1.8:1	<1.7:1				
W Terminated					10W											0.25W Term.				
3ms					5ms									3ms						
					Electro-mechanical															
SMB, MCX					SMA, SMB, SMZ, 1.0/2.3			SMB, SMA	1.0/2.3, SMB	SMB SMA	1.0/2.3, SMB	SMB, SMA	1.0/2.3, SMB	SMB	MS-M RF	SMB				
1-Slot					1 or 2-Slot										1-Slot	1 or 2-Slot				

MICROWAVE SWITCHING

36			24		35			
• Choice of Bandwidths • Choice of Connector Types • LED Indicators			• Extended Life Versions • Faster Operate Time • LED Indicators		• 1-Slot Remote Mount Versions Available • LED Indicators			
40-780A		40-781	40-782A	40-784A		40-785B		
50Ω	75Ω			50Ω			75Ω	
Single, Dual, Triple or Quad SPDT		Single or Dual SPDT Terminated	Single or Dual Transfer Switch	Single, Dual or Triple SP8T & SP4T		Single, Dual or Triple SP8T MUX		
Up to 65GHz		Up to 40GHz		6GHz, 18GHz, 26.5GHz, 40GHz		Up to 40GHz	40GHz	
<1.1dB		<0.5dB	<0.7dB	<1.1dB			<1.5dB	
<1.9:1		<1.5:1	<1.7:1	<2:1			<1.3:1	
Up to 70W		1W Terminated	Up to 240W	Up to 150W		Up to 240W		
15ms				10ms		15ms		
Microwave Relay								
N-type, SMA, SMA-2.9, SMA-2.4, SMA-1.8, 1.6/5.6		SMA, SMA-2.9					1.6/5.6	
1, 2 or 3-Slot		1 or 2-Slot		2-Slot		1, 3, 4 or 6-Slot		

Number shows the quantity of modules in a particular range

Features
Model Family
Impedance
Configurations
Max Frequency
Insertion Loss
VSWR
Max Power
Typical Operate Time
Relay Type
Connector Type
Width (PXI-1, PXI-hybrid)

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TCP Throughput Testing To The RFC6349 Framework

By Juergen Rummelsberger from Anritsu

Network service quality is one of the most important elements in achieving customer satisfaction for a network operator's business clients. Typically, the service level agreements (SLAs) for Ethernet services provided to business clients using video conferencing, YouTube, Facebook or cloud-based applications are based on Layer 2/3 attributes. In this context, the relevant parameters are bandwidth, latency, packet jitter and packet loss, for which network operators and service providers currently check their networks by testing to standards such as IETF RFC 2544 or ITU-T Y.1564.

However, some end users still complain about unsatisfactory throughput, even though these performance tests have shown good results. This could be from other factors such as non-optimised or incorrectly-configured network elements for the TCP (Transmission Control Protocol) connection.

Layer 2 Throughput Is Not Enough

Throughput is a key parameter in the performance of an Ethernet service, defined as the maximum bandwidth that can be achieved without frame loss.

If two network devices want to successfully exchange information, a series of protocols are required to allow them to communicate. Nearly all network connections use the transmission-orientated TCP for communication over the application layer. Consequently, to obtain the effective bandwidth available to the end user, the service provider must adapt throughput testing to the requirements of the TCP layer.

Figure 1 illustrates the Internet

> *"Some end users still complain about unsatisfactory throughput, even though these performance tests have indicated good results"*

Reference model, based on the US Department of Defense (DoD) four-layer model. It shows the gap between the RFC2544/Y.1564 test methods and client expectations related to the experience at the application layer. The only way to resolve this conflict is for the service provider to verify TCP-layer performance. Otherwise, there will inevitably be customer complaints – with their associated support calls or on-site support – or worse, customer churn or fluctuation. In addition to the negative impact on customer satisfaction and loyalty, operating expenses may also increase.

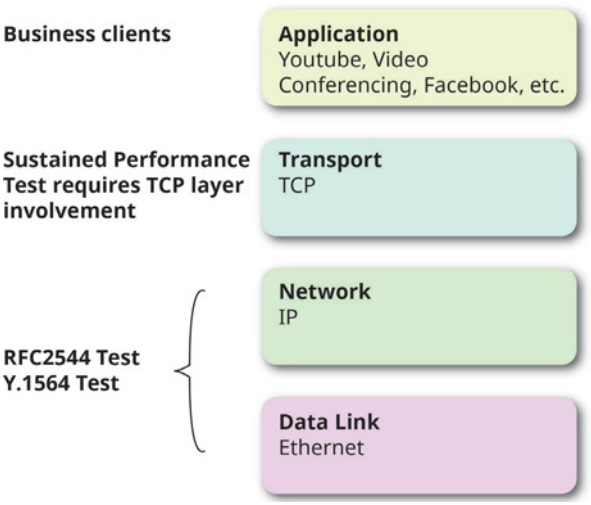
Equally, quality of service (QoS) management processes on Layers 2 and 3 can affect the TCP throughput, because the "bursty" nature of the TCP application and the use of traffic policing may lead to frame loss.

Figure 2 shows some possible causes for a mismatch in a network and the corresponding responsibility of each segment.

TCP Basics

TCP is an end-to-end connection in full duplex mode, allowing the transmission of information in both directions at the same time. Each TCP connection can be

Figure 1: Internet reference model



identified by two endpoints, provided by a structured pair with IP address and port. Hence, a TCP connection is determined by:

- Source IP address;
- Source port;
- Destination IP address;
- Destination port.

A TCP connection is established with a three-way handshake (SYN/SYN-ACK/ACK) and finished with a FIN, ACK. If a client wants to establish a connection, a SYNC signal is sent to the server, which will respond with a SYN-ACK, followed by an ACK from the client.

For security reasons, a "stateful" firewall usually keeps track of the state of network connections. Accordingly, only after the client's ACK response is the connection authenticated as bidirectional and passed by the firewall. Consequently, it is essential for measuring equipment to base a TCP connection on a stateful protocol, since only packets matching a known active connection will be allowed by the firewall. All others will be rejected, resulting in a connection not being established.

The release of a connection is similar. Instead of the SYN, a FIN is used to indicate that no further data will come from the sender. The receipt is confirmed with an ACK followed by a FIN (or shortened ACK-FIN to fit in one packet).

Test Methodology

The test procedure specified in the RFC6349 framework consists of three sequential steps:

- Identify the path MTU (maximum transmission unit) to ensure that the test device is properly configured and

Figure 2: Reasons and responsibility for mismatch

Reason	Network Operator	Service Provider	End User
MTU is small / RTT is large	√	√	
Poor window size optimization		√	√
Sliding window by poor performance of TCP host		√	√
Congestion Control is not appropriate		√	√
Qo5 Configuration / Many Frame Loss	√	√	√

Figure 3: TCP CWND phases

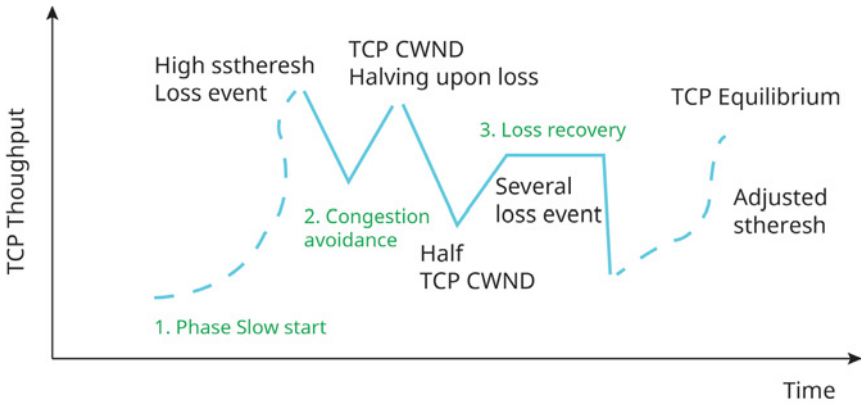


Figure 4: IP network operator

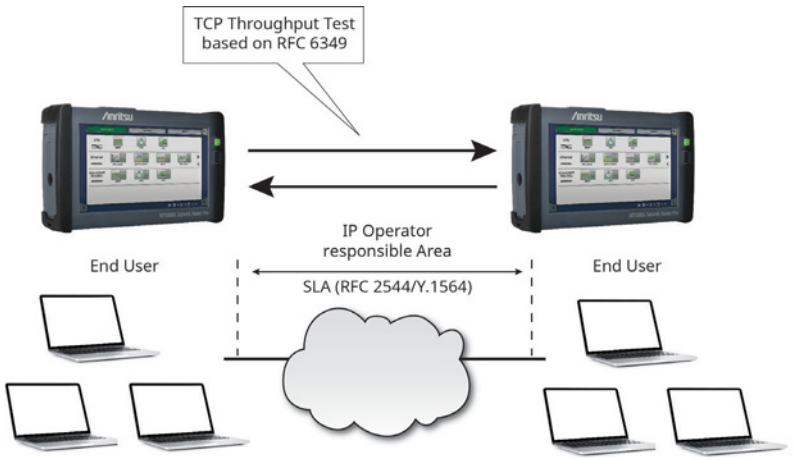


Figure 5: Multiple steps: windows scan (top) and TCP throughput (bottom)

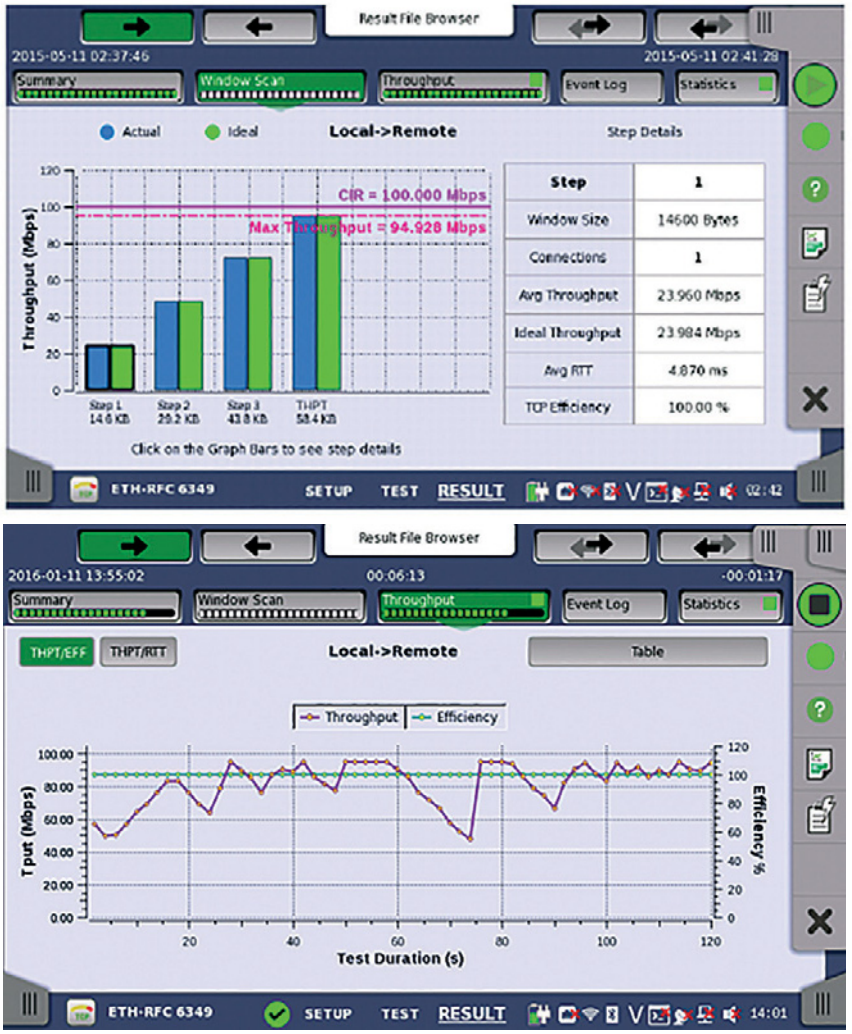
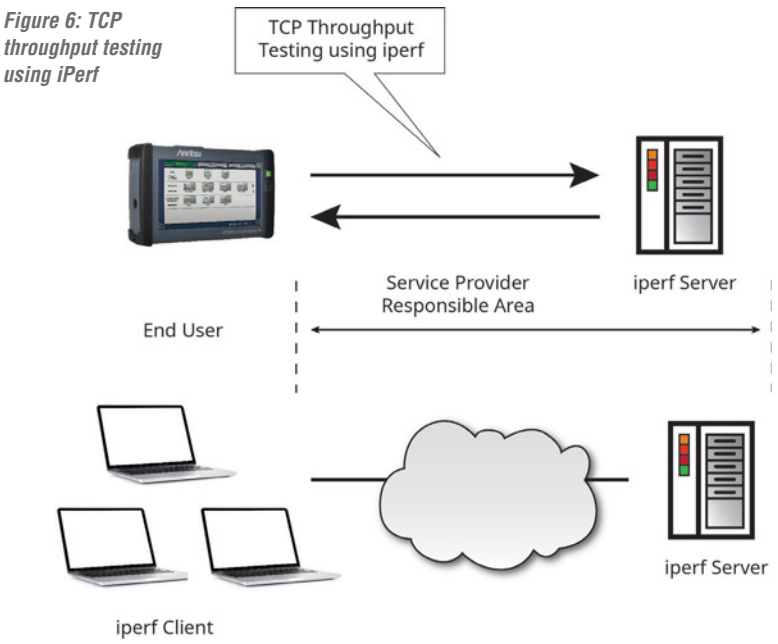


Figure 6: TCP throughput testing using iPerf



fragmentation is prevented.

- Carry out baseline RTT (round-trip time) and BB (bottleneck bandwidth) measurements on the end-to-end network path. The results help estimate the TCP RWND (received window size) and send socket buffer sizes used in further test steps.
- TCP connection throughput test.

TCP is connection-orientated and uses a TCP congestion window on the transmit side. To inform the transmit side how many bytes the receiver can accept for a given time, a TCP receive window is used. The send and receive socket buffer sizes are determined by the bandwidth delay product (BDP), with the goal of achieving the maximum TCP throughput. So as not to limit the TCP performance, the TCP measuring equipment must make it possible for the send-socket buffer and the receive window to be set higher than the BDP.

Based on the network path loss rate, the slow start and the congestion avoidance algorithm (Figure 3), the TCP CWND (congestion window) can then be calculated.

The send-socket buffer must be adjusted to the same value at each end of the network to achieve optimal results.

Finally, the TCP throughput can be calculated.

Usually, network operators test their networks based on RFC2544 and/or Y.1564 to verify the SLA. Considering all these factors, the performance of the TCP connection cannot be ascertained accurately. Only by testing TCP throughput based on RFC6349 can operators help end users configure their networks by emulating the end-user network elements.

After the MTU has been discovered and the round-trip time tested, the optimised window size is tested by verifying the TCP throughput at multiple steps and displaying the results; see Figure 5.

The calculated ideal and tested TCP throughput are displayed, along with details like re-transmitted bytes, round-trip delay, and so on.

Graphs of TCP throughput/time and other parameters can be generated, helping users identify possible issues quickly. Conducting bidirectional tests to display TCP throughput performance across non-symmetrical networks helps in more realistically emulating real networks.

Service providers also face the challenge of allocating servers and networks with maximum achievable performance. Since those services are often on TCP connections, a software-based TCP-throughput test tool is used. iPerf is one commonly applied network testing tool with client and server functionality. However, it depends on the end-user's terminal performance, so its repeatability is correspondingly lower. Modern test instruments like the Anritsu MT1000A/MT1100A portable field testers use hardware-based TCP throughput tests in conjunction with a connected iPerf server for high reliability and high accuracy (Figure 6).

Figure 7: Determining issues

	RFC2544	Y.1564	RFC6349
Single service; issues Layer 2/3 (loss, jitter, etc)	✓	✓	N/A
Multi service; issues Layer 2/3 (loss, jitter, priorisation, etc.)	✗	✓	N/A
Policing effects to the TCP performance	✗	✗	✓
Bursty applications; insufficient buffers	✗	✗	✓
Effect of TCP windows size on thoughput	✗	✗	✓

Certain Testing

As outlined in this article, even if a Layer 2/3 test was passed, the test method chosen may still lead a client to complain about an application's poor performance (browsing, file transfer, etc.) due to a slow network. An indication of the suitability of various test scenarios to different network issues is shown in Figure 7.

Finally, it is important to emphasise that the test methods used on Layer 2/3 and the TCP throughput test should be perceived as complementary. A comprehensive evaluation requires using all available test methods.

To summarise, the implementation of the RFC6349 test method should allow a complete automated measurement procedure, so that even novice technicians can perform measurements and generate a detailed report within minutes. These tests can be performed using instruments such as the Anritsu MT1000A/MT1100A, which support TCP throughput tests in addition to RFC 2544 and Y.1564 for true analysis of network performance. These tests help improve the quality of expanding networks. ●

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Testing For NFC Interoperability In Automotive Applications

The automotive industry is increasingly using near-field communications. However, before market introduction, intensive testing is needed, and at an early development stage too.
By Dr. Michael Jahnich, Director for Contactless Test Solutions at Comprion

Near-field communication (NFC) is a mature technology – certainly in some applications, such as ticketing, identification (e-passports), access control and, nowadays, consumer electronics, where contactless payment schemes using NFC have become standard.

NFC in automotive applications, however, is an emerging market. Market penetration of NFC-enabled phones and service trends such as car sharing, corporate fleet management and the digitalisation of car rental services are the main drivers here.

Digital car keys will enable a lot of new services and innovations. It will be possible to share car keys with others on a temporary basis, send car keys to a smartphone and store them in a secure area such as the SIM or an embedded secure element (eSE). The mobile device will become the physical carrier of digital keys used for secure car access. In this scenario, NFC is the key for authentication.

Beside secure car access, there are other innovative uses, including:

- One-touch Bluetooth or Wi-Fi pairing to open car doors;
- Personalised car configuration;
- Infotainment system using smartphone for Internet access;
- Car diagnostics, reminders and warnings sent to the driver;

> *"In the automotive environment, performance testing, design validation and pre-conformance are crucial parts of design and quality assurance"*

- In-car payment of parking, tolls and drive-through.

The crucial part of all these cases is the user experience – these scenarios will fail if NFC doesn't work, immediately and conveniently. Thus, the interoperability of mobile NFC devices and NFC-enabled cars is one of the major challenges in this market.

Test Challenges For Automotive NFC

From a technical point of view, the car's NFC modules mainly work in reader/writer mode or in peer-to-peer mode (see 'NFC Basics' box at the end of this article), whereas the smartphone will operate in card emulation mode. Today, there are numerous tests for the reader/writer mode, from the physical layer to the application layer.

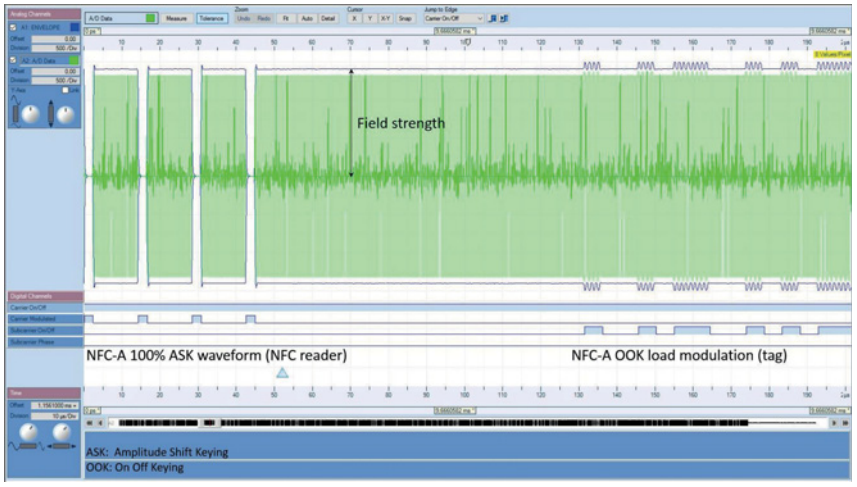
First, the NFC touch point of a car is not as well-defined as in other applications, such as mobile payment. There are many ways of touching a door handle with an NFC-enabled phone; the so-called operating volume must be robust enough to cover different use patterns.

Automotive NFC must work under severe operational environments like high or low temperatures and humidity. Different design parameters have an influence on NFC communication and the operating volume, such as materials, car lacquer finish and coil geometries.

Moreover, interference with other RF technologies may cause problems for the car's NFC connectivity; for example, wireless power-charging modules, Wi-Fi or Bluetooth.

Usually, the NFC stack's digital protocol is not affected by the integration; the module manufacturer might even have

Figure 1: RF characteristics type A



pre-certified the protocol stack. The analogue parameters vary during the integration of an NFC module into a car door or handle, dashboard or console, so for every design the integrating company must validate these parameters.

In the automotive environment, performance testing, design validation and pre-conformance are crucial parts of design and quality assurance. The integrated NFC module need not only be ready for certification but needs to provide a high level of interoperability with NFC-enabled smartphones.

NFC Conformance Requirements

The NFC Forum has defined electrical device requirements to characterise its magnetic field (downlink) and the reader's sensitivity to load modulation from the tag (uplink). These requirements comprise the following:

- Carrier frequency (MHz);
- Field strength (H/m);
- Waveforms characteristics (modulation depth, rise and fall times of the three NFC technologies, A, B and F);
- Load modulation sensitivity;
- Reset behaviour.

Conformance tests verify these characteristics in a predefined operating volume, for a minimum level of interoperability. It is rather coarse volume, with a total of only fifteen measurement points – assuming the NFC antennas are parallel to each other.

To certify an NFC module, it must pass successfully a subset of these measurement points. Passing conformance tests will thus be necessary for certification, but will not suffice for an acceptable level of interoperability. Better results can be achieved by completely characterising the reader's near-field.

For conformance testing, so-called reference PICCs (tags) are used. These reference PICCs influence the magnetic RF field and simulate tags with different load modulation and antenna geometries. However, conformance tests don't account for other electrical parameters, such as resonance frequency, quality factor and loading effect; conformance testing defines a minimum number of tag types with load modulation and different antenna classes to provide interoperability.

To assess the reader's real performance, it is advisable to supplement the conformance tests with additional tests, varying more tag parameters, thus simulating a variety of tags.

Figure 2: NFC Forum operating volume

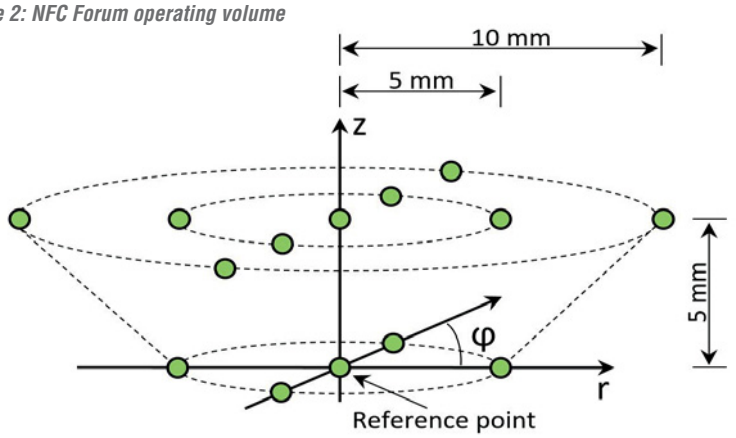


Figure 3: ISO calibration coil

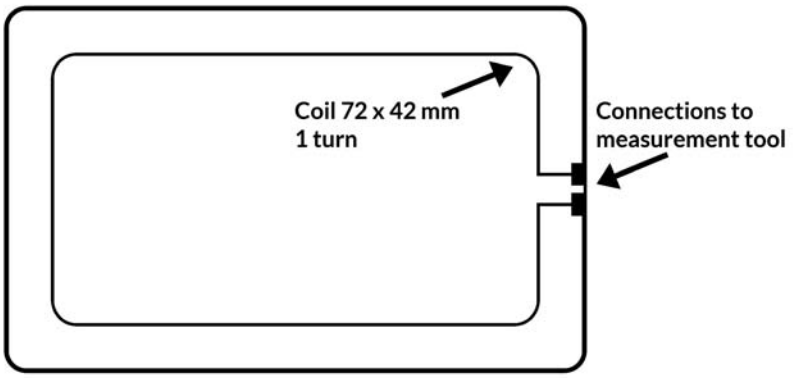
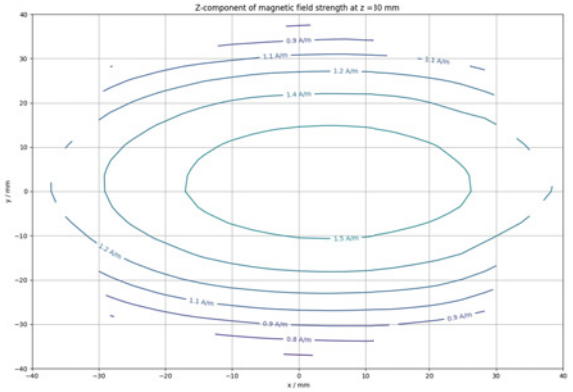


Figure 4: Z-component of magnetic field strength at z = 30mm



Describing The Near Field

The operating volume of an NFC reader is defined as the three-dimensional space in which an NFC device can exchange data with a tag or another NFC device. This space is represented by a set of n points pi (x, y, z), i = 1...n. Thus, most physical parameters of an NFC reader are a function of these spatial points.

For conformance testing, the operating volume is the minimum required space and is device-independent. Conformance tests are performed for each point pi, yielding a pass/fail result. The graphical visualisation of the results is called a shmoo plot. Today's conformance tests are limited to parallel coil scenarios, which is not always the case in real life.

For performance testing as part of design validation, one question is the actual operating volume of the NFC reader. Thus, the operating volume is the result or, rather than, the input to testing.

Moreover, it is possible analyse the near field as a vector field and to test scenarios in which readers and tag coils are positioned at certain angles to each other.

There are several approaches to characterise the reader's near-field. First, field strength is measured through the reference PICC that has a certain loading effect on the field. Here, field strength H is proportional to the rectified DC voltage induced in the reference PICC. Waveform parameters are measured on a separate coil that doesn't influence the reader's field.

Second, the ISO calibration coil can be used to measure field strength and waveform; it's rather neutral, having no significant loading effect on the near field.

Both, the reference PICC and the calibration coil have a big surface area, so these coils measure the integrated value of the flux density B through the coil area (the magnetic flux).

A third approach is to minimise the coil dimensions, which results in lower measured voltages but more precise measurements. These coils (<1cm in diameter) can be combined into one probe to measure all three components of the field strength vector at each spatial point.

A similar approach can be applied to characterise the NFC reader's reception performance or sensitivity. A shmoo plot can visualise at which spatial positions the communication between reader and simulated tag is successful. Moreover, it is possible to include the minimal load modulation amplitude needed for a successful communication as a function of the reference points.

Figure 4 shows the field strength of an NFC reader in z-direction measured by a reference PICC at position z = 30mm.

Overall, near-field characterisation as part of performance testing can generate valuable and extensive results for design validation and enhance conformance tests. It will help design a more robust product and thus increase interoperability to acceptable levels.

Test Tool Requirements

The performance tests described here were derived from the corresponding conformance tests, so a conformance test tool is fundamental to perform them. Moreover, the degree of automation and speed of instrumentation are important, since there are measurements at numerous positions. For example, only 20 measurements in each direction yield as many as 8,000 recorded results; for a vector field, 24,000.

Exact and flexible positioning is vital, too. The most flexible positioning system is a 6-axis industrial robot arm. ●

NFC BASICS

Near-field communication (NFC) is a standardised RF technology that enables two devices to exchange information over short ranges (<10cm) at a carrier frequency of 13.56MHz. It uses electromagnetic induction, where devices have loosely coupled coils to transmit both power and data. Inductive coupling allows one device, usually a passive tag or smart card, to be powered externally.

This wireless technology is based on ISO standards 14443 and 18092, which the NFC Forum (an industry consortium) adapted to create the NFC architecture – mainly for consumer electronics – that manufacturers implement in their NFC-compliant systems and devices.

The NFC Forum has defined three operation modes for NFC devices; see the figure below. The first mode is "reader/writer", in which a device emits a magnetic field, reads data from and writes data to a passive device such as a tag.

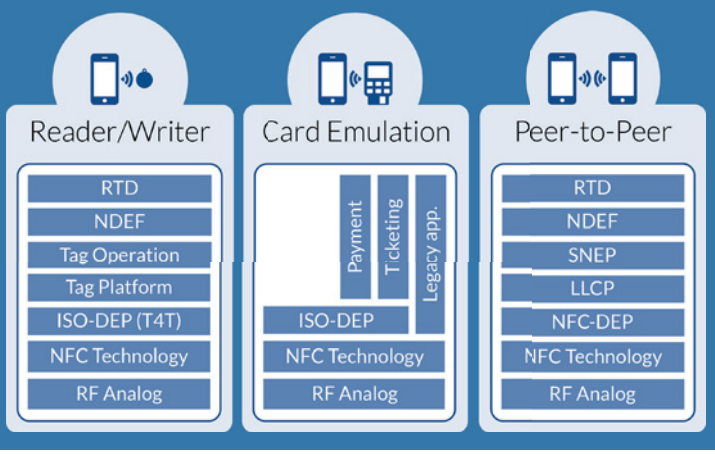
Second is the "peer-to-peer" mode which enables two peer devices to establish a point-to-point communication, for example an IP connection.

Third is the "card emulation" mode, which specifies the counterpart to the "reader/writer" mode. Here, devices simulate a passive tag or smart card.

NFC ARCHITECTURE

The RF analogue and digital protocol layers are the same for all three modes. The protocol layer comprises three modulation types, A, B and F, at a maximum data rate of 424kbit/s.

NFC is a certified technology. There are certification schemes for mobile payments provided by EMVCo, and for consumer devices as provided by the NFC Forum. Even for mobile phones, there are numerous test cases mandated by the Global Certification Forum to certify UICC-based NFC services.



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Powered by external 150W power supply with 90-264VAC input.

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Phase Stability Measurements In A Ranging-Tone System For Space Applications

By Francesco Spadafora, Application Engineer, and Giuseppe Savoia, Solution Architect, at Keysight Technologies

The world's first artificial satellite, known as Sputnik-I, was launched by the Soviet Union over 50 years ago, followed by the United States who launched Explorer-I in January 1958. These two great events opened a new era for practical use of the outer space.

Keeping the orbit control of a spacecraft or a satellite is fundamental, and all of associated technologies – hardware and software – must be highly reliable; failure can lead to unimaginable damage and financial loss.

The usual way to establish a satellite's orbit is based on measuring the distances between the satellite and the Earth station; normally determined by measuring the time needed for a radio signal to make a round trip. The system that performs this kind of measurement is known as "ranging tone system".

A classical radar is used to determine the range, but such a system requires high-powered pulse generators and a lot of dedicated equipment.

Ranging-tone systems take advantage of the existing communications equipment between a spacecraft and ground station by transmitting a range tone from the ground station to the satellite, and then re-transmitting the same signal back to the Earth station. A comparison circuit of the phases between the two signals provides the correct distance.

Ranging Tone Basics

Figure 1 shows a simplified block diagram of a ranging tone system.

A baseband source generates the CW tone, the modulator performs the up-conversion at a desired carrier frequency, then the signal is transmitted to the satellite through the antenna. The satellite transponder transmits the same signal to the Earth station, where down-conversion and phase comparison operations are performed between the transmitted (Tx) and received (Rx) signals. Usually all the processes are controlled by a host PC.

The phase shift between the Tx and Rx signal is directly proportional to the turnaround signal travel time and then to the distance between the Earth station and satellite.

The following equations show how the phase shift between the two tones is related to the distance between the satellite and the Earth station.

Considering a simplified approach, the complex Tx signal transmitted by the Earth stations can be expressed as:

$$Tx_{tone} = Ae^{jwt} = Ae^{j2\pi ft} \quad (1)$$

where A is the amplitude of the signal and f is the carrier frequency.

The corresponding received signal retransmitted by the satellite transponder can be expressed like an attenuated and phase-shifted copy of the Tx tone:

$$Rx_{tone} = ae^{j\omega(t-\tau)} = ae^{j\omega(t-\frac{2R}{c})} \quad (2)$$

In the phase term of Equation 2, the propagation delay τ is equal to 2R/c, where R is the distance between the antenna and the satellite and c is the speed of light [$3x10^8$m/s].

Calculating the range between the Earth station and satellite is performed by analysing the phase difference between the Tx and Rx signal:

$$\phi_{tx} - \phi_{rx} = \omega t - \omega\left(t - \frac{2R}{c}\right) = \frac{2R}{c} \quad (3)$$

In the ranging-tone system design, ±15m of accuracy in calculating the satellite distance is acceptable, which translates in ±100ns accuracy in the measurement of propagation delay τ.

In real terms, both signals are a bit different, for example in the Tx signal at least one additional phase term must be considered:

$$Tx_{tone} = e^{jwt+\phi} \quad (4)$$

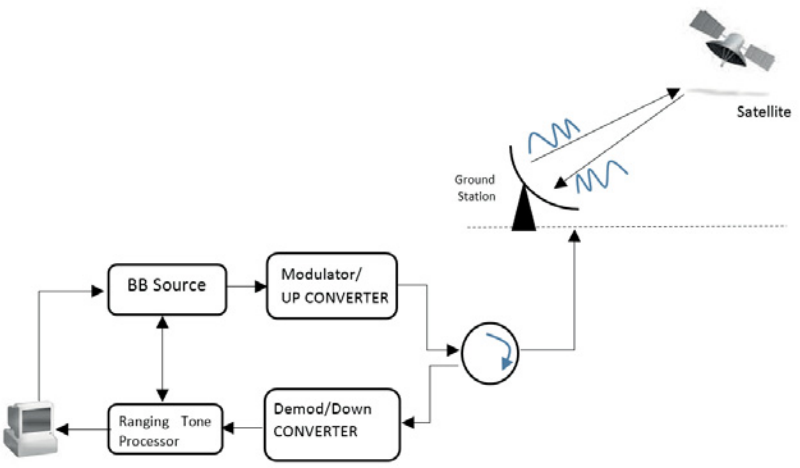


Figure 1: Ranging tone set-up

where Φ is transmitter-side phase fluctuations. This term can be introduced by several factors such as temperature, mixer instability and local oscillator inaccuracy, which all depend on time. Therefore, Φ can compromise the correct measurement of the satellite range.

Since this term will be also present in the phase of the Rx signal, the phase fluctuations at the output of the Tx must be limited as much as possible, to have a good detection of the satellite position; this means the phase must remain constant and negligible with respect to 2R/c.

Phase Stability Measurement

Here we'll describe step by step how to perform phase stability measurement in a Tx ranging-tone system; see its setup in Figure 2.

The measurement is performed at the output of the upconverter; the instrument used to accomplish this measurement is Keysight Technologies's new X series spectrum analyser N9040B with VSA 89601B software, used to perform demodulation and phase measurement and log.

The baseband source is used to generate the low-frequency baseband signal (i.e. CW signal). This signal is divided into two paths; the first is applied to the upconverter, and the second is used as a trigger on the N9040B on which are performed down-conversion and log of the phase over the time.

The phase stability term measured by the vector spectrum analyser is composed of two parameters. It is the sum of the phase stability at the output of the DUT and a phase error introduced by the instrument N9040B:

$$\Phi_{Measured} = \Phi_{DUT} + \Phi_{UXA} \qquad (5)$$

The phase term introduced by the spectrum analyser UXA N9040B must be stable over time and it at least one order of magnitude smaller than the Φ_{DUT}; meaning, it must be negligible. This can be established by doing a preliminary calibration of the system as shown in Figure 3.

During the calibration, the signal source MXG N5183B is used to generate the ranging tone with a phase modulation, and the internal low-frequency generator of the MXG is used to trigger the spectrum analyser.

A dedicated setup has been implemented on the VSA software to retrieve and log the ranging tone phase; see a screen shot in Figure 4.

As it can be seen in the phase-logging window, the calibration system's phase stability is plotted with 2mdeg/div on the Y scale and with a phase variation in the range of ± 20mdeg.

The operational frequency of a ranging tone is usually equal to 27kHz phase-modulated at the desired carrier frequency. The phase modulation is preferred as it is not sensitive to amplitude variation and it eliminates any frequency conversion issues.

To ensure a good detection of the satellite distance, the phase stability at the output of the antenna connector must be ±1deg, ensuring distance accuracy of ±15m. Taking into account Equation 5, the term Φ_{UXA} introduced by the spectrum analyser is negligible compared to the phase term of the DUT. This means the new UXA N9040B is well suited for this type of test.

The technique described here can easily be expanded to measure the phase stability response of the entire channel by sweeping the carrier frequency, including the Tx and Rx path. ●

Figure 2: Ranging tone set-up

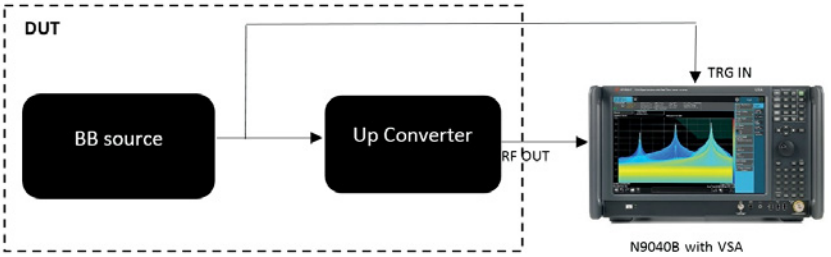


Figure 3: Ranging tone test-system calibration

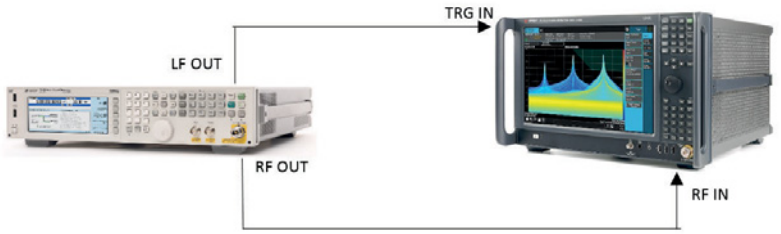


Figure 4: VSA 89601B test results

Manycore Processor Technologies And The Underlying Software Are Becoming Indispensable In T&M

By Neil Crossan, Field Marketing Engineer (Aero and Defence) and Adam Foster, Senior Product Marketing Manager for Automated Test, at National Instruments, and Shahram Mehraban, Director of Industrial and Energy Solutions at Intel

A common misconception about test systems is that the data they generate is purely pass/fail. This could not be further from the truth.

Traditional, fixed-functionality instruments may appear to simply send this information to a host PC, but inside their shells a lot of signal processing goes on before the pass/fail result is passed along. The processor inside them directly affects the measurement speed, especially true for applications where intense signal processing is needed to determine a result, like in RF, sound and vibration and waveform-based oscilloscopes.

For example, even the fastest FFT-based spectrum analysers today still spend only 20% of their measurement time acquiring a signal, with the remaining 80% spent on processing it by applying known algorithms. Applying this same theory to an instrument released five years ago, the time taken to process the signal is even worse.

Realistically, signal processing can end up taking up to 95% of the total measurement time. The easiest way would be to invest in a completely new instrumentation portfolio each year; however this is rarely an option, resulting in the use of antiquated test equipment to test modern, complex devices. Most test departments end up with a large performance gap between the processing power of their systems and their needs.

Modular Test Systems

Modular test systems feature three main and separate parts: controller, chassis and instrumentation. The controller contains the CPU and works like an industrial PC. The main benefit of this approach is the ability to replace the controller containing the CPU with the latest processing technology, while re-using the remaining components in the test system (chassis/backplane and instrumentation). For most uses, keeping the instrumentation and upgrading the processing power of the CPU extend the life of a modular test system well beyond that of a traditional instrument.

Both modular and traditional instruments rely on the same advancements in processor technology to increase test speed, but modular systems are more easily and cost-effectively upgradable than traditional instruments.

Processor Market Changes

In 2005, Intel released the first multicore processor, the Intel Pentium D. Accustomed to harnessing the power of ever-increasing processor speeds, software developers were forced to consider new parallel programming techniques to continue to reap the benefits of Moore's Law. As spelled out by Geoffrey Moore in his book *'Crossing the Chasm'*, technology adoption follows a bell curve with respect to time, and features five progressive participant states: innovators, early adopters, early majority, late majority and laggards. Certain industries, such as gaming and video rendering, were quick to adopt parallel programming techniques, while other industries have been slower to embrace them.

Unfortunately, automated test engineers fall into the late majority category when it comes to adopting parallel programming techniques. Perhaps the biggest reason for this is they had no incentive to re-do their software architectures for multicore processors. Until now, most automated test engineers have used technology such as Intel Turbo Boost to increase the speed of a single core on a quad-core processor and reduce the test times of sequential software architectures, but this technology has reached a plateau.

Many factors such as heat dissipation prevent processor speed from increasing at its previous, Moore's Law, rate. To keep power use down whilst boosting performance, Intel and other processor manufacturers are turning to manycore technology, as seen in the Intel Xeon processor with eight logical cores. The

Figure 1: Signal processing dominates the total time for CPU-hungry measurements

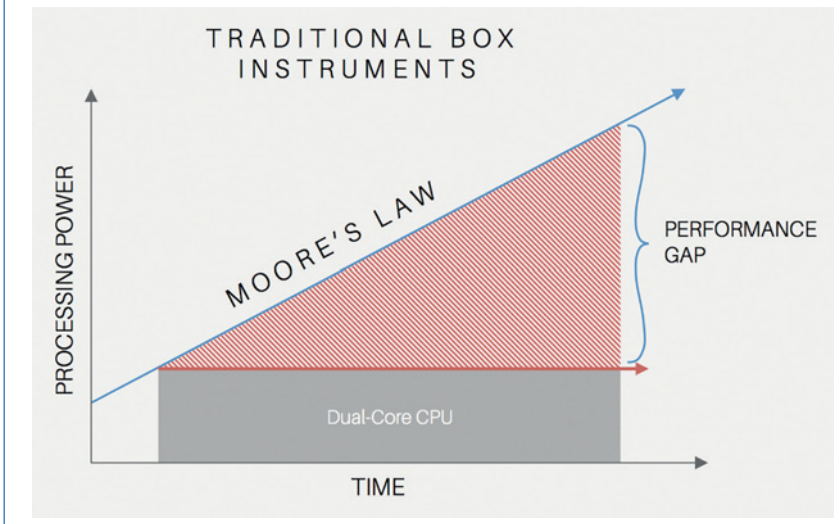


Figure 2: Traditional box instruments with fixed CPUs exhibit a costly performance gap over their lifetimes

result is a processor with clock speed like the previous processor but with a greater number of computational cores to crunch data.

Manycore Processor Applications

Certain test applications are prime candidates for manycore processors. In the McClean Report 2015, IC Insights researchers examine many aspects of the semiconductor market, including its economics. They state: "For some complex chips, test costs can be as high as half the total cost"; "Longer test times are driving up test times"; and "Parallel testing has been and continues to be a big cost-reduction driver".

In semiconductor test, operators use something called parallel test efficiency (PTE) to measure the test system's overhead. If the test software is written properly, increasing the available processing cores in a test system should positively affect the PTE for a given test routine. Alhough test managers must consider many factors such as floor space, optimal parts-per-hour throughput and capital expense when investing in automated test systems, an upgrade to the system's parallel-processing power typically has a positive impact on the business by improving the PTE.

Not Alone

The semiconductor industry is not alone in adopting parallel test – you'd be hard pressed to find a wireless test system that tests fewer than four devices at a time. Manycore processors are also targeted at any industry that must test the wireless connectivity or cellular communication protocols of a device. It is no secret that 5G is currently in its prototype stage, with technology that exceeds the bandwidth capabilities of current RF instrumentation.

In addition to processing all the data sent back from the high-bandwidth signal analyser for a single protocol, wireless test systems must test multiple protocols in parallel. For example, a smartphone manufacturer needs to test not only 5G when it is released, but also most of the previous cellular technologies, including Bluetooth, IEEE 802.11 and any other connectivity variants.

Each new communication protocol requires test algorithms that are more processor-thirsty than its predecessor. Just as manycore processors help increase

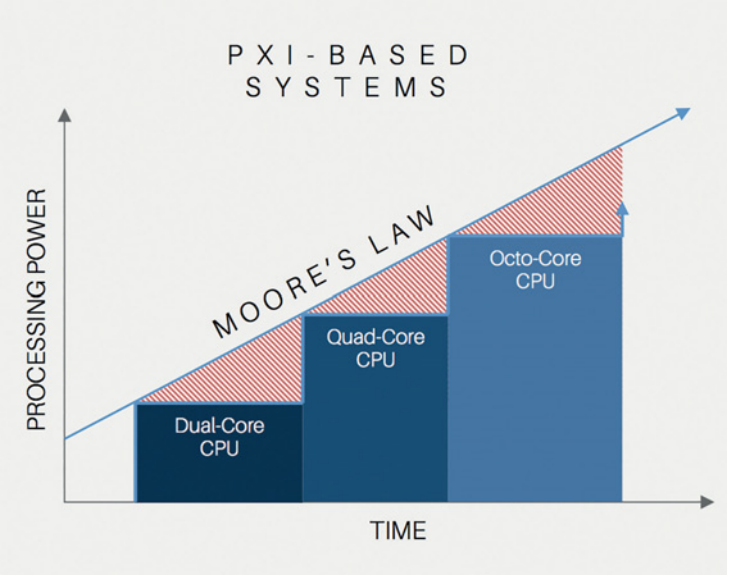
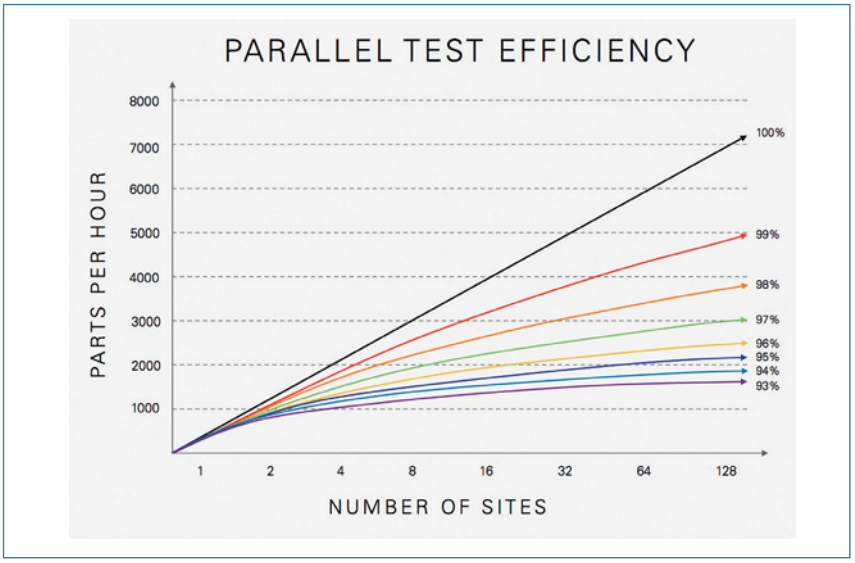


Figure 3: The CPU in a modular test system can be economically upgraded to increase processing performance

Figure 4: The relationship between parallel test efficiency, parts per hour and number of sites in a multisite semiconductor test system



the PTE of a semiconductor test system, increasing the ratio of processing cores to protocols and devices under test will reduce the test time further.

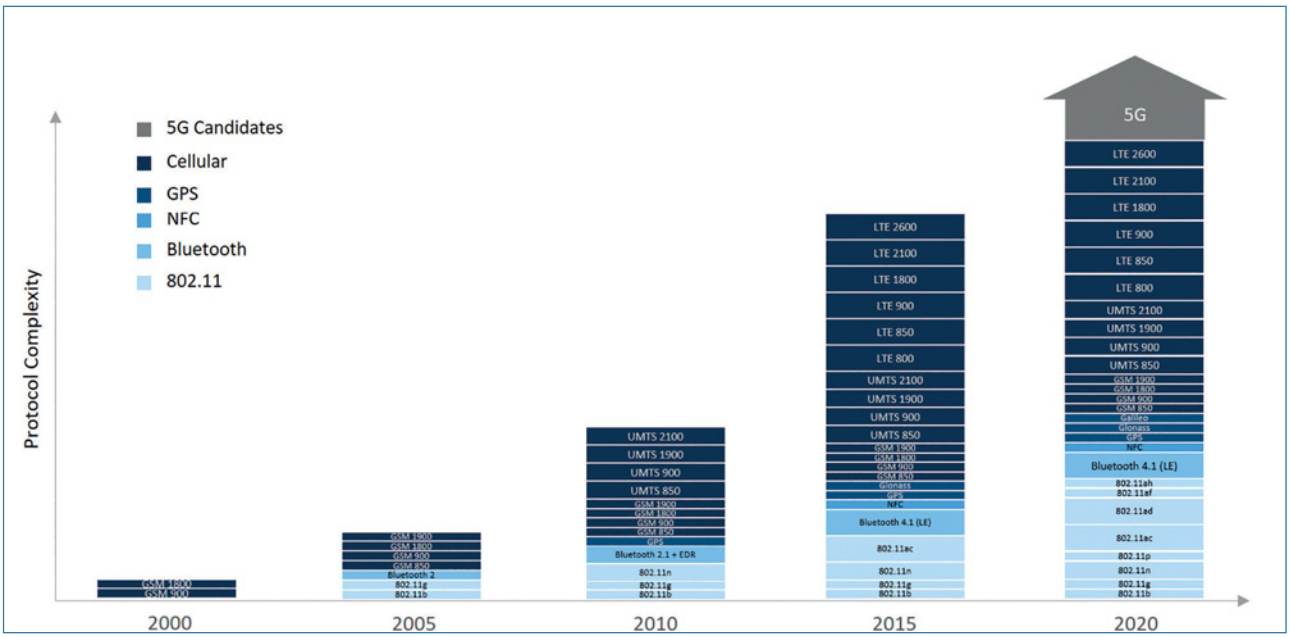
Application Software

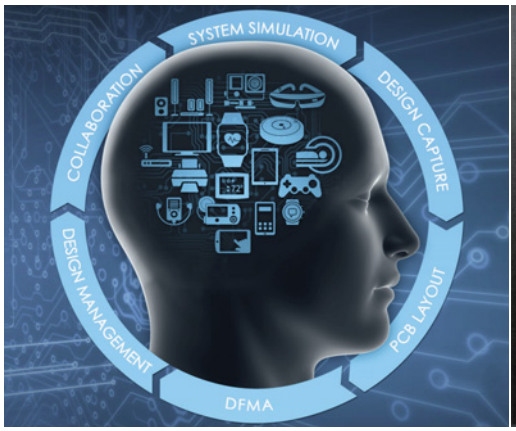
Software has evolved from a minor component to a leading role in test and measurement, and test engineers now face the daunting challenge of implementing parallel test software architectures. When using a general-purpose programming language such as C or C++, properly implementing parallel test techniques often requires many man-months of development. When time to market is a priority, test managers and engineers must emphasise developer productivity. Adopting application-specific test code development software (for example, NI LabVIEW) and test management software (for example, NI TestStand) moves the administrative work of parallel processing and thread-swapping from test departments to the software R&D staff of the commercial software company. Application-specific software enables test engineers to focus on the code that's critical to testing their devices.

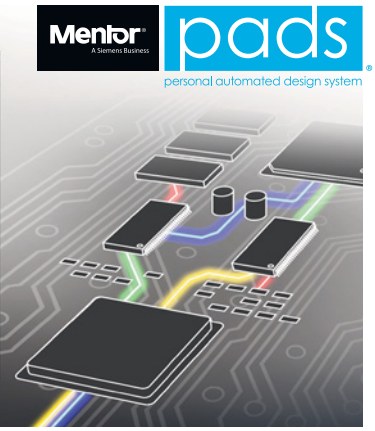
Preparing For The Future

Complexity has increased at an extraordinary pace over the past decade and it shows no signs of slowing down. The next generation of mobile communication should arrive in 2020. Gartner estimates that every household in most of the world will have more than 500 connected devices by 2022, and some sensors within these devices will most likely be smaller than the diameter of a human hair. Consumers expect high-quality products with an easy, seamless and rich user experience. This demand will require manufacturers to design and vigorously test their products to remain competitive. Test engineers will be called on to test these products and ensure that they function safely and reliably. If manufacturers hope to achieve economic benefit, they will need to adopt a modular, software-centric approach that enables parallel testing. Using manycore processing technology is no longer an option, it is now a requirement to stay economically viable. The only remaining question is how test departments will change their software approaches to take advantage of the additional processing cores. ●

Figure 5: Increasing signal processing complexity of wireless communication protocols over time







PADS® Strengthens DFT Capability with XJTAG® Boundary Scan Know-How

"Testing with Boundary can help boost test coverage, accelerate design verification and debugging, and increase production-test efficiency for Mentor, a Siemens Business. Mentor PADS users can now leverage XJTAG's experience to maximise the power of boundary scan in their designs without leaving their favourite environment, using the new, free XJTAG DFT Assistant for PADS."

Mentor PADS personal automated design solutions streamline product creation and help designers optimise all aspects of performance and manage their projects from design entry, through simulation and analysis, to sign-off for production. Optional extensions allow users to add capabilities such as advanced board layout, power-delivery analysis, thermal analysis, and support for RF design, high-speed design, and high-density or timing-critical routing.

PADS is now even more powerful with XJTAG's boundary scan test know-how built-in. "Boundary scan can add value from the beginning of the product lifecycle, and is becoming increasingly important to our customers," explains Jim Martens, Product Marketing Manager, PADS Solutions Group. "We saw the opportunity to enhance PADS with class-leading design for boundary scan test capability, by integrating the features of XJTAG's highly regarded DFT Assistant."

Boundary scan can check a high proportion of a board's connections early in the design phase, before any hardware is produced, and only requires the Test Access Port (TAP) pins of JTAG-compliant components to be correctly linked and routed to a connector. The simple four-signal interface allows easy software-based access to I/O pins that are otherwise hard to reach with probes, such as BGA I/O connections. The TAP, and traces comprising the scan chain that links the JTAG pins, occupy minimal real estate on the board.

When designing and prototyping boards, boundary scan tools help check for design errors before any hardware is built. First prototypes can be tested quickly to pinpoint connection errors, potentially saving hours buzzing out boards looking for shorts or opens that may cause errors or prevent the board starting up. In production, boundary scan can quickly check a high percentage of connections to help isolate defective boards and boost overall test efficiency.

Engineers can maximise the test coverage achievable with boundary scan by connecting JTAG compatible components into a JTAG chain. Using the JTAG chain, testing can be further extended to non JTAG compatible devices. PADS users can take advantage of XJTAG's Design-for-Test (DFT) know-how, acquired through years working with clients and refining the XJTAG test development suite, by using the XJTAG DFT Assistant for PADS now included in their favourite design environment.

XJTAG DFT Assistant for PADS features an Access Viewer that gives a graphical view of JTAG chain access across the board, which help users visualise the extent of test coverage and see how their design changes affect testability as the project progresses. In addition, the Chain Checker verifies that all the JTAG and TAP pins are correctly connected and terminated before committing to hardware. The information can be exported directly to the XJTAG test-development environment, where the testing to be carried out can be configured.

"Our customers can now use PADS to produce even better board designs that benefit from higher test coverage, faster debugging and prototyping, and more efficient testing in production. Working with XJTAG enabled us to achieve a high-quality result within a fast turnaround time," concludes Jim Martens.

opinion

Jim Martens
Product Marketing Manager
PADS Solutions Group

"Our customers can now use PADS to produce even better board designs that benefit from higher test coverage, faster debugging and prototyping, and more efficient testing in production. Working with XJTAG enabled us to achieve a high-quality result within a fast turnaround time."

"Boundary scan can add value from the beginning of the product lifecycle, and is becoming increasingly important to our customers. We saw the opportunity to enhance PADS with class leading design for boundary scan test, by integrating the features of XJTAG's highly regarded DFT Assistant."

Data Bank

Mentor® A Siemens Business

Company	Mentor Graphics Corporation A Siemens Business
Nature of business	World leader in electronic hardware and software design solutions providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor, and systems companies
Location	Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777
Web site	www.mentor.com

APACER ZOOMS IN ON NETWORKING AND TELECOMMUNICATIONS MARKET

Responding to key trends, such as cloud computing, IoT and big data, Apacer Technology has launched the DDR4 VLP Mini RDIMM memory module. Compliant with new-generation ATCA (Advanced Telecommunications Computing Architecture) specifications for telecommunications and communication equipment, the DDR4 VLP Mini RDIMM memory module is only 0.738in high. It is suitable for space-constrained 1U rack systems, blade servers and embedded systems, effectively improving heat dissipation, and improving system stability and reliability.

The module is JEDEC-compliant and is available in 4GB and 8GB capacities; its 1.2V ultra-low operating voltage offers up to 30% more power saving. The DDR4 also supports deep power-down mode, reducing close to 50% standby power consumption. Its power efficiency is particularly significant in satisfying the requirement for low power consumption in industrial, embedded, networking and server systems.

www.apacer.com

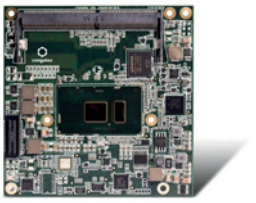
NEW COM EXPRESS MODULES BASED ON GEN 7 INTEL CORE PROCESSORS

Congatec has released new Computer-on-Modules (COM) Express Compact modules alongside the launch of the 7th generation of Intel Core SoC processors, codename Kaby Lake. The new conga TC175 COMs include features such as greater CPU performance, more dynamic HDR graphics thanks to 10-bit video codec, and support of the optional, super-fast 3D Xpoint-based Intel Optane memory.

Thanks to its compatibility with the previous generation, the widely-improved microarchitecture can be integrated in existing embedded systems without additional design effort.

The new modules are equipped with 15W dual-core variants of Gen 7 Intel Core SoC processors; specifically, these are the 2.8GHz Intel Core i7 7600U, the 2.6GHz Intel Core i5 7300U and the 2.4GHz Intel Core i3 7100U processors as well as the Intel Celeron 3695U processor with 2.2GHz.

www.congatec.com



APACER DEBUTS NEW HIGH-ENDURANCE MICROSDHC/XC MEMORY CARD

With expanding applications of security surveillance systems, Apacer Technology has launched the new industrial-grade microSDHC/XC memory cards, custom-built for video-monitoring equipment to endure long hours of continuous data writing. The cards are available in capacities from 4GB to 128GB, and their ultra-high-speed class 3 specification also supports smooth full-HD, 3D and 4K video recording, which is particularly significant in video-monitoring applications that need continuous recording and sustain high wear rate. Their durability, endurance and performance make them suitable for surveillance video recorders, dashcams for fleet vehicles and government use, and webcams.

When using the 128GB ultra-high-capacity microSDXC memory card to record full-HD in 20FPS, it can record for up to 20,000 hours; in loop recording, it can store 32 hours of video footage with automatic write-over.

www.apacer.com

NEW FAMILY OF LOW-VOLTAGE PRECISION HALL-EFFECT LATCH ICS

Allegro MicroSystems Europe has announced a low-voltage family of AEC-Q100-qualified three-wire Hall-effect latches.

The APS12205, APS12215 and APS12235 are produced on the Allegro advanced BiCMOS wafer fabrication process, which implements a patented high-frequency chopper stabilisation technique, which achieves magnetic stability over the full operating temperature range and eliminates offsets inherent in devices with a single Hall element that are exposed to harsh environments.

The new family is ideal for systems where the sensor ICs will be behind a voltage regulator or that do not require double battery or reverse battery protection.

The APS122x5 family was optimised for the speed and position sensing of motors/encoders, and is targeted at 2.8-5.5V automotive and industrial markets.

www.allegromicro.com

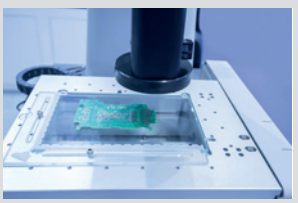
MACHINE VISION IS A CRUCIAL TECHNOLOGY FOR INDUSTRY 4.0

Machine vision is an image-processing technology that enables automated object scanning. Plant operators can mount cameras on production lines or cells for real-time process control, product inspection and sorting and robot guidance.

The technology enables robots to interpret their visual surroundings, which can allow them to move around independently. Visual information can be used to recognise the environment and make decisions that are not directly programmed.

Machine vision is central to the idea of the smart factory, which is based upon a self-organised system comprising a communicating network and an intelligent exchange of information. Acting as the eyes of the factory, image-processing systems based on industrial cameras can compute information that was previously done by manual testing. This reduces human error and enables robots to react flexibly to information for production control.

www.euautomation.com



KYOCERA ANNOUNCES NEW INNOVATIONS

Kyocera has recently developed a high-thermal-conductivity epoxy moulding compound with a thermal conductivity of 6W/mK. This is a significant increase in the conventional thermal conductivity of 0.9-3W/mK and thus enhances the protection of semiconductor components from light, temperature, humidity, dust and physical shock.

In addition, the company launches an innovative environmentally-friendly silver sintering paste in Europe – a high-performance proprietary formulation. Kyocera's lead-free pressureless silver sintering paste exhibits excellent thermal and electrical performance as well as an extremely strong adhesion to bare copper.

Another ground-breaking innovation of the Japanese technology company is its new Torokeru Sheet. With curing temperatures of 100-120°C and a curing time of 30-120 minutes, the innovative sheets will reinforce and protect mounted parts from environmental stress in power semiconductor packages, passive components and general parts.

www.kyocera.co.uk

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