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THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

SPECIAL REPORT – MOBILE COMMUNICATIONS:
- Basestation design
- RF design
- Network design

24-Bit Sensor High Precision Acquisition Modules

from Teledyne LeCroy

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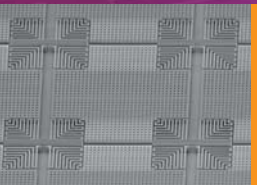

Trend
Solving stiction in MEMS inertial sensors

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CMOS clocks: the basics, uses and best applications

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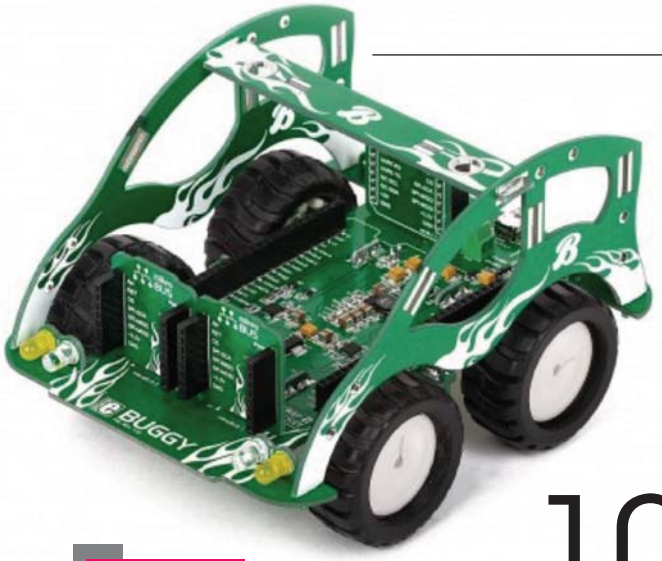

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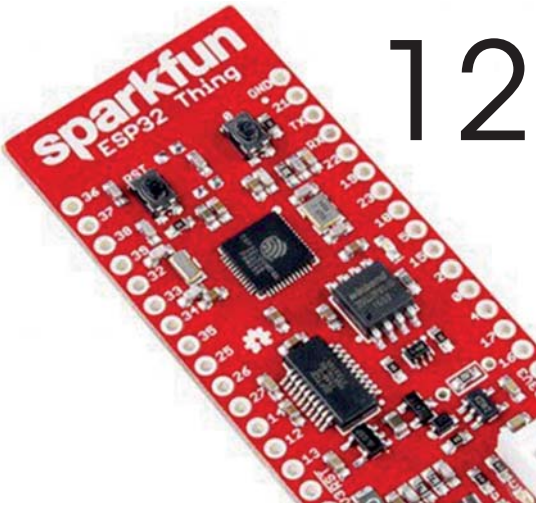

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PIC18F "K42" Family

MCUs For Every Space

The PIC18F "K42" family features the highest integration of Core Independent Peripherals (CIPs), high-resolution analog, Direct Memory Access (DMA) and vectored interrupts for fast processing. CIPs allow many functional tasks to be done in hardware—reducing code, validation time, core overhead and power consumption.

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BREAKING THE GLASS CEILING OF DISPLAY INNOVATION

> Clearly, e-paper displays aren't the right solution for every situation, but the trend points to a very bright future for EPDs

Glass displays have become ubiquitous – being so cheap and abundant has made them the default option for product displays. However, electronics engineers and product designers are beginning to realise the limitations of glass and the shackles it places on product innovation.

Weight, power, ruggedness, flexibility and visibility are very important factors for customers, and glass displays often fall short. Emerging technologies such as wearables, the Internet of Things and augmented reality are also creating demand for new type displays that can curve, bend and flex in ways that glass can't, at least not very easily.

Similarly, designers behind established terminals, devices and gadgets are always on the lookout for ways to improve each subsequent generation of their products and at the same time be different in highly competitive markets.

This backdrop has given rise to alternative display technologies, one of which is glass-free electrophoretic displays (EPDs), more commonly known as e-paper. Allied Market Research recently forecast that the annual global e-paper display market will grow to $4.2bn in 2022, from $490m in 2015.

EPD technology has been in development for over fifteen years, but it has had something of a chequered past. With the initial hype, experimentation and learning from failures now complete, the industry entered 2017 with a strong, more mature and serious focus on growth and clear applications where e-paper is better than glass. These applications include:

● Smartcards

Integrating e-paper displays into multi-function credit and bank cards offers major benefits in terms of flexibility and improved security. Re-writable e-paper technology can also be used to create smart labels for warehouses or logistic businesses as a quick and easy way to track merchandise.

● Wearables

E-paper is already widely used in the wearables industry – from smart jewellery and watches to backpacks and hats. The flexibility, low power, ruggedness and innovative potential offered by plastic display technology can elevate simple wearable products into ground-breaking, fashionable and aspirational ones that enable individuals to customise and express their personality.

● Portable Devices

In the portable-device space, e-paper can be an effective remedy to many of the frustrations users have with their devices when accessing information on the move – such as reading in bright sunlight, coping with low battery through prolonged use and the fragility of the screen if dropped.

● Digital Signage

From shelf-edge labels, smart meters and security tags to wayfinding, transportation and retail, digital signage applications all require a robust display that is legible and always on. E-paper displays tick all these boxes as a superior alternative to LED, OLED and LCD options. They are also thinner and lighter per square inch, whilst remaining extremely robust and shatterproof.

The bi-stable nature of e-paper displays (i.e., energy is only required when updating the display) is a particular power advantage, since maintaining an always-on screen can be extremely energy-intensive. Dresden Elektronik's deZign e-paper transport timetables are a good example of e-paper displays in outdoor signage where their low power, weather- and vandal-proof, and low-maintenance functionality are superior to traditional electronic glass displays.

E-paper displays also crop up in a range of unexpected places. The engineers at Land Rover BAR recently used EPDs for data displays on Ben Ainslie's latest America's Cup boat. In this environment e-paper displays' daylight readability is a key advantage over more conventional marine LCD or LED displays that rely on backlighting to make the display visible in bright sunlight. The e-paper was completely configurable by the team's software engineers.

Will The Market For Glass Displays Shatter?

Not quite. Clearly, e-paper displays aren't the right solution for every situation, and glass will retain a large fragment of the display market for many years to come, but the trend points to a very bright future for EPDs.

For the right application, e-paper displays have a very powerful business case, and this article merely scratches the surface of its limitless possibilities. ●

By Tim Burne, CEO, Plastic Logic (www.plasticlogic.com)

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WEARABLE ELECTRONICS MAY BENEFIT FROM COLOUR-SHIFTING ELECTRONIC SKIN

Electronic skin promises to change colour

Chinese researchers have developed a user-interactive electronic skin that changes colour, promising to transform applications such as wearables, prosthetics and robotics.

Scientists from Tsinghua University in Beijing used flexible electronics made from graphene in the form of a highly-sensitive resistive strain sensor, and combined it with a stretchable organic electrochromic device, or ECD.

"We designed a modulus-gradient structure to use graphene as both the highly-sensitive strain-sensing element and the insensitive stretchable electrode of the ECD layer," said team lead Dr Tingting Yang. "We found that a strain of up to 10% was enough to cause an obvious colour change, and the red-green-blue value of the colour quantified the magnitude of the applied strain."

"It's important to note that the capability we found for interactive colour changes with such a small strain range has been rarely reported before. This user-interactive e-skin is promising for applications in wearable devices, robots and prosthetics in the future," he added.

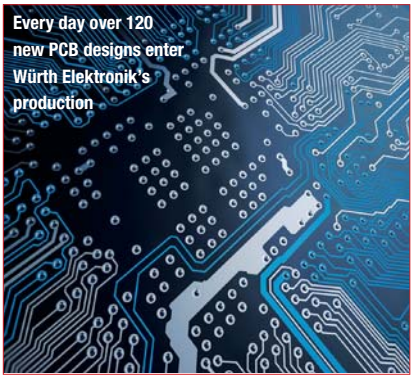
Skin colour changes are widespread in the animal kingdom, where animals such as chameleons, octopus and squid use it for camouflage, temperature control or communication. While science has been able to replicate these abilities with artificial skin, the colour changes are often only visible to the naked eye when the material is put under huge mechanical strain. Now graphene promises to improve this, with characteristics of high transparency, rapid carrier transport, flexibility and large specific surface area. As such it can be used in flexible electronics including stretchable electrodes, supercapacitor, sensors and optical devices.

COMPANIES JOIN FORCES TO EVOLVE PRINTED CIRCUIT BOARDS

German circuit-board manufacturers Würth Elektronik and FELA, both based in Baden-Württemberg, embarked on a partnership to improve circuit board technology.

Advancements in assembly and 3D-printed solder masks promise miniaturisation and a technological leap in circuit board manufacture. The two firms will pool their resources and expertise and share their findings to move the PCB industry forward.

"The partnership with FELA is based on both companies' passion for innovation, strategically using future-forward technologies," said Andreas Gimmer, managing director of Würth Elektronik.



Every day over 120 new PCB designs enter Würth Elektronik's production

NANUSENS SOLVES THE PROBLEM OF STICTION IN MEMS INERTIAL SENSORS

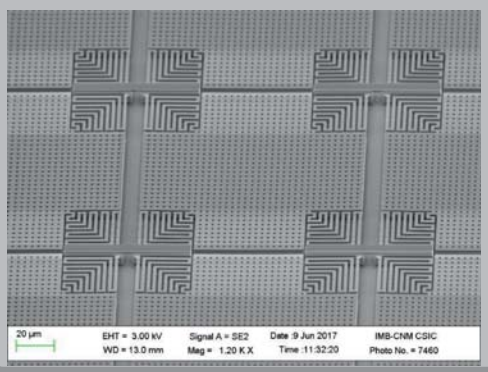
Barcelona start-up Nanusens claims to have solved the problem of stiction in micro-electromechanical systems (MEMS) inertial sensors. Stiction in MEMS is caused by microscopic-level Van der Waals and Casimir attractive forces, a major source of failure in these sensors. Nanusens's solution is to use CMOS nano-sensor technology, which shows great resistance to stiction.

In a typical inertial sensor, there is a proof mass connected to a spring, which moves under acceleration. The movement is detected by the mass acting as electrode, and the change in capacitance is measured relative to a fixed electrode. However, if there's large movement, such as from a shock or collision, the mass goes beyond the normal range of travel and touches a surface enclosing the sensor, where it 'sticks' due to attractive forces, and stops working. Stronger springs have been used to address the problem but this reduces sensor sensitivity. Sensitivity can be increased with a bigger mass but this adds to the surface area and, hence, to the attractive forces.

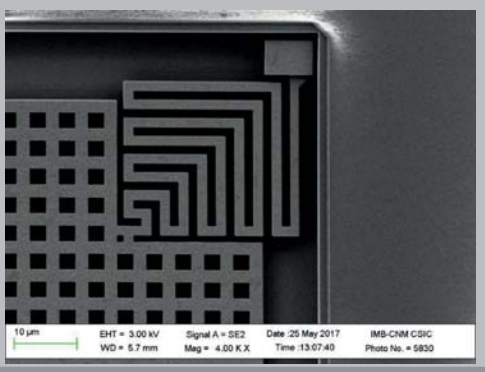
Nanusens reduced the sensor design in size, from 1-2um to 0.3um, which effectively reduced the attractive forces by almost two orders of magnitude.

"Our first silicon nano-sensor samples exceeded our expectations, showing outstanding resilience to stiction, with the devices going through more than 10,000 switching cycles, each equivalent to more than 1000G shock," said Nanusens CEO, Josep Montanyà i Silvestre. "The sensitivity is an order of magnitude above what's needed for a motion sensor in most applications."

The new nano-sensors are made using standard CMOS processes and mask techniques, and the sensors can directly be integrated with active circuitry, which helps deliver high yields, like with CMOS devices.



Nanusens NEMS motion sensor



A close-up of the spring

TELEDYNE LECROY LAUNCHES 24-BIT SENSOR HIGH PRECISION ACQUISITION MODULES

The SAM40 provides up to 24 input channels for low frequency (sensor signal) acquisition and analysis. It connects to a 4 or 8 channel Teledyne LeCroy 12-bit resolution high definition oscilloscope (Teledyne LeCroy HD4096 HDOs and MDAs) to provide Analog + Digital + Sensor (up to 8+16+24 channel) acquisitions. This capability is ideal for system debug and analysis of deeply embedded, electromechanical, and mechatronic designs in the medical, mil/aero, motors and drives, power, appliance, Internet of Things (IoT), vehicle/automotive and other applications.

24-bit High Precision

All channels have 24-bit resolution (stored in 32-bit floating point format) with ~0.05% total accuracy. Built-in filters with settings as low as 100 Hz further reduce noise. Adjustable gain ranges (1 mV to 10 V/div) accurately acquire a wide range of signal levels.

Plug-and-play

The SAM40 simply connects to the supported Teledyne LeCroy oscilloscope with a USB2.0 cable for data transfer and control/trigger commands, and BNC cables for clock/timebase synchronization. No programming or complex setups are required.

Unit Conversion and Rescaling

More than 65 different SI and English system physical units are supported for length, mass, temperature, angle, velocity, acceleration, volume, force/ weight, pressure, electrical, magnetic, energy and rotating machine quantities. Math and measurements applied to rescaled waveforms correctly read and convert to new units as required.

Deep Toolbox

The oscilloscope math, measure, analysis, pass/fail and option packages utilize the sensor inputs the same as any other channel. Teledyne LeCroy's deep toolbox just got even more powerful. High Definition Oscilloscopes have the greatest breadth and depth of tools, ensuring quick resolution of the most complicated debug tasks. Our Periodic Table of Oscilloscope Tools provides a framework to understand the toolsets that Teledyne LeCroy has created and deployed in our oscilloscopes

Sensor Signal and High Bandwidth Acquisitions

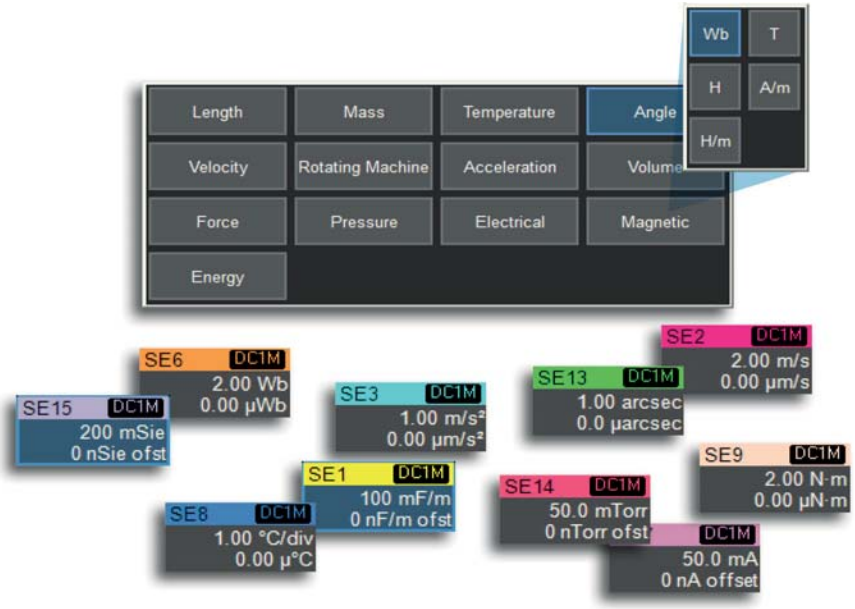
The SAM40 sensor acquisition module simply and quickly interfaces to a supported Teledyne LeCroy 12-bit high definition oscilloscope (HDO). The SAM40 acquires very low speed (40 kHz bandwidth) sensor and other signals and the HDO acquires higher speed analog, digital and serial data signals. The HDO cross-triggers the SAM40, and the SAM40 sends acquisition data to the HDO for time-synchronized display with the high bandwidth HDO analog and digital channels.

More Than 65 Different Supported Unit Conversion

Leverage your SAM40 24-bit acquisition system with the unit conversion and rescaling capability. Teledyne LeCroy's unit conversion package provides the most intuitive display of sensor, mechatronic and electromechanical data. Each sensor channel input has a unique rescaling setup directly in the setup dialog with y=mx+b rescaling capability and selection of physical units. All unit conversions carry through logically when unitized sensor inputs are used in math or measurements.

Up to 8 Analog + 16 Digital + 24 Sensor Channels

Engineers commonly use multiple instruments to debug and validate complex deeply embedded control systems, mechatronics, and electro-mechanical systems. Multiple instruments report different information on different displays and in different formats. An HDO with a sensor acquisition module cost-effectively replaces multiple instruments with one consolidated view of system performance. Leverage the Teledyne LeCroy deep toolbox to perform math, measurements, pass/fail and other analysis on all acquired data, or apply an application package to gain even faster time to insight.



4 + 16 (Analog + Digital) Channel Oscilloscope with SAM40-8 Sensor Acquisition Modul

The most basic system available combines a 350 MHz, 500 MHz, or 1 GHz 12-bit resolution, 4 channel oscilloscope (HDO4000A or HDO6000A Series) with a SAM40-8 eight channel acquisition module. This triples the number of available inputs for a very modest price, and preserves high bandwidth oscilloscope inputs for the most important uses, or provides capability to view more high bandwidth signals than would have previously been possible without the SAM40. 16 and 24 channel acquisition modules may also be used. MSO oscilloscope models further add 16 digital logic input channels.

8 + 16 (Analog + Digital) Channel Oscilloscope or Motor Drive Analyzer with a SAM40-24 Sensor Acquisition Module

Pair the SAM40-24 with the world's only 8 channel, 1 GHz, 12-bit resolution oscilloscope and obtain an unbelievable 8+16+24 analog+digital+sensor inputs. Make fast debug work of deeply embedded systems that combine power electronics, motors, and sensors into one complex, dynamic system. Utilize the SAM40 for analog speed or torque sensor signals, vibration sensors or accelerometers, and other mechatronic signals. For the ultimate in motor drive analysis, pair the SAM40 with the MDA800A and gain the deepest static and dynamic understanding of tree-phase power system and mechanical motor behaviors.

Visit **teledynelecroy.com** for details

HDO Oscilloscopes - Debug in High Definition up to 4 GHz

High Defi nition Oscilloscopes with HD Technology have a variety of benefi ts that allow the user to debug with unsurpassed precision. Waveforms displayed by High Defi nition Oscilloscopes are cleaner and crisper. More signal details can be seen and measured; these measurements are made with unmatched precision resulting in better test results and shorter debug time. Visit http://teledynelecroy.com/hdo/ for details:

	HDO4000A	HDO6000A	HDO8000A	HDO9000
HD Technology	HD4096 12-Bits	HD4096 12-Bits	HD4096 12-Bits	HD1024 10-Bits
Bandwidth	200 MHz – 1 GHz	350 MHz – 1 GHz	350 MHz – 1 GHz	1 GHz – 4 GHz
Input Channels	2, 4	4	8	4
Sample Rate	10 GS/s	10 GS/s	10 GS/s	40 GS/s
Analysis Capability	Basic	Advanced	Advanced	Exceptional

Notes from a Croatian island

BY **LUCIO DI JASIO**, MCU8 BUSINESS DEVELOPMENT MANAGER AT MICROCHIP TECHNOLOGY

If you haven't taken your holiday yet, look away now, since I am writing this column from a gorgeous little island on the sunny coast of Croatia, under the cool shade of an umbrella, by a sparkling pool, cold drink in hand. I am recovering from two weeks in Arizona during which I attended the 2017 Microchip Masters event and spent some time at the HQ.

It's a tough life, I know!

Masters 2017

If you don't already know, the Microchip Masters Conference is a huge training event in August, in Scottsdale, Arizona, running for the last 21 years. Over 80 technical classes are presented each year, large number of which are hands-on.

Figure 1: MikroElektronika Buggy

> "The number of architectures started multiplying, growing in complexity to the point that the class had to be split

This is not a corporate event; it is only engineers – real experts – who are allowed to present. Unfortunately, this applied to me too, since I moved to the 'dark side' (marketing) a few years ago – even though I am still occasionally tolerated as a class facilitator. I am, however, 'allowed' to present at the European Masters, a spin-off event that's only a few years old, in Berlin, hosted by the HTW (Berlin's historical technical university).

This year I got a ticket to Arizona because I'd been asked to present two classes in Berlin based on the original Masters classes: "What's new" and "Architecture selection".

The "What's new" used to be a short but very popular class, presenting new microcontroller models introduced over the year. In the beginning, when Microchip was only making two things – PIC (8-bit) microcontrollers and serial EEPROMs – this was easy. But then things became more difficult, since the pace of new product introductions grew frantically. The number of architectures started multiplying (dsPIC, PIC24, PIC32...), growing in complexity to the point that the class had to be split; after all, we also needed to discuss all those new analogue and connectivity products launched each year. This year, there were five different "What's new" classes in total. Enough said!

In my second "Architecture selection" class, I discuss the vastly expanded portfolio of the newly-introduced microcontroller architectures (following the Atmel acquisition), with AVR and the many Cortex M/A additions.

Castaway

Beyond the training though, with 600-plus attendees, Masters is a huge networking event and one I always truly enjoy, since I meet and keep in touch with many smart people.

Figure 2: PIC18F25K42, vectored interrupts and DMA

Now, after all the excitement, I am taking a few quiet days off to enjoy the Adriatic coast. As I am writing this, my thoughts go to an old ad in the Doctor's Dobbs Journal some time ago. Picture a tiny island, so small there's room for a single palm tree and a man; castaway but with a laptop(!?). He's in the shade, with feet touching the water and, although the sea level is rising, he appears content. You can't help wonder why.

That made me think: what software would you take if stuck alone on an island with a laptop? I'm quite sure my son would choose Minecraft, which is somewhat recursive and ironic, since the game is about being stranded in a semi-deserted world and surviving. There are monsters – and bizarre ones, too – but you can also choose to be completely 'creative' and ignore all the hardship of the "real" world and just start digging and building.

As for me, an engineer, if I'm to settle on a futuristic solution, it'll be a next-generation waterproof MacBook with an integrated solar-panel charger (try patenting that, Apple!). My obsessed mind will then be able to relax, and I can start dreaming.

Things To Do With (Un)Limited Time

To be happy on that island I would need a few simple things; here's my shortlist:

- A Mikroe Buggy (Figure 1) (https://learn.mikroe.com/development-platform-with-wheels/), which would give me five mikroBUS slots (if you read my previous columns, you'll know my obsession with these). Thanks to MPLAB Code Configurator (MCC) I will be able to customise efficient drivers for the five Click boards in no time; but then, with the amount of time only a castaway has on his hands, I'll focus 100% on that self-driving algorithm I've been dreaming about.
- A PIC18F25K42 so I can put to good use the brand-new vectored interrupts and PIC18 DMA. I will start writing the code in C for now, but with all that time on my hands, I might be able to design that next, ideal programming language I have been thinking about. Although it seems impossible now, I'd like to believe that in a few years we'll be looking back on C and wonder at the speed with which we transitioned over to the "new" language. Just like the transition from assembly to C in what seemed a blink of an eye, after being stuck for so many years.
- An iPad and a copy of Pythonista (https://itunes.apple.com/us/app/pythonista-3/id1085978097?mt=8), because life is too short to become a full-stack embedded developer, which means not only becoming a proficient embedded programmer of the Buggy, but also a Swift programmer who can quickly create an iOS interface and connect an iPad to the Buggy via BLE. Pythonista can get me there fast; in fact, writing iOS apps is so easy in Python (see Listing 1) that it takes an hour maximum (if you're new to BLE).
- GitHub (https://github.com), which, of course, means I need an Internet connection. I know that sounds like cheating – with an Internet connection, what kind of a castaway would I be? But instead of using it for help, I'll get to my repositories on GitHub (https://github.com/luciodj/In10LinesOfCode)! I find it quite surprising how few embedded programmers know of and use Git (and GitHub). It's a real life-saver!
- Flask, an HTTP server library for Python. Since I'll have an Internet connection, I might as well create an IoT dashboard to allow others to control my Buggy remotely. There's a plan I will also share the data produced by those five Click sensor boards. Driving the Buggy around a tiny island might be a little boring and pointless, but I am told that IoT applications are all the rage among trendy castaways.

Back To Reality

Perhaps it was just the effects of the last Mojito, but as I look over my list, I am just realising now that it won't take a lifetime to turn any of those ideas into reality – except for that next-generation programming language. In fact, I did get free access to the Internet (broadband) even on this beautiful Croatian island, so I might be able to get it all done in just a few hours. That is, of course, only if I can prise the iPad away from my son's hands! ●

```
class BLEManager (object):
def __init__(self):
self.peripheral = None
self.buffer = ''

def did_discover_peripheral(self, p):

def did_discover_services(self, p, error):

def did_discover_characteristics(self, s, error):
```

Listing 1 – Creating an iPad BLE connection with Pythonista

The ESP32 processor in embedded applications

BY **DR DOGAN IBRAHIM**, PROFESSOR AT NEAR EAST UNIVERSITY, CYPRUS

As the demand for Internet of Things and intelligent automation systems increases, semiconductor companies create ever-more complex microcontrollers. High processing power, coupled with various communication options and interface modules – all incorporated onto a single chip – seem to be the way the next generation of microchip technology is going.

Many manufacturers now offer small development modules with their complex microcontrollers on board. Some examples include the recently-developed Raspberry Pi Zero W, a very small board with a powerful microcontroller, which communicates via Wi-Fi and Bluetooth. Additionally, this module incorporates a GPIO with its many digital inputs and outputs, I2C, SPI, UART and camera interfaces, plus the Linux operating system, on a micro-SD card with a large on-board memory. The module can be programmed with the state-of-the-art Python language, supporting many mathematical, graphics and input-output libraries.

The user can start developing an application very quickly and without having to solder any components or buy applications development software. In addition, there are hundreds of projects, tutorials, application notes and books on the Internet to reference whilst developing an application.

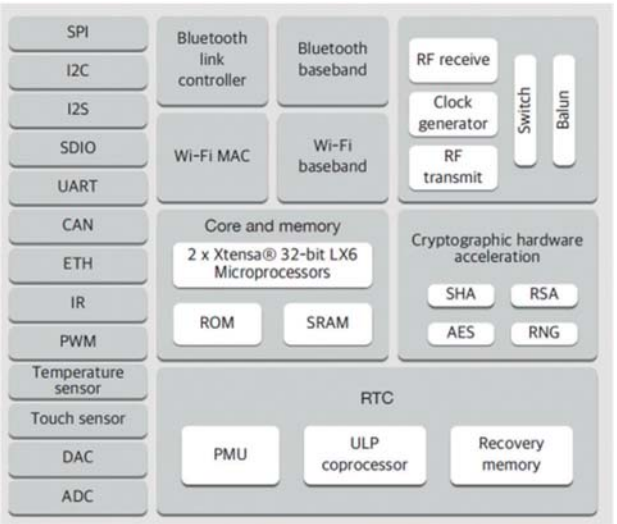


Figure 1: Internal structure of the ESP32 chip

The ESP32 Processor

Another complex processor is the ESP32, manufactured by the Shanghai-based manufacturer Espressif Systems. This is the big brother of the ESP8266 processor I wrote about in the last issue of Electronics World, which provides Wi-Fi capability but no Bluetooth. In addition, the ESP32 is a dual-core processor with much higher throughput than the ESP8266.

ESP32 is a very affordable, general-purpose microcontroller, costing around £10, and incorporating on-chip communication technologies such as Wi-Fi and Bluetooth, GPIO with the usual many digital and analogue ports, I2C, SPI and UART interfaces, and memory. For advanced applications requiring access to the chip's internals, the processor can be programmed using the highly-popular Arduino IDE or its native development framework.

In this article we'll discuss the ESP32 processor and give an example of its use in a typical mobile-phone-based remote-control application using the Arduino IDE.

The ESP32 uses a 32-bit Tensilica Xtensa LX6 processor with two cores, operating at up to 240MHz with a performance of 600DMIPS; see Figure 1 for its internal structure. The chip's basic features are:

- Wi-Fi (802.11 b/g/n compatible);
- Bluetooth V4.2;
- 448kB ROM;
- 520kB RAM;
- 36 GPIO pins;
- 16-channel 12-bit ADC;
- Two 8-bit DACs;
- 16-channel PWM;
- Capacitive touch sensor;
- Two UARTs;
- I2C, SPI, I2S, CAN interfaces;
- On-chip temperature sensor.

ESP32 Development Boards

Several manufacturers include the ESP32 chip for additional functionality in their development boards, most of which are small, yet incorporate a power regulator and serial USB interface for PC connectivity. The boards can either be used on their own as general-purpose microcontrollers with Wi-Fi and Bluetooth, or as host processors by larger microcontrollers to provide Wi-Fi or Bluetooth functions.

Sparkfun ESP32 Thing is an ESP32 development board (Figure 2) that includes an FTDI FT231x to convert USB to serial signalling. In addition, it features a LiPo charger so the board can be battery-powered. LEDs and an on-board pushbutton are also provided for simple applications, particularly suitable for beginners.

Nano32 combines an ESP32 chip with an FTDI chip for USB-to-serial programming. It also includes two pushbuttons and is breadboard-friendly; see Figure 3.

Noduino Quantum (Figure 4) is another development board based on the ESP32 chip. It measures 50 x 60 x 4 mm and provides a CP2102 for UART and debugging. The board features Arduino-compatible sockets, making it attractive to Arduino users.

ESP32 DevKitC (Figure 5) is one of the most popular ESP development boards, measuring only 5.8 x 3 x 1.1 cm. The board has two buttons, one for reset and one for putting the chip in programming mode; a micro-USB socket is provided for connection to a PC. The board receives its power from this USB port, which is also used to program the ESP32 chip.

The ESP32 DevKitC can be used on its own as a standalone microcontroller with Wi-Fi and Bluetooth functionalities, and many GPIOs.

Example Project

The ESP32 can either be programmed using the Arduino IDE, or the ESP-IDF official development framework from Espressif. Although ESP-IDF allows low-level programming and gives access to all ESP32's features, including a powerful set of APIs, it is difficult to learn to program in this development environment.

In this example, we'll use the Arduino IDE to program the ESP32 and the ESP32 DevKitC development board. The example will show how easy it is to create a Wi-Fi-based application using this processor and the Arduino programming environment; see Figure 6.

Here, one LED (called LED0) is connected to the DevKitC, where it is controlled from a mobile phone over Wi-Fi. The DevKitC is configured as a UDP client, with UDP packets sent from a server mobile phone to control the LED. In a real project, the LED can be replaced by a relay to, for example, easily and remotely control home appliances.

Valid commands are as follows; any other commands are ignored by the program:

Figure 2: Sparkfun ESP32 Thing

0=ON	**Turn ON LED0**
0=OFF	**Turn OFF LED0**

The LED is connected to GPIO port 23 through a 330Ω current-limiting resistor. The LED turns ON when the port output is at logic 1, and OFF when 0.

Mobile Phone Application

In this example, an Android-based mobile phone is used to send the UDP commands. Although one could develop a mobile application to send them, there are many freely-available UDP apps in the Play Store that send and/or receive UDP packets. This one is called UDP RECEIVE and SEND by Wezzi Studios, version 4.0.

Before sending a packet, the user must enter the destination IP address, port number and the message to be sent. Clicking the SEND UDP MESSAGE button sends the packet to its destination. The local IP address is confirmed in the receiver. The user must specify the required port number, and received packets will then be displayed on the screen.

In this example, the IP address of the ESP32 DevKitC is 192.168.1.156.

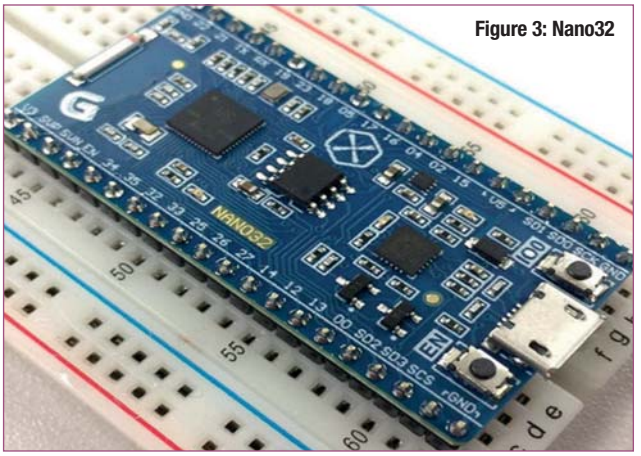


Figure 3: Nano32

Figure 6: The example setup

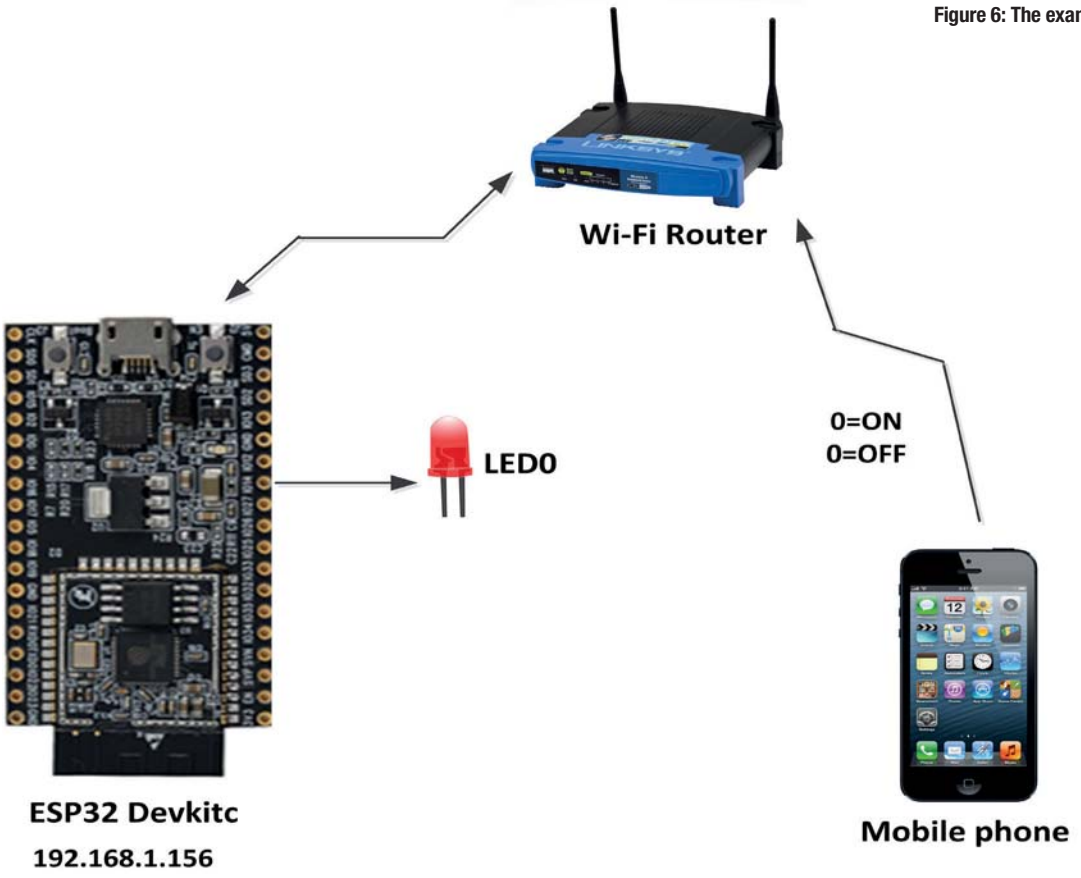
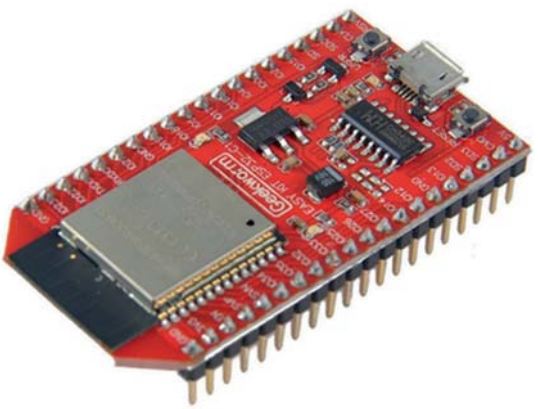


Figure 4: Noduino Quantum

Figure 5: ESP32 DevKitC



ESP32 DevKitC Program Listing

Listing 1 shows the complete program of the DevKitC example. At the beginning, the Wi-Fi library headers are added, LED0 is assigned to GPIO port 23, a local port number is defined, along with the local Wi-Fi name and password. Function Connect_WiFi connects to the local Wi-Fi network.

Inside the setup routine, the LED port is configured as output and the LED is initially OFF. Then, function Connect_WiFi is called upon to connect to the local Wi-Fi, and the UDP client is started on the local port.

The remainder of the program executes endlessly. Inside this loop the program waits to receive a packet (command) from the UDP server (in this case a mobile phone). The received packet is stored in character array Packet. The program checks the validity of the received commands. If the command sent by the mobile phone is “0=ON” then the LED is turned ON. But, if it’s “0=OFF” then the LED is turned OFF. ●

>

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```
/*************************************************************
******
 * UDP BASED CONTROL FROM MOBILE PHONE
 * ===================================
 *
 * This is an UDP based control program where 2 LEDs
are connected to GPIO
 * port 23 of the ESP32 DevKitC board, and named as
LED0. Commands are
* sent from an Android mobile phone to turn the LED
ON/OFF. The ESP32
* DevKitC is configured as an UDP client in this
application. The format of
 * the commands are as follows:
 *
 * 0=ON turn ON LED0
 * 0=OFF turn OFF LED0
 *
 *
 * File: UDPControl
 * Author: Dogan Ibrahim
 * Date: August, 2017
 *
 *************************************************************
****/
#include "WiFi.h"
#include <WiFiUdp.h>
//
// LED assignments
//
#define LED0 23
WiFiUDP udp;
//
// Use local port 5000
//
const int Port = 5000;
char Packet[80];
//
// Local Wi-Fi name and password
//
const char* ssid = "BTHomeSpot-XNH";
const char* password = "49345abxab";
//
// This function connects the ESP32 Devkitc to the local
Wi-Fi
// network. The network name and passwors are as
specifed earlier
void Connect_WiFi()
{
 WiFi.begin(ssid, password);
 while(WiFi.status() != WL_CONNECTED)
 {
 delay(1000);
 }
}

//
// Configure LED as outputs, turn OFF the LED to start
with,
// Connect to the local Wi-Fi. Also, UDP is started in
local port
//
void setup()
{
 pinMode(LED0, OUTPUT);
 digitalWrite(LED0, LOW);
 Connect_WiFi();
 udp.begin(Port);
}

//
// This is the main program loop. Inside the main
program we read
// UDP packets and then control the LED as requested.
The format
// of the control commands are:
//
// 0=ON or 0=OFF for LED0
//
// Any other commands are simply ignored by the
program
//
void loop()
{
 int PacketSize = udp.parsePacket();
 if(PacketSize)
 {
 udp.read(Packet, PacketSize);

 if(Packet[1]=='=')
 {
 if(Packet[0]=='0')
 {
 if(Packet[2]=='O' && Packet[3]=='N')
 {
 digitalWrite(LED0, HIGH);
 }
 else if(Packet[2]=='O' && Packet[3]=='F' &&
Packet[4]=='F')
 {
 digitalWrite(LED0, LOW);
 }
 }
 }
}
```

Listing 1: The example program

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- Built in remote sense and power fail signal
- Short circuit, over current, over voltage and over temp. protection
- 12V 0.3A DC fan supply
- Full international safety approvals & EMC standards

Standard Models

Model Number	Output Voltage	Output Current (Convection)	Output Current (Fan cooled)	Output Current (peak for 160mS)
PSY300S12	12V	16.67A	25.00A	33.33A
PSY300S18	18V	11.10A	16.60A	22.20A
PSY300S24	24V	8.33A	12.50A	16.66A
PSY300S30	30V	6.66A	10.00A	13.30A
PSY300S36	36V	5.55A	8.33A	11.10A
PSY300S48	48V	4.16A	6.25A	8.33A
PSY300S54	54V	3.70A	5.55A	7.40A

NOTE: Other models are available with output voltages from 9V to 57V DC.
These may be subject to minimum order quantities and specifications may differ to above depending on output voltage required. Consult sales office for further details.

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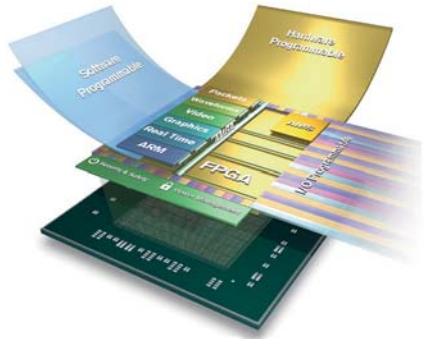


GPU for training FPGA for inference

BY **GILES PECKHAM** AND **ADAM TAYLOR** OF XILINX

So far in this series, we have examined how to implement image processing and machine-learning applications both at the edge and within the cloud. When it comes to implementing machine-learning applications, the neural network needs to be trained before use, providing the weights and biases used by the inference engine to implement the neural network.

For image-processing applications, the most common network type is a Convolutional Neural Network (CNN) since it processes two-dimensional inputs. Several different CNN implementations have evolved over the years, from AlexNet to GoogleNet, SDD and FCN; Table 1. However, they are formed of the same basic functional blocks, but with different parameterisations, and these stages are Convolution, Rectified Linear Unit (reLU), Max Pooling and Fully-Connected. Training defines parameters for the Convolution (filter weights) and Fully-Connected layers (weights and bias). While the Max Pool and reLU elements require no weights or biases, they do require parameterisation to define the sizes of the filter kernel and the stride.

GPU-Centred Training

Training introduces an additional layer to the network, which performs the loss function. This enables the algorithm to determine if the network correctly identified the input image from the image set. For an image-processing application, we can obtain image sets from sources such as www.image-net.org.

During training, both forward and backward propagation are used to determine if the image is correctly classified, and update the weights and biases based on the error signals and calculated gradients. To apply the image sets and calculate the network coefficients as quickly and efficiently as possible, large farms of graphical processing units (GPUs) are used to generate weights and biases in the shortest time. Therefore, power efficiency, real-time response and determinism for each image frame are not as critical as in the actual application.

	FP-32	FIXED-16 (INT16)	FIXED-8 (INT8)	Difference vs FP32
VGG-16	86.6%	86.6%	86.4%	(0.2%)
GoogLeNet	88.6%	88.5%	85.7%	(2.9%)
SqueezeNet	81.4%	81.4%	80.3%	(1.1%)

Table 1: Accuracy of networks with different weight representations

Machine-learning applications are increasingly using more efficient, reduced-precision fixed-point number systems, such as INT8 representation. The use of these systems comes without a significant accuracy loss compared to traditional floating-point 32-bit (FP32) approach. However, since fixed-point mathematics is considerably easier to implement than floating-point; this move to INT8 provides for more efficient, faster solutions in many implementations.

To support this generation of reduced-precision number systems, the automated Ristretto tool for Caffe enables training of networks using fixed-point number systems, removing the need for converting training data into fixed-point and so avoiding any potential impact on performance.

Machine Learning With reVISION

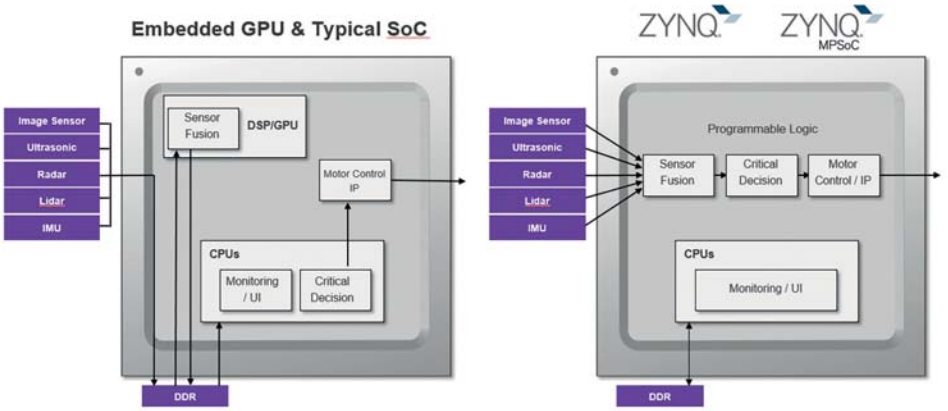
Many machine-learning inference applications are at the edge, requiring a solution not only capable of high performance, but also power-efficient, secure and deterministic.

By using a GPU-based machine learning inference engine, performance, power efficiency and determinism can be mutually exclusive. To achieve these requirements, many solutions use the All Programmable Zynq-7000 or Zynq UltraScale+ MPSoC devices, which combine a programmable logic fabric with high-performance ARM cores. These devices offer improved response time, flexibility, future modification and power efficiency.

A low latency decision and response loop is of critical importance for many applications, such as vision-guided autonomous robots, where the response time is critical to avoid injury or damage to people and its environment. This improved response time is achieved by the programmable logic that implements a vision processing pipeline and the machine-learning inference engine. Using programmable logic for this reduces system bottlenecks, when compared with traditional solutions.

With a CPU/GPU-based approach, each stage of operation requires external DDR, since the images cannot be passed between functions within a limited internal cache. The programmable-logic approach (Figure 1) allows streaming, with the internal RAM providing buffering when needed. Removing the need to store intermediate elements within

Figure 1: Streaming benefits of the programmable logic implementation



DDR reduces not only the latency of the image processing, but also the power used, and increases the determinism since there's no need to share access with other system resources or transfer image data off-chip to and from DDR memory.

The reVISION acceleration stack enables the development of these devices with industry-standard frameworks and libraries such as Caffe, OpenCV and OpenVX. Developers can accelerate framework and library functions into the programmable logic half of the Zynq-7000 or Zynq UltraScale+ MPSoC devices (Figure 2), gaining significant performance, power and latency improvements, without the need to be an HDL specialist. To achieve this, reVISION provides both hardware-optimised OpenCV functions and machine-learning inference stages such as Conv, reLU, Max Pooling and Fully-Connected stages. This enables the reVISION stack to support a more responsive Caffe inference solution out of the box, using just a prototxt file; see Figure 3.

Within the programmable logic, the machine-learning inference engine is implemented using the INT8 number system, allowing it to use DSP48E2 slices available within the UltraScale+ architecture. Using these DSP elements provides a performance increase since they are dedicated multiply-accumulate elements designed for fixed-point math.

The structure of these DSP elements also enables a resource-efficient implementation, since each can perform up to two INT8 MACC operations if they use the same kernel weights. This provides up to 1.75-times throughput improvement, enabling both a cost-optimised solution and up to six-fold increased power efficiency (GOPS per watt) compared with competing devices.

Automotive Example

One common autonomous vehicle application is a collision-detection and automatic braking system. Comparing solution implementations using GoogLeNet CNN running on Nvidia TX1 with 256 cores and a batch size of eight, with a Xilinx ZU9 with a batch size of one developed with reVISION, demonstrates some of the benefits of a reVISION-based approach. Assuming an initial vehicle speed of 65mph, the ZU9 example reacts within 2.7ms, applying the brakes and avoiding a collision, which the less-responsive GPU cannot achieve. ●

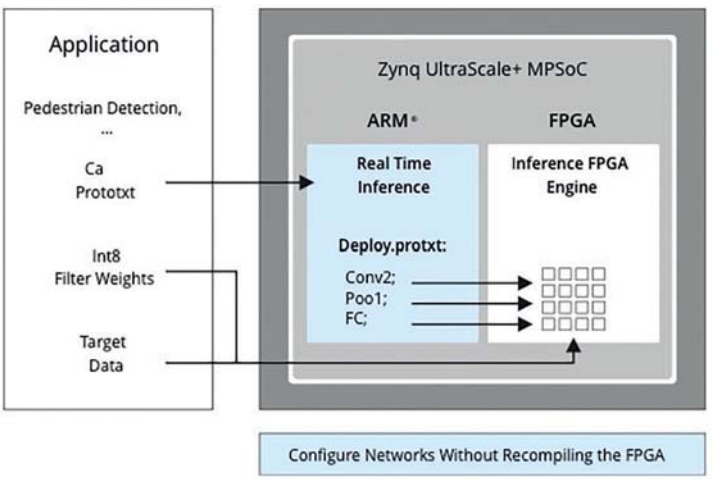


Figure 2: Caffe flow integration

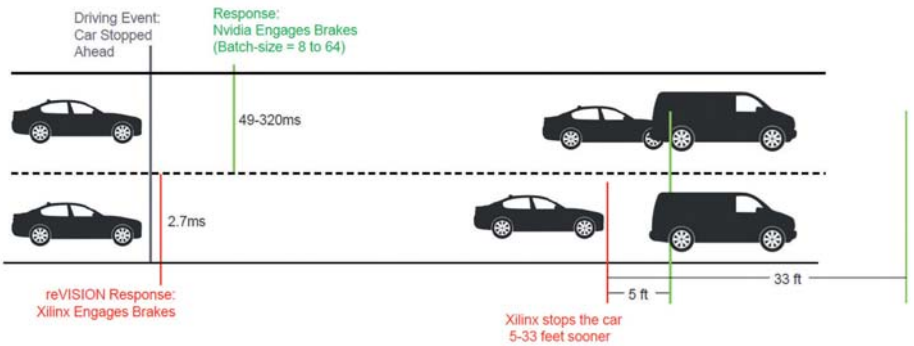


Figure 3: A more responsive solution using reVISION and UltraScale+ MPSoC

Understanding CMOS clocks

BY **ROB RUTKOWSK**I, BLILEY TECHNOLOGIES

Welcome to the CMOS clock series! You're about to learn everything (well, almost!) about these devices, including their basics and how they differ from and relate to each other. We'll clear up some common confusions about clocks in general, and specifically about CMOS clocks, and explain why they are important and how to use them best in an application.

Different Devices

There are very many different devices for frequency generation and timing, but between all the acronyms and complex terminology of the RF industry, it can be confusing to understand precisely what a clock or oscillator does, and their individual applications.

So, how do clocks differ from oscillators?

One reason some people confuse the two is that the terms "clock" and "oscillator" are sometimes mistakenly used interchangeably. An oscillator has a crystal to which an electrical charge is applied. This charge causes the crystal to vibrate and oscillate at a specific frequency, which produces a signal. Whereas a clock is an oscillator without any form of temperature compensation/control (TCXO) or oven control (OCXO).

One way to think of clocks would be as an OCXO without the "oven controlled" part, i.e. clocks are just XOs!

Clocks

The term "clock" in electronic design is a little more abstract. Fundamentally, the purpose of a clock is to regulate a process or device in some way. The clock's job is to maintain and regulate the timing of cycles and instructions, to keep the larger system functioning properly and in sync. Some specific applications range from your car to more advanced timing devices in communications equipment.

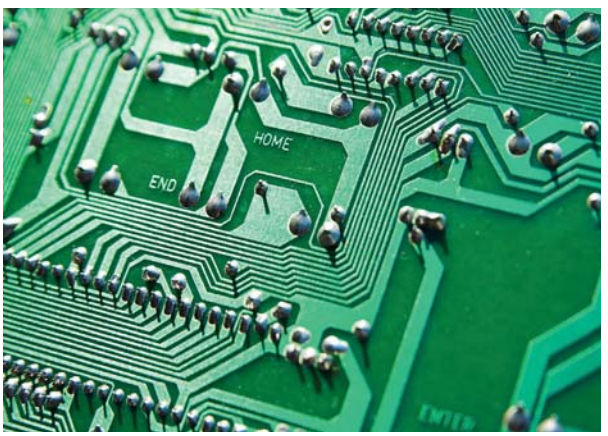
A crystal oscillator can be used to produce a clock signal, which is probably the reason for the confusion. Essentially, oscillator can refer to simple clocks that output a timing signal, or more complex modules used for accurate signal references; clocks just refer to the first.

This can lead to further confusion, which we'll clear up here, as well.

CMOS Clocks

CMOS clocks are just like the clocks discussed earlier, but where clocks output logic-level timing references, CMOS clocks output CMOS logic! CMOS clocks help timing devices function just

Wristwatches are the simplest example of where CMOS technology is used as a digital clock



PCB traces act like highways, carrying the clock signal throughout

like general clocks. Their role is analogous to that of an orchestra conductor – they make sure everything in a circuit happens at the right time and in the right order.

CMOS outputs are primarily used for digital circuits, whereas analogue circuits are usually better served by sine-wave outputs. The simplest examples with CMOS technology are digital clocks, found in wristwatches, cars, microwaves, ovens and other home appliances.

The same technology also provides advanced timing capabilities in more complex systems, in more extreme environments, including military applications, communication systems, spacecraft and satellite equipment, and anywhere strong external vibrations or g-forces may be a threat.

One of the biggest benefits of CMOS clocks is their low power consumption. Compared to other solutions, they are also relatively inexpensive to implement. CMOS clocks also offer good jitter performance and generally low phase noise. They come in different variations, including low-voltage (LVCMOS) and high-speed (HCMOS) designs.

PCBs And CMOS Clocks

Printed circuit board (PCB) traces act almost like highways, carrying the clock signal throughout. However, the higher the frequency of a clock signal, the more vulnerable it is to phase noise, distortion and attenuation.

One of the most basic steps to minimise these risks is to select the right type of clock output for the application. The outputs of CMOS clocks are especially well suited to circuits with shorter trace lengths and lower-frequency clock sources, defined as below 200MHz. ●

> The same technology is also used to provide advanced timing capabilities in more complex systems and anywhere where strong external vibrations or g-forces may be a threat

In the next issue: What's the difference between LVCMOS and CMOS?

RF SIMULATION FOR IOT APPLICATIONS WITH ANALOGUE AND MIXED-SIGNAL DESIGN TOOLS

ART SCHALDENBRAND, SENIOR PRODUCT MANAGER AT CADENCE DESIGN SYSTEMS, EXPLORES HOW ANALOGUE AND MIXED-SIGNAL DESIGN METHODOLOGIES CAN HELP RF DESIGN

Designing RF components, especially for industrial IoT applications, presents many challenges, most of which relate to achieving high performance at very low power. To make it easier, by integrating the RF design flow with proven analogue and mixed-signal design flows, engineers can access advanced tools developed for design verification and reliability analysis.

RF Component Integration

Integrating RF components into a product brings its own set of challenges:

1) Adapting designs to new process technologies;

To reduce cost and size, the level of integration required for RF components for IoT applications is much higher than for cell phones. As a result, designers need processes more suitable to low-power digital design than high-performance analogue design. However, using low-cost processes means that designs must be adapted to meet the performance requirements.

2) Variation-aware design;

Because there are more variations of low-cost processes, analogue designers may need to characterise their design across hundreds or thousands of process corners, and account for mismatch effects. This requires Monte Carlo analysis.

3) Design for reliability.

The reliability requirements for industrial components are stricter than for consumer applications; circuits must operate longer across a wider temperature range. This means that all circuits, components and interconnects need to be verified they satisfy the more stringent requirements.

Adapting Designs To New Process Technologies

Integrating RF components into new process technologies requires allowing for the limitations of CMOS process technologies, whilst taking advantage of what CMOS does best to meet the design specifications.

As process technologies scale down, the density and performance of digital gates increase. Using the advantages of dense logic to improve the performance of analogue design is called digitally-assisted analogue design. One example of this approach is the integrated channel filter used in receivers.

This channel filter is a bandpass filter with five bi-quad sections, that must be controlled to ±1%, even though the process variation of the on-chip resistors and capacitors is 30%. The solution is to implement the filter capacitors with digital-to-analogue converters to digitally tune their values to compensate for process variation. The tuning is done by reversing the inputs of the final bi-quad stage in the filter, giving it a positive feedback, turning the stage into an oscillator. The frequency of oscillation is the same as the bandpass centre-frequency of the stage. Calibration is performed by tuning the oscillator frequency to the centre frequency of the bandpass filter.

With calibration, the filter achieves high accuracy at low cost. In addition, since the filter is calibrated before use, phenomena such as temperature drift are eliminated.

Figure 1a shows a block diagram of the channel filter, whose frequency and bandwidth meet the specification after tuning.

These simulations must be verified to confirm that the calibration will work across all process, environment and operating variations, and not just the nominal conditions. In addition to designing for variation, calibration of the complete circuit also needs be accounted for. For example, the calibration of the RCs in the bi-quad might be used elsewhere in the design, thereby providing precision control of the PLL filter.

Designs may have multiple calibrations, such as channel filter calibration, VCO free-running frequency calibration and frequency splitter/combiner calibration, helping build high-performance RF components even in processes intended for low-cost digital designs.

Variation-Aware Design

Analogue engineers have tools and methodologies for variation-aware design that allow them to develop high-performance components using low-cost digital processes. These tools are also required when SoC designers need to use analogue IP blocks. In addition, using variation-aware design to reduce a design's margins at older processes results in smaller die size and lower cost, which improves competitiveness.

Tools for Monte Carlo and corner analyses have evolved significantly over the last few years, to everyone's benefit. Variation-aware design can be integrated into an existing design environment; see Figures 2a and 2b. The results show LNA compliance with the target specification across different corner conditions (2a) and Monte Carlo analysis (2b). The figures also highlight that the corner analysis needs to

Figure 1a: Digitally-assisted channel filter

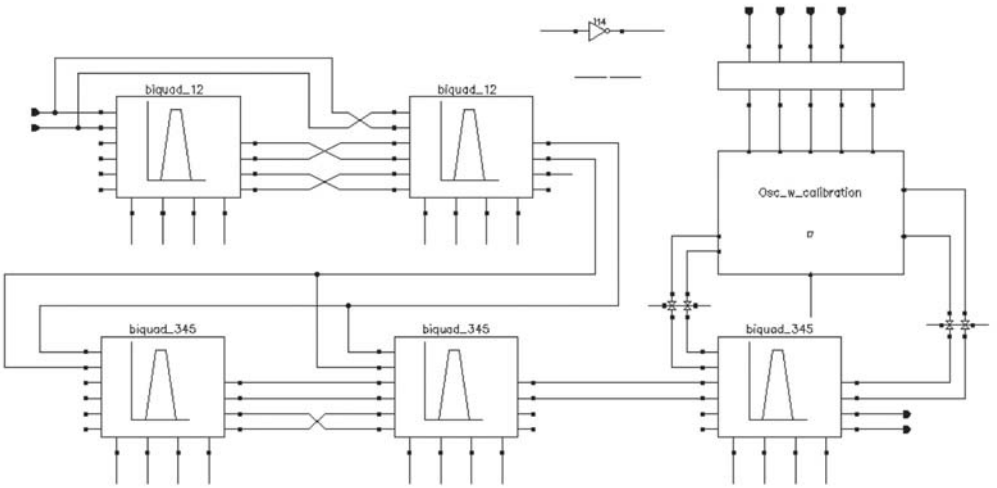


Figure 1b: Channel filter calibration

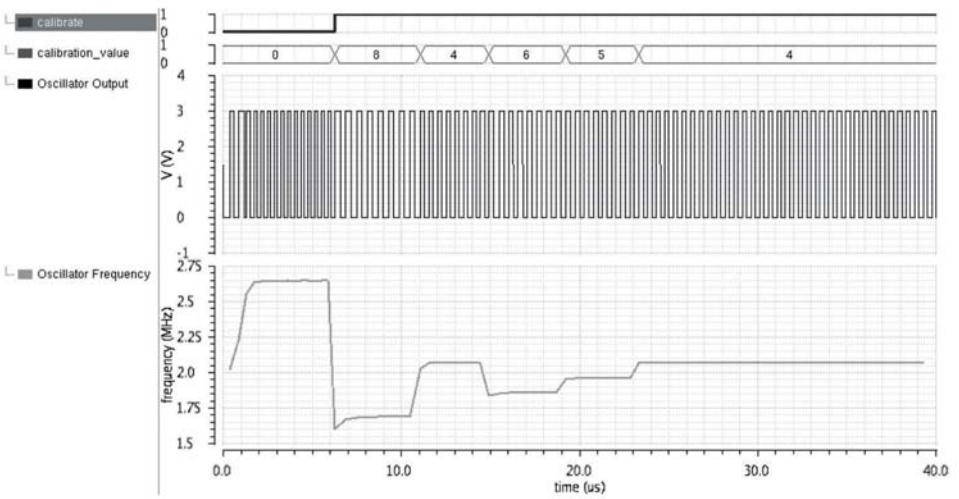


Figure 1c: Effect of calibration on channel filter frequency response

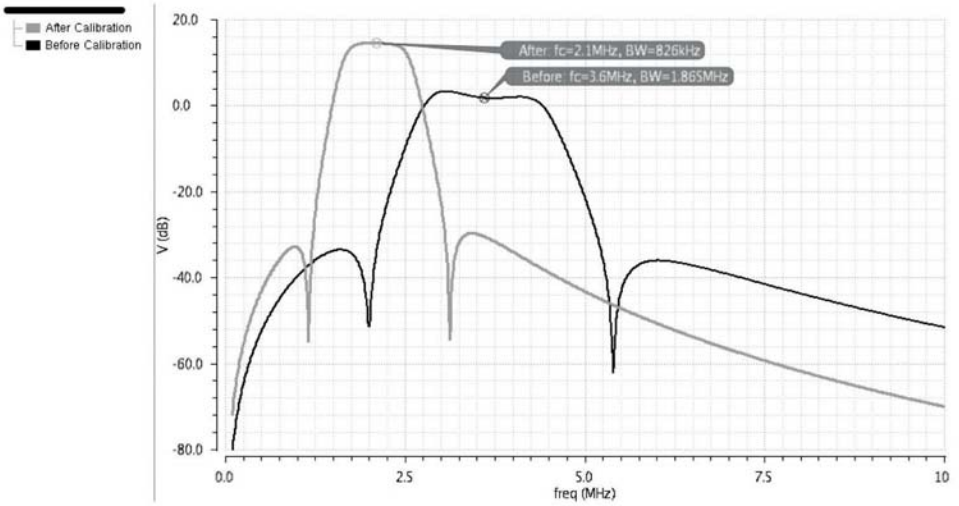


Figure 2a: Corner analysis results for LNA

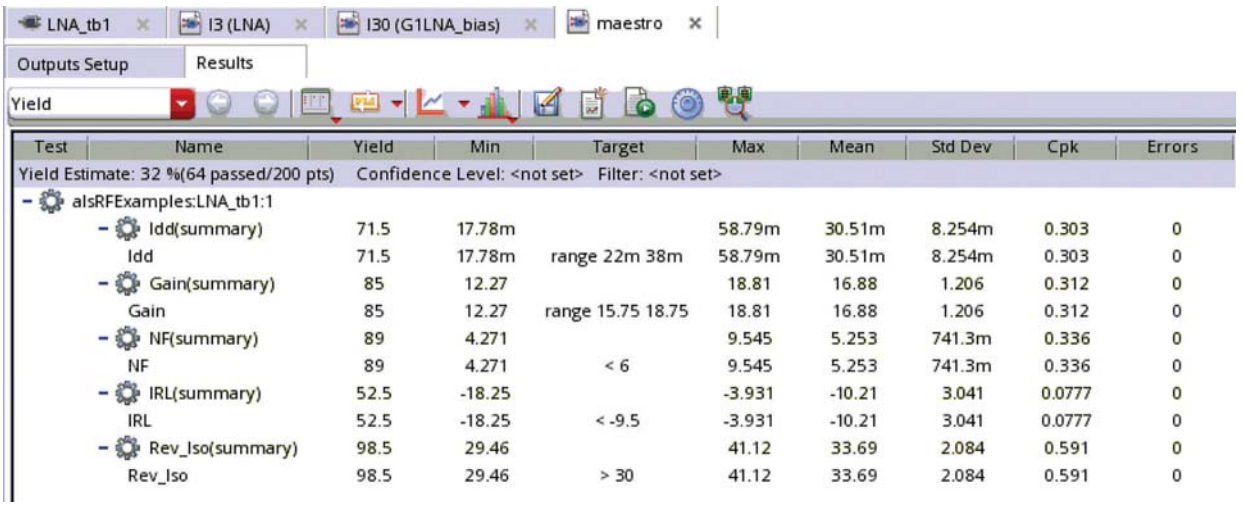


Figure 2b: Monte Carlo analysis results for LNA

include more corners since the PVT corners pass but the total yield is only 32% for the Monte Carlo analysis. Increasing the number of simulations helps thoroughly characterise the design, but on the flip side, it will also increase design turnaround time.

Shortening Simulation

Most simulations take a long time. A typical example is the very time-consuming simulation for multi-tone harmonic balance analysis required to calculate intercept points IP2 and IP3. But, there are ways to reduce this simulation time; for example, Cadence's Spectre RF Option offers the possibility of harmonic balance analysis called rapidIP2 and rapidIP3, which estimate distortion from small-signal analysis. This speed is important when facing long simulation times for verifying many PVT corner simulations or Monte Carlo analysis runs. Once the worst-case conditions have been identified using these analyses, harmonic balance analysis can be used for detailed simulation.

Rapid IP3 results are shown in Figure 3; the IP3 point is extrapolated from the simulation results. The rapid triple beat analysis is based on rapidIPx analysis, which addresses the challenge of simulating transmitter tones leaking in the receiver. Using harmonic balance analysis for this requires simulation with four large-signal tones and presents significant performance and convergence challenges. Rapid triple-beat analysis only requires simulation with one large signal tone to calculate the periodic operating point, then for the remaining tones it calculates the distortion based on small-signal analysis.

The VCO Challenge

Simulating with process variation creates several challenges for designers, including characterising a VCO.

VCO performance is specified at a given free-running frequency, with its own set of conditions. The target frequency for the nominal conditions comes from the testbench's input voltage, which is fixed, and since the free-running frequency has process, environment and operating conditions, this input voltage must change with each simulation – and that's quite a challenge.

A solution is to have the simulator tune the VCO input voltage to force the VCO to a desired frequency; see Figure 4. In this case, VCO tuning is used to force the VCO to oscillate at 3GHz, then phase noise is measured at 1MHz offset from the carrier as a function of tank inductance.

By automatically tuning the VCO frequency, characterising the VCO across process is simplified.

Design For Reliability

Why is reliability analysis necessary; aren't design guidelines enough? Simply put, yes, since designing for industrial applications is different from designing for consumer or automotive applications. While the requirements for industrial designs are not as challenging as for automotive, consideration of the effects of device degradation on performance is crucial. Comparing the two, the operating temperature range is roughly double and there are similar changes to the expected lifetime of a component.

However, it's worth remembering that while automotive requirements are much tougher, a car is not always running. So, while the absolute requirements may not be as strict, overall, designing for two environments is challenging.

When developing consumer applications, designers have used safe operating checks and design margin to meet their reliability requirements, impacting die size, cost and competitiveness. Due to the more relaxed requirements, consumer applications have fewer devices that impact reliability, so the cost of increased design margin is acceptable. However, industrial products must operate in harsher conditions, and designing for worst-case scenarios means that die size, cost and competitiveness concerns come back.

One solution is to perform reliability analysis, where an ageing model is used to predict operation-linked device degradation. Based on device characteristics and operating and environmental conditions, degradation is calculated as a function of time.

Figure 5 shows reliability analysis results where the VCO free-running frequency was simulated with periodic steady-state analysis across PVT corners and frequency changes for a 10-year operation. The gradual ageing method performs the calculation incrementally, so it includes effects of degradation on the circuit characteristics and the acceleration of ageing. The results show that for some corner conditions, the change in free-running operating frequency is unacceptable. Reliability analysis thus offers a tool to analyse the effect of device degradation on circuit performance. ●

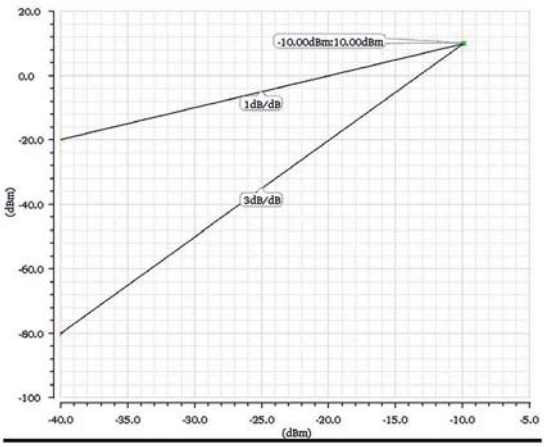


Figure 3: Rapid IC3 simulation results

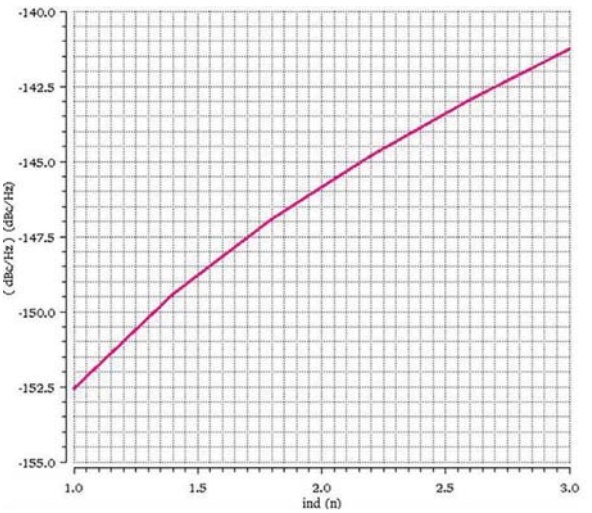


Figure 4: Example of VCO tuning

Point	Age	Test	Output	Nominal	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2
Parameters: years=1												
1	fresh	Osc	/out									
1	fresh	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
1	stress	Osc	/out									
1	stress	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
1	1 yr	Osc	/out									
1	1 yr	Osc	Frequency	792.7M	> 780M		fail	360.3M	1.293G	1.293G	991.9M	360.3M
Parameters: years=2												
2	fresh	Osc	/out									
2	fresh	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
2	stress	Osc	/out									
2	stress	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
2	2 yr	Osc	/out									
2	2 yr	Osc	Frequency	787.4M	> 780M		fail	357M	1.287G	1.287G	986.1M	357M
Parameters: years=3												
3	fresh	Osc	/out									
3	fresh	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
3	stress	Osc	/out									
3	stress	Osc	Frequency	854.4M	> 780M		fail	406.4M	1.351G	1.351G	1.053G	406.4M
3	3 yr	Osc	/out									
3	3 yr	Osc	Frequency	784M	> 780M		fail	355M	1.283G	1.283G	982.4M	355M

Figure 5: Effects of device ageing on VCO free-running frequency

BUILDING A BETTER WIDEBAND RF POWER AMPLIFIER

BY **JAWAD H QURESHI**, **WALTER SNEIJERS** AND **JOHN GAJADHARSING**
FROM AMPLEON IN NIJMEGEN, THE NETHERLANDS

RF power amplifier (PA) designers have long used the Doherty architecture to increase the efficiency of their designs. Its effectiveness and simplicity have made it the most commonly used architecture for high-power mobile basestations, although its bandwidth is sometimes limited. Recent research has shown that simple modifications to the basic Doherty power amplifier (DPA) architecture can overcome this limitation, making it more suitable for applications such as broadcast TV transmitters.

The modified Doherty architecture offers excellent efficiency and bandwidth, but its integration in circulator-less transmitters with a harmonic reflective filter is complicated by its single-ended nature and absence of second-harmonic traps. The modified architecture also needs a Doherty power combiner designed to work at the base impedance of the PA devices. This is difficult to do at the required very high power levels, due to the size of the transmission lines needed.

Most high-power wideband class-AB PAs deal with these issues by using a push-pull topology, but this is difficult to implement for ultra-wideband DPAs because it requires a wideband balun (balanced to unbalanced converter) with an electrical length of between 20 and 30 degrees at impedances as low as 2Ω. One way to achieve this is to combine the function of a quarter-wave transmission line with the balun, but, although the performance of the resultant DPA is quite impressive, it cannot amplify the full UHF band due to the difficulty of making a good wideband balun.

We're trying to address these issues by using an odd-mode wideband Doherty structure that integrates the balun and the wideband Doherty combiner, thus providing the required bandwidth and second-harmonic signal suppression. Our prototype offers more than 40% average efficiency over most

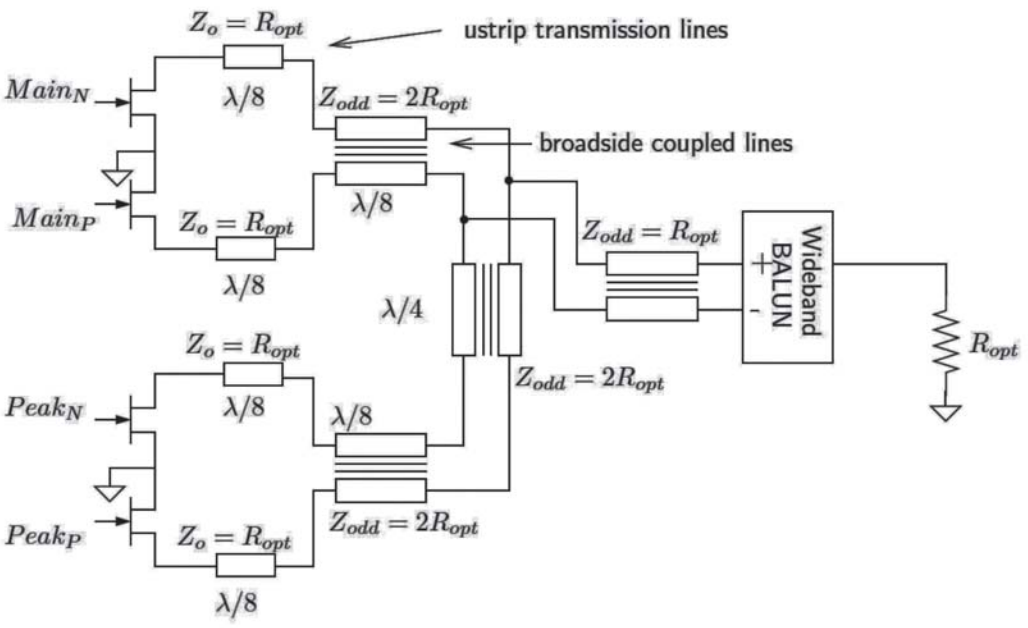


Figure 1: Schematic of the odd-mode Doherty combiner

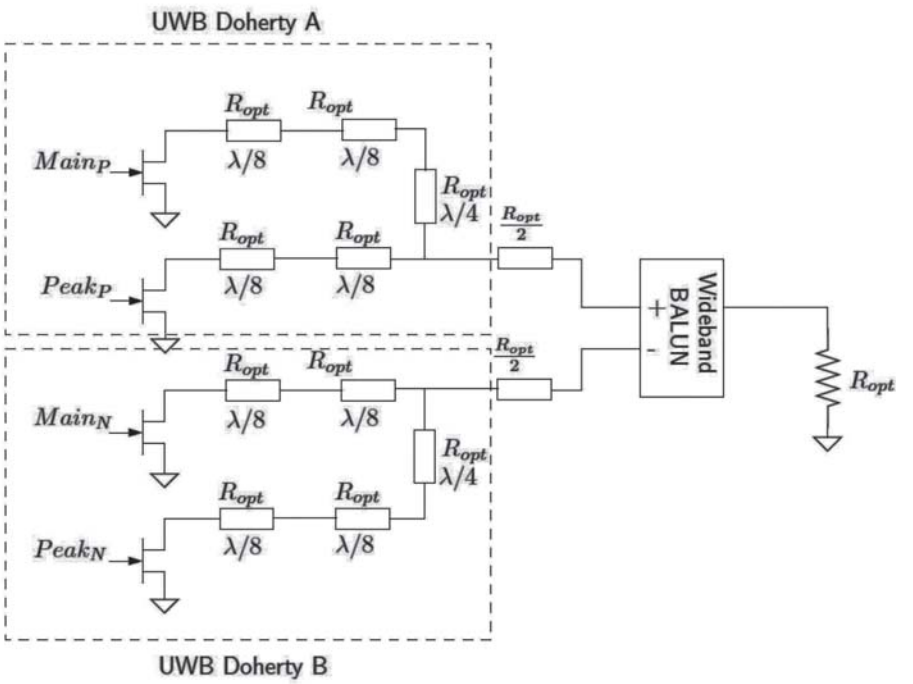


Figure 2: The equivalent circuit of the odd-mode Doherty

of the UHF broadcast band (from 470-810MHz) at an average output power of 220W, with a peak power capability of more than 1.4kW. The PA is also compatible with digital pre-distortion techniques, as verified using commercially-available DVB-T signal exciters.

Odd-Mode Doherty Combiner Design

Figure 1 shows a simplified schematic of the proposed wideband combiner.

Most of the circuit is built using broadside-coupled transmission lines, with an ideal wideband balun at the output. Broadside-coupled lines can be designed for almost any impedance level, and offer very high common-mode impedances if the ground plane is far compared to the thickness of the substrate. Broadside-coupled lines also offer much lower characteristic impedances than micro-strip transmission lines of similar size, due to the higher capacitances between transmission-line conductors.

Circuit analysis can be simplified if evaluated separately for odd (differential) and even (common) mode conditions. If the inputs of the main and peak transistor pairs are driven by differential signals, odd-mode analysis of the circuit represents its response to fundamental signals and even-mode analysis to second-harmonic signals.

Odd-Mode Analysis

For odd-mode analysis, the transistor inputs are excited differentially and the circuit is analysed at fundamental frequencies from 470-810MHz. Under these conditions, the broadside-coupled transmission lines act like micro-strips and the circuit becomes like two Doherty amplifiers, excited differentially and combined with a balun; see Figure 2. This results in very wideband performance in both back-off and full power conditions; see Figure 3.

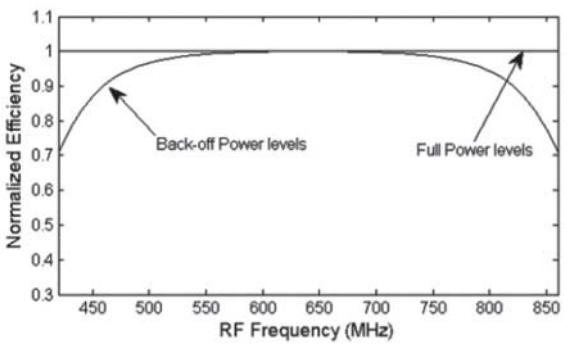


Figure 3: Normalised efficiency of an odd-mode Doherty combiner

Even-Mode Analysis

To analyse the circuit for second harmonic current, the input signals to the main and peaking transistor pairs are assumed to be in phase, and the circuit analysed for second harmonic frequencies between 900MHz and 1900MHz. Under these conditions, all the broadside-coupled transmission lines in combination with the output balun present an open-circuit – see Figure 4's frequency response plot.

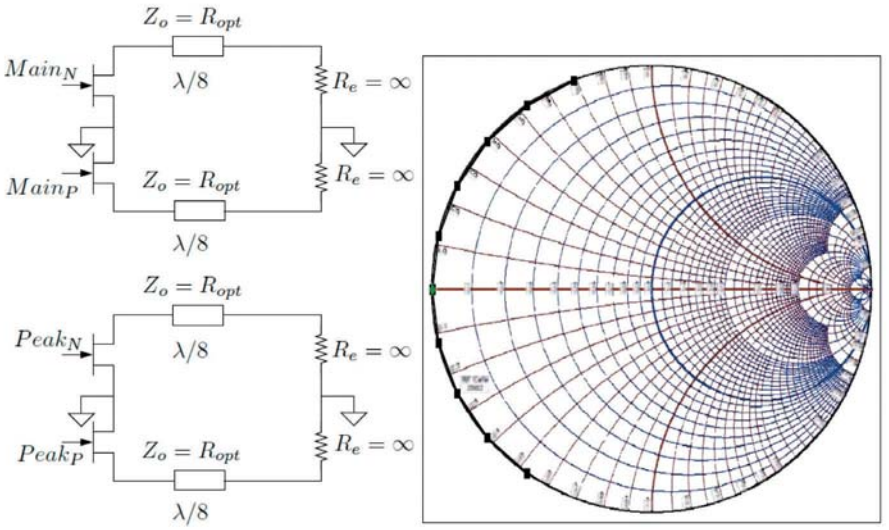


Figure 4: Even-mode equivalent circuit of odd-mode Doherty and its response to second harmonic frequencies

The Output Balun

For our modified Doherty circuit to work well, it needs a very-wideband planar balun that can transform the circuit's output impedance to 50Ω. For our 1.4kW wideband UHF DPA prototype, the required fractional bandwidth is close to 55% and the required impedance transformation ratio is over 20. To meet these specifications, we exploited the transmission-line characteristics of a commonly-used planar balun to implement a wideband multi-section impedance transformer, shown in Figure 5.

The combined structure acts as a balun and impedance transformer (transformation ratio of 20) over more than 55% fractional bandwidth, with input reflection lower than -25dB and loss of below 0.5dB.

Building A Prototype

To demonstrate the odd-mode Doherty architecture in practice, we built a prototype for UHF broadcast TV applications using Ampleon's BLF888A/B LDMOS devices.

The use of broadside-coupled transmission lines complicates the layout, so we used a multi-layer PCB, shown in Figure 6, with the circuitry on the inner layers shown by the shaded path in the figure. The PCB is mounted on a base plate with air cavities, to provide high common-mode impedances to the coupled lines.

Measuring The Prototype

We measured the prototype using a commercial DVB-T exciter; the results are shown in Figure 8.

The input signal of the DPA was a DVB-T signal with a peak-

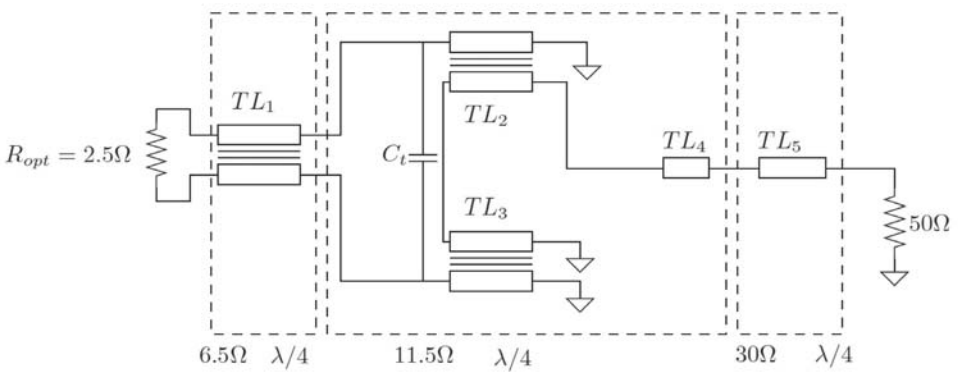


Figure 5: Output impedance transformer and balun

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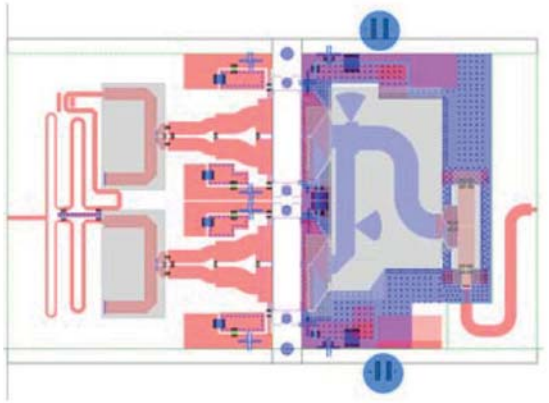

Figure 6: Layout of the odd-mode Doherty prototype

to-average ratio (PAR) of 9.5dB, and the measurements were performed at 220W output, so that the output PAR was always more than 8dB. The prototype was more than 40% efficient across most of the band.

The same DVB-T exciter was used to pre-distort the output of the DPA, showing that the prototype can be used with pre-distortion to achieve the required adjacent channel leakage power ratio, a measure of the amplifier's ability to restrict its output to the intended channel.

Good Efficiency

The Doherty architecture combines at least two PAs, each tuned to be most efficient at a different power level, to offer good efficiency at the wide variety of instantaneous power levels presented by complex modulation schemes such as DVB-T.

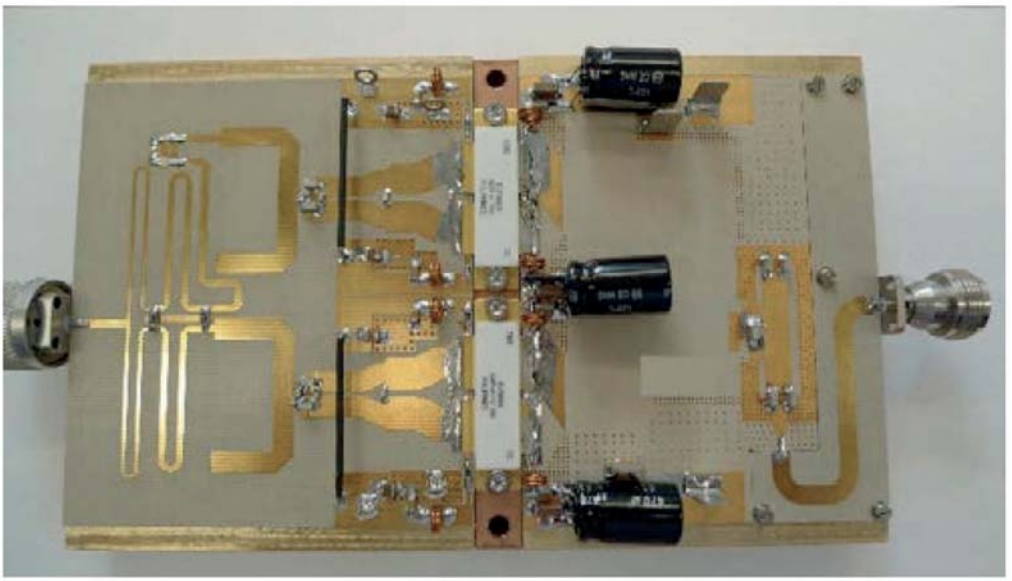

Figure 7: Odd-mode Doherty amplifier prototype

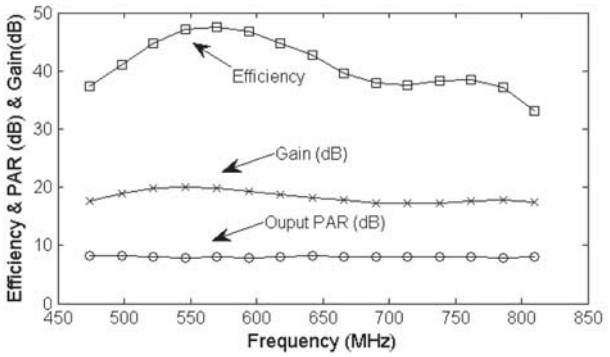

Figure 8: Measured average efficiency, gain and output PAR at 220W output power

Such architectures can be very efficient, but it is usually at the cost of having to manage complex trade-offs elsewhere in the design, such as in the combining circuitry, or the circuitry that couples the output of the PAs to the load.

In our differential Doherty architecture, we produced good wideband efficiency and control of the wideband harmonics that would otherwise make it more difficult to apply the design to transmitters that don't use circulators.

Our approach could also be applied to asymmetric wideband DPAs and to three-way DPAs. It can also be thought of as two ultra-wideband DPAs operating on the top and bottom of the same substrate in differential mode, thereby packing twice as much power into the same area while reducing the size of the transmitter. ●

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OPTIMAL CELL-PATTERN SETTING ALGORITHM FOR COMMUNICATIONS SYSTEMS

BY **EREN KUREN** AND **AKIN CELLATOGLU** FROM THE EUROPEAN UNIVERSITY OF LEFKE GEMIKONAGI IN CYPRUS

In certain pulse-type range-detection systems replica correlation is employed to achieve better results in communication. In replica correlation, obtaining optimum cell pattern in a packet of transmitted pulses is an important requirement for high performance. Here, we present an algorithm embedded in simulation software, to find the optimal pattern for a given n-cells packet, where n can be any chosen number for an application.

Replica Correlation Simulation Software

The replica correlation technique involves transmitting a coded pattern of binary phase shift keyed (BPSK) signal incorporated as a packet in the transmitted pulse. The received echo is fed to a tapped digital delay line where analogue inversions are given in taps in the reverse form of the transmitted pattern. The summation of all analogue signals at taps will boost the amplitude of the received signal required for easy threshold detection.

We developed simulation software using dynamic programming with a modular-based approach, which finds the optimal pattern for a given cell length n. The software simulates and emulates all circuits and devices used in the replica correlation.

By simulation, the source pulse and CW signals are generated and BPSK signal produced. Also, the received signal is added to noise converted into a binary word sequence by an ADC, delayed accordingly by FIFO organisation. Tap inversions are performed and summed to produce replica correlated output.

All properties and parameters used in the devices and circuits are considered while preparing the software. Creating signal graphs for coded signals and producing result graphs are the software's additional features, which incorporates Matlab and Simulink functionalities.

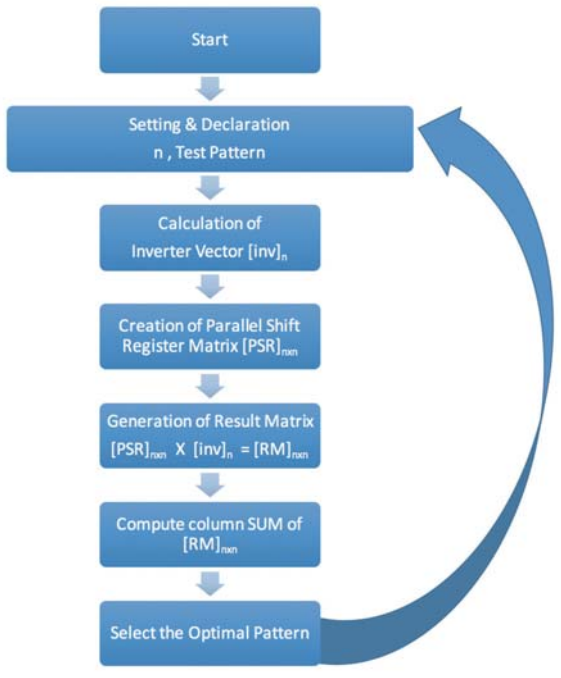

Figure 1: Generating the optimal pattern

Automatic Pattern Setting

Automatic cell-pattern setting is an important concern for easy detection of targets. This pattern gets the signal boosted in the last cell and suppresses it at the lowest possible level in all other cells. The simulation software finds the signal levels during n-pulse periods for all the set patterns, and assesses the best pattern needed for the given n. The optimal-pattern-setting algorithm works as follows:

Processing starts by setting cell density n at 7, and an initial test pattern is set at all zeros (0 0 0 0 0 0 0). The inverting vector [inv]7 required for processing is obtained by checking the test pattern cell value in a loop. If the value is zero, then assign the inverting vector value to -1, otherwise 1.

Parallel shift register [PSR]7x7 matrix is generated by using the [inv]7. With repeated iteration we obtain a lower triangular matrix. By using [PSR]7x7 and [inv]7 we arrived at the result matrix [RM]7x7 as follows:

Each element in a row of [PSR]7x7 is multiplied by one element of [inv]7 to obtain one corresponding row of [RM]7x7. A sum of the elements in each column of [RM]7x7 is computed and a voltage level pattern obtained. The best voltage pattern is (-1, 0, -1, 0, -1,

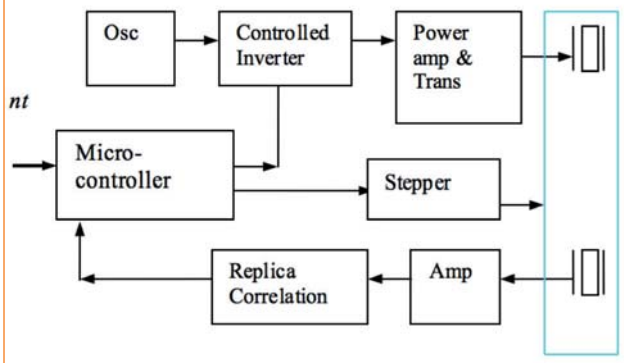

Figure 2: Simplified schematic of the sonar transceiver

0, 7) and the corresponding cell pattern giving this best voltage pattern is (0 1 0 0 1 1 1).

This calculation is repeated up to the cell density of 31.

As shown in Table 1, the replica correlation simulation software (RCSS) gives the optimum cell pattern for selected lengths ranging from 7 to 31 and the voltage level contained in all other cells of the packet.

Cell Density *n*	Cell Pattern	Voltage Level
7	-+--+++	1
9	+++--++-+	3
11	+-++-+++---	1
13	+++++--++-+-+	1
15	+-+-++--++-----	3
17	++++---+---+--+-+	3
19	+----+----+-+++-+--	3
21	++++++---++--+--+-+-+	3
23	+----+----+---+-+++–+--	3
25	++++++---+++--+--+--+-+-+	3
27	+++----+++-+++-+++-+++-+-+-	3
29	+---+-++---+-++----+--++++-++	3
31	+++-+++--+++----+-++-++--+---+-	5

Table 1: Optimum cell pattern

Dynamic Setting Of Cell Length

Depending on the requirements of the application, the packet can be set as a 7-cell pattern (for a low-range and low-noise environment), or a 31-cell pattern for a long-range noisy environment.

We consider an application of underwater exploration sonar buoys launched at sea; see Figure 2.

A hex number nt indicates the type and number of the buoys to be used; this is input to a microcontroller, which finds the best cell-density number (n) from a lookup table in memory, and calls the algorithm to set the cell pattern. The set pattern is delivered serially to a controlled inverter to produce the BPSK signal accordingly.

The source for CW input is a phase set oscillator. The BPSK generated is power amplified and fed to a piezoelectric transducer (PZT) to produce an acoustic wave in water. The reflected acoustic wave from a target is picked up by the receiver's PZT, amplified and a replica correlated. The envelope of the replica-correlated output is fed to the microcontroller for threshold detection and range estimation. The microcontroller also issues a drive signal to the stepper motors driving the PZTs to produce angular sweep of the acoustic beam.

A set of buoys is thrown in sequence in a selected area for underwater exploration. Depending on the distance from the shore, the buoys need a particular cell-density n to reach the optimal requirements. The nt value needs to be fed into the RCSS in accordance with the type of buoy thrown in each instance.

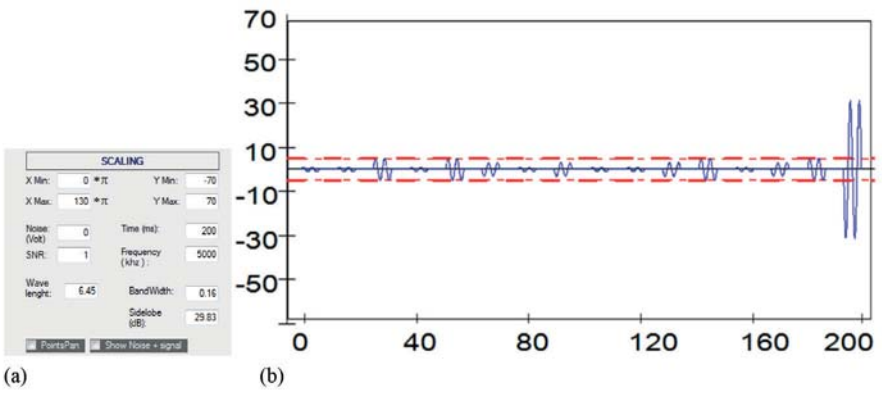

Figure 3: The replica correlated output produced by the RCSS for the length of 31 cells: (a) Adjusting the noise level in software; (b) The transmitted BPSK without noise addition is used to produce this output

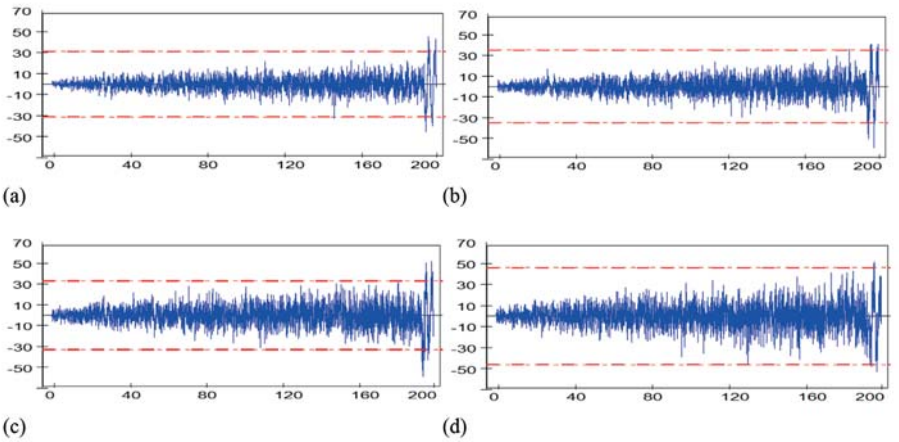

Figure 4: Replica correlated output under varied noise environment: (a) 31-cell pattern with 200% noise; (b) 31-cell pattern with 400% noise; (c) 31-cell pattern with 600% noise; (d) 31-cell pattern with 800% noise

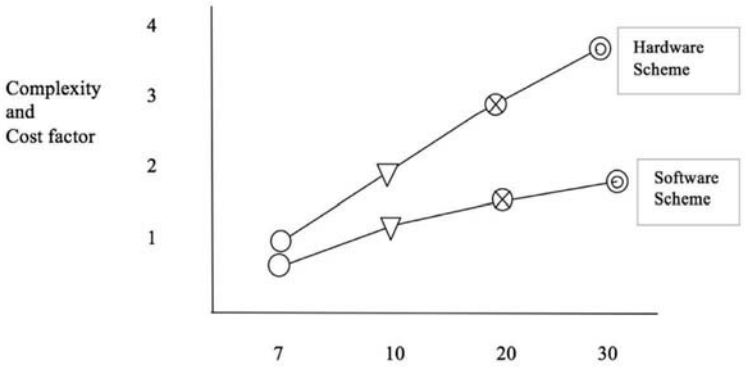

Figure 5: Complexity vs n

Performance Analysis

The RCSS software assesses the performance of the transceiver system for set parameters. The performance of the buoy on a number of cells n in a packet is then determined.

The cell-density n chosen for an application influences the detection process to an extent. Since the probability of detection is an essential parameter, the estimation of its dependence on n is worthwhile.

The probability of detection also depends on the probability of a false alarm and on the signal-to-noise ratio of the received signal. Moreover, the level of signal-plus-noise depends on the number of cells n present in the transmitted pulse packet. The relationship between the probability of detection and n is almost linear, therefore detecting the desired target on a threshold is easier with a larger n; see Figure 3b.

Noisy Environments

The sonar buoy works under water, where there is background noise, and which is an unknown parameter. And, the farther from the target, the greater the noise, so it is important to determine the detection performance of targets under various conditions.

The RCSS makes provisions for such cases, adding degrees of noise to the signal (Figure 3a) and assessing the performance of the replica correlation (Figure 4). Gaussian noise is added to the signal and performance is evaluated by the RCSS.

During the pulsing period (n cell-length) of the target's return echo signalm, we see boosting of the signal-plus-noise level in the nth cell. The RCSS dynamically sets the threshold level, determined by the average of peak levels in the nth cell and the maximum peak levels of any other cell. When the signal-plus-noise exceeds the threshold, the target is detected and the range determined accordingly. In this process, the RCSS senses the consistency of the signal-plus-noise level crossing the bidirectional threshold levels, and keeps false alarm detection to a minimum. When there is no echo returned from the target, there will be no boost in the nth cell.

Hardware And Software Complexity

The replica correlation could be performed by hardware or software. The hardware uses digital delay lines and grows in complexity as cell density n rises. On the other hand, the software method uses FIFO memory to gather the data required for processing. While the processing is performed instantaneously, there is a very small processing delay, also delaying the results. Nevertheless, with recent high-speed processors, this delay becomes negligible.

The complexity of the software method is largely associated with the size of the FIFO memory, but with technological developments this complexity and cost decrease compared to the hardware methods. Figure 5 shows a typical variation in complexity associated with n.

Useful Applications

The optimal cell-pattern-setting algorithm is useful in all projects involving replica correlation. Without additional hardware, the simulation software analyses the performance of communications system, such as radar and sonar, when operating in various noisy environments. Certain communications systems may demand greater cell density, and for those requirements the software accommodates by increasing cell density to the required value. ●

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TEMPERATURE PREDICTION SCHEME FOR ACCURATE CONTROL OF BASE STATIONS

BY **SHUAI LV, BENZHI SU, ZIGAO LIU** AND **QIANG MENG** FROM THE QINGDAO HARBOUR VOCATIONAL AND TECHNICAL COLLEGE IN CHINA

With rapid development of communications, operators have accelerated the pace of installing new base stations to guarantee quality of service.

Base stations consist of amplifiers, filters, radio frequency (RF) circuits and other electronic components, all of which need to work in temperatures between -40°C and +46°C. Research shows that some 55% of electronic equipment failures are due to temperature; also, elevated temperatures age electronic devices quicker. In addition, base stations are in typically confined spaces, so heat removal is neither quick nor easy, therefore the base station's thermal aspect is very important in its overall design.

In traditional base station designs, a series of environment-monitoring systems control the temperature. When it deviates from normal, the system sends an alarm and adjusts the temperature accordingly. But, this type equipment normally requires more space and funds.

More recently, a front-end thermal design has taken hold in industry, which uses comprehensive thermal analysis during the design stages of electronic equipment. The scheme can estimate the base station's internal temperature during normal operation and when fitted in specific environments. As such, it shortens the development cycle, reduces the need for external temperature-control equipment and, hence, lowers the overall cost of the base station.

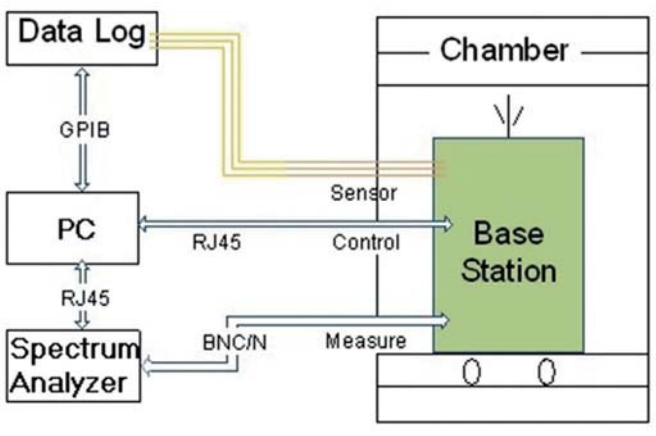

Figure 1: Our 'high-low' temperature test system

Appropriate Tests

According to the ITU 3GPP2 standard, the working environment of a base station needs to meet certain external environmental conditions, which among other things include temperature and humidity. We designed an appropriate 'high-low temperature' test circuit, simulated these conditions and measured the temperatures. We then derived a temperature prediction function that determines the base station's operating temperature in various conditions. We then used MATLAB to simulate the temperature range of these environmental scenarios based on this function.

Our test system consists of a PC, spectrum analyser, thermal sensor, chamber and base station; see Figure 1. The chamber provides the environmental temperature for the base station to be tested in. Thermal sensors located inside the base station convert thermal signals into voltage, which are then digitised and sent to the PC via the GPIB port.

The spectrum analyser measures the performance of the base station under test, with the results displayed on the PC.

According to the ITU 3GPP2 requirements, when the environmental temperature changes, the voltage and humidity required for the base station's normal operation need to change, too. Figure 2 shows the high-low temperature test for these requirements.

Base Station Structure

Typically, the base station consists of a baseband unit (MT-BBU), transceiver unit (MS-TRDU), power supply, distribution panel (PDP), and others. The components of the MT-BBU and MS-TRDU are sensitive to the environmental temperature, and both units are designed to stop working when the temperature goes up, to protect the components. On the other hand, if the environmental temperature drops too low, performance of the RF filter will suffer.

Of course, the air flow inside the base station also affects thermal performance.

All these conditions have called for many thermal sensors to be placed inside the MT-BBU and MS-TRDU to measure the operating

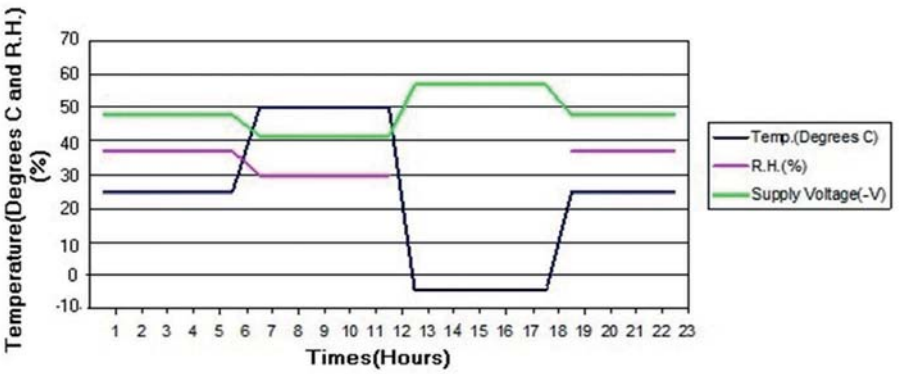

Figure 2: The environmental requirements for the 'high-low' temperature test

temperature. A base station and the positions of the 26 test points are shown in Figure 3.

Temperature Change Tests

Based on our test results, when the environmental temperature changes, say from low (-5°C) to normal (25°C), the test point at the right MS-TRDU circuit-board shows the highest operating temperature; see Figure 4. This temperature increases with time, reaching a steady state after about an hour.

We used the three-element method of the first-order circuit theory to analyse the temperature variation function; the mathematical model between temperature and time is a one-order linear differential equation. The Tp (temperature) and t (time) fit into an exponent equation, with b(1), b(2) and b(3) the unknown coefficients:

$$Tp = b(1)(1 - b(2)e^{-b(3)t}) \quad (1)$$

By applying the measured results from our tests, we can determine those coefficients:

$$Tp = 41.21(1 - 0.37e^{-0.0876t}) \quad (2)$$

According to the test data, when the temperature is steady, the tolerance is within ±1°C, which is acceptable. For simplification, we assume that when the theoretical value reaches Tp(max) – 1, it is a stable temperature. Plugging this into Equation 2 shows that t = 53.52 minutes.

Correspondingly, at this same test point, when the environmental temperature changes from normal (25°C) to high (50°C), the equation becomes:

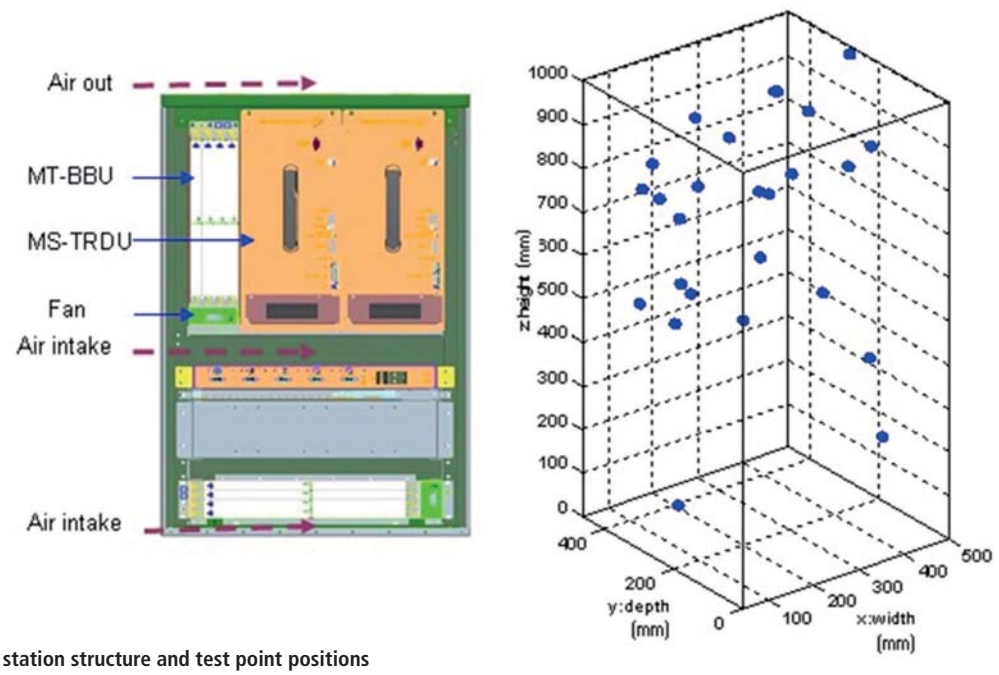

Figure 3: Base station structure and test point positions

test point (°C)	Te-Normal1 (27.25°C)	Te-High (50.02°C)	Te-Low (-4.52°C)	Te-Normal2 (29.14°C)
Control-Board-HTSNK2 (°C)	60.68	73.05	40.62	60.43

Table 1: Different temperatures at the HTSNK2 control board

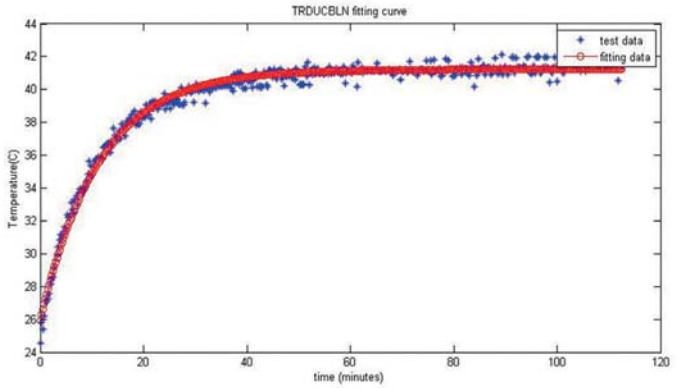

Figure 4: Temperature change from -5°C to 25°C

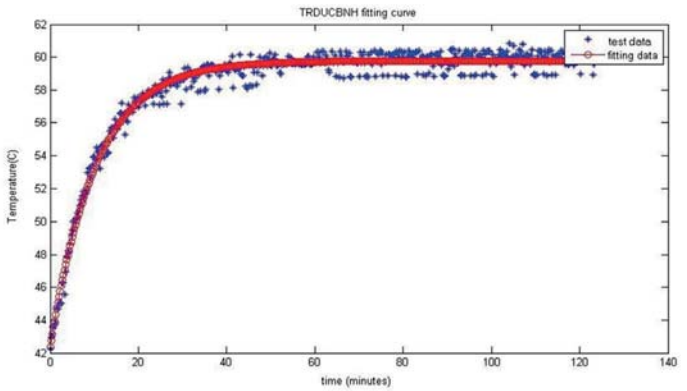

Figure 5: Temperature change from 25°C to 50°C

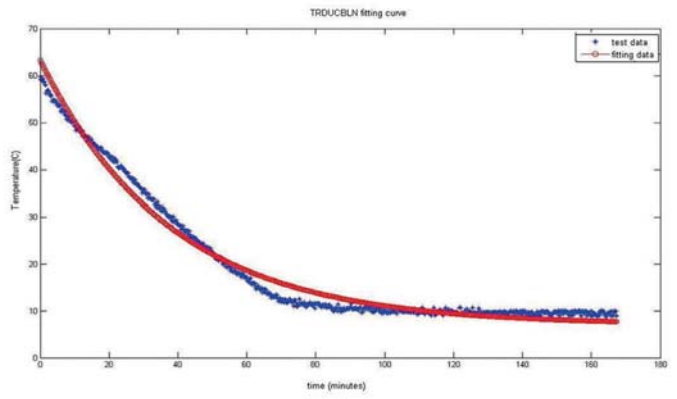

Figure 6: Temperature change from 50°C to -5°C

$$Tp = 59.77(1 - 0.29e^{-0.097t}) \quad (3)$$

The coefficient is then 0.9698, and the fitting curve is shown in Figure 5. When Tp reaches stable value, t = 54.75 minutes.

Furthermore, when the environmental temperature drops from 50°C to -5°C, the results at this test point become:

$$Tp = 7.0488(1 + 7.97e^{-0.0264t}) \quad (4)$$

The coefficient is then 0.9821; see the fitting curve in Figure 6. When Tp = 8, or near the stable value, t = 152.6 minutes.

We thus determine that when the environmental temperature rises, the temperature at the test point will increase correspondingly and reach a steady state in an hour. When the environmental temperature decreases, the temperature at the test point decreases and reaches a steady state in two and a half hours. In our experiments, each run of the high-low temperature test lasted at least five hours, but the period for each process can also be shorter.

Fixed Temperature Test

When the environmental temperature is fixed, the temperature at the test point will eventually reach a stable value, indicating a link between the test point temperature and that of the environment.

Four environmental temperatures have been selected for our test process. According to the results, the test point at the control board of HTSNK2 has the highest temperature. Table 1 shows its steady-state temperature at different environment temperatures.

We can derive Equation 5 for the Tp (test point temperature) and Te (environment temperature):

$$Tp = -0.00071Te^2 + 0.63Te + 43 \quad (5)$$

Based on this equation, we can determine Tp by the applied Te. For example, when Te = 85, Tp is 92. If Tp reaches the working temperature limit, it will trigger the alarm and shut down for protection. Of course, there are some variations since not all influencing factors have been considered here.

Temperature Distribution

When work temperatures are considered as a fourth dimension, the 4D (four-dimensional) steady-state base station temperature distribution can easily be obtained, and so can the temperature scope and changes at different environmental temperatures. ●

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DESIGNING MOBILE COMMUNICATION NETWORKS USING PROPLAB SOFTWARE

BY **YUNUS UCAR** FROM THE UNIVERSITY OF LEICESTER IN THE UK AND BOZOK UNIVERSITY IN TURKEY

Many parameters influence the design of mobile communication networks, including signal behaviour, propagation environment, operating frequency, transmitted power, type of antenna, its elevation angle – even the ionosphere. Network performance-predicting tools are of utmost importance when determining these factors, and programs such as Proplab and Winprop were developed specifically to analyse end-to-end signals.

The Effects On Radio Signals

Radio signals can be ground, direct or sky waves. Ground waves travel near the ground at short distances of about 80km over land and 300km over sea. A direct wave travels in a direct line of sight from transmitter to receiver, and a sky wave is transmitted toward the sky and reflected by the ionosphere to a distant receiver.

The ionosphere, sunspots, climate and atmosphere are environmental conditions that affect the propagation of radio waves. The ionosphere is the upper atmosphere, where there are large concentrations of free ions and electrons at high densities. This electron density is measured by the number of free electrons per cubic metre in the four layers of the ionosphere, D, E, F1 and F2.

Computer programs such as Proplab are used to predict the RF signal parameters for the ionosphere, including maximum usable frequencies (MUF), paths and ray lines.

Penetrable Signals

When designing a mobile communication network, parameters such as receiver and transmitter position, transmitter power, operating frequency and sunspot numbers are crucial. We set out to investigate the effects on these parameters of changing elevation angle, frequency and time of day. We simulated the propagation of HF signals between Uppsala, Sweden, and Leicester in the UK.

To investigate the effect of the elevation angle requires a ray-tracing model that determines how signals propagate into and through the ionosphere. We used such a model, with elevation angles varying from 0° to 40°; see the results in Figure 1.

As shown in Figures 2, 3 and 4, signals with elevation angle of 0°, 16° and 20° landed near the receiver while others far from it. It can also be seen that as the elevation angle increases, it becomes difficult for the signal to return to Earth, which means it may be lost altogether, depending on the distance from the receiver.

Furthermore, signals with elevation angles of 0°, 4°, 8°, 12° and 16° penetrated the ionosphere's E layer, whereas those with angles of 20°, 24°, 28°, 32° and 36° penetrated the F region. These results are important for mobile communications since they show which signals reflect back to Earth.

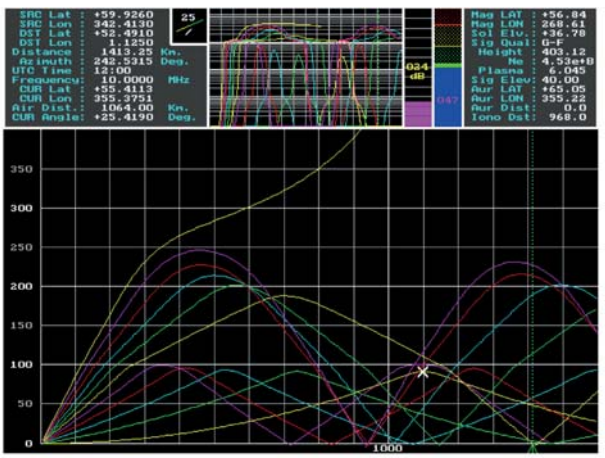

Figure 1: Signals linked to changing elevation angles

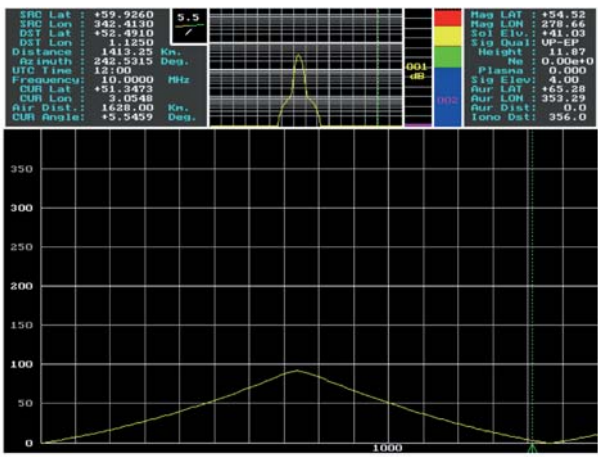

Figure 2: The signal linked to the elevation angle of 4° near the receiver

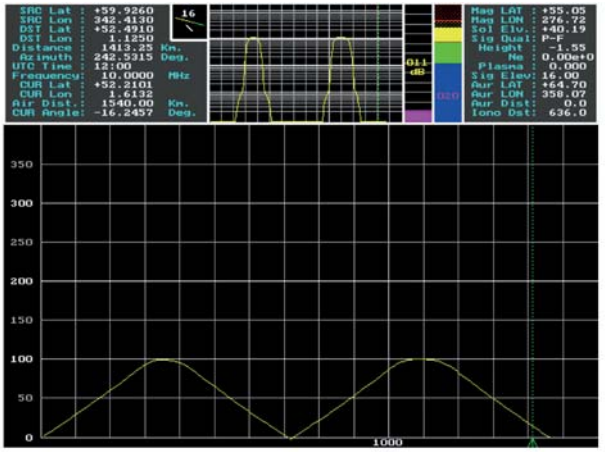

Figure 3: The signal linked to the elevation angle of 16° near the receiver

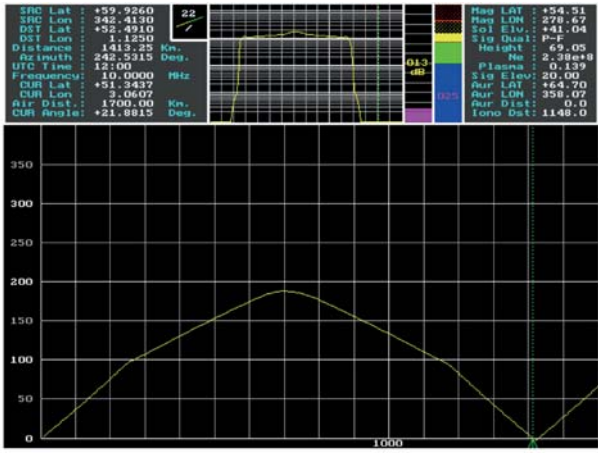

Figure 4: The signal linked to the elevation angle of 20° near the receiver

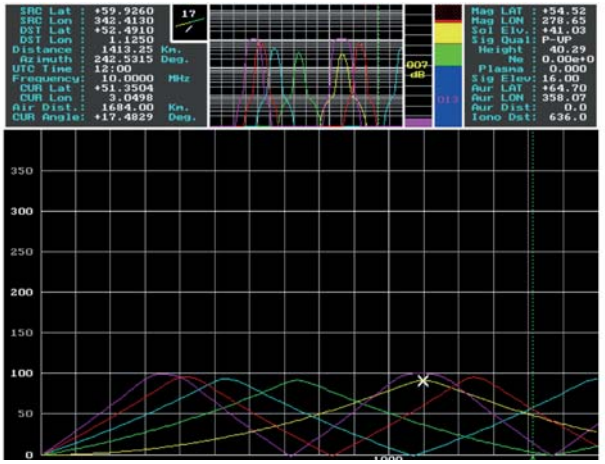

Figure 5: Different elevation angle signals that penetrate the E region

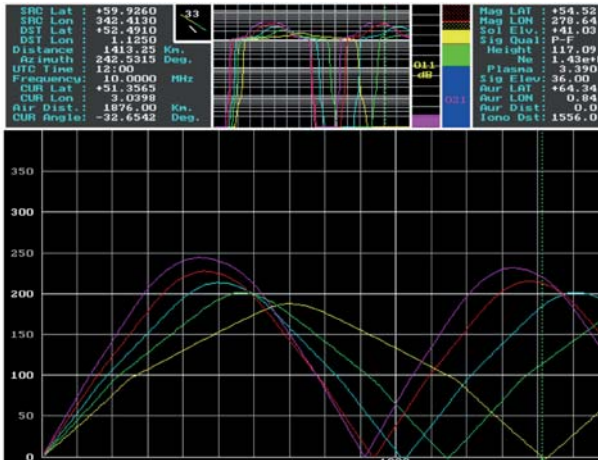

Figure 6: Different elevation angle signals that penetrate the F region

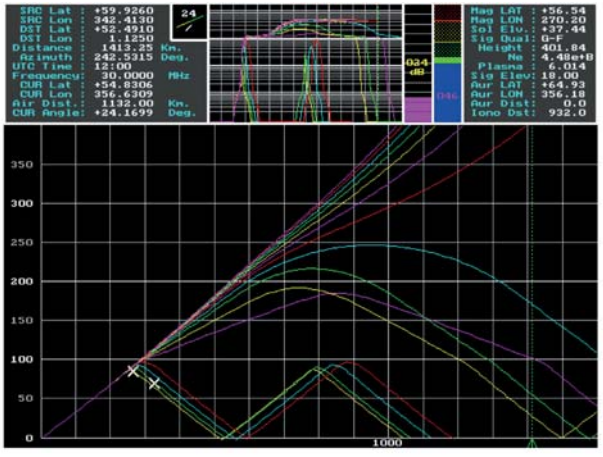

Figure 7: All signals at frequencies between 2MHz and 30MHz

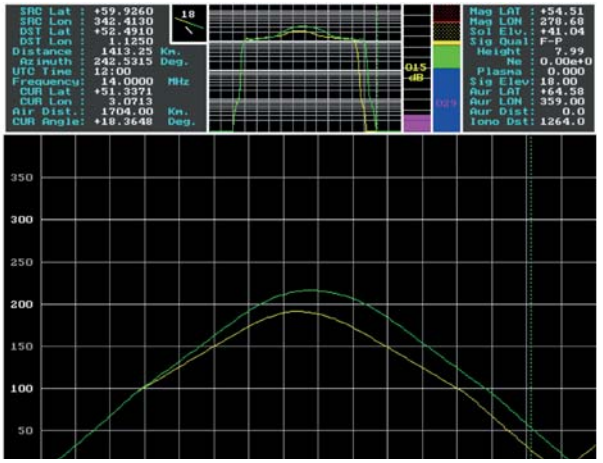

Figure 8: Signals near the receiver at frequencies of 12-14MHz

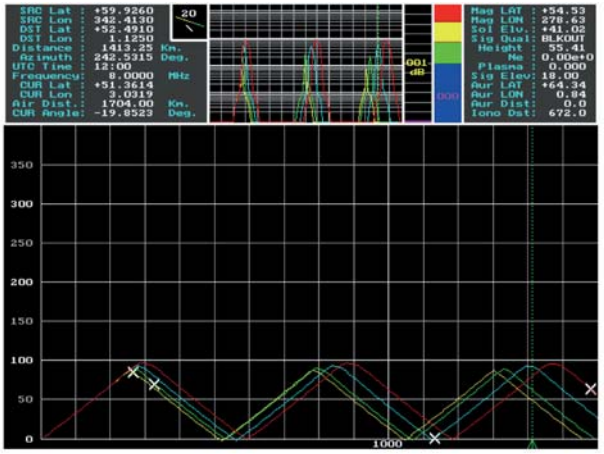

Figure 9: Signals penetrate the E region at frequencies of 2, 4, 6 and 8MHz

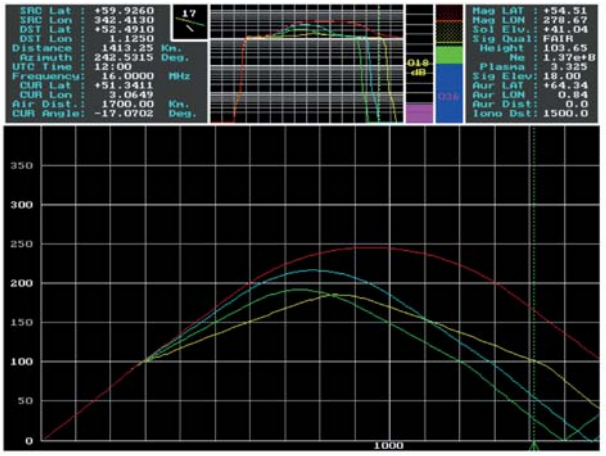

Figure 10: Signals penetrate the F region at frequencies of 10, 12, 14 and 16MHz

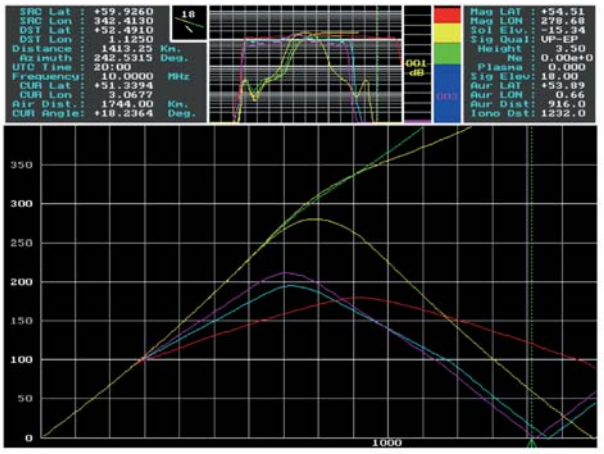

Figure 11: All signals at between 0 hours UT and 20 hours UT

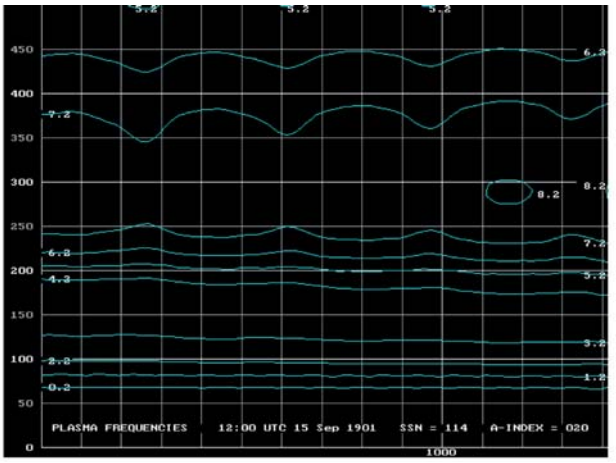

Figure 12: Plasma frequencies

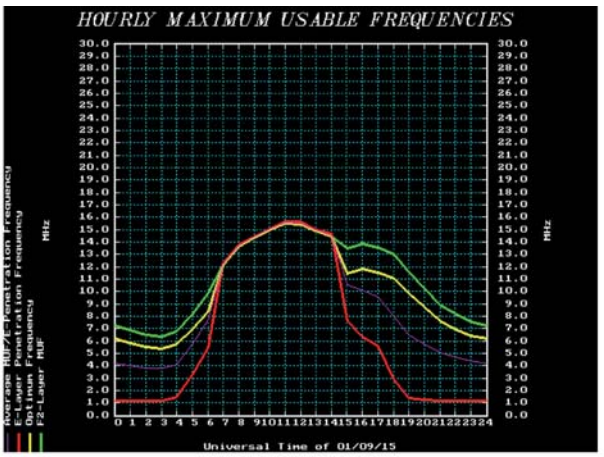

Figure 13: Maximum usable frequencies (MUF)

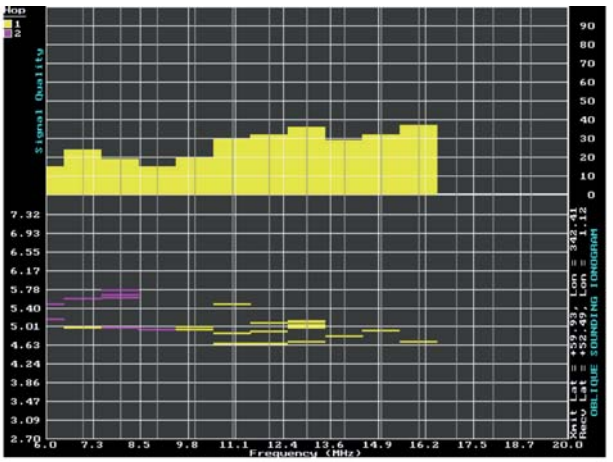

Figure 14: Ionogram for midday at 50km distance

Effect Of Signal Frequency

One of the important parameters in designing mobile communications systems is the signal frequency. Here, a ray-tracing model is used whilst changing the operating frequency, starting from 2MHz to 30MHz; see the results in Figure 7.

In the RF spectrum, the usable frequency range for radio waves extends from about 20kHz to over 30GHz. HF radios mostly use the spectrum from 1.6-30MHz, and most long-range communications are between 4MHz and 18MHz. Ionospheric conditions occasionally let in higher frequencies between 18MHz and 30MHz.

Figure 8 shows that signals landing near the receiver at 12-14MHz are the best operating frequencies for better quality of communications. For this frequency range, for the path from Upsala to Leicester, two signals landed near the receiver and the rest either far from it or passed through the ionosphere; the two signals that came through reflected from the E layer.

Signals at 2, 4, 6 and 8MHz penetrated the E region, and signals at 10, 12, 14 and 16MHz penetrated the F flayer. It might be said that the 2, 4, 6 and 8MHz signals reflected from the E layer and those at 10, 12, 14 and 16MHz passed through it and reflected from the F layer. The other signals passed through the ionosphere.

Time Of Day Affects The Signal

Another important parameter is the time of day. Because ionisation in the ionosphere changes during the day, we investigated this, starting at 0 hours UT (Universal Time, a standard based on Earth's rotation) until 20 hours UT; see the results in Figure 11.

Some frequencies are more suitable for night use, because the ionospheric layers absorb lower frequencies and reflect higher ones during daytime. At night, the ionosphere becomes thinner and reflects the lower frequencies, allowing the higher ones to pass straight through.

Figure 11 shows that at 0 hours UT and 12 hours UT ionosphere-reflected signals landed far from the receiver, whereas at 4 hours UT and 8 hours UT they landed near it. However, at 16 hours UT and 20 hours UT, signals passed through the ionosphere.

In the ionosphere, the D layer is the lowest region affecting HF radio waves. This layer reaches its maximum ionisation when the sun is at its zenith and dissipates quickly toward sunset. The E layer also reaches maximum ionisation at noon, and begins dissipating toward sunset, reaching minimum activity at midnight.

The F region consist of the F1 and F2 layers, where F1 is not significant for HF communications. The F2 layer reaches its maximum ionisation at noon and changes during the night, decreasing to a minimum before sunrise.

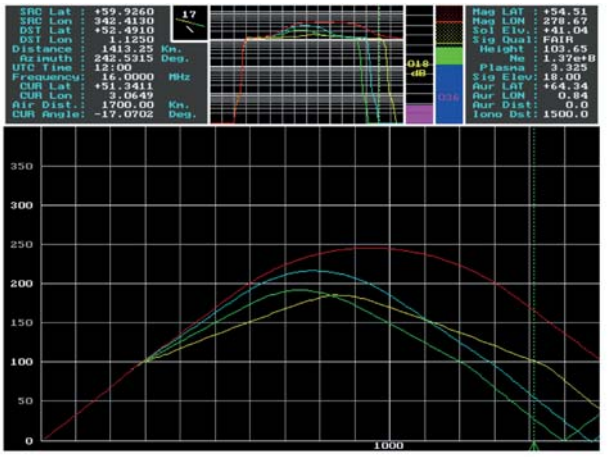

Figure 15: Detailed ionogram for midday at 50km distance

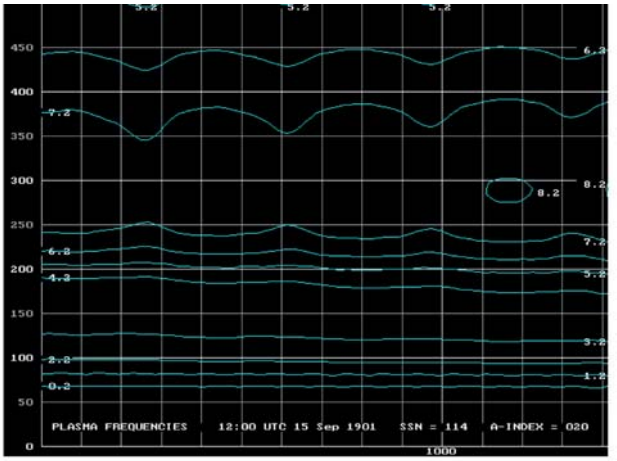

Figure 16: Ionogram for midday at 100km distance

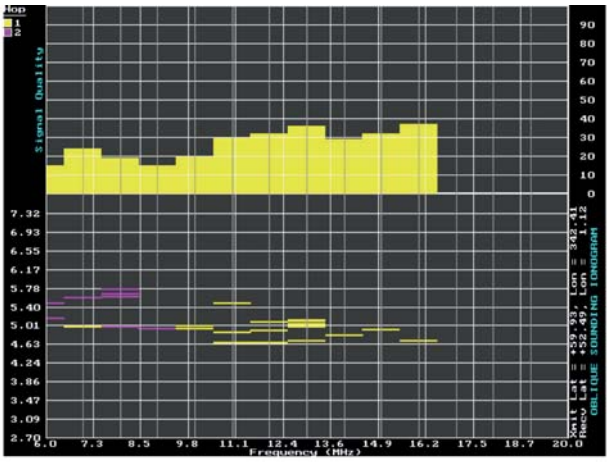

Figure 17: Ionogram for midnight

Plasma Frequency Map And MUF Graph

Critical frequencies are crucial in radio communications; these are the limiting frequency at or below which a wave component is reflected by an ionospheric layer, or above which it passes through it. Critical frequencies are used to detect maximum usable frequencies (MUF) for propagated radio waves and detect other ionospheric parameters.

The ionospheric layers E, F1 and F2 each have their own critical frequency. Maximum electron density occurs in the F2 layer, so this is the one used to determine MUF. Plasma frequency, or critical frequency, on the other hand, is the resonant frequency of the ionised gas; see Figure 12. Convention has it that the plasma frequency is 8.2MHz, with its highest centre point being at about 300km. However, it too changes with time of day, season and distance between transmitter and receiver.

For our model, the MUF is about 16MHz; see Figure 13. Figure 9 shows that for a fixed elevation angle of 18 degrees, the MUF is about 16MHz. This frequency differs from the penetration frequency by 2MHz (Figure 9), and the penetration frequency occurs after 16MHz.

Spectrum Analysis

Ionograms are produced by an ionosonde – a combination radio transmitter and receiver that transmits signals into the ionosphere and then measures the character of the returned signals. The signals are analysed with an oblique ionogram, at operating frequencies from 6MHz to 20MHz and an elevation angle from 2° to 45° at a distance of 50km to 100km.

Low-frequency signals are reflected by the ionosphere, giving a good understanding of the composition of the lower layers. As the frequency of the transmitter increases, the signals penetrate deeper into the ionosphere before they return to Earth. If the frequency exceeds the critical, the signal will reflect from the ionosphere.

Oblique ionograms (Figure 14) depict the ionosphere by measuring all received energy, from low to high frequencies. This helps determine the operating frequencies, MUF, minimum usable frequencies and so on.

Figure 14 shows that signal quality between 13MHz and 16MHz is good, but above 16MHz there's no signal. In addition, there's a nearly 4ms delay in signal reception from transmitter to receiver. For example, at 11.1MHz there are likely to be three rays, received at approximately 4.65ms, 4.85ms and 5.03ms, with a time difference of 0.38ms between the fastest and slowest arriving signal. Furthermore, the maximum usable frequency (determined from the oblique ionogram) is about 16MHz.

If the frequency and angle resolutions increase (through smaller steps), the ionogram becomes clearer (Figure 15); there is a small time difference between the two signals.

Figure 17 shows that signal quality weakens at midnight. Furthermore, comparing midnight and midday, the best signal is at 16MHz at midday, but 6MHz at midnight. ●

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NEXT-GENERATION SMARTPHONE CASINGS

DR TAMIM SIDIKI, GLOBAL MARKETING MANAGER FOR ELECTRONICS AT DSM, DISCUSSES THE TREND FOR NEW MATERIALS IN SMARTPHONES

Apple launched its first iPhone in 2007, kick-starting a whole new market. Ten years on, this market has reached maturity and has shifted into commodisation. Until now, the OEMs landscape has seen drastic changes, with well-known brands like Nokia and Motorola disappearing, and companies like Vivo and OPPO reaching the top five in the world due to their strong market positions in China. Even though these brands are still unknown in many countries, they are competing with Huawei to secure the third biggest market share after Samsung and Apple. Yet, performance, features and designs of the smartphone remain largely similar between all manufacturers.

Now the race is on for the next new thing to add to the smartphone, and OEMs are focusing on wearables and connected home features to capture market share. In 2017 and 2018, to make the smartphone an even closer companion to its users, the mobile industry will make incremental improvements to its performance, and add new hardware and software technologies such as flexible displays and artificial intelligence.

Metal Casings

For many years Apple favoured the aluminum smartphone body. With iPhone's popularity came a trend for metallic cases in aluminum, stainless steel, titanium and magnesium, all combining superior mechanical performance with valued aesthetic and feel. In most mid- to high-end models, metallic cases have replaced plastic housings altogether.

While the metals' intrinsic thermal conductivity helps spread heat from ever-more powerful processors, their electrical conductivity causes radio frequency (RF) attenuation and therefore weaker transmission and reception of radio signals. One way to overcome the electromagnetic interference (EMI) shielding issues of metallic casing is to ground the case, and make it an extension of the antenna.

Modern smartphones have multiple antennas: cellular, GPS, WiFi and Bluetooth. Smartphones have two cellular antennas, to ensure good reception, regardless of the absorption caused by hand-holding the device. The phone switches between these two antennas, depending on which one is offering better reception.

To ensure good reception efficiency in combination with the design, the metal casing is typically separated into three parts. The metal-body upper back of the phone is connected to the top antennas, and doubles as signal amplifier. The main body is grounded, and the bottom of the back enclosure is connected to the secondary antenna, again doubling as its amplifier.

To function correctly, the top and bottom antennas must be electrically isolated from each other, which is the main role of the plastic antenna separator.

The latest generations of iPhones, 6 and 7, have increased the width of these insulating separators and made them more RF-transparent, which increases reception sensitivity; increased thickness helps reduce the separator's capacitive leakage.

The insulation provides both electrical resistance and capacitance, and can conduct current through both paths. These separators therefore need a high resistance, to minimise leakage.

Figure 1: The evolution of substrates

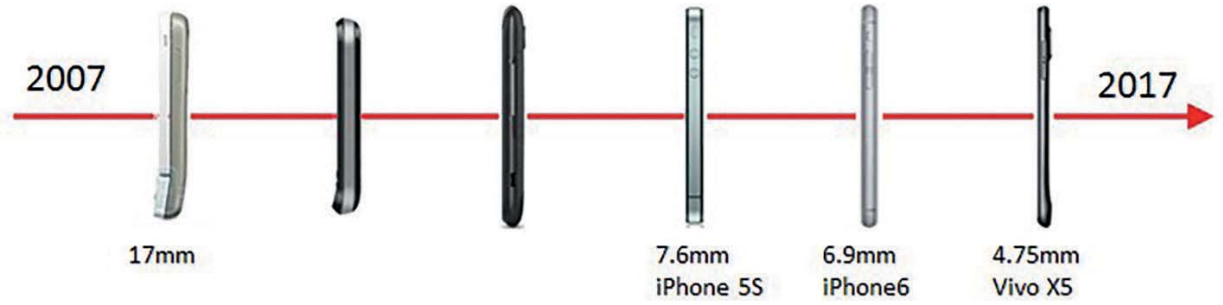


Figure 2: Smartphone thickness has decreased since the launch of the iPhone ten years ago

Capacitive power is frequency-dependent. With smartphones' increase in data rates, the increased separation directly contributes to less leakage through the insulator.

Glass Strength

Despite sophisticated engineering, the metallic casing is not ideal for RF design, particularly if frequencies continue to increase.

Since metal casings have become a common design choice, the material no longer serves as a differentiator among OEMs. The industry has seen a stronger shift to glass front- and back-covers in 2017. Unlike metal enclosures, glass covers support wireless charging and do not absorb magnetic resonances.

OEMs push the boundaries further, designing aesthetic smartphones that get thinner and thinner. The world's thinnest phone is currently the Vivo X5, at only 4.75mm; see Figure 2.

An all-glass smartphone housing may be an industrial designer's ambition, yet it may not have the required mechanical integrity needed to pass product tests, such as drop and tumble, necessary to ensure life-long reliability. As a result, we'll see high-end models with all-glass designs continue to use metallic frames for support and as antenna amplifiers to counteract RF attenuation linked to parts in the smartphone housings, such as printed circuit boards (PCBs), EMI shields and metallic coatings.

The selection of metal used for the frame has implications for the phone's mechanical integrity, weight, durability, finishing processes and effect; see Table 1. Aluminum is an attractive choice, due to its low density, recyclability and low cost of materials and fabrication; however, aluminum alloys exhibit long-term corrosion in metal frames.

Stainless steel alloys are capable of a wider selection of finishes than aluminum alloys, from matte to high gloss, from polished to brushed metal, and even fine airline-style finishes. Its surface can be treated with Vacuum Metallisation (VM), Physical Vapour Deposition (PVD) or Electrodeposition (ED).

PVD can also be considered as an alternative to nickel plating, but its waste treatment has environmental restrictions. Increased weight, due to higher density, may be a concern; however, its better mechanical properties also allow for reduced wall thickness, making the increase in device weight negligible.

If weight is a concern, titanium can also be considered.

New Demands For Metal-To-Polymer Bonding

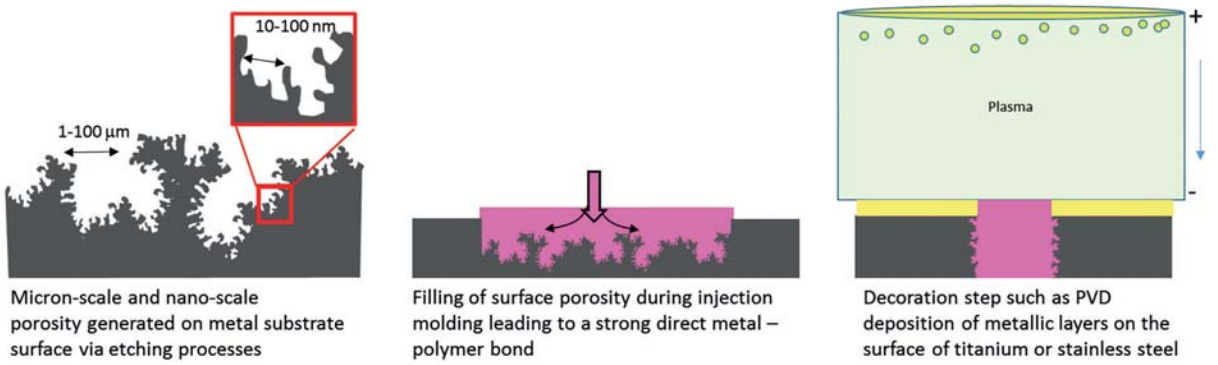
Nano Mold Technology (NMT) provides direct metal-to-polymer bonding, and is an important secondary process prior to decoration processes such as anodisation or PVD (Figure 3). NMT coats a specially textured metal surface with a polymer to generate a strong bond. The bond's strength is influenced by the metal surface, the processing conditions, or the properties of the compound.

Different substrates require different treatments to achieve a suitable surface texture, but the key characteristic of the surface texture is a multi-scale roughness that contains micro and nano features to allow for optimum polymer infiltration and interlock. It's important to achieve strong bonding that avoids trapped air, and prevents delaminating under stress or poor conditions.

PROPERTY	ALUMINUM	STAINLESS STEEL	TITANIUM
Density	2700 kg/m^3	8030 kg/m^3	4540 kg/m^3
Melt temperature	660 °C	1399 °C	1668 °C
Tensile strength	72 MPa	290 MPa	400 MPa
Elongation	60 %	55 %	27 %
Modulus of Elasticity	70 GPa	286 GPa	116 GPa
Corrosion resistance	Very good	Excellent	Excellent

Table 1: Alloy properties

Figure 3: Nano Mold Technology (NMT) processing steps:



Micron-scale and nano-scale porosity generated on metal substrate surface via etching processes

Filling of surface porosity during injection molding leading to a strong direct metal – polymer bond

Decoration step such as PVD deposition of metallic layers on the surface of titanium or stainless steel

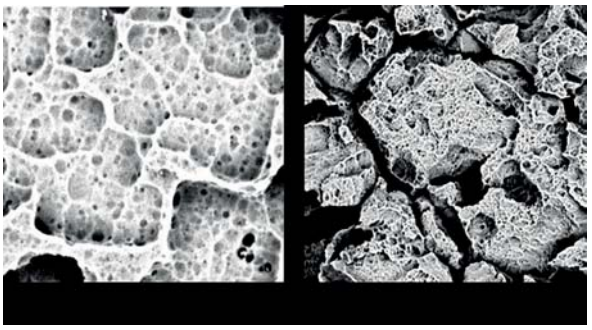


Figure 4: Scanning electron microscope images of aluminum (left) and stainless steel (right) substrate surfaces suitable for NMT bonding

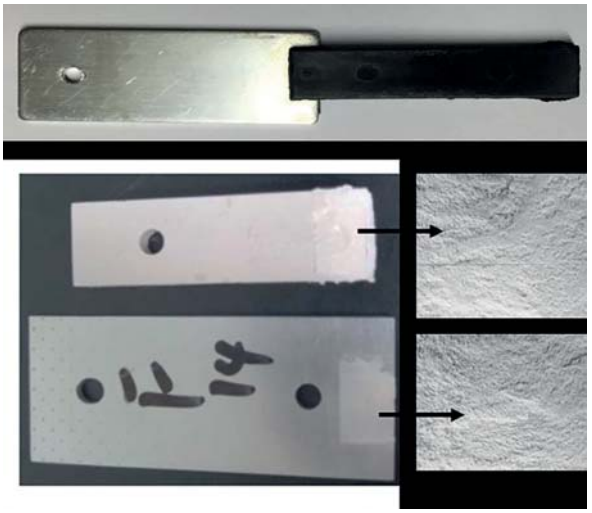


Figure 5: The top image shows a shear specimen using NMT to join the polymer to the metal substrate.
The bottom image shows the specimen after testing to demonstrate that performance and bond strength are not limited by the interface

The selection of stainless steel over aluminum poses additional challenges in selecting polymers for NMT. Aluminum is commonly anodised to protect the soft aluminum surface from scratches and corrosion, and to add colour, depending on the design. Since anodisation occurs after NMT, polymers capable of surviving this process must be used, such as polybutylene terephthalate (PBT), PBT/polyethylene terephthalate (PET) blends, or polysulfone (PSU).

While anodisation is ideal for aluminum, it is not suitable for stainless steel or titanium. These alternatives are prime candidates to provide structural integrity to next-generation smartphones, yet they require polymers for NMT that can withstand the higher temperature of processing techniques such as PVD; see Figure 4. PVD processing requires three hours at temperatures of 150-180°C, making the polymers used for NMT unsuitable. PPS is not an ideal material for external parts that need to meet high aesthetic requirements, due to its poor UV resistance and colourability.

OEMs must therefore select between higher temperature plastics, such as polyether ether ketone (PEEK), and the new and specialised PPAs with high glass-transition (T_g) and heat-deflection temperatures (HDT), with performance competitive with PEEK.

The Next Jump In Smartphone Innovation

As the smartphone matures, the push to innovate new design and features grows rapidly. Both small startups and global multinationals are putting huge efforts into new design concepts that allow differentiation in a lucrative multibillion-dollar market.

The trend in smartphones for 2017 has been to move away from aluminum bodies to glass or ceramic enclosures with metal frames made from materials with higher mechanical strength, such as stainless steel or titanium. These designs will rely on proven plastic-to-metal bonding techniques based on high-performance engineering plastics. ●

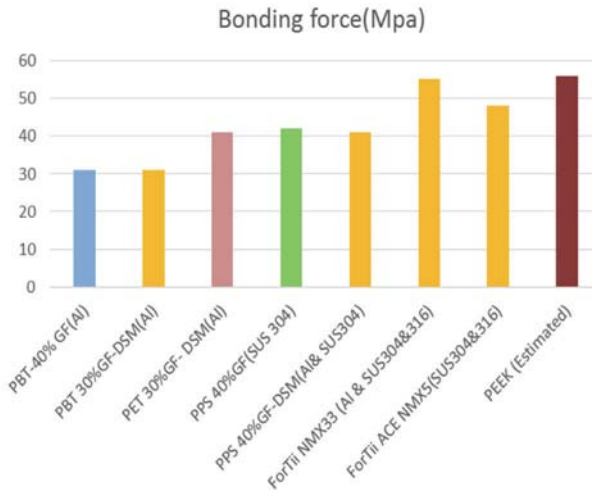


Figure 6: Bonding strength of common plastics to stainless steel via NMT processing

New High-Temperature Materials For NMT

DSM has developed a new material, based on its high-performance ForTii Ace polymer, suitable for NMT. ForTii Ace has the highest T_g of all polyphthalamides (PPAs), and its uniqueness is in the chemistry of the C4 molecules, which enable crystallisation behaviour superior to other PPAs. Additionally, the high T_g driven by aromatic content brings the temperature and chemical resistance in line to that of PEEK, while outperforming PEEK in stiffness at high processing temperatures. ForTii Ace's high polymer/molecular strength gives it the highest mechanical strength of all PPAs.

The material can achieve exceptionally high NMT bonding forces with titanium and stainless steel, due to its high polymer strength and processability. Control over flow and crystallisation is essential to good bonding via NMT, to allow sufficient filling of the micro-/nano-pores. Once the metal surface structure is sufficiently filled, crystallisation ensures excellent bond strength and high stiffness and strength of the compound.

For bonding to titanium and stainless-steel alloys, DSM has developed two dedicated NMT grades, ForTii NMX33 and ForTii Ace NMX5. For applications where dimensional stability, resistance to heat and UV of light colours or dielectrics play an essential role, the ForTii Ace polymer is an ideal material. Both grades are commercially available, enabling designers to realise next-generation all-glass casings or other creative metal-to-plastic bonds that exhibit the highest aesthetics and material performance.

NMT is an elegant technology for bonding metal to plastic (Figure 5), and is used in various applications and industries, including the aerospace and automotive sectors.

NEW PORTABLE RF ANALYSER PHASE STABLE CABLE ASSEMBLIES

Fairview Microwave, a supplier of on-demand microwave and RF components, has introduced a new series of rugged, portable, phase-stable RF analyser cables. Typical applications include handheld network analysers, basestation analysers, portable spectrum analysers, field testing, tower measurements, distance-to-fault measurements and site maintenance.

Fairview's 19 new, portable, RF analyser models provide optimal amplitude and phase stability with flexure. They deliver a maximum operating frequency of 27GHz and VSWR as low as 1.2:1, depending on the model. These rugged test cables are designed with a UV-resistant jacket, stainless-steel body connectors and silver-plated copper cable conductors. They feature a multi-layer armour for torque resistance and 1200psi of crush resistance, and they boast an operating temperature range of -55°C to +105°C. The cables are available with 7/16, N, SMA, TNC or 3.5mm connector options.

www.fairviewmicrowave.com

HIGH EFFICIENCY 3.0GHZ, 250W, 50V GAN HEMT

Wolfspeed extends its family of 50V unmatched GaN HEMT RF power devices by adding a 250W part with a frequency range up to 3.0GHz and the highest efficiency of any comparably-rated GaN device available. It enables RF design engineers to use fewer components to design smaller and lighter linear amplifier circuits for commercial and military wireless communications and S-band radar applications.

The new 50V GaN HEMT devices provide a combination of high power and high gain with high-efficiency operation, making it possible for RF design engineers to replace several lower-power GaN HEMTs or multiple silicon LDMOS devices with a single device in their power amplifier designs. Packaged in a four-leaded metal-flanged ceramic "Gemini" package, the new 250W GaN HEMTs operate efficiently at full rated power, reducing the need for complex thermal management systems.

www.wolfspeed.com

USB SMART MODULES FOR IN-VEHICLE CONNECTIVITY

Molex has merged automotive-grade durability with mass availability on its line of USB Smart Charge Modules. Manufactured specifically for vehicles that require a smart-charge USB module. Molex products feature state-of-the-art design to give users maximum performance.

Along with their unique design, USB Smart Modules were created to fit into limited spaces, making them ideal for a wide spectrum of vehicles, ranging from farm equipment and trains to cars, trucks and SUVs.

The modules are available in both single- and dual-port models, featuring over-voltage, over-current and short-circuit protection, and equipped with a 2.4A output current, a battery operating voltage of 9-16V. Additionally, each have an automotive-grade USB and are compliant to Apple MFI.

www.molex.com

SWIFT-DOCK INTERFACE ARRAYS FROM CODA SYSTEMS

The UK manufacturer of spring-loaded components Coda Systems showed its latest Swift-Dock connector assemblies for docking stations. Now there are three ranges of spring-loaded interface arrays from Coda Systems that are ideal for power and data transfer in devices such as handheld computers, medical instruments, data loggers and telecoms equipment.

Swift-Dock has a pitch of 7mm, whereas Swift-Dock-mini is available on a 3mm pitch. Both families are available in 2-, 3-, 4-, 5- and 6-pin configurations and can handle XA. Each unit comes as a pair of complete arrays, ready-fitted with spring-loaded contacts on one side and contact lands on the other, although each side is available separately. The PCB can be supplied with or without a connector.

Swift-Dock-Power has been designed for use in applications up to 10A.

www.coda-systems.co.uk

PANASONIC'S NEW HIGH-PERFORMANCE POWER RELAY DZ-S

Panasonic's DZ-S relay has been specially developed for switching the main power supply from the energy supplier to the consumer, one of the main functions in smart meters.

Besides the market for smart meters, the relay is ideal for any application where currents up to 90A have to be switched, such as in building and industrial automation markets.

As proven by conformity to the IEC 62055-31 UC3 standard, the newly-developed relay handles short circuits up to 3000A. Moreover, this latching-type relay helps save energy for the entire application.

Its compact design (30mm x 38.5mm x 17.5mm) and low coil power dissipation of 1.5W for the 1-coil latching type or 3W for the 2-coil latching type make this relay extremely attractive for energy-efficient applications.

www.panasonic-electric-works.co.uk

NEW AUTOMOTIVE BIPOLAR STEPPER MOTOR DRIVER IC

Allegro MicroSystems Europe has introduced a new automotive bipolar stepper motor driver IC or dual DC motor driver IC, designed for pulse-width-modulated (PWM) control of low-voltage stepper motors and dual or single high-current DC motors.

Allegro's AMT49702 is capable of output currents up to 1A per channel and operating voltages from 3.5-15V. Key applications include: heads-up-display (HUD) – mirror positioning and dust cover, navigation – screen lift, driver attention monitor – camera movement or focus, and steering wheel feedback – vibration alert.

The AMT49702 is an automotive-grade device, tested across extended temperature and voltage ranges to ensure compliance in automotive or industrial applications. An output fault flag notifies of a TSD or overcurrent protection event.

www.allegromicro.com

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