May 2018
Volume 124
Issue 1983
£5.90

www.electronicsworld.co.uk

Electronics WORLD

THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

Special Report:
Low Power Design:

- New field-programmable analogue array
- Line-based compressive sensing
- Energy harvesting

ANALOG DEVICES | POWER BY LINEAR

INSIDE THIS ISSUE

Latest
- Silicon breakthrough will lead to new high-performance bendable electronics

Embedded
- MicroPython and the Lonely32

Digitisers
- Using probes and sensors with modular digitisers

Also inside:
* CURRENT-MODE FULL BALANCED NTH-ORDER LEAPFROG LADDER FILTER

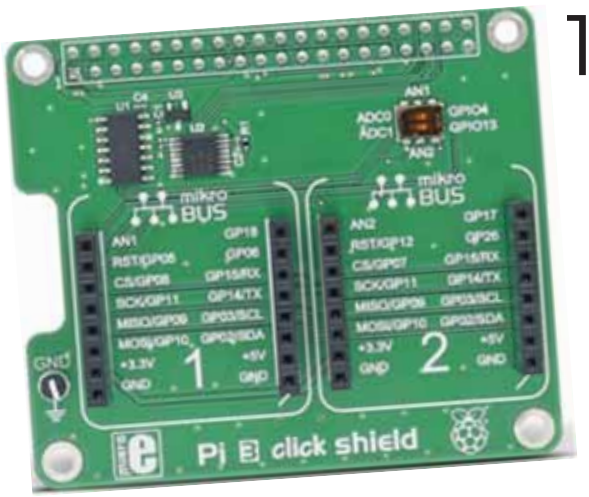
CONTENTS

REGULARS

04 > **Trend**
Future trends in the battery industry

05 > **Technology**

42 > **Products**



12

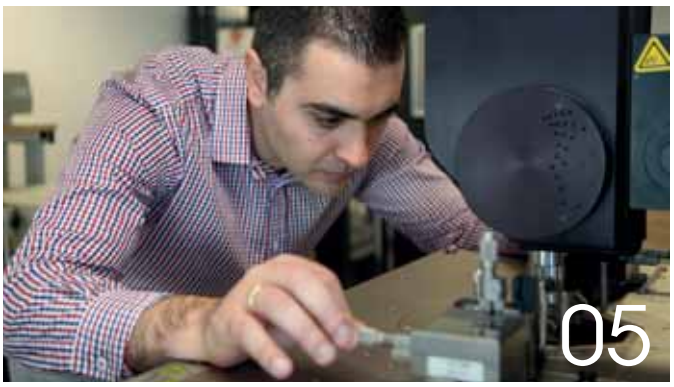
COLUMNS

06 > **Digitisers**
By Oliver Rovini and Greg Tate, Spectrum Instrumentation

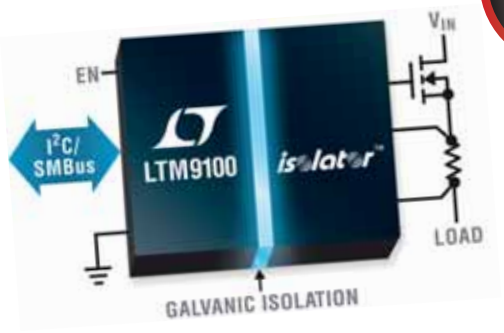
08 > **PCB cleaning**
By Mike Jones, MicroCare

12 > **Embedded design**
By Dr Dogan Ibrahim, Near East University, Cyprus

16 > **MCUs**
By Lucio di Jacio, Microchip Technology



Cover supplied by ANALOG DEVICES
See p10-11



FEATURES

19 > **Micropower zero-drift op-amp enables wireless current sense**
By Kris Lokere, Strategic Applications Manager, Signal Conditioning Products, Analog Devices

22 > **CDTA-based resistorless current-mode full balanced nth-order leapfrog ladder filter**
By Jun Xu, Hunan University, China

26 > **Line-based compressive sensing for low-power visual applications**
By Mansoor Ebrahim, Sunway University, Malaysia, and Syed Hasan Adil, Daniyal Nawaz and Kamran Raza, Iqra University, Pakistan

30 > **Design of low-power DC-DC converters for energy harvesting**
By Maurizio di Paolo, Technical Writer based in Italy

33 > **A fully-restored 26-T full adder for energy-efficient arithmetic applications**
By Dr. Shabbir Majeed Chaudhry, Assistant Professor, Department of Electrical Engineering at the University of Engineering and Technology in Taxila, Pakistan

37 > **Applications for a new field-programmable analogue array based on current differencing transconductance amplifiers**
By Haizhen He and Rongming Luo, Hunan University, Changsha, China

FUTURE TRENDS IN THE BATTERY INDUSTRY

One could almost see the parallels between diamonds and batteries. A diamond is formed under extremely high pressure and is the world's most valuable gemstone. Likewise, battery technology is developing under increased pressure from end users and manufacturers, while remaining one of the most valuable components in electronic devices.

Three top trends are shaping the way batteries are developed: Safety concerns are leading battery manufacturers to re-think their active materials and cell construction techniques. Increase in wearable devices is driving the trend for batteries with increased power density, and the growing battery 'grey' market is making battery manufacturers conscious of end-user safety.

Safety Concerns

Recent battery scandals have caused concern about the safety of lithium-ion batteries. The US Federal Aviation Administration (FAA) recently prohibited certain smartphones on their flights, which were at risk of exploding. Design flaws in the battery caused the separator between the positive and negative tabs to break down. This meant the battery short-circuited, overheated, and in some cases caught fire. Following this controversy, researchers at Stanford University suggested introducing flame-retardant material into Li-ion batteries to prevent fires caused by overheating.

Electronic device Original Equipment Manufacturers (OEMs) need to ensure that the batteries they are purchasing meet the latest international standards for safety and performance, which means checking that requirements are met both at a cell- and battery-level.

Suppliers of batteries should work under strict design control because if a seemingly trivial design change has not been properly validated it can have damaging consequences further down the supply chain.

Wearable Devices

The Consumer Electronics Show (CES) in Las Vegas last January saw an abundance of wearable health and fitness devices. From sleep-tracking headphones to an infrared thermometer with a smartphone app, the show confirmed that the wearable device market continues to grow. Now, battery manufacturers face the challenge of making smaller batteries that deliver longer runtimes.

To meet this demand, scientists have recently created what has been dubbed the "bendy" battery, a flexible battery containing aluminium and graphite foam, surrounded by liquid salt. The battery has attracted a lot of interest from manufacturers for its lightweight design and potential for use in powering flexible displays. However, there is still a long way to go, as the bendy battery currently only delivers half the voltage of a lithium-ion battery.

The 'Grey' Market

The use of batteries for life-critical devices, whether in the medical or military sector, has led to increasing safety and security concerns. This is combined with the global rise in counterfeiting and the battery 'grey' market, with counterfeit goods accounting for almost 2.5% of global imports.

Counterfeit batteries pose a risk of overheating or catching fire, as well as not delivering a reliable performance. To counter this, some battery makers, such as Accutronics, use algorithmic security in their smart batteries; meaning, if a counterfeit battery is inserted into a properly-equipped device, it can display a warning message or shut down completely.

Counterfeit batteries often look identical to branded batteries, so OEMs must look for security features such as this to protect their devices from battery counterfeiting.

Meeting Needs

The demand for more energy-dense yet smaller batteries means that the battery market is looking for ways to stay ahead of the needs of device OEMs. Also driven by concerns over counterfeiting and the grey market, battery manufacturers are looking to innovate sustainably and safely. It is clear that this pressure is creating a 'diamond' of the global battery market, expected to be worth over $17bn by 2021. ●

By Michele Windsor, global marketing manager, Accutronics (www.accutronics.co.uk)

EDITOR: Svetlana Josifovska
Tel: +44 (0)1732 883392
Email: svetlanaj@electronicsworld.co.uk

SALES: Suzie Pipe
Tel: +44 (0)20 8306 0564
Mobile: +44 (0)7799 063311
Email: suziep@electronicsworld.co.uk

DESIGN: Tania King

PUBLISHER: Wayne Darroch

ISSN: 1365-4675
PRINTER: Buxton Press Ltd

SJP business media

2nd Floor,
52-54 Gracechurch Street,
London, EC3V 0EH

SUBSCRIPTIONS:
Subscription rates:
UK - 1 year digital only £53.00+VAT
UK - 1 year print and digital sub £68.00
UK - 2 year print and digital sub £109.00
UK - 3 year print and digital sub £143.00
International - 1 year digital only £53.00
International - 1 year print and digital sub £164.00
International - 2 year print and digital sub £290.00
International - 3 year print and digital sub £409.00
Tel/Fax +44 (0)1635 879361/868594
Email: electronicsworld@circdata.com
www.electronicsworld.co.uk/subscribe

Follow us on Twitter @electrowo

Join us on LinkedIn

SCIENTISTS MANIPULATE THE MEMRISTOR TO CREATE NEW TYPE OF ELECTRONICS

Scientists at the University of Southampton believe that memristors could start a new era of electronics. Being smaller and simpler than transistors, with lower energy and the ability to retain data by 'remembering' the amount of charge that has passed through them, memristors can bring computers that switch on and off instantly and never lose data.

The researchers have found a way to alter memristor resistance and make it store up to 128 discernible memory states per switch, almost four times more than previously reported. They managed to alter the memristor's resistance by reconfiguring its core component, an oxide material.

"This is a really exciting discovery, with potentially enormous implications for modern electronics. By 2020 there are expected to be more than 200 billion interconnected devices within the Internet of Things ecosystem, generating an incredible amount of data that will need processing," said Themis Prodromakis (pictured), Professor of Nanotechnology and EPSRC Fellow at the University of Southampton.

Professor Themis Prodromakis, University of Southampton

Memristors are a key enabling technology for next-generation chips, which need to be highly reconfigurable yet affordable, scalable and energy-efficient.

Prodomakis added: "Working with industry, we'll bring innovations into new electronic systems that require bespoke customisation, systems that can be employed in inaccessible environments like inside the human body, space or other remote or harsh locations. At the same time, this technology is ideal for developing novel hardware that can learn and adapt autonomously, much like the human brain."

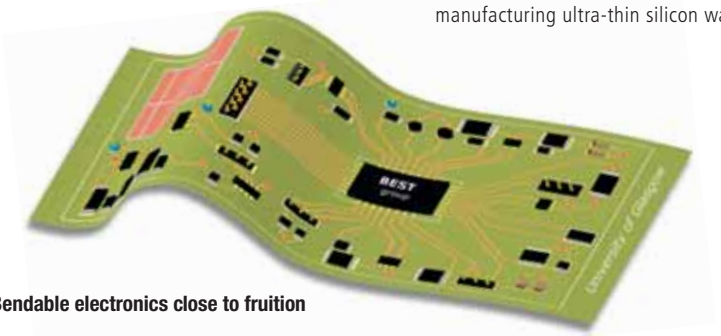
SILICON BREAKTHROUGH COULD LEAD TO HIGH-PERFORMANCE BENDABLE ELECTRONICS

University of Glasgow engineers have developed a new method of creating bendable silicon chips that could pave the way for a new generation of high-performance flexible electronic devices.

The University's Bendable Electronics and Sensing Technologies (BEST) scaled up the established processes for making flexible silicon chips to the size required for delivering high-performance bendable systems in the future.

They made an ultrathin silicon wafer that delivers high-performance computing yet remains flexible. The process has been demonstrated with wafers four inches in diameter, but it can be implemented for larger wafers as well. The team transferred several different types of ultra-thin silicon chips of around 15 microns thick onto flexible substrates; for comparison, a human blood cell is about five microns across.

The scale was proven to be sufficient for manufacturing ultra-thin silicon wafers capable of delivering satisfactory computing power.



Bendable electronics close to fruition

"Silicon-based circuits have advanced in complexity with remarkable speed since their initial development in the late 1950s, making today's world of high-performance computing possible. However, silicon is a brittle material that breaks easily, which makes it very difficult to use in bendable systems on anything other than nano scale," said Professor Ravinder Dahiya, head of the BEST group.

Flexible electronics is projected to be worth $300bn by 2028. These systems have many potential applications, including implantable electronics, bendable displays and wearable technology that provides constant feedback on users' health. The BEST group has already made significant progress in wearable technology, including a flexible sensor with accompanying smartphone app that provides feedback on the pH levels of users' sweat.

Using probes and sensors with modular digitisers

BY **OLIVER ROVINI** AND **GREG TATE**, SPECTRUM INSTRUMENTATION

Sensors or transducers convert physical phenomena into electrical signals, and probes convert signal levels, change impedances and offer convenient connections; examples include current probes, accelerometers and photomultipliers.

Probes

Most passive oscilloscope probes work with digitiser inputs, but they change the circuit whilst probing.

Figure 1 shows a 1MΩ input of a digitiser connected to a measurement point using a coaxial cable. A digitiser's input capacitance is typically about 35pF, and a coaxial cable 10-30pF per foot, which means the total capacitance of this setup is about 95pF, hence the capacitive reactive (Xc) for a 95pF capacitance at 10MHz is:

$$Xc = \frac{1}{2\pi fC}$$

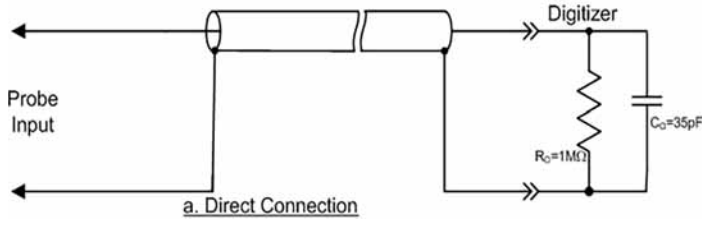


Figure 1: Simplified schematic showing a direct connection using a coaxial cable

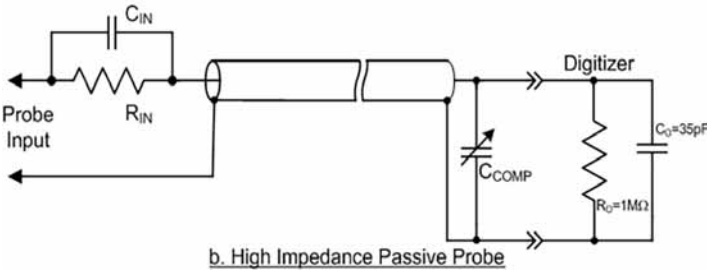


Figure 2: Simplified schematic of a 10:1 high-impedance passive probe

At 10MHz, 95pF results in an impedance of 168Ω, which can significantly attenuate the measured voltage. This means that using a shielded cable to connect the digitiser to the device being measured loads down the circuit with this capacitance.

High-Impedance Passive Probes

High-impedance passive probes use a capacitively-compensated voltage divider that divides the amplitude by a factor of (typically) ten to one (10:1). This will result in an input capacitance of 10pF minimum with times-ten attenuation, increasing the probe loading resistance by approximately 10x; see Figure 2.

Input capacitance can be further reduced by increasing the probe attenuation, but this will reduce the signal coming into the digitiser and make it more difficult to measure small signals. In practice, 10:1 attenuation generally represents a good compromise between signal amplitude and loading impedance.

A high-impedance passive probe can have a bandwidth of up to 500MHz, and at higher frequencies even a lower value of probe capacitance can be too much. At 500MHz with a 10pF probe capacitance, the input impedance is about 32Ω, loading down all but the lowest-impedance circuits; at lower frequencies, this is less of a problem.

The probe also attenuates the input voltage by a factor of 10, which must be accounted for in the digitiser output.

Transmission-Line (Low Capacitance) Probes

High-frequency measurements require probes with very low input capacitance, which can be drastically reduced by considering the coaxial cable as a transmission line. If the digitiser input is terminated in 50Ω, the impedance looking into the probe end of the cable is a constant 50Ω, independent of frequency. This very-low loading impedance can be increased using a voltage divider. A 450Ω series-resistor will divide the amplitude ten times and result in a relatively constant loading impedance of 500Ω. A low capacitance or transmission-line probe (Figure 3) uses a terminated transmission line.

The input capacitance of a transmission-line probe such as this is quite low, typically about a fraction of a pF; however, the limiting factor with this probe is the low input resistance. For a 10x probe, the input resistance is only 500Ω and may load circuits too heavily.

Transmission-line probes find application in high-frequency designs, where circuits normally run on 50Ω traces.

Active Probes

An active probe uses a compensated voltage divider driving an amplifier. The buffered output of the amplifier drives a coaxial cable terminated in its characteristic impedance just like the transmission-line probe. Here, it also isolates the probe from the cable's capacitive loading and the input circuitry of the digitiser.

Active probes are normally powered and controlled by an oscilloscope; to use them with a digitiser, the probe needs a standalone power supply and, if necessary, a control interface.

Selecting Passive Probes

High-impedance passive probes are available in several attenuation factors, with 10:1 and 100:1 the most common. Working into the digitiser's 1MΩ input termination, they offer 10MΩ or 100MΩ input resistance. Digitisers with 14- to 16-bit resolution are well matched to the 100:1 probes, since they have sufficient dynamic range to show small signals after the probe attenuation.

Probes must be matched to the input capacitance of the digitiser. For a digitiser channel with a 35pF input capacitance, a probe with a compensation range covering that capacitance must be used.

Most high-impedance passive probes use BNC connectors. It's great if the digitiser has BNC inputs, but BNC connectors need a lot of space and digitiser front panels are often very small, so an adapter should be used. For example, if the digitiser uses SMA connectors, then an SMA-to-BNC adapter is required to mate with the probe.

It's great if the digitiser has BNC inputs, but BNC connectors need a lot of space and digitiser front panels are often very small, so an adapter should be used

Transmission-line probes work into the digitiser's 50Ω input termination. Because these probes generally support bandwidths into the GHz range, they usually use SMA connectors.

Sensors

Sensors or transducers are sensitive to a physical property and convert it into a voltage level proportional to the value of the property being measured. A common example is a current probe, which converts current to voltage, with the voltage level proportional to the measured current level.

Matching a sensor or transducer to the digitiser requires knowledge of the sensor output range, output impedance, bandwidth and sensitivity. The output range must be within the digitiser's voltage range; if not, attenuators or amplifiers may be required to bring it within this range.

Most sensors are designed to work into a fixed impedance. Like other measuring instruments, digitisers generally offer input terminations of 1MΩ or 50Ω. Most broadband transducers are designed to match 50Ω load impedance. Lower bandwidth sensors may require a 1MΩ load. Some specialised transducers can be designed to work into other impedances, such as 75 or 600Ω. In these cases, matching pads may be required along with suitable adjustments to the sensor sensitivity.

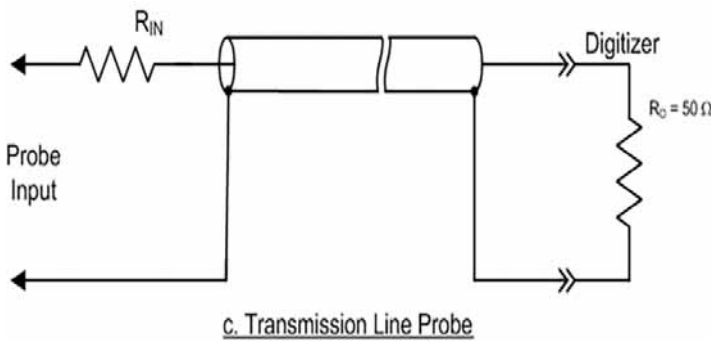


Figure 3: Simplified schematic for a 10:1 transmission line probe operating into 50Ω input termination of a digitiser analogue channel

The bandwidth of the digitiser should be significantly greater than the bandwidth of the sensor to avoid reducing the effective bandwidth of the sensor-digitiser system. A digitiser-to-sensor bandwidth ratio of over 7:1 will result in a 1% or less uncertainty in amplitude measurements.

Sensitivity is the ratio of the given value of the sensor's electrical output to the equivalent measured property. For instance, an accelerometer's sensitivity may be specified as 10mV/g, which means for a measured physical input of 1g, the transducer produces a 10mV signal.

Knowledge of the sensitivity is important when calibrating the digitiser to read in the measured units rather than electrical units.

Most transducers require a separate power source, which is normally external to the digitiser. ●

Working the wetting index for the right cleaning choice

BY **MIKE JONES**, VICE PRESIDENT, MICROCARE

Choosing the correct cleaning chemical for a job can be confusing, especially with so many options to choose from. Fortunately, there's a 'secret weapon' that can help predict how good a cleaner can be, called the 'wetting index'. This index is a measure of a fluid's ability to clean complex shapes, calculated quickly from the product's specification or datasheet.

"Wetting" refers to the liquid's ability to remain in contact with a surface; there's a general rule that "it can't clean if it can't wet", hence better wetting means better cleaning. The relative capacity of a fluid to wet a surface can be measured with the wetting index, which combines the relevant chemical characteristics to predict the quality of the cleaning.

Modern planet-friendly solvents do a much better job cleaning small, delicate or intricate shapes

Evaluating a cleaning solution's ability to penetrate between parts is particularly important in the electronics industry, where components are getting smaller and more complex. More densely populated circuit boards make managing faults, quality and product longevity highly challenging. This is the reason so many companies consider their PCB cleaning a mission-critical process: if the cleaning is not effective, the device will simply not function reliably over its required life. It is also important to remember that wettability should be considered even for relatively flat surfaces, since agents with better wettability will penetrate more layers of soil and better lift particles off surfaces.

Accessing the 'Wet Index'

As Figure 1 shows, the cleaning abilities of water are not sufficient for today's modern electronics. Although water-based cleaning was once the preferred choice, this perception has changed, and many manufacturers are now opting for solvent cleaning because they find it more effective, flexible, less expensive and more suitable for cleaning smaller spaces. Water has a very poor wetting index, a function of its inherent molecular structure, whereas modern planet-friendly solvents do a much better job of cleaning small, delicate or intricate shapes.

The surface tension of water is the highest of any cleaning agent available. The high surface tension results in a low wetting index — a score of only 14. For modern, non-flammable solvents it is 100 or higher, making solvent cleaning faster, more consistent and easier to use.

Solvents outperform other cleaning methods because of the very-low surface tension, high density and low viscosity of the different fluids:

- Low surface tension means the solvent can get into tight spaces more easily than solvents with high surface tensions (like aqueous systems).
- A heavy solvent can literally 'float away' contamination that other types of cleaning agents cannot move.
- A solvent with low viscosity flows in and around objects more effectively than solvents with high viscosity due to their greater fluid consistency.

Combining the density, viscosity and surface tension of a solvent into an index score gives a number on the wetting index. The higher the score, the better the cleaning.

The formula for calculating the wetting index is:

(Density x 1000)

(Surface Tension x Viscosity)

To improve the wetting index score of water-based cleaners, a surfactant can be added to lower the surface tension; but, even then, the surface tension will still be twice that of any solvent.

The viscosity of water or other inefficient cleaners like Isopropyl Alcohol (IPA) also works against good cleaning. Higher viscosities mean the solvent will not flow into tight spaces easily, and if water gets into small crevices it may not come out, resulting in an ineffective cleaning effort. Modern solvents are heavier – typically 20-30% heavier than water, and over 50% heavier than alcohol, which means solvents can get under particulates and lift them off the surface.

Working out the wetting index scores will give a clearer indication of a cleaner's ability to do its job well. Knowing the score through a simple calculation will save time and money, since the right cleaning solution will be chosen, and clean effectively first time. ●

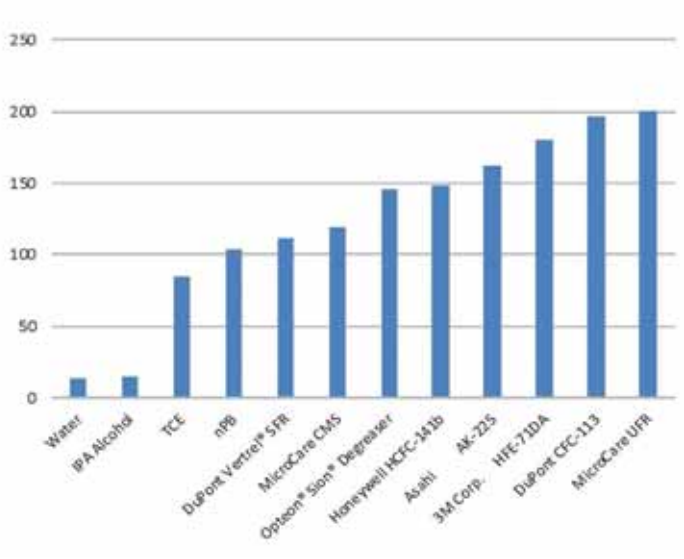


Figure 1: Wetting abilities of water and other solvents

SWITCHING AND MONITORING HIGH-VOLTAGE DC POWER SUPPLIES

By Pinkesh Sachdev, Product Marketing Engineer, Power by Linear Products, Analog Devices

DC power supplies in the hundreds of volts are not as uncommon as one might think. An application that may first come to mind is electric vehicles where Li-Ion battery stack voltages range up to 400V. But some lesser-known high-voltage applications are in modern fighter aircraft, such as the F-22 Raptor and the F-35 Lightning II, which are primarily powered from 270V DC for faster and precise performance.

Large solar arrays can output 600V or higher, while rectifying AC voltages in industrial motor drives yield DC voltages ranging from 170-680V. And for many years, there has been research and development to move power distribution within a data centre from AC to high-voltage DC (380V or ±190V), lowering power conversion steps, facility footprint and operational costs while easing integration with renewable energy such as solar.

Distributing power at higher voltages lowers current levels, reducing resistive losses (I^2R), which can be used to reduce cabling weight. All of these high-voltage supplies need to be switched on or off and soft-started into loads. For energy monitoring and optimisation, it is essential to digitally monitor the voltage and current flowing on these high-voltage buses. Any circuit controlling these supplies needs to be galvanically isolated for operator safety and to protect the low-voltage electronics from the dangerously high voltage.

Methods to Control Inrush Current & Monitor Power

When designing high-voltage supplies, an important goal is to safely control the startup inrush current into the capacitive load, e.g. the DC bus capacitors following a typical bridge rectifier. A simple method to lower inrush current is by using negative temperature coefficient (NTC) thermistors, also known as inrush current limiters, or ICL (Figure 1a). These thermistors start with high resistance (e.g., a few ohms) at room temperature before the supply or load is turned on; the high resistance limits the inrush current at turn-on. As current flows, the thermistor heats up and its resistance drops by one to two orders of magnitude (by 10-100x to below an ohm). These thermistors cost anywhere from $0.13 to $7 each, depending on current and resistance ratings.

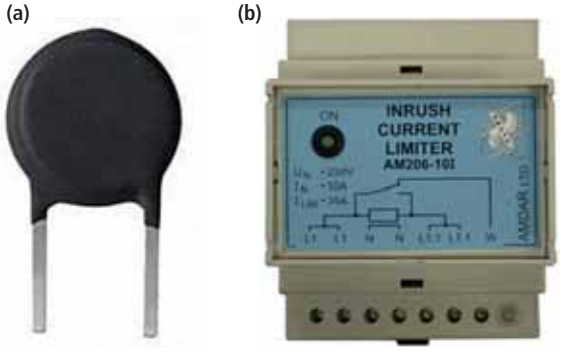


Figure 1: Inrush control limiters: (a) negative temperature coefficient (NTC) thermistor; (b) step-start relay

While simple to use, one problem is that a quick power cycling (on-off-on) may not limit inrush on the second power-up if the thermistor didn't have sufficient time to cool down to the high resistance state. NTC thermistors suffer from wide tolerances (±25%), and since the inrush current is tied to the steady state current through the resistance drop ratio, the inrush cannot be flexibly adjusted to arbitrarily low levels. ICLs find applications in vacuum cleaners, fluorescent lamps and switched-mode power supplies, reducing inrush to the bridge rectifier's DC bus capacitors.

To overcome the NTC thermistor downside of no inrush limiting on a quick restart, a shorting relay is used in parallel with the resistor. This is known as a step-start relay (Figure 1b). At turn-on, the parallel relay is open and inrush is limited by the resistor. A timer is also started; when it expires, the relay is shorted across the resistor. Load current now flows through the relay. On a quick restart, the step-start relay is able to provide inrush limiting. This technique requires the addition of a shorting relay and a timer to control its turn-on. The increased complexity increases the cost to the $20-30 range.

Other inrush current control techniques include zero crossing triacs, active power factor control circuits, and inductive input filtering with damping. Most of these are complicated, bulky, expensive and applicable only to AC inputs. One method for isolated current monitoring is by using an isolation amplifier across a current sense resistor and a differential-to-single-ended conversion amplifier feeding an ADC. Another method is to use an isolated delta-sigma (ΔΣ) modulator with an external digital filter.

As seen, controlling, protecting and monitoring high-voltage DC supplies requires cobbling many components together and making them work safely and seamlessly. This is not a trivial task. These discrete solutions are large, component-intensive, expensive and lack safety certifications. An integrated and certified solution is needed to shorten design time and certification effort from many months into a few weeks.

Integrated Solution for High Voltage Power Control & Telemetry

The LTM9100 µModule IC is a compact all-in-one solution for controlling, protecting and monitoring high-voltage power supplies up to 1000V DC (Figure 2a). A $5kV_{RMS}$ isolation barrier separates the logic and digital interface from the switch controller driving an external N-channel MOSFET or IGBT switch. The isolation

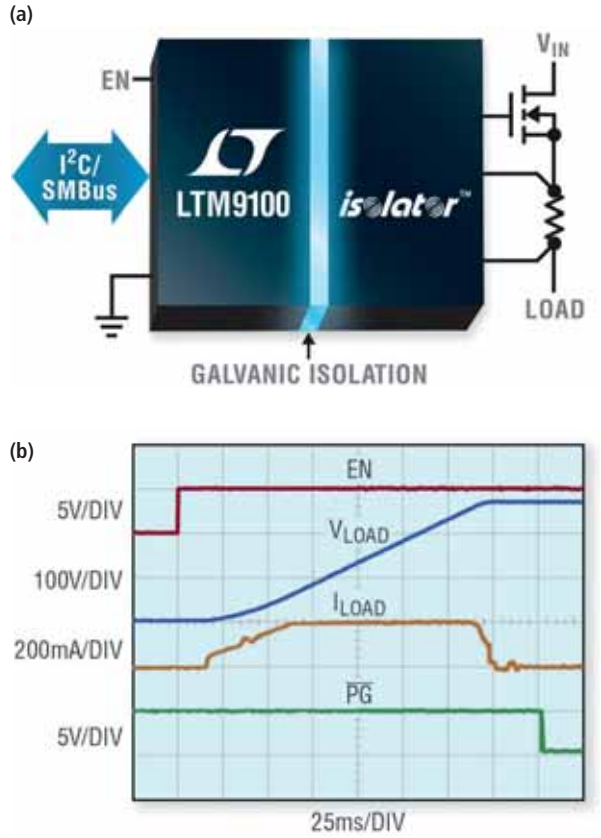


Figure 2: (a) LTM9100 Anyside high-voltage isolated switch controller with telemetry; (b) LTM9100 soft-starting a 270V load with controlled 200mA inrush current

is needed for control circuit protection, operator safety and breaking ground paths. The load is soft-started (Figure 2b) and the supply is protected from overload with a current-limited circuit breaker. Isolated 10-bit ADC measurements of load current and two voltage inputs are accessed via the I²C/SMBus interface, enabling power, energy and thermal monitoring of the high-voltage bus.

The LTM9100 uses Analog Devices's isolator µModule technology (Figure 3) to translate signals and power across an isolation barrier. Signals are encoded into pulses and passed across the isolation boundary using coreless transformers formed in the µModule substrate, resulting in an extremely robust bidirectional communication scheme. Uninterrupted communication is guaranteed for common mode transients of 50kV/µs. The isolated side is powered by a fully integrated DC/DC converter, including the transformer, eliminating the need for external components. To guarantee a robust isolation barrier, each LTM9100 controller is production-tested to $6kV_{RMS}$. The LTM9100 will be recognised by the UL 1577 standard, saving months of certification time for the end-equipment manufacturer. High distance through-insulation translates to a high ±20kV ESD level across the barrier. The µModule package integrates several components and technologies to deliver a cost effective, advanced solution that minimises board space and improves electrical and thermal performance. Due to its isolated nature, the LTM9100 is easily configured for high side, low side (ground return) and floating applications (Figure 4). The LTM9100 is versatile enough to control inrush current not just in hot-swappable cards, but also in AC transformers, motor drives and inductive loads. Adjustable undervoltage and overvoltage lockout thresholds ensure that the load operates only when the input supply is in its valid range. The 22mm x 9mm x 5.16mm BGA package provides 14.6mm of creepage distance between the logic and the isolated sides.

Conclusion

Traditionally, high-voltage DC supplies are found in industrial environments, but other electronic systems are also moving towards higher voltages to lower costs and raise the efficiency of power distribution, especially in power-hungry systems. These supplies need a simple way to control inrush current, protect themselves and to monitor their usage. The first-of-its-kind LTM9100 delivers this simple and compact solution, beating discrete and relay-based circuits by providing a certified ready-to-go solution, saving board area and multiple months of design time and certification effort. All the needed functionality, including digital telemetry and isolated power, is wrapped in a compact, surface mount and low-profile BGA package. ●

Analog Devices (UK) Ltd • Tel: 01628 477066
Email: uksales@linear.com • www.analog.com

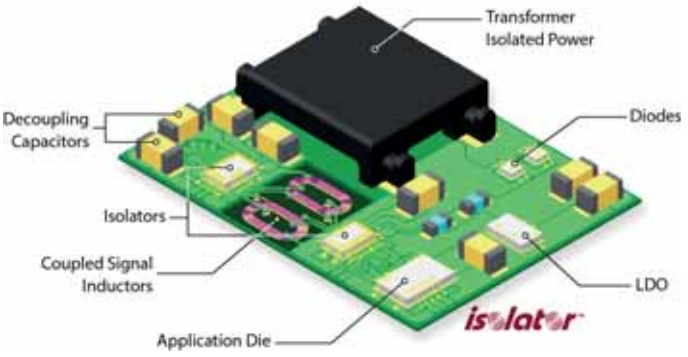


Figure 3: Inside peek at the Analog Devices isolator µModule technology

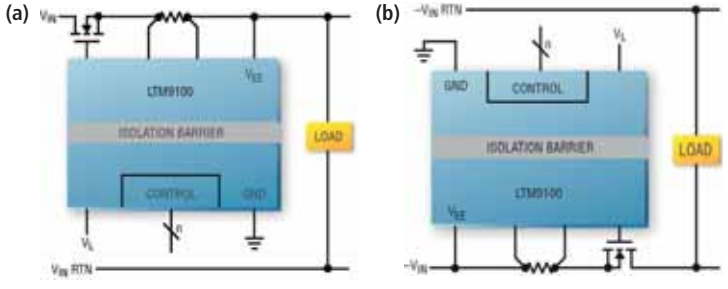
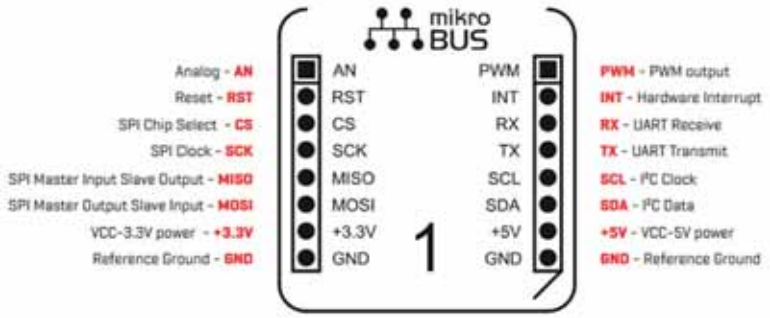


Figure 4: LTM9100 in a high-side or low-side switching application

Figure 1: The mikroBUS pinout specification



MikroBUS in embedded applications

By **Dr Dogan Ibrahim**, Professor at Near East University, Cyprus

MikroBUS is a standard originally developed by mikroElektronika to define the interface between a microcontroller or microprocessor development board and integrated circuits or add-on boards. The mikroBUS standard specifies the size and shape of the add-on boards, pinouts, communication and power supply pins used, the positioning of the mikroBUS socket on the mainboard, and silkscreen marking conventions for both the add-on boards and sockets. Typically, mikroBUS add-on boards may carry a sensor, transceiver, display driver, encoder, motor driver, relay driver, extension connector, power converter, or other modules or integrated circuits.

MikroBUS is an open standard where its details are available on the Internet, and anyone can implement it, as long as they follow the required specifications.

The MicroBUS Standard

The mikroBUS socket consists of a pair of 1x8 female headers, with their sockets spaced at standard 100mil pitch and indicated with silkscreen markings. As shown in Figure 1, the pinout consists of three groups of communications pins, six additional pins and two power supply groups:

- SPI, UART, and I2C;
- PWM, interrupt, analogue input, reset, and chip select;
- +3.3V and GND (on the left);
- +5V and ground (on the right).

The SPI interface consists of four signals – CS, SCK, MISO and MOSI; the I2C interface of two – SCL and SDA; and the UART also two – Rx and Tx. Analogue input and reset, and the PWM output signals have a pin each. Both +3.3V and +5V outputs are available from a mikroBUS add-on board; there are also two GND pins. It's important to note that not all mikroBUS add-boards have all the specified pins, since this depends on their functionality. However, the power and ground pins are compulsory and always present.

MikroBUS Compatible Boards

The mikroBUS standard has been so popular that currently there are over 400 mikroBUS compatible add-on boards available, covering a wide range of interface requirements. Although several companies develop and manufacture these boards, the Serbian company mikroElektronika produces at least one mikroBUS-compatible board every week. These boards are also known as 'Click boards', since they are just plugged on top of (or clicked into) the mikroBUS sockets on the microcontroller development boards.

There are many Click boards, with functionalities such as:

- Wireless connectivity;
- Sensors;
- Interface;
- Display;
- Human-machine interface;
- Storage;
- Clock and timing;
- Motor control;
- Mixed signal;
- Power management;
- Shields.

An example is shown in Figure 2; it's an RS232 Click board used to convert standard UART serial communication signals to RS232 signal levels. A 9-pin standard D-type connector on the board provides the RS232 interface.

Figure 3 shows a more complex Click board – the LoRa Click – a long-range radio transceiver add-on board operating at the sub-gigahertz frequency of 868MHz using spread spectrum communications. Communication between the host and add-on boards is through an UART. An external SMA-type antenna can be connected to this board.

A sensor-based Click board, the DHT22 Click, is shown in Figure 4. It uses the DHT22 chip to measure ambient temperature and relative humidity. Communication is through an I2C interface.

Click Board Shields

In addition to the standard add-on Click boards, many manufacturers such as Microchip and mikroElektronika offer Click board shields that enable these boards to be used with various other development boards, such PIC, Raspberry Pi 3, Arduino Uno, Arduino Mega, STM32F4 Discovery, Intel Joule, and others. Figure 5 shows the Pi 3 Click shield that plugs into a Raspberry Pi 3 computer. It provides two on-board mikroBUS-compatible sockets, extending the selection to over 400 Click boards.

Click Board Compatible Development Boards

Several manufacturers offer microcontroller development boards with built-in mikroBUS sockets, including PIC Clicker, EasyPIC V7, Clicker 2 for PIC18FJ, PIC32MX Clicker, Clicker 2 for CEC1302, Microchip DM160228, ADM00576, and others.

Figure 6 shows the Clicker 2 for PIC18FJ development board with two mikroBUS-compatible sockets. This is a medium performance 8-bit, 12MIPS (48MHz) microcontroller development board incorporating the PIC18F87J50 microcontroller.

Example Project

Here we show how a Click board can be used in a microcontroller application. A GPS Click board is used to receive and display the latitude and longitude of the current position on an LCD; see Figure 7.

In this project, the EasyPIC V7 microcontroller development board is used with the LEA-6S-chip-based GPS Click board, plugged into the development board's mikroBUS socket 1. The development board uses the medium-performance PIC18F45K22 microcontroller.

The NMEA sentences generated by the GPS receiver start with the "$" character, followed by the name of the sentence and then its parameters, with parameters separated by a comma, and a checksum added to the end of a sentence. Sample NMEA sentences generated by the LEA-6S GPS chip are shown in Listing 1.

The $GPLL sentence in this project is decoded as follows:

$GPGLL,517.35744,N,0003.13373,E,103109.00,A,A*65	
5127.35744,N	**Latitude 51 deg. 27.35744 min. North**
00003.1276,E	**Longitude 000 deg. 03.1276 min. East**
10124100	**Fix taken at 10:31:09 UTC**
A	**Data valid (V = data invalid)**
A	**Mode (A=autonomous, D=diferential)**
***65**	**Checksum**

We developed the software using the mikroC Pro for PIC language and compiler; see Listing 2.

At the beginning of the program the connection between LCD and microcontroller is defined, and PORTB and PORTC are configured as digital. The UART is initialised to operate at 9600 baud, and after initialising the LCD, the program runs in an endless loop.

At the beginning of the loop, the buffer that holds the GPS data is cleared. The program then reads data from the GPS and looks for the NMEA string "$GPGLL,". Once detected, the function Uart1_Read_Text is used to read data from the GPS, until the delimiting character "*" is detected (at the end of the $GPGLL sentence, just before the

Figure 2: RS232 Click board

Figure 3: LoRa Click board

Figure 4: DHT22 Click board

Figure 5: Pi 3 Click board

Figure 6: The Clicker 2 for PIC18FJ board

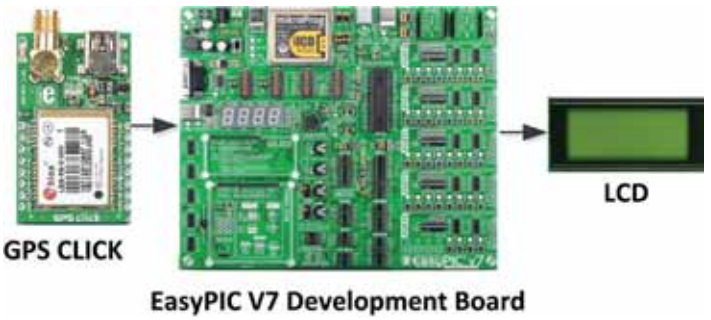


Figure 7: Project setup

Figure 8: Sample display

checksum). At this point the buffer contains all the parameters of the NMEA sentence $GPGLL, starting from the latitude parameter. The remainder of the program extracts the latitude and longitude parameters and loads them into two string arrays, called LAT and LON, respectively. These arrays are then displayed on the LCD after adding the degree signs and spaces. The loop repeats every five seconds.

Figure 8 shows a sample display from the program. ●

```
$GPRMC,101241.00,A,5127.36070,N,0003.12726,,0.118,,28813,,,A*7F
$GPVTG,,T,M,0.118,N0.218,K,A*0
$GPGGA,01241.00,527.36070,N00003.1272,E,1,06,1.0,40.8,M,4.4,M,,*63
$GPGSA,A,329,02,31,1,25,14,,,,,,2.57,1.6,2.01*0C
$GPGSV,,2,09,24,0,142,,25,7,072,21,2967,189,34,1,52,298,3*79
$GPGLL,517.35744,N,0003.13373E,103109.00,A,A*65
```

Listing 1: Sample NMEA sentences

```
/************************************************************
                    USING THE GPC CLICK
                    ===================
$GPGLL,5127.35744,N,00003.13373,E,103109.00,A,A*65

5127.35744,N      Latitude 51 deg. 27.35744 min. North
00003.1276,E      Longitude 000 deg. 03.1276 min. East
103109.00         Fix taken at 10:31:09 UTC
A         Data valid
A         Data autonomous
*65       Checksum
************************************************************/
// Define LCD connections
sbit LCD_RS at RB4_bit;
sbit LCD_EN at RB5_bit;
sbit LCD_D4 at RB0_bit;
sbit LCD_D5 at RB1_bit;
sbit LCD_D6 at RB2_bit;
sbit LCD_D7 at RB3_bit;
sbit LCD_RS_Direction at TRISB4_bit;
sbit LCD_EN_Direction at TRISB5_bit;
sbit LCD_D4_Direction at TRISB0_bit;
sbit LCD_D5_Direction at TRISB1_bit;
sbit LCD_D6_Direction at TRISB2_bit;
sbit LCD_D7_Direction at TRISB3_bit;
// End of LCD connections

// Start of MAIN program
void main()
{
 unsigned char buffer[50];
 unsigned char i,flag,c;
 unsigned char Lat[13], Lon[13];
 unsigned char gps[]="$GPGLL,";

 ANSELB = 0;                    // PORTB digital
 ANSELC = 0;                    // PORTC digital
 LCD_Init();                    // Initialise LCD
```

```
Uart1_Init(9600);                // Baud rate is 9600

while(1)                         // Do forever
{
for(i = 0; i < 50; i++)buffer[i] = 0;        // Clear the buffer
i=0;
flag=0;
//
// Read until NMEA sentence "$GPGLL," is detected
//
while(flag == 0)
{
if(Uart1_Data_Ready() == 1)
{
c = Uart1_Read();
if(c == gps[i])
{
i++;
if(i == 7)flag=1;
}
else i = 0;
}
}
//
// NMEA sentence "$GPGLL," has been detected, now decode it
//
Uart1_Read_Text(buffer,"*",255);       // Read until "*" detected
if(buffer[37] == 'A')            // If the sentence is valid
{
    Lat[0] = buffer[0];
    Lat[1] = buffer[1];                  // Latitude degrees
    Lat[2] = 178;                // Degree character
    Lat[3] = ' ';
    Lat[4] = ' ';
    for(i=0; i < 6; i++)Lat[5+i] = buffer[2+i];     // Latitude minutes
    Lat[11] = buffer[11];         // Latitude direction
    Lat[12] = 0x0;                // Terminate the string
    Lon[0] = buffer[13];          // Longitude Degrees
    Lon[1] = buffer[14];
    Lon[2] = buffer[15];
    Lon[3] = 178;                 // Degree character
    Lon[4] = ' ';
    for(i=0; i < 6; i++)Lon[5+i] = buffer[16+i];    // Longitude minutes
    Lon[11] = buffer[25];         // Longitude direction
    Lon[12] = 0x0;  // Terminate the string
    Lcd_Cmd(_LCD_CLEAR);              // Clear the LCD
    Lcd_Out(1,1,"LAT=");          // Display string LAT=
    Lcd_Out_Cp(Lat);              // Display the latitude
    Lcd_Out(2,1,"LON=");          // Display string LON=
    Lcd_Out_Cp(Lon); // Display the longitude
}
else                         // If data is not valid
{
        Lcd_Cmd(_LCD_CLEAR); // Clear the LCD
        Lcd_Out(1,1,"DATA NOT VALID"); // Display data is not
valid
}
Delay_Ms(5000);  // Wait 5 seconds
}
}
```

Listing 2: Project program

MicroPython and the Lonely32

BY **LUCIO DI JASIO**, MICROCHIP TECHNOLOGY

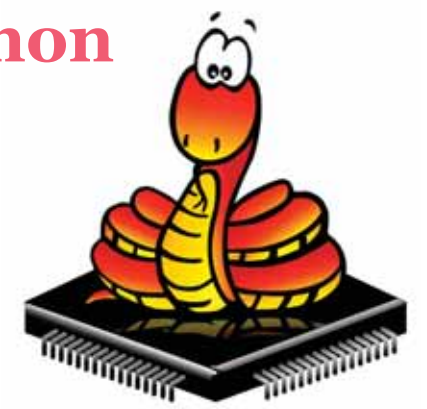


Figure 1: MicroPython (old) logo

It's been almost a decade since I started adding Python to my daily programming. In the beginning it was only to create small scripts to perform "dirty" jobs, such as converting the odd file format or creating a quick visualisation while debugging a complex embedded application. Python is the kind of (programming) language that is usable and useful almost immediately, but you can continue learning it for years.

One summer I even tried to join a small community of developers working on PyMite, an open-source project running Python on small microcontrollers. The community developed AVR, dsPIC and several 32-bit versions of the PyMite compiler/interpreter, and I ported it into the very first PIC32 models. The project eventually fizzled out (as many such projects eventually do), when the original author and maintainer changed jobs and lost interest in it; the small group of contributors then dissolved. You can still find PyMite in the Google Code archives today, but another open-source project – MicroPython – has replaced it, achieving much wider popularity.

Constrained Devices

MicroPython, just like the real Python language, is partly compiled and partly interpreted. The compilation process makes the executable code very compact, which is great for the constrained devices used in embedded control. And even more so, since the executable code is not based on the machine language of any particular architecture but is designed to be interpreted at run-time.

The Python interpreter understands and directly manipulates objects and complex data structures. This is in stark contrast to other, similar languages such as Java for example, where the virtual machine is limited to relatively low-level instructions and data structures. Unfortunately, this means that the interpreter can be quite large, using a lot of RAM and (worse) making extensive use of dynamic memory allocation. None of these characteristics bode particularly well for its adoption in the kind of constrained devices used in embedded applications today.

Fortunately, the definition of constrained devices is changing. In the ten years between the PyMite project and MicroPython, 32-bit microcontrollers with multi-megabyte Flash memories have become common – even larger systems on chip (SoCs) feature tens of Megabytes of RAM.

And since the performance of such devices increases too, could MicroPython soon become viable for general use in embedded control?

Wi-Fi SoCs

In the last three years, the small Chinese start-up Espressif has introduced an interesting new concept: a small SoC that integrates a general-purpose embedded application processor with a Wi-Fi radio. While not entirely revolutionary, the company's first new product (ESP8266) has struck a chord with the large community of hackers and hobby developers. This is probably because of the small size of the evaluation modules, but mostly because of the unprecedentedly low price ($2-5) for what is essentially a small but complete IoT node in a chip!

Even more recently, the company has produced a second-generation product (ESP32) that doubles the number of cores on the SoC, with Bluetooth connectivity.

Software is Eating the World

As most of you will have experienced, powerful hardware is useless if not matched by a complete software development suite and proper documentation. Like most Chinese companies, this would have been a huge challenge for Espressif if they had not been blessed with an open community of dedicated developers. While the (compiler) tool suite is mostly composed of free components from Tensilica (the vendor of the original IP used by the manufacturer for the 32-bit cores), peripheral libraries and TCP/IP and Wi-Fi stacks have been assembled by a mostly self-organised team of developers. Similarly, the best documentation for the silicon and software libraries has been coming from the open source community.

Yet, developing connected (IoT) applications using Wi-Fi and Bluetooth stacks in C/C++ remains a very complex job that only a minority of embedded developers can tackle; the new low price and reduced size did little to change the hard reality of the matter.

MicroPython to the Rescue

It is at this interesting juncture that MicroPython and Espressif paths crossed. Python is a great language for abstracting the kind of complex functionality required by typical IoT, networked applications. In fact, there are many such examples in the general Python libraries and its literature.

It turns out that the 512kB of RAM of the latest ESP32 is sufficient for a MicroPython interpreter, even though part of it must be shared with the Wi-Fi and Bluetooth stacks.

A MicroPython porting to the Espressif SoCs has been in steady development for a while by the community, and a relatively stable version is now available for download from the official website.

Taking the Plunge

Recently, I was looking for a MicroPython-capable evaluation board on Amazon and I stumbled upon the LOLIN32 lite model (a product of Wemos Electronics); see Figure 2. To avoid shopping around for a cheaper unit, I shelled out $12.

Despite it being listed in stock, Amazon immediately and very politely notified me that the actual shipment (to my home office in Germany) would take an extraordinary three weeks! This was annoying, even though, admittedly, I was not in a hurry.

Once the package arrived – quite precisely three weeks later – the unboxing experience begun; or, rather, the "unwrapping", since there was no box. Instead, it was just a ball of bubble-wrap foil, oddly bulging from inside a small bubbly envelope. The envelope itself contained no indication of its origin (fading magic ink?). Nothing intelligible anyway, only my home address (handwritten) was on the envelope, but there was no company branding anywhere to be found. Not even a small sliver of paper, a sticker or any other recognisable marking. Nothing on the inner wrap, either.

Once I cut the strip of scotch tape holding it together, the tiny board literally fell into my hands. My puzzlement grew as I realised that even the board did not bear any markings on either top or bottom. There was simply no silk screen, just a black PCB – a very thin one, in fact. I had to look back at the order page on Amazon and zoom into the product images (Figure 2) to realise that all visible markings had been PhotoShopped; but, the board did match the product I'd ordered.

Feeling LONELY

By now, I had already a new nickname for the orphan board, the "Lonely32".

In the absence of any documentation, I followed my worst instinct and decided to do the only thing possible, plug the micro-USB connector into my MacBook and see what would happen. A pretty, blue LED lit up – and no smoke!

The joy produced by the little blue light was not to last long though, since there was no other perceptible feedback coming from the board or the laptop. No new drives appeared (not a USB-MSD

Figure 2: Lolin32 lite

Figure 3: MicroPython "Hello World" message

device) or new serial ports (not a USB-CDC device) – nothing popped up on screen. Nothing! How was I supposed to communicate with the little Python?

So, I went back to the Amazon order page, this time looking for a link to the vendor website. Eventually I found a link to what appears to be a Wiki link, mostly under construction. It offered some encouraging (if basic) information about the board features (four lines), a link to a schematic (a good start!) and a link to a driver download page (which I assumed was for all Windows users).

Strangely, there was no mention of MicroPython, but instead there was a link to a page for "Getting started with Arduino". Unfortunately, even that turned out to be a dead end – an empty page! Had I been duped?

Open Support Odyssey

After searching for a couple of hours, reading across several forums, many blogs and watching a few videos, I had reached a sad realisation: the only support I could count on was coming from a "community" of desperate souls (like me) that had eventually managed to figure out what to do by proceeding in random steps, much like ants exploring an

unknown territory, revealing a complete and utter ignorance of the terrain – for us the technical details of the product at hand.

Often, the resulting recommendations/advice would include unnecessary steps and loops that obviously made no sense, which an "expert" would admit to but recommend keeping "just in case".

To spare you the agony, here's the summary:

- The (in)famous SoC did not have a USB port, so instead the board developers used a serial-to-USB bridge chip of Chinese origin (Winchiphead). This is apparently so cheap and poorly supported that it is the only such device to my knowledge to require a custom USB driver – even on a Mac!
- A version of the driver compatible with recent OSX versions can only be downloaded from Bjorn Sengotta's personal blog!
- Once the driver is installed (this requires full admin rights and a complete reboot), the serial port is exposed to the OS, but the board is still mostly unusable.
- The user is now supposed to install Python on the laptop first, then use standard Python tool (PIP) to download and run a special script (esptool.py) from the command line. Only through this tool the user can for the first time truly communicate with the board SoC. Notice that the user might have to install a second copy/version of a Python (v3) interpreter on his laptop in case the pre-installed version (Macs ship with Python v2.7) doesn't match that of the script.
- Only if the output of the esptool.py script resembles that in Listing 1 do you know the Lonely 32 is indeed alive!

```
> esptool.py --port /dev/tty.usbmodem14522 flash_id
esptool.py v2.2
Connecting.....__
Detecting chip type ... ESP32
Chip is ESP32D0WDQ6 (revision 0)
Uploading stub...
Running stub...
Manufacturer: c8
Device: 4016
Detected flash size: 4MB
Hard Resetting...
```

Listing 1: Status report: It's alive!

But that's not all. To get from here to a running copy of MicroPython, more commands are needed, installed via the same special Python script, as follows:

- First, erase the SoC companion serial flash memory (Listing 2).

```
> esptool.py --port /dev/tty.usbmodem14522 erase_flash
esptool.py v2.2
...
Erasing flash (this may take a while)...
Chip erase completed successfully in 3.1s
Hard resetting ...
```

Listing 2: Erasing flash

- Then, access the MicroPython website https://micropython.org.
- Select the download page and choose the latest ESP32 image.

  Note this image is not specifically built for the Lonely32 board, but rather generic to all ESP32 boards. Users will have to hope that the board in their hands is sufficiently compatible (pinout, buttons locations, serial flash memory sizes, etc.) with the MicroPython default.
- Finally, upload to the SoC companion serial flash memory the MicroPython image; see Listing 3.

```
> esptool.py --port /dev/tty.usbmodem14522 write_flash
esptool.py v2.2
...
Configuring flash size...
Autodetected flash size: 4MB
Compressed 935888 bytes to 587151...
Wrote 935888 bytes at 0x1000 in 51.7 seconds
Hash data verified.
Leaving...
Hard resetting...
```

Listing 3: Uploading the MicroPython image

Notice the hexadecimal offset value (0x1000), cross your fingers and pray that it's indeed the correct value for the board! It is at this point, and only at this point, that MicroPython actually starts running.

Connecting your favourite serial terminal (CoolTerm in my case) to the virtual serial port (use 115,200 baud), you'll get the first MicroPython command prompt and you'll be able to run your first MicroPython script: "Hello World"!

Following the Money Trail

While it all ended well and the Lonely32 board proved functional, I was left somewhat bitter after this first experience. If this had been the same experience with a product from any US or European company, there would have been a public outrage, social media mocking and mobs with pitchforks outside their corporate offices. It would have happened regardless of the cost of the tool and the target audience.

Surprisingly, instead, the general response that I could observe on the many forums and social postings was "enthusiastic", to say the least. Is this because we (collectively) have become accustomed to receiving such a poor service from Far Eastern firms that anything that eventually works is celebrated as a great success?

If we follow the money trail to see who's benefitting from this business model, it is interesting to observe that only a small fraction of the SoC price goes to the actual manufacturer (< $2). A tiny fraction went to the board manufacturer (< $1), but none to the many people worldwide who contributed with their expertise and hard work to create the software tools, libraries and documentation. Interestingly, it appears that Amazon took the lion's share from this sale – by my estimates, some $6-8.

Miracles of the global economy, eh?! But, also, a sad moment of reflection about the sustainability of a model that seems to be spreading and gaining acceptance in our industry. ●

Micropower zero-drift op-amp enables wireless current sense

By Kris Lokere, Strategic Applications Manager, Signal Conditioning Products, Analog Devices

Many current sense circuits follow the same simple recipe: develop a voltage drop across a sense resistor, amplify the voltage, then read it with an ADC to know the current. However, if the sense resistor is at a voltage that is different from system ground, things can quickly get complicated. Typical solutions bridge the voltage difference in either the analogue or digital domain. Now, there is a different approach – wireless.

High-side current sense amplifiers operate in the analogue domain. The ICs are compact, but the voltage difference they can withstand is limited by semiconductor processes. Devices rated over 100V are rare, and these circuits often lose accuracy if the sense resistor common-mode voltage changes quickly or swings both above and below system ground.

Magnetic or optical isolators usually break the isolation barrier in the digital domain. The hardware can be a bit more bulky, but works without loss of accuracy and can typically withstand thousands of volts. These circuits need an isolated power supply but that can sometimes be integrated into the isolator component. If the sense resistor is physically separated from the main system, you may also need to run long wires or cables.

Recent low-power signal conditioning and wireless technologies offer a new approach. By allowing the entire circuit to float with the common mode of the sense resistor, and transmitting the measured data wirelessly, there are no voltage limitations. The sense resistor can be anywhere, without the need to run cables. If the circuit is very low power, then it won't even need an isolated power supply and can run for many years from a small battery.

Wireless Current Sense

The current sense circuit in Figure 1 employs the LTC2063 chopper-stabilised op-amp to amplify the voltage drop across a sense resistor. The micropower SAR ADC AD7988 digitises the value and reports the result via an SPI interface. The LTP5901-IPM is the wireless module that automatically forms an IP-based mesh network with other nearby nodes. It also has a built-in microprocessor that reads the AD7988 ADC SPI port.

The LTC3335 is a nanopower buck-boost regulator that converts the battery voltage to a constant output voltage. It also includes a Coulomb counter which reports cumulative charge pulled from the battery.

Micropower Zero-Drift Op-amp

To minimise heat dissipation in sense resistors, the voltage drop is typically limited to the 10mV-100mV range. To measure this requires an input circuit with low offset errors, such as a zero-drift op-amp.

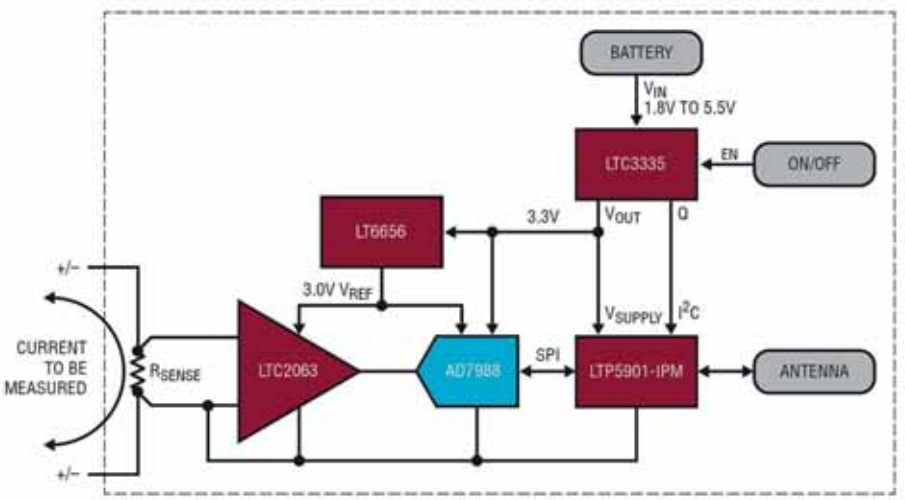


Figure 1: A low-power wireless current sense circuit

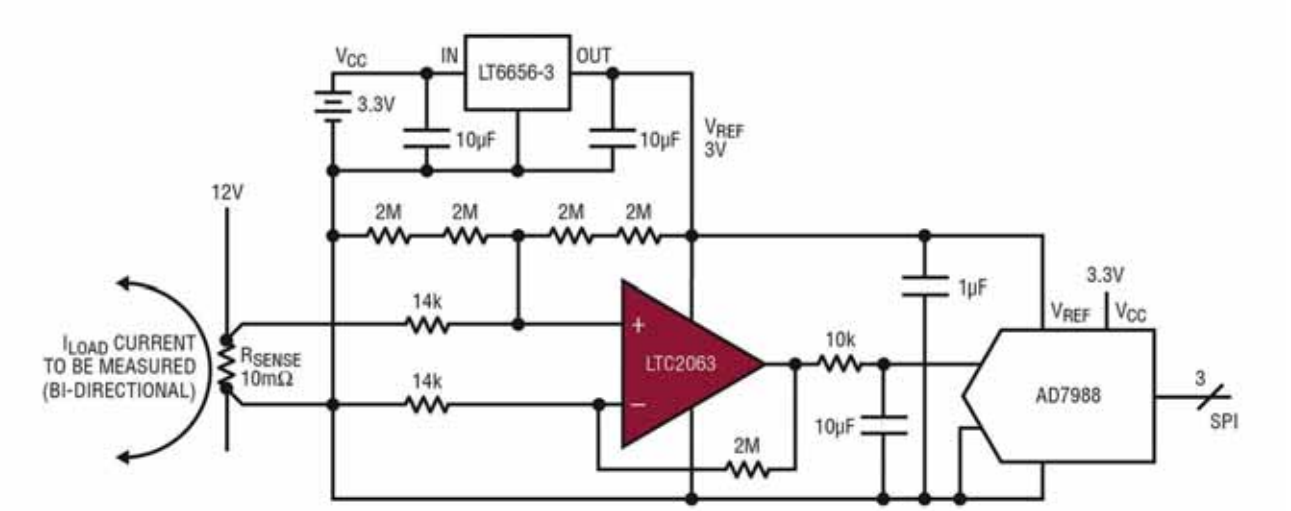


Figure 2: The current sense circuitry floats with the sense resistor voltage

The LTC2063 is an ultralow power, chopper-stabilised op-amp with a maximum supply current of 2µA. Because the offset voltage is less than 10µV, it can measure even very small voltage drops without loss of accuracy.

Figure 2 shows the LTC2063 configured to amplify and level-shift the voltage across a 10mΩ sense resistor. The gain is selected so that ±10mV full-scale at the sense resistor (corresponding to ±1A of current) maps to a near full-scale range at the output, centred around mid-supply. This amplified signal is fed into a 16-bit SAR ADC. At low sample rates, the ADC automatically shuts down in between conversions, resulting in average current consumption as low as 10µA at 1ksps. The LT6656 voltage reference consumes less than 1µA, and biases the amplifier, the level-shift resistors and the ADC's reference input.

Industrial-Strength Wireless Mesh

SmartMesh wireless modules such as LTP5901-IPM include the radio transceiver, embedded microprocessor and networking software. When multiple SmartMesh motes (wireless nodes), are powered up in the vicinity of a network manager, they automatically recognise each other and form a wireless mesh network. All motes in a network are automatically time-synchronised, which means that each radio is only powered on during very short, specific, time intervals. As a result, each can function as a source of sensor information, as well as a routing node to relay data from other nodes toward the manager. This creates a highly reliable, low-power mesh network, where multiple paths are available from each node to the manager, even though all nodes, including the routing ones, operate on very low power.

The LTP5901-IPM includes an ARM Cortex-M3 microprocessor core, which runs the networking software. In addition, users may write application firmware to perform tasks specific to the user application. In this example, the microprocessor inside the LTP5901-IPM reads both the SPI port of the current measurement ADC (AD7988) and the I²C port of the Coulomb counter (LTC3335). The microprocessor can also put the chopper op-amp (LTC2063) in shutdown mode, further reducing its current consumption from 2µA to 200nA. This provides additional power savings when there are extremely long intervals between measurements.

Nanopower Coulomb Counter

Typical power consumption for a mote reporting once per second is less than 5µA for the measurement circuit and can be 40µA for the wireless radio. In practice, power consumption depends on various factors, such as how often the signal chain takes a reading and how the nodes are configured in the network.

The example circuit is powered from two alkaline primary battery cells. The battery input voltage is regulated by the LTC3335 nanopower buck-boost converter with integrated Coulomb counter. It can provide a regulated 3.3V output from an input supply between 1.8V and 5.5V. Load current in duty-cycled wireless applications can vary from 1µA to 20mA, depending on whether the radio is in active or sleep mode.

Recent low-power signal conditioning and wireless technologies offer a new approach to current sense circuits

The LTC3335 has a quiescent current of just 680nA at no load, which keeps the entire circuit at very low power when the radio and signal chain are in sleep mode. Still, the LTC3335 can output as much as 50mA, which provides enough power during radio transmit/receive and for a variety of signal chain circuits.

In high-reliability wireless sensor deployments it is not acceptable for batteries to ever run out. At the same time, replacing batteries too often incurs unwanted downtime and cost. The upshot is that accurate battery drain circuitry is needed. The LTC3335 has a built-in Coulomb

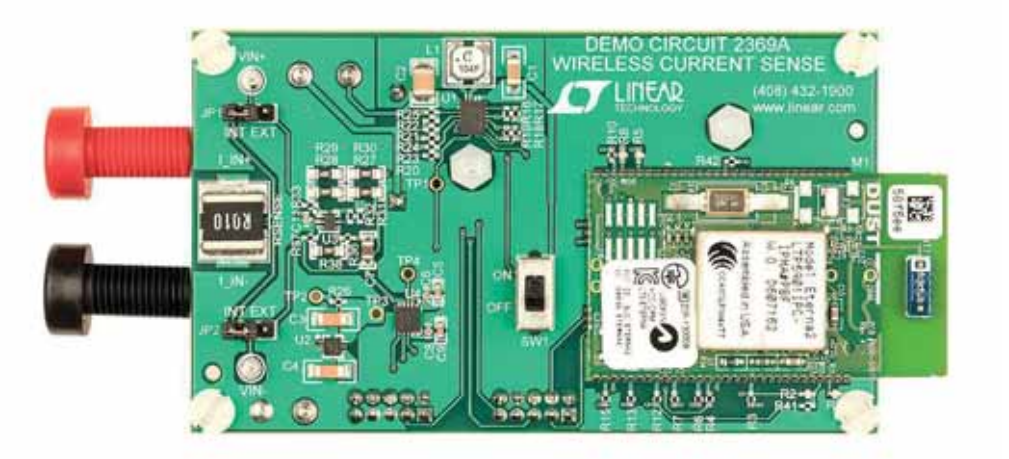


Figure 3: A complete wireless current sense circuit is implemented on a small circuit board

counter. Whenever the regulator switches, it keeps track of the total charge it draws from the battery. This information can be read out using an I²C interface, and can then be used as a predictor of the timing for battery replacement.

Example Implementation

Figure 3 shows an example implementation of a wireless current sense circuit. The ultralow power LTC2063 chopper op-amp can accurately read small voltage drops across a sense resistor. The entire circuit, including micropower ADC and voltage reference, floats with the common mode of the sense resistor. The nanopower LTC3335 switcher can power the circuit for years from a small battery, while reporting cumulative battery usage with its built-in Coulomb counter. The LTP5901-IPM wireless module manages the entire application and automatically connects to a highly reliable SmartMesh IP network. ●

CDTA-based resistorless current-mode full balanced n^{th}-order leapfrog ladder filter

By Jun Xu, Hunan University, China

In the past few years, current-mode techniques have received wide attention due to their high slew rate, wide bandwidth, low voltage and low power consumption. Many current-mode devices, such as CCII, CFA and OTA, are widely used in circuit design. Recently, a new current-mode active element with two current inputs and two different current outputs has been introduced – the current differencing transconductance amplifier (CDTA). This device offers wider bandwidth than its close relative, the current differencing buffered amplifier (CDBA), so it has become more widely used in circuits, such as inductance simulators and sinusoidal oscillators, and is especially promising for building current-mode filters. However, for some high-order filters it is not well suited, especially in CDTA-based n^{th}-order filter circuits. Researchers have proposed two types of n^{th}-order current-mode filters using CDBAs.

Filter Design

Filters are found in many applications, such as radio-frequency (RF) filters for image rejection, or intermediate-frequency (IF) filters for channel selection in wireless receivers.

The design method of a high-order filter is mainly based on cascading second-order filters and negative feedback. The leapfrog structure is one of the most popular choices in active filter design due to its lower sensitivity than the cascade method.

In leapfrog filter simulation of a current-mode ladder network, it is common to use combinations of active and passive components to simulate the inductances and operations of high-order LC ladder circuits.

We propose a circuit that adopts a minimum number of active and passive components to build an n^{th}-order filter, which consumes very little power. The circuit has grounded capacitors and no resistors, which is convenient for

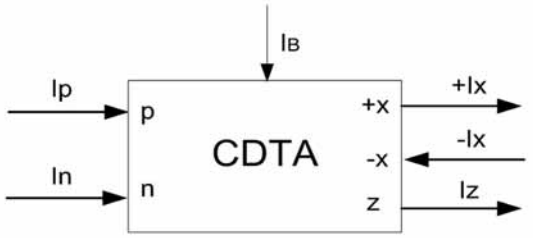


Figure 1: CDTA symbol

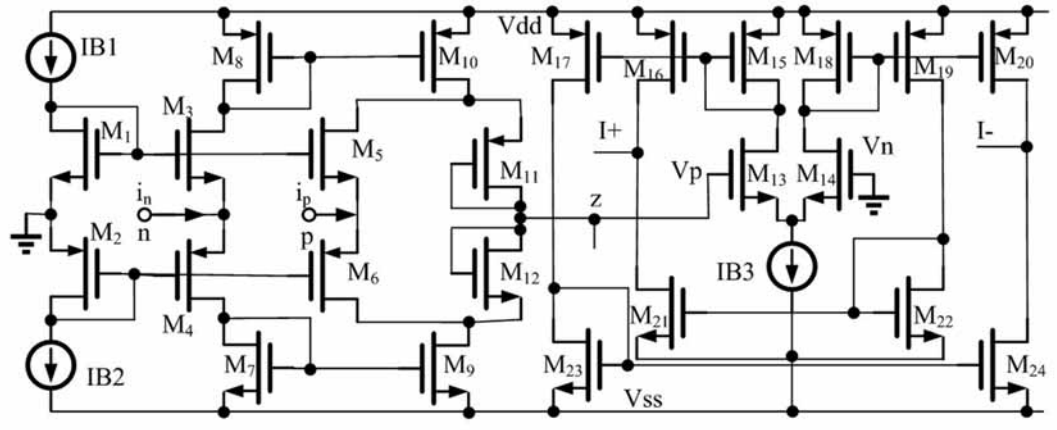


Figure 2: Realisation circuit of a CMOS-based CDTA

integrated circuit (IC) fabrication. This filter can be applied in many fields, including RF transmitters/receivers, phase-locked-loop FM demodulators, wireless communication and instrumentation, among others. It can also be used in the design of active filters instead of the surface acoustic wave (SAW) filters used in GSM systems.

CDTA Realisation

The circuit symbol of CDTA is shown in Figure 1, where p and n are positive and negative current input terminals, and z and x are current output terminals. Its characteristics are:

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & \pm g_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ V_x \end{bmatrix} \quad (1)$$

where $V_x = I_z * Z_z$, g_m is the transconductance gain, and Z_z is an external impedance connected to terminal z. According to Equation 1, current through terminal z follows the difference of the currents through terminals p and n (I_p - I_n), and flows from terminal z into impedance Z_z. The voltage drop at terminal z becomes current at terminal x ($\pm I_x$) with g_m, controlled by the external bias current (I_B).

Usually this circuit can be built with techniques such as CMOS-based CDTA, which is good for monolithic IC fabrication; see Figure 2. Also, the transconductance stage can be copied in a circuit, so the number of CDTA x ports can be tailored as needed.

Leapfrog Ladder Filter Design Method

An integrator is the basic unit of a filter circuit. A first-order integrator can be divided into two categories: lossless and lossy; see Figure 3.

Their transfer functions can be written as:

$$\frac{I_{o+} - I_{o-}}{I_{in+} - I_{in-}} = \frac{2g_m}{sC} \quad (2)$$

$$\frac{I_{o+} - I_{o-}}{I_{in+} - I_{in-}} = \frac{2g_m/C}{s + 2g_m/C} \quad (3)$$

Figure 4 shows a current-mode nth-order all-pole passive LC low-pass filter network, with node equations:

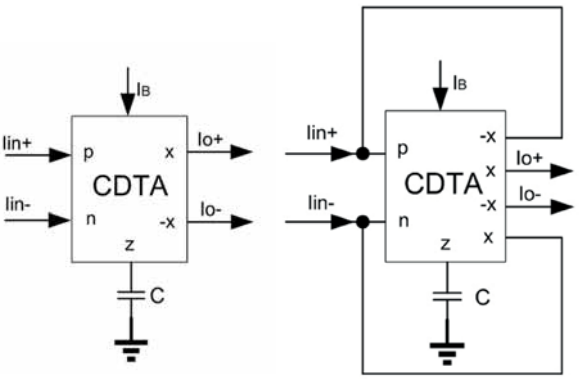


Figure 3: CDTA-based lossless integrator circuit; CDTA-based lossy integrator circuit

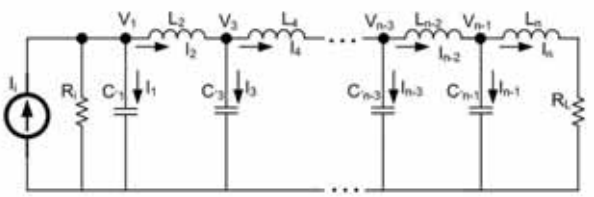


Figure 4: Current-mode nth-order passive LC ladder network

$$V_1 = (I_i - I_2)\frac{R_i / sC_1'}{R_i + 1/sC_1'}, \quad I_2 = (V_1 - V_3)\frac{1}{sL_2} \quad (4)$$

$$V_3 = (I_2 - I_4)\frac{1}{sC_3'}, \quad I_4 = (V_3 - V_5)\frac{1}{sL_4} \quad (5)$$

$$V_{n-3} = (I_{n-4} - I_{n-2})\frac{1}{sC_{n-3}'}, \quad I_{n-2} = (V_{n-3} - V_{n-1})\frac{1}{sL_{n-2}} \quad (6)$$

$$V_{n-1} = (I_{n-2} - I_n)\frac{1}{sC_{n-1}'}, \quad I_n = V_{n-1}\frac{1}{sL_n + R_L} \quad (7)$$

To implement these equations, the voltage variables are divided by resistance R_o (the conversion factor), leading to:

$$I_1 = (I_i - I_2)\frac{1/R_oC_1'}{s + 1/R_iC_1'}, \quad I_2 = (I_1 - I_3)\frac{R_o}{sL_2} \quad (8)$$

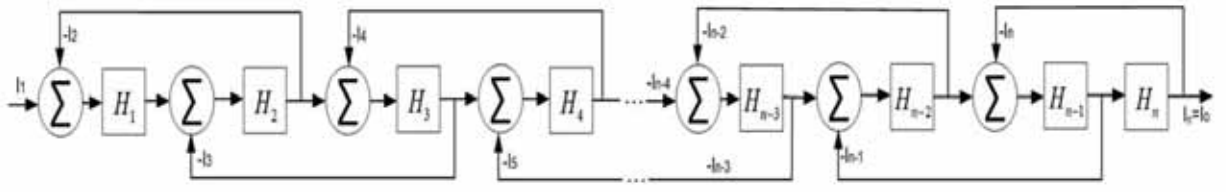


Figure 5: Signal flow diagram of a current-mode nth-order passive LC ladder network

$$I_3 = (I_2 - I_4)\frac{1}{sC_3'R_o}\ ,\ I_4 = (I_3 - I_5)\frac{R_o}{sL_4} \quad (9)$$

$$I_{n-3} = (I_{n-4} - I_{n-2})\frac{1}{sC_{n-3}'R_o}\ ,\ I_{n-2} = (I_{n-3} - I_{n-1})\frac{R_o}{sL_{n-2}} \quad (10)$$

$$I_{n-1} = (I_{n-2} - I_n)\frac{1}{sC_{n-1}'R_o}\ ,\ I_n = I_{n-1}\frac{R_o/L_n}{s + R_L/L_n} \quad (11)$$

We then have:

$$H_1 = \frac{1/R_oC_1'}{s + 1/R_iC_1'}\ ,\ H_2 = \frac{R_o}{sL_2} \quad (12)$$

$$H_3 = \frac{1}{sC_3'R_o},\ H_4 = \frac{R_o}{sL_4} \quad (13)$$

$$H_{n-3} = \frac{1}{sC_{n-3}'R_o}\ ,\ H_{n-2} = \frac{R_o}{sL_{n-2}} \quad (14)$$

$$H_{n-1} = \frac{1}{sC_{n-1}'R_o}\ ,\ H_n = \frac{R_o/L_n}{s + R_L/L_n} \quad (15)$$

which help determine the circuit's signal flow diagram; see Figure 5.

The proposed CDTA-based current-mode n[th]-order leapfrog ladder filter is shown in Figure 6. The circuit's simple structure adopts n active components, n grounded capacitors and uses no resistors, which safeguards the bandwidth and is convenient for IC fabrication.

Circuit Parameters

Assuming

$$R_i = R_L = R_o \quad (16)$$

and using Equations 2-15 helps determine the parameter relationships of the components in the circuits of Figures 4 to 6.

$$\frac{2g_{m1}/C_1}{s + 2g_{m1}/C_1} = \frac{1/R_oC_1'}{s + 1/R_iC_1'} \quad (17)$$

then $C_1 = 2g_{m1}R_oC_1'$ (18)

when $i = 2, 4, K, n-2$:

$$\frac{2g_{mi}}{sC_i'} = \frac{R_o}{sL_i} \quad (19)$$

then $C_i = 2g_{mi}L_i/R_o$ (20)

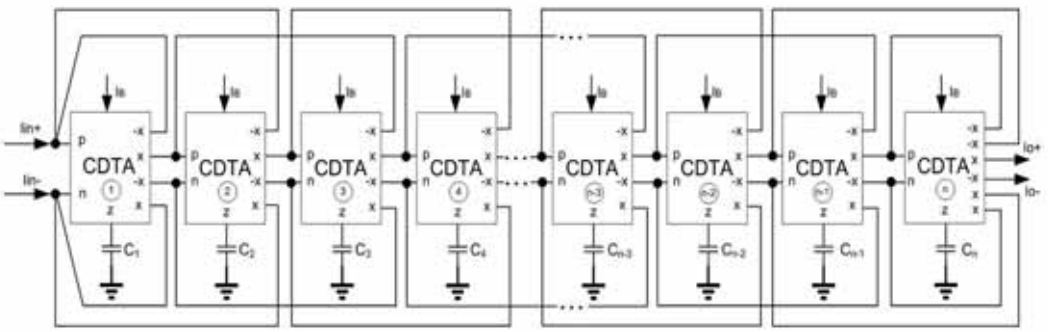


Figure 6: Proposed CDTA-based resistorless current-mode full balanced n[th]-order leapfrog ladder filter

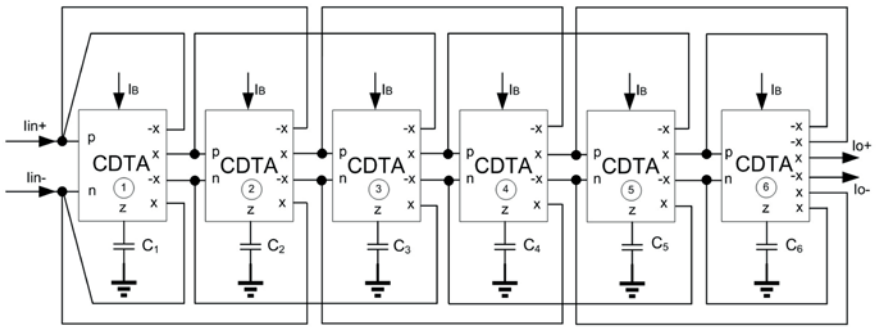


Figure 7: Proposed CDTA-based resistorless current-mode full balanced 6[th]-order leapfrog ladder filter

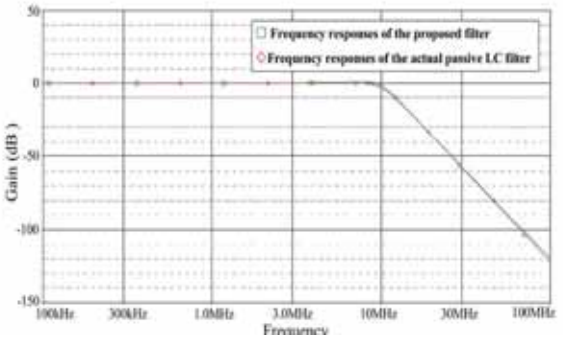


Figure 8: Frequency response of the proposed filter and actual filter

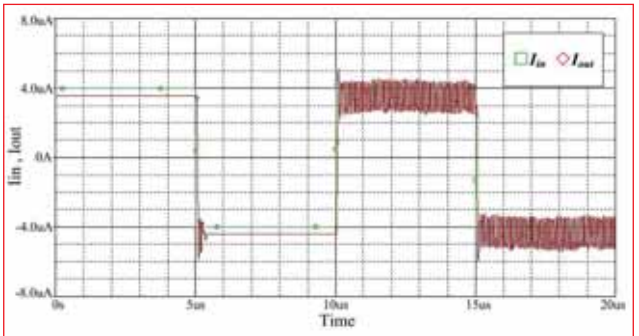


Figure 9: The transient response of the proposed filter as a square wave

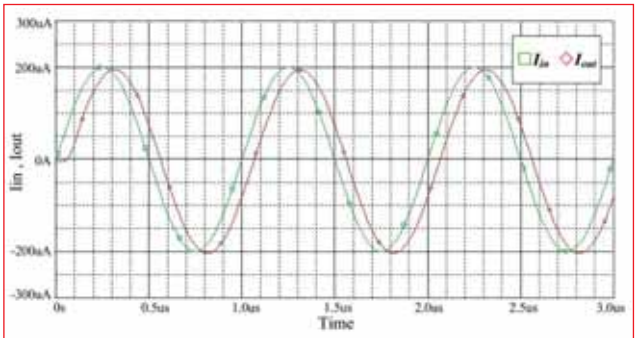


Figure 10: The transient response of the proposed filter as a sinusoidal wavewave

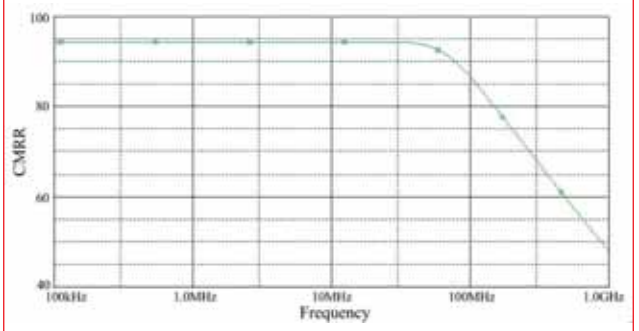


Figure 11: The transient response of the proposed filter as a square wave

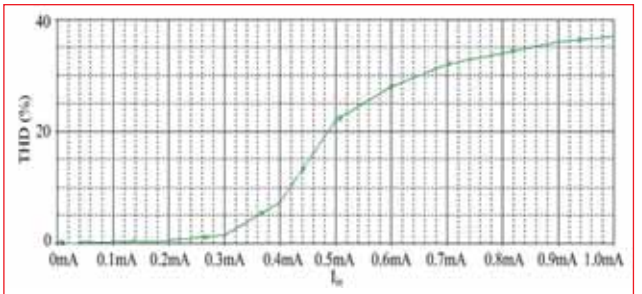


Figure 12: The filter's total harmonic distortion (THD)

$$\frac{2g_{mi}}{sC_i} = \frac{1}{sC_i' R_o} \quad (21)$$

$$\text{then } C_i = 2g_{mi} C_i' R_o \quad (22)$$

$$\frac{2g_{mn}/C_n}{s + 2g_{mn}/C_n} = \frac{R_o/L_n}{s + R_L/L_n} \quad (23)$$

$$\text{then } C_n = 2g_{mn} L_n / R_o \quad (24)$$

So synthesising Equations 17-24, and when $i = 1, 3, K, n-1$:

$$C_i = 2g_{mi} C_i' R_o \quad (25)$$

when $i = 2, 4, K, n-2$:

$$C_i = 2g_{mi} L_i / R_o \quad (26)$$

It is easy to confirm the parametric values of the elements from the known filter parameters. The cutoff angular frequency (ω_o) of the filter can be adjusted properly by I_B.

Simulation and Results

To verify the theoretical analysis, in PSpice we simulated a current-mode 6th-order Butterworth filter according to the proposed configuration, based on the CMOS-based CDTA circuit of Figure 2. This circuit is shown in Figure 7. We chose the parameters of a 0.5µm MIETEC transistor model.

The filter's cutoff frequency is 10MHz and the passive component parameters are: $C_1' = 0.824$pF, $L_2 = 0.225$mH, $C_3' = 3.076$pF, $L_4 = 0.307$mH, $C_5' = 2.25$pF and $L_6 = 0.082$mH. The CDTA circuit is supplied with symmetrical voltages of ±2.5V. The external bias currents are $I_{B1} = I_{B2} = 85$µA and $I_{B3} = 200$µA, and the transconductance gain g_{mi} is 457.83µS. It is easy to get the value of C_i from the above parameters, so $C_1 = 3.77$pF, $C_2 = 10.3$pF, $C_3 = 14.08$pF, $C_4 = 14.08$pF, $C_5 = 10.3$pF and $C_6 = 3.77$pF.

Figure 8 shows the simulation results, which show the theoretical and simulation values to be in good agreement. The circuit's total power consumption is low, at 0.02W.

Figures 9 and 10 show the transient response of the proposed filter. In the simulation, the input signals are a square-wave current (±2µA/100kHz) and a sinusoidal current (±100µA/1MHz). The switching delay time of the filter is about 0.4µs. The filter's total harmonic distortion (THD) analysis is also investigated using the PSpice program (sinusoidal current at 1MHz). It can be seen in Figure 11 that for an input current signal below 300µA, the circuit's THD is no more than 2%. ●

Line-based compressive sensing for low-power visual applications

By Mansoor Ebrahim, Sunway University, Malaysia, and Syed Hasan Adil, Daniyal Nawaz and Kamran Raza, Iqra University, Pakistan

In digital signal processing systems, images are usually first transformed into digital signals and then compressed using standard codec algorithms like JPEG, JPEG 2000, MPEG and others. Most of these conventional algorithms require a significant amount of processing and hence computing power, which increases the encoder's energy consumption, making them unsuitable for low-power applications such as wireless or visual sensor networks.

Recently a new method called compressive sensing (CS) has been shown to be more efficient at complex processing at low power. With CS, computation is shifted from the encoder to the decoder – a direct opposite of conventional approaches.

Conventional methodologies such as JPEG, JPEG 2000, MPEG and H.264 use the Shannon sampling theorem, or the so-called Nyquist rate, to transform signals, whereas with CS a signal is represented by a few non-zero coefficients – fewer than the Nyquist rate. The CS scheme effectively decreases the computational requirements (memory, processing power and transmission bandwidth) at the encoder, by combining into a single process the signal acquisition (sampling) and dimensionality (the amount of data that will stream out).

A New Method

In this article we propose a line-based sampling approach for visual applications using CS, for fast, efficient and less computationally-complex sampling of images.

With our method, the original image is first divided into N multiple lines of the same size, with each line processed independently using the sampling operator Φ. Such an approach benefits CS because:

(i) line-based measurement is faster for practical applications, since sampled image data need not be encoded in its entirety but line by line, until sampling of the whole image is complete;

(ii) practical implementation and storage of the sampling operator are simpler because they deal with a minimum number of samples;

(iii) the individual processing of each image-data block results in an easy solution with a significantly faster and better

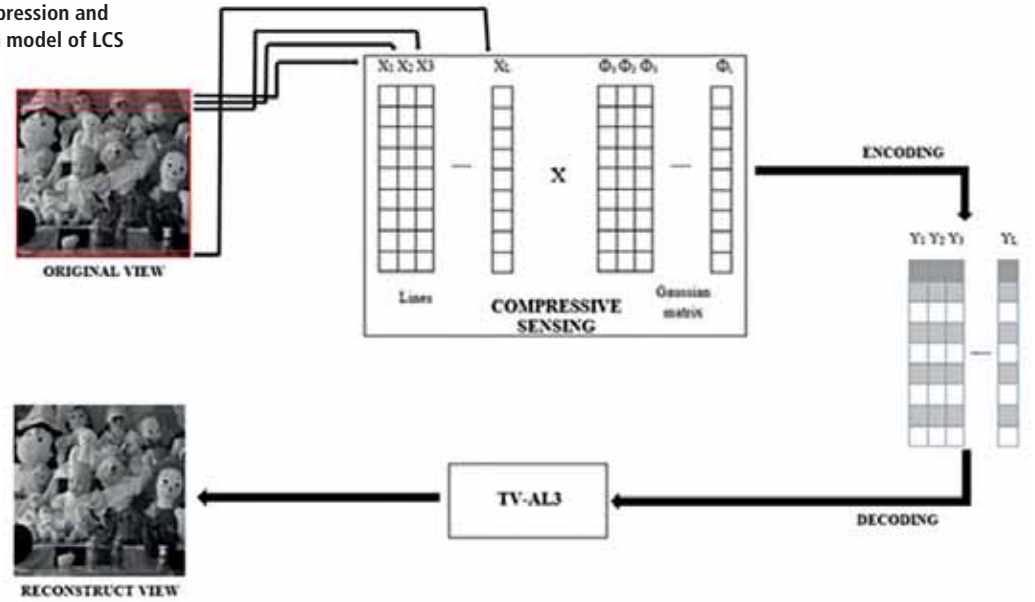


Figure 1: Compression and reconstruction model of LCS

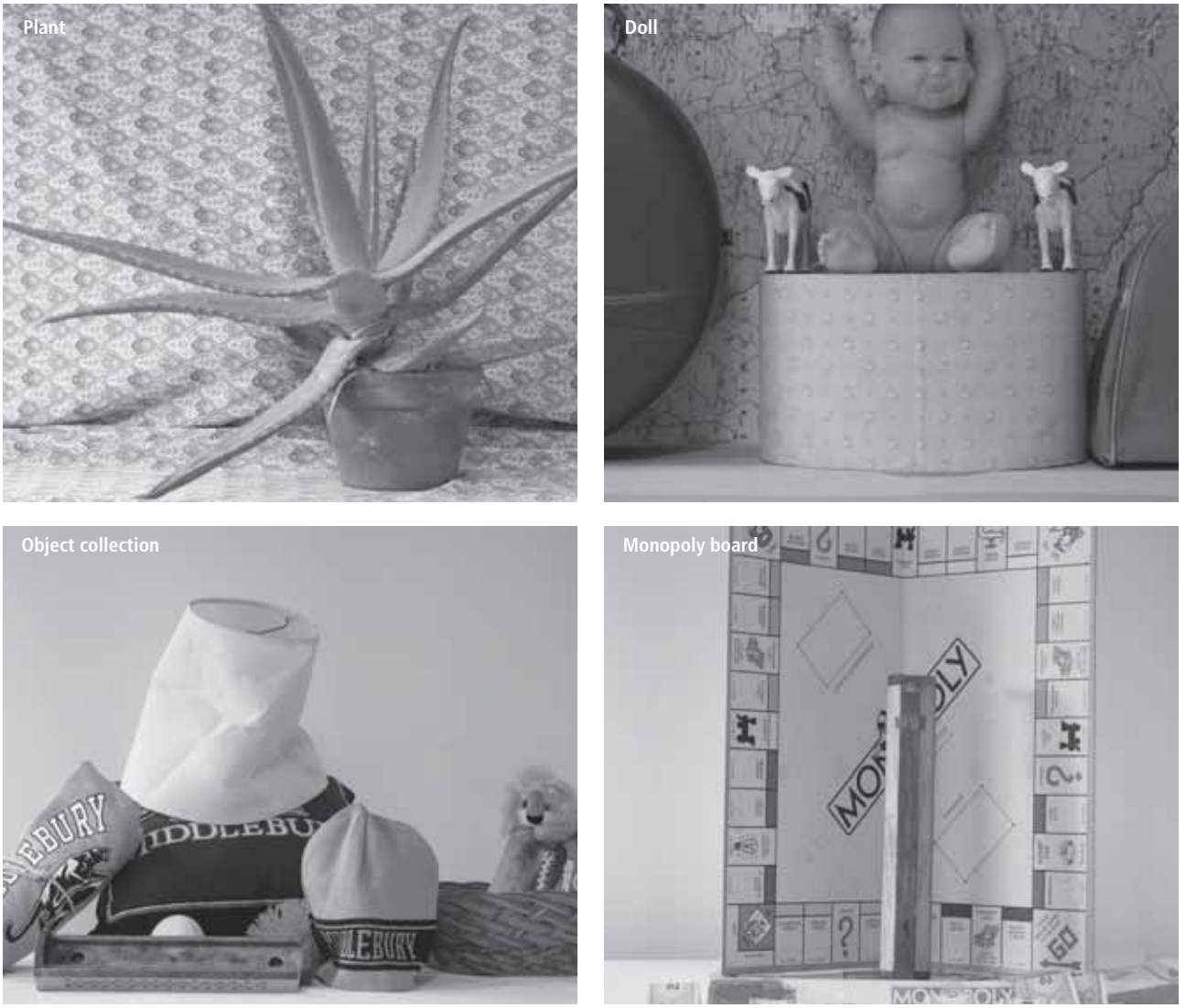


Figure 2: Several standard grayscale test images of 512 x 512 size

reconstruction process.

The CS method relies on two important parameters:

- Sparsity, which is important for sampling and reconstruction of a signal; and
- Incoherence (sensing modality), which helps determine the maximum correlation measured between any two elements from two different matrices.

If we consider a signal X with length N to be recovered from M measurements (M << N), sparse in some transformation domain Ψ, with random measurement matrix Φ, the set of measurements y is then:

$$y = \Phi X \quad (1)$$

where $X \in R_N$ is the input signal and $y \in R_M$ is the measurement vector. It is assumed that the random sampling matrix Φ is orthonormal (a matrix with a transpose equal to its inverse, or 1), i.e. $\Phi \times \Phi^T = A$, where A is the identity matrix, or unit matrix.

As the number of unknowns is much larger than the number of observations, recovery of $X \in R_N$ from its corresponding $y \in R_M$, i.e. inverse projection of $X' = \Phi^{-1} y$, is not sufficient.

In our approach, the line-based encoded image is reconstructed by using Total Variation (TV) minimisation, which uses piece-wise smooth characteristics of the signals rather than finding the sparse solution in the transformation domain. The basic TV minimisation function is given as:

$$TV(X) = \sum i,j \; ||Xi+1,j - Xi,j||+||Xi,j+1 - Xi,j|| \quad (2)$$

$$min_x \; X \; E|| \; y - \Theta \; X|| + \lambda \; TV(X) \text{ subject to } \Theta = \Phi \; \Psi \quad (3)$$

where E is the ℓ_2 norm (also known as 'least squares', used

Sampling Rate	0.05	0.1	0.15	0.2	0.25	0.3
Plant						
Conventional CS scheme	23.93	24.95	26.32	27.52	28.45	29.32
Proposed scheme	24.76	26.16	27.54	28.78	29.87	30.86
Doll						
Conventional CS scheme	24.29	29.31	31.83	33.47	35.2	36.6
Proposed scheme	25.75	31.38	34.18	36.09	37.92	39.39
Monopoly board						
Conventional CS scheme	23.7	27.4	29.67	32.65	35.07	37.34
Proposed scheme	24.54	28.38	30.88	34.01	36.47	38.93
Object collection						
Conventional CS scheme	24.53	27.53	29.44	32.05	33.98	35.7
Proposed scheme	26.74	30.19	32.71	35.42	37.49	39.33

Table 1: R-D performance (dB) achieved by five trials of a previous scholarly scheme and our proposed scheme for different images

to minimise the sum of squares of differences between the target and estimated values). However, the basic TV minimisation CS reconstruction problem in Equation 3 is exposed to additional computational burden, i.e. memory usage, processing and transmission power, restricting its use for CS reconstruction. There's a scheme called TV-AL3 that can solve this equation, which combines the conventional Augmented Lagrangian (AL) method with variable-splitting and alternating-direction methods. The TV-AL3 depends on global structurally-random matrices (mainly used for producing fast and efficient sensing matrices in CS measurements), and can generate the same high-quality reconstructed image as the standard Total Variation method but with less processing.

Line-Based Compressive Sensing

Consider an I_R x I_C image captured by a visal node, where I_R and I_C are the total number of pixels in each row and column, respectively. At the encoder, the proposed line-based CS is applied to the image, which first has been divided into N multiple lines (each 1 x L in size), and then each line processed independently using the sampling operator Φ.

If X_i is the vectorised signal of the i^{th} line of the image, then the compressed CS vector output Y_i is:

$$min_X ||D_m X||_n, \text{ subject to (s.t.) } Y_i = \Phi_L X_i \quad (4)$$

where $D \in (D_X, D_Y)$ are the horizontal and vertical gradients respectively, and Φ_L is an ortho-normalised, independent, identically-distributed Gaussian matrix.

For the whole image, each line is then individually sampled using the same measurement matrix Φ_L with a constrained structure, or the optimal solution. The measurement Y is then transmitted to the decoder for reconstruction. The encoding process then goes as follows:

LCS ENCODER

Input: Grey scale image (2-dimensional image);

Image to lines (%)
Consider an image I
for r = 1 to r_{Max}
for c = 1 to c_{Max}
re-arranges each distinct block I_{rc} into a column of X.

Compressive sensing (%)
Now consider vector X (lines)
for i = 1 to i_{Max}
for each line i, sampled with measurement matrix Φ
$Y_i = \Phi X_i$
Output: Y, the encoded sample

At the decoder, the line-based encoded measurements Yi of the image are decoded by solving the TV minimisation problem of Equation 3, using the AL method with variable splitting, and alternating it with the direction method, to reconstruct the original image:

$$\text{TV-AL3}(X) = \min_X ||W_m||_n + \lambda ||X - AX||^2 \quad (5)$$

subject to $W_m = D_m X$, A = Augmented Lagrangian filter where λ = extra plenty parameter.

The proposed decoding process of the encoded sample is defined as follows:

DECODER

Input:
Y = encoded sample;
Φ = measurement Gaussian matrix;

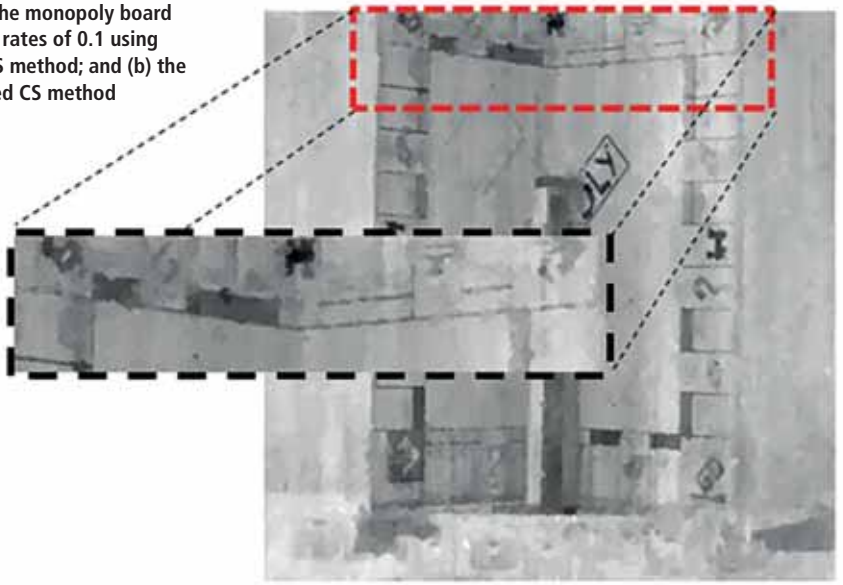


Figure 3: Visual quality comparison for reconstruction of the monopoly board image at sampling rates of 0.1 using (a) conventional CS method; and (b) the proposed line-based CS method

a) Visual results of conventional compressive sensing

b) Visual results of proposed line-based compressive sensing

R = number of rows of the actual image;
C = number of columns of the actual image,
λ = Plenty Parameter (line size, compressive ratio)

Rearrangement (%)
for r = 1 to R
for c = 1 to C
re-arranges each block of encoded image into a column of X.

Reconstruction of the encoded image of size R x C (%)
Now consider vector X
I <- TVAL3(X, λ)
Output: I, the reconstruction of the encoded sample image

Improved Images

The overall process of line-based compression and reconstruction is shown in Figure 1.

The proposed scheme is implemented using Matlab version 8.3.0.532 (R2014b) on an Intel Xeon CPU E5-1620 desktop computer with a 3.6GHz processor and 8GB RAM. Its performance was evaluated with a set of standard greyscale images 512 x 512 in size; see Figure 2.

The evaluation was carried out by measuring the rate distortion (R-D) in terms of peak signal-to-noise ratio, or PSNR (dB), for different sampling rates. Because of the random nature of the measurement matrix Φ, the quality of the reconstructed image varies, so we did five independent trials. All images are encoded at sampling rates of 0.05, 0.1, 0.15, 0.2, 0.25 and 0.3; see Table 1.

Table 1 shows that the proposed scheme is better than the conventional CS scheme, with improved gain of 1-3dB, for example. Moreover, for more complex images such as 'object collections' the performance gain at 2-3dB is even higher.

By comparing the visual results in Figure 3, it can be seen that the image reconstructed using the proposed scheme improves the blurring in the image reconstructed by the conventional CS method. Equally, by comparing the highlighted regions (red dotted area), it can be seen that the image reconstructed using our scheme is much sharper than the conventional one.

Fast and Efficient

This study presents a line-based compressed sensing scheme for low-power visual applications. The scheme is simpler, provides faster and more efficient initial recovery solution of images, than other, conventional methods.

However, there is further work to be done, especially on the optimisation criteria of the line-based sampling operator, and the comparison between this method with the block-based CS scheme. ●

Design of low power DC-DC converters for energy harvesting

By Maurizio di Paolo, Technical Writer based in Italy

Energy harvesting increases the operational life of low-power devices, eliminating the necessity to replace or recharge batteries. In wireless sensor network (WSN) applications, the device's long-life is a key element of the design. Ultra-low power DC-DC converters are a big part of this design too, enabling high performance with minimal power consumption in both operational and standby modes.

The Quest for Low Power

The march of mobile devices and their ever-decreasing power consumption has led microelectronics toward environmental energy sources such as kinetics, solar, thermal and RF. But getting the most out of these sources is not simple; detecting that energy and controlling and conditioning its ultra-low power are key factors in the design of an energy-harvesting system and its overall efficiency.

Anywhere on Earth – and in the universe – there is a temperature gradient, creating sufficient energy to power a device. The well-known Seebeck effect is a phenomenon in which a temperature difference between two dissimilar electrical conductors or semiconductors produces a voltage difference between the two.

RF energy is electromagnetic waves, currently harnessed by so many devices, such as mobile phones, base stations, antennas and more; see Figure 1. Some of these systems, and especially most low-power IoT applications, also use remote sensors powered by batteries. Although batteries may have a long life, they eventually expire and must be replaced, which is expensive and a serious threat to the environment.

Energy harvesting makes low-power devices self-sufficient, in some cases eliminating the use of batteries entirely. The supporting energy-management system should provide high energy efficiency by storing small energy packets, so there's always power for the desired application.

Low-Power Design

The challenge of a power management system is to provide constant voltage output with maximum efficiency. With recent technology advances, energy harvesting can easily provide power in the nanowatt to microwatt range, suitable for some devices, such as sensors.

In a WSN, autonomous devices collect data and communicate with each other to perform a task. A typical WSN architecture consists of transducers that convert environmental energy into electrical signals, a DC-DC converter and other electronic components to manage the signals to and from a microcontroller, and a transceiver.

Estimating the power to operate such a device is an important design step. Other parameters to consider are, for example, how much time is required for a data read/write operation, or the size

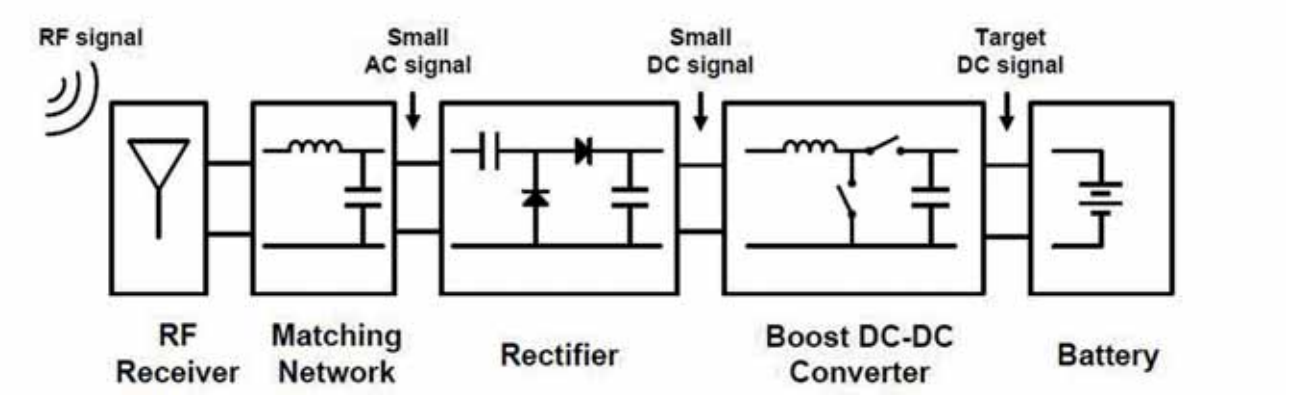


Figure 1: Block diagram of an RF energy harvesting system

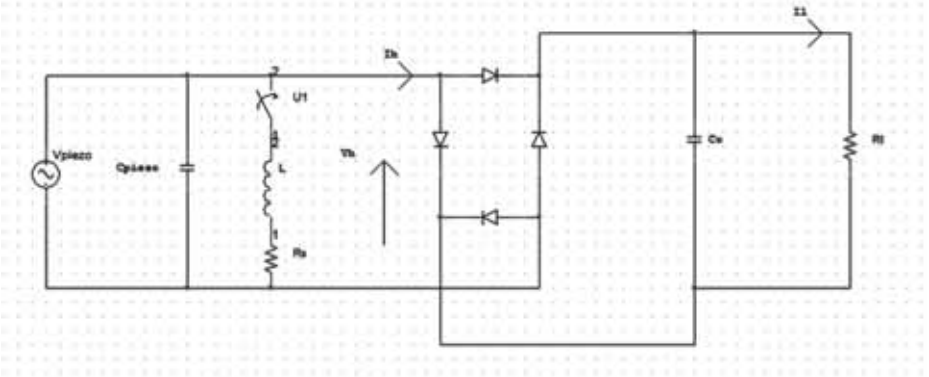


Figure 2: Synchronous switched harvesting on inductor (SSHI)

of the data packet. Several other factors influence the energy consumption characteristics of a WSN system powered by energy-harvesting circuits, such as how long the source will be available for, and the power density it provides.

Energy Harvesting

Usually, energy harvesting doesn't provide constant power levels, so therefore a storage device becomes necessary to compensate for the total absence of environmental energy; for example, with a solar-energy-harvesting system, there's no available energy during the night. Since the output from energy-harvesting devices is generally small and intermittent, such a system should also include a charge controller for a rechargeable Li-ion or thin-film battery, and a wireless connection module. Furthermore, digital power management is essential to maximising efficiency. It handles the output of the transducer, ensuring safe and reliable operation of the battery or supercapacitor, and maintains correct voltage and current levels for the application.

Power management for energy-harvesting applications requires minimal start-up and supply voltage, standby power at zero, ultra-low losses and standby currents, and maximum efficiency during operation with reduced loads. Very-low-power DC-DC converters solve most of these problems, ensuring stable voltage and uniform current for the application.

Conditioning Circuits

Conditioning circuits play a fundamental role in energy-harvesting systems by handling various parameters, such as input impedance, power control and filtering. Energy-harvesting systems using piezoelectric transduction have a highly reactive output impedance. A typical approach for these transducers is called Synchronous Switched Harvesting on Inductor (SSHI) (Figure 2), which involves reversing the charge polarity of the piezoelectric material twice per cycle when the mechanical part reaches its maximum displacement.

In the conditioning system with passive circuits, such as a rectifier, the problems are concentrated on the input impedance: a null voltage on the storage capacitor implies a short on the harvesting circuit.

DC-DC Converter Design

The DC-DC converter is widely used in energy-harvesting systems to convert the voltage generated by the transducer into a stable form required by the back-end circuit or battery.

Efficiency and stability are fundamental design requirements for DC-DC converters. Conventional PWM control is usually not suitable for them in energy-harvesting situations due to its poor stability and low power conversion efficiency. Adaptive on-time/off-time control (AOOT) is an excellent alternative, and zero current switching (ZCS) can be applied to further improve the DC-DC converter's performance.

Three basic methods can be applied to achieve DC-DC voltage conversion. One uses linear voltage conversion on resistive dividers, also called low-dropout regulator (LDO). The control takes place by means of a resistor that regulates the output voltage, thus representing a step-down converter. A drawback is the low conversion efficiency.

Another approach is to implement a switch-mode charge-pump circuit to achieve step-up or step-down configuration. This solution implements energy-storage capacitors and power switches. The circuit is modified according to the operation of the power switches, thus obtaining power conversion; see Figure 3.

A third method exploits the inductor/capacitor combination. By using the switch in an on or off position, the energy from the input voltage source is periodically stored in the inductor and sent

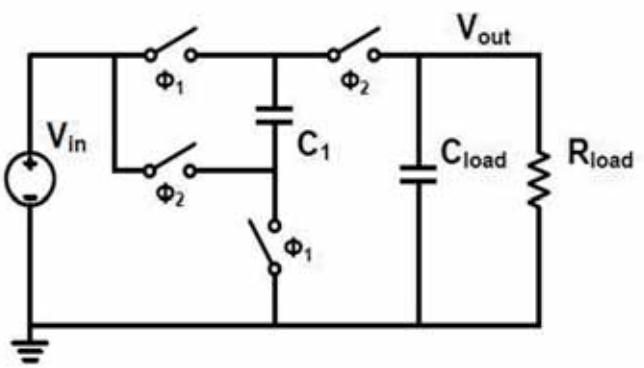


Figure 3: Switch-mode charge-pump DC-DC converter

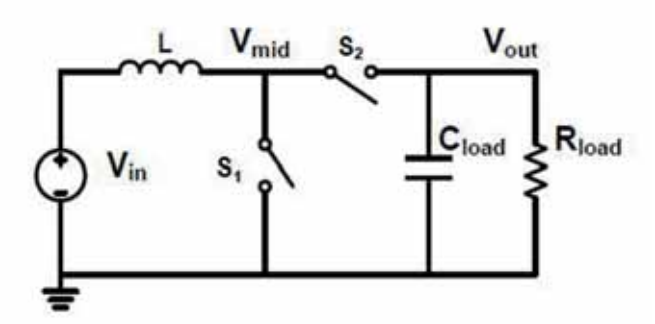


Figure 4: Circuit of an inductor-based boost DC-DC converter

to the load capacitor, thus obtaining the step-up or step-down conversion; see Figure 4.

The DC-DC boost converter is used to change a low DC voltage to a higher DC one. Based on different waveforms of the inductor current, there are two conduction modes for the boost converter: continuous conduction (CCM) and discontinuous conduction mode (DCM). In CCM, the current in the energy-transfer inductor never goes to zero between switching cycles, whereas in DCM currents go to zero during a part of the switching cycle.

Power Losses in the DC-DC Converter

Several elements in a DC-DC converter contribute to power losses: non-ideal external components, such as coils and capacitors, and non-ideal switches that cause switching losses. These losses are dominant in heavy load conditions. However, there are also losses that stem from the internal control blocks, such as a zero-crossing detector, a current sensor and a reference voltage. These losses are dominant in light load conditions.

Using larger switches helps reduce switching losses, but this is undesirable in small applications, such as wearable devices that may exploit energy harvesting; and, increasing the die area also increases the cost of the IC.

In light load cases, energy loss can be limited by reducing the power supplied to the internal control blocks, which unfortunately also reduces the speed and accuracy of the system. Equally, features such as zero-crossing detection and current sensing must operate at high performance levels or the entire converter operation will be compromised.

In modern switching converters the main techniques to improve losses use MOSFETs rather than rectifier diodes. When a MOSFET is used as a synchronous switch, the current normally flows in reverse (source to drain), allowing the integrated diode to conduct current during its inactive time. Because of the very low channel resistance in power MOSFETs, the voltage of the rectifier diode can be reduced to a few millivolts, increasing peak efficiency to well above 90%.

MOSFET manufacturers have optimised their features primarily in two ways: by improving the switching characteristics (speed) and increasing cell density, which means that on-state resistance is significantly lower; $R_{DS(on)}$ and current are the two dominant factors in MOSFET conduction loss.

The power loss of the MOSFET in the buck converter can be split into four categories: switching losses, on-state losses, off-state losses and gate losses. Switching losses are difficult to study accurately because the parameters vary greatly with temperature and parasitic elements in the circuit; see Figure 5.

Suitable Power Solutions

The proliferation of energy harvesting is a key factor for low-power solutions such as WSN devices and system status monitoring in machines. The development of new processes and power management technologies can help reduce energy consumption of devices, and selecting the right active and passive components for a product will greatly improve the sensor node's energy profile.

One key parameter for getting a good battery life is to ensure that the processor is in a low-power standby mode as much as possible, and that wireless communication is kept to a minimum.

With many factors affecting battery life, it can be a complex task to estimate it correctly for a project, and it takes a long time to compare different approaches.

The power demands of a smartwatch with a colour screen, wireless connection, on-going alerts and notifications and even call-making ability have greatly increased its power requirements. By studying new opportunities for energy harvesting with low power DC-DC solutions will help significantly improve the efficiency of such wearable electronic systems. ●

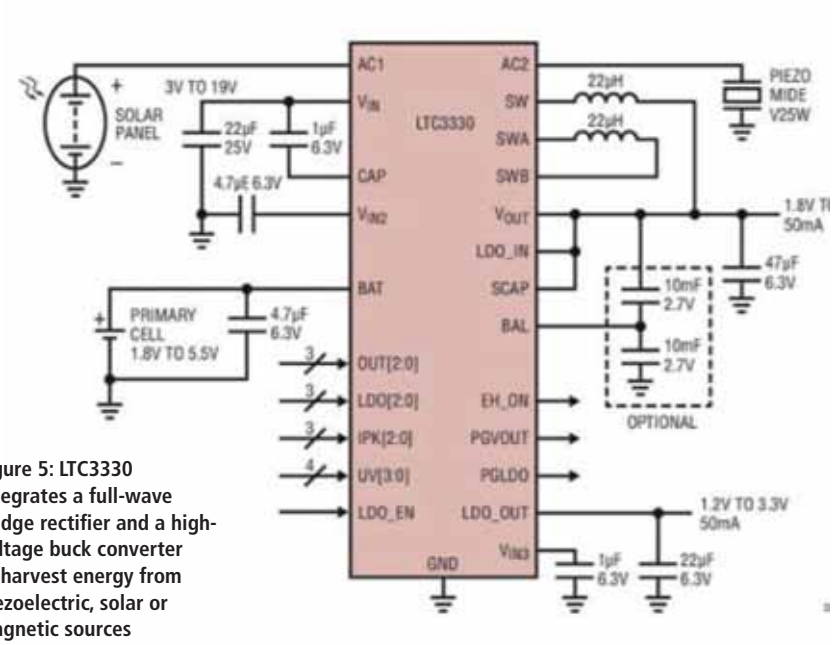


Figure 5: LTC3330 integrates a full-wave bridge rectifier and a high-voltage buck converter to harvest energy from piezoelectric, solar or magnetic sources

A Fully-Restored 26-T Full-Adder for Energy-Efficient Arithmetic Applications

By Dr. Shabbir Majeed Chaudhry, Assistant Professor, Department of Electrical Engineering at the University of Engineering and Technology in Taxila, Pakistan

The rapid integration of electronic devices in a single chip is placing a major strain on power consumption, especially in mobile and portable systems. Energy efficiency has become one of the most important requirements in modern electronics, making embedded design challenging for engineers who are expected to deliver high-performance circuits on super-small chips but at very low power.

In arithmetic circuits, the amount of energy spent during a task's operation is called the power delay product (PDP). In most modern VLSI circuits, including MPUs and application-specific digital signal processers, the full adder is a significant building block for performing arithmetic operations, such as addition, subtraction, multiplication, division and address generation. So, the PDP generated by the full adder affects the overall performance of the entire system, making the design of an energy-efficient full adder of significant interest to researchers. In addition to low power consumption, the full adder also needs to have small delays for better system performance.

Performance Comparisons

In this article we present a new full-adder design and compare it with full adders with alternative internal logic structures. The full adders are implemented using different Boolean functions to obtain XOR/XNOR and AND/OR outputs, which are then multiplexed to obtain balanced sum and carry outputs. Some of the logic circuits used for their implementation include a differential cascade voltage switch (DCVS), CMOS standard design, complementary pass transistor logic (CPL), swing restored CPL (SRCPL), double-pass transistor logic (DPL) and other, hybrid logic structures.

The structure shown in Figure 1 is used as a basic unit in most enhancements of the 1-bit full-adder module. In this configuration the adder has been designed with three main blocks: XOR and XNOR (Block 1), a multiplexer to obtain the sum (S_o) (Block 2), and a second multiplexer to obtain the carry (C_o) (Block 3).

Table 1: Truth table for the 1-bit full-adder

INPUTS			OUTPUTS	
C_i	B	A	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

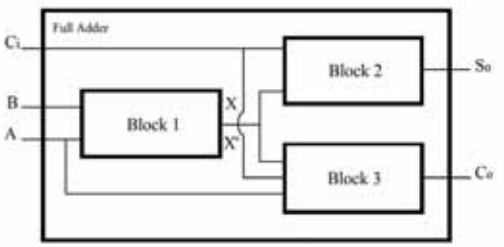


Figure 1: Three-block full adder

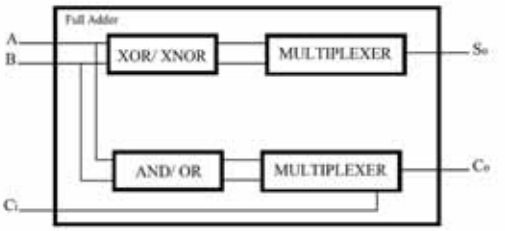


Figure 2: Alternative logic design

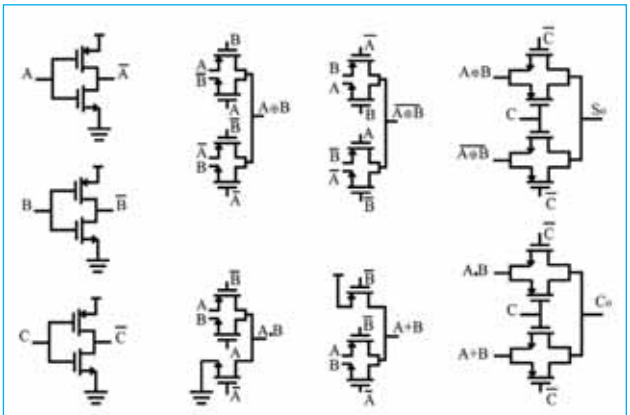


Figure 3: 28-TDPL-based full-adder design

The configuration of the block helps the propagation delay problem, which largely depends on the voltage swing generated by $A \oplus B$ and its complement $\overline{A \oplus B}$ created within that block. This signal is further used to drive the other blocks in the circuit, where delay occurs. The maximum voltage swing here is the difference between VDD and VSS, and this design requires intermediate signals (X and X') on which the output selection depends. But this hinders the efficiency of this design, so a solution is required that doesn't depend on intermediate signals for output selection.

Figure 2 shows an alternative logic structure, designed to derive $A \oplus B$ and $\overline{A \oplus B}$. Another block is used to obtain $A \bullet B$ and $A + B$ signals, with two more multiplexers to obtain the sum (S_o) and carry (C_o). The multiplexers are driven by C_i to get the respective outputs; in the truth table of this full adder (Table 1), it can be seen that S_o is $A \oplus B$ when C_i is 0, and becomes $\overline{A \oplus B}$ when C_i is 1. Similarly, C_o is $A \bullet B$ when C_i is 0, and $A + B$ when C_i is 1.

For low-power adders, hybrid CMOS logic styles have also been used; see the structures of 28-T, 26-T (our own design), 15-T and MCIT full adders in Figures 3-6.

The Proposed 26-T Adder

For our full adder, we've used double-pass transistor logic. We replaced the XOR and XNOR block with fully-restored logic to obtain the XNOR/XOR function. In a fully-restored logic gate, a PMOS transistor is used only to pass a 1 and an NMOS a 0, ensuring that the output levels are not degraded.

Our design resulted in a reduced number of transistors in the circuit – only six in total, with minimal size. All PMOS transistors have width(W)/length(L) of 120nm/120nm, while NMOS W/L = 120nm/ 240nm.

One other approach to realise the XOR/XNOR function is to implement the XOR logic and then generate the XNOR function using an inverter. However, this approach results in delayed outputs and unequal output arrival time of the XOR and XNOR outputs to the successive stages, increasing the chance of glitches in the system.

A better approach would be to use separate blocks to implement the XOR and XNOR functions, but this will increase transistor count. By comparison, our XOR/XNOR block produces the XOR and XNOR outputs simultaneously and overcomes the problem of unequal delays.

We made two more modifications to our structure to address delays:

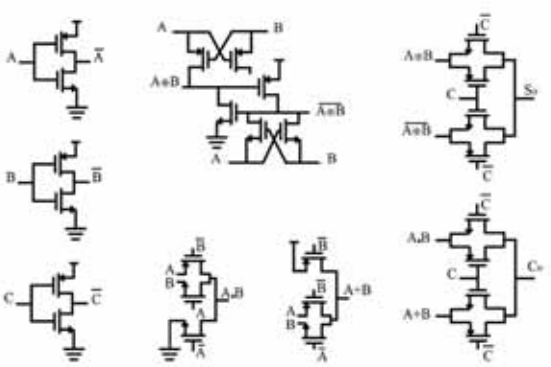


Figure 4: The proposed 26-T fully-restored full-adder structure

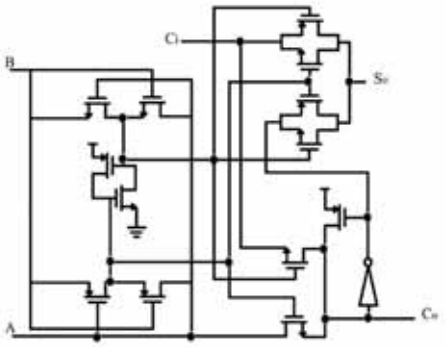


Figure 5: 15-T full-adder structure

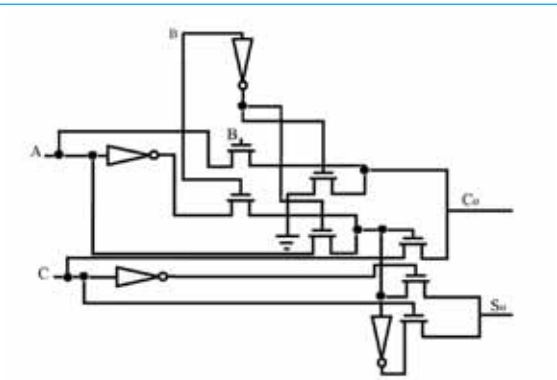


Figure 6: 15-T MCIT-based full adder

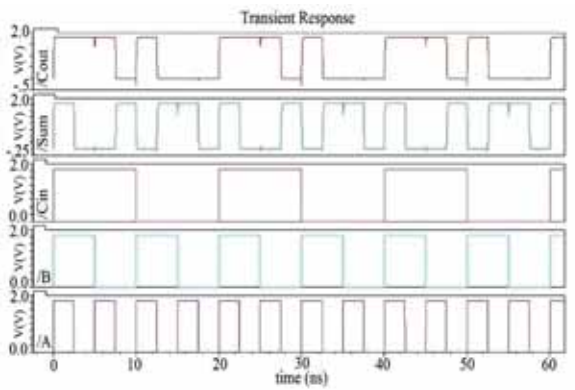


Figure 7: The input and output waveforms of the 28-T DPL-based full adder

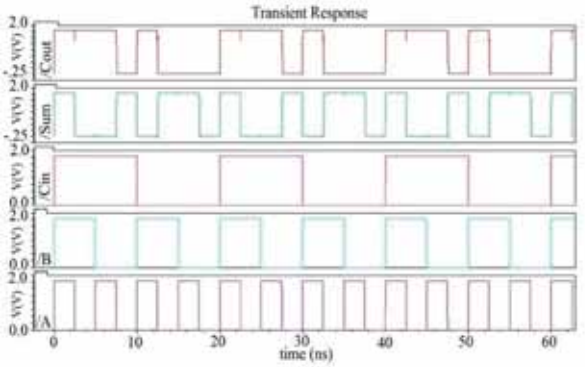


Figure 8: The input and output waveforms of the proposed 26-T DPL-based full adder

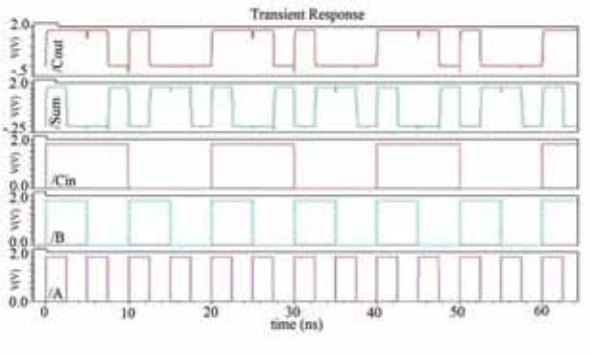


Figure 9: The input and output waveforms of the 15-T full adder

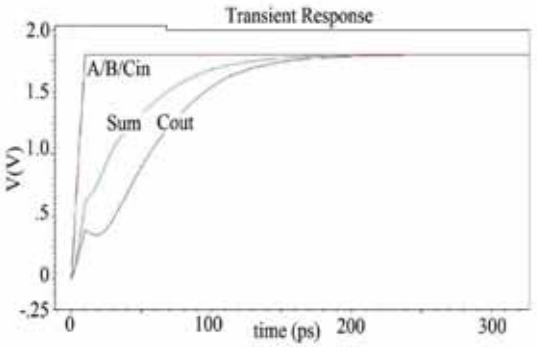


Figure 10: Time delay simulation results for the 28-T DPL-based adder

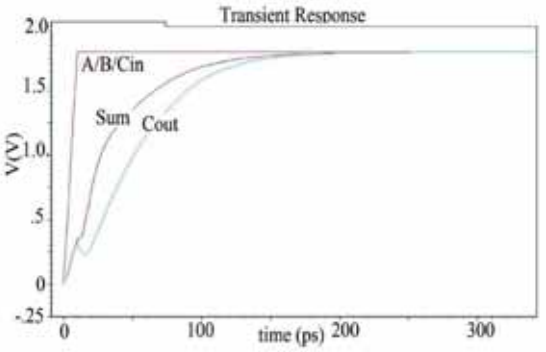


Figure 11: Time delay simulation results for the proposed 26-T structure

- Instead of internally-generated control signals, we used the C_i input signal to select the output of the multiplexers.
- We added separate blocks for S_o and C_o to separately adjust the propagation delay for each; S_o can be precisely matched at the output to make the output delays equal.

Due to the regenerative feedback introduced by the pull-up and pull-down transistors, the threshold voltage drop problem that occurs in the pass transistor logic is eliminated from both outputs, hence a full voltage swing is achieved.

Our proposed full-adder cell implements the following Boolean expressions to produce the S_o and C_o outputs:

$$S_o = (A \oplus B)\overline{C} + \overline{(A \oplus B)}C$$

$$C_o = (A \bullet B)\overline{C} + (A + B)C$$

These outputs are taken from the multiplexers (MUX). They were realised with transmission gates (TGs) that are simple and fast.

$$P_{AVG} = P_{DYNAMIC} + P_{LEAK} + P_{SHORT\text{-}CIRCUIT}$$

$$P_{DYNAMIC} = f \times C \times V_{DD}^2$$

where f = frequency, C = Capacitance

$$P_{SHORT\text{-}CIRCUIT} = I_{SHORT\text{-}CIRCUIT} \times V_{DD}$$

$$P_{LEAK} = I_{LEAK} \times V_{DD}$$

The layouts of the proposed full adder on 90nm and 180nm CMOS are shown in Figures 14 and 15. Compared to other structures, the chip area of our design was reduced by 58% and power by 91%.

Performance parameters measured at the input frequency of 200MHz are shown in Table 2. The 15-T full-adder structure of Figure 5 has fewer transistors than the 26-T unit, but it consumes more power, making our solution an appropriate choice for energy-efficient applications requiring small chip sizes. ●

Figures 12-15 & Table 2 >

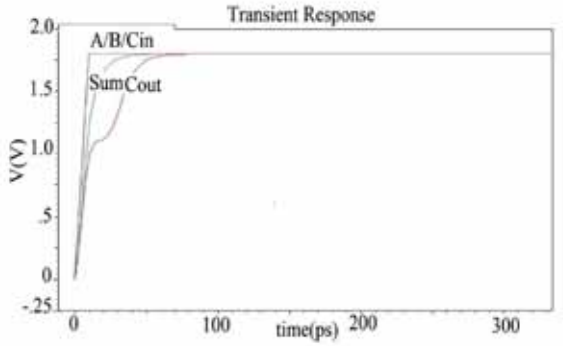


Figure12: Time delay simulation results for the 15-T structure

Figure 13: Power comparison for the frequency range of 25-300MHz

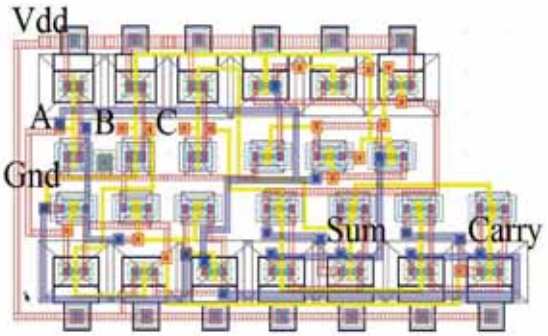


Figure14: Layout for the proposed full-adder in 90nm CMOS

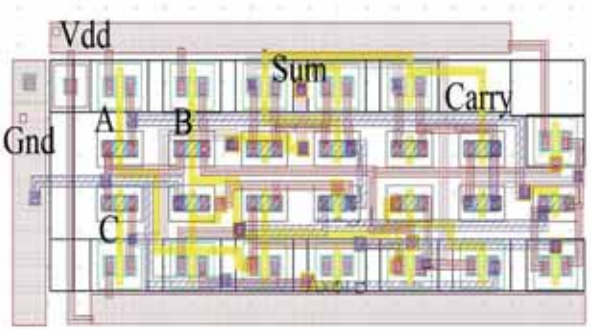


Figure15: Layout for the proposed full adder in 180nm CMOS

RESULTS OFSIMULATION FOR FULL-ADDERS COMPARED (POWER (µW), DELAY (pS), PDP IN (µW.nS), AREA (µm^2) AND VDD(V)

SCHEME	TECHNO-LOGY	AVG POWER	POWER SUPPLIED	DYNAMIC POWER	STATIC POWER	SHORT CIRCUIT POWER	DELAY	PDP	AREA	$V_{DD(MIN)}$
NEW 14 T	180nm	293.8	101.2	145.8	2.7	145.3	372	109.3	257	1.2
HPSC	180nm	291.3	169.0	186.7	0.0	104.7	425	123.8	412	1.2
HYBRID	180nm	238.7	124.2	204.1	0.0	34.6	287	68.5	459	0.7
HYBRID CMOS	180nm	225.5	176.8	177.5	0.0	48.0	325	73.3	427	0.8
CPL	180nm	145.3	135.7	103.7	0.2	41.4	284	41.3	378	0.6
SR-CPL	180nm	60.6	48.4	54.5	0.0	6.1	278	16.8	243	0.6
MCIT *	65nm	8.165	-	-	-	-	60	0.5	800	-
Internal Logic** Structure	90nm	4.938	-	-	-	-	38.54	0.18	-	0.4
MCIT-90 Ours***	90nm	31.07	11.03	31.06	0.0	4.2n	34	1.1	-	1
MCIT-180Ours	180nm	48.54	14.29	48.53	0.0	3.1n	46	2.23	-	1
15T-90 Ours	90nm	25.1	16.3	25.08	0.0	19.15n	10	0.25	-	0.8
15T-180 Ours	180nm	11.57	7.5	11.55	0.0	10.5n	15	.17	-	0.8
DPL-90 Ours	90nm	5.62	3.82	5.61	0.0	5.38n	50	0.28	166	0.8
DPL-180 Ours	180nm	55.1	34.7	53.8	0.0	1.3	289	15.9	246	0.6
Our 26T-90 DESIGN	90nm	4.89	3.02	4.88	0.0	6.39n	48	0.23	103	0.8
Our 26T-180 'DESIGN	180nm	13.34	8.77	13.33	0.0	3.02n	167	2.23	161	0.8

Table 2: Comparison table
* supply voltage = 2.5V
** supply voltage = 1.2V and operating frequency of 100MHz
*** "Ours" means that the design is tested and simulated by us in UMC 90nm and TSMC 180nm CMOS processes for comparison

Applications for a new field-programmable analogue array based on current differencing transconductance amplifiers

By Haizhen He and Rongming Luo, Hunan University, Changsha, China

Field-programmable analogue arrays (FPAAs) are reconfigurable integrated circuits (ICs) that implement a wide variety of analogue signal processing functions. Unlike their digital counterparts, field programmable gate arrays (FPGAs), FPAAs contain configurable analogue blocks, or CABs.

FPAAs can be mainly classified into two types: discrete- and continuous-time, with the first being highly adaptable but short of bandwidth and rather noisy compared to the second. Continuous-time FPAAs are usually based on operational amplifiers, OTA-C techniques, current conveyors, or combinations of these. Although higher in bandwidth than discrete-time FPAAs, they suffer from parasitics.

CDTAs

Many active devices can be used for building current-mode circuits, including second-generation current conveyors (CCIIs) and current differencing buffered amplifiers (CDBAs).

A current-mode five-terminal active element, or a current differencing transconductance amplifier (CDTA), is shown in Figure 1.

There is a pair of low-impedance and low-parasitic input ports, virtually grounded, converting current into a difference current that flows from the Z terminal to the (outside) load. The Z terminal voltage is converted into a couple of output currents through the X terminals by an internal operational transconductance amplifier (OTA). The current gain of the whole circuit is a product of the Z-terminal impedance and the OTA transconductance. The equivalent circuit can be characterised by:

$$\begin{cases} V_p = V_n = 0V; I_{z+} = I_p - I_n \\ I_{x+} = g_m V_{z+}; I_{x-} = -g_m V_{z+} \end{cases} \quad (1)$$

where $V_{z+} = I_{z+} Z_z$, Z_z is the external impedance connected to the Z terminal and g_m the transconductance gain of the CDTA. In this case, the CDTA current gains I_{x+} and I_{x-} can be controlled with g_m.

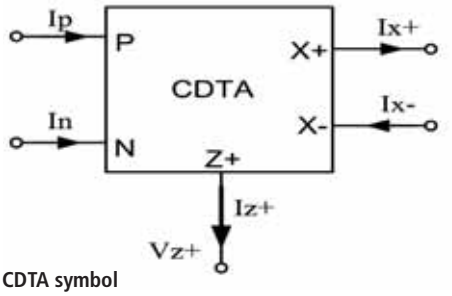


Figure 1: CDTA symbol

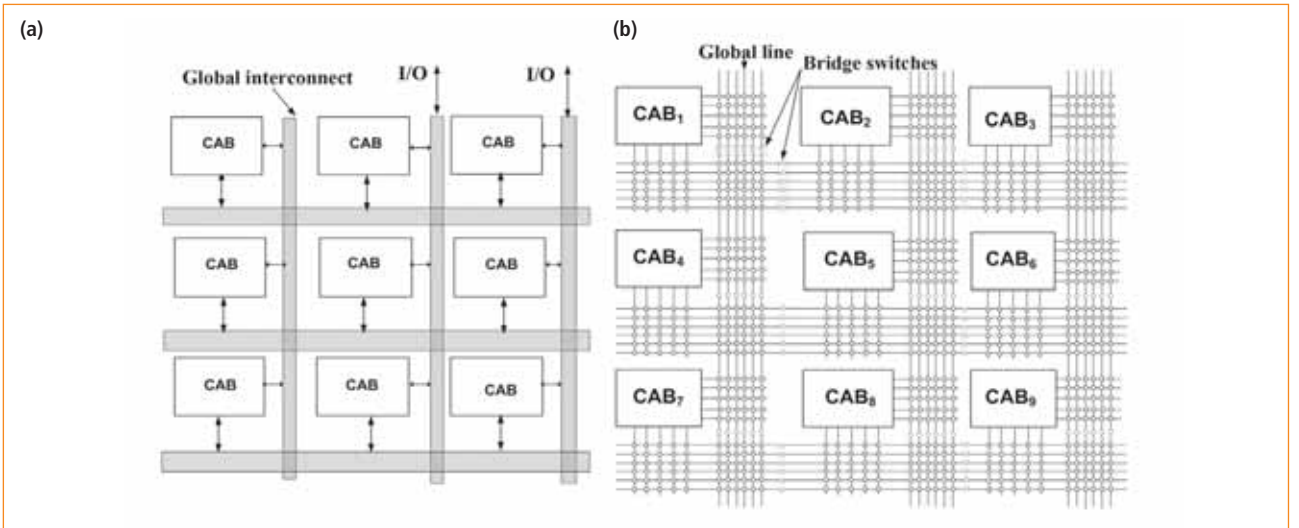


Figure 2: (a) General architecture of the proposed FPAA; (b) its routing

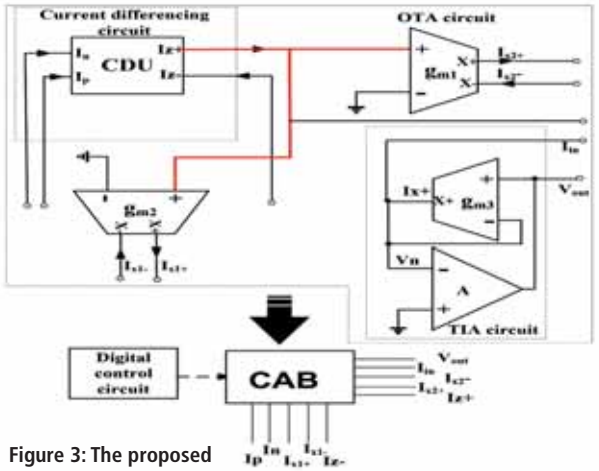


Figure 3: The proposed configurable analogue block

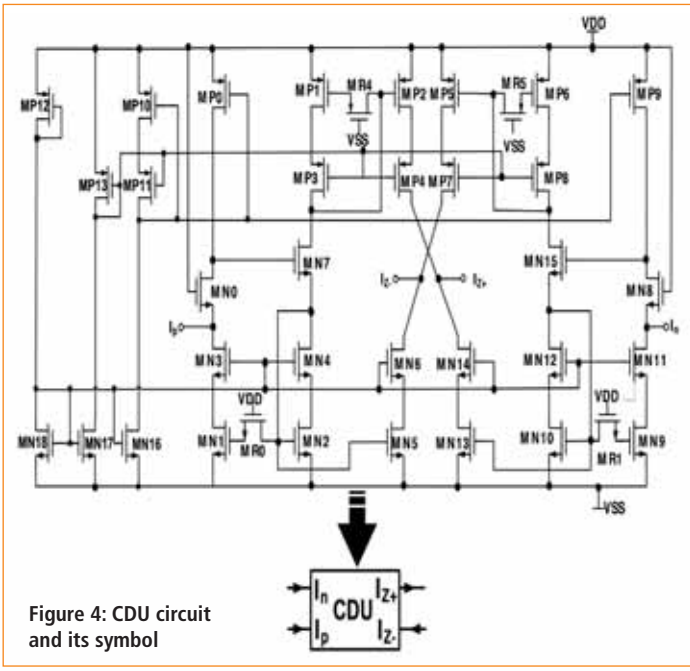


Figure 4: CDU circuit and its symbol

Even though there are many types of CDTAs, they are difficult to apply in an FPAA without modification. CDTA is a relatively complex circuit compared to others, such as the operational amplifier or OTA, for example. When using CDTA as a part of a configurable analogue block (CAB), the programmability of the FPAA will be affected.

Here, we present a novel FPAA structure with nine CABs. The CDTA in each CAB is divided into two separate sections: current differencing unit (CDU) and OTA. The solution takes full advantage of CDTA without affecting the flexibility and reusability of the FPAA. By using this type FPAA, multiple function filters, such as low-pass (LP), band-pass (BP) and with transmission zeros, can be built without changing their structure.

FPAA Architecture

The architecture of our FPAA is shown in Figure 2a. Its nine CABs are arranged in a 3×3 matrix. An interconnecting matrix comprising MOS switches allows for arbitrary connectivity between the components. The state of the switches can be set with SRAM – it's easy to obtain different circuits with its simple programming.

The routing in the proposed FPAA is shown in Figure 2b. The global lines can be vertical or horizontal, each with six further lines. Each line contains switches that bridge the

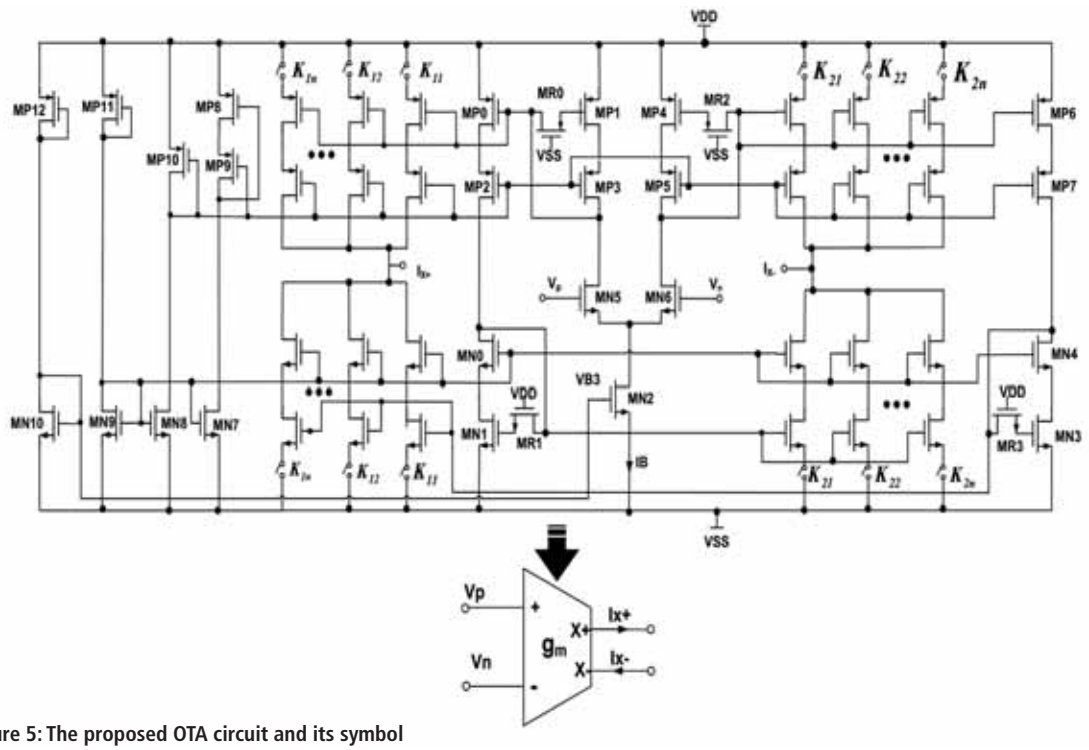


Figure 5: The proposed OTA circuit and its symbol

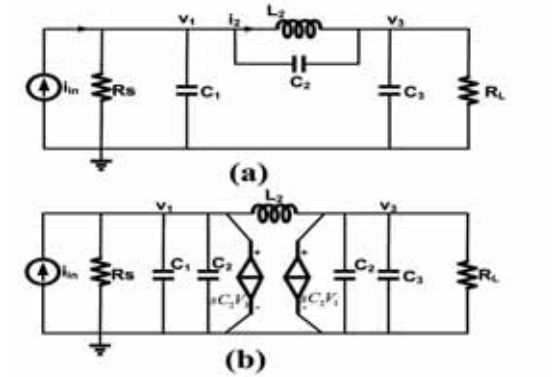


Figure 6: (a) Third-order low-pass RLC ladder filter with transmission zeros; (b) its equivalent circuit

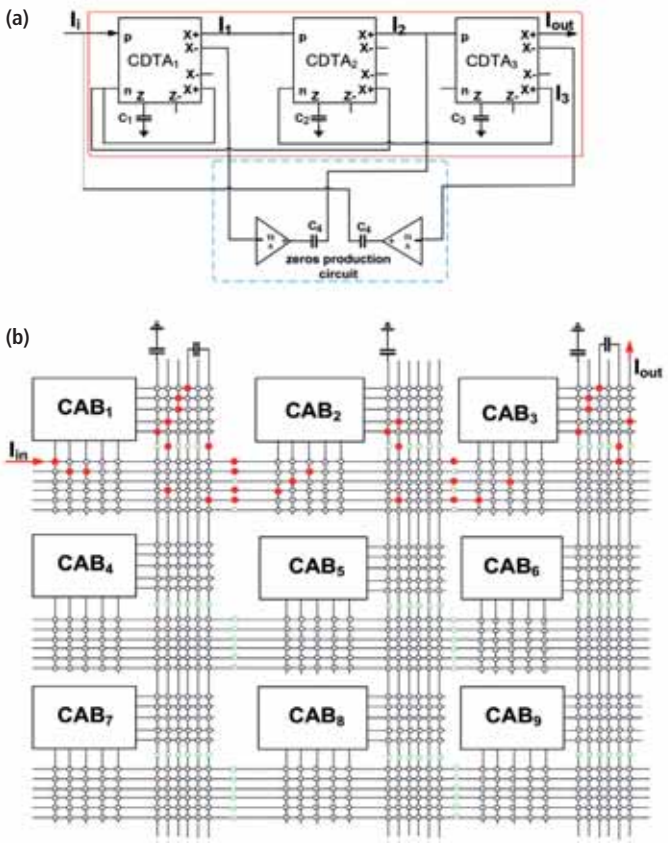


Figure 7: (a) Three-order low-pass filter with transmission zeros based on CDTA-C; (b) its wiring in the FPAA

global lines between CABs, facilitating variable-length connections without incurring any capacitance penalty. This type of structure allows for maximal programmability of the FPAA.

CAB Circuit Description

Figure 3 shows the components in our proposed CAB. Each block contains a current differencing unit, three reconfigurable operational transconductance amplifiers and a common operational amplifier.

The CDU circuit, which has been modified from CDTA, is shown in Figure 4. It is based on a current-mirror resistive compensation technique, which improves the overall bandwidth. To expand the application function of the CDU, there's an auxiliary output terminal z- that produces a differential current I_n-I_p; its equivalent circuit can be characterised with $I_{z+} = I_p$-$I_n = -I_{z-}$.

Programmable OTA Elements

Figure 5 shows the proposed OTA. The tunability of a traditional OTA circuit was achieved by varying the tail current source to adjust the transconductance gain (g_m) of the OTA stage. Nonetheless, this analogue tuning approach will affect the operating point and linearity of the circuit. Moreover, the magnitude of g_m is the square root of the tail current source I_B, which means a large change in I_B incurs only a small change in g_m.

To optimise the OTA performance, an evolutionary approach to tune the current gain I_{x+} and I_{x-} is to digitally control the output of the OTA via a programmable current mirror. Assuming MN5 and MN6 are matched and operated in the saturation region, the OTA's I_{x+} and I_{x-} are then:

$$I_{x+} = \sum_{i=-n}^{n} 2^i K_{1i} \sqrt{\mu C_{ox}(W/L) I_B} V_Z = \alpha_1 g_m V_Z$$
$$I_{x-} = \sum_{i=-n}^{n} -2^i K_{2i} \sqrt{\mu C_{ox}(W/L) I_B} V_Z = \alpha_2 g_m V_Z \quad (2)$$

where I_B is the bias current, controlled by the gate voltage of transistor MN2; μ is the carrier mobility; C_{ox} is the gate oxide capacitance per unit area; and W and L are the channel width and length of MN5 and MN6, respectively. K_{1i} and K_{2i} indicate the switch state of each programmable current mirror, which can be controlled by the FPAA's digital control circuit. The symbol α is an n-bit digitally-programmable gain factor controlled by K_{1i} and K_{2i}. Equation 2 shows that the variable transconductance gain can be determined by setting different values for α.

The programmable OTA can be used alone or in combination with a CDU to build a standard current-mode device, or CDTA. The red line in Figure 3 shows how the CDTA might be connected.

To apply the FPAA to a voltage-mode circuit, in each CAB there's a transimpedance amplifier (TIA), consisting of an OTA and an amplifier. The input and output characteristics are then:

$$V_{out} = -I_{in} / g_m \quad (3)$$

Filter Circuits

The proposed FPAA can be used to build different current- or voltage-mode analogue signal processing systems. In this article, we will describe the performance of the FPAA in a high-order current-mode low-pass and band-pass filter with transmission zeros.

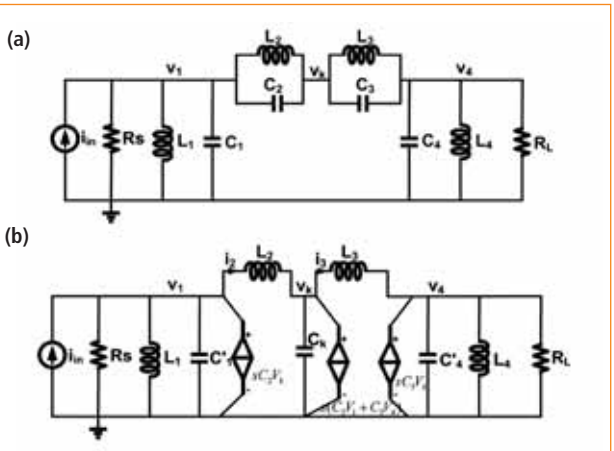


Figure 8: (a) Three-order band-pass RLC ladder filter with transmission zeros; (b) its equivalent circuit

Low-pass filter

Here we propose a configuration of a continuous-time current-mode leap-frog low-pass filter with transmission zeros, based on CDTA-C that uses a passive RLC ladder circuit. This would be a third-order low-pass RLC ladder with transmission zeros circuit, as shown in Figure 6. For simplification, we replaced the capacitor C_2 in the series branch with a voltage-controlled current source (VCCS).

The current-mode low-pass filter with transmission zeros can be developed with Equation 4 and analysis of its equivalent circuit. To apply voltage-mode circuits to current mode, a gain coefficient A is needed:

$$\begin{cases} v_1(s) = \dfrac{1}{sC_1' + G_{Rs}}\left(i_{in}(s) - i_2(s) + sC_2 v_3(s)\right) = \dfrac{I_1(s)}{A} \\ i_2(s) = \dfrac{1}{sL_2}\left(v_1(s) - v_3(s)\right) = \dfrac{I_2(s)}{A} \\ v_3(s) = \dfrac{1}{sC_3' + G_{RI}}\left(i_2(s) + sC_2 v_1(s)\right) = \dfrac{I_3(s)}{A} \end{cases} \quad (4)$$

where $G_{RI} = 1/R_I$, $G_{Rs} = 1/R_s$, $C_1' = C_1 + C_2$, $C_3' = C_2 + C_3$. We can transform the passive RLC ladder circuit into a filter based on CDTA-C according to Equation 4; see Figure 7a. Equation 5 shows its transfer function H(s):

$$H(s) = \frac{I_o(s)}{I_i(s)} = \frac{1 + L_2 C_2 s^2}{(C_1' L_2 C_3' - L_2 C_2^2)s^3 + L_2 C_3' s^2 + (C_1' + C_3' - 2C_2)s + 1} \quad (5)$$

where $C_1' = c_1/g_{m1}$, $L_2 = c_2/g_{m2}$, $C_3' = c_3/g_{m3}$, $C_2 = c_4/g_{m4}$. In this case, the frequency of the transmission zeros ω_k is:

$$\omega_k = \sqrt{\frac{g_{m2} g_{m4}}{c_2 c_4}} \quad (6)$$

Clearly, ω_k can be controlled electronically by adjusting the values of g_{m2} and g_{m4}.

Figure 7b shows the map of this filter implemented in an FPAA. The red spots on the global lines indicate that the switches are turned on to allow the FPAA's CABs to access the global lines or to enable the interconnections.

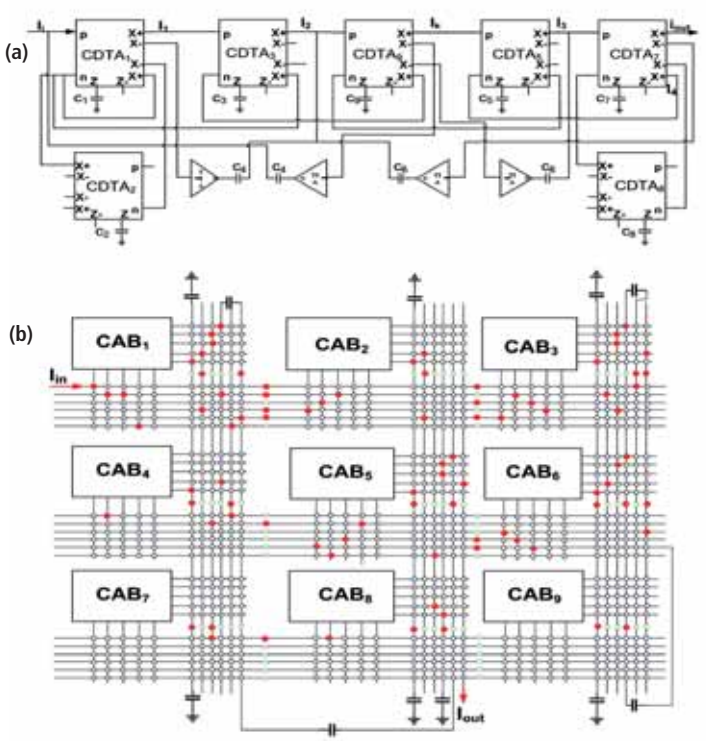


Figure 9: (a) Three-order band-pass filter with transmission zeros based on CDTA-C; (b) its wiring in FPAA

Band-pass filter

For a band-pass filter, the band-pass RLC ladder filter with transmission zeros is shown in Figure 8.

The circuit can be described by the following set of equations:

$$\begin{cases} v_1(s) = \dfrac{1}{sC_1' + G_{Rs}}\left(i_{in}(s) - i_2(s) - \dfrac{v_1(s)}{sL_1} + sC_2 v_4(s)\right) = \dfrac{I_1(s)}{A} \\ i_2(s) = \dfrac{1}{sL_2}\left(v_3(s) - v_4(s)\right) = \dfrac{I_2(s)}{A} \\ v_4(s) = \dfrac{1}{sC_4'}\left(i_2(s) - i_3(s) + sC_2\left(v_1(s) + v_4(s)\right)\right) = \dfrac{I_4(s)}{A} \\ i_3(s) = \dfrac{1}{sL_3}\left(v_4(s) - v_4(s)\right) = \dfrac{I_3(s)}{A} \\ v_4(s) = \dfrac{1}{sC_4' + G_{RI}}\left(i_3(s) + sC_2 v_1(s) - \dfrac{v_4(s)}{sL_4}\right) = \dfrac{I_4(s)}{A} \end{cases} \quad (7)$$

where $C_1' = C_1 + C_2$, $C_k = C_2 + C_3$, $C_4' = C_3 + C_4$. The same principles are applied to obtain the map of the filter based on the CDTA-C in Figure 9a. Its parameters are determined by:

$$\begin{cases} C_1' = \dfrac{c_1}{g_{m1}}, L_1 = \dfrac{c_2}{g_{m2}} ; C_2 = \dfrac{c_4}{g_{m4}}, L_2 = \dfrac{c_3}{g_{m3}} \\ C_3 = \dfrac{c_6}{g_{m6}}, L_3 = \dfrac{c_5}{g_{m5}} ; C_4' = \dfrac{c_7}{g_{m7}}, L_4 = \dfrac{c_8}{g_{m8}} ; C_k = \dfrac{c_9}{g_{m9}} \end{cases} \quad (8)$$

Following on from Equation 7, the frequency of the transmission zeros ω_{k1} and ω_{k2} of the band-pass filter are:

$$\omega_{k1} = \sqrt{\frac{g_{m3} g_{m4}}{c_3 c_4}}, \omega_{k2} = \sqrt{\frac{g_{m5} g_{m6}}{c_5 c_6}} \quad (9)$$

Equation 9 shows that the locations of two transmission zeros can be adjusted by varying the g_m values. Figure 9b shows the wiring of this filter in the FPAA.

Non-Ideal Analysis

Considering the non-ideal CDU and OTA, the performance of the proposed filter may deviate from the theoretical frequency response due to tracking errors and parasitic effects. Then, the output currents can be rewritten as:

$$\begin{cases} I_{z+} = \beta_p I_p - \beta_n I_n ; I_{z-} = \beta_n I_n - \beta_p I_p \\ I_{x+} = \gamma g_m V_{z+} ; I_{x-} = -\gamma g_m V_{z+} \end{cases} \quad (10)$$

where β_n and β_p denote the current transfer gains from n and p to the Z+ and Z- terminals, γ is the transconductance inaccuracy factor from Z+ to the X± terminal, and $\beta_n = 1-\varepsilon_n$, $\beta_p = 1-\varepsilon_p$, $\gamma = 1-\varepsilon_g$, where ε_n, ε_p and ε_g are the tracking errors. These tracking errors slightly deflect the transfer gains β_n, β_p and γ from the ideal unit values, which are a lot lower than 1. In practice this means that the errors will affect the magnitude gain, cutoff frequency and quality factor of the filter.

In the case of parasitic effects for the CDTA, the filter frequency response associated with these influences can be easily determined. The model of a non-ideal CDTA is shown in Figure 10a, characterised by the input impedances R_n and R_p and output parasitic impedances, including parasitic resistors R_{z+}, R_{z-}, R_{x+} and R_{x-} and capacitors C_{z+}, C_{z-}, C_{x+}, C_{x-}. Here R_{x+} and R_{x-} and C_{x+} and C_{x-} typically depend on the switch state in the OTA.

For simplicity, a lossy integrator is shown in Figure 10b. It is easy to observe that the parasitic capacitors C_{Z+} can be absorbed into the external capacitor and the parasitic resistor R_{Z+} at terminal Z will change the type of impedance, which should be of a purely capacitive character. In practice, $C >> C_{Z+}$. We'll ignore R_{Z+}, C_{Z+} and the two OTAs with same g_m, making the transfer function of the lossy integrator:

$$H(s) = \frac{R_{g1}}{C_{g1}R_{g1}R_g s + (R_g + R_{g1})} \cdot \frac{\gamma_1\beta_p g_m \left[C_{z2}R_{z2}R_g s + (R_g + R_{z2})\right]}{CR_gC_{z2}R_{z2}s^2 + C(R_g + R_{z2})s + \gamma_2\beta_p g_m R_{z2}} \quad (11)$$

From Equation 11 it's clear that the parasitic parameters affect the high-frequency performance of the integrator. This can be helped by a good CDTA design, which will alleviate the non-ideal effects.

Simulation Results and Applications

We verified the characteristics of the proposed circuits with the Cadence IC5141 tool. We implemented it in BSIM3v3.3 model in a standard Chartered 0.18µm CMOS process. We used CMOS for the simulation programme, and a ±1.2V power supply. The OTA g_m was set to roughly 1mS by adjusting the tail current source I_B. In this process, one example is given for each type of filter. Other frequency response curves can be obtained with similar methods.

The parameters of the three-order low-pass RLC ladder filter with transmission zeros were set with software tools. For a filter with a cutoff frequency of 10MHz, the source and load resistance values are 1Ω, passband ripple is 0.05dB, and C_1, L_2, C_2 and C_3 are 6.89nF, 5.96nH, 24.98nF and 6.89nF, respectively. We also set c_1, c_2, c_3 and c_4 to 30pF, 6pF, 30pF and 25pF, respectively.

(a) (b)

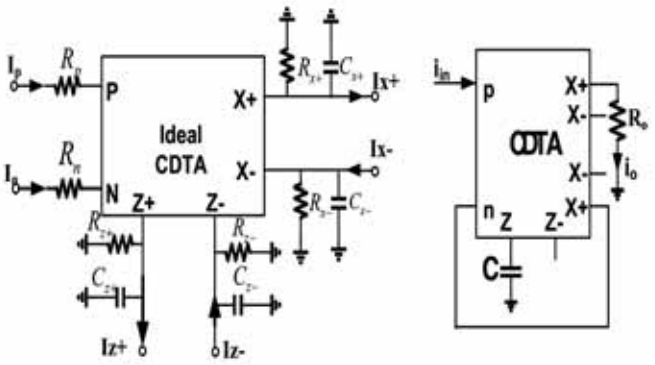
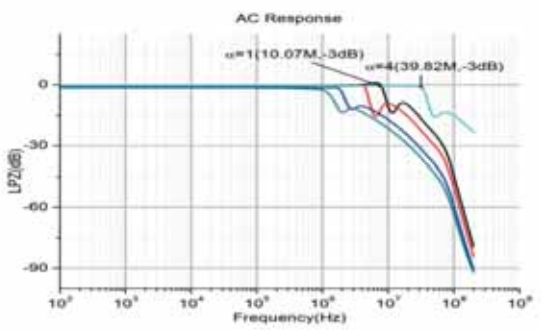


Figure 10: (a) Non-ideal CDTA model; and (b) lossy integrator model

(a)



(b)

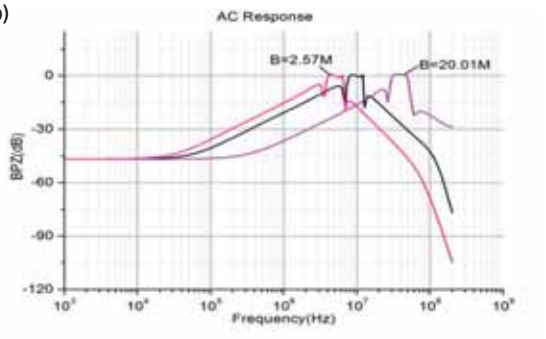


Figure 11 (a) Frequency response of the low-pass filter with transmission zeros for various cutoff frequencies; (b) Frequency response of the band-pass filter with transmission zeros for various centre frequencies and bands

When α of every OTA is set to 1, the simulation result for the cutoff frequency of the low-pass filter with transmission zeros is 10.07M, very close to the theoretical value. The frequency response of the filter for variable cutoff frequency is shown in Figure 11a. The five curves correspond to the different values of α: 0.125, 0.25, 0.5, 1 and 4; the cutoff frequency varies from 1.31-39.82MHz.

As for a band-pass filter with transmission zeros, consider a filter with a centre frequency of 10MHz, bandwidth of 5MHz, source and load resistance values of 1Ω, passband ripple of 0.05dB and stop-band ratio of 1.2. The filter has been designed with $\alpha = 1$, $c_1 = 40pF$, $c_2 = c_8 = 35pF$, $c_3 = 13.5pF$, $c_4 = 32pF$, $c_5 = 6.5pF$, $c_6 = 20pF$, $c_7 = 25pF$, $c_9 = 52pF$.

Figure 11b shows the frequency response of the band-pass filter with transmission zeros. The three curves correspond to different centre frequencies, i.e. 4.83, 9.81 and 38.56, and bandwidths of 2.57, 4.72 and 20.01, respectively.

Significant Simplification

Our proposed FPAA considerably simplifies the design of current-mode high-order filter circuits. Different high-order filters can be created by employing a different number of CABs and appropriately connecting the internal components. These filters don't use any resistors, which avoids the impact of resistance and reduces the area and power consumption of the FPAA. In addition, these filters exhibit both low-input and high-output impedance characteristics.

The filter parameters can be digitally tuned with α, which is the original part of the programmable OTA circuit. ●

DATA AND WORKFLOWS FOR INDUSTRY 4.0

Rittal has created a system capable of merging real and physical workflows, delivering significant improvements in efficiency for panel builders and switchgear manufacturers.

The new Rittal VX25 large enclosure system supports the control and switchgear engineering industry on the path toward Industry 4.0. The new system combines a physical enclosure with its digital twin, ensuring it will meet all future digital needs – from online configuration and engineering to assembly, automation and tracking.

The VX25 ensures 3D data is available in consistent maximum quality. The digital element supports control and switchgear manufacturers across every process along their value chain. This means electrical planning, mechanical design, purchasing, cost calculation, manufacturing and other areas of switchgear construction can always access complete, high-quality data, opening new ways to digitise processes in accordance with Industry 4.0.

www.rittal.co.uk

ALLEGRO MICROSYSTEMS ANNOUNCES NEW TECHNOLOGY

Allegro MicroSystems launched a new AxMR technology platform, which integrates high-sensitivity MR (magnetoresistive) sensor elements and high-precision BiCMOS circuits on a single silicon integrated circuit (IC). Through integration Allegro has combined its automotive grade, high-voltage wafer processes with high-accuracy, automotive-grade MR sensors. The result is a family of high-reliability, innovative, small form-factor, monolithic ICs that easily fit into industry standard packages.

Allegro's AGMR withstands harsh conditions, typically found in the automotive sector. AGMR is thermally stable to over 150°C, even in the presence of large magnetic fields.

Allegro's first generation AxMR ring-magnet Speed Sensor ICs are already in production at a Tier 1 automotive supplier of wheel speed sensors. The ICs rely on Allegro's patented signal processing algorithms to meet the needs of both standard and direction detection wheel speed sensor platforms.

www.allegromicro.com

ARDUINO AND DISTRELEC LAUNCH AUTOMATION AND ROBOTICS CONTEST

Arduino launched a global contest that challenges users of its open-source electronics platform to create innovative products that help advance the development of Industry 4.0 automation and robotics applications. The contest runs in partnership with electronics and automation distributor Distrelec.

Contestants are required to tap into the extensive range of boards, libraries and online platform available within the Arduino ecosystem. Project ideas for use in industrial automation could target remote control, energy management or predictive maintenance, for example, using the Arduino Create Cloud platform to set up, control and connect Arduino-, Intel- and Arm-based devices. Robotics projects could include designs for surveillance drones, robotic arms, rovers, or self-drive transportation, using boards such as the Arduino MKR1000 or Arduino Due to read sensors and control motors and actuators for prototyping advanced robotics systems.

https://create.arduino.cc/projecthub/contests/arduino-automation-robotics