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THE ESSENTIAL ELECTRONICS ENGINEERING MAGAZINE

High power outputs and small solution footprints

By Analog Devices

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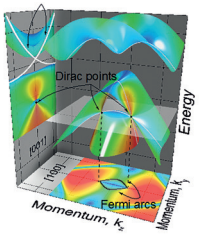

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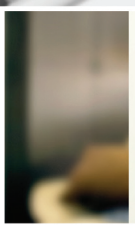
Making the Complex Simple



The IoT Security Suite for the SAMA5D2 MPU enables rapid and easy use of its advanced security features, such as ARM® TrustZone® technology and hardware cryptography, without a long learning curve. The suite covers the security requirements for IoT device manufacturers in a single, easy-to-use package. It supports storing, encrypting, decrypting and exchanging keys between devices and applications, and its easy-to-use APIs save you time.

Features

- **Trusted Boot** – Root of Trust (RoT) verified startup
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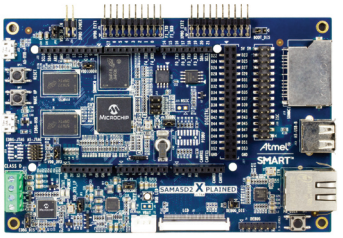
- **Secure Communications** – Authenticated device pairing and IoT cloud communications
- **Secure Firmware Update** – Securely upgrade firmware remotely

Download the IoT Security Suite Evaluation Kit (free) to get started.



SAMA5D2 Xplained Ultra Evaluation Board (ATSAMA5D2-XULT)

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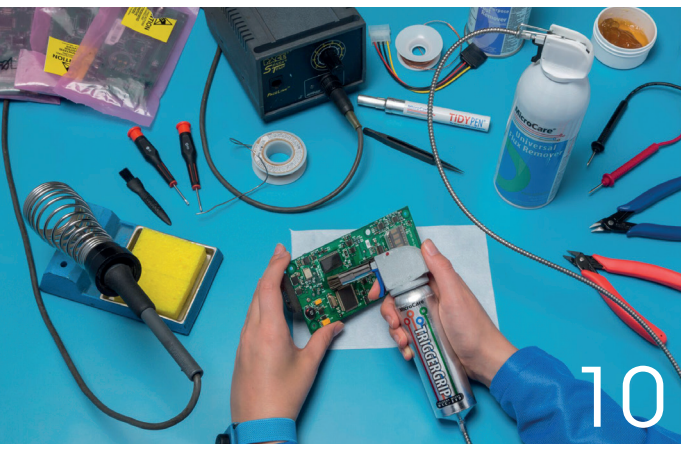

Cover supplied by ANALOG DEVICES
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HIRING THE RIGHT EMBEDDED DESIGNERS FOR THE IOT

As the Internet of Things (IoT) continues to evolve, businesses are realising that they need a whole new generation of talent with the right skills to meet the new demands. Yet, as the IoT is still relatively new, many business leaders are concerned by their own lack of knowledge of this market, and find themselves running headfirst into a set of technology and business challenges they do not yet fully understand.

In fact, Canonical's recent study of IoT professionals found that 68% are struggling to hire employees with the right skills and expertise needed to make the IoT successful. The report, called *"Defining IoT Business Models"*, found that the two most difficult IoT employees to hire are those with knowledge of embedded software development (33%) and embedded electronics (32%). These results are quite surprising given that embedded development has been around for quite some time. With hardware quickly commoditising, and monetisation and differentiation increasingly coming via software, it's only natural that businesses invest in updating their embedded software capabilities.

While 55% of IoT professionals who took part in the study see their long-term profits coming from the sale of hardware, today's engineers are taking a more cost-effective approach by abandoning custom IoT microcontrollers, made possible by the greater availability and functionality of single-board computers with fully-functioning IoT operating systems. Rather than solely focusing on the development of standalone IoT software, engineers must start looking at their hardware designs as a base upon which complex software-defined functions can be managed and run. And with vendors and consumers now expecting their devices to be endlessly upgradable, the days of selling a single-function connected device are truly over. Hence, it's no wonder that 71% of IoT professionals identify software development as one the most needed skills of the modern age.

While we believe that software development and IT department rules will still be valid for a long time to come, 'full stack' developers must be familiar with many more components – from artificial intelligence to blockchain and robotics. If companies choose a software development stack that can run as easily on the edge of the IoT network as in the cloud, then they will benefit not only from code re-use, but also from being able to use the same developer across the stack. This is particularly true in the new world of IoT where gateways run software similar to the cloud and where heavier development languages can be used at the edge thanks to increasingly powerful IoT chipsets.

Businesses also need to ensure that they choose the right operating system as this can have a huge effect on operational costs. By implementing one that can be used from the edge to the cloud affords engineers the ability to integrate the new IoT operations much faster into their workflow.

The two most difficult IoT employees to hire are those with knowledge of embedded software development and embedded electronics

To alleviate the apparent skill shortage in the near-term, we expect many businesses to outsource embedded software development through consultancies, freelance developers or system integrators. This will allow them to come to a decision whether to build these departments internally or continue to outsource. Businesses will then need to consider who is best placed within their organisation to lead IoT projects, and who is best placed to bridge the gap between the complete technologies involved and the need to create a profitable business model.

Essentially, businesses must be more agile when it comes to deciding on the 'right' people for such jobs and realise that working in IoT should not require an extensive variety of skills. After all, what is decided upon today is unlikely to remain the same in one or two years.

By Mike Bell, Executive Vice President of Devices and IoT, Canonical (www.canonical.com)

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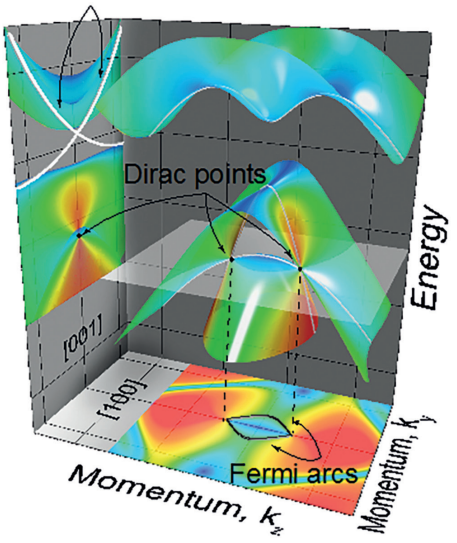
RESEARCH INTO ELECTRON STATES IN SOLIDS COULD REVOLUTIONISE ELECTRONIC DEVICES

Research led by the Universities of St Andrews and Tokyo reveals a new understanding of how to create topological electronic states in solids, which could fuel the development of improved materials for fast and energy-efficient electronic devices.

The way electrons behave inside a solid is governed by its electronic structure, an intertwined network of bands that define the allowed energies and momenta of electrons in the solid. If the right type of bands cross over, it can give rise to interesting – and potentially very useful – physical properties of materials. For example, it's been observed that isolated touching points of these bands can be stabilised by some crystalline symmetries, creating so-called Dirac fermions in the bulk electronic structure. This allows electrons to behave as though they were massless particles, effectively a bulk analogue of the atomically-thin material graphene. As well as being an exciting playground for studying fundamental concepts of particles in physics, this can lead to ultra-high mobility of charge carriers, a property that could be used to make extremely good conductors.

If the crossing is not protected, another exitation state termed a 'topological insulator' can be stabilised. Here, the bulk of the material behaves like a normal electrical insulator, but its surface supports so-called 'topological surface states' – additional bands forming protected crossing points containing only electrons localised to the material surface. In practical terms, these surface states provide a conductive shell around the material bulk, which can remain intact even when the material has defects or damage. An electronic insulator can, therefore, be transformed into a good conductor at its surface, with potential applications in proposed schemes for electronics that exploit the electron's spin as well as its charge.

Given both the theoretical and practical interest in such systems, recently there's been enormous effort in identifying compounds where these states can be found. To develop a set of guiding principles toward achieving this, an international team of scientists from the UK, Asia and Europe have combined detailed theoretical modelling with state-of-the-art experimental studies. Their findings demonstrate a mechanism for generating multiple sets of topological surface states and three-dimensional Dirac fermions, all within the same material.



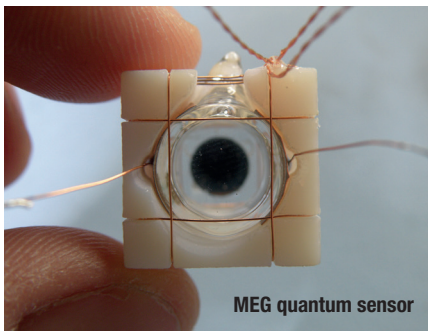
Topological surface states of electrons in solids

Key to the researchers' findings is a disparity in how electrons can move along different directions of the crystal, coupled with a simple rotational symmetry that can protect some band crossings.

LETI DEVELOPS MEG TECHNOLOGY TO GUIDE SURGEONS DURING BRAIN SURGERY

Leti, a research institute of CEA Tech, is developing next-generation magneto-encephalography (MEG) technology that could significantly reduce the cost of MEG systems and scans, improve diagnosis and treatment for epilepsy patients, and guide surgeons performing brain surgery.

MEG is an imaging technique that measures brain function based on magnetic fields produced by the brain's electrical activity. It identifies the locality of neural signals with improved spatial resolution.



MEG quantum sensor

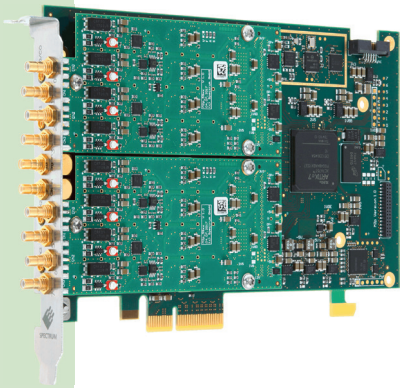
Current MEG systems are cooled cryogenically, a process that requires periodic re-filling of super-cold liquids. The maintenance-free Leti device operates at room temperature, eliminating the need for cryogenic cooling and reducing the weight of the device's magnetic shield from 5,000kg to 150kg.

Leti refined its space quantum sensor, a device used in European Space Agency missions, to achieve performance superior to current MEG systems but still be five times cheaper. In addition, Leti's sensors can provide more information on brain activity due to their vector-type nature, improving localisation of epileptic foci.

The quantum sensor is an optical pumping magnetometer with improved sensitivity thanks to the use of a low-noise laser source and the choice of magnetic resonance optimised for measurement of very low magnetic fields. The laser, which can sense the movement of 100 billion atoms acting like small magnets, is an essential component of the high-performance sensor.

The MEG project was coordinated by Blumorpho, a Paris-based innovation accelerator.

"This new generation of MEG equipment will deliver dramatically-improved visualisation of brain activity to support neuromedicine's evolution to non-invasive surgery and regenerative medicine," said Regis Hamelin, Blumorpho CTO.



Triggering and synchronisation in modular digitisers

BY OLIVER ROVINI AND GREG TATE, SPECTRUM INSTRUMENTATION, AND ARTHUR PINI, INDEPENDENT CONSULTANT

Digitisers convert signals into a series of measurements, output as a numerical array of amplitude values versus time. To make this information useful, the time information is typically related to a specific reference point, most commonly the trigger position. The trigger point can be something that occurs within the measured signal or other, external source. For repetitive signals, the trigger must be stable to enable comparisons between measurements from different acquisitions.

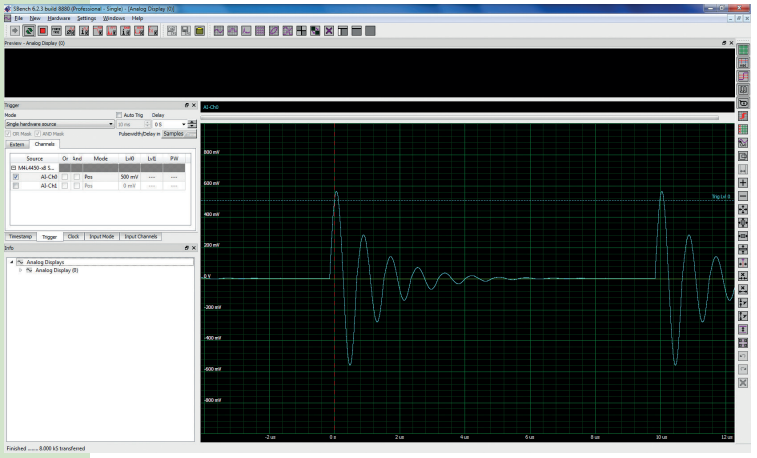


Figure 1: Example of a basic edge trigger defining the zero-time value on the time axis (marked by the vertical dashed line), when the waveform crosses the trigger level (horizontal dashed line) with a positive slope

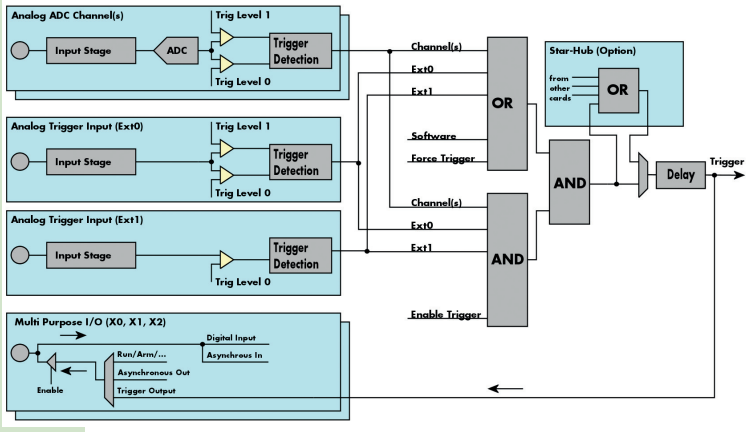


Figure 2: The block diagram of the 'Trigger Engine' of a digitiser showing the trigger sources and trigger logic for this general purpose digitiser

Triggering

Triggering is an essential function for any instrument that acquires and digitises signals. The most common trigger method uses the signal that's fed into one of the digitiser's channels. The basic principle is that a defined point on the waveform is detected and this 'trigger event' is marked as a known position on the acquired data.

Figure 1 shows an example of a basic edge trigger. The signal source is the input channel, with the trigger event occurring when the waveform crosses the trigger level at 500mV with a positive slope. This position is marked as the zero-time point on the time axis. If the signal is repetitive, the digitiser will be triggered at the same point each time a new acquisition is made, resulting in a stable display.

The wide variation in possible signal waveforms, levels and timing requires that the digitiser's trigger circuit be extremely flexible. Figure 2 shows a block diagram of the trigger 'engine' of a digitiser. This shows the wide range of trigger conditions that are supported in modern digitisers.

The hardware trigger sources are shown on the left side of the block diagram. They include any of the input channels and either of the two external trigger inputs (Ext0 or Ext1). Each of these sources supports multiple trigger types. The multi-purpose I/O lines can be used to report the digitiser's run/arm state and provide a trigger output signal, among other functions. In addition to the hardware trigger sources, there is also a software trigger that allows triggering under program control.

A digitiser will also include powerful trigger AND/OR logic elements, used to combine inputs from multiple sources into a complex, multi-element trigger. The functionality can be used to ensure that the digitiser will only trigger when specific patterns occur.

Trigger Modes

The principal trigger sources contain dual trigger level comparators and support multiple trigger modes. These include single and dual slope edge triggers, re-arm (hysteresis) triggers, window triggers and, for the multiple source trigger, there are related trigger gate generators.

- Edge triggers are the most basic trigger type. The user sets a trigger level and selects the desired trigger slope. When the trigger source crosses the trigger threshold with the

selected slope, the digitiser triggers. The slope selection is positive, negative, or both. Edge trigger is the most commonly-used trigger mode.

- Re-arm or hysteresis triggers set two levels, first the arm level and then the trigger level. As with the edge trigger, the user selects a slope. The signal must cross the arm level with the selected slope first, to arm the trigger. In addition, the re-arm trigger modes can be used to prevent the digitiser from triggering on the wrong edges of noisy signals.
- Window triggers use two trigger thresholds per trigger source to define an amplitude window. There are two operational modes for the window trigger; trigger upon entering the window and trigger upon exiting it. Window triggers are used when the source signal can change states in either direction.

When using a multi-source trigger mode with the built-in trigger logic, it is often necessary to use one channel to create a gate waveform to enable a trigger from another channel, by using the high-level, low-level, inside-window or outside-window selections. These trigger modes generate an internal gate signal that can be used together with a second trigger source and AND logic to gate the trigger. Figure 3 shows the use of the high-level trigger to gate a trigger source on another channel.

Whenever the sine wave on channel CH0 exceeds the trigger level, a positive gate is generated for the entire time the signal is above the threshold. This gate signal is ANDed with the signal on channel CH1; since the gate signal is positive only while the low amplitude pulse is present on CH1, the digitiser triggers when the pulse waveform crosses the trigger level shown as a horizontal, red, dashed line in the figure.

For a summary of different trigger modes, see the next two pages.

Trigger Logic Examples

Figure 3 shows the use of trigger logic when dealing with multiple trigger sources. Both AND and OR logic elements are supported. Inputs to the OR function include any of the channels, the external trigger inputs, the software trigger and the force trigger function. The logical OR function permits any of these trigger sources to trigger the digitiser.

Inputs to the AND logic function include all the channels, external trigger inputs and the enable trigger function. The AND function requires that all selected trigger inputs be asserted at the same time to initiate a digitiser trigger. Keeping in mind that gating trigger modes like high-level and low-level can logically invert inputs; other logic, such as NAND and NOR, can be realised.

Figure 4 is an example of a radio-location application

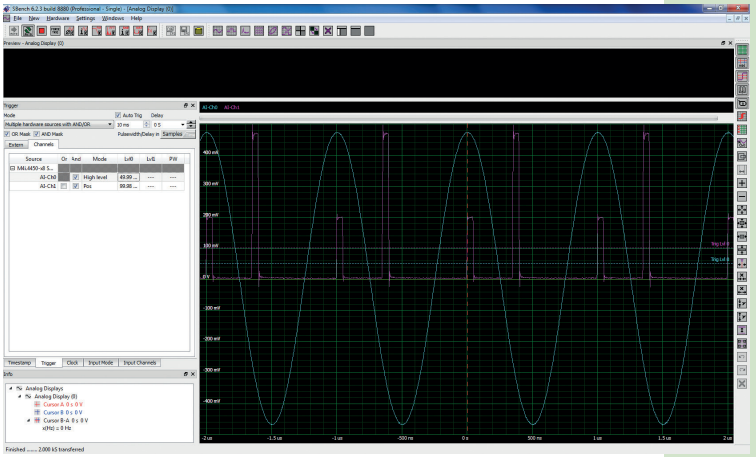


Figure 3: Use of the high-level trigger on CH0 to create a gate signal to select the lower of the two pulses on channel CH1

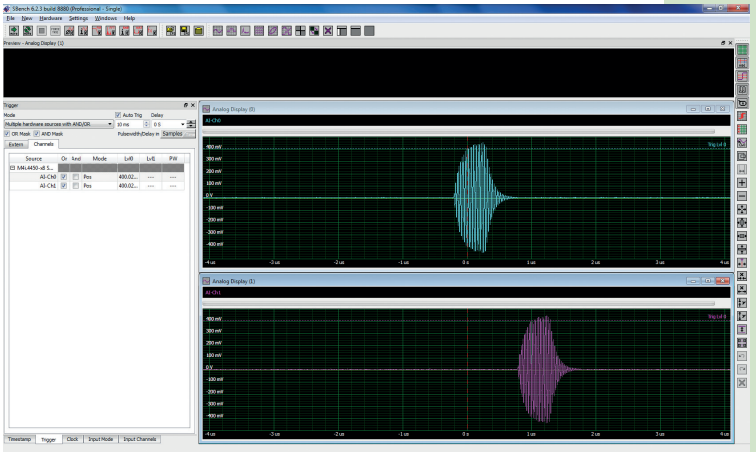
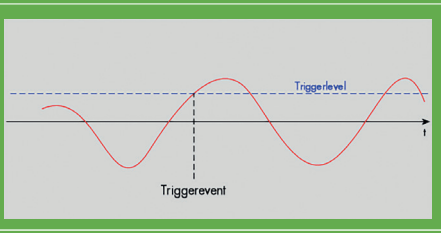
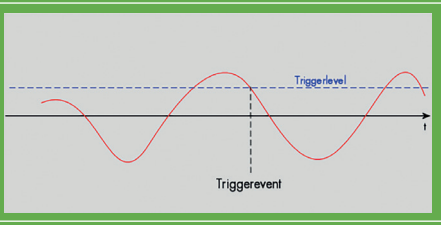
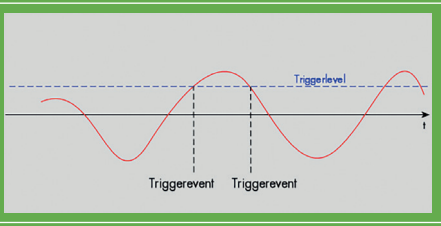
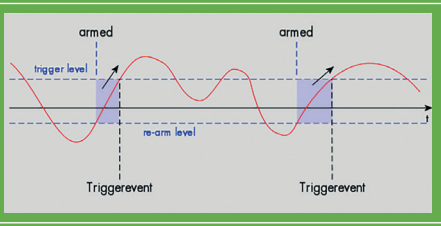
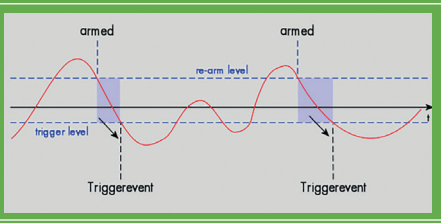
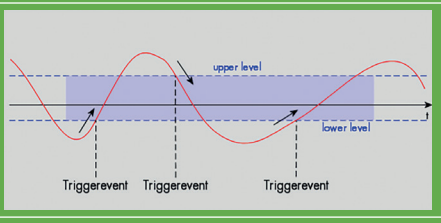
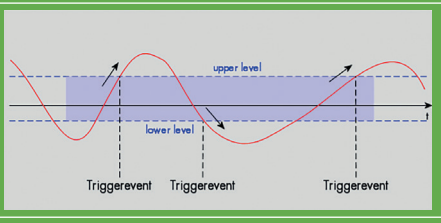
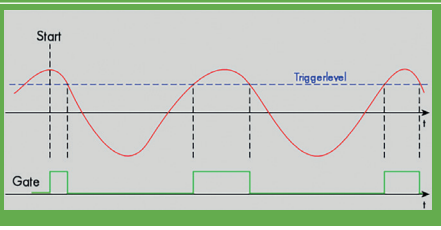


Figure 4: Use of OR trigger logic to trigger on the channel where the earliest RF burst occurs

Figure 5: Another example of using the AND trigger function with an inverted logic element (low-level mode on Ch0), which triggers when a missing pulse occurs in Ch0 compared with the pulse train on Ch1

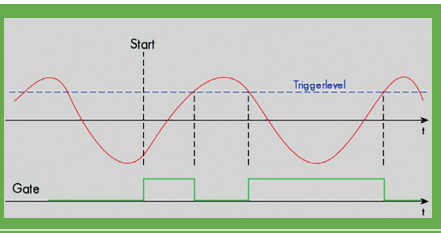
that uses OR trigger logic. Each of the input channels is connected to a sensor. Direction to the source is determined by the arrival time of the emitted pulse at each sensor.

The location of the source determines which channel sees it

MODE DESCRIPTION	DIAGRAM
Positive edge trigger The trigger occurs if the trigger source signal goes from a lower to a higher value (positive slope or rising edge) crossing the predefined trigger level.	
Negative edge trigger The trigger occurs if the trigger source signal goes from a higher to a lower value (negative slope or falling edge) crossing the predefined trigger level.	
Dual edge trigger The trigger occurs if the programmed trigger level is crossed by the trigger source signal with either a rising or falling edge.	
Re-arm (hysteresis) trigger on positive edge The trigger circuit is armed when the source signal crosses the re-arm level with a positive slope. After arming, if the programmed trigger level is then crossed by the source signal with a rising edge, the trigger is generated and the trigger circuit disarmed. A new trigger event is only detected if the trigger engine is armed again.	
Re-arm trigger (hysteresis) on negative edge The trigger circuit is armed when the source signal crosses the re-arm level with a negative slope. After arming, if the programmed trigger level is then crossed by the source signal with a falling edge, the trigger is generated, and the trigger circuit will be disarmed. A new trigger event is only detected if the trigger engine is armed again.	
Channel window trigger for entering signals The upper and lower level define an amplitude window. Every time the source signal enters the window from the outside, a trigger is generated.	
Channel window trigger for exiting signals The upper and lower level define an amplitude window. Every time the signal leaves the window from the inside, a trigger is generated.	
High-level trigger This mode generates an internal gate signal that can be used with a second trigger mode to gate the trigger. If using this mode with a single trigger source, the card only triggers when the source signal exceeds the trigger level (acting like a positive edge trigger).	

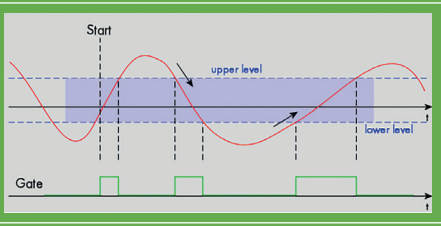
Low-level trigger

This mode generates an internal gate signal that can be used with a second trigger mode to gate the trigger. If using this mode with a single trigger source, then the card only triggers when the source signal is below the trigger level (acting like a negative-edge trigger).



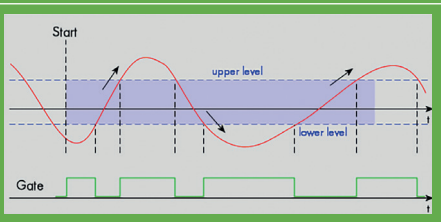
Inside window trigger

This trigger mode will generate an internal gate signal that can be used with a second trigger mode to gate the trigger. Using this mode as a single trigger source, the card will only trigger when entering the window defined by the two trigger levels (acting like a window-enter trigger).



Outside window trigger

This trigger mode generates an internal gate signal that can be used with a second trigger mode to gate the trigger. If using this mode as a single trigger source, the card will only trigger when leaving the window defined by the two trigger levels (acting like a window-exit trigger).



first. The OR trigger logic allows the channel with the earliest burst to trigger the digitiser, guaranteeing that both sensor outputs will be captured.

Another example of a multi-source trigger is shown in Figure 5. Here, two clock signals are compared. The low-level trigger is set up on channel Ch0, which generates a gate positive signal when that channel's amplitude is below the trigger level. Channel Ch1 triggers on the positive edge. Both trigger sources are ANDed, which results in a trigger event when there is a missing pulse in Ch0. The missing pulse in Figure 5 appears at the trigger point (time = 0).

Synchronisation

When multiple digitisers or acquisition instruments are integrated into a multi-channel system, meaningful data can only be obtained when all channels are referenced to a common time axis, which requires time synchronisation.

Theoretically, there are two issues when synchronising instruments. The first is to arrange for a common trigger, and the second to have both instruments operate from a synchronised clock. As simple as this seems, there are issues that arise when attempting to synchronise multiple digitisers.

The clock can be synchronised by using an external clock at the desired clock rate. A second method is to supply an external reference such as 10MHz, which is then applied to a phase locked loop (PLL) used to multiply the frequency of the reference clock to the desired clock rate. There are digitisers that handle both types of external clock through a common external clock input.

On the trigger side of the synchronisation process it should be considered that each digitiser's external trigger input uses a separate comparator to detect the trigger level crossing. Small differences in reference level and setup-and-hold times can result is discrete changes in the trigger point location in time, a form of trigger jitter.

The only way to guarantee exact synchronisation of multiple digitisers is to distribute the clock to each module and then synchronise the trigger event to the system clock.

Capturing Signals

Digitisers with smart trigger engines make it possible to trigger on and capture a wide variety of complex signals. This feature is further enhanced when combined with innovative acquisition modes such as ring buffer, FIFO, memory segmentation and gated sampling with time stamps marking trigger events. ●

Worker safety should drive cleaning choices

BY **MIKE JONES**, VICE PRESIDENT, MICROCARE

There are several dimensions to worker safety around chemicals: toxicity, corrosivity and flammability, to name a few. While the risk of fire and corrosiveness may be well understood, David Ferguson, MicroCare product manager, feels that most end users may not clearly understand toxicity, and mistakes can put workers at risk. One type of toxicity rating is 'threshold limit value', expressed in parts per million (ppm), included in any modern safety datasheet; managers should choose products with higher ratings.

Keep Your Score High

The purpose of a toxicity rating is to protect workers from excessive levels of exposure that could be dangerous, either in the short or long term. Toxicity ratings can be identified in several ways. Usually called TLV (threshold limit value), they may also be listed as PEL (personal exposure limit), generated by the manufacturer and AEL (assigned exposure limit) that are assigned by a government body. These values are usually – but not exactly – equivalent, with the rating systems working in the same general manner.

A ppm value helps to gauge if a chemistry can safely be used in a workplace. These values may also be specified in milligrams per cubic metre (mg/m^3) or milligrams per litre (mg/l). High numbers – those approaching 1,000ppm (the highest rating possible) – indicate a safe chemistry; lower numbers indicate greater risk. A higher score is better, as it indicates that a larger concentration of exposure could occur without causing adverse effects.

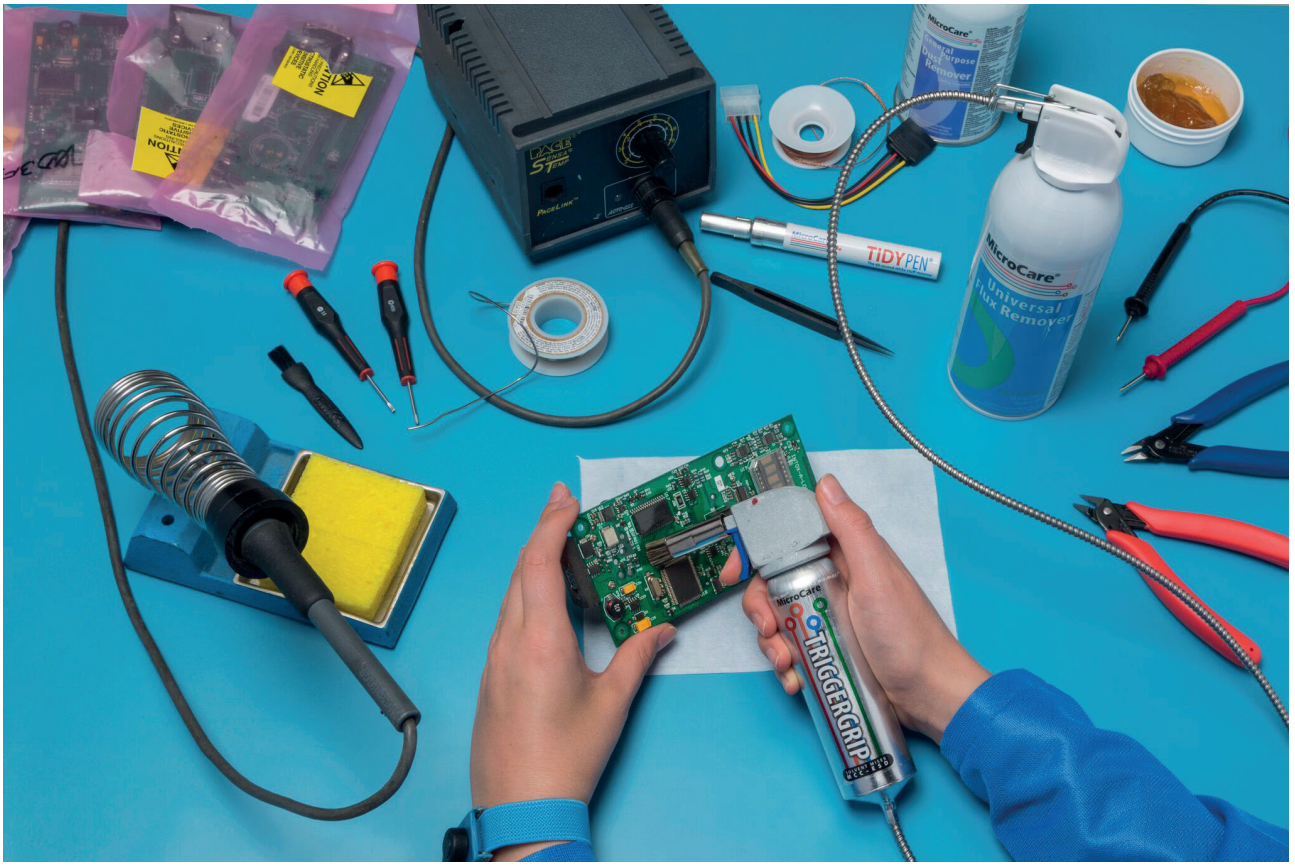
The scores estimate worker risk from exposure to the liquid for eight hours per day, five days a week, for a hypothetical thirty-year working career. A lower score means even brief exposure to the chemical may pose hazards. Therefore, a chemical that would warrant greater review might have a TLV of 10-25ppm.

Fluids, cleaners or coatings with a TLV value of 50-100ppm can be used safely with proper equipment and training. Fluids with AELs of 100-200ppm or higher are better still. They may require personal protective equipment, but their potential for harm is manageable.

A brief note here: these values are not the only statistic to measure the chemistry's safety; vapour-pressure of the fluid is also worth a note. A high vapour pressure fluid will evaporate easily, possibly putting a higher concentration of vapours near the inhalation zone of the workforce.

There are cleaning chemistries that are paving the way with progressive and careful chemicals

Minimise solvent vapour with a dispensing system



"Most exposure limits are 'time-weighted' and are designed to prevent long-term damage from exposures lasting days, weeks or even years," said Ferguson. "However, this does not take into consideration how the chemical is dispensed. For example, a chemical with a lower exposure may be acceptable when used in properly-designed cleaning equipment. But, this same chemical in a highly-emissive application, such as an aerosol spray, could present a higher risk for workers."

When looking at your cleaning processes, find chemistries that address TLV concerns

Aerosol sprays that volatilise a solvent can expose workers to fumes. Excess fluid can also pool below the cleaning site, creating a hazard if the solvent is flammable. This risk must be reduced for worker safety; one method is to use less solvent.

One way to achieve this ideal is by using a dispensing system with aerosol cleaners, which minimises solvent vapours and, as an extra advantage, uses less solvent, resulting in savings.

Reduce Risk – Study the Facts

It is essential to obtain as much information as possible concerning the identity of the chemicals a product contains. To reduce risk, it is important to read and understand the safety data sheet (SDS), which gives specific details on the product's potential hazards, helping users understand the threats and make informed decisions about their use.

Every product will have an SDS, organised into several sub-sections; for example, identification of the substance and manufacturer, toxicological information, exposure controls and personal protection.

It is important to remember that concentrating on just the TLV figure is insufficient for a comprehensive assessment. It's crucial to look at the whole picture to determine safety, and key aspects including flammability, storage, handling and disposal – details that need to be included in any safety analysis.

Choose Wisely

When looking at your cleaning processes, find chemistries that address TLV concerns. There is no standardised certification about hazards and safety, but do the research. Some manufacturers of cleaning solutions are paving the way with progressive and careful chemistries that consider safety and hazard risks, whilst still cleaning effectively. Before selecting a solvent, contact a safety expert if you are unfamiliar with these issues and worried about the implications. The chemistry is out there. Be proactive and examine your cleaning products' SDS to choose wisely. ●

COMMUNICATIONS EQUIPMENT MAKERS DEMAND HIGH-POWER OUTPUTS & SMALL SOLUTION FOOTPRINTS

By Tony Armstrong, Marketing Director, Power Products, Analog Devices

Many communications systems are powered via a 48V backplane. This voltage is normally stepped down to a lower intermediate bus voltage, typically to either 12V, 5V or even lower, in order to power the racks of boards within the system. However, most of the sub-circuits or ICs on these boards are required to operate at voltages ranging from 3.*x*V down to 0.5V at currents ranging from tens of milliamps to hundreds of amps. As a result, point-of-load (PoL) DC/DC converters are necessary to step down from these higher bus voltages to the lower voltage necessitated by the sub-circuits or ICs. These rails also have strict requirements for sequencing, voltage accuracy, margining and supervision that need to be considered, too. Since there can be hundreds of POL voltage rails in communications equipment, system architects need a straightforward way to manage these rails.

Many of today's deep submicron digital processors demand that their I/O voltage rises before their core voltage, and many DSPs require their core voltage to be brought up before their I/O. Moreover, power-down sequencing is also necessary. Therefore, an effortless way is needed to make changes to optimise system performance and to store a specific configuration for each DC/DC converter for a simplified design effort.

Nowadays, most communications equipment manufacturers are being pushed to increase the data throughput rate and performance of their systems, in addition to more features. At the same time, there's pressure to decrease the system's overall power consumption. For example, a typical challenge is to reduce overall power consumption by rescheduling the work flow and moving jobs to underutilised servers, thereby enabling shutdown of other servers. To meet this, it is essential to know the power consumption of the end-user equipment. Thus, a properly-designed digital power management system (DPSM) can provide the user with power consumption data, which in turn allows for smart energy-management decisions to be made.

A principal benefit of DPSM is reduced design cost and faster time to market. Complex multi-rail systems can be efficiently developed using a comprehensive development environment with intuitive graphical user interface (GUI). Such systems also simplify in-circuit testing (ICT) and board debug by enabling changes via the GUI instead of soldering in "white wire" fixes. Another benefit is the potential to predict power system failures and enable preventive measures, thanks to the availability of real-time telemetry data.

Perhaps most significantly, DC/DC converters with digital management functionality allow designers to develop "green" power systems that meet target performance (compute speed, data rate, etc.) with minimum energy usage at the point of load, board, rack and even installation level, reducing infrastructure costs and the total cost of ownership over the life of the product. After all, the largest operating cost of a data centre is the cost of electricity used to power the cooling systems to keep the inside of the data centre below its predefined optimal operating temperature.

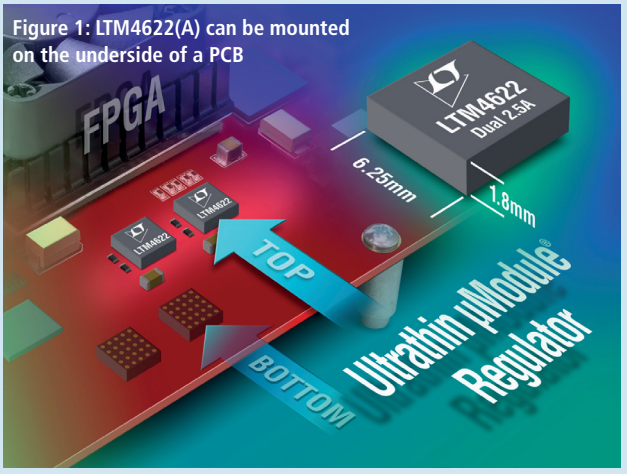


Figure 1: LTM4622(A) can be mounted on the underside of a PCB

In addition, system architects still need relatively simple power converters to satisfy various power rails on their boards but on an ever-shrinking board area. Converters cannot be fitted on the underside of circuit boards due to a 2mm maximum component height restriction forced on them due to multiple boards placed side-by-side in a rack-mounted configuration. What's really needed is a complete power supply in a small form factor that does not exceed 2mm when mounted onto a printed circuit board (PCB). Fortunately, such solutions exist and will be discussed in more detail herein.

Converter Solutions

Analog Devices's Power by Linear µModule regulators are complete system in a package (SiP) solutions that minimise design time and solve the common problems of board space and power density issues routinely found in communications systems. These µModule products are complete power management solutions with integrated DC/DC controller, power transistors, input and output capacitors, compensation components and inductor within a compact, surface-mount BGA or LGA packages. Designing with Power by Linear's µModule products can significantly reduce the time needed to complete the design process by as much as 50%, depending on the complexity of the design. This family of µModule regulators transfers the design burden of component selection, optimisation and layout from the designer to the device, thereby shortening the overall design time, system troubleshooting and ultimately improving time-to-market.

The µModule solutions integrate key components commonly used in discrete power, signal chain and isolated designs within a compact, IC-like form factor. Supported by Power by Linear's rigorous testing and high-reliability processes, the µModule portfolio simplifies the design and layout of power management and conversion designs. The product family embraces a wide range of applications including PoL regulators, battery chargers, DPSM products (PMBus digitally-managed power supplies), isolated converters and LED drivers. As highly integrated

solutions with PCB Gerber files available for every device, the µModule power regulators address time and space constraints while delivering high efficiency and reliability. Furthermore, many of Analog's newer products enable low EMI solutions that are compliant to EN55022 class B standards. This gives the system designer confidence that the end system will meet the strict noise performance criteria required by the many noise-immunity industry standards.

Moreover, as design resources become stretched by increased system complexity and shortened design cycles, the focus falls on development of the key intellectual property of the system. This often means the power supply gets put to one side until late in the development cycle. With little time, and perhaps limited specialist power design resource, there is tremendous pressure to come up with a high-efficiency solution with the smallest possible footprint, while utilising the underside of the PCB.

This is a key area where a µModule regulator can provide an ideal solution. Careful design, PCB layout and component selection are very important in the design of a switching regulator, and many experienced designers have smelt the distinctive aroma of a burning circuit board in the early days of their career. The ready-made µModule regulator reduces risks to the program.

A recent example of an ultrathin µModule solution is the LTM4622. This is a dual 2.5A, or single two-phase 5A output step-down power regulator in a 6.25mm x 6.25mm x 1.8mm ultrathin LGA package. At nearly the height of a soldered down 1206 case size capacitor, it can be mounted on the board's topside. The thin profile allows it to meet demanding height restrictions such as those required by PCIe and advanced mezzanine cards in embedded computing systems; see Figure 1.

Furthermore, the LTM4622A was recently released. A variant of the LTM4622, this "A" version has a higher output voltage of 1.5-12V, in lieu of the non-A version at 0.6-5.5V. This enables the system designer to have a broader output voltage range on the higher end, if needed. In either case, the input voltage range is 3.6-20V.

Power by Linear's µModule DC/DC regulators also provide a straightforward way to deliver both high power and DPSM capability. Since many of the µModule regulators can be paralleled for high load current with precision current matching (within a nominal 1% of each other), they can mitigate the potential for hot spots. Moreover, only one of the µModule regulators needs to contain DPSM capability, since it can supply the complete digital interface.

With DPSM devices a system designer can also:

- Configure voltages, define complex on/off sequencing arrangements and fault conditions such as OV and UV limits and set important power supply parameters such as switching frequency, current limit, etc. over a digital communication bus.
- Over the same communication bus, important operating parameters such as input and output voltage, current and power, internal and external temperature can be read, and consumed energy measured.
- Implement very precise closed-loop margin testing of the designs and trim power supply voltages to very precise levels.
- These devices have been designed to be autonomous. Once they are configured and input power applied, they sequence up the power supplies, regulate very accurate voltages at the point of load, continuously supervise voltage and current while implementing the user-configurable fault management scheme and arm a non-volatile fault recorder that stores information about the power system at the time of a detected fault.
- DPSM devices can be cascaded to build large power supply systems that are coherent, achieved with an inter-chip coordination bus that operates at wireline speeds.
- Internal NVM for device configuration and fault-logging capability are included.
- These devices contain I²C/PMBus communication ports and use an industry-standard PMBus command set to control and manage the power system.
- These PSM devices are all supported by a common, engineering-level LTpowerPlay GUI, developed specifically for power system design and debug as well as remote customer support.

Figure 2 shows an application schematic of one LTM4677 (36A DPSM µModule regulator) in parallel with three LTM4650s (50A µModule regulators) for an 180A plus DPSM PoL solution. ●

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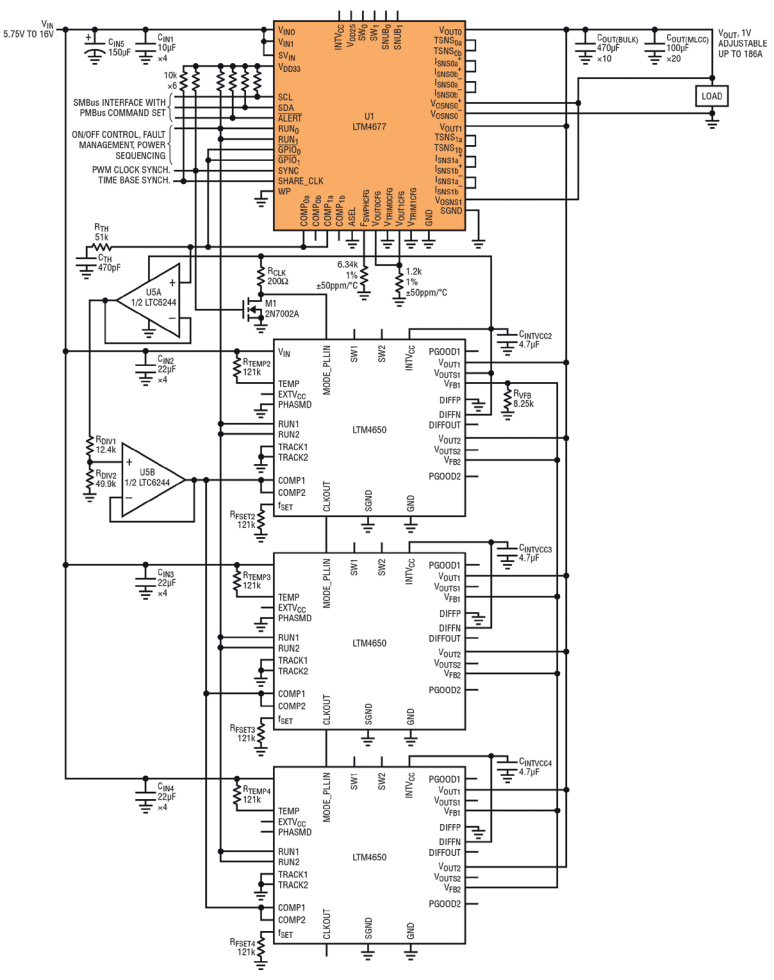


Figure 2: A combination of 1 LTM4677 DPSM µModule and three LTM4650 µModule regulators delivers 186A at 1V from a nominal 12V input

DR. MURAT UZAM, ACADEMIC AND TECHNICAL AUTHOR, TURKEY

Analogue input/output modules

Programmable logic controllers (PLCs) are widely-applied computer-based digital systems, from simple traffic and environmental control to complex electrical power grids and industrial processes.

PLCs typically consist of a power supply, a central processing unit (CPU) and various digital and analogue inputs and outputs. Commonly-used analogue input and output current and voltage ranges include 4-20mA (industrial process-control systems), 0-5V, 0-10V, -5V to +5V, and -10V to +10V (actuator controllers).

Analogue input signals require analogue-to-digital converters (ADCs) and, likewise, analogue output signals require digital-to-analogue converters (DACs) for processing by the PLC's CPU. In this case, PLC system hardware-design tasks focus on input-signal and output-signal conditioning.

In high-precision solutions, for each analogue input signal there must be an input-signal conditioning module containing an ADC (12- or 16-bit) with the necessary amplifiers, isolators and so on. Likewise, in high-precision solutions, for each analogue output signal there must be an output-signal conditioning module containing a DAC (12- or 16-bit) with the necessary amplifiers, buffers, isolators, etc., needed for very-high-accuracy industrial applications.

As expected, this type of analogue-input and -output signal-conditioning modules are extremely expensive.

Low Cost and Easy to Use

Our project focuses on a set of low-cost and easy-to-use analogue-input and -output signal-conditioning modules for PLCs; see Figure 1. The CPU is assumed to be a 5V microcontroller with analogue inputs and outputs.

If the ADC is integrated with the CPU (as is the case in this project and desirable in embedded applications), it is very common for the on-chip ADC to be unipolar (0-5V). This means that the ADC can only sample positive voltage levels, as opposed to a bipolar ADC that samples signals with both positive and negative values, over time. Therefore, a special type of inverting op-amp (operational amplifier) called a level shifter is required here. For example, this is the case when designing -5V/+5V to 0-5V and -10V/+10V to 0-5V analogue-input signal converters. Similarly, a level shifter is also necessary when designing a 0-5V to -5V/+5V and 0-5V to -10V/+10V analogue-output signal converters.

Another signal-conditioning circuit that's required is a buffer amplifier, or op-amp, used to transfer signal from high-output-impedance to low-input-impedance.

There are thirteen analogue input modules developed in this project (Table 1), and a further seven analogue output modules (Table 2). It can be seen that there are five variants of the 0-5V analogue input module because each one withstands a different maximum voltage and has a different power supply requirement. The remaining analogue input modules come in two versions, each requiring a different set of power supplies, analogue outputs and signal converters.

Analogue Input and Output Modules

Analogue-input and -output modules developed in this project are specifically designed around the low-cost LM358P op-amps manufactured by Texas Instruments (TI). Hence, any variant of the LM358P, such as LM358, LM358A, LM358N, etc., or LM358P op-amps manufactured by other companies, may not necessarily function in all the modules discussed here. The LM358P op-amps are used in this project in the design of level shifters from bipolar to unipolar and unipolar

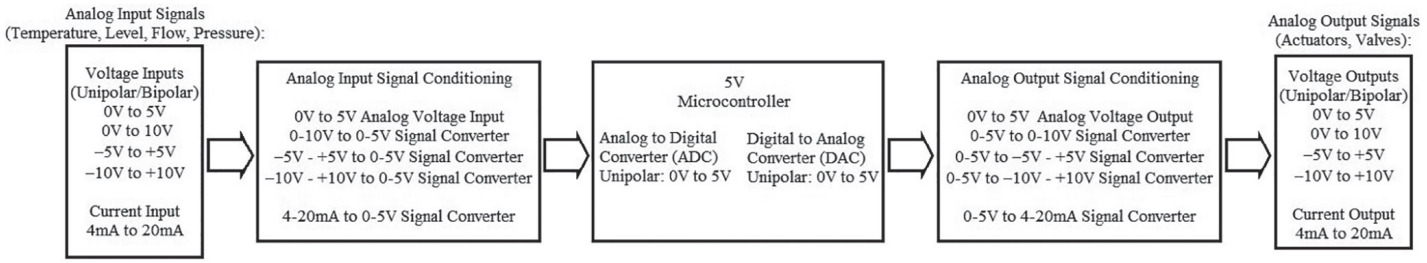


Figure 1: Block diagram of developed analogue-input and -output modules and their connections to a 5V microcontroller through ADC and DAC channels

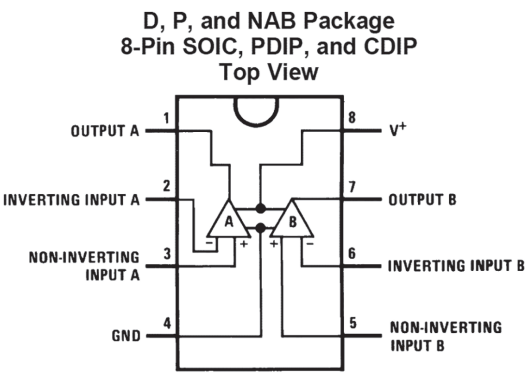
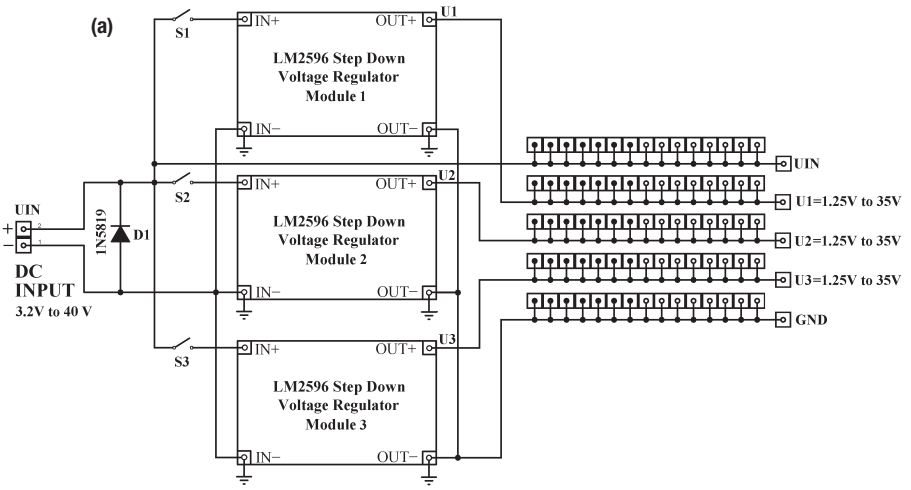


Figure 2: Top view of the LM358P PDIP package



(b)

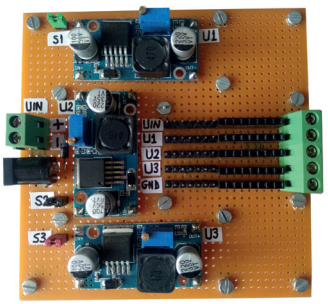


Figure 3: (a) Schematic diagram of the voltage regulator module consisting of three adjustable LM2596 step-down voltage regulators; (b) the voltage regulator module

to bipolar signal level shifters, buffer amplifiers (voltage followers) and non-inverting summing amplifiers.

A top view of the LM358P PDIP package is shown in Figure 2. Figure 3a shows the schematic diagram of the voltage regulator module consisting of three adjustable LM2596 step-down voltage regulators, while Figure 3b is a photo of the module, with which three independent voltage values can be adjusted. D1 ensures the correct polarity of the DC input voltage. Switches S1, S2 and S3 (implemented with jumpers) are used to turn on and off the adjustable LM2596 voltage regulators 1, 2 and 3, respectively. ●

	Analogue Signal Input Modules	Acceptable input voltage / current		Required Power Supplies
		Minimum	Maximum	
1	0V to 5V Analogue Input Module 1	0V	+6.26V	+6.26V
2	0V to 5V Analogue Input Module 2	0V	+12V	+6.26V, +12V
3	0V to 5V Analogue Input Module 3	0V	+24V	+6.26V, +24V
4	0V to 5V Analogue Input Module 4	0V	+12V	+12V
5	0V to 5V Analogue Input Module 5	0V	+24V	+24V
6	0-10V to 0-5V Signal Converter - Analogue Input Module 1	0V	+24V	+6.26V, +12V
7	0-10V to 0-5V Signal Converter - Analogue Input Module 2	0V	+24V	+12V
8	–5V - +5V to 0-5V Signal Converter - Analogue Input Module 1	–12V	+12V	+5.00V, +6.26V, –12V, +12V
9	–5V - +5V to 0-5V Signal Converter - Analogue Input Module 2	–12V	+12V	–12V, +12V
10	–10V - +10V to 0-5V Signal Converter - Analogue Input Module 1	–12V	+12V	+5.00V, +6.26V, –12V, +12V
11	–10V - +10V to 0-5V Signal Converter - Analogue Input Module 2	–12V	+12V	–12V, +12V
12	0-5V or 4-20mA to 0-5V Signal Converter - Analogue Input Module 1	0V / 0mA	+12V / 48mA	+6.26V, +12V
13	0-5V or 4-20mA to 0-5V Signal Converter - Analogue Input Module 2	0V / 0mA	+12V / 48mA	+12V

Table 1: Thirteen analogue input modules developed in this project

	Analogue Signal Output Modules	Required Power Supplies
1	0V to 5V Analogue Output Module	+12V
2	0-5V to 0-10V Signal Converter – Analogue Output Module	+12V
3	0-5V to –5V - +5V Signal Converter - Analogue Output Module 1	+5.00V, –12V, +12V
4	0-5V to –5V - +5V Signal Converter - Analogue Output Module 2	–12V, +12V
5	0-5V to –10V - +10V Signal Converter - Analogue Output Module 1	+5.00V, –12V, +12V
6	0-5V to –10V - +10V Signal Converter - Analogue Output Module 2	–12V, +12V
7	0-5V to 4-20mA Signal Converter - Analogue Output Module	+12V

Table 2: Seven analogue output modules developed in this project

This series continues in the next issue.

LoRa in private and public networks

By Martin Keenan, Technical Director, Avnet Abacus

Wireless communications and the IoT seem inextricably linked. While it is likely that gateways will use a combination of wireless and wired connections for the backhaul to cloud services, it is probably reasonable to estimate that every gateway hardwired to the Internet could easily have ten endpoints wirelessly connected to it. Most endpoints connect wirelessly if it offers a lower installation cost, in locations where no existing wired connection is available, which will be the majority.

The number of wireless technologies available to provide that link increased over the last decade and, more recently, the concept of the low-power wide area network, or LPWAN, have gained attention. While the network topology is similar, the distance between endpoint and gateway in a LPWAN can be several kilometres, as opposed to mere metres with personal area networks (PANs) such as ZigBee, Bluetooth and even Wi-Fi. This range comes with some compromises in terms of bit rates, but the proponents of LPWAN technologies are quite open and accepting of this limitation. LPWANs will service applications that need to communicate small amounts of data over long distances on a relatively infrequent basis, such as sensors. It is reasonable to say that LPWANs will not make the shortlist for some typical IoT applications, such as home or office automation or industrial control. But given that data in its raw form is now seen as the currency of the IoT, remote sensors in particular will benefit from LPWANs.

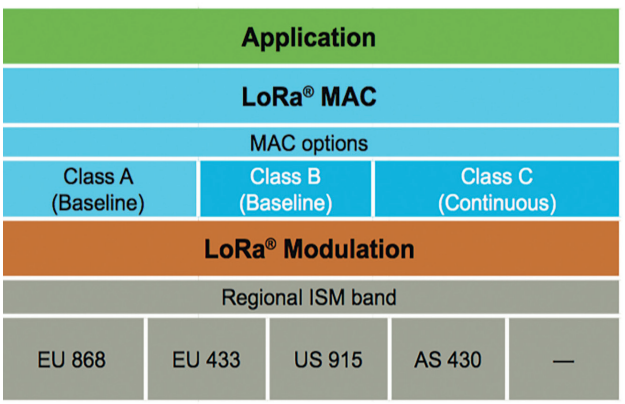


Figure 1: LoRa provides a PHY and MAC, and the potential to build private or public networks

Low Power is the Key

Low power is crucial to the success of LPWANs, and that translates into many years of service from a single primary cell or even the use of harvested energy. Compared to PANs, there is arguably less competition among LPWANs both in terms of their competing technologies and providers.

A large part of the LPWAN market is already addressed by members of the LoRa Alliance, based on technology owned by Semtech and fundamental to services built to deliver networks running the LoRaWAN protocol. This highlights an important point, one that is very different from other wireless technologies developed for use in the IoT for license-free ISM bands – network management.

In general, PANs operate over shorter distances and provide higher bandwidths than LPWANs; but, more importantly, they are typically described as ad hoc networks, meaning there isn't really a formal network topology. LPWANs differ in this respect and, while this can be unimportant to users who simply need to get data from a remote sensor, it does mean that LPWANs cannot really be compared directly to incumbents such as Bluetooth and ZigBee, or even newcomers like Thread.

LPWANs fall rather cleanly into two categories: public and private networks. The operative word here is "network", as opposed to "connections", because LPWANs are effectively predicated on establishing an 'end to end' data flow, from the sensor to the cloud, and to do that requires homogeneity throughout the system. The way the LoRa Alliance has achieved this is through the LoRaWAN protocol, which is used to build public networks. However, it is still possible to use the LoRa physical layer to create private networks, which is the source of some confusion.

Two Technologies, One Objective

The IEEE 802.15.4 standard defines a physical layer (PHY) and the media access control (MAC) for low-power PANs, and underpins several protocols such as ZigBee, Thread and 6LoWPAN. Similarly, the LoRa PHY is used for networks running the LoRaWAN MAC; see Figure 1. However, 802.15.4 PHY is also used for a wide range of other wireless technologies, including proprietary solutions like the MiWi protocol, designed by Microchip Technology. Almost any PHY can be used to enable a proprietary wireless solution, so it follows that the LoRa PHY can also be used to create private networks based on proprietary MACs.

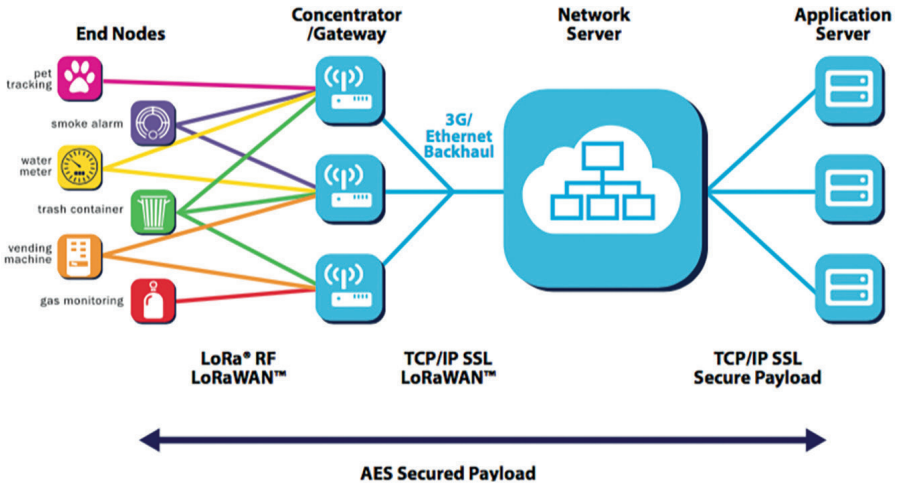


Figure 2: The LoRaWAN protocol uses a 'star of stars' network topology for end-to-end communication

The two technologies are separate and not entirely co-dependent; the LoRaWAN MAC depends on a LoRa PHY but the PHY can be and is used by others to create competitive solutions. Although at the chip level it is not uncommon for a solution based on a LoRa PHY to also support LoRaWAN, it does not follow that a private network based on a LoRa PHY will support LoRaWAN devices. In fact, it is quite likely that only those features of LoRaWAN that are deemed useful for the private network will be present.

Physical Differences

It's clear that not all LPWANs are the same; for example, the LoRa PHY employs spread-spectrum technology over a wide bandwidth, while others use ultra-narrowband modulation as Sigfox does, which also applies a binary phase shift keying scheme that's arguably simpler at the transmitting end than the chirp spread-spectrum scheme used by LoRa.

The modulation scheme at the heart of the LoRa PHY is a proprietary technology owned by Semtech and implemented as a hardware-defined radio. This means that all LoRa-based communication uses hardware supplied by Semtech at the RF layer but may use any MAC layer.

The availability of hardware-defined radios implementing the LoRa PHY from Semtech allows companies including Link-Labs, Advantech and Digital Six Labs to develop solutions that use the LoRa PHY with their own MAC technology on top. It even allows manufacturers to create their own private networks using an alternative MAC layer, perhaps even one developed in house.

The LoRa Alliance includes a growing number of interested parties, with a rapidly increasing membership since its launch in 2015 – a good indication of the potential of LPWANs for IoT applications. Any product certified by the alliance must use the LoRaWAN MAC layer, as well as the LoRa PHY, which means private networks created using just the PHY can remain just that – private.

Part of the strength of LoRa-based networks is the chirp itself, which contains little information, but a distinctive signature, which means that any receiver in the transmitter's range will lock onto the signal and attempt to demodulate it. This gives rise to the distinctive 'star of star' topology of a LoRa-based network; see Figure 2. All gateways within range of an endpoint will lock onto its chirp, demodulate it and relay the message farther up the network.

The spread-spectrum nature of the chirps means that even receivers with low-cost crystals can achieve high sensitivity, supporting longer ranges for signals with lower RF energy. It also supports the demodulation of multiple chirps on the same frequencies, as long as the chirp rates vary, which means large wide-area networks can be created with many endpoints and relatively few gateways.

Many of these features are managed at the MAC layer and above, which is where the LoRaWAN protocol sits in a public network, permitting protocols such as Link-Labs's Symphony Link, Advantech's WISE-Link and Digital 6 Labs's Whisker.io operate in private networks.

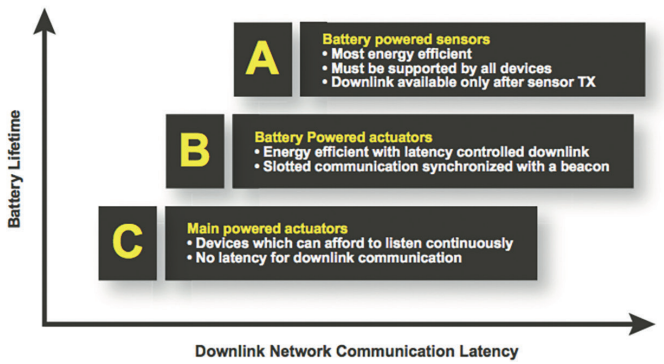


Figure 3: The LoRaWAN protocol supports three classes of device, suitable for ultra-low-power, low-power and AC-powered endpoints

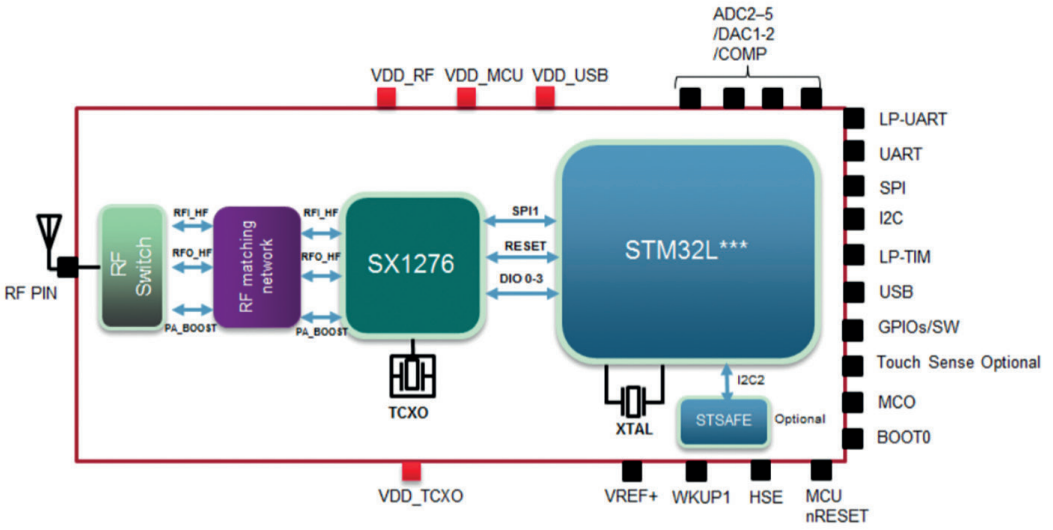


Figure 4: The CMWX1ZZABZ module from Murata supports LoRa PHY and MAC, and Sigfox network

The LoRaWAN Protocol

While it may not appear so at first, there's a lot of choice when it comes to selecting the right protocol for a LoRa-based LPWAN. The preference of the LoRa Alliance, LoRaWAN, was developed to offer all the right features to support public networks, while proprietary protocols invariably cite features that are specifically important to users looking to implement a private network. A growing number of LoRaWAN network providers offer access to both public and private networks.

The LoRa Alliance claims that LoRa and LoRaWAN deliver a link budget greater than any other standardised communication technology and, therefore, provide greater range than other technologies do.

It is at the protocol layer that the network architecture is defined. While many protocols now implement mesh networking as a way to extend range, LoRaWAN uses a star network, where multiple gateways receive all messages and feed them back to the network server. This is where the real work is done, such as identifying and discarding redundant messages, varying the data rate between gateways and endpoints, and applying security.

This topology means that handover is not required between gateways; if an endpoint is located on a moving asset, such as a vehicle, all the gateways within range will receive its chirps without 'confusing' the endpoint or the gateways. This, according to the LoRa Alliance, is a major feature of the protocol, because mobile asset tracking is expected to be a key application for LoRaWAN-based networks.

This highlights a critical part of the entire proposition: the number of concurrent connections the network can reliably maintain. The protocol handles this by implementing adaptive data rates, while the PHY supports multiple channels: together they can handle multiple data rates on the same channel at the same time. The LoRaWAN protocol delivers data rates from 290bit/s to 50kbit/s, which is more than other ISM-based LPWANs, and comparable to some cellular solutions targeting the IoT, such as narrowband LTE (NB-LTE).

Adapting data rates is a technique used by other networks to increase capacity. It works because endpoints with a strong signal can deliver their payload faster than those with a weak one, meaning they transmit for a shorter time and thus consume less of the overall available bandwidth. It is a technique that relies on a good downlink, the reason not all LPWANs are able to implement it. The alliance states that these features also make the network easily scaleable.

Most endpoints will be connecting wirelessly if it offers a lower cost of instalment, which will be the case in locations where no existing wired connection is available

The frequency bands, data rates, number of channels and channel bandwidths vary by geographical region, as does transmit power, but the up- and downlink budgets remain largely consistent at between 154dB and 157dB.

Another feature of the LoRaWAN protocol that supports scaleability is the classification of endpoints based on their features and requirements. As shown in Figure 3, there are three device classes: A, B and C. LoRaWAN is possibly the only IoT protocol to offer this level of flexibility in the IoT.

The main difference between the three classes is their respective receive windows – the time when they are listening for messages from the gateway. During the receive window, the endpoint must be active and unable to go into a power-saving sleep mode; but, for endpoints powered from an AC outlet (defined as Class C devices) this isn't a concern, so they can stay in receive mode nearly all the time. Whereas for battery-powered endpoints or those powered from scavenged

power, being able to spend as long as possible in power-saving deep-sleep mode is important and so these (Class A) devices only open their receive-window briefly after transmitting. Class B devices have receive slots that are coordinated with the gateway, so they know when to wake up and start listening. This class of device could be used as an actuator that must respond to server-side commands in a timely manner, but may still operate from battery power, if necessary.

Practicalities

Because the intelligence resides in the protocol, the LoRaWAN protocol makes it simple to add endpoints, since the network handles most of the work. This ability to put an endpoint into service, provisioning an entire network, is helping to fuel the rollout of public LoRaWAN networks across the globe.

A small but growing number of modules are now available, simplifying the development of endpoints for use in LoRaWAN-based networks. Some support multiple PHY technologies to provide redundancy in critical systems.

For example, the CMWX1ZZABZ from Murata features transceivers that support both FSK and spread-spectrum, allowing it to be used in networks based on LoRaWAN or Sigfox: one module but multiple networking possibilities. Figure 4 shows a block diagram of the module, using the SX1276 transceiver and the STM32L0 ARM Cortex-M0+ microcontroller from STMicroelectronics.

Great Potential

The technologies targeting IoT and LPWANs have the greatest potential to connect disparate 'things' in the simplest way possible. The rise of public networks ready to accept an almost limitless number of endpoints removes a huge amount of the effort needed to create an IoT framework.

While the compromises necessary in LPWANs will not suit every application, for those requiring relatively simple, low-bandwidth, bi-directional communication between server applications and low- or no-maintenance endpoints, LoRaWAN offers clear benefits. ●

Optical fibre speeds up automotive applications

By Carlos Pardo, CEO and Co-Founder, KDPOF

The IEEE's latest standard amendment for 1000Mbps Ethernet, Standard 802.3bv, defines the physical layer and management parameters for automotive, industrial and home-networking applications using plastic optical fibre (POF).

Traditionally, there are two alternatives for physical layers in automotive applications: optical and copper-based, copper in the form of UTP (unshielded twisted pair), STP (shielded twisted pair), or coaxial cable. And copper-based networks are still the default choice for new architectures because of the risks and challenges of adopting new physical media. However, looking closer, copper solutions suffer from electromagnetic interference, immunity issues and lack of galvanic isolation, not to mention their weight and variable costs; see Figure 1.

The IEEE Standard

In March 2017, the IEEE Standards Association published *'IEEE Std 802.3bv – Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for 1000Mbps Operation Over Plastic Optical Fibre'* in response to demands for high-speed Ethernet solutions for automotive, industrial and home-network connectivity. POF provides unique capabilities for these applications where long link-lengths are not required.

The 1000BASE-H comprises a physical coding sublayer (PCS) and a physical medium attachment (PMA) sublayer that support physical medium dependent (PMD) sublayers for operation at 1000Mbps using dual-POF as the transmission medium. Three port types with different PMDs are defined. 1000BASE-RHC specifications are driven by requirements for automotive applications. Connection of PMD to the SI-POF medium is achieved with a PMD receptacle and mating plug. PMD, in-line connectors and cables have to support specific requirements for installation in a vehicle: Kojiri-safe (a property of the mechanical design for receptacles and mated plugs to protect sensitive functional elements, especially fibre-optic ferrules and receptacles, also called scoop-proof), dust protection, vibration robustness, tensile strength, and others.

The 1000BASE-H PCS couples a gigabit media independent interface (GMII) to the PMA sublayer, with signals transmitted in PAM-16.

The PMA sublayer includes the transmit and receive functions and protocols for managing the 1000BASE-H link. This management includes exchange of information encoded within the Physical Header Data and the state diagrams that control both the local and remote PHYs. Physical header data information is encoded into the physical header subframe. Finally, the PMD translates the transmit and receive PMA signals to and from optical signals suitable for the specified medium. The fibre-optic cabling model is shown in Figure 2.

The 1000BASE-RHx operation requires that the fibre-optic cable meets the requirements of IEC 60793-2-40 sub-category A4a.2 multimode, plastic, optical fibres with appropriate augmentation. The link segment uses two optical fibres, one for each direction, and is comprised of one or more cable sections and their in-line connections.

The 1000BASE-RHC fibre-optic channel supports a reliable link per the standard's specifications with reach of at least 40m. The channel should have a maximum insertion loss of 8dB without in-line connections and the transfer function specification, measurement techniques, spectral distribution and launching

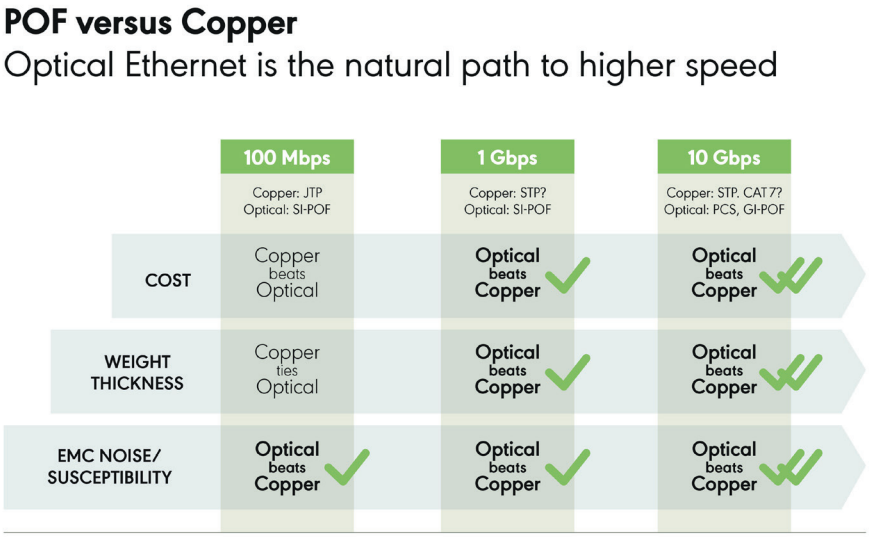


Figure 1: POF beats copper regarding cost, weight and EMC

modal power distribution per encircled angular flux (EAF) lower bound limits of the specification. The number of supported in-line connections depends on the specific in-line connection technology and the unallocated link margin.

Complete Ecosystem

POF systems are now well-proven in the automotive market, being part of several communications standards, including FlexRay, ByteFlight and MOST. It's been used in production since 1996 by several vehicle manufacturers, ensuring a large market and suppliers that comply with the strict requirements of the industry. As a plastic, large-diameter fibre, POF is cheap to manufacture and install. It does not require any sophisticated equipment or professional qualification, and harness manufacturing processes don't need to be changed.

Well-established engineering collaboration between key leading optoelectronic and connector vendors worldwide ensures a well-supplied and competitive market for all the components needed in the system: physical layer (PHY), fibre optic transceiver (FOT), fibre cable and connectors. All these companies such as Broadcom (formerly Avago), Hamamatsu, KDPOF, TE Connectivity and Yazaki, as well as the standards

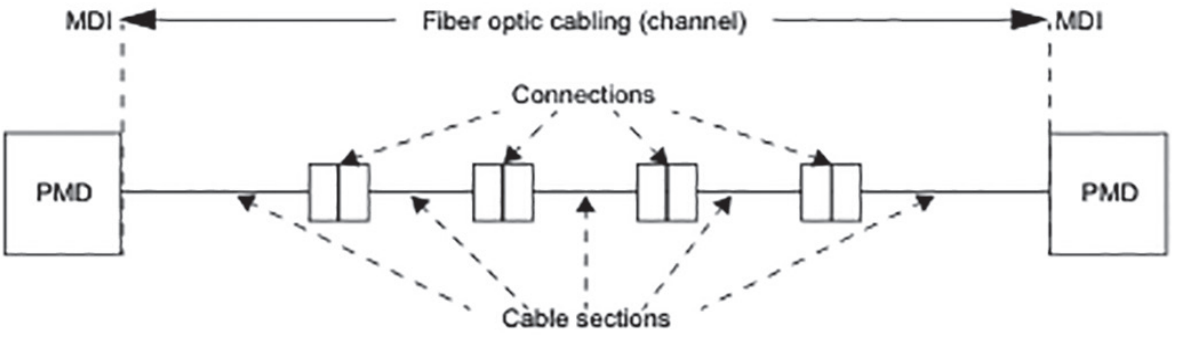


Figure 2: Fibre optic cabling model (channel)

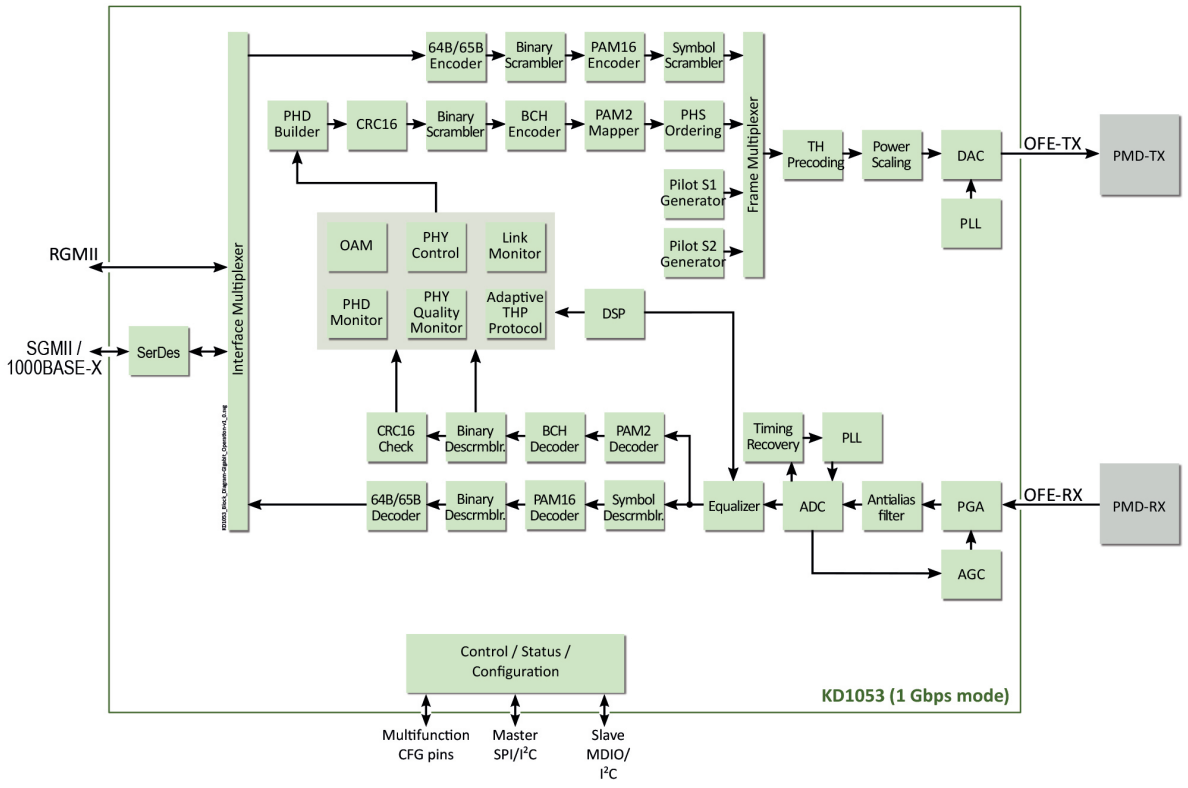


Figure 3: KD1053 block diagram for 1Gbps operation

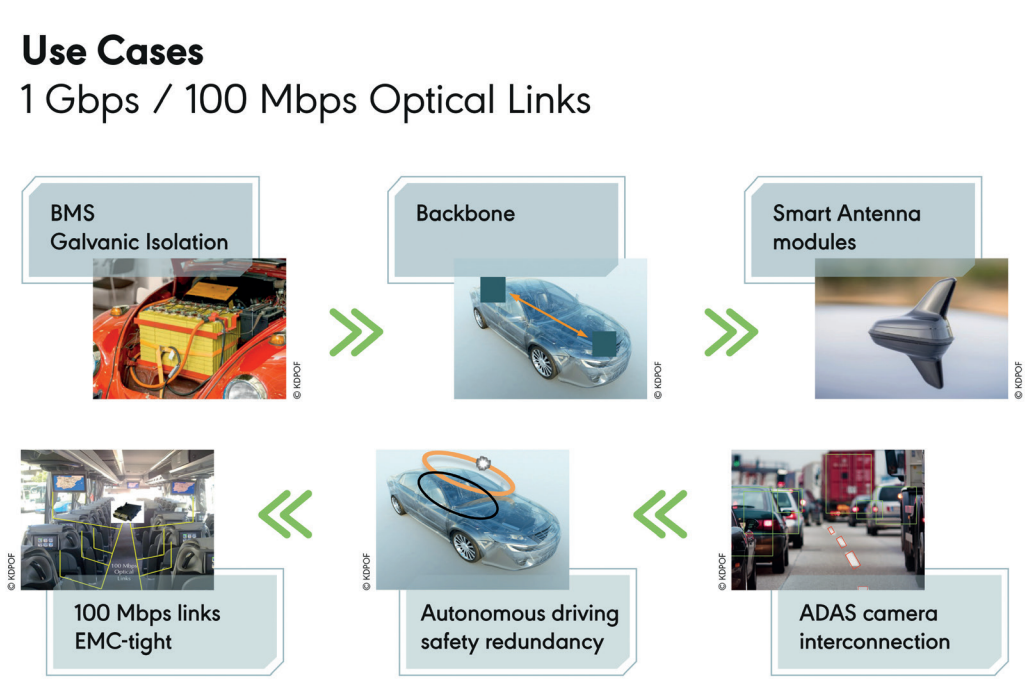


Figure 4: Applications for POF in the car range from battery management and smart antenna modules to autonomous driving and ADAS

1000BASE-H-COMPLIANT ASSP

KDPOF is a Spanish start-up that develops high-data-rate transmission solutions. Its KD1053 (Figure 3) is the first 65nm CMOS ASSP to implement the PCS and PMA sublayer of a 1000BASE-RHx PHY, compliant with the IEEE Std 802.3bv-2017 standard for gigabit optical communications over POF. KD1053 must connect to a compatible fibre optics transceiver (FOT), which implements a PMD sublayer and a medium-dependent interface (MDI) to form a complete automotive 1000BASE-RHC physical layer.

The ASSP operates at 100Mbps or 1Gbps, and is optimised for electromagnetic compatibility, low power and small footprint. It is targeted for automotive applications using optical Ethernet over POF for in-vehicle communication. Its built-in analogue interface simplifies connectivity to the PMD sublayer. It supports different parallel and serial MAC interfaces for connecting a MAC station, an MCU, or a switch.

Automotive applications with the KD1053 incorporate battery management systems, inter-domain communications backbones, antenna hubs, Ethernet 100Mbps links, autonomous driving and ADAS with surround view; see Figure 4.

bodies like the IEEE and ISO, are involved in creating new market opportunities for gigabit POF technology. Thanks to this ecosystem, customers need not worry about continuity of supply or monopolistic market situations.

Example Applications

Infotainment and beyond

Cars are not solely about driving anymore – electronic devices such as anti-collision cameras and navigation systems make the difference. Like infotainment systems, automotive driver assistance systems (ADAS) are becoming an integral part of the vehicle, with interfaces to several in-car electric/electronic systems.

Battery management systems

Electric and hybrid powertrains present different voltage domains with big level-differences: the ECU has a domain of 12V, the actuators 48V and the electric power 400V. Galvanic isolation between these domains is a must, due to ground parasitic resistance and potential shorts. Optical connections with POF provide the best means to achieve galvanic isolation in data communication.

Inter-domain communications backbone

All major carmakers agree on the advantages of segregating different functional domains such as powertrain, body, transmission and safety systems. Consequently, the typical vehicle contains several different domains, working and sharing information with others.

Going one level up in the network hierarchy, a broadband network is needed to interconnect all these domains in a reliable way. As of today, Ethernet seems the best choice. One optical PHY based on POF will deliver the needed 1Gbps, together with a full galvanic decoupling of domains, fulfilling all the requirements of today's and future systems.

Integrated smart antenna (ISA) modules

If each of the several antennas in a car is routed to its respective ECU with its own cable, the complexity will soon be unacceptable. The antenna hub is a module that routes all the signals from each antenna to an Ethernet network, connected to all the signal receptors. Gigabit Ethernet over POF (GEPOF) is ideally suited for the connection due to its natural EMC-free property. Advantages are the easy integration with existing 100Mbps designs, thanks to the existing host bus being Ethernet-compliant (SGMII/RGMII), and simple re-positioning of the antenna module thanks to an EMC-problem-free link.

Optical links

The ability to extend the use of in-line connectors is a key feature for certain car and bus makers that rely on separated wire harness sections to build the complete vehicle network. The native EMC robustness of optical fibre ensures hassle-free implementation, with plenty of tolerance of other surrounding systems that either radiate or are susceptible to electromagnetic noise.

Autonomous driving

Even the best-designed safety measure can fail. To get around this and reduce the odds of such a failure becoming a problem, engineers design complex systems with multiple layers of redundancy, so if one safety system fails, others can replace it. For automotive networks this results in copper and optical connections in parallel.

ADAS camera interconnection

A four-camera surround-view system affords the driver 360-degree visibility around the vehicle. Future camera surround-view systems will connect up to eight cameras via Ethernet. At least one 1Gbps network will be needed to provide transmission with sufficient image quality and acceptably low latency. The surroundings can be seen from different perspectives, including top-down. Such views eliminate blind spots and provide visual assistance for safe driving.

Using low-voltage drivers to boost RF power amplifier efficiency

By Mustafa Acar, Osman Ceylan, Felicia Kiebler, Sergio Pires and Stephan Maroldt, Ampleon

The growing use of wireless data is driving demand for communication systems that can transmit more data with greater energy efficiency to cut operating costs, as well as increase battery life in mobile devices. It's especially challenging for a transmitter's power amplifier (PA) to meet both demands at once, since it needs to achieve high average efficiency and at the same time cope with high peak-to-average-power ratios (PAR) of the complex wideband modulation schemes used by the latest cellular standards.

Highly-Efficient PA

The average efficiency of a PA is determined mainly by the efficiency of the driver and the end stage.

We have built a highly-efficient two-stage GaN RF PA MMIC that uses a GaN transistor operating at low voltage as a driver. This increases the average efficiency of the overall PA by decreasing the power consumption of the driver and eliminating the need for inter-stage matching between it and the end stage.

The end stage of the MMIC is terminated with a quasi-load-insensitive (QLI) Class-E load network to achieve high efficiency, despite the large output-power variation caused by load modulation. This load network is built in a standard RF package, using bond-wire and package-lead capacitance.

Load-pull measurements show that the overall power efficiency of the PA remains greater than 70%, despite a wide range of load modulations, such as an 8dB variation in output power. This sustained efficiency makes the MMIC very useful for PA architectures that rely on load modulation, such as the Doherty and Outphasing approaches.

We used our MMIC to create a demonstration PCB. The linear gain of this system measured around 27dB, with a maximum efficiency of 76% at an output power of 35.4dBm at 2.14 GHz. The supply voltages of the driver and the end stage are 5.5V and 25V, respectively. We applied a WCDMA signal with a vector-switched generalised memory polynomial digital pre-distortion (VS-GMP DPD) algorithm to the demo setup, achieving a -52.4dBc adjacent channel leakage ratio at 29.4dBm average output power.

Circuit Architecture

The schematics of the conventional and the new low-voltage driver RF PA line-ups are shown in Figure 1.

The conventional approach uses the same supply voltage for both the driver and the end stage, which means that the overall PA needs a matching network between the two. Using a low supply voltage on the driver reduces its output impedance

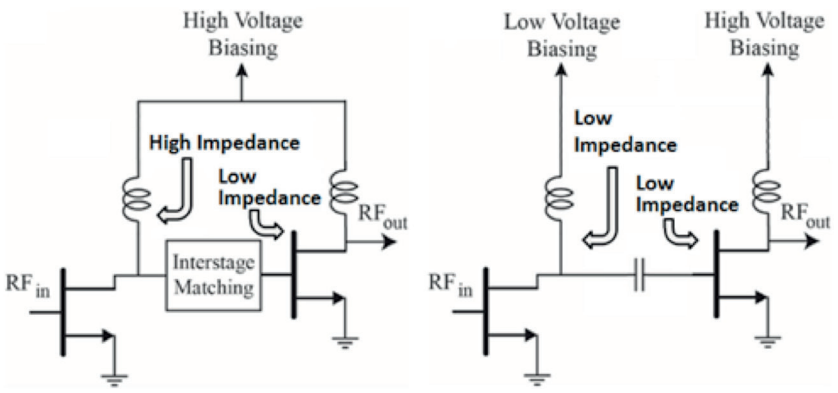


Figure 1: (Left) the conventional high-voltage driver RF PA; (Right) the low-voltage driver RF PA

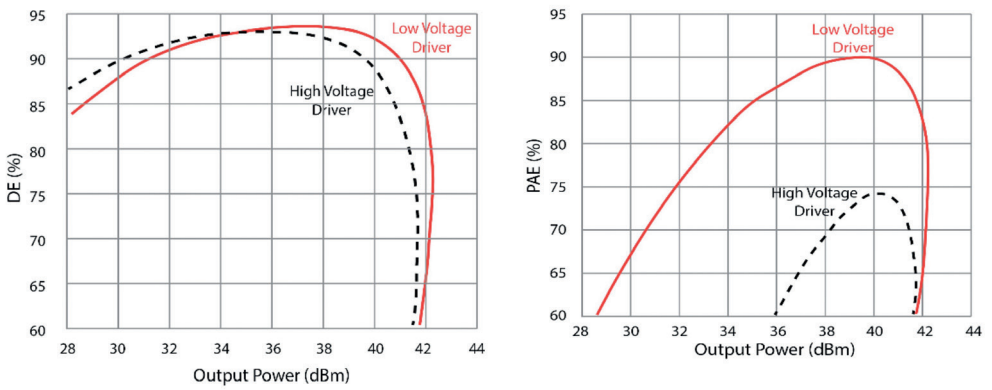


Figure 2: Simulated comparisons of drain efficiency (left) and power added efficiency (right) for the TWP driver architectures, when the PA is operating at 2.14GHz

enough that the overall PA does not need such a matching network, which reduces power losses. The low driver-supply-voltage also reduces its power consumption, which improves the overall efficiency. Removing the inter-stage matching network also cuts the size of the MMIC, lowering costs.

Figure 2 compares overall efficiency of the conventional high-voltage and the new low-voltage driver RF PA topologies in simulation. Although the simulated drain efficiencies (DE) are almost the same for high-voltage and low-voltage cases, there is a significant difference in power added efficiency (PAE).

Two-Stage GaN HEMT MMIC Design

The MMIC was built as a two-stage amplifier using Fraunhofer's IAF 0.25µm GaN HEMT technology on a multi-project wafer. The driver stage and the end stage have 0.488mm and 2.4mm total gate widths, respectively. The end-stage transistor and the driver transistor are integrated on a die with an AC-coupling capacitor and gate bias resistors, as shown in Figure 3.

The end stage of the MMIC is terminated with a QLI Class-E load network to ensure high efficiency, despite a wide variation in output powers caused by load modulation.

The MMIC and its QLI Class-E load network were assembled in a SOT1112A standard Ampleon air-cavity ceramic package using bond-wire and package lead capacitances to produce two key reactive elements: L1 at 4.9nH and C1 at 1.5pF.

Figure 4 shows the efficiency of the packaged MMIC under load-pull measurements, demonstrating it can sustain its high efficiency over large load variations.

The Demo Board

To prove the value of the low-voltage driver approach, we mounted the MMIC on a PCB and tuned its output load to match the impedance at which the MMIC alone achieved

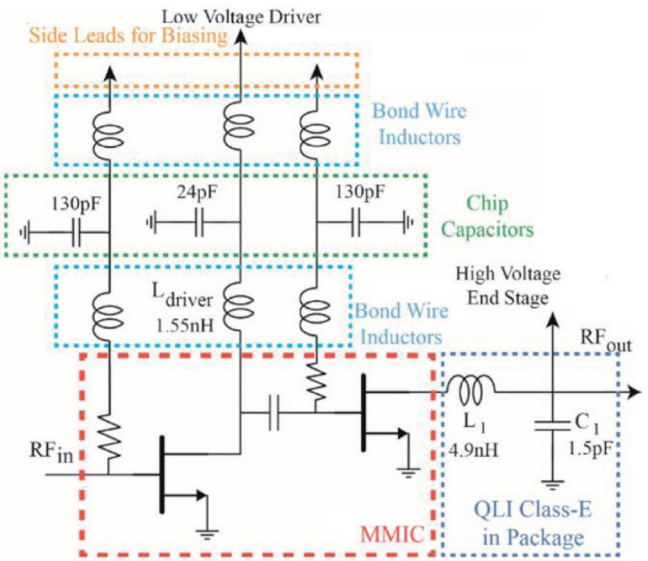


Figure 3: Schematic of the assembled MMIC and its load network

its maximum efficiency under the load-pull measurements referenced earlier.

The PCB was prepared using Rogers RO4350B as the substrate; see Figure 5, where it is shown with its biasing and matching components.

Figure 6 shows the drain efficiency, power-added efficiency and gain of the mounted PA, measured with a 2.14GHz continuous-wave signal. The peak PAE is 76%. The driver power consumption is so low that the difference between the drain and the power-added efficiency is negligible at low- and high-output power levels. The measured small signal gain is around 27dB at 2.14GHz.

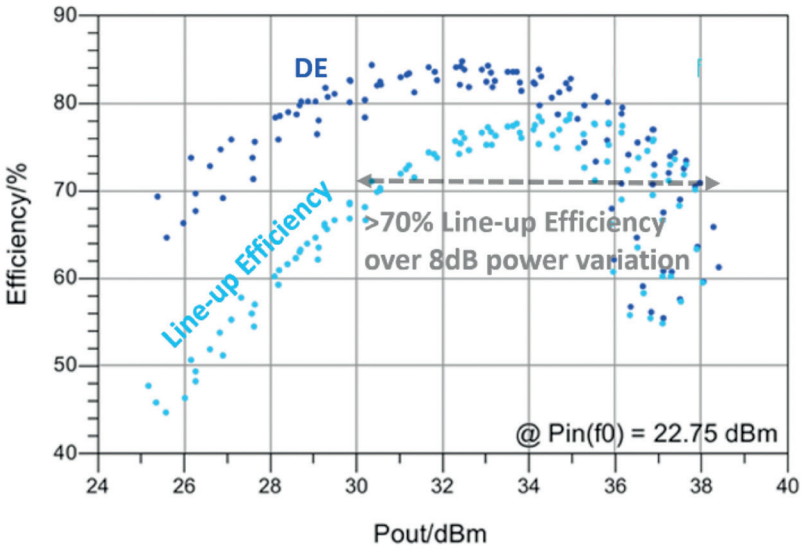


Figure 4: Drain efficiency and power added efficiency of the low-voltage driver MMIC during pulsed load-pull measurements at 2.14GHz

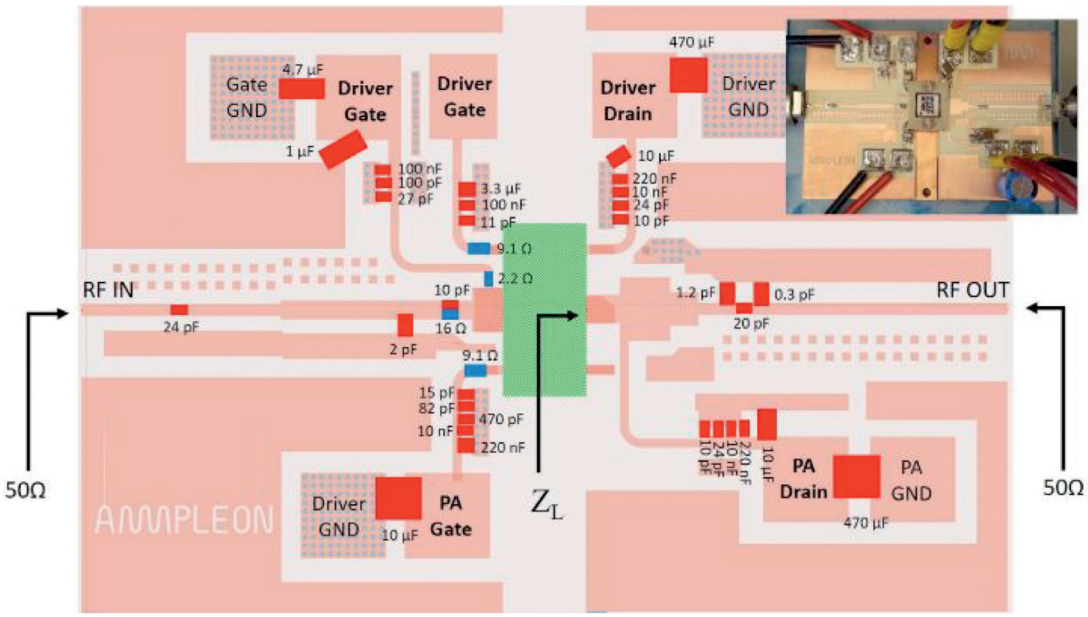


Figure 5: Components and their values on the PCB.
Inset: The mounted PA

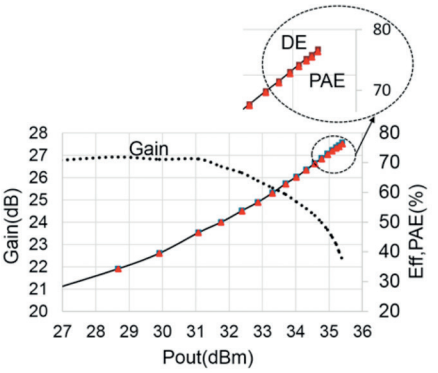


Figure 6: Measured gain, drain efficiency (black line) and power added efficiency (red squares) of the final circuit

Achieving Efficiency

Using low-voltage driver circuits can help achieve high overall PA efficiency in 0.25µm GaN HEMT technology. Our measurements show that a low-voltage driver MMIC, assembled in an RF package with a QLI Class-E load network, can create a PA with efficiency greater than 70% in the presence of an 8dB output power variation. This makes the MMIC suitable for PA architectures that rely on load modulation, such as the Doherty and Outphasing approaches. ●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VHF-band path-loss model for low-rise antennas

By Jiawei Zang and Xuetian Wang, Beijing Institute of Technology, China

Wireless sensor networks (WSN) and vehicle-to-vehicle (V2V) communications are typically characterised by antennas at low heights, generally up to 6m, leading to extensive development of near-ground path-loss modelling techniques.

A basic requirement in communications is to understand how signals propagate over a certain environment. This can be estimated with path-loss modelling, but because there's no single radio-wave propagation model that works for all environments, it means path-loss models need to be created on an ongoing basis.

The VHF Band

The 30-88MHz in the very-high-frequency (VHF) band is widely used for military and civilian applications, since it offers highly-reliable connections.

There are many path-loss models applicable to outdoor and indoor environments for this band, one of which is the empirical Hata model. This model is widely used in mobile radio services, where the base station and antenna are 30-200m above ground.

Other models cater for signal propagation inside buildings, well suited for low-rise antennas but not for rural environments. Then, there are path-loss models for vehicular communication, also based on low-height antennas. Here, however, the lower VHF band has not yet been thoroughly investigated.

In this article we will focus on path-loss measurements in the 30-88MHz range for open-space environments using whip antennas, then create a model using regression analysis.

Figure 1: Picture of the measurement site

Measurement Setup

We made measurements in a typical Chinese rural area, characterised by flat terrain covered with grass, in autumn, with a continental monsoon climate. The average annual rainfall then is 860mm and the average temperature is 14.6℃. The measurement site is an open space, with no obstructions in the signal path, which means that all measurements are line-of-sight (LOS); see Figure 1.

We placed a transmitter with an omnidirectional vertically-polarised whip antenna on top of a stationary van, about 5.5m long, 1.85m wide and 3m high. We used an Agilent E8257 signal generator to feed the antenna through a coaxial cable. The signal generator operated in continuous wave (CW) transmitting mode, with the output power fixed at 10dBm.

The receiving system in another van consisted of an Agilent E4447A spectrum analyser, connected to an omnidirectional vertically-polarised whip antenna, like that at the transmitter, also fed through a coaxial cable. Both antennas were mounted on a wooden holder located on top of the vans, about 5m above the ground.

For the measurements we kept the transmitter stationary and moved the receiver 40-270m away from it. For the path-loss calculation, we incorporated factors such as port impedance mismatch and cable loss.

The measurement setup parameters are shown in Table 1. Please note that to meet the far-field condition the measurements started at 40m, since for wire antennas the distance should be at least three wavelengths; we also added more distance as a safety margin. The

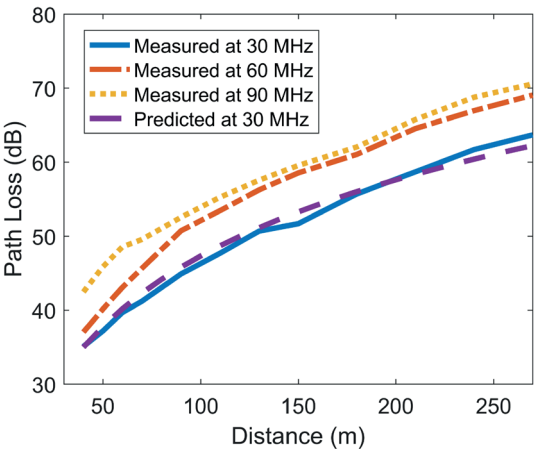

Figure 2: Path loss versus distance for various frequencies

Transmitting antenna	Omnidirectional radiation, vertical polarisation
Measurement equipment	Agilent E8257 signal generator, coaxial cable, Agilent E4447 spectrum analyser
Receiving antenna	Omnidirectional radiation, vertical polarisation
Frequency (MHz)	30, 40, 50, 60, 70, 80, 90
Distance (m)	40, 50, 60, 70, 90, 130, 150, 180, 210, 240, 270

Table 1: Measurement setup parameters

far-field condition means that all measurements are conducted in the far-field region of the antenna, because antennas are very sensitive to the nearby environment, or the so-called near-field region. We choose the far-field region to conduct all the measurements to ensure test accuracy.

Path loss is the difference between radiated and received power, and with our recordings the measured path-loss PL_m can be calculated as:

$$PL_{mea}(dB) = P_t - P_r + G_t + G_r - L_{cable} \quad (1)$$

where P_t is the transmitted power (dBm), P_r the received power (dBm), G_t is transmitting-antenna gain (dB), G_r is the receiving-antenna gain (dB) and L_{cable} is the total coaxial-cable loss of the measurement system (dB).

Next, we examine the characteristics of the signal propagation in the lower VHF range (30-90MHz). Figure 2 shows the measured path-loss as a function of distance for different frequencies. It can be seen that a longer distance leads to a greater path loss, which is not surprising, since increase in distance results in a reduction in power density.

The path loss increases exponentially with distance, too. That is $PL_{mea} \propto d^n$, where n is the path loss exponent, which can be derived using linear regression of the measured path-loss data versus the logarithm of the propagation distance. Different environments have different path-loss exponent values; for example, $n = 2$ for free space, and between 2.7 and 3.5 for urban cellular communications. Clearly, the larger the path-loss exponent, the greater the path loss with distance.

Figure 3 shows the plot of the path loss as a function of frequency for different distances. It can be seen that the path loss increases with frequencies at a fixed distance, which means that path loss depends on both distance and frequency.

Ground-Wave Model

The physics behind the measured data can be explained by a ground-wave model. "Ground wave" refers to the propagation of radio waves parallel and adjacent to the surface of the Earth, following its curvature. A radiative ground wave is known as the Norton surface wave. In addition to direct and ground-reflected waves, a Norton surface wave occurs in the lower VHF band because the wavelength in this frequency range is comparable to the antenna elevation,

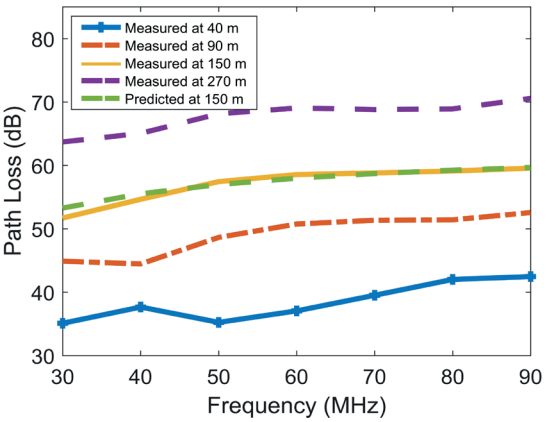

Figure 3: Path loss versus frequency for various distances

usually about 2-6m above ground. In such situations the surface wave can't be neglected and plays an important role on wave propagation.

Based on the ground-wave model, path loss can be expressed as:

$$PL(dB) = 20\log\left(\frac{\lambda}{4\pi d}\right) + 20\log\left(1 + \Gamma e^{j\Delta} + (1-\Gamma)Ae^{j\Delta}\right) \quad (2)$$

where d is propagation distance, λ is the wavelength in free space, Γ is the ground reflection coefficient, Δ is the phase difference between the direct and the reflected waves, and A is the surface wave attenuation factor. Δ and A are then:

$$\begin{cases} \Delta = \dfrac{4\pi h_t h_r}{\lambda d} \\ A = \dfrac{-1}{1 + j\dfrac{2\pi d}{\lambda}(\sin\theta + z)} \end{cases} \quad (3)$$

where h_t and h_r are the transmitting and receiving antenna elevations, respectively; θ is the angle of incidence; z is $\sqrt{\varepsilon - \cos^2\theta}/\varepsilon$ for vertical polarisation, and ε is the complex relative permittivity of the ground.

Results of the predicted path loss using Equation 2 are also shown in Figures 2 and 3. They show that the measured and predicted results using the ground-wave model are in strong agreement.

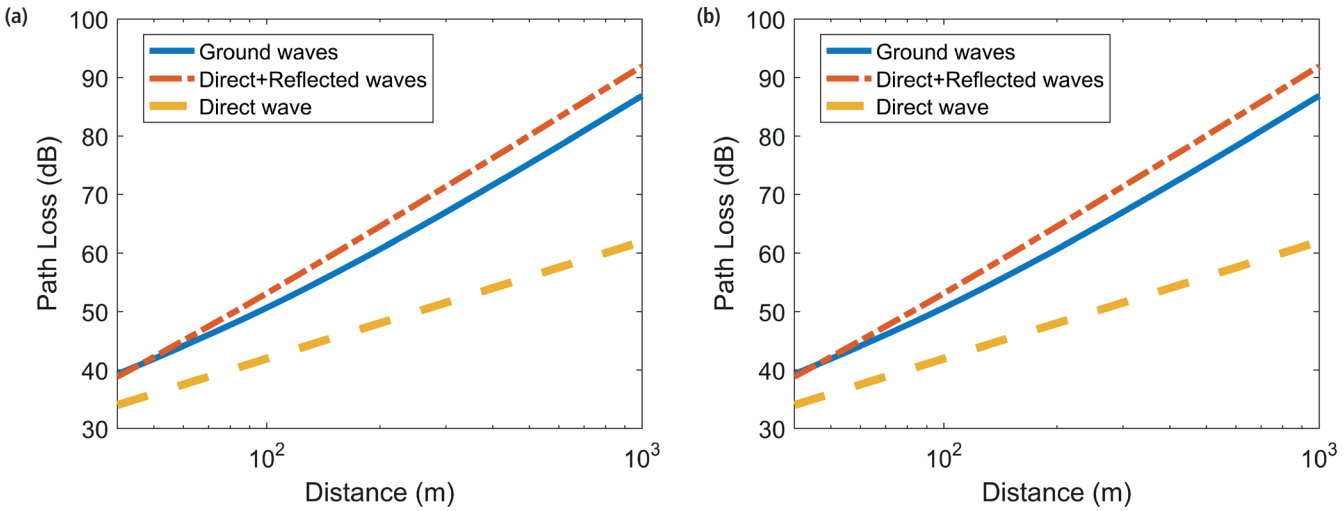

Figure 4: Effects of various wave components on path loss: (a) path loss versus distance, (b) path loss versus frequency

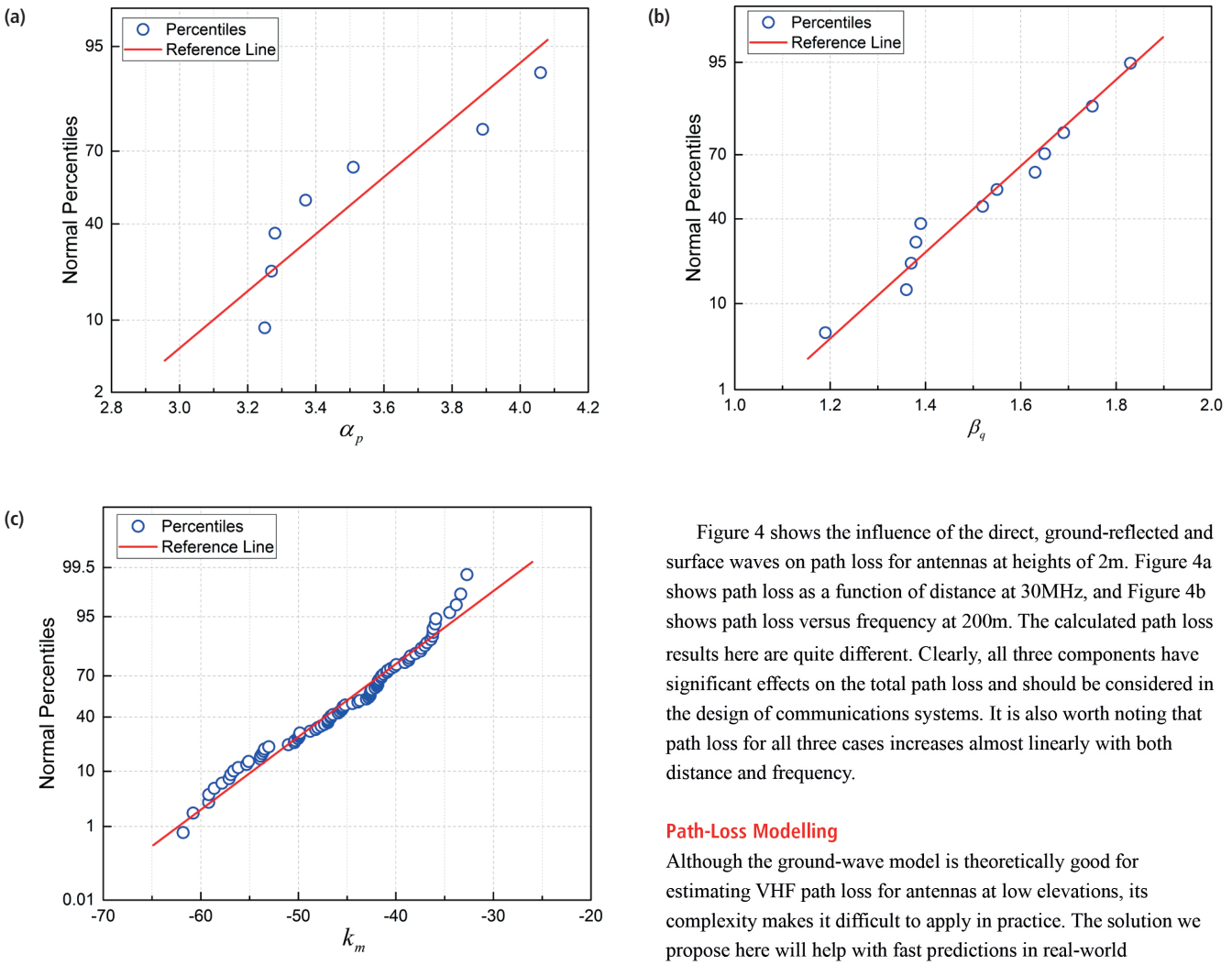

Figure 5: Results and distributions of the derived parameters: (a) α_p ; (b) β_q ; (c) k_m

Figure 4 shows the influence of the direct, ground-reflected and surface waves on path loss for antennas at heights of 2m. Figure 4a shows path loss as a function of distance at 30MHz, and Figure 4b shows path loss versus frequency at 200m. The calculated path loss results here are quite different. Clearly, all three components have significant effects on the total path loss and should be considered in the design of communications systems. It is also worth noting that path loss for all three cases increases almost linearly with both distance and frequency.

Path-Loss Modelling

Although the ground-wave model is theoretically good for estimating VHF path loss for antennas at low elevations, its complexity makes it difficult to apply in practice. The solution we propose here will help with fast predictions in real-world applications.

Parameter	μ_α	μ_β	μ_k	δ_α	δ_β	δ_k
Value	3.52	1.53	-45.4	0.33	0.19	7.2

Table 2: Statistical results of parameters in the path-loss model

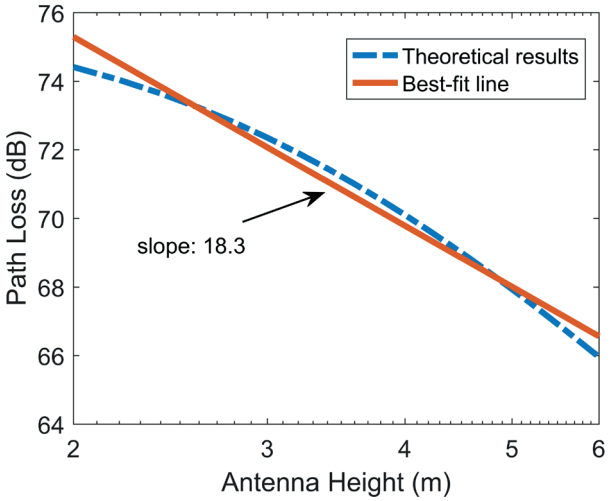

Figure 6: Effects of antenna elevation on path loss

The path loss in free space can be written as:

$$PL_{fre} = -27.6 + 20\log\_10(d) + 20\log\_10(f)$$

where d is in meters and f in MHz. However, in a real environment the free-space condition can't be met, so the contributions of direct, reflected and surface waves must be included. As discussed earlier, path loss varies linearly with both distance and frequency on a logarithmic rate. Therefore, a general path-loss formula based on a real environment is given by:

$$PL_{pro} = k + 10\alpha\log\_10(d) + 10\beta\log\_10(f) \quad (4)$$

where α indicates how fast the path loss increases with distance, β indicates how fast the path loss increases with frequency, and k is a constant for the measured data. All the parameters can be derived from the measured path-loss data using regression analysis.

First, we investigate the relation between the measured path-loss PL_{mea} and distance d. Through regression analysis of PL_{mea} by d at each frequency listed in Table 1, the regression coefficient α_p in Equation 4 can be determined for all frequencies, where p denotes the different frequencies; see Figure 5a.

Next, we examine the regression coefficient β in Equation 4. The coefficient β_q can be obtained by regression analysis of PL_{mea} by f for each distance displayed in Table 1. Similarly, the subscript q denotes different measured distances in the experiments.

The obtained values of β_q are shown in Figure 5b, which helps determine k_m, or the residual of $PL_{mea} - 10\alpha_p\log\_10(d) - 10\beta_q\log\_10(f)$. Here, the subscript m denotes the measured data. The results for k_m are shown in Figure 5c.

Then, we study the statistics of the derived parameters α_p, β_q and k_m. It is necessary to display the normal probability plot of these parameters; see Figure 5, where they all have a near-normal distribution, depicted by the straight line. The mean and standard deviation values of those parameters are given in Table 2. Here we use $\mu\_$ and $\delta\_$ for the mean and standard deviations of a normal distribution, respectively. Based on the above findings we can approximate α, β and k as Gaussian variables, thus the parameters α, β and k can be written as:

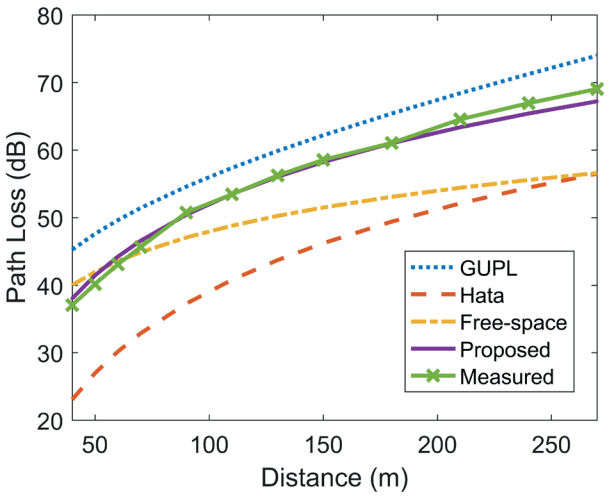

Figure 7: Comparisons of models with measured data at 60MHz

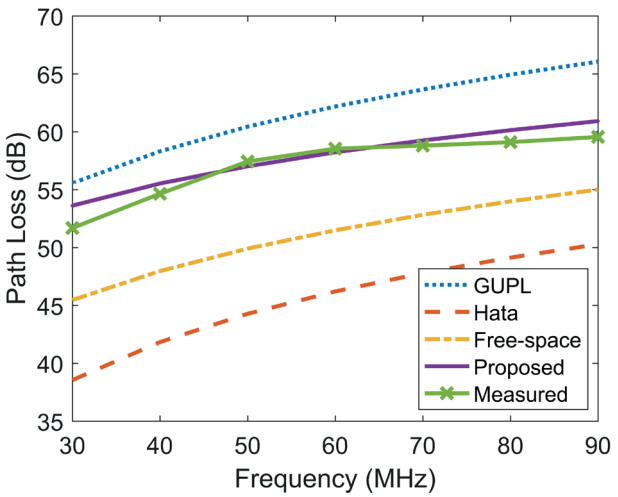

Figure 8: Comparisons of models with measured data at 150m

$$\begin{cases} \alpha = \mu_\alpha + \delta_\alpha x_1 \\ \beta = \mu_\beta + \delta_\beta x_2 \\ k = \mu_k + \delta_k x_3 \end{cases} \quad (5)$$

where x_1, x_2 and x_3 are zero-mean, unit-standard deviation Gaussian variables $N[0,1]$. So, Equation 4 can be written as:

$$PL_{pro} = [\mu_k + 10\mu_\alpha \log\_10(d) + 10\mu_\beta \log\_10(f)] + [\delta_k x_3 + 10\delta_\alpha x_1 \log\_10(d) + 10\delta_\beta x_2 \log\_10(f)] \quad (6)$$

where the term inside the first set of square brackets is the median path-loss and the term inside the second set is the random variation from the corresponding median. Equation 6 provides a prediction interval due to the inclusion of the variable component. In engineering, it is only necessary to obtain the median path-loss with minimal complexity. Thus, considering the derived parameters in Table 2, the practical version of Equation 6 can be re-written as:

$$PL_{pro} = -45.4 + 35.2\log\_10(d) + 15.3\log\_10(f) \quad (7)$$

It should be noted that we used 5m in Equation 7 for the antenna elevation. To predict path loss for scenarios with arbitrary antenna elevations, this should be included in the equation accordingly.

Figure 6 shows path loss versus transmitting antenna elevation. The linear best-fit line is also displayed. The same is true for the receiving antenna (not shown). Taking the 5m antenna elevation as reference, the final proposed empirical path-loss formula is then:

$$PL_{pro} = -20 + 35.2\log\_10(d) + 15.3\log\_10(f) - 18.3\log\_10(h_t) - 18.3\log\_10(h_r) \quad (8)$$

where d, h_t and h_r are in meters, and f in MHz.

The prediction accuracy of Equation 8 is compared to the Hata, GUPL and free-space models. The equation of the open-space case with the Hata model is evaluated, and so is the equation for an outdoor scenario with the GUPL model.

For comparison, we extrapolated the applicable distance and frequency of the Hata model from 40-1000m and 30-150MHz. Figure 7 shows the path loss as a function of distance at a frequency of 60MHz, and Figure 8 shows the path loss as a function of frequency at a distance of 150m.

We observe that the measured path loss is larger than the predicted path loss using the free-space model. This confirms that both ground-reflected and surface waves are important in wave propagation for low antenna elevations and can't be ignored as in the free-space model. The Hata model underestimates the path loss, mainly because it was developed based on measured data for a land mobile radio service, which is characterised by base-station antenna heights over 30m. Antennas at high elevations lead to low path loss.

In turn, the GUPL model overestimates the path loss because

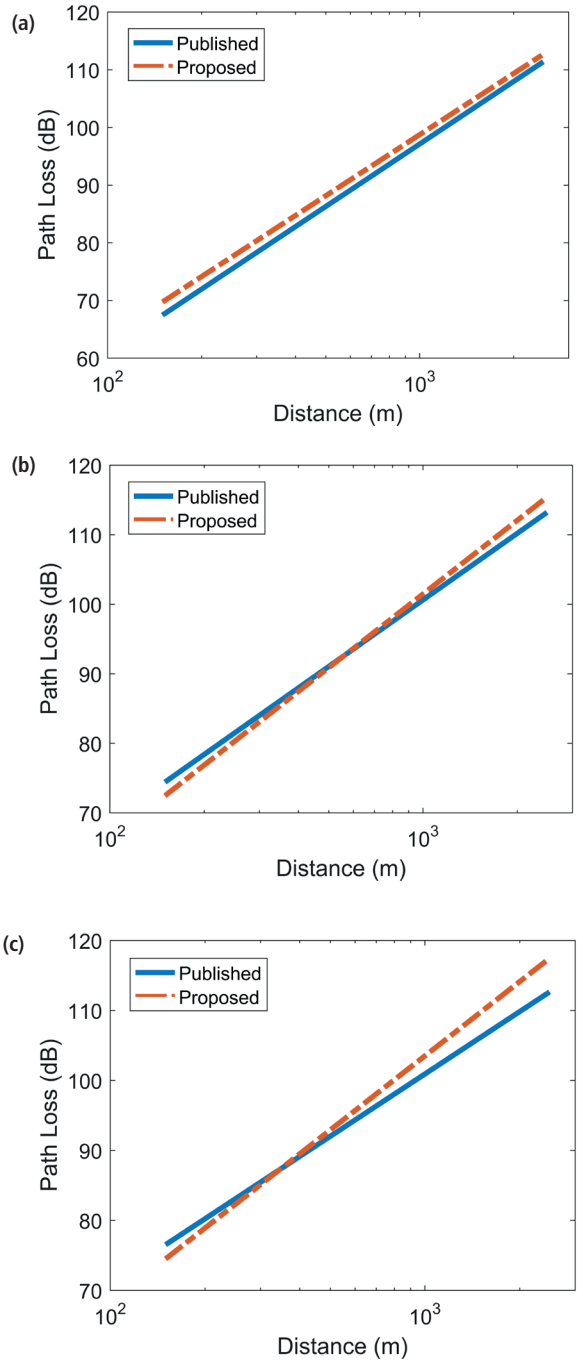

Figure 9. Comparisons of the proposed empirical model with published data at various frequencies with antennas at heights of 2m: (a) 37.8MHz; (b) 57MHz;(c) 77.5MHz

antenna elevations are not included, and the model is established using collected data with antenna heights of about 2m.

The measured results in Figures 7 and 8 were obtained with antenna heights of 5m, and thus we find that the proposed model (Equation 8) can closely predict path loss.

Independent researchers tested our model in a rural environment, with the results shown in Figure 9 for 37.8, 57 and 77.5MHz and antenna heights of 2m. Good consistency between the proposed model and published measurements were observed in all cases. ●

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New quad-mode crossed resonator and its use in bandpass filters

By Jun Cheng, Qin Zhang, Xiu Shan Liu, Yi Fan, Li Gong Wang and Xiong Ying Liu

Multi-band filters are widely employed in wireless communications, leading to many diverse types of microwave filters, including in dual- and tri-band bandpass circuits. Recently, we've started seeing more quad-band bandpass filters; a popular method of their implementation is to combine two or more different bandpass filters (BPFs) together. Unfortunately, such combinations often lead to larger size and more complex feed structure.

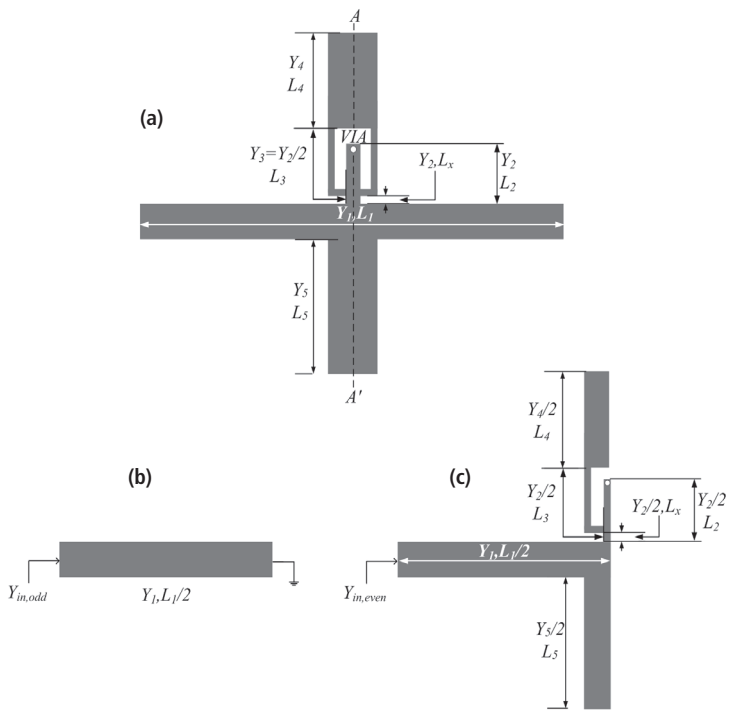

Figure 1:
(a) Configuration of the proposed resonator;
(b) Odd-mode equivalent circuit;
(c) Even-mode equivalent circuit

Multi-mode resonators (MMRs) can be used to implement quad-band filters, but sadly with poor passband selectivity and greater complexity.

In this article we propose a new quad-mode crossed resonator for the design of quad-band bandpass filters. Due to its simplicity, the filter has a small footprint and can be easily analysed.

The proposed resonator consists of a microstrip half-wavelength resonator, open and short stubs, and a stepped-impedance stub (SIS); see Figure 1a. All the stubs are loaded at the centre of the half-wavelength resonator.

The proposed resonator has four operating frequencies, three adjustable and one fixed, enabling the design of a quad-band bandpass filter with multiple transmission zeros. We applied a pseudo-inter-digital coupling format between resonators to improve out-of-band performance.

The Proposed Resonator

The proposed resonator is symmetrical on the A-A' plane, allowing odd- and even-mode analysis. The equivalent circuit for odd-mode excitation is shown in Figure 1b, with odd-mode input admittance of:

$$Y_{in,odd} = \frac{Y_1}{j \tan(\theta_1 / 2)} \quad (1)$$

where $\theta_1 = \beta L_1$ is the electric length of the half-wavelength microstrip line. When $Y_{in,odd} = 0$, the first odd-mode resonant frequency can be expressed as:

$$f_{odd} = \frac{c}{2L1\sqrt{\varepsilon_{eff}}} \quad (2)$$

where c is the speed of the light in free space, and ε_{eff} is the effective dielectric constant of the substrate. Equation 2 shows that the odd-mode resonant frequency is not affected by any loaded stubs.

Figure 1c shows the equivalent circuit for even-mode excitation;

it contains three resonant circuits: an open stub, a short stub and an SIS.

For the short stub resonator in Figure 2a, the input impedance can be expressed as:

$$Y_{in,even1} = -jY_1 \frac{Y_2 - 2Y_1 \tan(\theta_1/2)\tan(\theta_2)}{2Y_1 \tan(\theta_2) + Y_2 \tan(\theta_1/2)} \quad (3)$$

where $\theta_i = \beta L_i$ is the electric length of the microstrip line. For $Y_{in,even1} = 0$:

$$\tan(\theta_1/2)\tan(\theta_2) = \frac{Y_2}{2Y_1} \quad (4)$$

For $Y_2 = 2Y_1$:

$$\theta_1/2 + \theta_2 = \frac{(2n-1)\pi}{2} \quad (5)$$

or

$$L_1/2 + L_2 = \frac{(2n-1)\lambda_g}{4} \quad (6)$$

where λ_g is the guided wavelength at even-mode resonance. Thus, the first resonant frequency of this stub can be determined with:

$$f_{even1} = \frac{c}{(2L_1 + 4L_2)\sqrt{\varepsilon_{eff}}} \quad (7)$$

For the open-stub resonator (Figure 2c), the input impedance can be expressed as:

$$Y_{in,even3} = jY_1 \frac{2Y_1 \tan(\theta_1/2) + Y_2 \tan(\theta_5)}{2Y_1 - Y_2 \tan(\theta_1/2)\tan(\theta_5)} \quad (8)$$

For the resonance condition of $Y_{in,even3} = 0$ the equation is:

$$\cot(\theta_1/2)\tan(\theta_5) = -\frac{2Y_1}{Y_5} \quad (9)$$

For the special case of $Y_5 = 2Y_1$, it can be derived as:

$$\theta_1/2 + \theta_5 = n\pi \quad (10)$$

or

$$L_1/2 + L_5 = \frac{n\lambda_g}{2} \quad (11)$$

Thus, the first resonant frequency of this stub can be determined with:

$$f_{even3} = \frac{c}{(L_1 + 2L_5)\sqrt{\varepsilon_{eff}}} \quad (12)$$

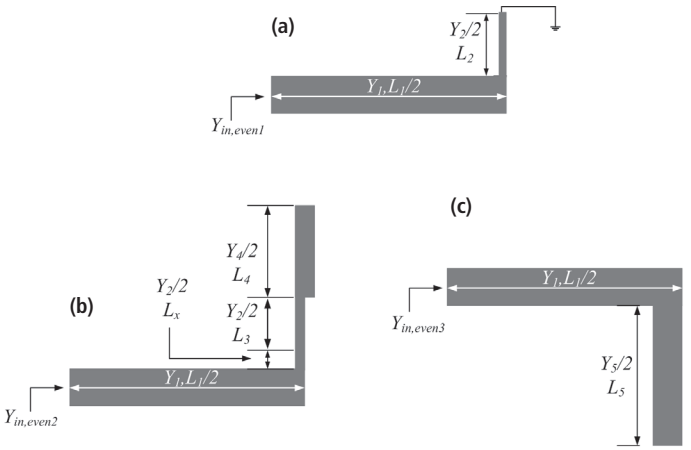

Figure 2:
(a) Part 1 of even-mode equivalent circuit;
(b) Part 2 of even-mode equivalent circuit;
(c) Part 3 of even-mode equivalent circuit

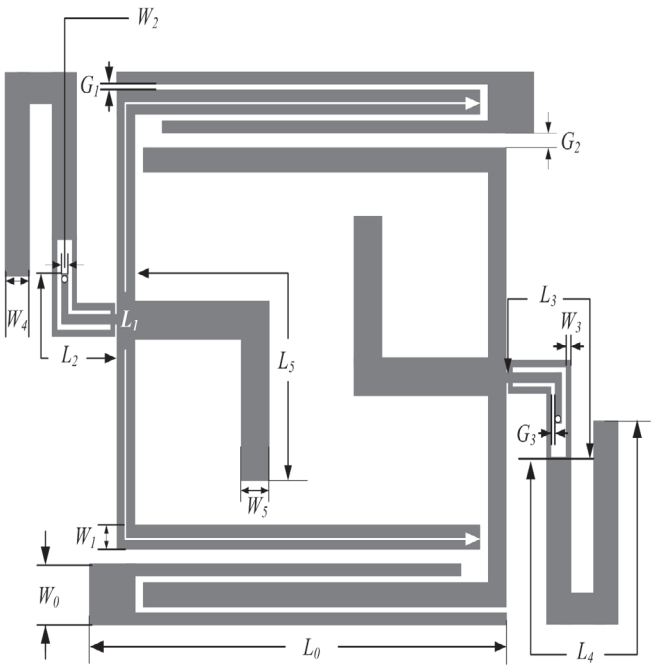

Figure 3: Configuration of the proposed bandpass filter

For the SIS resonator (Figure 2b), the input impedance is:

$$Y_{in,even2} = \frac{Y_1[Y_{in,sis} + jY_1 \tan(\theta_1/2)]}{Y_1 + jY_{in,sis}\tan(\theta_1/2)} \quad (13)$$

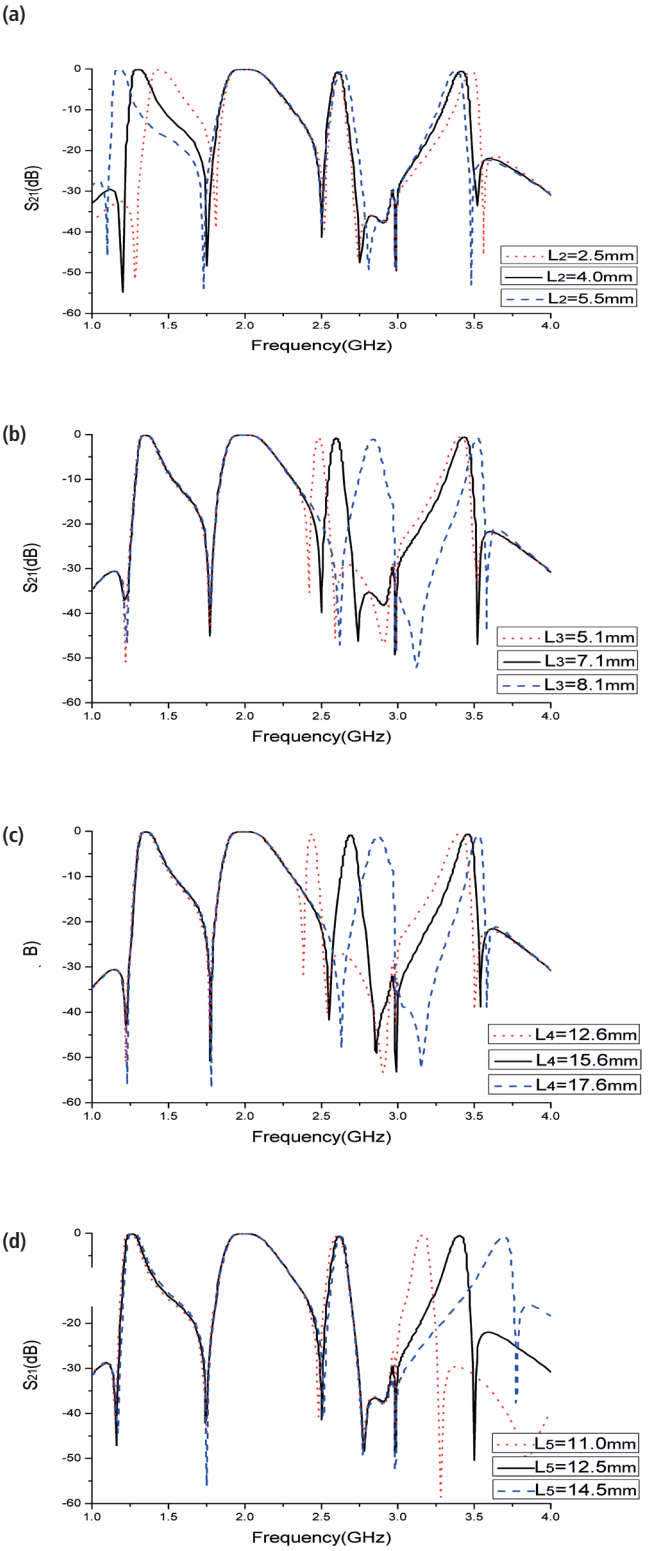

Figure 4: Simulated S21 against (a) L2; (b) L3; (c) L4; (d) L5

$$Y_{in,sis} = \frac{(\frac{Y_2}{2})[j\frac{Y_4}{2}\tan\theta_4 + (j\frac{Y_2}{2})\tan(\theta_3+\theta_x)]}{\frac{Y_2}{2} + j[j\frac{Y_4}{2}\tan\theta_4\tan(\theta_3+\theta_x)]} \quad (14)$$

where $\theta_i = \beta L_i$.

From $Y_{in,even2} = 0$, and according to Equation 14, the first resonant frequency of this stub can be achieved as f_{even2}. L_x should be as short as possible to reduce coupling between the short stub and the SIS. In practice, the effect of L_x can be ignored.

From the above analysis, we learn that f_{odd} is determined by L_1; f_{even1} is determined by L_1 and L_2; f_{even2} is mainly governed by L_1, L_3 and L_4; and f_{even3} is mainly controlled by L_1 and L_5. Thus, the design procedure for the quad-band bandpass filter with our proposed resonator is as follows:

- Select the appropriate length for L_1 according to Equation 2;
- Adjust the length of the short stub L_2 according to Equation 7;
- Tune the length of the open stub L_5 according to Equation 12;
- Change the lengths of L_3 and L_4 according to Equations 13 and 14.

Quad-Band Bandpass Filter Design

The filter's configuration is shown in Figure 3. It comprises two quad-mode crossed resonators coupled in a cascaded format. Its passband frequencies are mainly determined by the entire length L_1 of the half-wavelength resonator and the lengths of the loaded stubs. To verify our analysis, a full-wave simulation was carried out by a high-frequency structure simulator (HFSS), with a fixed length L_1.

As Figure 4a shows, by changing the short stub length L_2, the first passband frequency can be shifted greatly, whereas the second passband frequency remains fixed, with the third and fourth passband frequencies varying a little. Figures 4b and c show that L_3 and L_4 have a main influence on the third passband frequency and a minor influence on the fourth passband frequency. From Figure 4d

The coupling characteristics between the corresponding microstrip lines tend to influence the pass-bandwidth of the filter

we can determine that L_5 has a marked impact on the fourth frequency and almost no effect on the others.

The coupling characteristics between the corresponding microstrip lines tend to influence the pass-bandwidth of the filter, so it's necessary to study them to understand how to control the bandwidth.

This confirms that the lengths of the microstrip lines determine the filter's resonant frequencies, and vice versa. Thus, changing the gap widths between microstrip lines controls the bandwidth of the filter accordingly.

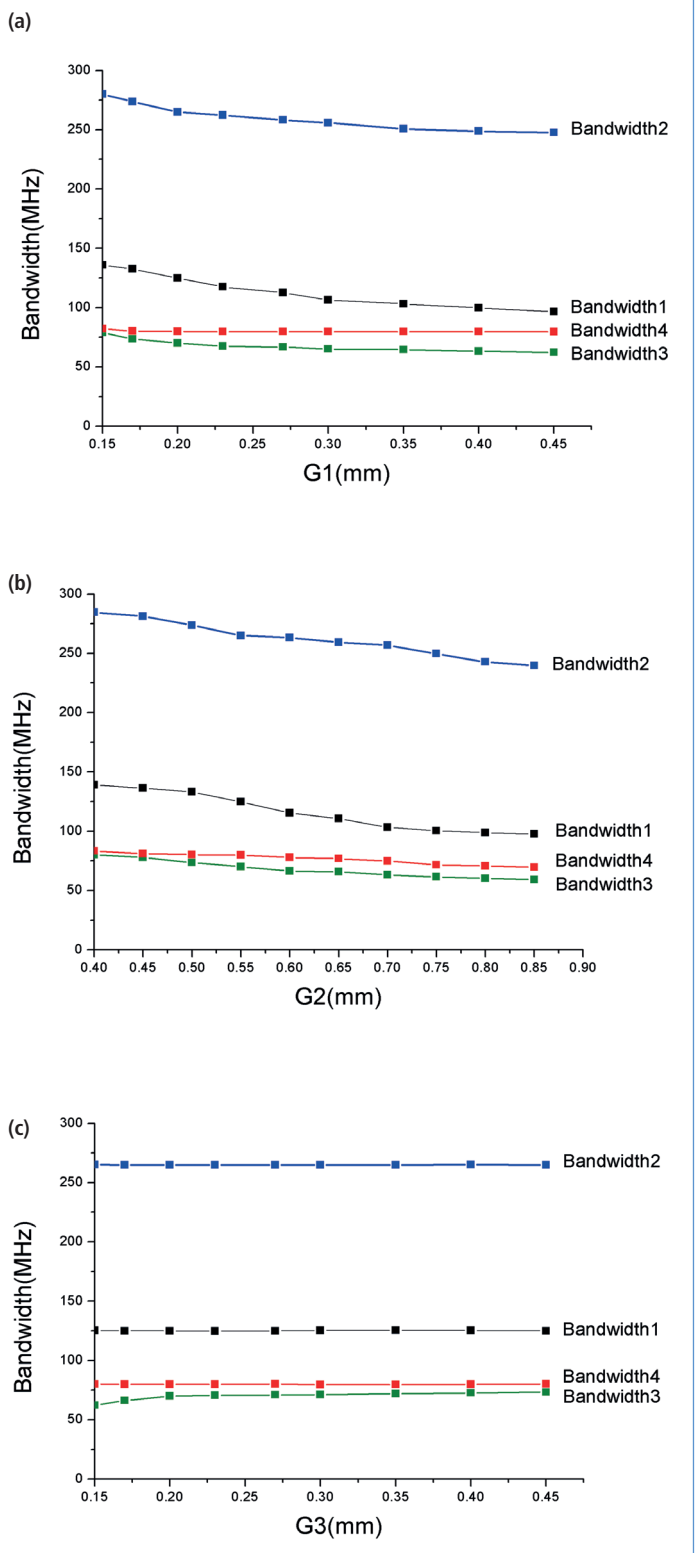

Figure 5: Simulated bandwidths against (a) G1; (b) G2; (c) G3

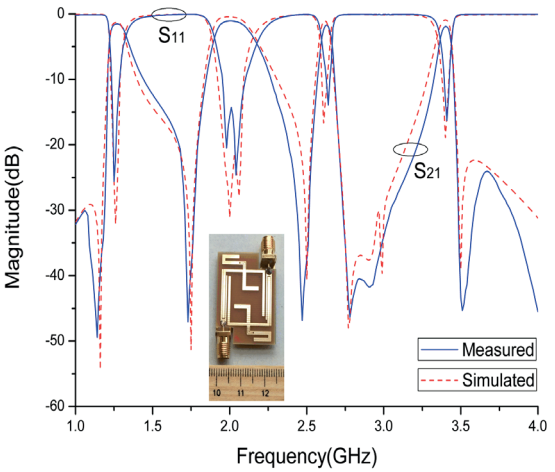

Figure 6: Simulated and measured results of the proposed filter

The specific positions of the gaps are shown in Figure 3, as G_1, G_2 and G_3. As shown in Figure 5a, when G_1 increases, the bandwidth of the first, second and third passband decrease accordingly, while the fourth passband keeps almost constant. Figure 5b shows that when G_2 increases, the four passbands shrink.

From Figure 5c we can tell that G_3 only affects the bandwidth of the third passband and has almost no impact on the others. Thus, by changing G_3 we can control the bandwidth of the third passband and, then, by adjusting the values of G_1 and G_2 we can control the bandwidths of the other passbands. It should be noted that when G_1 or G_2 increase, the insertion loss of each passband will increase accordingly, which needs to be considered when designing the filter.

Filter Design

We made the quad-band bandpass filter on a substrate 0.8mm thick with a relative dielectric constant of 2.33. Its total size is less than 21mm × 32mm, with $0.18\lambda_g$ x $0.13\lambda_g$, where λ_g is the guided wavelength of the substrate at the centre frequency of the first passband.

We selected the following dimensions (mm):

$L_0 = 21.8$, $L_1 = 54$, $L_2 = 4.2$, $L_3 = 6$, $L_4 = 16.6$, $L_5 = 12.5$, $W_0 = 2.4$, $W_1 = 1$, $W_2 = 0.4$, $W_3 = 0.2$, $W_4 = 1.28$, $W_5 = 1.5$, $G_1 = 0.2$, $G_2 = 0.55$, $G_3 = 0.2$.

Figure 6 shows that the simulated and measured results are in good agreement. The fabricated filter has four measured passbands centering at 1.27, 2.0, 2.63 and 3.4GHz; and the 3dB fractional bandwidths in the same sequence are 9.84, 13.25, 2.66 and 2.35%. The minimum insertion losses are 1.5, 1.1, 1.7 and 1.9dB, whereas the return losses in all bands are below -13dB. In addition, the proposed quad-band bandpass filter has multiple transmission zeros, which gives it greater selectivity.

A 60GHz CMOS differential power amplifier with capacitive cross-coupling neutralisation

By Wang Wei, Huang Meng Jia, Yang Hao, Chen Ting, Yang Zheng Lin, Yuan Jun and Wang Guan Yu, Chongqing University of Post and Telecommunications, China

Interest in 60GHz high-density, short-range, wireless communication for wireless personal area networks (WPANs) has led to efforts to optimise power amplifiers (PAs). Although CMOS technology offers low cost, low power and easy integration, CMOS power amplifiers are still the most challenging part of an RF transceiver due to their low-Q passive components, high substrate losses, low transconductance (G_m) and low breakdown-voltage limits.

On the other hand, millimeter-wave PAs are based on gallium arsenide (GaAs), which offers excellent performance, but is more expensive. Nowadays, a blend of the two technologies – high-performance yet low-cost PAs, may be found in the so-called mm-wave CMOS PAs. Here, the power gain and output power are limited by the scale of the CMOS technology and the breakdown-voltage limits are improved. However, some combining methods can raise the output power gain at the expense of a large layout area and poor power density.

The PA's Structure

Performance of the 60GHz PA is greatly influenced by the gate drain capacitance C_{gd} of the transistor, which may result in reduced power gain, reduced stability and reverse isolation. To solve this, using a two-stage fully-differential power amplifier with a cross capacitor counteracts the influence of C_{gd} without increasing power consumption. By using matching network optimisation, the PA's performance and power density can be improved.

One of the main challenges in designing a mm-wave CMOS PA is performance degradation due to various parasitic parameters. The negative feedback of the C_{gd} capacitance results in very low reverse isolation, reducing power gain and stability. For PAs with a certain output power, transistors are usually large, so their corresponding parasitic capacitance C_{gd} is larger too. Using capacitive cross-coupling neutralisation techniques helps.

Figure 1 shows a differential structure PA with capacitive cross-coupling neutralisation. The cross-coupling capacitance C_c is connected to the opposite transistor through its gate electrode; transistor leakage can be considered as negative C_c, so it can neutralise the influence of C_{gd} and improve reverse isolation.

The role of the cross-coupling capacitance C_c is analysed as follows: The small-signal analysis diagram of the PA is shown in Figure 2, and can be regarded as a differential two-port network, with difference Y parameters expressed as:

$$Y_{11}=\text{Ggs}+j\omega[Cgs+Cgd+Cc] \quad (1)$$

$$Y_{12}=-j\omega[Cgd-Cc] \quad (2)$$

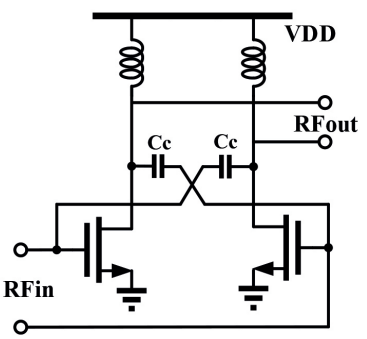

Figure 1: Capacitive cross-coupling neutralisation

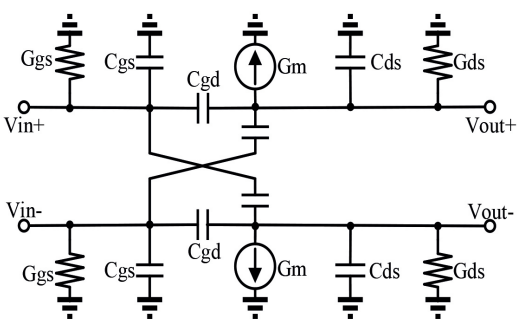

Figure 2: Small signal equivalent circuit of C_c

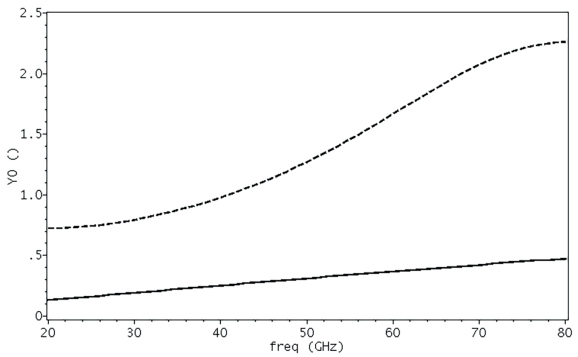

Figure 3: Simulated stability for the factor K

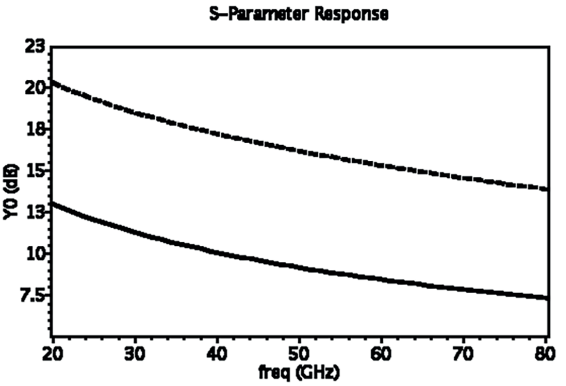

Figure 4: Simulated maximum available gain

$$Y_{21} = Gm - j\omega[Cgd - Cc] \quad (3)$$

$$Y_{22} = Gds + j\omega[Cds + Cgd + Cc] \quad (4)$$

where C_c is the cross-coupling capacitance, C_{gd} the parasitic capacitance between the grid and the drain electrode, C_{gs} the capacitance between the gate and the source electrode, C_{db} the drain-to-bulk capacitance, G_{gs} gate transimpedance, G_{ds} drain transimpedance and G_m transconductance. Equation 2 shows that the cross-coupling can reduce the effect of the gate-to-drain parasitic capacitance, improving reverse isolation.

The stability factor K can be expressed by the two-port Y-parameter as per Equation 5. When the amplifier is unconditionally stable, the stability factor K is greater than one.

$$K = \frac{2\,\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|} = \frac{2Ggs \times Ggd + \omega^2[Cgd - Cc]^2}{\omega|Cgd - Cc|\sqrt{\omega^2[Cgd - Cc]^2 + Gm}} \quad (5)$$

Simulation results of the differential pairs' stability are shown in Figure 3. The use of cross-coupling capacitance has improved the stability of the circuit at 60GHz, with K increasing from 0.38 to 1.68, putting the circuit in a stable state.

Maximum available gain is obtained by matching the input and output ports to their conjugate impedances. The maximum available gain G_{mag} is then:

$$G_{mag} = \left|\frac{Y_{21}}{Y_{12}}\right|(K - \sqrt{K^2 - 1}) = \frac{\sqrt{\omega^2(Cgd - Cc)^2 + Gm}}{\omega|Cgd - Cc|}(K - \sqrt{K^2 - 1}) \quad (6)$$

Maximum stable gain G_{msg} is reached when the maximum available gain of K = 1. Maximum stable gain of the capacitive cross-coupling amplifier can also be represented by:

$$G_{msg} = \left|\frac{Y_{21}}{Y_{12}}\right| = \frac{\sqrt{\omega^2(Cgd - Cc)^2 + Gm}}{\omega|Cgd - Cc|} \quad (7)$$

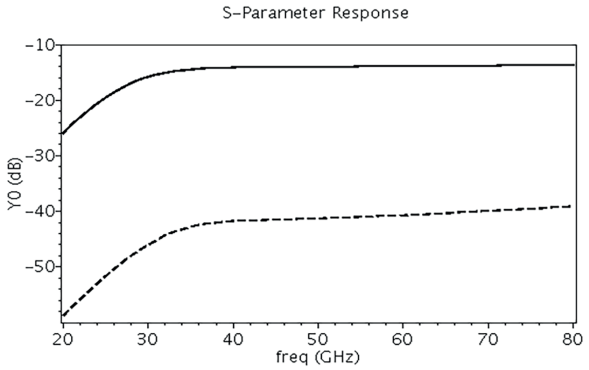

Figure 5: Simulated reverse isolation

Figure 6: Inductance of the top metal

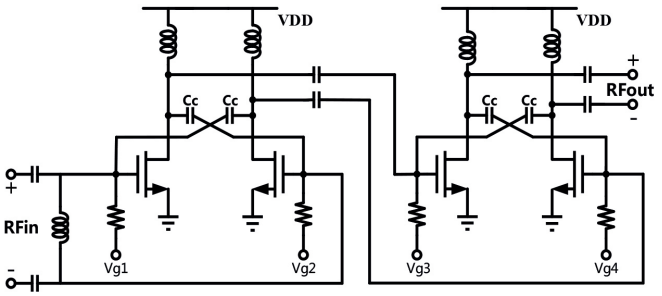

Figure 7: Two-stage capacitive cross-coupling PA

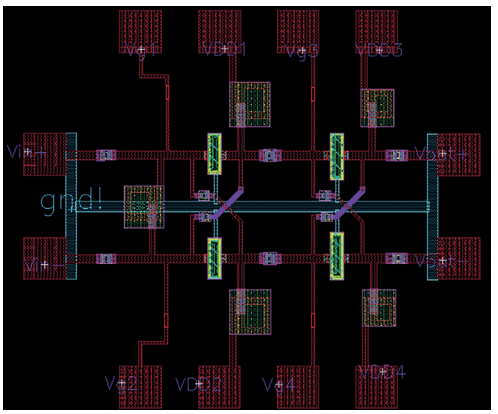

Figure 8: Layout of the PA chip

From Equations 2, 6 and 7 it can be seen that when cross-coupling neutralises the capacitance C_c and the transistor grid leakage capacitance C_{gd} becomes equal to it, reverse isolation is best and gain is largest. Therefore, the cross-coupling capacitance C_c should be equal to the transistor grid leakage capacitance C_{gd}.

Figures 4 and 5 show comparisons of the gains G_{mag}, G_{msg} and reverse isolation S_{12} at different frequencies. At 60GHz, the gain is about 6_{dB} and the reverse isolation is improved from -15dB to -40dB.

Power Amplifier Design

The 60GHz PA consists of two pairs of common-source pseudo-difference pairs. PAs are usually designed either with a common-source or cascode structure. In the common-source structure, the Miller capacitance (C_{gd}) is the main cause of gain, reverse isolation and stability degradation, therefore the coherent topology is conditionally stable. At high frequency the stability can be improved with the cascode structure, but there are significant disadvantages of low voltage difference and leakage current.

In our work, the Miller capacitance of the common topology is compensated by the cross-connection of the differential transistor, and by the gate connected directly to the neutral capacitance. Compared with the cascode structure, the common-source structure has a larger output swing. The neutralised capacitance is a MOS transistor, which acts as a capacitance terminal and whose drain and source are connected together as another capacitance terminal. The value of cross-capacitance C_c is determined by adjusting the size of the MOS transistor, and the MOS capacitance-based neutralisation capacitance matches the Miller capacitance of the normal source amplifier, which is less sensitive to changes in PVT (pressure-volume-temperature). In this way, the Miller effect is compensated to ensure stability and increase power gain.

In the 60GHz band, the inductance value required is relatively small, between 50pH and 200pH. The transmission line structure is usually implemented in mm-wave circuits to achieve small inductance. However, using a spiral inductor can improve the quality factor Q and, with respect to the

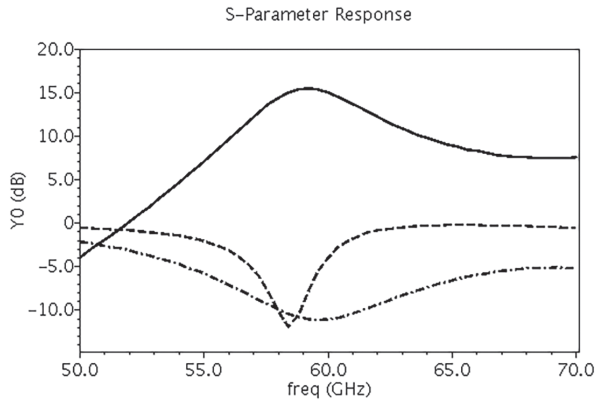

Figure 9: The PA's S-parameter simulation results

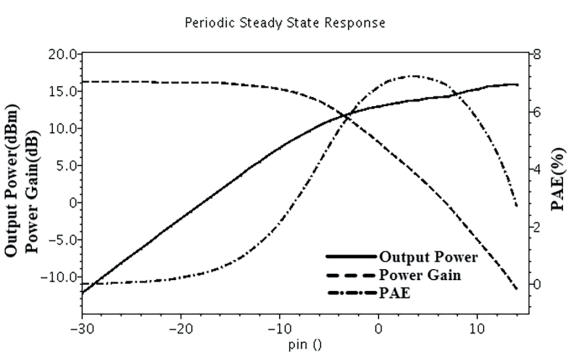

Figure 10: Large signal simulation results for the gain, output power and PAE

transmission line, also greatly reduce the passive device area.

In our project we used top metal (metal_9) for our spiral inductors with small inductance. The inductance model for the PA circuit is shown in Figure 6. The inner diameter is 25μm, the line width is 6μm, the equivalent inductance is 90pH and the quality factor is 21.

The overall structure of the two-stage power amplifier is shown in Figure 7. The output matching network, which consists of a large signal load pull, can get higher output power and better efficiency. The drain inductance and blocking resistance of the transistor are connected to the supply voltage and the bias voltage, respectively. The input, output and inter-stage matching networks are constituted of these inductors and series capacitances. The maximum oscillation frequency (f_{max}) of the transistor is main indicator of the performance of the mm-band transistor, when the transistor current density f_{max} is 0.2mA/um. Current density of the secondary transistor is biased to 0.28mA/um to obtain sufficient linearity.

The larger the transistor, the greater the output power; but, on the other hand, the greater the parasitic effect and substrate coupling loss, the greater the degradation of the PA.

A multi-stage PA with a transistor fork width of 2um achieves maximum gain, therefore the bias voltages of the circuit is 0.8V and 0.85V. The size of the transistor in the first stage is 2um×40/0.1um, and in the second stage 2um×48/0.1um.

Simulation Results

The proposed PA is designed in SMIC 90nm RF-CMOS process with two top-metal options. The chip is 450um×400um large, including pads, as shown in Figure 8.

The input port of the circuit is matched to 50Ω, and the output terminal adopts load-pull of 27Ω to achieve maximal output power. The geometric parameters of the spiral inductors used in the layout are given by the EM simulator (HFSS 13.0). The capacitance is the metal-insulator-metal (MIM) capacitance with density of 1fF/um².

The power supply is 1.2V, and the partial voltage V_g is 0.8V at all levels. The S-parameters (S_{11}, S_{22} and S_{21}) of the two-stage capacitive cross-coupling power amplifier are shown in Figure 9; S_{21} is 15.1dB. The 3dB bandwidth is more than 5GHz (56.9GHz-62.1GHz).

The PA is stable in the desired frequency band of 60GHz. Figures 10 and 11 show the variation of the large signal performance with increasing input power at the operating frequency of 60GHz.

The experimental results show that the power gain is over 15dB and that the gain curve is flat. Output power at the 1dB compression point ($OP1_{dB}$) is 9.1dBm, saturation output power (P_{sat}) is 13.9dBm, and peak power added efficiency (PAE) is 7.3%. ●

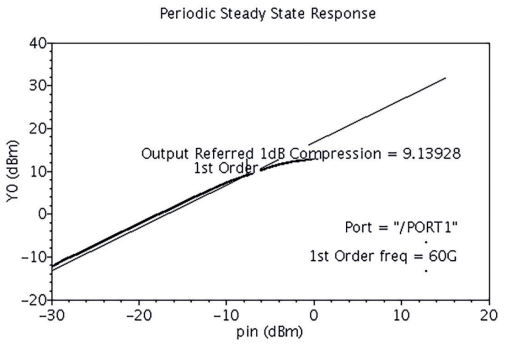

Figure 11: Large signal simulation results for the gain, output power and PAE

ROHDE & SCHWARZ PRESENTS NEW HIGH-PERFORMANCE OSCILLOSCOPE

Rohde & Schwarz launched the R&S RTP high-performance oscilloscope family that combines signal integrity with a high acquisition rate. In standard acquisition mode, it can measure a million waveforms per second, making it more than a thousand times faster than other oscilloscopes in its class, picking up sporadic errors faster.

The R&S RTP combines various instruments, making it particularly suitable for debugging, e.g. embedded components with fast digital or wideband RF interfaces. The R&S RTP is available as a 4GHz, 6GHz or 8GHz model, with higher bandwidth models expected in 2019.

The R&S RTP compensates transmission losses from the signal source to the oscilloscope, so-called de-embedding, in real time. The advantage is that the oscilloscope is still extremely fast even with signal correction activated. A time-saving feature is its hardware acceleration for a range of analysis functions.

www.rohde-schwarz.com/rtp

LATEST XR-DIMM FROM APACER

As applications of memory in high vibration and shock environments are becoming more diverse, Apacer launches its latest XR-DIMM (eXtreme Rugged Dual Inline Memory Module), showcasing incomparable reliability and flexibility space usage in the memory industry. Following its success in the automotive systems market, Apacer is expanding its business into high-end niche market of industrial applications, such as transportation, defence and aerospace, and intelligent logistics, where superior anti-shock and anti-vibration abilities are required.

Apacer's XR-DIMM uses the innovative board-to-board connector design to fit tightly and securely onto the motherboard. In addition, it adopts the highly durable 300-pin connector and mounting holes to effectively prevent memory modules from dislocating or coming away due to vibration or strong impact. This greatly improves the reliability of memory signal transmissions, serving as the strongest support for applications working under severe environments.

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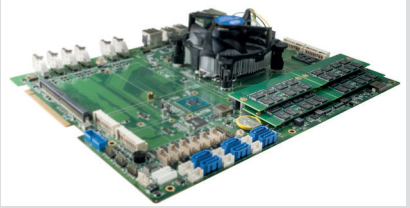

RIGOL LAUNCHES NEW HIGH-PERFORMANCE OSCILLOSCOPE FAMILY

Rigol Technologies has introduced four new high-end oscilloscopes with a large 10.1" touch-colour display.

The MSO/DS7000 is a versatile mixed-signal high-performance oscilloscope that incorporates many of the latest Rigol own-designed ChipSet ASIC technology and integrated processes. With bandwidths of 100-500MHz (bandwidth upgrade), sample rates up to 10GS/s and with four analogue and 16 digital channels, the MSO/DS7000 series is perfectly suited to many application areas, including research and development, universities and schools, production and quality control as well as the communications, automotive, aerospace, industrial and power electronics sectors among others.

All models provide a large 10.1" touch-colour display for better and clear signal representation and for optimal display of additional information, such as cursor positions and their coordinates, mathematical parameters and more. Memory depth is up to 500 million points.

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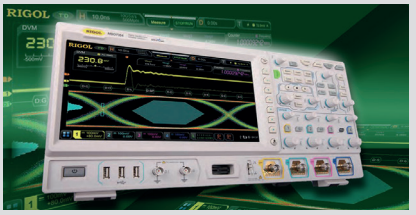

ALLEGRO MICROSYSTEMS SHIPS ITS BILLIONTH GEAR TOOTH SENSOR IC

Allegro MicroSystems is celebrating a milestone for its Gear Tooth Sensor (GTS) ICs, which surpassed one billion total units shipped. These revolutionary ICs were first released to market over 15 years ago, and are staples in engine management, transmission and braking applications in advanced vehicles.

Allegro's GTS product line was the first fully-integrated sensor of its kind on the market. These unique ICs use custom, high-volume and high-accuracy semiconductor-grade equipment to combine a magnetic sensor IC with an Allegro-patented magnet, all within a small 10mm diameter package. This innovative packaging technology, when combined with subsequent Allegro circuit design and algorithm advancements, enhances automotive engine and transmission performance, vehicle fuel economy and emissions, as well as overall vehicle performance.

Each year Allegro delivers nearly 900 million magnetic sensors, with GTS sensors accounting for over 100 million units.

www.allegromicro.com

MICROCHIP RELEASES 32-BIT MCUS WITH CHIP-LEVEL SECURITY

Microchip announced two new families of 32-bit microcontrollers (MCUs), SAM10 and SAM L11, to meet the growing need for security in Internet of Things (IoT) endpoints.

The devices are based on the Arm Cortex-M23 core, with the SAM L11 featuring Arm TrustZone for Armv8-M, a programmable environment that provides hardware isolation between certified libraries, IP and application code. There's also chip-level tamper resistance, secure boot and secure key storage which, when combined with TrustZone technology, protect applications from remote and physical attacks.

In addition to TrustZone technology, the SAM L11 security features include an on-board cryptographic module supporting Advanced Encryption Standard (AES), Galois Counter Mode (GCM) and Secure Hash Algorithm (SHA). The secure boot and secure key storage with tamper detection capabilities establish a hardware root of trust and bootloader for secure firmware upgrades.

www.microchip.com

HP RENEWS COMMITMENT TO PLANET, PEOPLE AND COMMUNITY

HP released in the UK its 2017 Sustainable Impact Report, documenting annual progress and outlining new efforts to drive lasting improvements to the planet, people and communities where the company operates.

HP set ambitious GHG emissions reduction goals across its value chain – operations, products and supply chain. In 2017, HP's Scope 1, 2 and 3 goals were validated by the Science Based Targets initiative (SBTi). Since 2015, the company has decreased its Scope 1 and Scope 2 GHG emissions from global operations by 35% compared to 2015, exceeding its 2025 goal of a 25% reduction. The reductions came through a combination of energy efficiency efforts, and purchase of renewable energy and renewable energy certificates (RECs) in the US. In 2017, HP reached its goal to use 40% renewable electricity in its global operations.

It is also adopting a more efficient low-carbon economy and workforce well-being, as well as delivering more inclusive, equitable, tech-enabled learning.

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